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# United States Patent [19]

**Yamauchi**

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 [45] **Date of Patent:** **May 16, 2000**

[54] **INTERNAL VOLTAGE GENERATION  
CIRCUIT HAVING RING OSCILLATOR  
WHOSE FREQUENCY CHANGES  
INVERSELY WITH POWER SUPPLY  
VOLTAGE**

5,391,979 2/1995 Kajimoto et al. .... 323/313  
 5,394,372 2/1995 Tanaka et al. .... 365/226  
 5,557,193 9/1996 Kajimoto .... 323/282  
 5,689,460 11/1997 Ooishi .... 327/530

## FOREIGN PATENT DOCUMENTS

7-129265 5/1995 Japan .

## OTHER PUBLICATIONS

Horiguchi, Masashi et al., "A Tunable CMOS-DRAM Voltage Limiter with Stabilized Feedback Amplifier", *IEEE Journal of Solid-State Circuits*, vol. 25, No. 5, Oct. 1990, pp. 1129-1134.

*Primary Examiner*—Siegfried H. Grimm  
*Attorney, Agent, or Firm*—McDermott, Will & Emery

[75] **Inventor:** Tadaaki Yamauchi, Hyogo, Japan  
 [73] **Assignee:** Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan  
 [21] **Appl. No.:** 09/318,240  
 [22] **Filed:** May 25, 1999

## Related U.S. Application Data

[62] Division of application No. 08/780,909, Jan. 9, 1997, Pat. No. 5,982,162.

## Foreign Application Priority Data

Apr. 22, 1996 [JP] Japan ..... 8-100055

[51] **Int. Cl.<sup>7</sup>** ..... H03L 7/00; G05F 3/16  
 [52] **U.S. Cl.** ..... 331/57; 327/534; 331/177 R  
 [58] **Field of Search** ..... 331/57, 177 R;  
 327/534, 535, 536, 537

## References Cited

### U.S. PATENT DOCUMENTS

5,097,198 3/1992 Holmdahl ..... 323/280

## [57] ABSTRACT

An internal voltage generation circuit down converts an external power supply voltage on the basis of a reference voltage. An oscillator outputs a pulse voltage according to a power supply voltage. A pump circuit generates the internal voltage according to the pulse voltage. A control circuit for the oscillator may include a current mirror amplifier so that when the power supply voltage is reduced the frequency of the pulse voltage becomes higher a corresponding amount and when the power supply voltage is increased the frequency of the pulse voltage becomes lower a corresponding amount.

**6 Claims, 7 Drawing Sheets**

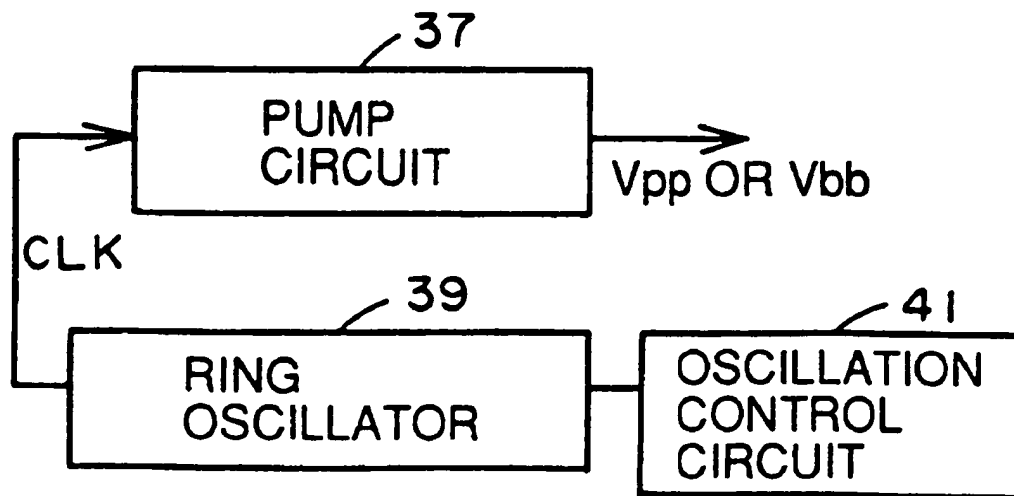


FIG. 1

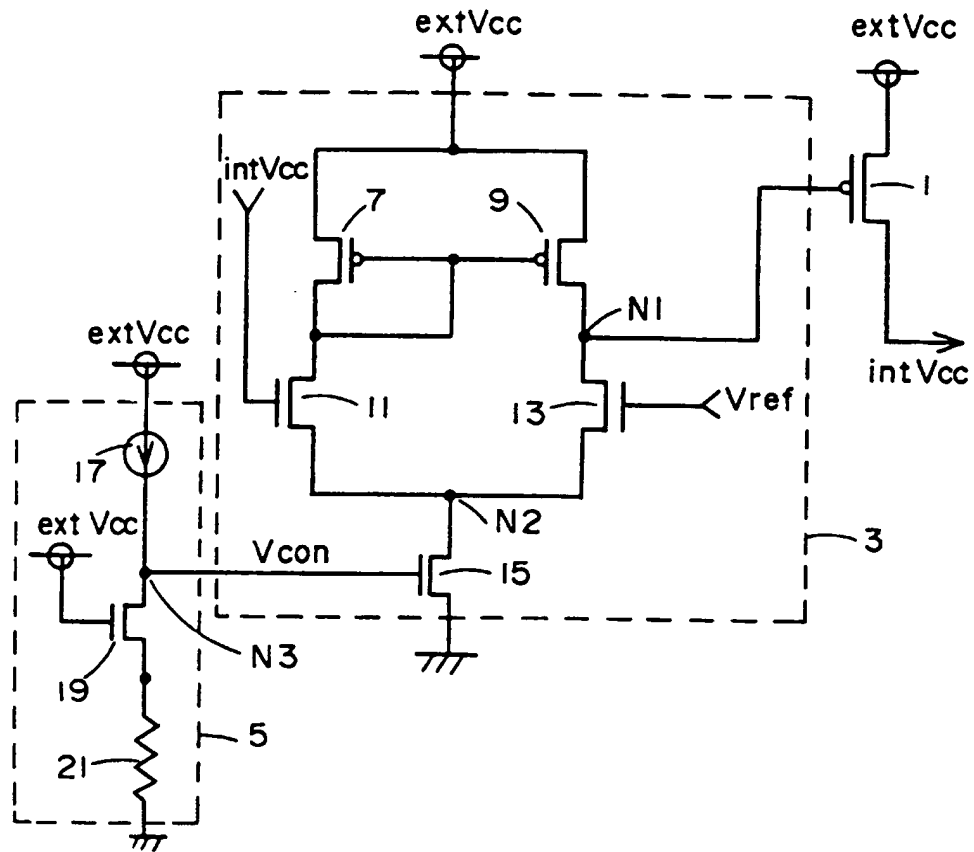


FIG. 2

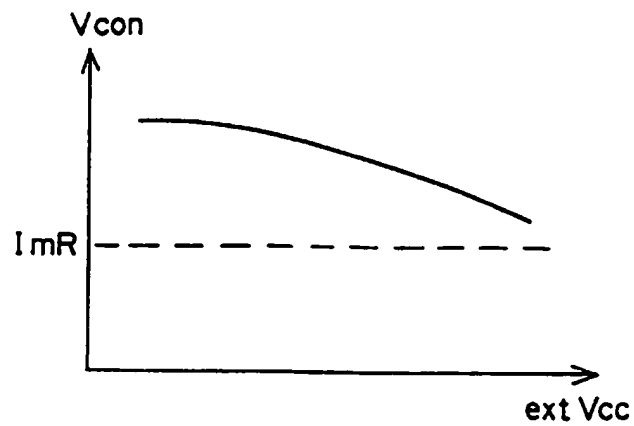




FIG. 3

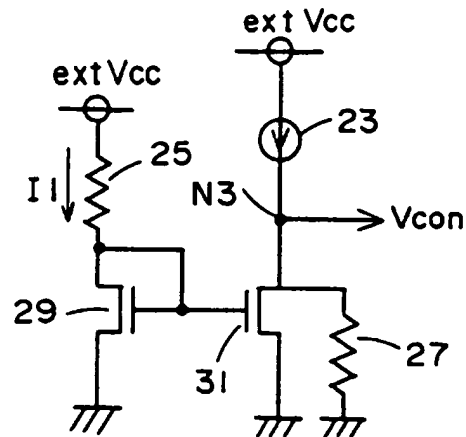


FIG. 4

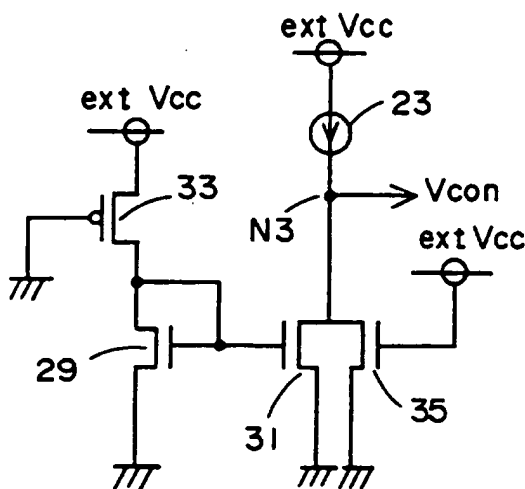
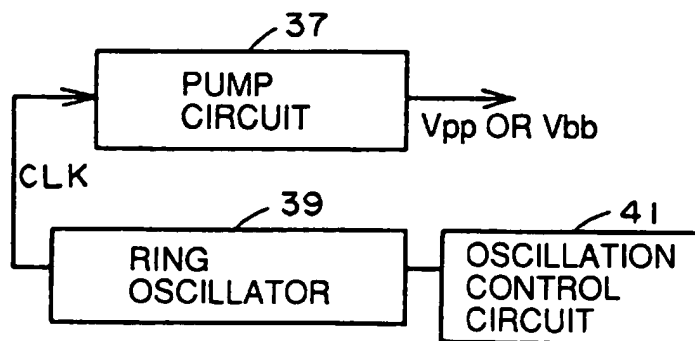
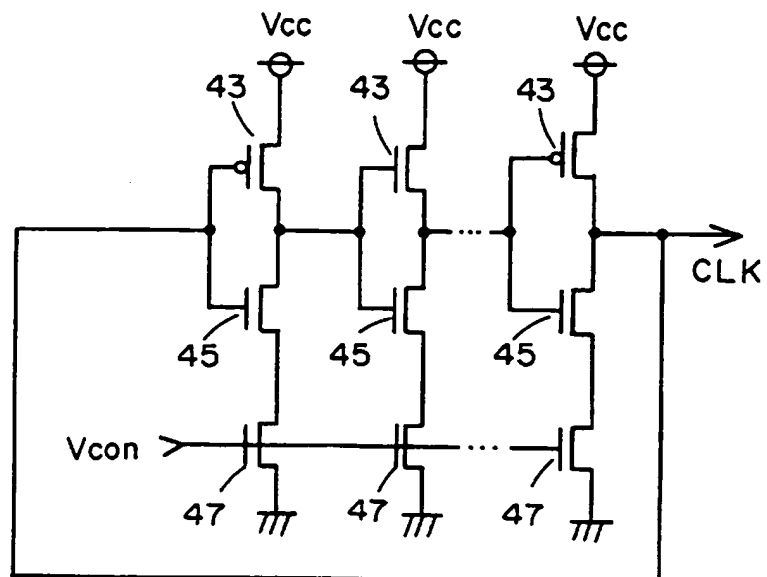


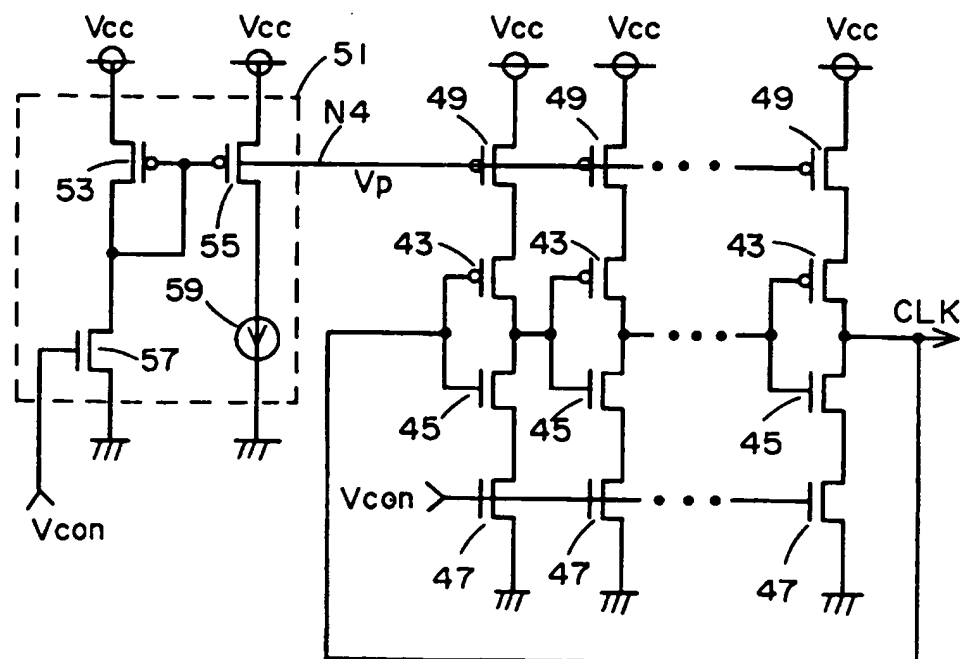
FIG. 5



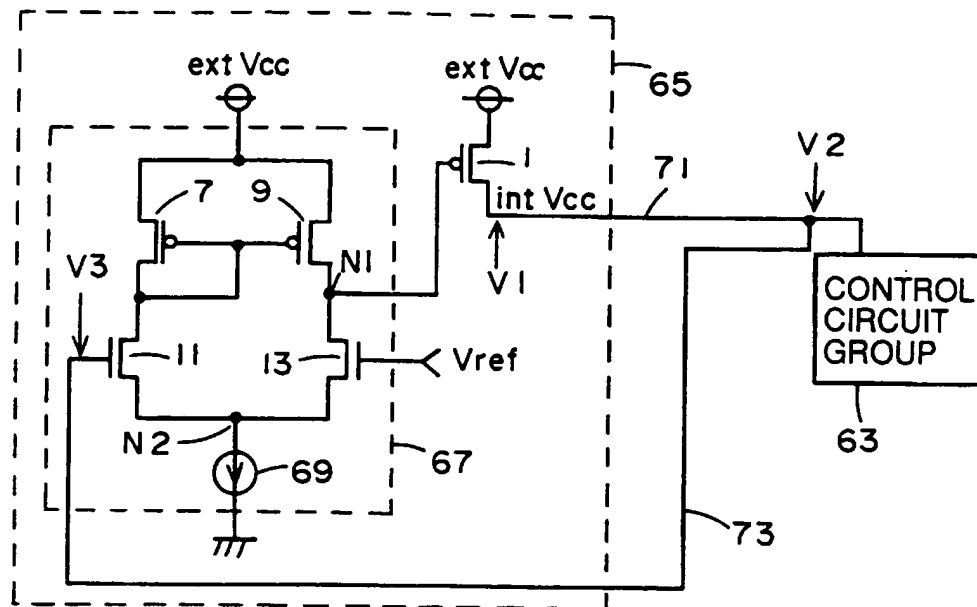
**FIG.6**



**FIG. 7**



**FIG.8**



**FIG.9**

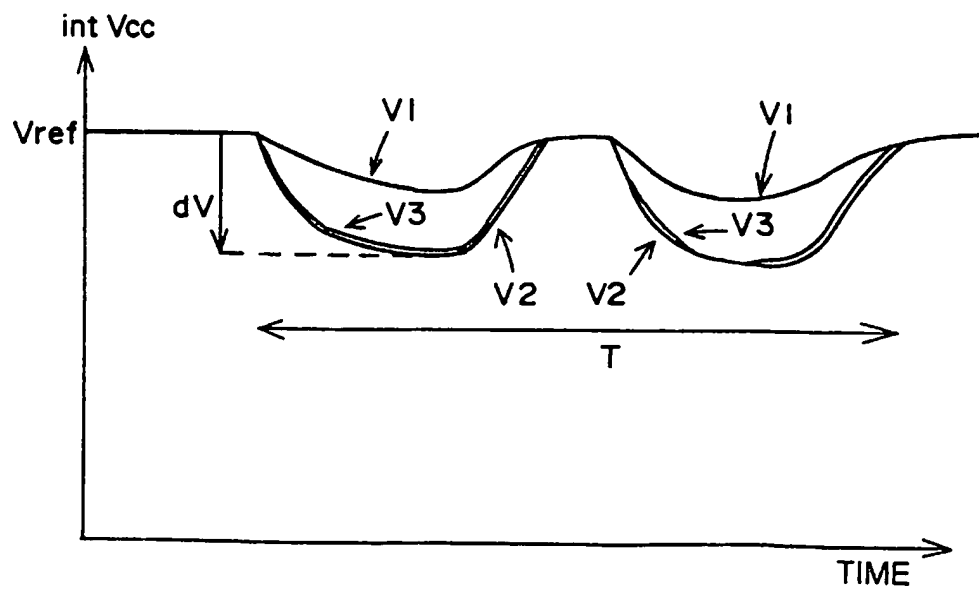


FIG. 10

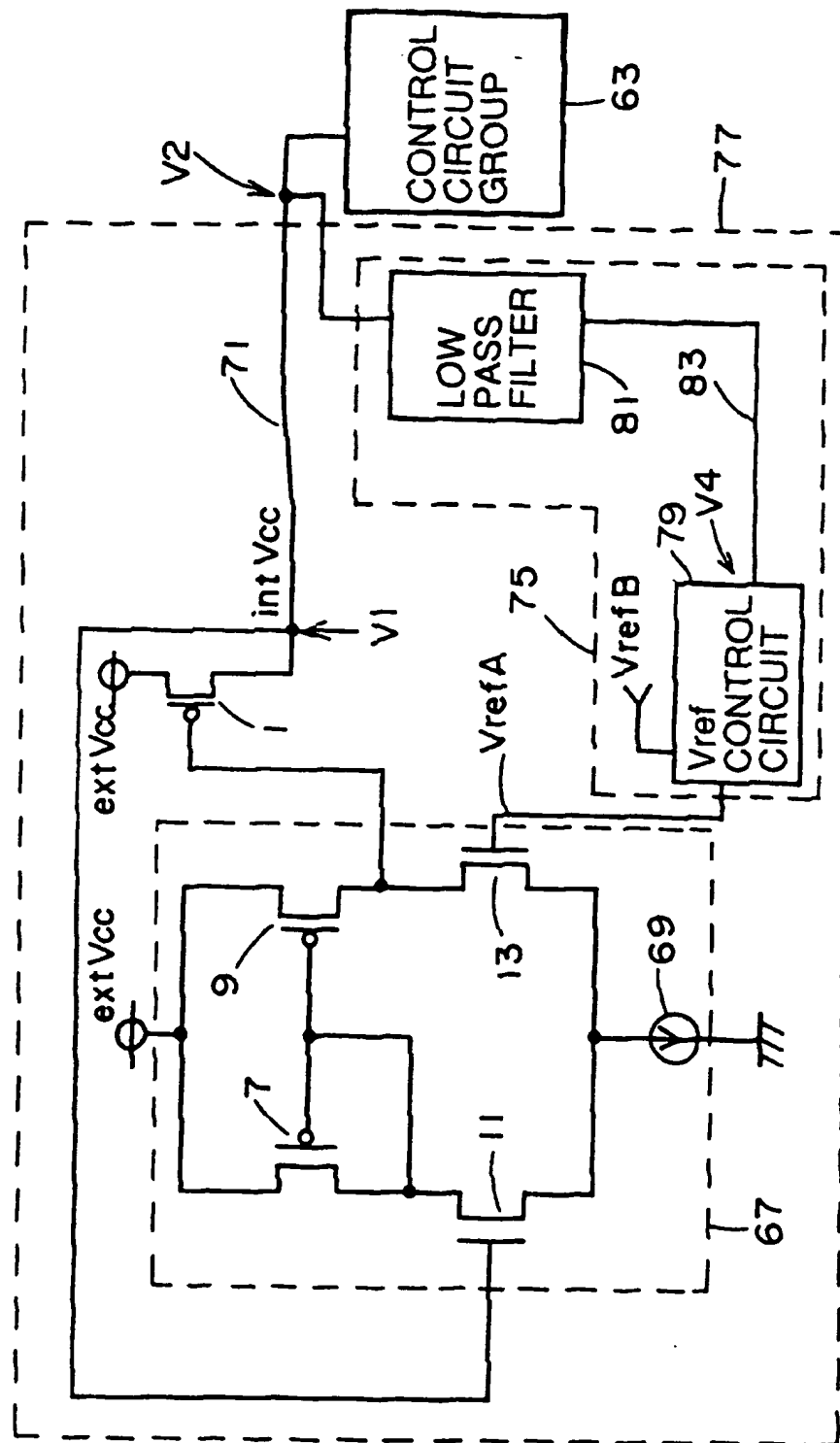


FIG. 11

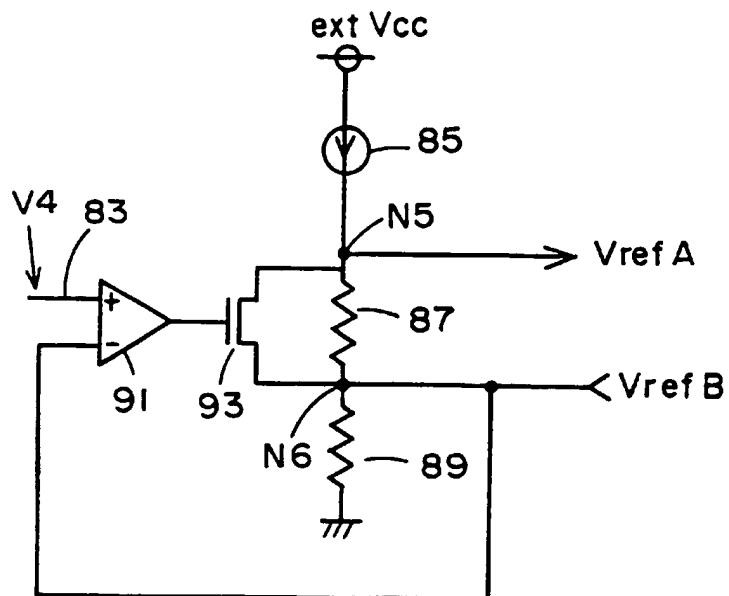


FIG. 12

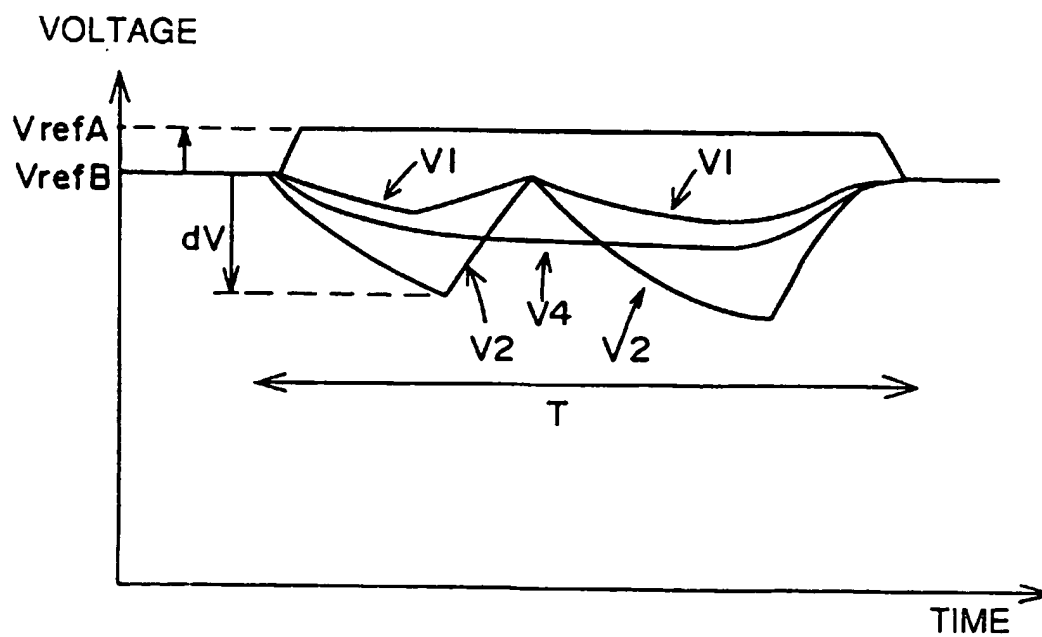


FIG. 13 PRIOR ART

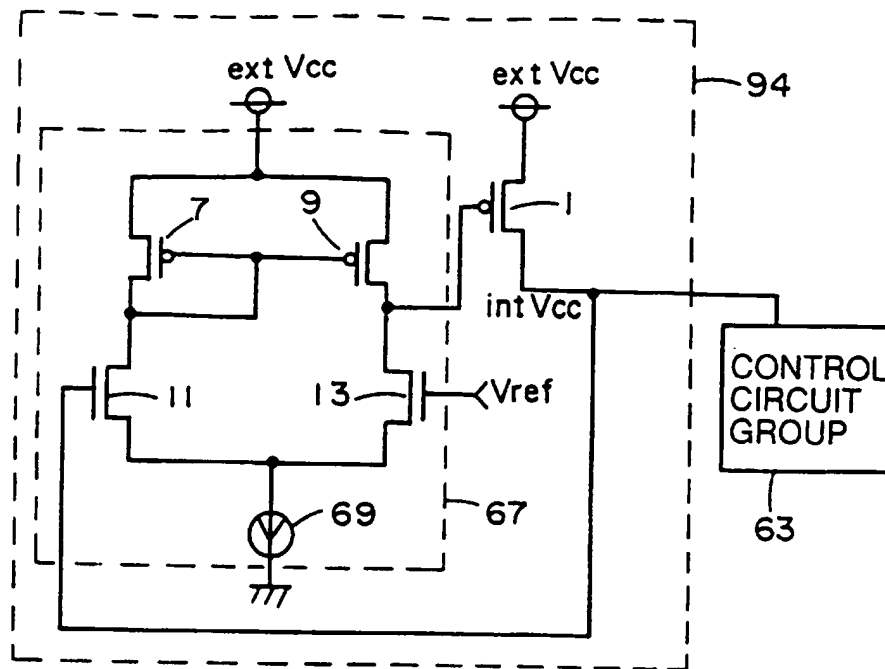
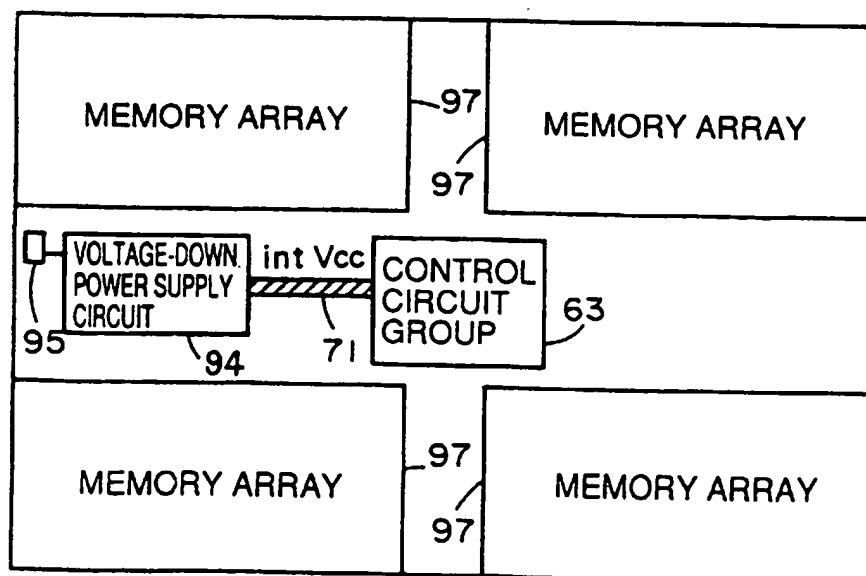


FIG. 14 PRIOR ART



# INTERNAL VOLTAGE GENERATION CIRCUIT HAVING RING OSCILLATOR WHOSE FREQUENCY CHANGES INVERSELY WITH POWER SUPPLY VOLTAGE

This application is a divisional of application Ser. No. 08/780,909 filed Jan. 9, 1997 and now U.S. Pat. No. 5,982,162.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to internal power supply voltage generation circuits, internal voltage generation circuits, and semiconductor devices, and more particularly, to an internal power supply voltage generation circuit immune to variation in external power supply voltage and temperature, an internal voltage generation circuit immune to variation in power supply voltage, and a semiconductor device immune to variation in internal power supply voltage.

### 2. Description of the Background Art

FIG. 13 is a circuit diagram showing in detail an internal voltage-down power supply circuit as a conventional internal power supply voltage generation circuit.

Referring to FIG. 13, an internal voltage-down power supply circuit 94 generates and supplies to a control circuit group 63 an internal power supply voltage intVcc. Control circuit group 63 includes a plurality of control circuits which operate according to internal power supply voltage intVcc. Internal voltage-down power supply circuit 94 includes a comparator circuit 67 and a voltage-down circuit 1. Voltage-down circuit 1 is formed of a PMOS transistor. Comparator circuit 67 is formed of a current mirror type amplify circuit. Comparator circuit 67 includes PMOS transistors 7 and 9, NMOS transistors 11 and 13, and a constant current source 69.

An output voltage from comparator circuit 67 is applied to the gate of PMOS transistor 1. PMOS transistor 1 down-converts an external power supply voltage extVcc according to the level of the output voltage to generate internal power supply voltage intVcc. A reference voltage Vref is applied to the gate of NMOS transistor 13 of comparator circuit 67. Internal power supply voltage intVcc generated from PMOS transistor 1 is applied to the gate of NMOS transistor 11 of comparator circuit 67. Therefore, comparator circuit 67 provides a voltage to the gate of MOS transistor 1 so that the level of internal power supply voltage intVcc is equal to the level of reference voltage Vref.

FIG. 14 is a schematic block diagram of a conventional semiconductor device. Components corresponding to those of FIG. 13 have the same reference characters allotted, and their description will not be repeated.

Referring to FIG. 14, a conventional semiconductor device includes four memory arrays 97, and external power supply pad 95, an internal voltage-down power supply circuit 94, a power line 71, and a control circuit group 63. Memory array 97 includes a plurality of memory cells to store data. Internal voltage-down power supply circuit 94 is located in the proximity of external power supply pad 95 provided at the end of the chip. External power supply pad 95 serves to supply external power supply voltage extVcc to internal voltage-down power supply circuit 94. Power line 71 serves to supply internal power supply voltage intVcc generated from internal voltage-down power supply circuit 94 to control circuit group 63.

As described above, a conventional internal voltage-down power supply circuit forms a closed loop in which the output which is internal power supply voltage intVcc is applied to comparator circuit 67. When external power supply voltage extVcc is shifted to a greater value, or when the temperature during the operation of internal voltage-down power supply circuit 94 is low, the channel conductance of the transistors forming internal voltage-down power supply circuit 94 becomes greater to increase the voltage gain of comparator circuit 67 and voltage-down power supply circuit 1. This induces the problem that internal power supply voltage intVcc is easily oscillated unnecessarily which is the output of internal voltage-down power supply circuit 94.

As described above, a conventional semiconductor device has internal voltage-down power supply circuit 94 provided at the end of the chip. If control circuit group 63 that operates according to internal power supply voltage intVcc is arranged remote from internal voltage-down power supply circuit 94, the resistance of power line 71 is increased. This causes the level of internal power supply voltage intVcc in the proximity of control circuit group 63 to become lower than the level of internal power supply voltage intVcc in the proximity of internal voltage-down power supply circuit 94 by the parasitic resistance of power line 71 when the power consumption of control circuit group 63 is increased. It is to be noted that internal voltage-down power supply circuit 94 generates internal power supply voltage intVcc by feeding back internal power supply voltage intVcc in the proximity of internal voltage-down power supply circuit 94. There was a problem that internal voltage-down power supply circuit 94 does not easily follow the variation of internal power supply voltage intVcc in the proximity of control circuit group 63.

## SUMMARY OF THE INVENTION

In view of the foregoing, an object of the present invention is to provide an internal power supply voltage generation circuit that does not have an internal power supply voltage intVcc unnecessarily oscillated in response to variation in an external power supply voltage extVcc and temperature.

Another object of the present invention is to provide a semiconductor device including an internal power supply voltage generation circuit that can generate internal power supply voltage intVcc in response to variation in internal power supply voltage intVcc in the proximity of a control circuit group even when the internal power supply voltage generation circuit and the control circuit group are remote from each other. More specifically, the another object of the present invention is to provide a semiconductor device including an internal power supply voltage generation circuit that has superior followability to variation of internal power supply voltage intVcc in the proximity of a control circuit group.

A further object of the present invention is to provide an internal voltage generation circuits that has increase of the time for internal voltage to attain a predetermined voltage level suppressed even when power supply voltage is reduced.

According to a first aspect of the present invention, an internal power supply voltage generation circuit generates an internal power supply voltage. The internal power supply voltage generation circuit includes a current mirror amplify circuit, a voltage-down circuit, and a current source control circuit. The current mirror amplify circuit includes a current source. The current mirror amplify circuit is a comparator

circuit for comparing a reference voltage with an internal power supply voltage. The voltage-down circuit down-converts an external power supply voltage for generating an internal power supply voltage according to the comparison result of the current mirror amplify circuit. The current source control circuit controls the current source so that the current from the current source is reduced according to increase, if any, of the external power supply voltage, and increased according to decrease, if any, of the external power supply voltage.

In the internal power supply voltage generation circuit of the first aspect, control is provided so that, when the external power supply voltage becomes higher, the current from the current source of the current mirror amplify circuit is decreased according to increase of the external power supply voltage. Therefore, increase of the closed loop gain of the internal power supply voltage generation circuit can be suppressed even when the external power supply voltage is altered to a higher value. Therefore, unnecessary oscillation of the internal power supply voltage can be prevented.

According to a second aspect of the present invention, an internal power supply voltage generation circuit generates an internal power supply voltage. The internal power supply voltage generation circuit includes a current mirror amplify circuit, a voltage-down circuit, and a current source control circuit. The current mirror amplify circuit includes a current source. The current mirror amplify circuit includes a comparator circuit for comparing a reference voltage with an internal voltage. The voltage-down circuit down-converts an external power supply voltage to generate an internal power supply voltage according to the comparison result of the current mirror amplify circuit. The current source control means controls the current source so that the current from the current source is increased according to increase, if any, of the temperature, and reduced according to decrease, if any, of the temperature.

In the internal power supply voltage generation circuit of the second aspect of the present invention, control is provided so that, when the temperature becomes lower, the current from the current source of the current mirror amplify circuit is reduced according to reduction in the temperature. Therefore, increase of the closed loop gain of the internal power supply voltage generation circuit can be suppressed even when the temperature during operation is low. Thus, unrequired oscillation of the internal power supply voltage can be prevented.

According to a third aspect of the present invention, an internal power voltage generation circuit includes an oscillation circuit, a pump circuit, and an oscillation control circuit. The oscillation circuit oscillates a pulse voltage on the basis of a power supply voltage. The pump circuit generates an internal voltage according to the pulse voltage. The oscillation control circuit controls the oscillation circuit so that the frequency of the pulse voltage becomes higher according to reduction, if any, of the power supply voltage. The oscillation control circuit controls the oscillation circuit so that the frequency of the pulse voltage becomes lower according to increase, if any, of the power supply voltage.

In the internal voltage generation circuit of the third aspect, control is provided so that the frequency of the pulse voltage for driving the pump circuit becomes higher according to decrease, if any, of the power supply voltage. Therefore, sufficient level of pumping can be obtained even when the power supply voltage is lowered. Increase in the time required for the internal voltage to attain a predetermined voltage level can be suppressed.

According to a fourth aspect of the present invention, a semiconductor device includes an internal circuit, an internal power supply voltage generation circuit, a power line, and a conductor line. The internal power supply voltage generation circuit generates an internal power supply voltage. The power line supplies an internal power supply voltage to the internal circuit. The conductor line is connected to the power line in the proximity of the internal circuit, and is not connected to the power line except at the proximity of the internal circuit. The internal power supply voltage generation circuit compares a reference voltage with an internal power supply voltage in the proximity of the internal circuit to generate an internal power supply voltage according to the comparison result. The internal power supply voltage in the proximity of the internal circuit is transmitted to the internal power supply voltage generation circuit by the conductor line.

According to a fifth aspect of the present invention, a semiconductor device includes an internal circuit, and an internal power supply voltage generation circuit. The internal power supply voltage generation circuit generates an internal power supply voltage that is supplied to the internal circuit. The internal power supply voltage generation circuit generates an internal power supply voltage according to the comparison results of a reference voltage and an internal power supply voltage. The internal power supply voltage generation circuit includes a reference voltage generation circuit. The reference voltage generation circuit alters the reference voltage according to the internal power supply voltage in the proximity of the internal circuit.

According to the semiconductor devices of the fourth and fifth aspects of the present invention, an internal power supply voltage can be generated accommodating change in the internal power supply voltage in the proximity of the internal circuit. Therefore, followability can be improved with respect to the variation in the internal power supply voltage at the proximity of the internal circuit.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing in detail an internal voltage-down power supply circuit as an internal power supply voltage generation circuit according to a first embodiment of the present invention.

FIG. 2 is a diagram for describing an operation of the internal voltage-down power supply circuit of FIG. 1.

FIG. 3 is a circuit diagram showing in detail a current source control circuit used in an internal voltage-down power supply circuit as an internal power supply voltage generation circuit according to a second embodiment of the present invention.

FIG. 4 is a circuit diagram showing another example of a current source control circuit used in an internal voltage-down power supply circuit as an internal power supply voltage generation circuit according to the second embodiment of the present invention.

FIG. 5 is a schematic block diagram showing an internal voltage generation circuit according to a third embodiment of the present invention.

FIGS. 6 and 7 are circuit diagrams showing examples of a ring oscillator of FIG. 5.



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FIG. 8 is a circuit diagram showing a semiconductor device according to a fourth embodiment of the present invention, particularly an internal voltage-down power supply circuit thereof.

FIG. 9 is a diagram for describing an operation of the internal voltage-down power supply circuit of FIG. 8.

FIG. 10 is a circuit diagram of a semiconductor device according to a fifth embodiment of the present invention, particularly an internal voltage-down power supply circuit thereof.

FIG. 11 is a circuit diagram showing in detail a Vref control circuit of FIG. 10.

FIG. 12 is a diagram for describing an operation of the internal voltage-down power supply circuit of FIG. 10.

FIG. 13 is a circuit diagram showing in detail a conventional internal voltage-down power supply circuit.

FIG. 14 is a schematic block diagram of a conventional semiconductor device.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

An internal power supply voltage generation circuit, an internal voltage generation circuit, and a semiconductor device according to the present invention will be described hereinafter with reference to the drawings.

##### First Embodiment

Referring to FIG. 1, an internal voltage-down power supply circuit as an internal power supply voltage generation circuit of the first embodiment includes a voltage-down circuit 1, a comparator circuit 3, and a current source control circuit 5. Comparator circuit 3 includes PMOS transistors 7 and 9, NMOS transistors 11 and 13, and a current source 15. Current source control circuit 5 includes a constant current source 17, an NMOS transistor 19, and a resistance element 21.

Voltage-down circuit 1 is formed of an PMOS transistor. Comparator circuit 3 is formed of a current mirror type amplify circuit. An output node N1 of comparator circuit 3 is connected to the gate of PMOS transistor 1.

The connection of the elements forming comparator circuit 3 will be described hereinafter. PMOS transistor 7 and NMOS transistor 11 are connected in series between a node having external power supply voltage extVcc and a node N2. The gate of NMOS transistor 11 receives internal power supply voltage intVcc generated by PMOS transistor 1. PMOS transistor 9 and NMOS transistor 13 are connected in series between a node having external power supply voltage extVcc and node N2. The gate of NMOS transistor 13 receives a reference voltage Vref. PMOS transistors 7 and 9 have their gates connected to the drain of NMOS transistor 11. Current source 15 is connected between node N2 and a node having ground voltage. Current source 15 is formed of an NMOS transistor. NMOS transistor 15 has its gate connected to an output node N3 of current source control circuit 5.

The elements forming current source control circuit 5 will be described hereinafter. A constant current source 17 is connected between the node having external power supply voltage extVcc and output node N3. NMOS transistor 19 and resistance element 21 are connected in series between node N3 and the node having ground voltage. External power supply voltage extVcc is applied to the gate of NMOS transistor 19.

The operation will be described hereinafter. PMOS transistor 1 responds to a voltage provided from output node N1

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of comparator circuit 3 to down-convert external power supply voltage extVcc for generating an internal power supply voltage intVcc. When internal power supply voltage intVcc is smaller than reference voltage Vref, comparator circuit 3 provides a voltage of an L level (logical low) from output node N1 to the gate of PMOS transistor 1. In response, the channel conductance of PMOS transistor 1 becomes greater. This causes the level of internal power supply voltage intVcc to be increased. When internal power supply voltage intVcc becomes as high as the level of reference voltage Vref, comparator circuit 3 provides a voltage of an H level (logical high) from output node N1 to the gate of PMOS transistor 1. In response, PMOS transistor 1 is turned off. As a result, internal power supply voltage intVcc will become stable at the level equal to reference voltage Vref.

It is assumed that the current generated by constant current source 17 is Im, the channel resistance of NMOS transistor 19 is Rg, and the resistance of resistance element 21 is R. In this case, the voltage of node N3 is  $I_m(R+R_g)$ . When the gate-source voltage ( $V_{gs}=extVcc-I_m R$ ) of NMOS transistor 19 is increased, Rg becomes smaller. Therefore, the voltage of node N3 is reduced in proportion to increase of external power supply voltage extVcc. More specifically, when external power supply voltage extVcc rises, current source control circuit 5 provides a control voltage Vcon that is reduced according to the increase from output node N3 to the gate of NMOS transistor 15. Therefore, the current flowing towards NMOS transistor 15 is reduced. This causes the voltage gain of comparator circuit (current mirror type amplify circuit) 3 to become smaller. In the case of decrease in external power supply voltage extVcc, current source control circuit 5 provides a control voltage Vcon that is increased according to the decrease to the gate of NMOS transistor 15 from output node N3. In response, the current flowing to NMOS transistor 15 is increased, so that the voltage gain of comparator circuit (current mirror type amplify circuit) 3 is also increased. Thus, the voltage gain of comparator circuit (current mirror type amplify circuit) 3 becomes smaller as external power supply voltage extVcc becomes greater. When external power supply voltage extVcc becomes smaller and the gain voltage of comparator circuit (current mirror type amplify circuit) 3 increases, it is said that the voltage gain of comparator circuit (current mirror type amplify circuit) 3 has a negative dependence on external power supply voltage extVcc. As described above, NMOS transistor 19 is used as a resistance element.

FIG. 2 is a graph showing the relationship between external power supply voltage extVcc and control voltage Vcon. Control voltage Vcon is plotted along the ordinate, and external power supply voltage extVcc is plotted along the abscissa. It is appreciated from FIG. 2 that control voltage Vcon is reduced as external power supply voltage extVcc increases.

Thus, in the internal voltage-down power supply circuit of the first embodiment, the voltage gain of comparator circuit (current mirror type amplify circuit) 3 has a negative dependence on external power supply voltage extVcc. Therefore, increase in the closed loop gain of the internal voltage-down power supply circuit can be suppressed even when external power supply voltage extVcc is shifted to a higher level. Thus, unnecessary oscillation of internal power supply voltage intVcc can be prevented when external power supply voltage extVcc is shifted to a higher level.

In FIG. 1, resistance element 21 can be formed of a MOS transistor. In this case, resistance R of the MOS transistor

becomes larger as the temperature increases. In contrast, when the temperature becomes lower, resistance R becomes smaller. Therefore, by implementing resistance element 21 with a MOS transistor, the voltage of node N3 is reduced when the temperature becomes lower. More specifically, current source control circuit 5 provides from output node N3 a control voltage Vcon that becomes lower in response to a drop in temperature to the gate of NMOS transistor 15. As a result, the current flowing to NMOS transistor 15 becomes smaller, and the voltage gain of comparator circuit (current mirror type amplify circuit) 3 is reduced. In contrast, when the temperature is increased, the voltage of node N3 becomes higher. More specifically, current source control circuit 5 provides from output node N3 a control voltage Vcon that becomes higher in response to a rise in temperature to the gate of NMOS transistor 15. As a result, the current flowing to NMOS transistor 15 is increased, and the voltage gain of comparator circuit (current mirror type amplify circuit) 3 is also increased. When the voltage gain of comparator circuit (current mirror type amplify circuit) 3 becomes lower in response to reduction in temperature and becomes greater in response to increase in temperature, it is said that the voltage gain of comparator circuit (current mirror type amplify circuit) 3 has a positive dependence on the temperature.

According to a modification of the internal voltage-down power supply circuit of the first embodiment, the voltage gain of comparator circuit (current mirror type amplify circuit) 3 has a negative dependence and a positive dependence on external power supply voltage extVcc and temperature, respectively. Therefore, increase of the closed loop gain of the internal voltage-down power supply circuit can be suppressed even when external power supply voltage extVcc is altered to a higher level and the temperature during operation of the internal voltage-down circuit is low. Thus, unnecessary oscillation of internal power supply voltage intVcc can be prevented in the case where external power supply voltage extVcc is altered to a high level and the temperature during operation of the internal voltage-down power supply circuit is low.

#### Second Embodiment

The voltage-down circuit and comparator circuit (current mirror type amplify circuit) of an internal voltage-down power supply circuit as an internal power supply voltage generation circuit of a second embodiment of the present invention are similar to voltage-down circuit 1 and comparator circuit (current mirror type amplify circuit) 3 of the first embodiment shown in FIG. 1. The internal voltage-down power supply circuit of the second embodiment differs from the internal voltage-down power supply circuit of the first embodiment in a current source control circuit.

FIG. 3 is a circuit diagram showing the detail of a current source control circuit of an internal voltage-down power supply circuit of the second embodiment.

Referring to FIG. 3, the current source control circuit includes resistance elements 25 and 27, NMOS transistors 29 and 31, and a constant current source 23. Resistance element 25 and NMOS transistor 29 are connected in series between the node having external power supply voltage extVcc and the node having ground voltage. Constant current source 23 is connected between the node having external power supply voltage extVcc and output node N3. NMOS transistor 31 and resistance element 27 are connected in parallel between output node N3 and the node having ground voltage. NMOS transistors 29 and 31 have

their gates connected to resistance element 25. The current source control circuit of the above-described structure provided control voltage Vcon from output node N3 to the gate of NMOS transistor 15 of comparator circuit 3, as shown in FIG. 1. Control voltage Vcon is the voltage of output node N3.

It is assumed that the resistance values of resistance elements 25 and 27 are R1 and R2, respectively, the threshold voltage of NMOS transistor 29 is Vthn, the constant current generated from constant current source 23 is Iconst, and the current flowing to NMOS transistor 29 is I1. NMOS transistor 29 and NMOS transistor 31 form a current mirror circuit. Here, the ratio of the size of NMOS transistor 31 to NMOS transistor 29, i.e., the size of NMOS transistor 31/the size of NMOS transistor 29 is referred to as "k". This "k" is the so-called mirror ratio.

The current flowing through NMOS transistor 31 is k times current I1. The current flowing through resistance element 27 is Vcon/R2. Here, the sum of current (Vcon/R2) flowing through resistance element 27 and the current (k I1) flowing through NMOS transistor 31 is equal to current value Iconst of the constant current from constant current source 23. Current I1 flowing through NMOS transistor 29 is expressed as  $I1 = (extVcc - Vthn)/R1$ . Therefore, control voltage Vcon is expressed by the following equation.

$$Vcon = -(k R2/R1) extVcc + (k R2 Vthn/R1 + R2 Iconst)$$

It is appreciated from the above equation that increase in external power supply voltage intVcc causes a drop in control voltage Vcon, and decrease in external power supply voltage extVcc causes increase of control voltage Vcon. More specifically, when external power supply voltage extVcc increases, the current flowing to NMOS transistor 15 of comparator circuit 3 shown in FIG. 1 becomes smaller, so that the voltage gain of comparator circuit (current mirror type amplify circuit) 3 becomes lower. In contrast, when external power supply voltage extVcc becomes lower, the current flowing to NMOS transistor 15 of comparator circuit 3 becomes greater, so that the voltage gain of comparator circuit (current mirror type amplify circuit) 3 is increased.

According to the internal voltage-down power supply circuit of the second embodiment, the voltage gain of comparator circuit (current mirror type amplify circuit) 3 as shown in FIG. 1 has negative dependence on external power supply voltage extVcc. Therefore, increase of the closed loop gain of the internal voltage-down power supply circuit can be suppressed when external power supply voltage extVcc is altered to a high level. As a result, unnecessary oscillation of internal power supply voltage Iconst can be prevented when external power supply voltage extVcc is shifted to a high level.

FIG. 4 is a circuit diagram showing in detail another example of a current source control circuit of the internal voltage-down power supply circuit according to the second embodiment. Components corresponding to those of FIG. 3 have the same reference characters allotted, and their description will not be repeated.

Referring to FIG. 4, the current source control circuit has a PMOS transistor 33 instead of resistance element 25 of FIG. 3, and an NMOS transistor 35 instead of resistance element 27 of FIG. 3. More specifically, PMOS transistor 33 and NMOS transistor 29 are connected in series between the node having external power supply voltage extVcc and the node having the ground voltage. The ground voltage is applied to the gate of PMOS transistor 33. NMOS transistor

31 and NMOS transistor 35 are connected in parallel between node N3 and the node having the ground voltage. External power supply voltage extVcc is applied to the gate of NMOS transistor 35.

The current source control circuit of FIG. 3 differs from the current source control circuit of FIG. 4 in the elements used as the resistance. Therefore, the internal voltage-down power supply circuit employing the current source control circuit of FIG. 4 provides advantages similar to those of the internal voltage-down power supply circuit employing the current source control circuit of FIG. 3.

### Third Embodiment

First, a substrate voltage generation circuit and a boosted voltage generation circuit as a conventional internal voltage generation circuit will be described. Here, a substrate voltage generation circuit includes a negative value, and serves to generate a substrate voltage to be supplied to the semiconductor substrate. The boosted voltage generation circuit serves to generate a boosted voltage having a value greater than power supply voltage Vcc. The conventional substrate voltage generation circuit includes a ring oscillator circuit and a pump circuit. The pump circuit operates according to clock signal CLK oscillated by the ring oscillator circuit to generate a substrate voltage Vbb. The same can be said for the boosted voltage generation circuit.

When power supply voltage Vcc that drives the pump circuit is lowered, the pump efficiency is reduced. The pump efficiency is expressed as (the current flowing to the output terminal of the pump circuit)/(current consumed by the pump circuit). Also, reduction in power supply voltage Vcc driving the pump circuit causes reduction in the pump amount per one period of the clock signal CLK. The pump amount implies the current flowing through the output terminal of the pump circuit. Thus, there is a problem that, when power supply voltage Vcc is altered to a low level, the time for substrate voltage Vbb generated from the pump circuit or boosted voltage Vpp to arrive at a predetermined voltage level becomes longer than the case where the power supply voltage Vcc attains a high level. The boosted voltage generation circuit and the substrate voltage generation circuit as the internal voltage generation circuit of the third embodiment are directed to solve this problem. Accordingly, the internal voltage generation circuit (substrate voltage generation circuit, boosted voltage generation circuit) according to the third embodiment of the present invention includes a circuit identical to current source control circuit 5 of FIG. 1, a circuit identical to the current source control circuit of FIG. 3, or a circuit identical to the current source control circuit of FIG. 4. The details will be described hereinafter.

FIG. 5 is a schematic block diagram of the internal voltage generation circuit of the third embodiment. The internal voltage generation circuit of FIG. 5 can be considered as a substrate voltage generation circuit generating substrate voltage Vbb, and also as a boosted voltage generation circuit that generates boosted voltage Vpp.

Referring to FIG. 5, an internal voltage generation circuit according to the third embodiment of the present invention includes a pump circuit 37, a ring oscillator 39, and an oscillation control circuit 41. Description will be provided assuming that the internal voltage generation circuit of FIG. 5 is a substrate voltage generation circuit. Pump circuit 37 generates substrate voltage Vbb according to a clock signal (pulse voltage) CLK oscillated from ring oscillator 39. Oscillation control circuit 41 controls the frequency of clock

signal (pulse voltage) CLK oscillated from ring oscillator 39. Current source control circuit 5 of FIG. 1, current source control circuit of FIG. 3, or the current source control circuit of FIG. 4 can be used as oscillation control circuit 41.

Although external power supply voltage extVcc is used as the power supply voltage in the current source control circuits of FIGS. 1, 3 and 4, the power supply voltage of oscillation control circuit 41 of FIG. 5 may be external power supply voltage extVcc, or internal power supply voltage intVcc.

Oscillation control circuit 41 responds to a drop in power supply voltage Vcc to control ring oscillator 39 so that the frequency of clock signal (pulse voltage) CLK becomes higher according to the drop of power supply voltage Vcc. A higher frequency of clock signal CLK from ring oscillator 39 causes increase of the number of operations of pump circuit 37 per unit time. Therefore, the time required for substrate voltage Vbb to arrive at a predetermined voltage level in the case of a drop in power supply voltage Vcc can be prevented from increasing. The details thereof will be described hereinafter.

FIG. 6 shows the detail of ring oscillator 39 of FIG. 5.

Referring to FIG. 6, ring oscillator 39 is formed having an odd number of inverters connected in series. Each inverter includes a PMOS transistor 43 and an NMOS transistor 45. The output node of the inverter of the last stage (the output node of the ring oscillator) is connected to the input node of the inverter of the first stage. Furthermore, an NMOS transistor 47 is provided corresponding to each inverter.

NMOS transistor 47 is connected between the inverter formed of PMOS transistor 43 and NMOS transistor 45 and the node having the ground voltage. The gate of NMOS transistor 47 is connected to output node N3 (FIG. 1, FIG. 3, or FIG. 4) of oscillation control circuit 41. More specifically, control voltage Vcon from oscillation control circuit 41 is applied to the gate of NMOS transistor 47. The odd number of NMOS transistors 47 provided corresponding to the odd number of inverters form a current control circuit. When power supply voltage Vcc becomes lower, oscillation control circuit 41 provides control voltage Vcon that is increased according to the drop to NMOS transistor 47. Therefore, a drop in power supply voltage Vcc causes increase in the voltage flowing to NMOS transistor 47. As a result, the delay time of the output of the inverter formed of PMOS transistor 43 and NMOS transistor 45 is reduced, and the frequency of clock signal CLK becomes higher. When power supply voltage Vcc is increased, oscillation control circuit 41 provides control voltage Vcon that is reduced according to the increase to the gate of NMOS transistor 47. Therefore, increase of power supply voltage Vcc causes the current flowing to NMOS transistor 47 to be reduced. As a result, the delay time of the inverter output is increased, and the frequency of clock signal CLK becomes lower. Thus, when power supply voltage Vcc is reduced and increased to result in a higher and lower, respectively, frequency of clock signal CLK, it is said that the oscillation frequency of ring oscillator 39 has a negative dependence on power supply voltage Vcc.

The same applies to the case where the internal voltage generation circuit of FIG. 5 is a boosted voltage generation circuit.

In the internal voltage generation circuit (substrate voltage generation circuit, boosted voltage generation circuit) of the third embodiment, the oscillation frequency of ring oscillator 39 has a negative dependence on power supply voltage Vcc. Therefore, the frequency of clock signal CLK

oscillated from ring oscillator 39 becomes higher even when the power supply voltage  $V_{cc}$  is shifted to a low level and the pump amount per one operation of pump circuit 37 is reduced. Therefore, a sufficient pump amount can be achieved. In the internal voltage generation circuit (substrate voltage generation circuit, boosted voltage generation circuit) of the third embodiment, the time required for the internal voltage (substrate voltage  $V_{bb}$ , boosted voltage  $V_{pp}$ ) to attain a predetermined voltage level can be suppressed from increasing even when the power supply voltage  $V_{cc}$  is altered to a low level.

FIG. 7 is a circuit diagram showing another example of ring oscillator 39 (FIG. 5) of the internal voltage generation circuit (substrate voltage generation circuit, boosted voltage generation circuit) according to the third embodiment. Corresponding components have the same reference characters allotted, and their description will not be repeated.

Referring to FIG. 7, a ring oscillation includes a PMOS transistor 49 between PMOS transistor 43 and the node having power supply voltage  $V_{cc}$ , and a PMOS control circuit 51. PMOS control circuit 51 forms a current control circuit with the odd number of PMOS transistors 49 and the odd number of NMOS transistors 47. PMOS control circuit 51 includes PMOS transistors 53 and 55, an NMOS transistor 57, and a constant current source 59. PMOS transistor 53 and NMOS transistor 57 are connected in series between the node having power supply voltage  $V_{cc}$  and the node having ground voltage. Control voltage  $V_{con}$  from oscillation control circuit 41 is applied to the gate of NMOS transistor 57. PMOS transistor 55 and constant current source 59 are connected in series between the node having power supply voltage  $V_{cc}$  and the node having the ground voltage. PMOS transistors 53 and 55 have their gates connected to the drain of NMOS transistor 57. Output node N4 of PMOS control circuit 51 is connected to the gate of PMOS transistor 49.

Control voltage  $V_{con}$  applied to the gate of NMOS transistor 57 of PMOS control circuit 51 is a voltage that is increased according to a drop, if any, of power supply voltage  $V_{cc}$ . Therefore, a drop in power supply voltage  $V_{cc}$  causes increase of control voltage  $V_{con}$ , so that voltage  $V_p$  provided from output node N4 of PMOS control circuit 51 is decreased. Therefore, the current flowing to PMOS transistor 49 is increased, and the delay time of the inverter output is reduced. Thus, the frequency of clock signal CLK from the ring oscillator becomes higher when power supply voltage  $V_{cc}$  is reduced.

The ring oscillator of FIG. 6 has negative dependence on power supply voltage  $V_{cc}$  also in the ring oscillator (FIG. 7) including an odd number of PMOS transistors 49 and PMOS control circuit 51. Therefore, an advantage similar to the case where the ring oscillator of FIG. 6 is used as ring oscillator 39 can be provided even when the ring oscillator of FIG. 7 is used as ring oscillator 39 of the internal voltage generation circuit (substrate voltage generation circuit, boosted voltage generation circuit) of the third embodiment. In the ring oscillator of FIG. 7, NMOS transistor 47 can be removed, and the source of NMOS transistor 45 can be connected to the node having ground voltage. In this case, a similar advantage can be obtained since the oscillation frequency of the ring oscillator has a negative dependence on power supply voltage  $V_{cc}$ .

#### Fourth Embodiment

FIG. 8 shows a semiconductor device according to a fourth embodiment, particularly an internal voltage-down power supply circuit.

Referring to FIG. 8, the semiconductor device of the fourth embodiment includes an internal voltage-down power supply circuit 65 and a control circuit group (internal circuit) 63. Internal voltage-down power supply circuit 65 includes a voltage-down circuit 1 and a comparator circuit 67. Voltage-down circuit 1 is formed of a PMOS transistor, and is similar to voltage-down circuit 1 of FIG. 1. Comparator circuit 67 is formed of a current mirror type amplify circuit, and is similar to comparator circuit 3 of FIG. 1, provided that a constant current source 69 generating a constant current is disposed instead of current source 15 of comparator circuit 3 of FIG. 1. More specifically, comparator circuit 67 includes PMOS transistors 7 and 9, NMOS transistors 11 and 13, and a constant current source 69. Internal voltage-down power supply circuit 65 is arranged in the proximity of an external power supply pad not shown which is located at the chip end. Therefore, internal voltage-down power supply circuit 65 is arranged remote from control circuit group 63. Here, the external power supply pad not shown serves to supply external power supply voltage  $extV_{cc}$  to internal voltage-down power supply circuit 65.

Internal voltage-down power supply circuit 65 is connected to control circuit group 63 by a power line 71. Internal power supply voltage  $intV_{cc}$  generated in internal voltage-down power supply circuit 65 is supplied to control circuit group 63 via power line 71. Control circuit group 63 includes a plurality of control circuits, and operates with internal power supply voltage  $intV_{cc}$  as the power supply voltage. The gate of NMOS transistor 11 of comparator circuit 67 is connected to power line 71 in the proximity of control circuit group 63 as shown by arrow V2 by a conductor line 73. Conductor line 73 is a sense line, for example. Power line 71 (arrow V1) in the proximity of voltage-down circuit 1 is not connected to the gate of NMOS transistor 11 as in the conventional case.

Here, as shown in FIG. 8, conductor line 73 is connected to power line 71 only in the proximity of control circuit group 63 (indicated by arrow V2). Therefore, conductor line 73 will not be connected to power line 71 at locations other than in the proximity of control circuit group 63. When conductor line 73 is connected to power line 71 in the proximity of control circuit group 63, conductor line 73 will not be connected to power line 71 at locations other than in the proximity of control circuit group 63.

The operation of comparator circuit 67 will be described briefly. Internal power supply voltage  $intV_{cc}$  is applied to the gate of NMOS transistor 11 of comparator circuit 67. Reference voltage  $V_{ref}$  is applied to the gate of NMOS transistor 13. When internal power supply voltage  $intV_{cc}$  applied to NMOS transistor 11 becomes lower than reference voltage  $V_{ref}$ , comparator circuit 67 provides a voltage of an L level from output node N1 to the gate of PMOS transistor 1. In response, PMOS transistor 1 is turned on to down-convert external power supply voltage  $extV_{cc}$  and generate internal power supply voltage  $intV_{cc}$ . In other words, internal power supply voltage  $intV_{cc}$  is increased. When internal power supply voltage  $intV_{cc}$  applied to the gate of NMOS transistor 11 increases to the level of reference voltage  $V_{ref}$ , comparator circuit 67 provides a voltage of an H level from output node N1 to the gate of PMOS transistor 1. Therefore, PMOS transistor 1 is turned off. As a result, internal power supply voltage  $intV_{cc}$  is stable at a level equal to reference voltage  $V_{ref}$ . In contrast to the above-described general operation of an internal voltage-down power supply circuit, characteristic operations thereof will be described hereinafter.

FIG. 9 is a diagram for describing the operation of internal voltage-down power supply circuit 65 of FIG. 8. Time is

plotted along the abscissa, and internal power supply voltage intVcc is plotted along the ordinate. The curve labeled V1 in FIG. 9 corresponds to arrow V1 of FIG. 8, and indicates the variation of internal power supply voltage intVcc at power line 71 in the proximity of voltage-down circuit 1. The curve labeled V2 in FIG. 9 corresponds to arrow V2 of FIG. 8, and shows the variation of internal power supply voltage intVcc of power line 71 in the proximity of control circuit group 63. The curve labeled V3 in FIG. 9 corresponds to arrow V3 of FIG. 8, and indicates the variation of internal power supply voltage intVcc of conductor line 73 in the proximity of NMOS transistor 11.

The operation will be described with reference to FIGS. 8 and 9. Control circuit group 63 operates during an arbitrary period of a term T. Internal power supply voltage intVcc attains a level equal to reference voltage Vref prior to operation of control circuit group 63. This reference voltage Vref is referred to as "set voltage" hereinafter. In response to operation of control circuit group 63, internal power supply voltage intVcc in the proximity of voltage-down circuit 1 (arrow V1), in the proximity of control circuit group 63 (arrow V2), and in the proximity of NMOS transistor 11 (arrow V3) begins to drop. Here, the current flowing to power line 71 increases as power consumption of control circuit group 63 is increased. Therefore, the difference between the level of the internal power supply voltage in the proximity of voltage-down circuit 1 (arrow V1) and the level of the internal power supply voltage in the proximity of control circuit group 63 (arrow V2) becomes greater. No current flows through conductor line 73. Therefore, even when conductor line 73 is formed of a thin wiring with and the resistance is great, the level of internal power supply voltage in the proximity of control circuit group 63 (arrow V2) is substantially equal to the level of the internal power supply voltage in the proximity of NMOS transistor 11 (arrow V3). Therefore, variation in internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) is reflected by comparator circuit 67. More specifically, comparator circuit 67 operates according to variation in the internal power supply voltage (arrow V2) in the proximity of control circuit group 63. As a result, voltage-down circuit 1 generates internal power supply voltage intVcc according to variation of internal power supply voltage intVcc (arrow V2) in the proximity of control circuit group 63.

Thus, according to the semiconductor device of the fourth embodiment, a voltage of a level substantially equal to the internal power supply voltage (arrow V2) in the proximity of control circuit group 63 is applied to the gate of NMOS transistor 11. Therefore, when control circuit group 63 operates and internal power supply voltage intVcc becomes lower, the output of comparator circuit 67 is greatly amplified towards the L level in comparison to the case of a conventional semiconductor device (FIG. 14) where internal power supply voltage intVcc in the proximity of voltage-down circuit 1 (arrow V1) is applied to the gate of NMOS transistor 11. Therefore, the channel resistance of PMOS transistor 1 becomes lower than in a conventional semiconductor device (FIG. 14) when internal power supply voltage intVcc is reduced. As a result, the drop dV of the internal power supply voltage in the proximity of control circuit group 63 (arrow V2) becomes smaller than that of a conventional semiconductor device (FIG. 14) when control circuit group 63 is operated. More specifically, since an internal voltage-down power circuit 65 that reflects variation of internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) is provided in the

semiconductor of the fourth embodiment, variation of internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) can be reduced. This means that internal voltage-down power supply circuit 65 in the semiconductor device of the fourth embodiment has favorable followability with respect to variation in internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2).

#### Fifth Embodiment

FIG. 10 shows a semiconductor device according to a fifth embodiment of the present invention, particularly an internal voltage-down power supply circuit. Components corresponding to those of FIG. 8 have the same reference characters allotted, and their description will not be repeated.

Referring to FIG. 10, a semiconductor device according to a fifth embodiment of the present invention includes an internal voltage-down power supply circuit 77, and a control circuit group (internal circuit) 63. Internal voltage-down power supply circuit 77 includes a circuit-down circuit 1, a comparator circuit 67, and a reference voltage control circuit 75. Reference voltage control circuit 75 includes a low pass filter 81, and a Vref control circuit 79.

Excluding low pass filter 81, internal voltage-down power supply circuit 77 is arranged in the proximity of an external power supply pad not shown to supply external power supply voltage extVcc to internal voltage-down power supply circuit 77. Therefore, internal voltage-down power supply circuit 77 is remote from control circuit group 63, except for low pass filter 81. The external power supply pad not shown is arranged at the chip end.

Internal power supply voltage intVcc of power line 71 in the proximity of voltage-down circuit 1, as shown by arrow V1 is applied to the gate of NMOS transistor 11 of comparator circuit 61. Reference voltage VrefA from Vref control circuit 75 is applied to the gate of NMOS transistor 13 of comparator circuit 67. Internal power supply voltage intVcc of power supply line 71 in the proximity of control circuit group 63, as shown by (arrow V2) is applied to Vref control circuit 79 via low pass filter 81 and conductor line 83. Vref control circuit 79 also receives a reference voltage VrefB. Reference voltage VrefA having a level according to variation in internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) is applied to the gate of NMOS transistor 13 by Vref control circuit 79, which will be described in detail afterwards. Low pass filter 81 serves to apply low frequency components of internal power supply voltage intVcc to Vref control circuit 79.

FIG. 11 is a circuit diagram showing in detail Vref control circuit 79 of FIG. 10. Components in FIG. 11 corresponding to those of FIG. 10 have the same reference characters allotted, and their description will not be repeated.

Referring to FIG. 11, Vref control circuit 79 includes a comparator circuit 91, an NMOS transistor 93, a constant current source 85, and resistance elements 87 and 89.

Constant current source 85 is connected between the node having external power supply voltage extVcc and a node N5. NMOS transistor 93 and resistance element 87 is connected in parallel between node N5 and node N6. NMOS transistor 93 has its gate connected to the output node of comparator circuit 91. Resistance element 89 is connected between node N6 and the node having the ground voltage. Comparator circuit 91 has one input node connected to conductor line 83. More specifically, internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) is

applied to one input node of comparator circuit 91 via low pass filter 81. Comparator circuit 91 has the other input node connected to node N6. Reference voltage VrefB is applied to node N6. In other words, reference voltage VrefB is applied to the other input node of comparator circuit 91. Node N5 is the output node of Vref control circuit 79. Reference voltage VrefA is applied from this output node to the gate of NMOS transistor 13 (FIG. 10).

FIG. 12 is a graph for describing the operation of internal voltage-down power supply circuit 77 of FIG. 10. Time is plotted along the abscissa, and the voltage is plotted along the ordinate. This curve labeled V1 in FIG. 12 corresponds to arrow V1 of FIG. 10, and indicates the variation of internal power supply voltage intVcc in the proximity of voltage-down circuit 1. The curve labeled V2 of FIG. 12 corresponds to arrow V2 of FIG. 10, and indicates the variation of internal power supply voltage intVcc in the proximity of control circuit group 63. The curve labeled V4 of FIG. 12 indicates the variation of internal power supply voltage intVcc in the proximity (arrow V2) of control circuit group 63 (FIG. 10) that is applied to Vref control circuit 79 (FIG. 10) via low pass filter 11 (FIG. 10).

The operation of internal voltage-down power supply circuit 77 of FIG. 10 will be described with reference to FIGS. 10–12. Control circuit group 63 operates during an arbitrary time period of term T. When control circuit group 63 does not operate, the voltage (arrow V4) applied to one input node of comparator circuit 91 (FIG. 11) via conductor line 83 attains a level equal to that of reference voltage VrefB. Here, when the voltage applied to the one input node of comparator circuit 91 via conductor line 83 is equal to reference voltage VrefB applied to the other input node of comparator circuit 91, an offset is provided in comparator circuit 91 so that the output voltage of comparator circuit 91 attains an H level. In response to a voltage of an H level applied to the gate, NMOS transistor 93 is turned on. Therefore, the voltage of node N5 becomes equal to that of node N6. More specifically, reference voltage VrefA provided from node N5 becomes equal to that of reference voltage VrefB. More specifically, when control circuit group 63 is not operating, reference voltage VrefA applied to the gate of NMOS transistor 13 (FIG. 10) is equal to reference voltage VrefB. Therefore, internal power supply voltage intVcc is equal to reference voltage VrefB when control circuit group 63 does not operate.

When control circuit group 63 operates during term T, internal power supply voltage intVcc in the proximity (arrow V2) of control circuit group 63 begins to fall from the level of reference voltage VrefB due to the current flowing to control circuit group 63. The low frequency components of internal power supply voltage intVcc in the proximity (arrow V2) of control circuit group 63 are applied to Vref control circuit 79 (comparator circuit) 91. When control circuit group 63 operates and the internal power supply voltage is decreased, and when the low frequency components of internal power supply voltage intVcc in the proximity of control circuit group 63 (arrow V2) are applied to one input node of comparator circuit 91 via a low pass filter 81, comparator circuit 91 provides a voltage of an L level. NMOS transistor 93 (FIG. 11) receiving a voltage of an L level at its gate is turned off. Therefore, the voltage of node N5 becomes higher than the voltage of node N6. More specifically, the voltage of node N5 becomes higher than the voltage of node N6 by  $I_m R_t$  where  $I_m$  is the constant current generated from constant current source 85, and  $R_t$  is the resistance value of resistance element 87. This means that reference voltage VrefA becomes higher than reference voltage VrefB by  $I_m R_t$ .

When control circuit group 63 operates and internal power supply voltage intVcc in the proximity thereof (arrow V2) decreases, reference voltage VrefA becomes higher than reference voltage VrefB, and the increased reference voltage VrefA is applied to the gate of NMOS transistor 13 (FIG. 10). As a result, the output of comparator circuit 67 (FIG. 10) is greatly amplified towards the L level, whereby the channel resistance of PMOS transistor 1 (FIG. 10) becomes smaller than the case where reference voltage fixed to the gate of NMOS transistor 13 is applied. Thus, the drop dV of internal power supply voltage intVcc during operation of control circuit group 63 is smaller than the case where a reference voltage fixed to the gate of NMOS transistor 13 is applied.

When the operation of control circuit group 63 ends, reference voltage VrefA becomes equal to reference voltage VrefB. Therefore, the level of internal power supply voltage intVcc becomes equal to the level of reference voltage Vref.

In the semiconductor device of the fifth embodiment, the level of reference voltage VrefA applied to the gate of NMOS transistor 13 of comparator circuit 67 is varied according to a change in internal power supply voltage intVcc (arrow V2) in the proximity of control circuit group 63. More specifically, internal power supply voltage intVcc can be generated according to variation in internal power supply voltage intVcc in the proximity (arrow V2) of control circuit group 63. This means that the followability with respect to change in internal power supply voltage intVcc in the proximity (arrow V2) of control circuit group 63 is superior.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. An internal voltage generation circuit for generating an internal voltage, comprising:

oscillation means for oscillating a pulse voltage according to a power supply voltage,

pump means for generating said internal voltage according to said pulse voltage, and

oscillation control means, including a current mirror type amplifier, for controlling said oscillation means so that, when said power supply voltage is reduced, a frequency of said pulse voltage becomes higher according to said reduction of said power supply voltage, and when said power supply voltage is increased, the frequency of said pulse voltage becomes lower according to said increase.

2. The internal voltage generation circuit according to claim 1, wherein said oscillation control means generates a control voltage that is, when said power supply voltage is increased, reduced according to said increase, and when said power supply voltage is reduced, increased according to said reduction,

wherein said oscillation means comprises

a plurality of inverters, and

current control means for controlling current flowing through said plurality of inverters,

wherein said current control means conducts said current of a magnitude according to a level of said control voltage to said plurality of inverters.

3. The internal-voltage generation circuit according to claim 2, wherein said oscillation control means comprises a constant current source for generating a constant current, and

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resistance means connected to said constant current source,

wherein said resistance means includes a resistance element having a resistance value that is, when said power supply voltage is increased, reduced according to said increase, and when said power supply voltage is reduced, increased according to said reduction,

wherein said control voltage is provided from a node of said constant current source and said resistance means.

4. An internal voltage generation circuit for generating an internal voltage, comprising:

oscillation means for oscillating a pulse voltage according to a power supply voltage,

pump means for generating said internal voltage according to said pulse voltage, and

oscillation control means for controlling said oscillation means so that, when said power supply voltage is reduced, a frequency of said pulse voltage becomes higher according to said reduction of said power supply voltage, and when said power supply voltage is increased, the frequency of said pulse voltage becomes lower according to said increase,

wherein said oscillation control means generates a control voltage that is, when said power supply voltage is increased, reduced according to said increase, and when said power supply voltage is reduced, increased according to the reduction,

wherein said oscillation means comprises

a plurality of inverters, and

current control means for controlling current flowing through said plurality of inverters,

wherein said current control means conducts said current of a magnitude according to a level of said control voltage to said plurality of inverters, and

wherein said oscillation control means comprises

a first resistance element connected between a node having said power supply voltage and a first node, a first transistor connected between said first node and a node having ground voltage,

a constant current source connected between said node having said power supply voltage and a second node,

a second transistor connected between said second node and said node having said ground voltage, and

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a second resistance element connected between said second node and said node having said ground voltage,

wherein control electrodes of said first and second transistors are connected to said first node, and

wherein said control voltage is provided from said second node.

5. An internal voltage generation circuit for generating an internal voltage, comprising:

oscillation means for oscillating a pulse voltage according to a power supply voltage, said oscillation means comprising

a plurality of inverters each comprising a pair of transistors,

current control means for controlling current flowing to said plurality of inverters, said control means being connected to a source region of only one of the transistors of each said inverter,

pump means for generating said internal voltage according to said pulse voltage, and

oscillation control means for controlling said oscillation means so that, when said power supply voltage is reduced, a frequency of said pulse voltage becomes higher according to said reduction of said power supply voltage, and when said power supply voltage is increased, the frequency of said pulse voltage becomes lower according to said increase.

6. An internal voltage generation circuit for generating an internal voltage, comprising:

oscillation means for oscillating a pulse voltage according to a power supply voltage,

pump means for generating said internal voltage according to said pulse voltage, and

oscillation control means for controlling said oscillation means based on at least two kinds of control voltages so that, when said power supply voltage is reduced, a frequency of said pulse voltage becomes higher according to said reduction of said power supply voltage, and when said power supply voltage is increased, the frequency of said pulse voltage becomes lower according to said increase.

\* \* \* \* \*



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**United States Patent** [19]  
**Goldman**

[11] **Patent Number:** **6,081,165**  
[45] **Date of Patent:** **Jun. 27, 2000**

[54] **RING OSCILLATOR**

[75] **Inventor:** Stanley J. Goldman, Dallas, Tex.

[73] **Assignee:** Texas Instruments Incorporated,  
Dallas, Tex.

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[22] **Filed:** Jul. 17, 1998

**Related U.S. Application Data**

[60] Provisional application No. 60/053,818, Jul. 25, 1997.

[51] **Int. Cl.<sup>7</sup>** ..... H03B 27/00

[52] **U.S. Cl.** ..... 331/57; 331/175; 327/261;  
327/264

[58] **Field of Search** ..... 331/57, 175; 327/161,  
327/261, 264

[56]

**References Cited**

**U.S. PATENT DOCUMENTS**

5,461,591 10/1995 Kim et al. .... 327/534

*Primary Examiner*—Arnold Kinkad

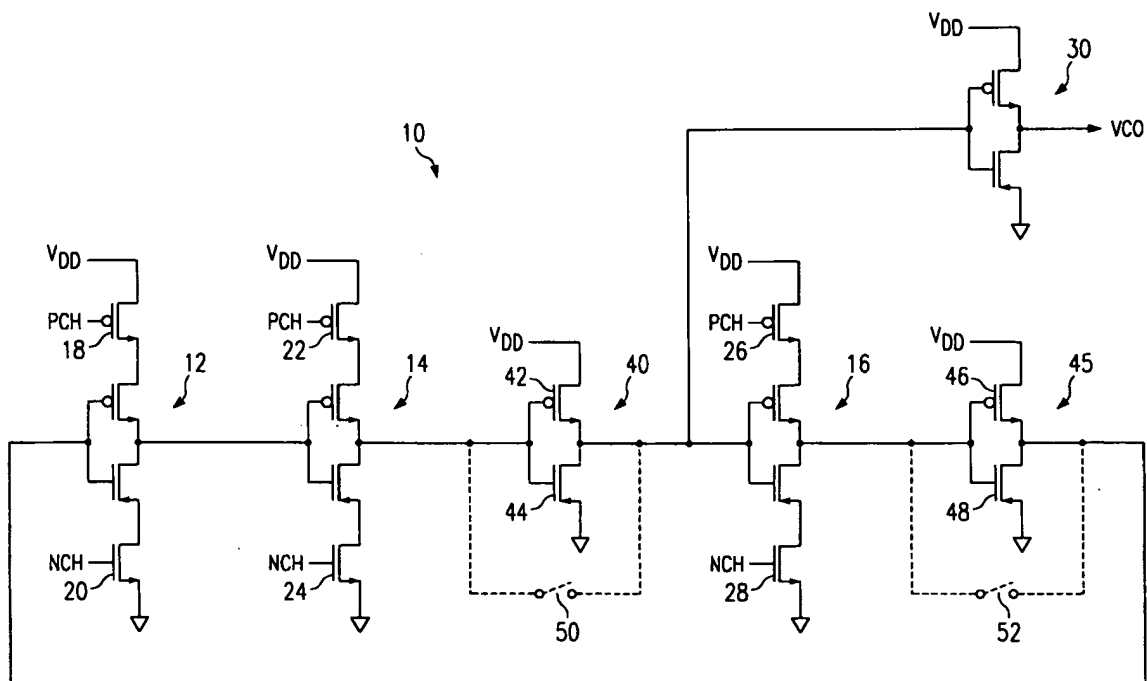
*Attorney, Agent, or Firm*—Robert D. Marshall, Jr.; Gerald  
E. Laws; Richard L. Donaldson

[57]

**ABSTRACT**

An improved ring oscillator (10, 70) includes a first, second and third current starved inverters (12, 14, 16) coupled in a ring, a first fast inverter (40) coupled between the second and third current starved inverters (14, 16), and a second fast inverter (45) coupled between the third and first current starved inverters (14, 16). An output buffer (30) coupled to the ring provides an output periodic waveform.

**12 Claims, 2 Drawing Sheets**





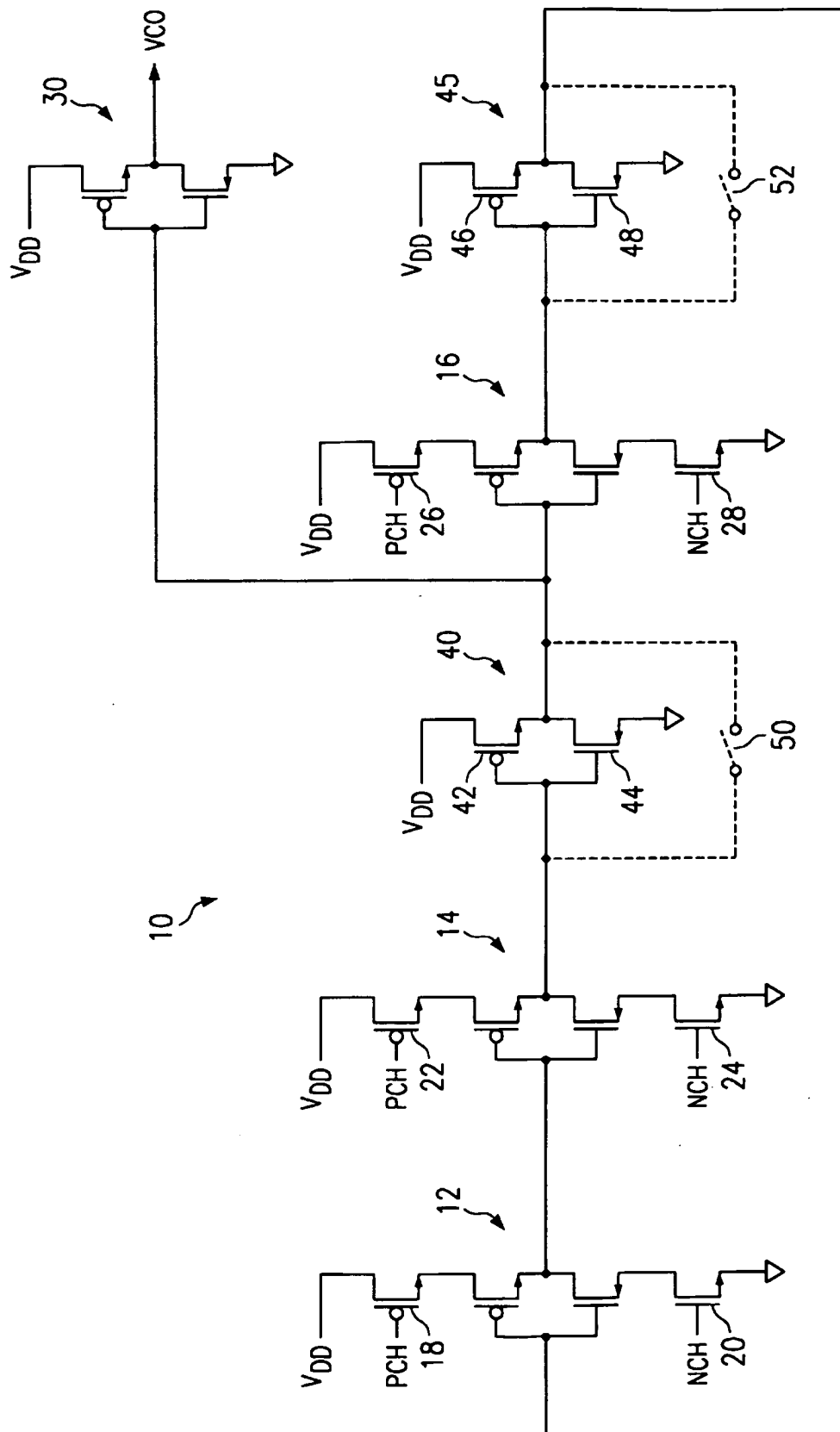


FIG. 1

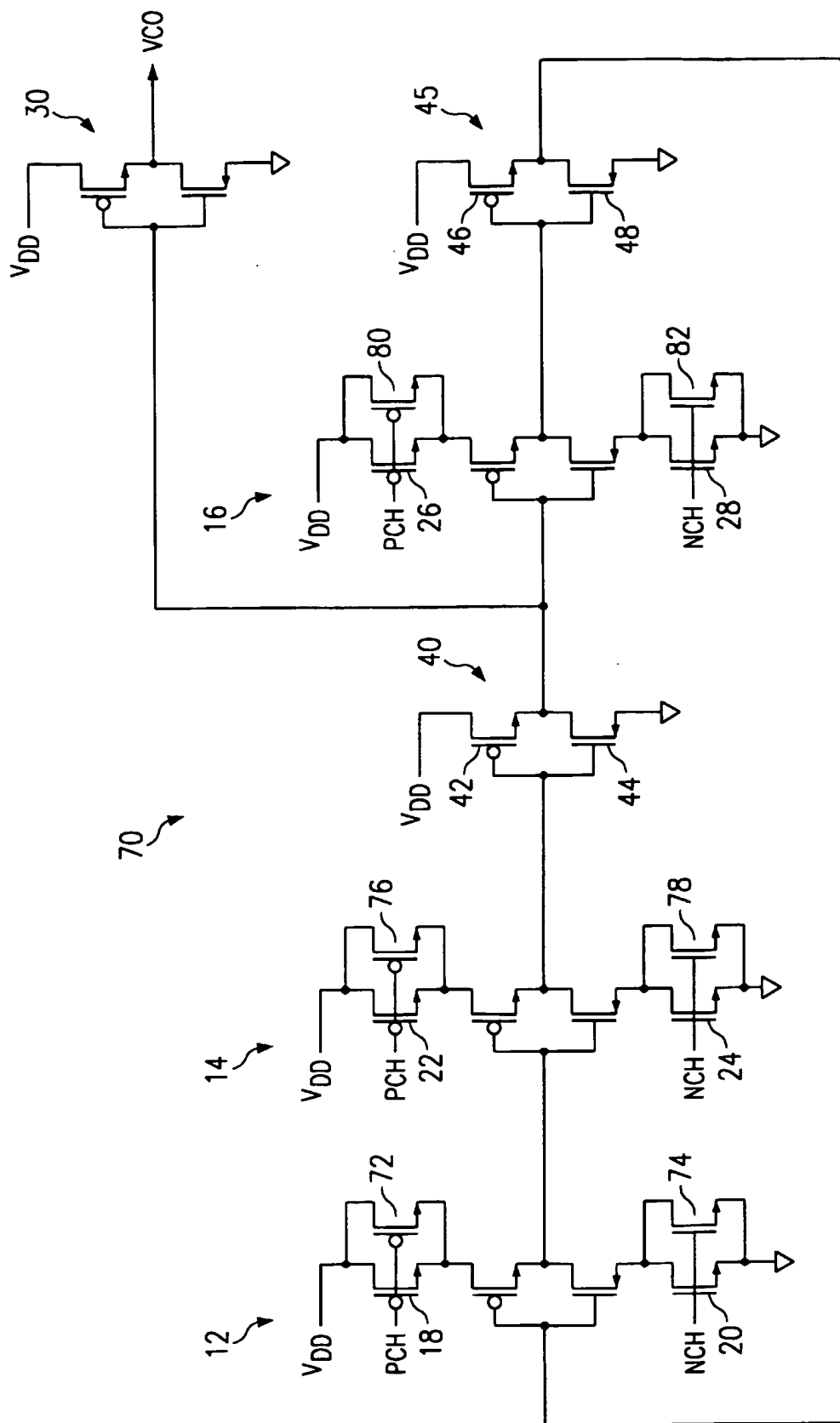


FIG. 2

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## RING OSCILLATOR

This application claims priority under 35 USC 119 (e) (1) of provisional application No. 60/053,818, filed Jul. 25, 1997.

## TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of electronic circuits. More particularly, the invention is related to an improved ring oscillator.

## BACKGROUND OF THE INVENTION

In the typical ring oscillator configuration, three inverters operating in a current starved mode are connected in a ring. The gate capacitances of the inverters are sequentially charged and discharged. Decreasing the peak available charging current increases the time to charge and discharge the gate capacitance and thus decreases the frequency of the generated periodic output waveform. Current starving the inverters in the ring slows down the output waveform edges of the inverters and keeps the transistors forming the inverters operating in a linear analog region. A linear analog oscillation mode exists if the ring oscillator operates in the linear region all of the time, if the electric length around the ring equals zero degrees, and if the gain around the ring is greater than zero dB. When the linear analog oscillation mode exists, the output periodic waveform of the ring oscillator exhibits a second higher oscillation frequency or non-harmonically related spurs or jitter. This phenomenon has been termed "moding" in the industry. Further, the two modes of oscillation at two frequencies may exhibit an injection locking condition that results in unpredictable behavior in the output waveform frequency.

Because ring oscillators are used as the voltage controlled oscillator in phase locked loop circuits commonly used in many industrial, automotive, and telecommunications applications, unpredictable behaviors such as moding and injection locking are highly undesirable.

## SUMMARY OF THE INVENTION

Accordingly, there is a need for an improved ring oscillator that does not exhibit the undesirable moding behavior.

In accordance with the present invention, an improved ring oscillator is provided which eliminates or substantially reduces the disadvantages associated with prior ring oscillators.

In one aspect of the invention, an improved ring oscillator includes a first, second and third current starved inverters coupled in a ring, a first switch coupled between the second and third current starved inverters and a second switch coupled between the third and first current starved inverters. An output buffer coupled to the ring provides an output periodic waveform.

In another aspect of the invention, an improved ring oscillator includes first, second and third current starved CMOS inverters coupled in a ring, a first switch coupled between the second and third current starved inverters, and a second switch coupled between the third and first current starved inverters. The first and second switches each includes a pMOS transistor coupled to a power supply voltage, and an nMOS transistor coupled to the pMOS transistor and ground. An output buffer is further coupled to the ring for outputting a periodic waveform.

In yet another aspect of the invention, a method for improving a ring oscillator which has a first, second and

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third current starved inverters coupled in a ring configuration includes the steps of inserting a first switch between the second and third inverters, inserting a second switch between the third and first inverters, and closing the first and second switches at different times so that there is always a discontinuity in the ring configuration. A periodic waveform is outputted between the second switch and the third current starved inverter.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of an embodiment of an improved ring oscillator according to the teachings of the present invention; and

FIG. 2 is a schematic diagram of a second embodiment of an improved ring oscillator according to the teachings of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiments of the present invention are illustrated in FIGS. 1 and 2, like reference numerals being used to refer to like and corresponding parts of the various drawings.

Referring to FIG. 1, a embodiment of an improved ring oscillator 10 constructed according to the teachings of the present invention is shown. Improved oscillator 10 is a CMOS circuit which includes a first, second and third inverters 12-16 coupled in series. Inverter 12 is further coupled to a power supply voltage,  $V_{DD}$ , through a pMOS transistor 18 and to ground through an nMOS transistor 20. Similarly, inverter 14 is also coupled to  $V_{DD}$  through a pMOS transistor 22, and to ground through an nMOS transistor 24. Inverter 16 is coupled to  $V_{DD}$  through a pMOS transistor 26, and to ground through an nMOS transistor 28. Bias voltages, PCH and NCH, are maintained at levels sufficient to turn on the respective pMOS and nMOS transistors coupled to each inverter 12-16 that function to change the rate at which the gate capacitances of each inverter charge and discharge. Inverters 12-16 operate in a current starved mode by adjusting the bias voltage levels, PCH and NCH. In addition, an output buffer 30 is coupled between second and third inverters 14 and 16 from which an output periodic waveform, VCO, is generated.

The circuit described above is a typical ring oscillator configuration which suffers from undesirable moding and injection locking conditions. According to the teachings of the present invention, two fast buffers 40 and 45 are inserted in the ring oscillator to cut off the analog oscillation mode by limiting the amount of time the oscillator spends in the linear region. Fast inverter 40 includes a pMOS transistor 42 coupled to an nMOS transistor 44 between  $V_{DD}$  and ground. Fast inverter 40 is coupled between second and third inverter 14 and 16. Fast inverter 45 is coupled between third inverter 16 and first inverter 12. Fast inverter 45 includes a pMOS transistor 46 and an nMOS transistor 48 coupled between  $V_{DD}$  and ground.

In operation, fast inverters 40 and 45 function as switches 50 and 52 (shown for illustration purposes only). For an oscillation mode at 220 MHz with a 45 ns period and a fast inverter edge of 0.5 ns, the fast inverter is in the linear region for only 3.6 degrees of the 220 MHz oscillation. Consequently, it is not in the linear region long enough for

the analog oscillation mode to get excited. Further disruption of the analog oscillation mode is obtained by staggering fast inverters 40 and 45 to switch (open and close) at different times. Because switches 50 and 52 never close at the same time, the analog feedback loop is thus disconnected.

FIG. 2 is a schematic diagram of a second embodiment of an improved ring oscillator 70 constructed according to the teachings of the present invention. In addition to fast inverters 40 and 45 inserted into the ring, parallel transistors are added to primarily increase the operating frequency of the ring oscillator which may be reduced by the addition of fast inverters 40 and 45. Inverter 12 is coupled to parallel pMOS transistors 18 and 72 and parallel nMOS transistors 20 and 74. Inverter 14 is coupled to parallel pMOS transistors 22 and 76 and parallel nMOS transistors 24 and 78. Inverter 16 is coupled to parallel pMOS transistors 26 and 80 and parallel nMOS transistors 28 and 82. The parallel pMOS and nMOS transistors are gated by the same PCH and NCH voltage levels, respectively. Typically, the frequency of output periodic waveform is increased by nearly a factor of two.

Accordingly, by inserting two fast inverters in the ring oscillator, problems such as moding and injection locking encountered by typical current starved ring oscillators are resolved. Further, optional parallel transistors may be added to improve the operating frequency of the circuit.

Although several embodiments of the present invention and its advantages have been described in detail, it should be understood that mutations, changes, substitutions, transformations, modifications, variations, and alterations can be made therein without departing from the teachings of the present invention, the spirit and scope of the invention being set forth by the appended claims.

What is claimed is:

1. An improved ring oscillator, comprising:  
first, second and third current starved inverters coupled in a ring;  
a first fast inverter coupled between the second and third current starved inverters;  
a second fast inverter coupled between the third and first current starved inverters, said first and second fast inverters having a speed of operation to conduct in a linear region insufficiently long at a frequency of operation of said ring oscillator to excite an analog oscillation mode; and  
an output buffer coupled to the ring oscillator and outputting an output periodic waveform.
2. The improved ring oscillator, as set forth in claim 1, wherein the first, second and third current starved inverters each comprises:  
a pMOS transistor coupled to a power supply voltage; and  
an nMOS transistor coupled to the pMOS transistor and ground.
3. The improved ring oscillator, as set forth in claim 2, wherein the first, second and third current starved inverters each further comprises:  
a second pMOS transistor coupled between the power supply voltage and the pMOS transistor, and being gated by a first predetermined bias voltage; and  
a second nMOS transistor coupled between the nMOS transistor and ground, and being gated by a second predetermined bias voltage.
4. The improved ring oscillator, as set forth in claim 3, wherein the first, second and third current starved inverters each further comprises:

- a third pMOS transistor coupled in parallel with the second pMOS transistor and between the power supply voltage and the pMOS transistor, and being gated by the first predetermined bias voltage; and
- a third nMOS transistor coupled in parallel with the second nMOS transistor and between the nMOS transistor and ground, and being gated by the second predetermined bias voltage.
5. The improved ring oscillator, as set forth in claim 1, wherein the first fast inverter comprises:  
a pMOS transistor coupled to a power supply voltage; and  
an nMOS transistor coupled to the pMOS transistor and ground.
6. The improved ring oscillator, as set forth in claim 1, wherein the second fast inverter comprises:  
a pMOS transistor coupled to a power supply voltage; and  
an nMOS transistor coupled to the pMOS transistor and ground.
7. The improved ring oscillator, as set forth in claim 1, wherein the first and second fast inverters do not conduct simultaneously.
8. An improved ring oscillator, comprising:  
first, second and third current starved CMOS inverters coupled in a ring;  
a first switch coupled between the second and third current starved inverters;  
a second switch coupled between the third and first current starved inverters; said first and second switches closing at different times thereby not exciting an analog oscillation mode in said ring oscillator;  
wherein the first and second switches each comprises:  
a pMOS transistor coupled to a power supply voltage; and  
an nMOS transistor coupled to the pMOS transistor and ground; and  
an output buffer coupled to the ring oscillator and outputting an output periodic waveform.
9. The improved ring oscillator, as set forth in claim 8, wherein the first, second and third current starved inverters each comprises:  
a CMOS inverter;  
a pMOS transistor coupled between a power supply voltage and the inverter, and being gated by a first predetermined bias voltage; and  
an nMOS transistor coupled between the inverter and ground, and being gated by a second predetermined bias inverter.
10. The improved ring oscillator, as set forth in claim 9, wherein the first, second and third current starved inverters each further comprises:  
a second pMOS transistor coupled in parallel with the pMOS transistor and between the power supply voltage and the inverter, and being gated by the first predetermined bias voltage; and  
a second nMOS transistor coupled in parallel with the nMOS transistor and between the inverter and ground, and being gated by the second predetermined bias voltage.
11. The improved ring oscillator, as set forth in claim 8, wherein the first and second switches do not close simultaneously.
12. An improved ring oscillator, comprising:  
a first current starved inverter having an input and an output;

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a second current starved inverter having an input connected to said output of said first current starved inverter and an output;

a first fast inverter having an input coupled to said output of said second current starved inverter and an output, 5  
said first fast inverter having a speed of operation to conduct in a linear region insufficiently long at a frequency of operation of said ring oscillator to excite an analog oscillation mode;

a third current starved inverter having an input connected 10  
to said output of said first fast inverter and an output;

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a second fast inverter having an input coupled to said output of said third current starved inverter and an output connected to said input of said first current starved inverter, said second fast inverter having a speed of operation to conduct in a linear region insufficiently long at a frequency of operation of said ring oscillator to excite an analog oscillation mode; and  
an output buffer coupled to the ring oscillator and outputting an output periodic waveform.

\* \* \* \* \*

[54] **DIRECT CURRENT POWER CONVERTERS EMPLOYING DIGITAL TECHNIQUES USED IN ELECTRONIC TIMEKEEPING APPARATUS**

3,824,447 7/1974 Kuwabara..... 307/110

## OTHER PUBLICATIONS

Electronics, p. 95, May 25, 1970.

[75] Inventor: **Brian Astle**, Princeton, N.J.

Primary Examiner—William M. Shoop

[73] Assignee: **Optel Corporation**, Princeton, N.J.

Attorney, Agent, or Firm—Joel F. Spivak

[22] Filed: **July 10, 1974**

[57] **ABSTRACT**

[21] Appl. No.: **487,319**

A converter utilizes a low voltage battery to develop a higher potential by the use of capacitors which are charged sequentially according to digital waveforms provided by counting type circuits and gates. The charge transfer circuits afford a low impedance charging path and a high impedance discharge path via a series of transmission gate controlled capacitors.

[52] U.S. Cl..... **58/23 BA; 58/50 R; 321/15**

[51] Int. Cl.<sup>2</sup>..... **G04C 3/00**

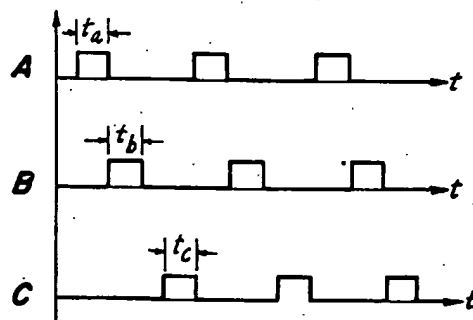
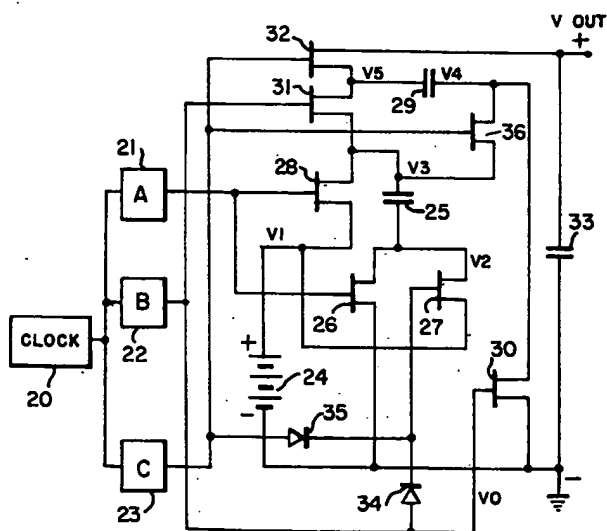
[58] Field of Search..... **58/23 BA, 50 R; 321/2, 321/15; 307/109, 110; 320/1**

The apparatus permits the conversion of low battery voltages while being completely compatible with ultra-miniature electronic systems.

[56] **References Cited****UNITED STATES PATENTS**

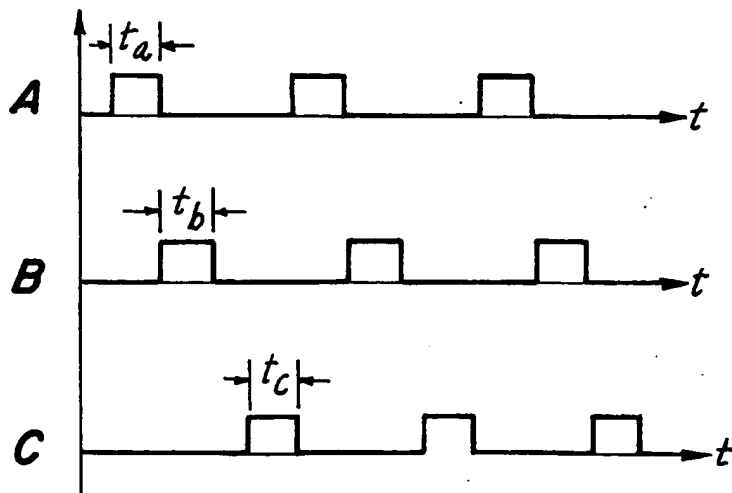
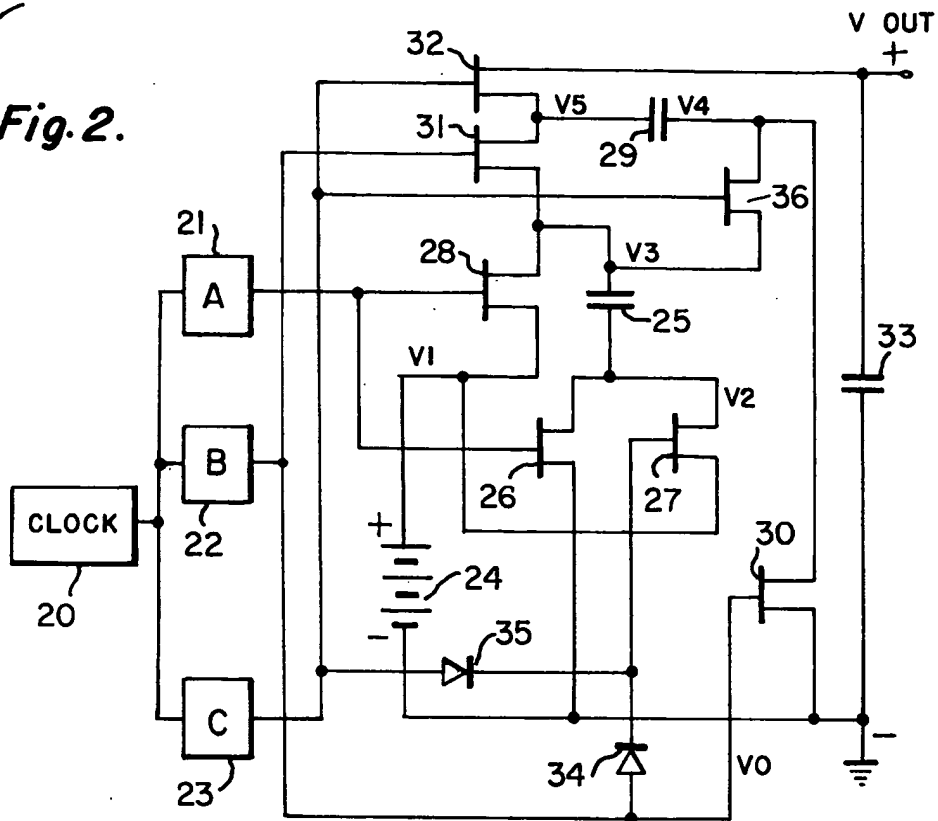
3,818,484 12/1972 Nakamura..... 58/23 BA

**15 Claims, 8 Drawing Figures**

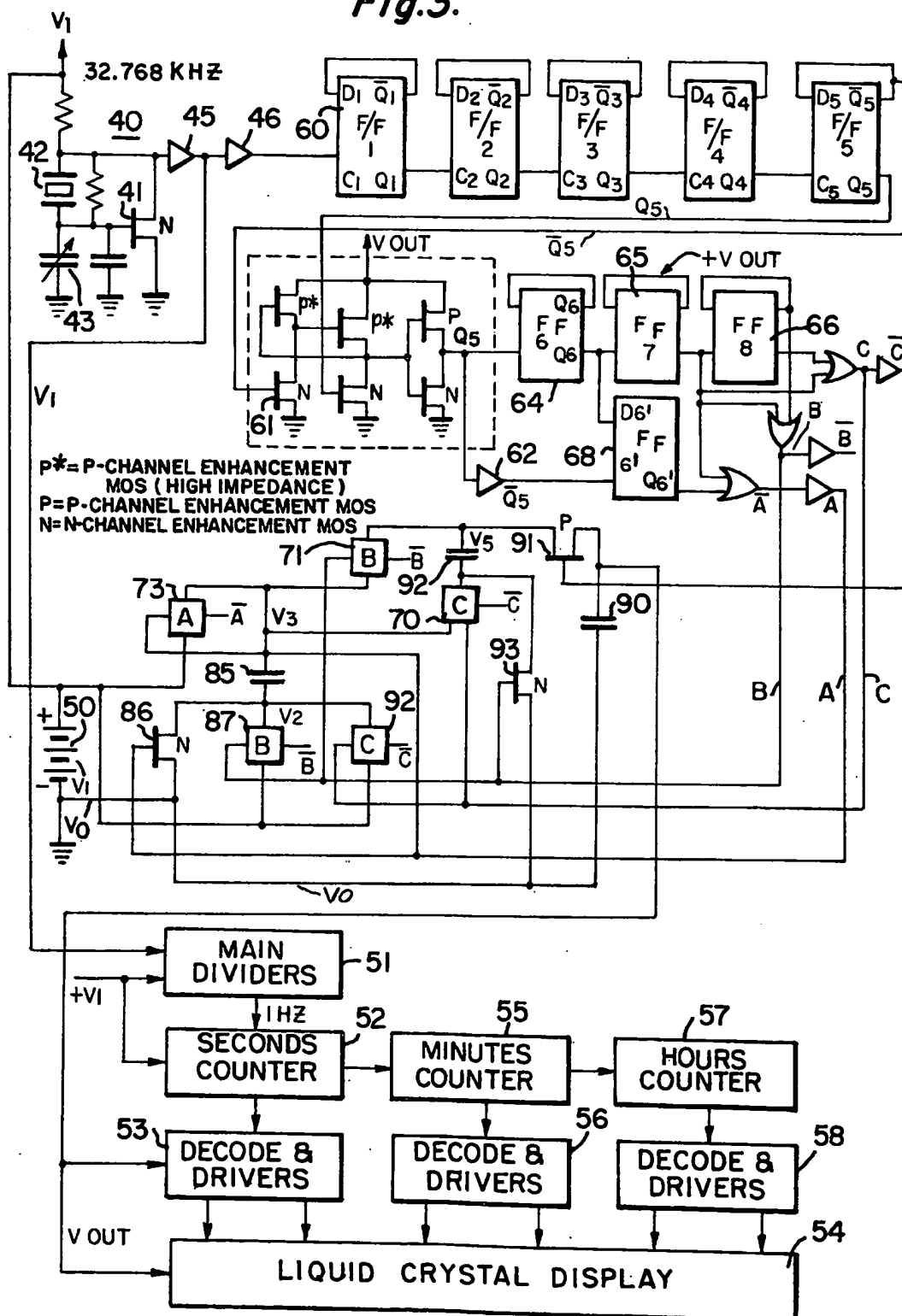




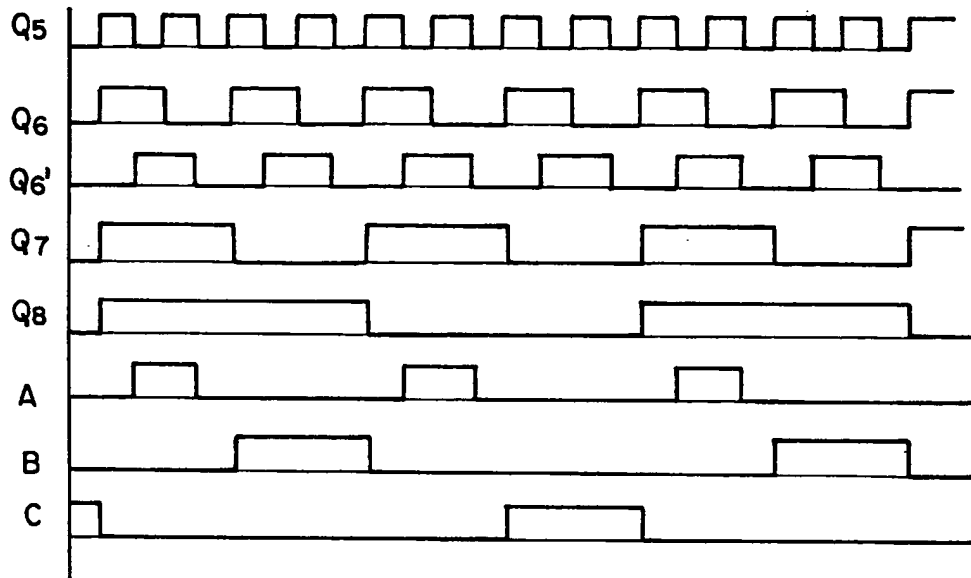
**Fig. 2.**



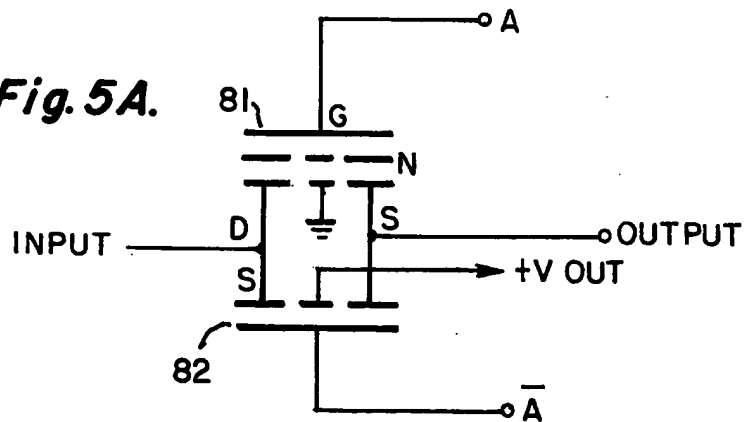




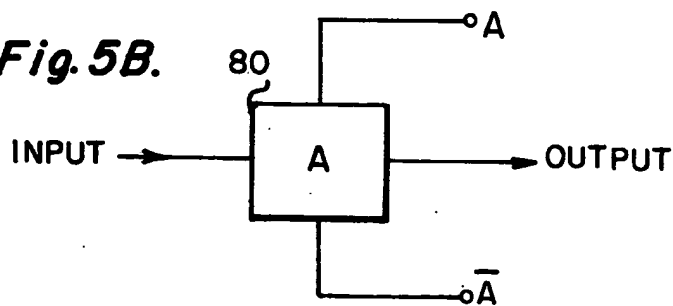
**Fig. 4.**



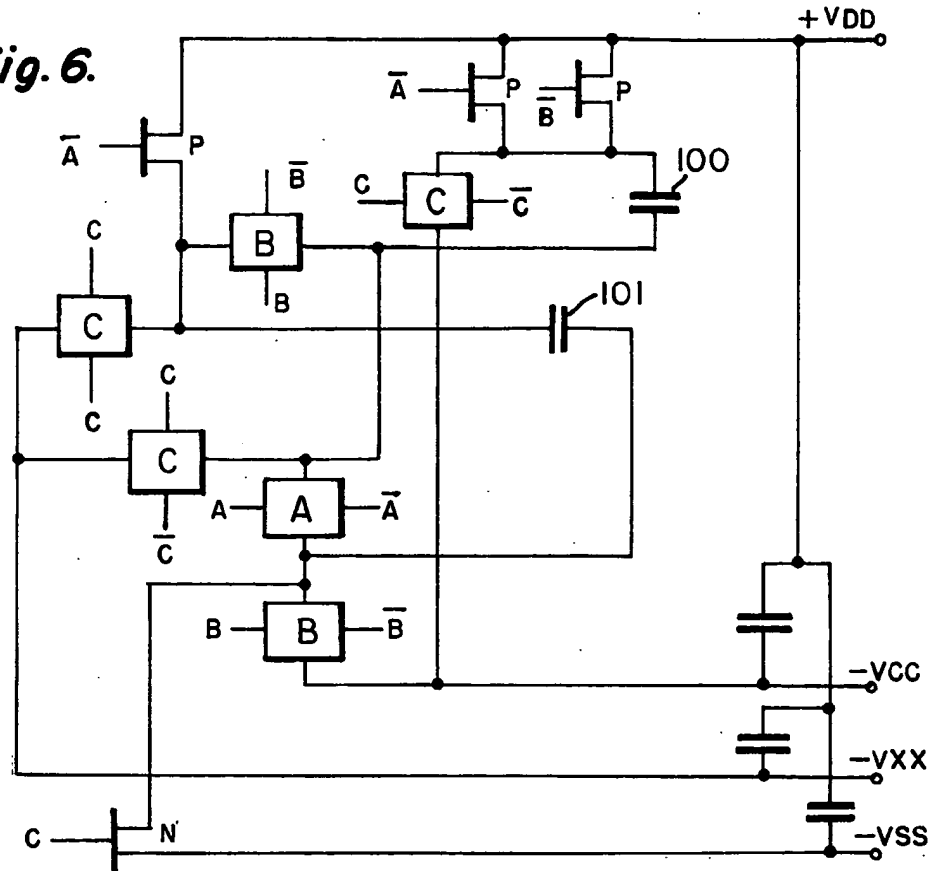
**Fig. 5A.**



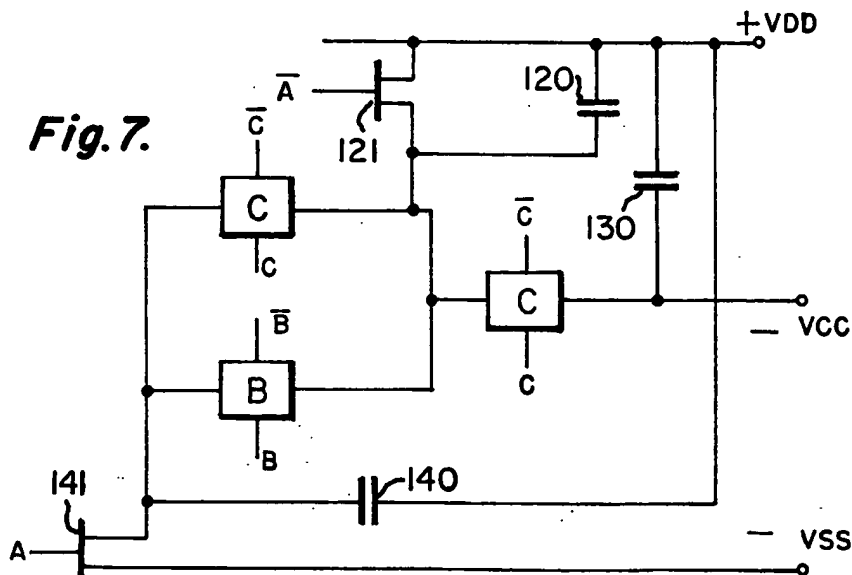
**Fig. 5B.**



**Fig. 6.**



**Fig. 7.**



## DIRECT CURRENT POWER CONVERTERS EMPLOYING DIGITAL TECHNIQUES USED IN ELECTRONIC TIMEKEEPING APPARATUS

### BACKGROUND OF THE INVENTION

This invention relates to direct current (DC) power converters for electronic watches and more particularly to a power converter employing capacitors arranged in circuit to develop high operating potentials from a low potential source.

The power converter, generally, functions to provide a high output potential from a lower potential source such as a battery.

An example of a typical use of such a converter is in an electronic timepiece or electronic watch. Such devices are relatively new and essentially are completely electronic time-keeping devices fabricated with integrated circuits and associated displays. Such watches are ultra-miniature and provide the user with extremely accurate time indication in a wrist watch configuration. As such, the watches are energized by means of small batteries which typically provide an output voltage of about 1.5 volts. This voltage, while capable of operating and biasing certain types of integrated circuits, is usually much too low to operate the display circuits associated with such watches. For example, a low power, reliable display employs the liquid crystal. Such displays require larger operating potentials than that supplied by the battery.

The system employed in such watches utilizes a relatively high frequency crystal oscillator. The oscillator utilizing a quartz resonator is extremely stable and provides an accurate output frequency. This frequency is conventionally divided down by means of multivibrator or other types of digital counting circuits, to produce, for example, a 1 Hz signal analogous to a 1 second time interval. In turn, this signal is counted by multiples of 60 for minute indication. The minute counter provides a reference to indicate the 60 minute per hour count and hence hours. The watch circuitry displays the contents of the second, minute and hour digital counters to provide signals for energizing a digital time display. Such counters may interface with the display, by means of gating circuits as AND gates and so on to indicate the time of day in a direct reading digital format. In conjunction with the fact that displays as liquid crystals, light emitting diodes and so on operate at higher potential levels than that supplied by the battery, it is also desirable in many instances to operate the logic circuitry at higher potentials (greater than 1.5 volts) to achieve greater immunity to noise and, hence, more reliable operation in general.

Thus, to obtain such potential levels, one utilizes a power converter to raise the battery potential to a desired value.

Many techniques for doing so exist in the prior art. Certain techniques employ the use of inductors which due to their response to current changes, can provide high voltage spikes or transients, which are then rectified and filtered to produce higher potential output levels. Inductors tend to be bulky and difficult to fabricate in ultra-miniature size so as to be compatible with the requirements of the electronic watch. Inductors also produce magnetic fields and the associated transients can adversely affect the operation of the digital timekeeping circuitry employed in such a watch, as the counters, dividers, and so on.

Another commonly employed technique uses a transformer to provide a voltage step-up at a secondary winding. The primary of the transformer is supplied with an AC frequency at a given level usually derived from an oscillator or a switching circuit. The turns ratio of such transformers is such that a higher potential signal is produced at the secondary which signal is then rectified and filtered to produce the required higher level DC. These circuits present similar problems to the inductor converters in that the transformers are also bulky, the transients produce noise interference and the output is difficult to regulate because of circuit component tolerance.

However, there are a variety of circuit configurations which employ capacitors to effectuate potential conversion.

Such circuits are typically classified as voltage multipliers and basically operate as the above-described generic power converter. Basically, these circuits include doublers, triplers, or quadruplers and use capacitors to avoid the use of inductors or transformers. The circuits operate to transfer charge through diodes to provide higher operating DC potentials from a lower DC source. Examples of such circuits as well as certain of the above described converters can be had by reference to a text entitled "Radio Engineering Handbook" by Keith Henney, Fifth Edition, Chapter 17, pages 17-24, 17-25 and 17-26, a McGraw-Hill publication (1959).

As can then be verified, many typical prior art capacitor converters rely on charge transfer via diode circuits and depend upon voltage developed across the capacitors to afford charge transfers by the forward and reverse biasing of the diode.

The magnitude of the available outputs of such circuits are limited as well as the fact that an increase in the multiplication factors is associated with a reduction in efficiency of power. Hence, a quadrupler is less efficient and dissipates more power than a doubler and so on.

It is therefore an object of the present invention to provide efficient converters employing ultra-miniature capacitor elements under control of digital circuitry to develop high operating potentials at increased efficiency from a lower power source.

The converters employed are particularly suitable for use in electronic timepieces although other uses are obvious and apparent.

### BRIEF DESCRIPTION OF PREFERRED EMBODIMENT

A converting apparatus is particularly adapted for use in electronic watch assemblies and provides a predetermined potential level at an output, which level is different from a source of output potential included in the watch, as, for example, a low voltage battery. The converting apparatus comprises a means for providing at least first and second waveforms synchronized one to the other; at least first and second capacitors each having a first and second terminal; one of said terminals of one of said capacitors being coupled to a point of reference potential, a plurality of transmission gates, each having an input, output and a control electrode and adapted to provide a low impedance path between said input and output electrodes upon application of said high potential to said control electrode, and means connecting said other terminals of said capacitors in circuit with said transmission gates, with said control

electrodes responsive to either said first or second waveforms to sequentially charge said capacitors in accordance with said waveforms via said controlled low impedance paths of said transmission gates to cause one of said capacitors to develop said different potential level thereacross.

#### BRIEF DESCRIPTION OF FIGURES

FIG. 1 is a partial block and schematic circuit diagram of a voltage doubler according to the invention including timing waveshapes.

FIG. 2 is a partial block and schematic circuit diagram of a voltage quadrupler including timing waveshapes.

FIG. 3 is a detailed circuit diagram of a voltage converter employed in an electronic watch apparatus.

FIG. 4 is a series of timing waveshapes useful in explaining the operation of the circuitry of FIG. 3.

FIGS. 5A and 5B are a schematic circuit diagram and a symbol diagram of a transmission gate useful in practicing the invention.

FIG. 6 is a simple block diagram of an alternate embodiment of a converter.

FIG. 7 is a block diagram of an arbitrary fractional converter according to the invention.

#### DETAILED DESCRIPTION OF FIGURES

Referring to FIG. 1, there is shown a schematic diagram of a level converter which serves to double the battery 10 voltage,  $V_1$ .

The description and circuitry is arranged for a negative ground designated as  $V_0$ , but it is understood that any polarity can be made available dependent upon which terminal of the battery 10 is referenced to ground potential.

Shown in the timing diagram of FIG. 1 are two pulse trains respectively designated as A and B. The pulse trains are synchronized in that the A pulse is high or positive when the B pulse train is low or negative and vice versa. Such pulse trains can be generated by a plethora of circuitry. For example, the waveforms A and B may be generated by the use of shift registers, counting chains and gates, monostable multivibrators and so on.

Thus, shown in FIG. 1 is a reference clock source 11, which may be a crystal oscillator as the one contained in an electronic watch for timekeeping purposes, an astable multivibrator or other suitable circuit.

Shown coupled to the output of the clock are waveform generators A and B, indicated as 12 and 14, respectively. While the generators 12 and 14 are shown schematically as separate modules, it is understood that the timing waveshapes A and B can, in fact, be generated by a common circuit such as a shift register, ring counter and so on, with appropriate decoding gates. Suffice it to say that generator (A) 12 provides the A waveshape, while generator (B) 14 provides the B waveshape shown in the above noted timing diagrams.

A capacitor 15 is shown with potential designations  $V_2$  and  $V_3$  at a first and second terminal.

The terminal designated  $V_2$  is coupled to the point of reference potential  $V_0$  via a low impedance switching device 16. Device 16 is schematically shown as a MOS transistor, with a source electrode connected to  $V_2$  and a drain electrode connected to  $V_0$ . It is understood that the opposite connections could be made as well as such devices as 16 can conduct current in either direction. The device 16 basically functions to provide a low

impedance (almost a short circuit) between its source and drain upon application to the gate electrode of a suitable biasing potential.

It is noted that any device so operating could be used in lieu of the MOS transistor 16, such as a junction transistor, relay contact and so on.

Similarly, the terminal designated at  $V_3$  of capacitor 15 is coupled to the positive battery terminal  $V_1$  via another controllable switching field effect device 17. Both the gate electrodes of transistors 16 and 17 are coupled to the A waveform generator 12 and will conduct or present the low impedance state when the A waveform exhibits a high or positive potential.

The terminal  $V_2$  of capacitor 15 is also coupled via a controllable switching device 18 to the positive terminal  $V_1$  of the battery 10. A further switch 19 has the source to drain electrode coupled between the output ( $V_{out}$ ) and the terminal  $V_3$  of the capacitor 15.

An output capacitor 20 is coupled across the  $V_{out}$  terminal to the point of reference potential  $V_0$ .

It is noted that both the control or drain electrodes of devices 18 and 19 are responsive to the waveform provided by the B waveform generator 14, and hence, will provide a low impedance between the source, and drain electrodes upon the application of a positive potential to the drain electrodes.

#### Operation of Voltage Doubler Circuit of FIG. 1

During the positive transition of the A pulse designated as  $t_a$  in the timing diagram, transistors 16 and 17 are forward biased, thus connecting terminal  $V_2$  of capacitor 15 to ground ( $V_0$ ) via transistor 16. Terminal  $V_3$  of capacitor 15 is also effectively connected to the positive terminal  $V_1$  of the battery 10. Hence, as one can verify during the positive transition of pulse A, the capacitor 15 is coupled across the battery 10, and hence, charges to the battery potential  $V_1$ . As soon as the positive transition of the A pulse terminates, the transistors 16 and 17 present a high impedance and the voltage across capacitor 15 is maintained at  $V_1$ . According to the timing waveshapes, the B waveform goes positive during the low transition of waveform A. This positive pulse duration  $t_b$  forward biases transistors 18 and 19. This condition then causes the terminal  $V_2$  of capacitor 15 to be connected to  $V_1$  or the positive terminal of battery 10. The terminal  $V_3$  is connected via transistor 19 to the output terminal or the positive terminal of capacitor 20.

The capacitor 15 transfers charge via device 19 to  $C_{20}$  and again via transistor 18 and capacitor 15 to cause the output voltage on capacitor 20 to charge to twice  $V_1$  or  $2V_1$ . Hence, at the termination of the B pulse ( $t_b$ ) capacitor 20 or the output voltage  $V_{out}$  has a voltage of two times the battery supply. This voltage is continuously maintained due to the action of the waveforms A and B in forward and reverse biasing the FET transmission gating devices 16, 17, 18, and 19. It is obvious to someone skilled in the art that the capacitor 20 could equally well be connected between  $V_{out}$  and  $V_1$ , and the output voltage be  $V_{out}$  to  $V_0$ .

#### Theory of Operation of the Voltage Quadrupler of FIG. 2

Referring to FIG. 2, there is shown timing waveforms A, B, C with positive transitions of  $t_a$ ,  $t_b$  and  $t_c$ , respectively.

The waveforms can be generated by a shift register, a counter, multivibrators, or other well-known and con-

ventional digital circuitry.

In the associated block diagram a clock source 20 supplies the input to the A, B, and C waveform generators 21, 22, 23.

A source of potential or battery 24 is shown having its negative terminal coupled to the point of reference potential  $V_0$ . A capacitor 25 has one terminal connected to a point designated as  $V_3$  and another terminal connected to a point designated as  $V_2$ . The  $V_2$  terminal is connected via a switch 26 to the reference potential  $V_0$  and via a switch 27 to the battery potential  $V_1$ . The terminal  $V_3$  of capacitor 25 is likewise coupled to the positive battery 24 terminal  $V_1$  via a switch 28. Another capacitor 29 has a first terminal designated as  $V_5$  and a second terminal designated as  $V_4$ . Terminal  $V_4$  is connected to the point of reference potential  $V_0$  via switch 30 and to terminal  $V_3$  of capacitor 25 via switch 36; while the  $V_5$  terminal is connected to terminal  $V_3$  of capacitor 25 via switch 31. A further switching device 32 connects the positive terminal of the output capacitor 33 to the  $V_5$  terminal of capacitor 29. The negative or other terminal of capacitor 33 is coupled to the point of reference potential  $V_0$ . Also shown coupled to the gate electrode of transistor 27 are diodes 34 and 35 which act as an "OR" gate, thus permitting transistor 27 to be forward biased by the positive transition of waveforms B and C from generators 22 and 23.

Thus, as seen from the FIG. 2, transistors 26 and 28 are forward biased during the positive transition (ta) of the A waveform from generator 21. Transistors 30, 31 and 27 are forward biased during the positive transition of waveform B (tb) of generator 22. The C waveform generator 23 forward biases transistors 32, 27 and 36 during the positive transition (tc) of timing waveform C. The A, B and C waveforms do not overlap as indicated in the timing diagrams of FIG. 2 to permit efficient charge transfer without undue discharging or loading.

As indicated, during the positive transition of waveform A (ta) capacitor 25 is charged to  $V_1$  or battery voltage due to the biasing of transistors 26 and 28 connecting capacitor 25 across the battery 24. Hence, capacitor 25 is charged to  $V_1$ . During the B waveform, transistor 27 connects terminal  $V_2$  to the battery voltage  $V_1$ , transistor 30 connects terminal  $V_4$  of capacitor 29 to ground  $V_0$  and terminal  $V_3$  of capacitor 29 is connected to terminal  $V_5$  of capacitor 25.

Hence, capacitor 29 charges to  $2V_1$  as the charge from capacitor 25 is transferred as well as the charge from the battery via transistor 27 and capacitor 25. Hence, at the end of the B pulse (tb) capacitor 29 is charged to  $2V_1$ .

During the pulse (tc), the terminal  $V_2$  is again connected to battery voltage  $V_1$  via transistor 26. The terminal  $V_4$  of capacitor 29 is connected to  $V_3$  of capacitor 25 via transistor switch 36, and  $V_5$  of capacitor 29 is connected to V out of the positive terminal of capacitor 33 via switch 32.

The output capacitor 33 then charges to  $4V_1$  by the charge transfer from capacitor 29 of  $2V_1$  and the additional transfer of  $2V_1$  due to the coupling of the capacitor 33 to capacitor 25 and thence to the positive battery potential  $V_1$ . Again the charging cycle is repetitive and the output voltage of  $4V_1$  is maintained across capacitor 33.

Referring to FIG. 3, there is shown a quadrupler circuit schematic according to the invention and incorporated as a power supply in an electronic watch appa-

ratus. Before proceeding with the circuit description, it will be noted that the high voltage output (V out) is used to bias and operate the converter circuitry which as due to the nature of the components utilized is self-starting. It is also noted at the onset, that the system previously described in conjunction with FIGS. 1 and 2, is a boot-strapping scheme since the output voltage V out is used to drive the converter switching logic circuitry, a portion of which is also biased from the low voltage battery supply  $V_1$ .

Numeral 40 references a crystal oscillator circuit employing a n-channel enhancement MOS 41 as an amplifier. The crystal 42 is selected at a frequency near 32,768 KHz, which frequency is that normally employed in present day electronic timekeeping assemblies. The capacitor 43 serves as a trimmer to adjust the exact frequency. The oscillator circuit is conventional and many examples of suitable circuitry exist in the prior art. The oscillator 40 is isolated by means of two inverting amplifiers 45 and 46, which present a high input impedance to avoid undue loading of the oscillator 40 and a low output impedance for efficient driving of additional circuitry. The oscillator 40 is biased by means of a battery supply 50, which typically is a ultra small battery operating at about 1.2 to 1.7 volts. As such, batteries as 50 are used presently to energize and power electronic watch assemblies. The low voltage is not sufficient to drive or bias certain types of displays as liquid crystals and so on. Hence, many electronic watches employ a power or voltage converter such as those described above in regard to the description of the prior art.

The oscillator's 40 output, which may be derived from either inverter 45 or 46, is directed to a divider chain 51, which may comprise cascaded multivibrators to provide a timekeeping signal at, for example, a 1 Hz duration. It is noted that the frequency of 32,768 Hz is a binary number and hence, cascaded multivibrators can provide the 1 Hz signal without employing complicated feedback or resetting techniques.

The 1 Hz signal has a 1 second rate which is extremely accurate as being derived from the crystal oscillator 40.

This signal is coupled to a SECONDS counter 52, which counts and stores sixty one second transitions and commences from zero upon completion of a count of sixty. The output of the seconds counter 52 is decoded to decimal format by means of decoder and driver circuits 53 and is used to activate the suitable digits indicating seconds of a liquid crystal display 54.

The transition pulse indicating a count of sixty by the second counter is coupled to a minute counter 55, which also counts and stores sixty such transition pulses to thence decode and display minutes via decoder and drivers 56. In a similar manner an hour counter 57 in conjunction with an hour decode and display driver 58, serves to monitor and display hours.

The liquid crystal display as well as the driver circuitry requires larger voltages than that supplied by the battery 50. Therefore, a converter is necessary to supply the voltage V out, which may be four or more times higher than  $V_1$  or the battery voltage 50.

For examples of typical liquid crystal displays and driving arrangements, reference is had to U.S. Pat. No. 3,744,049 entitled LIQUID CRYSTAL DRIVING AND SWITCHING APPARATUS UTILIZING MULTIVIBRATORS AND BIDIRECTIONAL SWITCHES by N. A. Luce, issued on July 3, 1973 and assigned to

Optel Corporation, the assignee herein.

The crystal oscillator 40 frequency is also used to derive the waveforms as A, B, and C of FIG. 2, for example, for the converter circuitry. Thus shown having a  $C_1$  (clock) input coupled to the output of inverter amplifier 46 is a flip-flop or multivibrator 60 further designated as F/F1. The flip-flop 60 has a normal output  $Q_1$  and an inverted output  $\bar{Q}_1$ . The particular configuration indicated for flip-flop 60 is referenced to in the art as a D type circuit. The circuit operates such that the logic level present at the D input ( $D_1$  for F/F1, 60) is transferred to the Q output ( $Q_1$  for F/F1, 60) during a positive clock transition. D flip-flops are well-known and are provided in COS/MOS circuit chips. For a clearer explanation of such circuits reference may be had to a publication entitled COS/MOS INTEGRATED CIRCUITS MANUAL by RCA - Solid State Division, Somerville, New Jersey, copyrighted 1971, on pages 20 and 21. It is noted that any other type of flip-flop can be used as well, depending upon power requirements and operating potentials.

The D type flip-flops F/F1 to F/F5 function to divide the oscillator 40 frequency by a factor of thirty-two. Each stage is a D flip-flop 60 and operates accordingly. It is also noted that the chain of flip-flops, as shown, F/F1 to F/F5, serves to divide the clock or oscillator frequency by, for example, thirty-two. Hence, one could actually use the main dividers 51 to obtain the required waveshapes or alternatively, one could utilize the output signal of F/F5 to obtain a frequency output signal of 1024 Hz which then may be divided by a 10 stage binary counter to produce an output of 1 Hz. Thus, it should be apparent that the divider shown can also be used in the previously described clock circuitry.

The outputs of F/F5 are designated as  $Q_5$  and  $\bar{Q}_5$  and the waveform is shown in FIG. 4 as  $Q_5$ , the  $\bar{Q}_5$  is the inverted version of the waveform  $Q_5$  of FIG. 4.

The oscillator 40, as well as the flip-flops F/F1 to F/F5 are all biased and operate from the battery 50 voltage  $V_1$ .

The output waveforms of F/F5 are applied to a MOS level converter circuit comprising stacked pairs of p-channel enhancement MOS devices with n-channel enhancement devices. The level converter 61 operates from the  $V_{out}$  voltage which is the output of the quadrupler circuit, and hence, the above-described bootstrapping operation is so implemented.

The level converter may also be obtained as an integrated chip and the above-referenced RCA publication contains examples of suitable circuits on pages 59 to 69. The output of the level converter is the  $Q_5$  waveform shown in FIG. 4 at a higher voltage level than the waveform available at the  $Q_5$  output of F/F5. The higher potential  $Q_5$  signal from the level converter 61 is inverted by inverter to obtain the  $\bar{Q}_5$  signal. These signals are used to control the operation of an additional counter chain comprising D type flip-flops F/F6 to F/F8 and designated as 64, 65 and 66, respectively. These flip-flops are the same configuration as F/F1 to F/F5, but operate at the higher voltage level from the converter +V out.

An additional D flip-flop 68 has its D input coupled to the  $Q_6$  output of flip-flop 64 and its clock is C input supplied by the inverter 62.

The outputs of the stages 64, 65, and 68 are shown in FIG. 4 as  $Q_6$ ,  $Q_6^1$ ,  $Q_7$  and  $Q_8$ . These waveforms are operated on by typical AND and OR gate logic assemblies to provide the waveforms A, B, and C of FIG. 4.

These waveforms do not overlap as indicated in regard to the description of FIG. 2 and permit the charging and discharging of the converter capacitors by the abovedescribed techniques.

It is noted that FIG. 3 shows both the inverted and noninverted outputs for waveforms A, B, and C of FIG. 4, namely  $\bar{A}$ ,  $\bar{B}$ , and  $\bar{C}$ .

In describing the operation of the doubler and quadrupler circuits of FIG. 1 and FIG. 2, it was indicated that the active transmission devices could be bidirectional FET devices to allow charging and discharging of the capacitors. It was also indicated that the switching devices could, in fact, be a relay contact as a single pole, single throw switch. FIG. 3 shows a series of modules as 70, 71 and 73, each is designated respectively as C, B, and A. They are transmission gates which perform the exact functions of transistors as 16 and 18 of FIG. 1 or 26 and 27 of FIG. 2.

Basically, a transmission gate such as 70, 71 or 73 can be implemented with COS/MOS logic circuitry. (See RCA reference, pages 17 and 18), and is, in fact, a close approximation to a single pole, single throw switch. It is formed by the parallel connection of a p-type and an n-type device. The gate electrode of one device is activated by the non-inverted clock and the gate electrode of the other device by the inverted clock as A and  $\bar{A}$ . The source and drain electrodes are connected together to provide the low impedance path required to reliably charge and discharge the capacitors as indicated in FIG. 2. The operation of the transmission gate is extremely simple and will be explained in regard to FIG. 5.

FIG. 5B shows the schematic used in FIG. 3 for a transmission gate. Hence, the gate 80 of FIG. 5B is a single pole electronic circuit which conducts or presents a low impedance path between the input and output when the A waveform exhibits a high potential level.

FIG. 5A shows the circuit. A first n-type MOS 81 has its drain connected to the source of a p-type MOS device 82. The source of 81 is likewise connected to the drain 82. The source and drain connections form the input terminal and the opposite connections form the output terminal. The gate of device 81 is coupled to an A waveform source while the gate of the p-device 82 is coupled to an  $\bar{A}$  waveform source. Biasing is applied as shown by +V out to the substrate connection of the p-device.

When the A clock is high, the  $\bar{A}$  is low. Thus, both transistors 82 and 81 are conducting and there is an extremely low impedance path between the input and output terminals. When the A clock reverses polarity, both transistors are biased off, and hence, there is an extremely high impedance between input and output.

The circuit shown in FIG. 5A is a bilateral as the drain and source electrodes are interchangeable. The gate shown in FIG. 5A is faster in operation than a single n-channel transmission gate.

Again, referring to FIG. 3, it can then be ascertained that the configuration shown is, in fact, a quadrupler as the one described in FIG. 2. The table below indicates corresponding parts and the operation is otherwise identical.

TABLE

FIG. 2 Component	FIG. 3 Counterpart
Battery 24	Battery 50
Capacitor 25	Capacitor 85

TABLE-continued

FIG. 2 Component	FIG. 3 Counterpart
Transmission Gate 27	Transmission Gate 87
Transmission Gate 26	Transmission Gate 86
Transmission Gate 28	Transmission Gate 73
Transmission Gate 36	Transmission Gate 70
Transmission Gate 30	Transmission Gate 93
Transmission Gate 27 (OR)	Transmission Gate 92
Transmission Gate 31	Transmission Gate 71
Transmission Gate 32	Transmission Gate 91
Capacitor 29	Capacitor 92
Capacitor 33	Capacitor 90
$V_{ss}, V_1, V_2, V_3, V_4, V_5, V_{out}$	$V_{ss}, V_1, V_2, V_3, V_4, V_5, V_{out}$

The circuit of FIG. 3 was constructed using  $C_{85}=C_{82}=C_{90}=0.047$  microfarads with a battery voltage  $V_1$  of 2.5 volts, the output was 6.66 volts.

Increasing the size of the capacitors indicated above to 0.47 microfarads gave an output of 9.04 volts. The logic circuits as well as the inverters, flip-flops and gates were implemented with RCA COS/MOS circuits available as the 4000 series and sold by the RCA Solid State Division of Somerville, New Jersey 08876.

The 0.047 microfarads capacitors used are approximately 0.050 inches wide, 0.050 inches high, and 0.080 inches long and are generally designated as chip capacitors. The circuitry shown in FIG. 3 supplied in excess of 1 microamp at the voltage of 9.04 volts and operated between 90 and 95 percent efficiency.

The circuit was self-starting in that substrate leakage in the integrated circuits causes a voltage to develop across capacitor 90. Once the voltage appears, the circuits become biased and the voltage across the capacitor 90 builds up until the quiescent value is achieved.

#### Converter for Providing Rational Fractional Voltages

FIG. 6 shows another embodiment of an aspect of this invention. The transmission gates designated as A, B, and C are as those shown in FIG. 3 and FIG. 5B and the A, B, and C waveforms are those shown in FIGS. 2 and 3, the  $\bar{A}$ ,  $\bar{B}$ , and  $\bar{C}$  being the non-inverted and the A, B, and C being the inverted or one hundred and eighty degrees out of phase waveforms.

From the circuit shown in FIG. 6, it can be ascertained that during the positive level of the A pulse capacitors 100 and 101 are connected in parallel and therefore share charge. During the B pulse, capacitors 100 and 101 are connected in series between  $+V_{DD}$  and  $-V_{cc}$ . During the C pulse, capacitor 100 is connected between  $-V_{cc}$  and  $-V_{xx}$  and capacitor 101 is connected between  $-V_{xx}$  and  $-V_{ss}$ .

If one applies a voltage between  $+V_{DD}$  and  $-V_{ss}$ , the circuitry shown under control of the A, B, and C waveforms generates  $\frac{1}{2}$  and  $\frac{1}{4}$  of the voltage. A voltage applied between  $+V_{DD}$  and  $-V_{cc}$  generates  $\frac{1}{2}$  and twice the voltage.  $V_{DD}$  is reference potential and is normally 0 volts. Hence, for a voltage of -1.6 volts applied between  $V_{DD}$  and  $V_{cc}$ ,  $V_{xx}$  would be at -2.4 volts and  $V_{ss}$  at -3.2 volts.

#### Converter for Developing Arbitrary Fractional Voltages

Referring to FIG. 7,  $+V_{DD}$  is a point of reference potential. The  $-V_{ss}$  is the battery source line and has a value equal to the battery value  $V_1$ . The timing waveforms A, B, and C are again identical with those shown in FIG. 2 or FIG. 3 and the transmission gates as indi-

cated either by the block diagram or the semiconductor symbology are those types above-described.

The operation is as follows:

During the A pulse, capacitor 120 is accessed by means of the transmission gate 121, and hence, is discharged or charged to zero volts. Capacitor 140 is connected to  $-V_{ss}$  of  $V_1$  via switch 141 and charges to  $-V_1$ . During the B pulse, capacitor 120 is in parallel with capacitor 140 and capacitor 120 charges to:  $-C_{140} V(C_{120} + C_{140})$ . During the C pulse, capacitor 130 is in parallel with  $C_{120}$  and  $C_{140}$ , and hence, changes to:

$$\frac{-C_{130} V_{ss}}{C_{130} + C_{120}}$$

Hence, as one can ascertain, the value of  $C_{140}$  and  $C_{120}$  determine the output voltage  $-V_{cc}$ . This, of course, can be of either polarity (positive or negative) depending upon the battery potential as applied between  $-V_{ss}$  and  $+V_{DD}$ . If  $C_{140} = C_{120}$  then:

$$V_{cc} = \frac{-V_{ss} - V_1}{2}$$

Thus, the above specification describes a variety of novel converters relying on the transfer of charge via high efficiency transmission gates which are controlled by digital waveforms generated by conventional digital circuitry.

It will be well understood by those skilled in the art how modifications and additional circuitry could be implemented using the above-described concepts.

I claim:

1. In an electronic watch assembly of the type employing an accurate source of oscillations for providing a timekeeping signal, said watch including a low voltage battery for energizing circuitry included in said watch, the combination therewith of apparatus for converting said low voltage battery potential to a higher voltage level, comprising:

- a means coupled to said accurate source of oscillations for providing at least first and second waveforms synchronized one to the other, said waveforms characterized in that said first one is at a positive level when said second one is negative and vice versa, said waveforms having no condition where both can be positive or both can be negative, as the waveforms do not overlap,
- a first capacitor having a first and second terminal,
- a second capacitor having a first and second terminal with said second terminal coupled to a point of reference potential,
- a plurality of transmission gates each having an input and output terminal and capable of operating in a low impedance state upon application of a predetermined potential level to a control electrode associated with each of said gates,
- means coupling one of said terminals of said first capacitor to an output terminal of a first one of said transmission gates and said other terminal to an output of another of said transmission gates, the input of said first transmission gate being coupled to a terminal of said low voltage battery and the input of said another gate being coupled to a point of reference potential, and



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f. means coupling said first terminal of said second capacitor to an output of still another transmission gate with said input of said gate coupled to a terminal of said first capacitor, said control electrodes of said gates being responsive to a selected one of said first and second waveforms to energize said gates in a predetermined sequence whereby said low battery voltage charges said capacitors via said gates in a manner to provide a different potential than said battery potential across said second capacitor, said second capacitor only being coupled to said battery during said second waveform and only when said first capacitor is not so coupled, whereby said first and second capacitors are never in parallel, and

g. means for transferring said charge across said first and second capacitors to a third output capacitor.

2. The converting apparatus according to claim 1, wherein said transmission gates comprise at least one field effect transistor having a source output terminal, a drain input terminal, and a gate control electrode.

3. The converting apparatus according to claim 2, wherein said field effect device is bilateral.

4. The converting apparatus according to claim 1, wherein said means coupled to said accurate source of oscillations comprise a plurality of cascaded multivibrators for dividing said accurate source by a given integer, and gating means coupled to said multivibrators for providing said first and second waveforms at respective outputs of gating means.

5. The apparatus according to claim 4, wherein said multivibrators are flip-flops employing MOS devices.

6. The apparatus according to claim 1, wherein said potential across said second capacitor is greater than said battery potential.

7. The apparatus according to claim 1, wherein said potential across said second capacitor is a rational fraction of said battery potential.

8. The apparatus according to claim 1, wherein said potential across said second capacitor is an arbitrary fraction of said battery potential.

9. The apparatus according to claim 1, wherein said potential across said second capacitor is relatively equal to said battery potential multiplied by the integer  $2n$ , where  $n$  is greater than 1.

10. The apparatus according to claim 1, wherein said first terminal of said second capacitor is coupled to said means coupled to said accurate source for energizing the same with said potential level across said capacitor.

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11. Converting apparatus for providing a predetermined potential level at an output, which level is different from a source of operating potential, comprising:

a. means for providing at least first and second waveforms synchronized one to the other, said waveforms characterized in that said first one is at a positive level when said second one is negative and vice versa, said waveforms having no condition where both can be positive or both can be negative, as the waveforms do not overlap,

b. at least first and second capacitors, each having a first and second terminal, one of said terminals of one of said capacitors being coupled to a point of reference potential,

c. a plurality of transmission gates, each having an input, output, and a control electrode and adapted to provide a low impedance path between said input and output electrodes upon application of said high potential to said control electrode,

d. means connecting said other terminals of said capacitors in circuit with said transmission gates, with said control electrodes responsive to either said first or second waveforms to sequentially charge said capacitors in accordance with said waveforms via said controlled low impedance paths of said transmission gates to cause one of said capacitors to develop said different potential level thereacross, wherein, due to said waveforms, one of said capacitors is only coupled to said battery when the other of said capacitors is not and said first and second capacitors are never in parallel, and

e. means for transferring said charge across said first and second capacitors to a third output capacitor.

12. The converting apparatus according to claim 11, wherein said means for providing at least said first and second waveforms comprises a crystal oscillator capable of providing a relatively stable output signal of a given frequency, and counting means coupled to said oscillator for providing a series of digital waveshapes, decoding means responsive to said waveshapes for providing at an output said first and second waveforms.

13. The converting apparatus according to claim 11, wherein said transmission gates are parallel  $p$  channel,  $n$  channel MOS devices.

14. The converting apparatus according to claim 11, wherein said level different from said operating potential is  $2n$  times the same, where  $n$  is an integer greater than 1.

15. The converting apparatus according to claim 12, wherein said crystal oscillator is that included as a time-keeping source in an electronic watch apparatus.

\* \* \* \* \*



US005392205A

**United States Patent** [19][11] **Patent Number:** 5,392,205**Zavaleta**[45] **Date of Patent:** Feb. 21, 1995**[54] REGULATED CHARGE PUMP AND METHOD THEREFOR**[75] **Inventor:** Mauricio A. Zavaleta, Austin, Tex.[73] **Assignee:** Motorola, Inc., Schaumburg, Ill.[21] **Appl. No.:** 789,248[22] **Filed:** Nov. 7, 1991[51] **Int. Cl.<sup>6</sup>** ..... H02M 3/18[52] **U.S. Cl.** ..... 363/59; 363/60;  
323/311; 323/285[58] **Field of Search** ..... 363/59, 60, 61;  
323/311, 275, 285; 307/296.6, 296.8**[56] References Cited****U.S. PATENT DOCUMENTS**

3,909,695	9/1975	Peck	363/25
4,278,929	7/1981	Lee et al.	323/311
4,291,366	9/1981	Nelson	363/17
4,430,641	2/1984	Baur et al.	340/347 DA
4,438,346	3/1984	Chuang et al.	307/297
4,471,290	9/1984	Yamaguchi	323/274
4,553,047	11/1985	Dillinger et al.	307/297
4,752,699	6/1988	Cranford, Jr. et al.	307/297
4,803,612	2/1989	Skovmand	323/284
4,807,104	2/1989	Floyd et al.	363/59
4,965,711	10/1990	Kamp et al.	363/60

**OTHER PUBLICATIONS**

"MPT 1375, Common Air Interface Specification",  
Department of Trade and Industry, London, 1989.

"MC145532 ADPCM Transcoder Product Review", in

Motorola Telecommunications Device Data, DL 136,  
Rev. 2, Motorola, Inc. 1989.

"MC145554/MC145557/MC145564/MC145567 PCM  
Codec-Filter", in Motorola Telecommunications De-  
vice Data, DL 136, Rev. 2, Motorola, Inc., 1989.

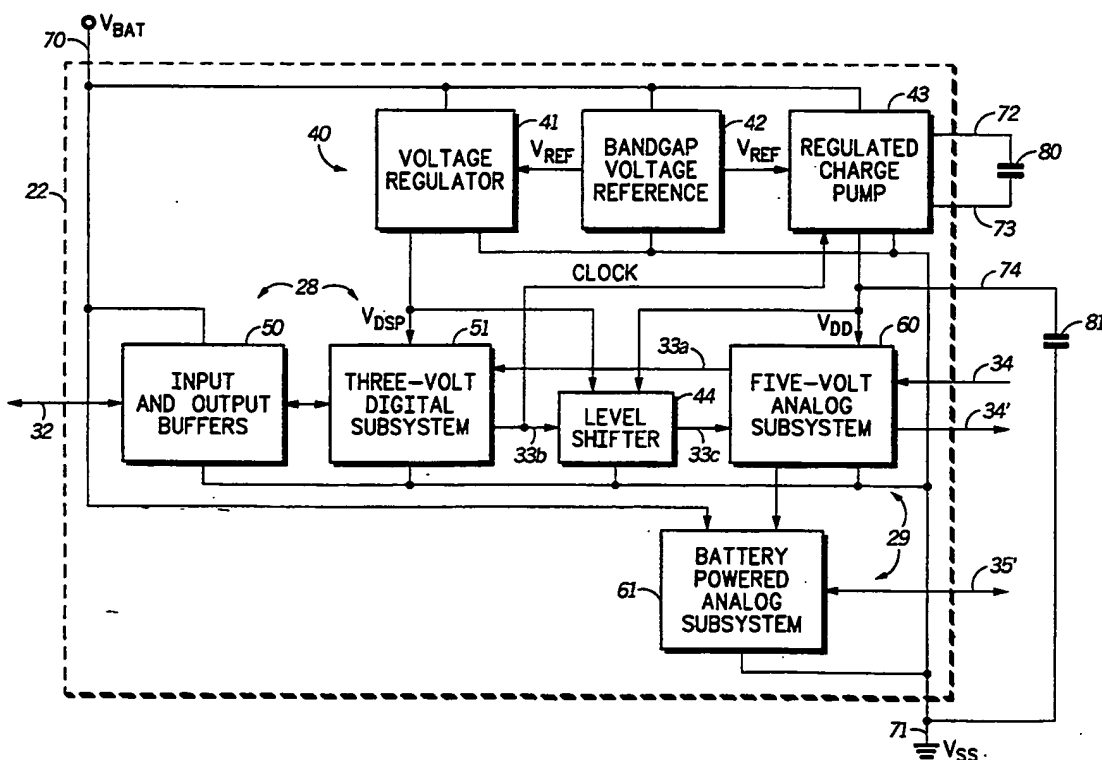
*Primary Examiner*—Steven L. Stephan

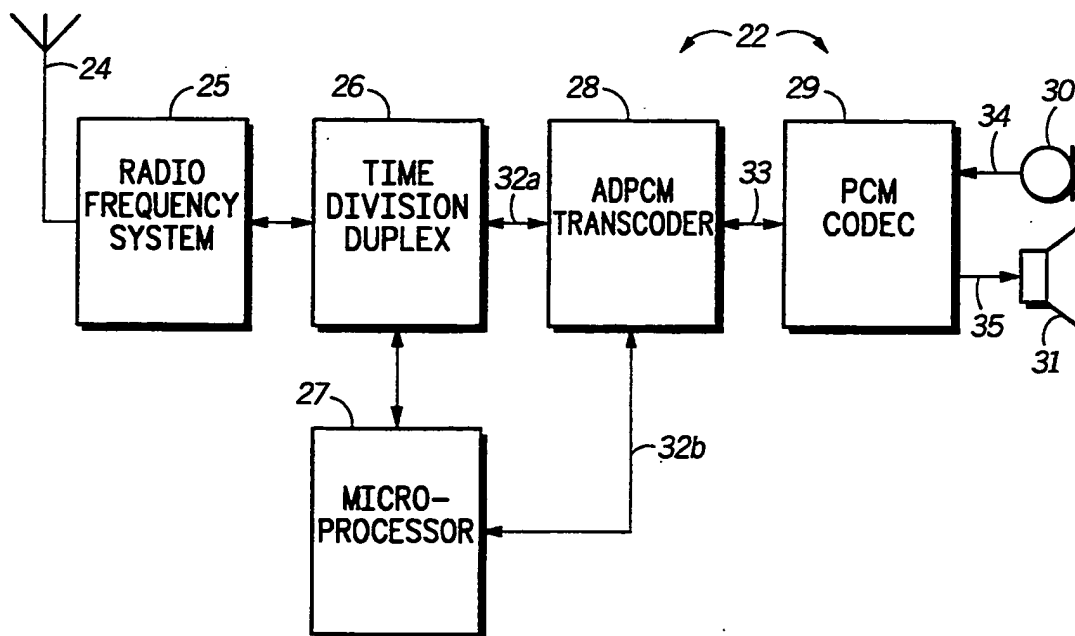
*Assistant Examiner*—Adolf Berhane

*Attorney, Agent, or Firm*—Paul J. Polansky

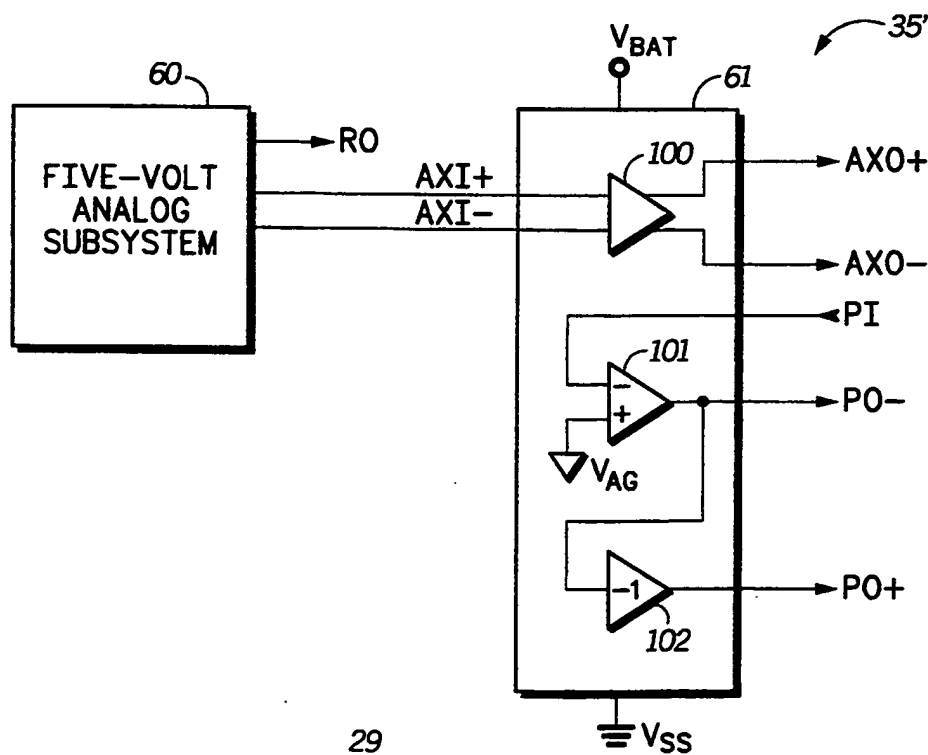
**[57] ABSTRACT**

A regulated charge pump (43) includes a charge pump core (114) having a charging capacitor (80). An output voltage on a first terminal (72) of the charging capacitor (80) is transferred to a holding capacitor (81). A second terminal (73) of the charging capacitor (80) is alternatively connected to positive and negative power supply voltage terminals in response to non-overlapping clock signals. The first terminal (72) of the charging capacitor (80) is connected through first (150) and second (151) transistors to the positive power supply voltage terminal. A proportional portion (112) provides a coarse regulation by biasing the first transistor (150) proportional to a comparison between a predetermined fraction of an output voltage and a reference voltage. An integrating portion (113) provides a precise regulation by biasing the second transistor (151) proportional to an integrated difference between the output voltage and a reference voltage.

**19 Claims, 4 Drawing Sheets**



20  
**FIG. 1**



29  
**FIG. 3**

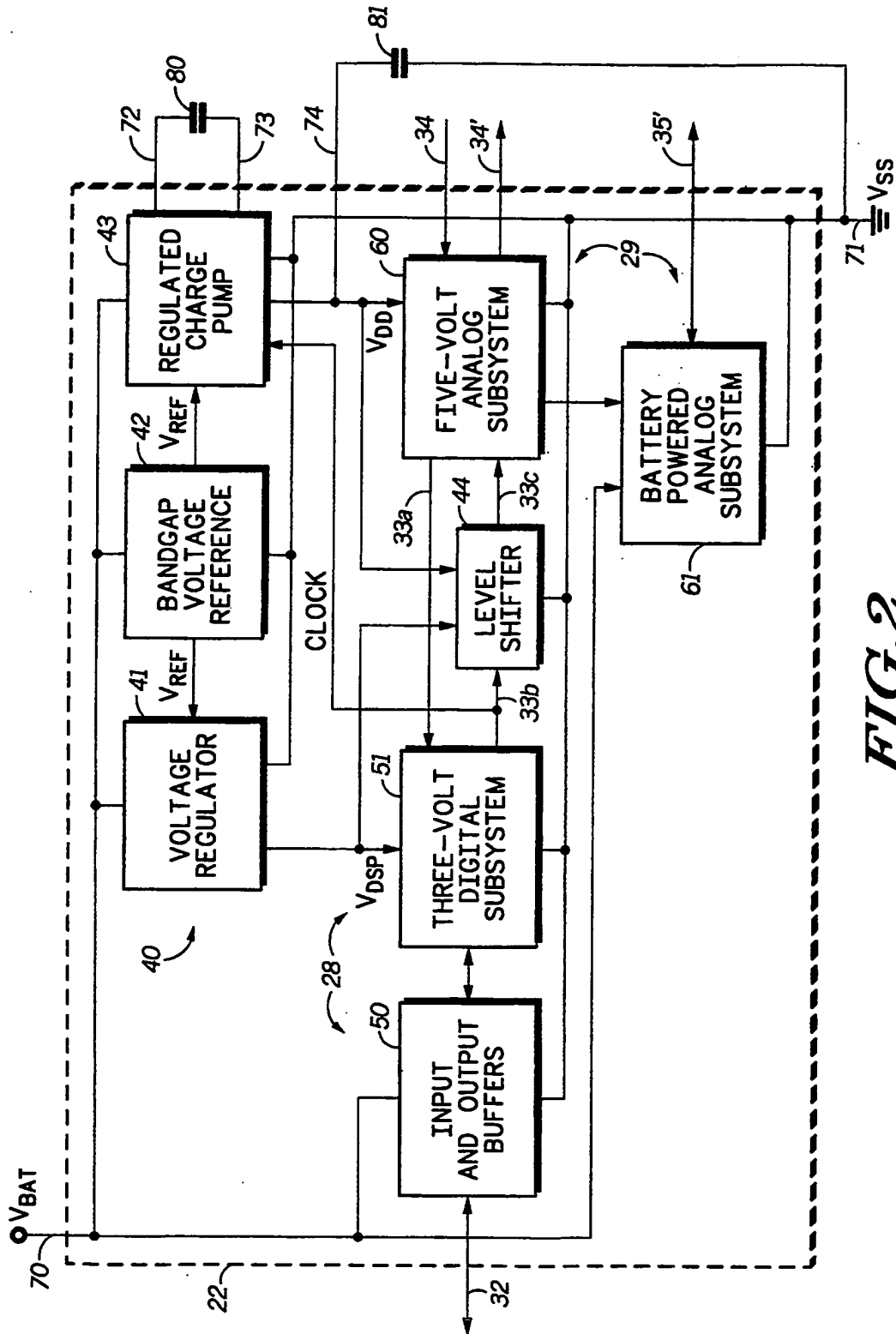
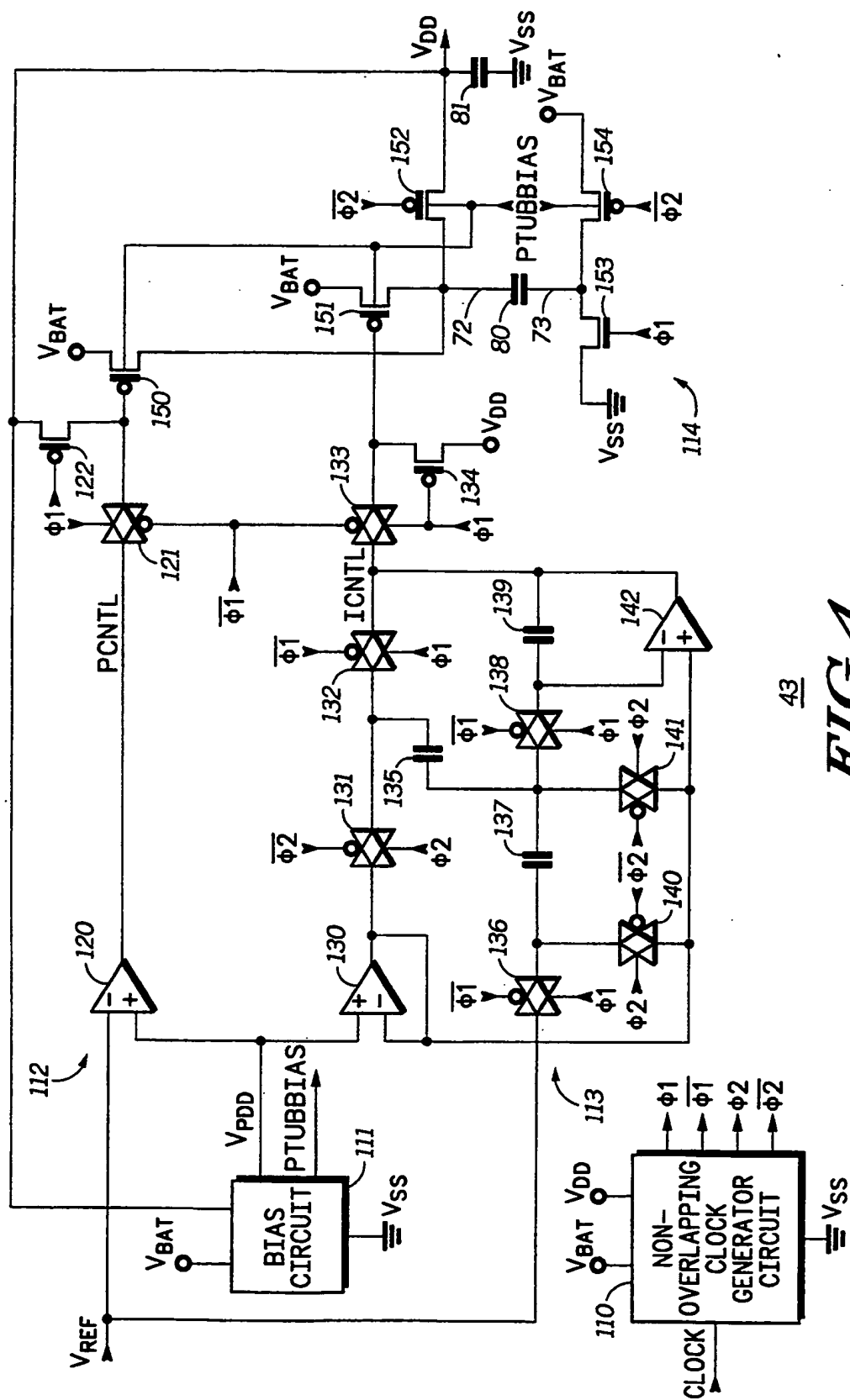
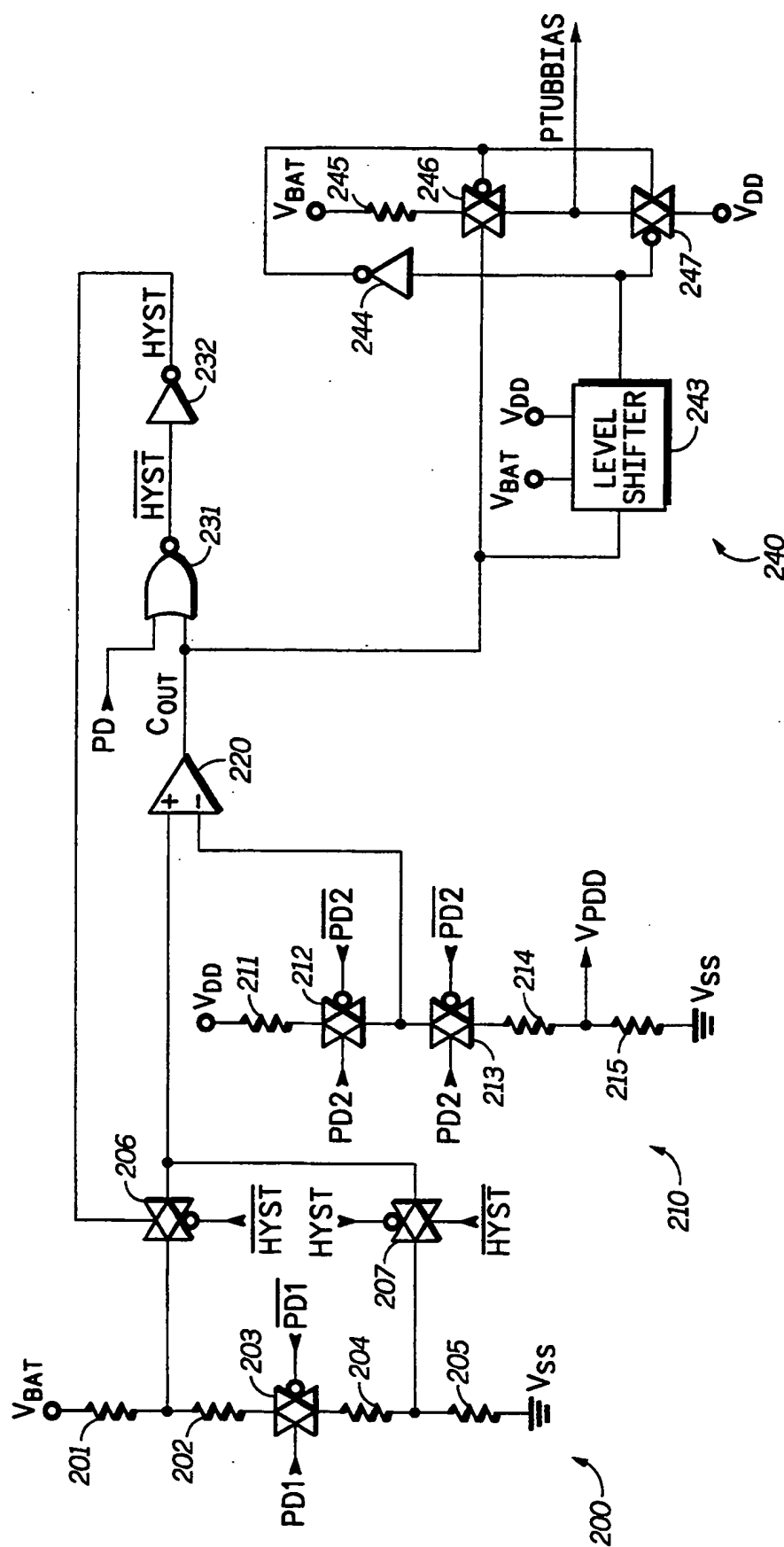


FIG. 2



**FIG. 4**



**FIG. 5**

## REGULATED CHARGE PUMP AND METHOD THEREFOR

### CROSS REFERENCE TO RELATED, COENDING APPLICATION

Related, copending application is application Ser. No. 07/788,977, filed concurrently herewith, by Luis A. Bonet et al., and assigned to the assignee hereof, entitled "Mixed Signal Processing System and Method of Powering Same".

#### 1. Field of the Invention

This invention relates generally voltage generator circuits, and more particularly, to regulated charge pump circuits.

#### 2. Background of the Invention

In some integrated circuits, it is necessary to increase an available power supply voltage to provide to internal circuitry. For example, electrically erasable programmable read only memories (EEPROMs) require a voltage substantially above the conventional +5.0-volt power supply to program a memory bit. An internal charge pump circuit increases the power supply voltage to the desired programming voltage. A conventional technique to increase the internal voltage is to use a voltage multiplier circuit. The voltage multiplier circuit is based on a charging capacitor and two phases of a clock. During one clock phase, the power supply voltage is applied to a first terminal of the charging capacitor while a second terminal is grounded. Then, during the second phase, the power supply voltage source is isolated from the first terminal of the charging capacitor. The second terminal is disconnected from ground, and the power supply voltage is applied to the second terminal. Thus, the first terminal of the charging capacitor is boosted to a voltage of twice the power supply voltage referenced to ground. This voltage, at the first terminal of the charging capacitor, is then used to charge a holding capacitor. At the end of the second clock phase, the first terminal of the charging capacitor is isolated from the holding capacitor and is again coupled to the power supply voltage. The voltage of the holding capacitor provides the charge-pumped voltage. This example demonstrated a voltage multiplier with an integer multiple of two; in the absence of loading, the charge-pumped voltage is equal to twice the power supply voltage. Other charge pump circuits have two such charge pumps connected in series to provide a voltage multiplier with an integer multiple of four.

A voltage-multiplying charge pump circuit may be useful also in battery-based systems. Since the battery voltage may be low, a charge pump circuit may be used to increase the voltage to internal circuitry. However, this creates problems. A battery voltage may vary widely between the time it is first used (either a new battery or a newly-recharged battery) and the time it goes dead. For example, three type AA batteries may be used to form a power supply with a nominal voltage of 3.75 volts, which is usually acceptable for integrated circuits which use the conventional +5.0 volt power supply. Before going dead, the battery voltage may fall to approximately 2.7 volts. Thus, a voltage-doubling charge pump circuit could be used to increase the 2.7-volt power supply voltage to 5.4 volts. However, when the batteries are new, each battery voltage may be as much as 1.8 volts, and the charge-pumped power supply voltage would be unacceptably high. For example, a voltage doubling charge pump would provide volt-

ages between 10.8 and 5.4 volts between recharges. A 10.8-volt power supply is harmful because reliability could be reduced in circuits designed to work at 5.0 volts. If complementary metal-oxidesemiconductor (CMOS) technology is used, gate rupture and latchup may occur. Thus, it is necessary to limit the power supply voltage to an acceptable level.

Several techniques are available to limit the voltage. A clamping device, such as a Zener diode, could be used to reduce the output voltage. The clamping device sinks current during the period of excess voltage to drop the voltage to the required level. Also, shunt regulation methods may be used to reduce the output voltage. However, in either case the charge pump wastes current through the Zener diode or regulation device. As more current is wasted, battery life shortens. Thus, techniques other than the use of passive devices to limit the voltage are needed.

### SUMMARY OF THE INVENTION

Accordingly, there is provided, in one form, a regulated charge pump comprising a charge pump core, proportional means, and integrating means. The charge pump core boosts a first voltage existing at a first terminal of a charging capacitor during a first predetermined time period, by an amount equal to a first power supply voltage referenced to a second power supply voltage during a second predetermined time period and provides a regulated charge-pumped voltage in response. The charge pump core comprises first and second transistors. The first transistor has a first current electrode for receiving the first power supply voltage, a control electrode, and a second current electrode coupled to the first terminal of the charging capacitor. The second transistor has a first current electrode for receiving the first power supply voltage, a control electrode, and a second current electrode coupled to the first terminal of the charging capacitor. The proportional means is coupled to the control electrode of the first transistor changes the first voltage proportionately in response to a difference between a reference voltage and a proportional voltage, by altering a conductivity of the first transistor the proportional voltage being a predetermined fraction of the regulated charge-pumped voltage, the predetermined fraction making the proportional voltage equal to the reference voltage when the regulated charge-pumped voltage is equal to a desired value. The integrating means is coupled to the control electrode of the second transistor, and further changes the first voltage proportionately in response to an integration of a difference between the proportional voltage and the reference voltage by altering a conductivity of the second transistor.

In another form, there is provided a method of providing a regulated charge-pumped voltage, comprising the steps of providing a charging capacitor; alternately, coupling a second terminal of the charging capacitor to a first power supply voltage terminal, or coupling the second terminal of the charging capacitor to a second power supply voltage terminal, respectively in response to first and second non-overlapping clock signals; providing the regulated charge-pumped voltage in response to a first voltage at a first terminal of the charging capacitor; forming a second voltage proportional to the regulated charge-pumped voltage; comparing the second voltage to a reference voltage; biasing a first transistor, coupled between the first power supply volt-

age terminal and a first terminal of the charging capacitor, to be conductive proportionally to a comparison of the second voltage to the reference voltage; integrating a difference between the second voltage and the reference voltage; and biasing a second transistor, coupled between the first power supply voltage terminal and the first terminal of the charging capacitor, to be conductive proportionally to an integrated difference between the second voltage and the reference voltage.

These and other features and advantages will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates in block form a digital cordless telephone handset utilizing a mixed signal processing system in accordance with the present invention.

FIG. 2 illustrates in partial block form and partial schematic form the mixed signal processing system of FIG. 1.

FIG. 3 illustrates in partial block form and partial schematic form the PCM codec of FIG. 2.

FIG. 4 illustrates in partial schematic form and partial block form the regulated charge pump of FIG. 2 in accordance with the present invention.

FIG. 5 illustrates in partial schematic form and partial block form the bias circuit used in the regulated charge pump of FIG. 4.

#### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates in block form a digital cordless telephone handset 20 utilizing a mixed signal processing system 22 in accordance with the present invention. Handset 20 implements a standard protocol, such as the U.K. Cordless Telephone, Second Generation (CT-2) or the Digital European Cordless Telephone (DECT) standard. For example, according to the CT-2 protocol, telephone signals are received and transmitted digitally in packets in a half-duplex or ping-pong scheme between handset 20 and a base station (not shown in FIG. 1). An antenna 24 is used for transmitting and receiving radio-frequency (RF) representations of telephonic signals. An RF system 25 is connected to antenna 24 for receiving and demodulating, and transmitting and modulating, digital streams of telephonic data. As used here, the term "signal" refers to a time-varying electrical signal, and the term "digital signal" refers to a series of digital samples of the signal. A "packet" includes a portion of the digital signal, or alternatively, a specified number of digital samples of the telephone signal, along with digital signalling bits.

A packet from the base station is received as a modulated RF signal on antenna 24. Radio frequency system 25 receives the RF signal and demodulates it. The modulation scheme is a two-level FSK shaped by an approximately Gaussian filter, as described in the CT-2 Common Air Interface Specification. The packet is then presented to a time division duplex block 26. Time division duplex block 26 splits the packet into its two constituent components, making the signalling bits available to microprocessor 27. Time division duplex block 26 makes the compressed digital signal available to mixed signal processing system 22 through input and output signals 32a. Subsequently, microprocessor 27 reads the signalling bits and performs associated signalling functions, such as call setup and disconnect.

Mixed signal processing system 22 includes an adaptive differential pulse code modulation (ADPCM) transcoder 28, and a pulse code modulation (PCM) coder-decoder (codec) 29. ADPCM transcoder 28 decompresses the compressed digital signal received from time division duplex block 26 by a conventional algorithm, such as the CCITT Recommendation G.721 or the American National Standard T1.301-1988. When decompressed, the digital signal exists as digital PCM data compressed by a conventional algorithm such as A-law or  $\mu$ -law. ADPCM transcoder is connected via input and output signals 32b to microprocessor 27. Microprocessor 27 initializes and controls the operation of ADPCM transcoder 28 through input and output signals 32b. PCM codec 29 receives the PCM data via input and output signals 33, performs A-law or  $\mu$ -law decompression to form an analog telephone signal, and provides the analog telephone signal to a speaker 31 and a ringer (not shown in FIG. 1) via output signals 35. Additional interface circuitry between ADPCM transcoder 28 and PCM codec 29 is not shown in FIG. 1.

A microphone 30 provides an analog telephone signal via input signal lines 34 to PCM codec 29. PCM codec 29 converts the analog telephone signal to a digital telephone signal and compresses it according to the A-law or  $\mu$ -law algorithm, and provides the digital telephone signal to ADPCM transcoder 28 via input and output signals 33. ADPCM transcoder 28 in turn compresses the digital telephone signal according to the conventional algorithm (such as the CCITT G.721 or ANSI T1.301-1988 standard) and provides the compressed digital signal to time division duplex block 26. Time division duplex block 26 then combines signalling bits from microprocessor 27 with the compressed digital data from ADPCM transcoder 28 to form a CT-2 packet. Time division duplex block 26 provides the CT-2 packet to radio frequency system 25, which modulates it and provides it as an RF signal to antenna 24, where it is radiated and eventually received by the base station. PCM codec 29 performs the function of a conventional integrated circuit, such as the Motorola MC145554 law PCM Codec-Filter or the Motorola MC145557 A-law PCM Codec-Filter. ADPCM transcoder 28 also performs the function of a conventional integrated circuit, such as the Motorola MC145532 ADPCM Transcoder.

PCM codec filter 29 is primarily analog, while ADPCM transcoder 28 is primarily digital; however, mixed signal processing system 22 is required to operate from a single battery power supply formed typically by three type AA batteries (not shown in FIG. 1). Mixed signal processing system 22 must operate on battery voltages varying from 2.7 volts to 5.25 volts and still meet the CT-2 specification. At the same time, power consumption must be kept to a minimum in order to maximize battery life. ADPCM transcoder 28 must perform its operation within the time required to process packets to operate on continuous, real-time speech signals. Also, reliable operation is required. Thus, a new approach which solves these problems is needed. Mixed signal processing system 22 satisfies these requirements as is now illustrated with reference to FIG. 2.

FIG. 2 illustrates in partial block form and partial schematic form mixed signal processing system 22 of FIG. 1. Mixed signal processing system 22 includes ADPCM transcoder 28 and PCM codec filter 29 as previously illustrated in FIG. 1. In addition, mixed signal processing system 22 includes a power supply



subsystem 40 having a voltage regulator 41, a bandgap voltage reference 42, and a regulated charge pump 43, a level shifter 44, and several power supply terminals and signal lines. The terminals include a terminal 70 for receiving a voltage labelled " $V_{BAT}$ ", a terminal 71 for receiving a voltage labelled " $V_{SS}$ ", a first capacitor terminal 72, a second capacitor terminal 73, and a third capacitor terminal 74. The signal lines include input and output signal lines 32, input signal lines 34, output signal lines 34', and input and output signal lines 35'. Signal lines corresponding to signal lines in FIG. 1 are given the same reference number. However, input and output signal lines 32 of FIG. 2 include input and output signal lines 32a and 32b as previously illustrated in FIG. 1, and input and output signal lines 35' include output signal line 35 of FIG. 1 and other input and output signal lines not shown in FIG. 1. ADPCM transcoder 28 includes input and output buffers 50, and a three-volt digital subsystem 51. PCM codec 29 includes a five-volt analog subsystem 60, and a battery-powered analog subsystem 61. A first capacitor 80 is connected between terminals 72 and 73, and a second capacitor 81 is connected between terminals 74 and 71.

$V_{BAT}$  is a battery voltage provided by, for example, three type AA nicad batteries (not shown in FIG. 2) having a nominal voltage of 3.75 volts but varying between 2.7 and 5.4 volts between recharges.  $V_{SS}$  is a common, or ground power supply voltage having a nominal value of zero volts. Thus, mixed signal processing system 22 is only connected to a single, battery-derived power supply. In power supply subsystem 40, bandgap voltage reference 42 is connected to  $V_{BAT}$  and  $V_{SS}$  and provides a stable, precise voltage labelled " $V_{REF}$ " in response. Bandgap voltage reference 42 is a bandgap voltage reference circuit which is able to operate at power supply voltages down to approximately 2.7 volts, such as is disclosed in patent application docket number SC-01229A, application number unknown, filed Oct. 28, 1991, by Greaves et al. and assigned to the assignee hereof, entitled "Bandgap Voltage Reference Circuit", which is herein incorporated by reference.

Voltage regulator 41 is connected between  $V_{BAT}$  and  $V_{SS}$ , and receives voltage  $V_{REF}$  to provide an internal reference. Voltage regulator 41 is a conventional CMOS voltage regulator which provides a regulated output voltage, labelled " $V_{DSP}$ ".  $V_{DSP}$  has a nominal value of 3.0 volts which remains substantially constant with variations in  $V_{BAT}$  until  $V_{BAT}$  approaches 3.0 volts. As  $V_{BAT}$  falls below 3.0 volts (when the voltage of the nicad batteries falls due to discharge),  $V_{DSP}$  likewise compresses.

Power supply subsystem 40 also includes regulated charge pump 43, which is connected between  $V_{BAT}$  and  $V_{SS}$ . Regulated charge pump 43 is connected to the first terminal of first capacitor 80 via terminal 72, to the second terminal of first capacitor 80 via terminal 73, and to the first terminal of second capacitor 81 via terminal 74, receives voltage  $V_{REF}$  and a clock signal labelled "CLOCK", and provides an output voltage labelled  $V_{DD}$ . Regulated charge pump 43 combines two conventional functions. First, regulated charge pump 43 increases the voltage of  $V_{BAT}$  through clocked capacitive charge pumping. In a preferred embodiment, mixed signal processing system 22 is included in a single monolithic integrated circuit. Capacitors 80 and 81 are too large to be provided monolithically and thus are external to the integrated circuit. Second, regulated charge pump 43 regulates the charge-pumped voltage to pro-

vide a voltage labelled " $V_{DD}$ ".  $V_{DD}$  has a nominal voltage of approximately 5.0 volts, but remains substantially constant as  $V_{BAT}$  changes (due to the regulation).

ADPCM transcoder 28 is a conventional ADPCM transcoder modified to separate internal circuitry in accordance with differing power supply requirements. In ADPCM transcoder 28, input and output buffers 50 are separated from three-volt digital subsystem 51 and are connected between  $V_{BAT}$  and  $V_{SS}$ , and provide and receive signals via input and output signal lines 32. Three-volt digital subsystem 51 performs all the functions of a conventional ADPCM transcoder except for the functions provided by input and output buffers 50. Subsystem 51 is connected between  $V_{DSP}$  and  $V_{SS}$ , connects to input and output buffers 50, receives input signals from five-volt analog subsystem 60, and provides output signals to level shifter 44 via signal lines 33b, one of which is signal CLOCK, which is also provided to regulated charge pump 43. Level shifter 44 receives power supply voltages  $V_{DSP}$  and  $V_{DD}$  and is coupled to  $V_{SS}$ , and level shifts the signals conducted on signal lines 33b and provides corresponding signals 33c to subsystem 60. PCM codec 29 is a conventional PCM codec modified to separate internal circuitry in accordance with differing power supply requirements. In PCM codec 29, five-volt analog subsystem 60 performs all the functions of a conventional PCM codec except the special functions performed by subsystem 61 as described below. Subsystem 60 is connected between  $V_{DD}$  and  $V_{SS}$ , receives a microphone signal via input signal lines 34, and connects to subsystem 51 via signal lines 33a. Battery-powered analog subsystem 61 is connected between  $V_{BAT}$  and  $V_{SS}$  and is connected to input and output signal lines 35'.

Mixed signal processing system 22 has several advantages over known mixed signal processing systems. First, mixed signal processing system 22 reduces power consumption. Voltage regulator 41 provides a power supply voltage,  $V_{DSP}$ , to subsystem 51 which is substantially constant with respect to changes in  $V_{BAT}$ . By setting the power supply voltage near the minimum voltage at which the circuitry will operate, power consumption of digital subsystem 51 is minimized. At the same time, digital subsystem 51 performs the ADPCM transcoder functions (except the input and output functions) quickly enough at ( $V_{DSP}$ =3.0 volts) to meet the specifications, including speech compression and decompression in real time. In a preferred embodiment, subsystem 51 uses CMOS digital logic. CMOS logic circuitry may be designed to operate at high speed and low power supply voltage, such as at 3.0 volts. However, such circuitry consumes large amounts of power when the power supply voltage is increased to around 4.0 or 5.0 volts, and in addition, integrated circuit area increases due to a need for additional area for power supply busses. At reduced power consumption levels, junction temperatures are reduced; thus, integrated circuit packaging specifications may be relaxed and reliability is enhanced. An added benefit is that digital subsystem 51 is designed to operate within a narrow range of power supply voltages, simplifying circuit design.

Second, mixed signal processing system 22 performs analog functions reliably despite changes in  $V_{BAT}$ . Regulated charge pump 43 provides a power supply voltage,  $V_{DD}$ , having a voltage high enough for desired analog operation. At  $V_{DD}$  of 5.0 volts, analog circuitry in analog subsystem 60 has sufficient headroom to oper-

ate linearly. In addition, harmfully high voltages provided by conventional integer charge pumping are avoided. As an example, if analog circuitry were powered directly from  $V_{BAT}$ , performance would diminish if  $V_{BAT}$  were near the low end of its range (about 2.7 volts). the other hand, if a standard 2X integer charge pump were used to power the analog circuitry, then the voltage range would be from 5.4 to about 10.8 volts. At the high end of the range, reliability is reduced.

Third, mixed signal processing system 22 reliably interfaces to external circuitry. Mixed signal processing system 22 separates input and output buffers 50 from digital subsystem 51. While digital subsystem 51 is connected to  $V_{DSP}$ , input and output buffers 50 are connected between  $V_{BAT}$  and  $V_{SS}$ . Thus, logic high output signal levels of input and output buffers 50 correspond to the output signal levels of other devices, such as microprocessor 27. As illustrated in FIG. 1, ADPCM codec 28 is connected both to time division duplex block 26 and to microprocessor 27. Internally, level shifter 44 similarly increases the logic levels of digital signals provided by digital subsystem 51 to analog subsystem 60.

Fourth, mixed signal processing system 22 reduces power consumption by powering analog subsystem 60 from  $V_{DD}$  and battery-powered output subsystem 61 from  $V_{BAT}$ . Circuitry in analog subsystem 61 includes drivers which require a high current drive. For example, subsystem 61 includes drivers to provide analog outputs to speaker 31 of FIG. 1. By separating the circuitry, efficiency losses introduced by regulated charge pump 43 do not include losses from the high current drivers.

FIG. 3 illustrates in partial block form and partial schematic form PCM codec 29. Illustrated in FIG. 3 is analog subsystem 60 and battery-powered analog subsystem 61, which includes amplifiers 100, 101, and 102. Analog subsystem 60 provides receive analog output signals labelled "RO", "AXI+", and "AXI-". AXI+ and AXI- form a differential representation of the analog output signal. In subsystem 61, amplifier 100 is a differential amplifier which receives signals AXI+ and AXI- on input terminals and provides a signal labelled "AXO+" on a positive output terminal thereof, and a signal labelled "AXO-" on a negative output terminal thereof. Amplifier 101 is an operational amplifier which receives an input signal labelled "PI" on a negative input terminal thereof, a signal voltage labelled " $V_{AG}$ " on a positive input terminal thereof, and provides a signal labelled "PO-".  $V_{AG}$  is an analog ground reference voltage which has a value of approximately  $V_{BAT}/2$ . Amplifier 102 is an inverting amplifier which receives signal PO- on an input terminal thereof, and provides a signal labelled "PO+" on an output terminal thereof. Signals AXO+ and AXO- may be used to drive an output device such as a ringer or the like (not shown in FIG. 1). Input signal PI typically receives signal RO and is used with external resistors to set the gain of push-pull signals PO+ and PO- provided by amplifiers 101 and 102. Amplifiers 101 and 102 are large enough to drive a telephone handset earpiece or small speaker. Powering subsystem 61 from  $V_{BAT}$ , instead of  $V_{DD}$ , reduces power consumption by preventing a large power loss due to the efficiency of regulated charge pump 43 being less than 100%.

FIG. 4 illustrates in partial schematic form and partial block form regulated charge pump 43 of FIG. 2 in accordance with the present invention. Regulated

charge pump 43 includes generally a non-overlapping clock generator circuit 110, a bias circuit 111, a proportional portion 112, an integrating portion 113, and a charge pump core 114. Proportional portion 112 includes an amplifier 120, a transmission gate 121, and a P-channel transistor 122. Integrating portion 113 includes an amplifier 130, transmission gates 131, 132, and 133, a P-channel transistor 134, a capacitor 135, a transmission gate 136, a capacitor 137, a transmission gate 138, a capacitor 139, transmission gates 140 and 141, and an amplifier 142. Charge pump core 114 includes capacitor 80, P-channel transistors 150, 151, and 152, an N-channel transistor 153, a P-channel transistor 154, and capacitor 81.

Non-overlapping clock circuit 110 receives signal CLOCK, is coupled to power supply voltages  $V_{BAT}$ ,  $V_{DD}$ , and  $V_{SS}$ , and provides non-overlapping clock signals labelled " $\Phi 1$ ", " $\Phi 1$ ", " $\Phi 2$ ", and " $\Phi 2$ ", which are level-shifted to  $V_{DD}$ . Bias circuit 111 is coupled between power supply terminals  $V_{BAT}$  and  $V_{SS}$ , receives power supply voltage  $V_{DD}$ , and provides an output signal labelled " $V_{PDD}$ " and an output signal labelled "PTUBBIAS".

In proportional portion 112, amplifier 120 is an operational transconductance amplifier (OTA) having a negative input terminal for receiving signal  $V_{REF}$ , a positive input terminal for receiving signal  $V_{PDD}$ , and an output terminal for providing a signal labelled "PCNTL". Transmission gate 121 has a first current terminal for receiving signal PCNTL, a second current terminal, a positive control terminal for receiving signal  $\Phi 1$ , and a negative control terminal for receiving signal  $\Phi 1$ . Transistor 122 has a source for receiving power supply voltage  $V_{DD}$ , a gate for receiving signal  $\Phi 1$ , and a drain connected to the second current terminal of transmission gate 121.

In integrating portion 113, amplifier 130 has a positive input terminal for receiving signal  $V_{PDD}$ , a negative input terminal, and an output terminal connected to the negative input terminal of amplifier 130. Transmission gate 131 has a first current terminal connected to the output terminal of amplifier 130, a second current terminal, a positive control terminal for receiving signal  $\Phi 2$ , and a negative control terminal for receiving signal  $\Phi 2$ . Transmission gate 132 has a first current terminal connected to the second current terminal of transmission gate 131, a second current terminal for providing a signal labelled "ICNTL", a positive control terminal for receiving signal  $\Phi 1$ , and a negative control terminal for receiving signal  $\Phi 1$ . Transmission gate 133 has a first current terminal for receiving signal ICNTL, a second current terminal, a positive control terminal for receiving signal  $\Phi 1$ , and a negative control terminal for receiving signal  $\Phi 1$ . Transistor 134 has a source for receiving power supply voltage  $V_{DD}$ , a gate for receiving signal  $\Phi 1$ , and a drain connected to the second current terminal of transmission gate 133. Capacitor 135 has a first terminal connected to the second current terminal of transmission gate 131, and a second terminal. Transmission gate 136 has a first current terminal for receiving signal  $V_{REF}$ , a second current terminal, a positive control terminal for receiving signal  $\Phi 1$ , and a negative control terminal for receiving signal  $\Phi 1$ . Capacitor 137 has a first terminal connected to the second current terminal of transmission gate 136, and a second terminal connected to the second terminal of capacitor 135. Transmission gate 138 has a first current terminal connected to the second terminals of capacitors 135 and

137, a second current terminal, a positive control terminal for receiving signal  $\Phi 1$ , and a negative control terminal for receiving signal  $\Phi 1$ . Capacitor 139 has a first terminal connected to the second current terminal of transmission gate 138, and a second terminal connected to the second current terminal of transmission gate 132. Transmission gate 140 has a first current terminal connected to the output terminal of amplifier 130, a second current terminal connected to the second current terminal of transmission gate 136, a positive control terminal for receiving signal  $\Phi 2$ , and a negative control terminal for receiving signal  $\Phi 2$ . Transmission gate 141 has a first current terminal connected to the output terminal of amplifier 130, a second current terminal connected to the second terminals of capacitors 135 and 137, a positive control terminal for receiving signal  $\Phi 2$ , and a negative control terminal for receiving signal  $\Phi 2$ . Amplifier 142 has a negative input terminal connected to the second current terminal of transmission gate 138, a positive input terminal connected to the output terminal of amplifier 130, and an output terminal connected to the second current terminal of transmission gate 132 and to the second terminal of capacitor 139.

In charge pump core 114, transistor 150 has a source connected to  $V_{BAT}$ , a gate connected to the second current terminal of transmission gate 121, a drain, and a bulk or well receiving signal PTBUBIAS. Transistor 151 has a source connected to  $V_{BAT}$ , a gate connected to the second current terminal of transmission gate 133, a drain connected to the drain of transistor 150 at terminal 72, and a bulk or well receiving signal PTUBBIAS. Transistor 152 has a first current electrode connected to the drains of transistors 150 and 151, a gate for receiving signal  $\Phi 2$ , a second current electrode for providing power supply voltage  $V_{DD}$ , and a bulk or well receiving signal PTUBBIAS. Note that which current electrode is designated as source or drain depends on the voltages applied. Capacitor 80 has a first terminal connected to terminal 72, and a second terminal connected to terminal 73, as previously illustrated. Transistor 153 has a drain connected to the second terminal of capacitor 80 at node 73, a gate for receiving signal  $\Phi 1$ , and a source connected to  $V_{SS}$ . Transistor 154 has a source connected to power supply voltage  $V_{BAT}$ , a gate for receiving signal  $\Phi 2$ , a drain connected to the drain of transistor 153, and a bulk or well connected to PTUBBIAS. Capacitor 81 has a first terminal connected to the second current electrode of transistor 152 via terminal 74, and a second terminal connected to  $V_{SS}$ , as previously illustrated.

Circuit 110 is a conventional non-overlapping clock generator circuit which receives signal CLOCK, and provides four clock signals labelled  $\Phi 1$ ,  $\Phi 1$ ,  $\Phi 2$ , and  $\Phi 2$ , which are level shifted to  $V_{DD}$ . Because of the non-overlap, signal  $\Phi 1$  is not the same as signal  $\Phi 2$ , and signal  $\Phi 2$  is not the same as signal  $\Phi 1$ . As previously illustrated with respect to FIG. 2, capacitors 80 and 81 are coupled to regulated charge pump circuit 43 via terminals 72 and 73, and 74 and 71, respectively. Although capacitors 80 and 81 may be viewed as integral parts of regulated charge pump 43, they are preferably external to an integrated circuit which includes regulated charge pump 43 because of their required size. For example, in the illustrated embodiment, capacitors 80 and 81 have values of approximately 0.1 and 1.0 microfarads, respectively, and thus it is impractical to build such capacitors on an integrated circuit.

Charge pump core 114 uses charging capacitor 80 to provide voltage  $V_{DD}$  above voltage  $V_{BAT}$ . However, proportional portion 112 and integrating portion 113 alter the operation of charge pump core 114 to integrally regulate  $V_{DD}$ . During  $\Phi 1$  ( $\Phi 1$  is active), transistor 153 is conductive and couples the second terminal of capacitor 80 to  $V_{SS}$ . In a conventional charge pump design, a single transistor would also couple the first terminal of capacitor 80 to  $V_{BAT}$  during  $\Phi 1$ .  $\Phi 2$  makes transistor 152 nonconductive, isolating the first terminal of capacitor 81 from  $V_{DD}$ . Thus, during  $\Phi 1$ ,  $V_{DD}$  is maintained by holding capacitor 81. Transistor 154 is also nonconductive. However, during  $\Phi 2$  ( $\Phi 2$  active), transistor 153 is inactive, and transistor 154 is conductive and connects the second terminal of capacitor 80 to  $V_{BAT}$ . This action boosts the voltage at the first terminal of capacitor 80 to approximately twice  $V_{BAT}$ . Transistor 152 is also conductive, and the charge stored in capacitor 80 is dumped into holding capacitor 81. At the end of  $\Phi 2$ , transistor 152 becomes nonconductive and holding capacitor 81 maintains the level of  $V_{DD}$ . By repeating this operation, capacitor 81 eventually charges up to approximately twice  $V_{BAT}$ .

However, in regulated charge pump circuit 43, the conventional transistor from the first terminal of capacitor 80 to  $V_{BAT}$  is replaced by transistors 150 and 151. Transistors 150 and 151 are made conductive in response to signals PCNTL and ICNTL, which are provided by proportional portion 112 and integrating portion 113. Amplifiers 120 and 142 have outputs reference to  $V_{DD}$ , whereas amplifier 130 has an output referenced to  $V_{BAT}$ . Proportional portion 112 makes transistor 150 proportionately conductive in response to a comparison of  $V_{PDD}$  and  $V_{REF}$ . Portion 112 has a fast response to bring  $V_{DD}$  to approximately a desired voltage. Integrating portion 113, however, operates somewhat slower to make transistor 151 proportionately conductive to bring  $V_{DD}$  very close to the desired value. Thus, regulated charge pump 43 charge pumps  $V_{BAT}$  and regulates the charge-pumped voltage to efficiently provide  $V_{DD}$  at the desired voltage (+5.0 volts).

Bias circuit 111 provides  $V_{PDD}$  at a predetermined fraction of a desired value of  $V_{DD}$ ; the predetermined fraction is that fraction that makes  $V_{PDD}$  equal to  $V_{REF}$  when  $V_{DD}$  is equal to its desired value. In the illustrated embodiment, the desired value of  $V_{DD}$  is +5.0 volts, and the value of  $V_{REF}$  is approximately 1.25 volts. Thus, in order to make  $V_{PDD}$  equal to 1.25 volts when  $V_{DD}$  is 5.0 volts, a fraction of 0.25 is applied. The accuracy of the fraction is determined by the technique used to generate it, which is described with reference to FIG. 5 below.

Amplifier 120 compares  $V_{REF}$  to  $V_{PDD}$ . In the illustrated embodiment, amplifier 120 is an operational transconductance amplifier (OTA), whose output voltage varies in response to a difference in voltage between the positive and negative input terminals. The gate of transistor 150 provides a capacitive load, with transistor 122 providing a pullup to  $V_{DD}$ . During  $\Phi 1$ , transmission gate 121 is active to pass the signal PCNTL at the output of amplifier 120 to the gate of transistor 150. Amplifier 120 varies signal PCNTL until the voltages at the positive and negative input terminals are equal; thus, amplifier 120 makes transistor 150 differentially more or less conductive until  $V_{DD}$  is approximately equal to its desired voltage. Proportional portion 112 operates very quickly in response to changes in load conditions on

$V_{DD}$ ; however, amplifier 120 and transmission gate 121 introduce offsets which limit the accuracy of  $V_{DD}$ .

Integrating portion 113 adjusts the conductivity of transistor 151 to further increase the accuracy of  $V_{DD}$ . Integrating portion 113 is a switched capacitor (switched-C) differential integrator which integrates a difference between  $V_{PDD}$  and  $V_{REF}$  over time. While slower in response than proportional portion 112, integrating portion 113 includes the history of the signal levels, which eventually cancels the offset error of proportional portion 112. Amplifier 130 is a unity-gain differential amplifier which buffers signal  $V_{PDD}$  and keeps integrating portion 113 from affecting the operation of proportional portion 112. At power up, signals PCNTL and ICNTL are low in potential, making transistors 150 and 151 strongly conductive to reach the desired value of  $V_{DD}$  quicker. Because of battery life reduction and a voltage drop in the power supply voltages due to a rapid change in current, known as a di/dt voltage drop, it is important to include a resistance in series with the gates of transistors 150 and 151 to decrease the switching speed somewhat (not shown in FIG. 4).

Regulated charge pump 43 provides  $V_{DD}$  at a desired value of approximately 5.0 volts without having to first charge pump the battery voltage to a multiple thereof, and then to regulate or clamp the charge-pumped voltage to a desired, lower voltage. This regulation can be very advantageous for some values of  $V_{BAT}$ . For example, immediately after recharge,  $V_{BAT}$  may be approximately 5.4 volts. A conventional voltage-doubling charge pump circuit provides a voltage of 10.8 volts, which may be harmful to circuitry designed to operate at 5.0 volts. Furthermore, conventional methods of shunt regulation or clamping also waste current. Regulated charge pump 43 provides regulation such that  $V_{DD}$  is never doubled. Regulated charge pump 43 also does not use clamping devices such as Zener diodes to limit the output voltage, but rather uses proportional and integrating action to provide  $V_{DD}$  with high accuracy and high efficiency.

FIG. 5 illustrates in partial schematic form and partial block form bias circuit 111 used in regulated charge pump 43 of FIG. 4. Bias circuit 111 includes generally a first resistor string circuit 200, a second resistor string circuit 210, a comparator 220, a hysteresis control circuit 230, and a bias generator circuit 240. First resistor string circuit 200 includes resistors 201 and 202, a transmission gate 203, resistors 204 and 205, and transmission gates 206 and 207. Second resistor string circuit 210 includes a resistor 211, transmission gates 212 and 213, and resistors 214 and 215. Hysteresis control circuit 230 includes a NOR gate 231 and an inverter 232. Bias generator circuit 240 includes a level shifter 243, an inverter 244, a resistor 245, and transmission gates 246 and 247.

In first resistor string circuit 200, resistor 201 has a first terminal connected to  $V_{BAT}$ , and a second terminal. Resistor 202 has a first terminal connected to the second terminal of resistor 201, and a second terminal. Transmission gate 203 has a first current terminal connected to the second terminal of resistor 202, a second current terminal, a positive control terminal for receiving a signal labelled "PD1", and a negative control terminal for receiving a signal labelled "PD1". Resistor 204 has a first terminal connected to the second current terminal of transmission gate 203, and a second terminal. Resistor 205 has a first terminal connected to the second terminal of resistor 204, and a second terminal connected to  $V_{SS}$ .

Transmission gate 206 has a first current terminal connected to the second terminal of resistor 201, a second current terminal, a positive control terminal for receiving a signal labelled "HYST", and a negative control terminal for receiving a signal labelled "HYST". Transmission gate 207 has a first current terminal connected to the second terminal of resistor 204, a second current terminal connected to the second current terminal of transmission gate 206, a positive control terminal for receiving signal  $\overline{\text{HYST}}$ , and a negative control terminal for receiving signal HYST.

In second resistor string circuit 210, resistor 211 has a first terminal for receiving power supply voltage  $V_{DD}$ , and a second terminal. Transmission gate 212 has a first current terminal connected to the second terminal of resistor 211, a second current terminal, a positive control terminal for receiving a signal labelled "PD2", and a negative control terminal for receiving a signal labelled  $\overline{\text{PD2}}$ . Transmission gate 213 has a first current terminal connected to the second current terminal of transmission gate 212, a second current terminal, a positive control terminal for receiving signal PD2, and a negative control terminal for receiving signal  $\overline{\text{PD2}}$ . Resistor 214 has a first terminal connected to the second current terminal of transmission gate 213, and a second terminal for providing signal  $V_{PDD}$ . Resistor 215 has a first terminal connected to the second terminal of resistor 214, and a second terminal connected to  $V_{SS}$ .

Comparator 220 has a positive input terminal connected to the second current terminal of transmission gate 206, a negative input terminal connected to the second current terminal of transmission gate 212, and an output terminal for providing a signal labelled "COUT". In hysteresis control circuit 230, NOR gate 231 has a first input terminal for receiving a signal labelled "PD", a second input terminal connected to the output terminal of comparator 220 for receiving signal COUT thereon, and an output terminal for providing signal HYST. Inverter 232 has an input terminal connected to the output terminal of NOR gate 231, and an output terminal for providing signal  $\overline{\text{HYST}}$ .

In bias generator circuit 240, level shifter 243 is connected to the output terminal of comparator 220, and provides an output signal on an output terminal thereof. Inverter 244 has an input terminal connected to the output terminal of level shifter 243, and an output terminal. Resistor 245 has a first terminal connected to  $V_{BAT}$ , and a second terminal. Transmission gate 246 has a first current terminal connected to the second terminal of resistor 245, a second current terminal for providing signal PTUBBIAS, a positive control terminal connected to the output terminal of comparator 220, and a negative control terminal connected to the output terminal of inverter 244. Transmission gate 247 has a first current terminal connected to the second current terminal of transmission gate 246, a second current terminal for receiving power supply voltage  $V_{DD}$ , a positive control terminal connected to the output terminal of inverter 244, and a negative control terminal connected to the output terminal of level shifter 243.

Bias circuit 111 performs two functions. First, bias circuit 111 provides signal  $V_{PDD}$  for use in the proportional and integrating functions of regulated charge pump 43. Second, bias circuit 111 provides signal PTUBBIAS to bias the bulk or well of P-channel transistors in regulated charge pump 43, namely transistors 150, 151, 152, and 154, with  $V_{BAT}$  or  $V_{DD}$ , whichever is greater. In order to understand the remainder of the

operation, it is first necessary to describe the control signal generation. Signal PD is a powerdown indication active at a logic high. Signal PD1 is equivalent to a logical AND of signals PD and *COUT* and is active at a logic low. Signal PD2 is equivalent to signal PD1 but is level-shifted to *VDD* and is active at a logic low.

Resistor string circuit 210 performs the first function of providing signal *V<sub>PDD</sub>*. When control signals PD2 and PD2 are inactive, *V<sub>PDD</sub>* is provided as the product of a resistive voltage division between resistors 211, 214, and 215. Thus,

$$V_{PDD} = V_{DD}(R_{215}/(R_{211} + R_{214} + R_{215}))$$

where *R<sub>211</sub>* is the resistance of resistor 211, *R<sub>214</sub>* is the resistance of resistor 214, and *R<sub>215</sub>* is the resistance of resistor 215. By choosing proper resistor values, *V<sub>PDD</sub>* can be made equal to 0.25*V<sub>DD</sub>*; thus, for a value of *V<sub>DD</sub>*=5.0 volts, *V<sub>PDD</sub>* is equal to 1.25 volts. When regulated charge pump 43 alters *V<sub>DD</sub>* until *V<sub>REF</sub>*=*V<sub>PDD</sub>*, and since *V<sub>REF</sub>*=1.25 volts, resistor string circuit 210 assures that *V<sub>DD</sub>* is equal to 5.0 volts with high accuracy.

It is important to provide relatively high values for resistors 211, 214, and 215 to limit the current flowing therethrough. In order to provide the high resistances, lightly-doped diffusion or well resistors are preferred. These resistors are preferable to polysilicon resistors because, although polysilicon resistors are more accurate, they require much more circuit area. For example, a typical resistivity of a polysilicon resistor is approximately 20 ohms per square, whereas the resistivity of a well resistor is approximately 1.4 kilohms per square. In the preferred embodiment, *R<sub>211</sub>* is 105 kilohms, *R<sub>214</sub>* is 53.2 kilohms, and *R<sub>215</sub>* is 51.8 kilohms. Thus, low current flow is assured.

The second function of bias circuit 111 is to provide voltage PTUBBIAS in order to assure reliable operation of regulated charge pump 43 under varying power supply conditions, such as during power up. Immediately after power up, *V<sub>DD</sub>* has not yet attained its target value of 5.0 volts and may in fact be very close to zero. If N-wells were always biased to *V<sub>DD</sub>*, then immediately after power up a diffusion-to-well PN junction may become forward biased, which would be harmful to the integrated circuit. Thus, bias generator circuit 240 provides PTUBBIAS at a voltage of essentially *V<sub>BAT</sub>* when either *V<sub>BAT</sub>* is greater than *V<sub>DD</sub>* or when signal PD is active.

In order to compare *V<sub>DD</sub>* to *V<sub>BAT</sub>*, resistor string circuit 200 performs a similar voltage division as resistor string circuit 210. There is one difference, however. Resistor string circuit 200 includes hysteresis. After powerup (PD is inactive), when the battery voltage *V<sub>BAT</sub>* exceeds *V<sub>DD</sub>*, signal *COUT* is activated. Since PD is inactive, hysteresis control circuit 230 activates signal HYST at a logic low, and activates signal HYST at a logic high, making transmission gate 206 active and transmission gate 207 inactive. Thus, the voltage proportional to *V<sub>BAT</sub>* applied to the positive input terminal of comparator 220 is taken from the second terminal of resistor 201 in resistor string circuit 200. However, as soon as *V<sub>PDD</sub>* exceeds the potential of the second terminal of resistor 201, *COUT* becomes negated. Hysteresis control circuit 230 inactivates HYST at a logic high, and inactivates signal HYST at a logic low. Transmission gate 206 is inactive, and transmission gate 207 is active and the proportional voltage is now taken from the second terminal of resistor 204. Since now an additional

voltage drop is introduced by resistors 202 and 204, *V<sub>DD</sub>* must decrease by an additional amount before *COUT* is again activated. Thus, the hysteresis provided by bias circuit 111 prevents instability under varying power supply conditions.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. For example, *V<sub>SS</sub>* could be the positive power supply with the other power supply voltages *V<sub>BAT</sub>*, *V<sub>DD</sub>*, and *V<sub>DSP</sub>* at negative voltages in reference thereto. Furthermore, although battery voltage *V<sub>BAT</sub>* was illustrated, mixed signal processing system 22 provides the same advantages when any highly variable power supply voltage is used. In addition, a different number and type of batteries may be used, as long as the voltage during the operating life is at least 2.7 volts. In another embodiment, a portion of digital subsystem 51 may be coupled to *V<sub>DD</sub>* to maximize speed. Also, *V<sub>DD</sub>* could be generated by a switching regulator, also called a switch mode regulator. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

I claim:

1. A regulated charge pump comprising:

a charge pump core for boosting a first voltage existing at a first

terminal of a charging capacitor during a first

predetermined time period, by an amount equal to a first

power supply voltage referenced to a second power supply

voltage during a second predetermined time period, and

providing a regulated charge-pumped voltage in response,

said charge pump core comprising first and second transistors;

said first transistor having a first current electrode for receiving

said first power supply voltage, a control electrode, and a

second current electrode coupled to said first terminal of

said charging capacitor;

said second transistor having a first current electrode for

receiving said first power supply voltage, a control electrode, and a second current electrode coupled to said

first terminal of said charging capacitor;

proportional means coupled to said control electrode of said first

transistor, for changing said first voltage proportionately

in response to a difference between a reference voltage and a proportional voltage by altering a

conductivity of said first transistor, said proportional

voltage being a predetermined fraction of said regulated

charge-pumped voltage, said predetermined fraction

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making said proportional voltage equal to said reference voltage when said regulated charge-pumped voltage is equal to a desired value; and  
 5 integrating means coupled to said control electrode of said second transistor, for further changing said first voltage proportionately in response to an integration of a difference between said proportional voltage and said reference voltage by altering a conductivity of said second transistor.  
 10 2. The regulated charge pump of claim 1 wherein said charge pump core comprises storing means coupled to said first terminal of said charging capacitor, for storing a voltage at said first terminal of said charging capacitor during said second predetermined time period.  
 15 3. The regulated charge pump of claim 2 wherein said storing means comprises:  
 a holding capacitor having a first terminal for providing said regulated charge-pumped voltage thereon, and a second terminal for receiving said second power supply voltage;  
 20 and  
 coupling means for coupling said first terminal of said charging capacitor to said first terminal of said holding capacitor during said second predetermined time period.  
 25 4. The regulated charge pump of claim 1 wherein said charge pump core further comprises:  
 a third transistor having a first current electrode coupled to a second terminal of said charging capacitor, and a second current electrode for receiving said second power supply voltage, said third transistor conductive during said first predetermined time period; and  
 30 a fourth transistor having a first current electrode for receiving said first power supply voltage, and a second current electrode coupled to said second terminal of said charging capacitor, said fourth transistor conductive during said second predetermined time period.  
 35 5. The regulated charge pump of claim 4 further comprising biasing means for biasing a bulk of said first, second, and fourth transistors at a higher one of either said first power supply voltage or said regulated charge-pumped voltage.  
 40 6. The regulated charge pump of claim 6 wherein said biasing means comprises:  
 means for providing first and second voltages of said biasing means respectively at first and second fractions of said first power supply voltage;  
 45 means for providing a third voltage of said biasing means at a

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third fraction of said regulated charge-pumped voltage;  
 a comparator having a positive input terminal, a negative input terminal, and an output terminal for providing a compare output signal;  
 5 means for coupling said first voltage of said biasing means to said positive input terminal of said comparator in response to said compare output signal, and for coupling said second voltage of said biasing means to said positive input terminal of said comparator otherwise; and  
 10 means for providing said first power supply voltage as a bulk bias voltage in response to said compare output signal, and for providing said regulated charge-pumped voltage as said bulk bias signal otherwise.  
 15 7. The regulated charge pump of claim 1 wherein said proportional means comprises means for making said first transistor nonconductive during a third predetermined time period, and wherein said integrating means comprises means for making said second transistor nonconductive during said third predetermined time period, said third predetermined time period occurring other than during said first predetermined time period.  
 20 8. The regulated charge pump of claim 1 wherein said reference voltage is characterized as being a bandgap reference voltage.  
 9. The regulated charge pump of claim 1 wherein said proportional means comprises a comparator having a first input terminal for receiving said reference voltage, a second input terminal for receiving said proportional voltage, and an output terminal, said proportional means changing said voltage at said first terminal of said charging capacitor in response to a voltage at said output terminal of said comparator.  
 25 10. The regulated charge pump of claim 1 wherein said first and second transistors each comprises a P-channel MOS transistor.  
 11. The regulated charge pump of claim 1 wherein said proportional means alters said conductivity of said first transistor during said first predetermined time period, and wherein said integrating means alters said conductivity of said second transistor during said first predetermined time period.  
 30 12. A regulated charge pump comprising:  
 a charge pump core comprising:  
 a charging capacitor having first and second terminals;  
 35 means for selectively coupling said second terminal of said charging capacitor to a first power supply voltage terminal in response to a first clock signal;  
 means for selectively coupling said second terminal of said charging capacitor to a second power supply voltage terminal in response to a second clock signal;  
 40 a first transistor having a first current electrode coupled to said first power supply voltage terminal, a control

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electrode, and a second current electrode coupled to said first terminal of said charging capacitor; a second transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode, and a second current electrode coupled to said first terminal of said charging capacitor; and means for storing a voltage existing at said first terminal of said charging capacitor in response to said second clock signal, and for providing a regulated charge-pumped voltage in response thereto; bias means for providing a proportional voltage as a predetermined proportion of said regulated charge-pumped voltage, said predetermined proportion being such that said proportional voltage is equal to a reference voltage when said regulated charged-pumped voltage has a predetermined value; proportional means for comparing said proportional voltage to said reference voltage and making said first transistor conductive in response; and integrating means for integrating a difference between said proportional voltage and said reference voltage and for making said second transistor proportionately conductive in response.

13. The regulated charge pump of claim 12 wherein said proportional means comprises: an operational transconductance amplifier having a positive input terminal for receiving said proportional voltage, a negative input terminal for receiving said reference voltage, and an output terminal; a transmission gate having a first terminal coupled to said output terminal of said operational transconductance amplifier, and a second terminal coupled to said control electrode of said first transistor, said transmission gate made conductive in response to said first clock signal.

14. The regulated charge pump of claim 12 wherein said integrating means comprises: an amplifier having a positive input terminal for receiving said proportional voltage, a negative input terminal, and an output terminal coupled to said negative input terminal thereof; a switched capacitor integrator coupled to said amplifier for providing an output voltage in response to an integration

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of said difference between said proportional voltage and said reference voltage; and a first transmission gate having a first terminal for receiving said output voltage of said switched capacitor integrator, and a second terminal coupled to said control electrode of said second transistor, said first transmission gate made conductive in response to said first clock signal.

15. A method of providing a regulated charge-pumped voltage comprising the steps of: providing a charging capacitor; alternately, coupling a second terminal of said charging capacitor to a first power supply voltage terminal, or coupling said second terminal of said charging capacitor to a second power supply voltage terminal, respectively in response to first and second non-overlapping clock signals; providing the regulated charge-pumped voltage in response to a first voltage at a first terminal of said charging capacitor; forming a second voltage proportional to the regulated charge-pumped voltage; comparing said second voltage to a reference voltage; biasing a first transistor, coupled between said first power supply voltage terminal and a first terminal of said charging capacitor, to be conductive proportionally to a comparison of said second voltage to said reference voltage; integrating a difference between said second voltage and said reference voltage; and biasing a second transistor, coupled between said first power supply voltage terminal and said first terminal of said charging capacitor, to be conductive proportionally to an integrated difference between said second voltage and said reference voltage.

16. A circuit for providing a bulk bias voltage comprising: means for providing first and second voltages respectively at first and second fractions of a first power supply voltage; means for providing a third voltage at a third fraction of a second power supply voltage; a comparator having a positive input terminal, a negative input terminal, and an output terminal for providing a compare output signal in either a first state in response to a voltage at said positive input terminal exceeding a voltage at said negative input terminal, or in a second



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state in response to said voltage at said negative input terminal exceeding said voltage at said positive input terminal;  
 means for coupling said first voltage to said positive input terminal of said comparator in response to said compare output signal being in said first state, and for coupling said second voltage to said positive input terminal of said comparator in response to said compare output signal being in said second state; and  
 means for providing said first power supply voltage as the bulk bias voltage in response to said compare output signal being in said first state, and for providing said second power supply voltage as said bulk bias voltage in response to said compare output signal being in said second state.

17. The circuit of claim 16 wherein said means for providing said first and second voltages comprises:  
 a first resistor having a first terminal for receiving said first power supply voltage, and a second terminal for providing said first voltage;  
 a second resistor having a first terminal coupled to said second terminal of said first resistor, and a second terminal;  
 a transmission gate having a first terminal connected to said second terminal of said second resistor, and a second terminal, and made conductive in response to a powerdown signal;

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a third resistor having a first terminal coupled to said second terminal of said transmission gate, and a second terminal for providing said second voltage; and  
 a fourth resistor having a first terminal coupled to said second terminal of said third resistor, and a second terminal for receiving a third power supply voltage.

18. The circuit of claim 16 wherein said means for providing said third voltage comprises:  
 a first resistor having a first terminal for receiving said second power supply voltage, and a second terminal;  
 a first transmission gate having a first terminal connected to said second terminal of said first resistor, and a second terminal connected to said negative input terminal of said comparator, and made conductive in response to a powerdown signal;  
 a second transmission gate having a first terminal connected to said second terminal of said first transmission gate, and a second terminal, and made-conductive in response to said powerdown signal;  
 a second resistor having a first terminal coupled to said second terminal of said second transmission gate, and a second terminal for providing a fourth voltage; and  
 a third resistor having a first terminal coupled to said second terminal of said second resistor, and a second terminal for receiving a third power supply voltage.

19. The circuit of claim 16 wherein said first power supply voltage is a battery voltage.

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**United States Patent** [19]

Chan et al.

[11] **Patent Number:** 5,306,954[45] **Date of Patent:** Apr. 26, 1994[54] **CHARGE PUMP WITH SYMMETRICAL +V AND -V OUTPUTS**[75] **Inventors:** Paul S. Chan, Cupertino; Raymond W. B. Chow, Saratoga, both of Calif.[73] **Assignee:** Sipex Corporation, Billerica, Mass.[21] **Appl. No.:** 893,519[22] **Filed:** Jun. 4, 1992[51] **Int. Cl.<sup>3</sup>** ..... H02M 3/18[52] **U.S. Cl.** ..... 307/110; 363/60[58] **Field of Search** ..... 307/108-110, 307/115, 125; 320/1; 361/245, 246; 363/59, 60, 63; H02M 7/25[56] **References Cited****U.S. PATENT DOCUMENTS**

3,470,443	9/1969	Berry et al.	321/2
3,731,112	5/1973	Smith	307/109
3,878,450	4/1975	Greatbatch	321/15
3,942,047	3/1976	Buchanan	307/297
3,943,428	3/1976	Whidden	321/15
3,955,353	5/1976	Astle	58/23 BA
3,975,671	8/1976	Stoll	321/15
4,047,091	9/1977	Hutchines et al.	363/59
4,061,929	12/1977	Asano	307/246
4,068,295	1/1978	Portmann	363/60
4,106,086	8/1978	Holbrook et al.	363/60
4,186,436	1/1980	Ishiwatari	363/60
4,321,661	3/1982	Sano	363/60
4,460,952	7/1984	Risinger	363/61
4,485,433	11/1984	Topich	363/60
4,527,277	7/1985	Kosaka et al.	375/82
4,547,682	10/1985	Bialas, Jr. et al.	307/297
4,596,963	6/1986	Lawton et al.	331/14
4,636,930	1/1987	Bingham et al.	363/60
4,679,134	7/1987	Bingham et al.	363/61
4,736,167	4/1988	Kojima et al.	331/17
4,745,372	5/1988	Miwa	331/8
4,750,193	6/1988	Bailey	375/81
4,766,397	8/1988	Adams	331/1 A
4,777,577	10/1988	Bingham et al.	363/60
4,797,899	1/1989	Fuller et al.	375/7
4,809,152	2/1989	Bingham et al.	363/61
4,829,391	5/1989	Vargas, Jr.	360/51
4,871,979	10/1989	Shearer et al.	330/253
4,897,774	1/1990	Bingham et al.	363/61

4,914,695	4/1990	Martin	380/7
4,922,141	5/1990	Lofgren et al.	307/595
4,970,472	11/1990	Kennedy et al.	331/8
4,970,475	11/1990	Gillig	331/25
4,999,761	3/1991	Bingham et al.	363/60
5,003,197	3/1991	Nojima et al.	307/296.2
5,008,629	4/1991	Ohba et al.	328/14
5,043,686	8/1991	Plunkett	333/181
5,237,209	8/1993	Brewer	307/110

**OTHER PUBLICATIONS**

Wakeman, Larry, "National's Process Enhancements Eliminate the CMOS SCR Latch-Up Problem in 56HC/74HC Logic," *National Semiconductor Application Note 339*, pp. 2-43 through 2-50, undated.

*Primary Examiner*—Jeffrey A. Gaffin

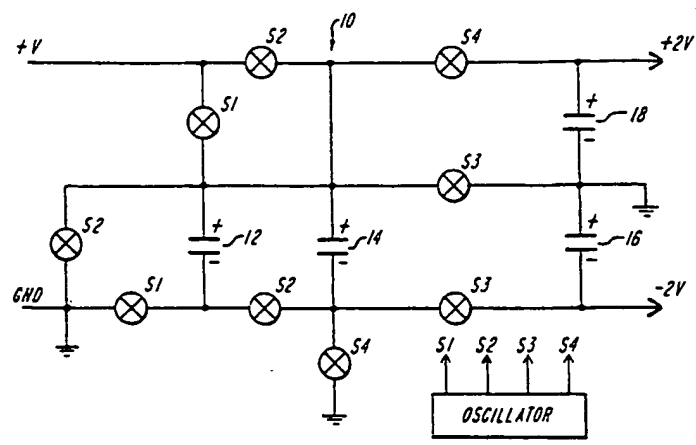
*Assistant Examiner*—Richard T. Elms

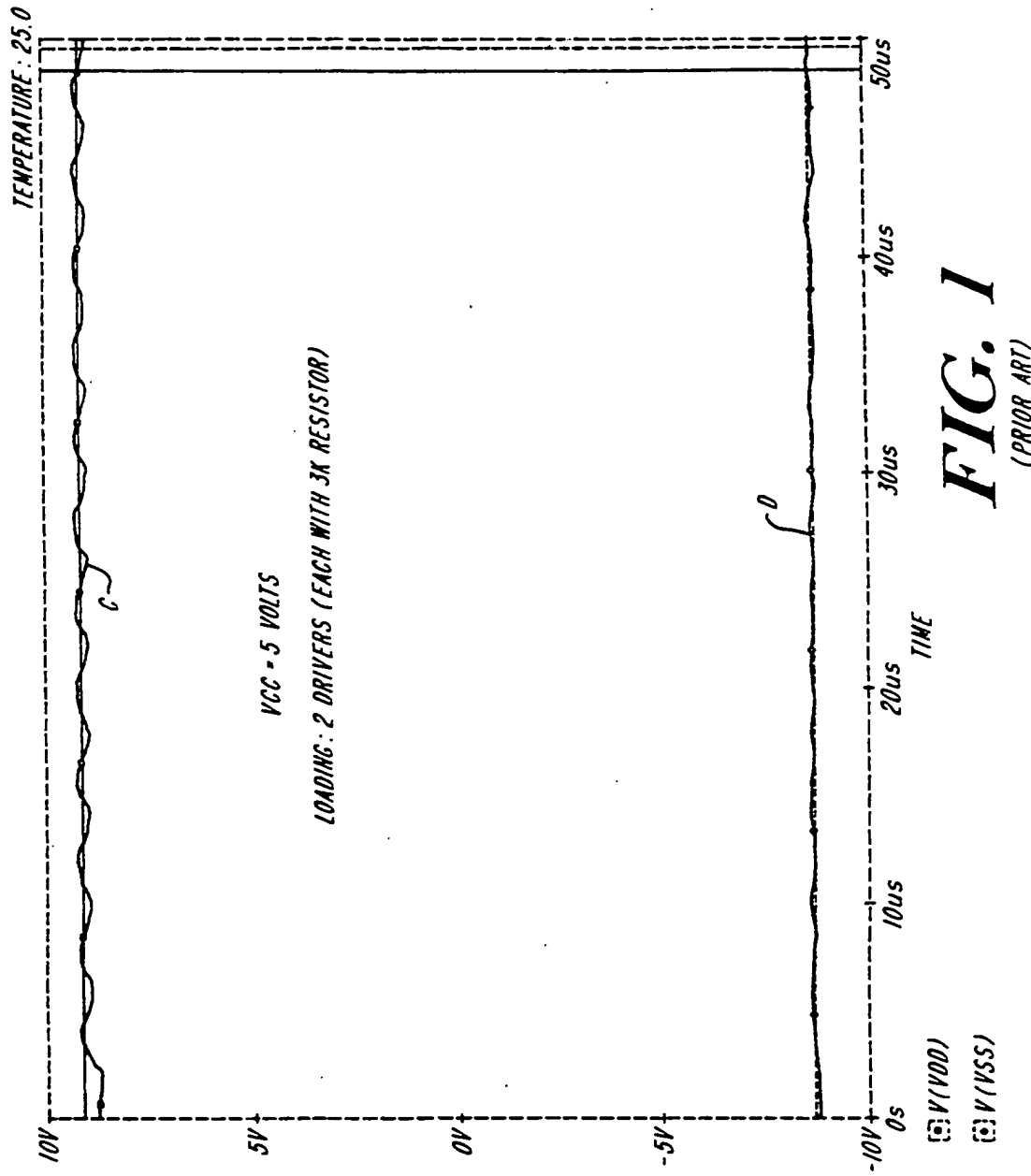
*Attorney, Agent, or Firm*—Weingarten, Schurgin, Gagnebin & Hayes

[57]

**ABSTRACT**

Charge pump circuitry is implemented using a voltage shifting technique to generate a symmetrical bipolar voltage. The symmetrical bipolar voltage charge pump power supply can be fabricated as an integrated circuit on a single substrate, and can be integrated with various interface circuits to provide symmetrical bipolar voltage thereto. The charge pump includes voltage shifting circuitry which generates an increased output voltage of a negative polarity and an increased output voltage of a positive polarity. The shifting circuitry is responsive to an internal oscillator which triggers charge accumulation and voltage shifting. Neither output voltage is generated from the other output voltage. Rather, the negative and positive supply voltages are each generated, in substantially the same manner, by charge transfer effected by the voltage shifting circuitry in response to triggering by the internal oscillator. Additional circuitry can be fabricated on a single substrate in combination with the presently disclosed charge pump to effect the optimum utilization of circuit board area while minimizing power consumption.

**25 Claims, 4 Drawing Sheets**



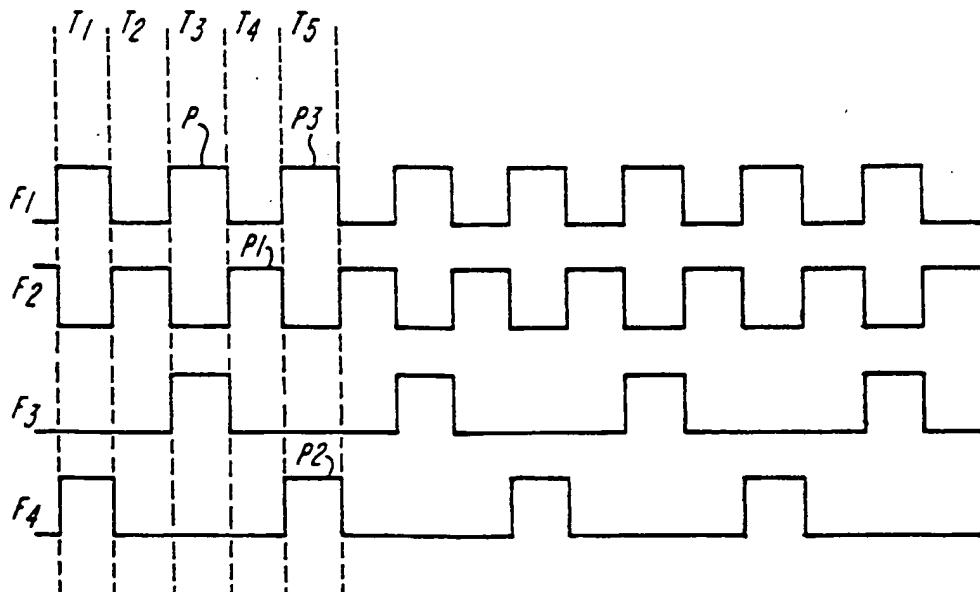
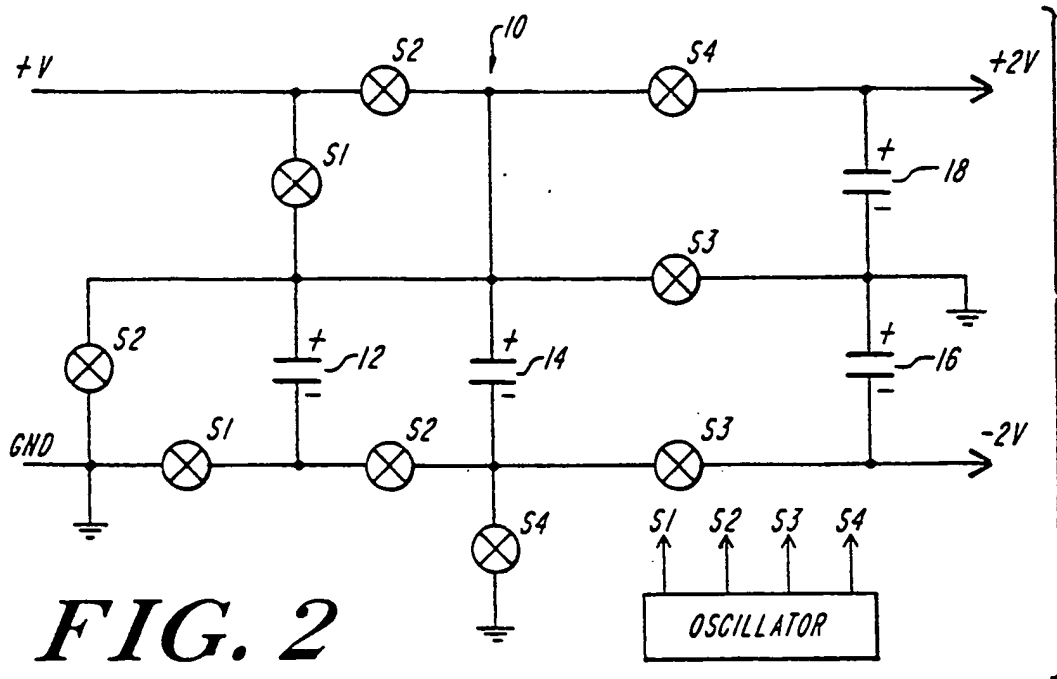


FIG. 3

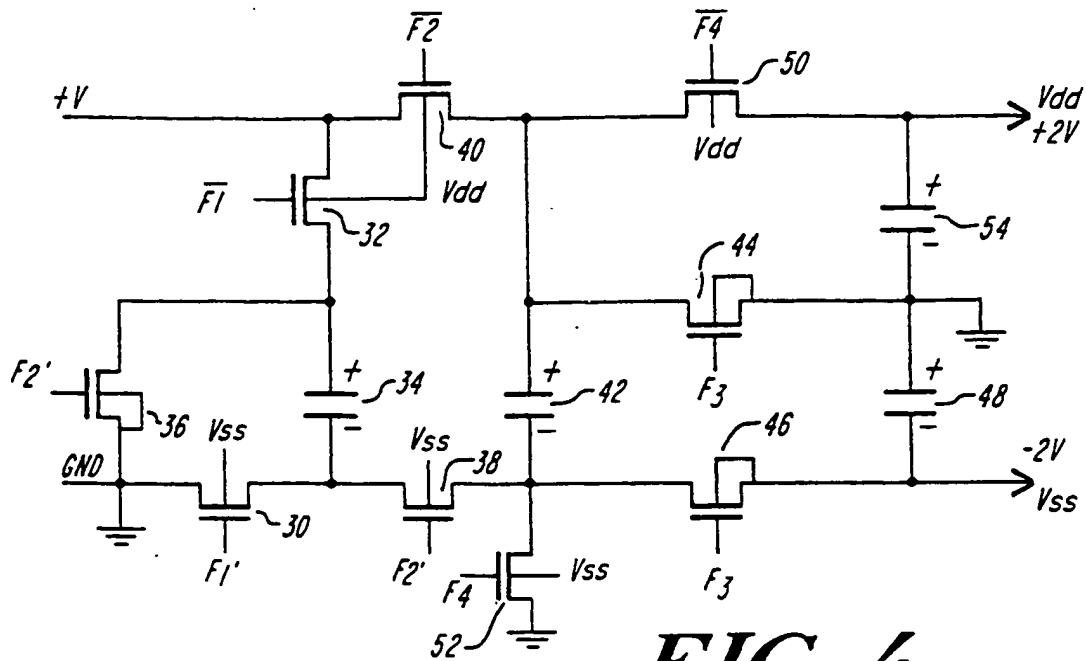


FIG. 4

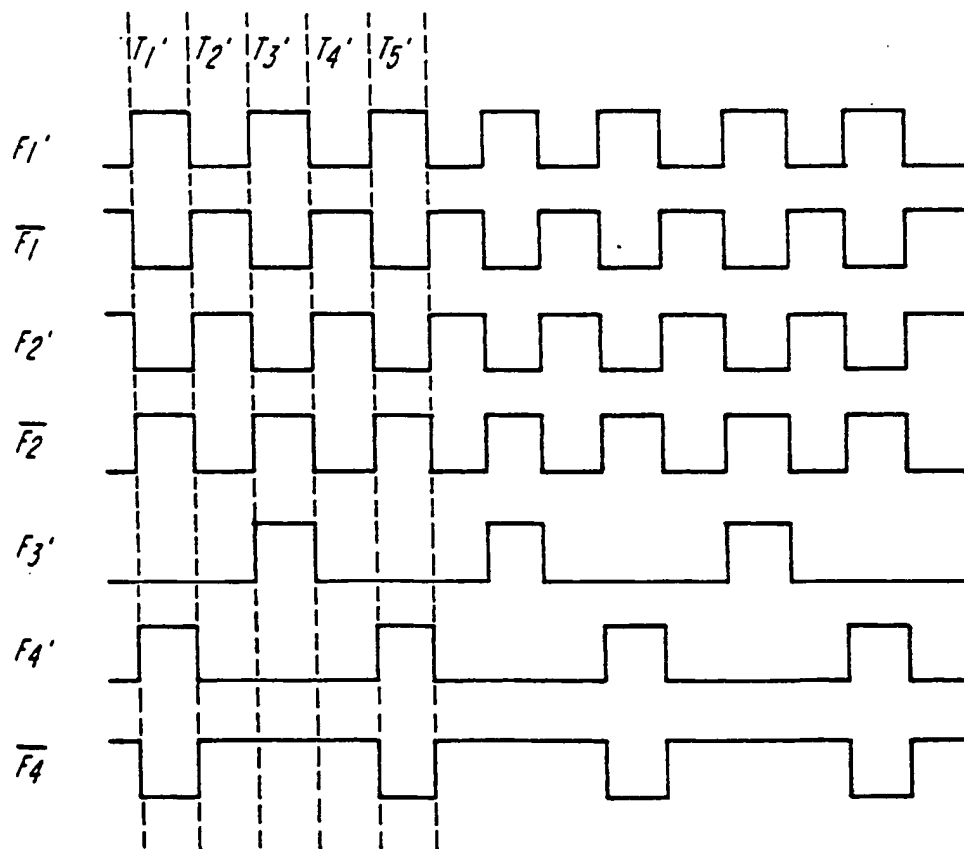


FIG. 5

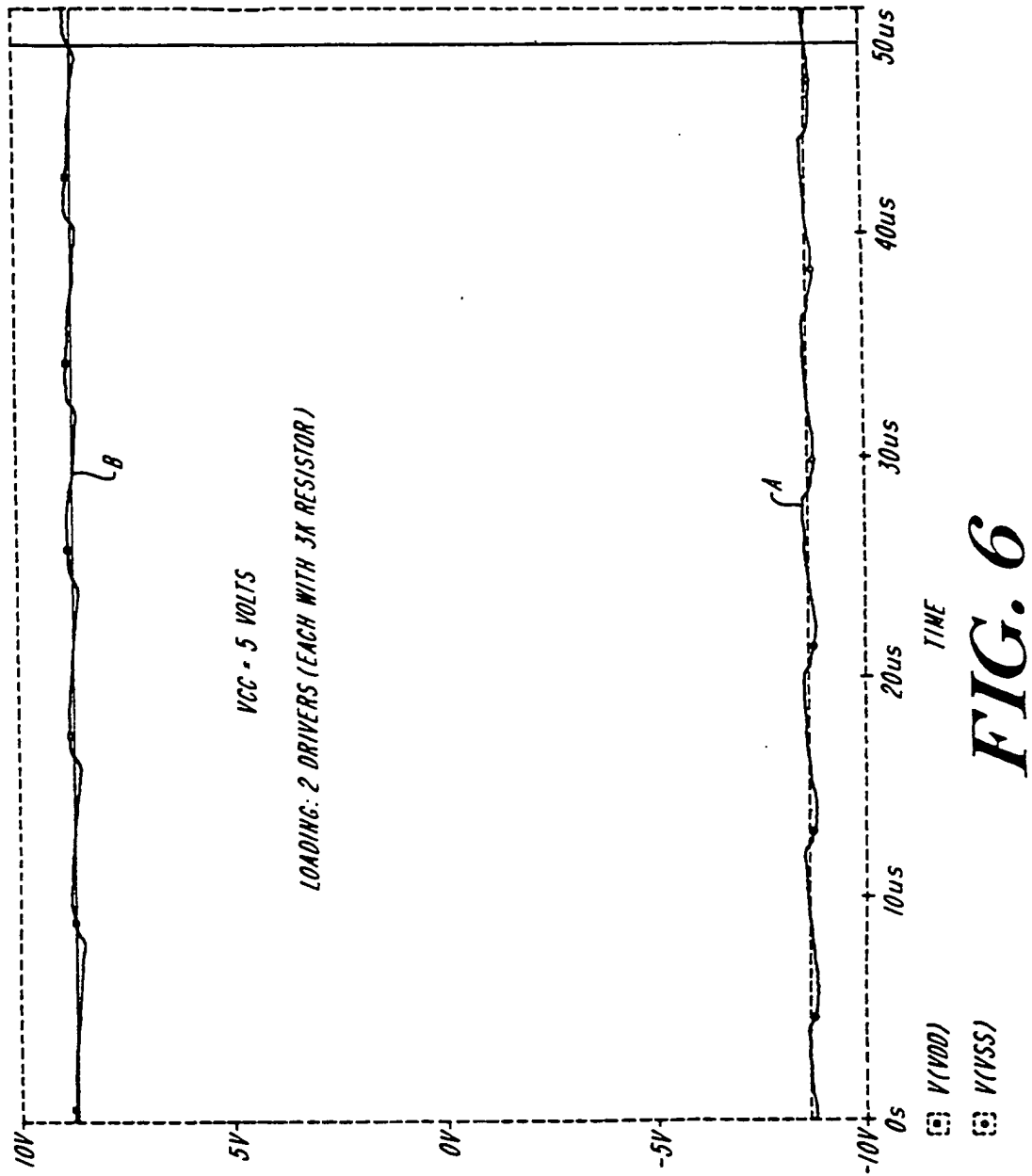


FIG. 6

## CHARGE PUMP WITH SYMMETRICAL +V AND -V OUTPUTS

### FIELD OF THE INVENTION

The present invention relates to charge pump circuits, and in particular to circuitry for converting a unipolar supply voltage to a bipolar voltage of greater magnitude.

### BACKGROUND OF THE INVENTION

Integrated circuits are known which contain inverting/non-inverting voltage doubler charge pump circuitry for converting a unipolar supply voltage to a bipolar supply voltage of greater magnitude. Typically, the charge pump circuitry is fabricated on a single chip that receives the unipolar supply voltage (e.g. +5 v) and doubles it. The doubled voltage is then inverted, resulting in the bipolar voltage of increased magnitude (e.g. +/- 10 v), which is used as a bipolar supply for on-chip circuitry, such as RS232 receivers and transmitters.

U.S. Pat. Nos. 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,636,930 and 4,999,761 illustrate various implementations of such circuitry. The devices disclosed and claimed therein include switches which act during a first phase to direct a source voltage (unipolar) to a first capacitor. The first capacitor charges to the unipolar source voltage. During a second phase, switches act to place the source voltage in series with the voltage stored on the first capacitor to create a source of positive voltage which is approximately two times the unipolar source voltage. A reservoir capacitor is charged to the doubled positive voltage. The doubled positive voltage is stored on a transfer capacitor and subsequently transferred to a reservoir capacitor. Inversion of the doubled positive source voltage is then provided to generate the negative doubled portion of the bipolar voltage. Thus, in the referenced prior art, the doubled positive voltage is generated first and the inverted (i.e. negative) voltage is generated from the doubled positive voltage.

Use of the positive voltage to generate the negative voltage in charge pump circuits known in the prior art is disadvantageous with respect to the asymmetrical loading characteristic of the respective outputs. As illustrated in FIG. 1, in the prior art, given similar loading the negative voltage output is lower than the positive voltage output, i.e., the positive and negative voltage signals are asymmetrical with respect to their common reference. For instance, in the simulation of the prior art which is illustrated, a unipolar +5 V source is provided to a charge pump with a voltage doubler and inverter. The conventional voltage doubler and inverter doubles the source voltage to provide a doubled positive voltage and the negative voltage is generated by inverting the positive doubled voltage. While the prior art charge pump circuitry results in a doubled positive voltage C, averaging +9.15 volts under a 3 K ohm resistive load, the negative portion D generated by inverting the positive voltage averages -8.67 volts, under the same load.

The asymmetry of the doubled positive and inverted voltages negatively affects operational tolerance of circuitry constituting a load to the charge pump.

### SUMMARY OF THE INVENTION

A charge pump is presently disclosed which implements a novel voltage shift technique to generate a bipolar voltage having balanced or symmetrical drive capability.

In one embodiment, a charge pump power supply is integrated into a single piece of semiconductor substrate material, and can be integrated with various interface circuits to provide a symmetrical bipolar voltage thereto. The shifting circuitry is responsive to an internal oscillator which triggers charge accumulation and voltage shifting. Unlike the prior art charge pumps referenced hereinabove, the negative bipolar output voltage is not generated from the positive bipolar output voltage. Rather, the negative and positive bipolar output voltages are each generated, in substantially the same manner, via the symmetrical charge transfer technique herein described.

Features of the invention include provision of symmetrical +V and -V output voltages under balanced load conditions. The charge pump can also be integrated with various other circuits including interface circuits in conformance with RS232, RS422, RS485 and other standards, or any other functional circuitry as desired.

### DESCRIPTION OF THE DRAWING

Other features and benefits of the invention will be more clearly understood with reference to the specification and the accompanying drawings in which:

FIG. 1 is a plot of circuit simulation outputs for a charge pump with a voltage doubler and voltage inverter according to the prior art;

FIG. 2 is a general schematic diagram of a charge pump circuit for generating symmetrical +V and -V output voltages;

FIG. 3 is a timing diagram of oscillator signals providing the timing sequence for the charge pump circuit of FIG. 2, for generating symmetrical +V and -V output voltages;

FIG. 4 is a schematic diagram providing greater detail of the charge pump circuit of FIG. 2 for generating symmetrical +V and -V output voltages;

FIG. 5 is a timing diagram of oscillator signals providing the timing sequence for the charge pump circuit of FIG. 4, for generating symmetrical +V and -V output voltages; and

FIG. 6 is a plot of circuit simulation outputs for a charge pump according to FIGS. 2, 3, 4 and 5 generating symmetrical +V and -V output voltages.

### DETAILED DESCRIPTION

A charge pump circuit implementing a symmetrical voltage shifting technique is generally illustrated in FIG. 2. The circuit 10 is triggered by an oscillator (not shown) which generates a timing sequence, illustrated in FIG. 3. A plurality of switches, working in conjunction and represented functionally as S1, S2, S3, and S4, are triggered by the timing sequence as described hereinafter. Though shown schematically for simplicity in FIG. 2, it should be understood that the switches comprise semiconductor switches.

During a first time interval T1, switches indicated as S1 are closed so as to be in a conductive state in response to a first frequency F1, causing a first transfer capacitor 12 to be charged to approximately the source voltage +V. During a second time interval T2,

switches S1 are opened so as to be in a non-conductive state and switches S2 are closed in response to a second frequency F2, causing the positive (+) side of the charged first transfer capacitor 12 to be shifted from +V and connected to ground, effectively changing the reference of the voltage on the positive side of the first capacitor 12. Closing the switches S2 during the second time interval T2 also connects a second capacitor 14 between the +V voltage source and the negative side of the transfer capacitor 12, thereby causing the capacitor 14 to be charged to a magnitude of twice the +V voltage, and to be biased between +V and -V respectively at the positive and negative ends thereof. During a third time interval T3, switches S3 are closed in response to a third frequency F3. While the first transfer capacitor 12 is again charged during a pulse P according to the first frequency F1, the bias of the second capacitor 14 undergoes a negative voltage shift such that the capacitor 14 is interconnected in the circuit with the positive side of the capacitor 14 switchably connected to ground and the negative side of the capacitor 14 switchably connected to the negative side of a first storage capacitor 16, to provide the negative portion, -2 V, of the bipolar output voltage.

The pulse P, illustrated in F1, causes the first capacitor 12 to become charged to the supply voltage (+V) during the time interval T3. A pulse P1, illustrated in F2, causes the switches S2 to close, causing the positive (+) side of the charged first capacitor 12 to be shifted from +V and connected to ground, effectively changing the reference of the voltage on the positive side of the first capacitor 12. Also during the same time interval, the second capacitor 14 is switchably connected between the +V voltage source and the negative (-) side of the transfer capacitor 12, thereby causing the capacitor 14 to be charged to a magnitude of approximately twice the +V voltage, with the (+) and (-) ends thereof being biased substantially symmetrically around the ground reference.

During a fifth time interval T5, a pulse P2 illustrated in F4 causes the switches S4 to close, while switches S3 are open, connecting the negative end (-V) of the capacitor 14 to ground and connecting the positive end (+V) of the capacitor 14 to the positive side of a storage capacitor 18. The voltage across the capacitor 14 is shifted and switchably connected in parallel with the storage capacitor 18, to provide the positive portion, +2 V, of the bipolar voltage of increased magnitude.

During the time interval T5, a pulse P3 illustrated in F1 causes another charge to be developed on the first capacitor 12 which is used as described hereinabove, in subsequent time intervals to provide the negative portion, -2 V, of the bipolar voltage of increased magnitude. The charge transfer effected by the voltage shifting circuitry in response to triggering by the internal oscillator thus provides a negative portion of the bipolar voltage of increased magnitude that is not generated by inversion of the positive portion. The charge transfer and voltage shifting as described above, is continued repetitively resulting in the symmetrical -V and +V charge pump outputs.

An illustrative embodiment of the present invention is shown in greater detail in FIGS. 4 and 5. The various switches, formerly represented generally as S1, S2, S3 and S4, are implemented using N and P channel metal oxide semiconductor (MOS) field effect transistors, (FETs), as shown in FIG. 4.

The timing diagram of FIG. 5 illustrates the various frequencies of the oscillator employed to cause charge transfer and voltage shifting which result in the symmetrical -V and +V charge pump outputs, according to this illustrative embodiment. The oscillator can be fabricated via any technique well known in the art and employs oscillation circuitry generally known in the art. The circuit illustrated in FIG. 4 receives a unipolar supply input voltage +V. The circuit includes P channel and N channel field effect transistors (FETs), which perform the switching functions, substantially as described hereinabove and as illustrated in FIG. 5. While FETs are depicted, it is understood that any semiconductor switches can be employed with appropriate modifications to provide for proper biasing and activation of such switches.

A first frequency F1', is received at the gate of a first N channel FET 30 which is configured as a switch that is conductive when its gate is taken high. An inverse signal  $\overline{F1}$ , is received at the gate of a first P channel FET 32 configured as a switch that is conductive when its gate is taken low. During a first time interval T1', F1 is active (high) putting the first N channel FET 30 in a conductive state, while  $\overline{F1}$ , an active low signal puts the first P channel FET 32 in a conductive state, connecting a first transfer capacitor 34 across the unipolar input supply voltage +V and charging transfer capacitor 34 to +V during the time interval T1'. During a second time interval, T2', F1' and  $\overline{F1}$  are both inactive and F2' and  $\overline{F2}$  are received by second and third N channel FETs 36, 38 and second P channel FET 40, respectively. With FET switches 30 and 32 in a non-conductive state, and with FET switches 36, 38 and 40 in a conductive state in accordance with their respective gating signals F2' and  $\overline{F2}$ , the positive side of the charged capacitor 34 is shifted from +V and connected to ground through the active FET 36, effectively changing the reference of the voltage on the positive side of the transfer capacitor 34. A second capacitor 42 is connected, via conducting FET switches 38 and 40 during the time interval T2', between the +V voltage source and the negative side of the first capacitor 34 causing the capacitor 42 to be charged to a magnitude of approximately twice the +V voltage and to be biased between +V and -V at the positive and negative ends respectively, substantially symmetrically around the ground reference. During a third time interval T3', a third frequency F3' causes a pair of n-channel FET switches 44, 46 to become electrically conductive to change the reference of the voltage across capacitor 42. A negative voltage shift is thereby effected, wherein the positive side of capacitor 42 is switchably connected to ground and to the positive side of a reservoir capacitor 48 and the negative side of capacitor 42 is switchably connected to the negative side of the reservoir capacitor 48, to charge the negative storage capacitor 48 and to provide the negative portion, -2 V, of the bipolar output voltage.

Also during time interval T3', frequencies F1' and  $\overline{F1}$  are active to again cause FET switches 30 and 32 to become conductive, resulting in the charging of capacitor 34 to +V. During a fourth time interval, T4' frequencies F2' and  $\overline{F2}$  are active causing FET switches 36, 38 and 40 to become conductive and to electrically connect the positive side of charged capacitor 34 to ground, changing the reference thereof, and to connect the negative side of capacitor 42 to the negative side of capacitor 34 while the positive side of capacitor 42 is

connected to the input voltage  $+V$ . The resultant connection of the capacitor 42 between the  $+V$  voltage source and the negative side of capacitor 34 results in the capacitor 42 being charged to a magnitude of approximately twice the  $+V$  input voltage, and symmetrically biased around the ground reference with a  $+V$  voltage at the positive end of capacitor 42 and a  $-V$  voltage at the negative end of the capacitor 42.

When frequencies  $\bar{F}4$  and  $F4'$  are active during a fifth time interval  $T5'$ , FETs 50 and 52 become conductive, while FETs 44 and 46 become non-conductive, electrically connecting the negative end of capacitor 42 to ground and the positive end of capacitor 42 to the positive side of a second storage capacitor 54. The voltage of approximately twice the  $+V$  input voltage source which was biased between  $+V$  and  $-V$  across the capacitor 42 is thus shifted across the positive storage capacitor 54, so as to charge the storage capacitor 54 and provide the positive portion,  $+2V$ , of the bipolar output voltage.

The frequencies  $F1'$  and  $\bar{F}1$ , connected to the gates of FETs 30 and 32 and active during the time interval  $T5'$ , cause another charge to be developed on the capacitor 34, which is used in subsequent time intervals to provide the negative portion,  $-2V$ , of the bipolar output voltage.

The repetitive charge transfer and voltage shifting in response to the various frequencies of the interval oscillator results in a symmetrical  $+V$  and  $-V$  bipolar output voltage as illustrated in FIG. 6, in response to balanced loading. The unipolar  $+5V$  input voltage provided to the charge transfer and voltage shifting circuitry described hereinbefore, results in a negative portion (A) of the bipolar voltage which averages approximately  $-8.69$  volts with an applied  $3K$  ohm resistive load. The positive portion (B) of the bipolar voltage generated by charge transfer and voltage shifting, averages  $+8.69$  volts when driving a  $3K$  ohm resistive load. The symmetry of the bipolar output voltages is thus significantly greater than is obtainable via the charge pump circuitry employing voltage doublers and inverters known in the art.

The circuitry described hereinbefore can be implemented in a monolithic silicon substrate using CMOS fabrication techniques to implement the charge pump having symmetrical  $-V$  and  $+V$  output voltages to supply RS232 transmitters and/or receivers fabricated in the same substrate. Additionally, the charge pump can be integrated with various other circuits including interface circuits in conformance with RS422, RS485 and other standards, as well as circuitry performing other functions such as analog to a digital conversion.

While an illustrative embodiment is disclosed hereinabove which employs FET switches to cause desired connections, it will be appreciated that other semiconductor switching means can be used in practicing the invention.

Although the illustrative embodiments described hereinabove implement a voltage shifting technique wherein the negative output voltage of increased magnitude is generated first via voltage shifting and the positive output voltage of increased magnitude is generated subsequently, it is appreciated that the switching and voltage shifting technique can be implemented so that the positive voltage is generated first with the negative voltage generated subsequently, while still employing the disclosed shifting technique.

Although the invention has been shown and described with respect to exemplary embodiments thereof, various other changes, omissions and additions in form and detail thereof may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A method for generating, from a first voltage source providing a unipolar input voltage of first polarity having a voltage reference connection, bipolar output voltages of magnitude approximately twice the unipolar input voltage comprising the steps of:
  - charging a first charge transfer device having first and second connection ends to a voltage approximating said unipolar input voltage by switchably connecting said second connection end of said first charge transfer device to said unipolar input voltage and said first connection end of said first charge transfer device to said voltage reference connection;
  - in a first generating step, generating a second voltage source at the first connection end of said first charge transfer device, with respect to said voltage reference connection, of magnitude substantially equal to the magnitude of said unipolar input voltage but of opposite polarity by switchably connecting said second end of said first charge transfer device to said voltage reference connection;
  - charging a second charge transfer device having first and second connection ends by switchably connecting said second connection end of said second charge transfer device to said unipolar input voltage and said first connection end of said second charge transfer device to said second voltage source;
  - in a second generating step, generating a third voltage source of magnitude approximately equal to twice the magnitude of said unipolar input voltage and of a selected polarity by switchably connecting one of said first and second connection ends of said second charge transfer device to said voltage reference connection;
  - in a third generating step, generating a fourth voltage source of magnitude approximately equal to twice the magnitude of said unipolar input voltage and of a polarity opposite to said selected polarity by switchably connecting the other of said first and second connection ends referenced in said second generating step to said voltage reference connection.
2. The method of claim 1 further including between said second and third generating steps a step of recharging said second charge transfer device between said unipolar input voltage and said second voltage source.
3. The method of claim 2 wherein said first charge transfer device is a capacitor.
4. The method of claim 3 wherein said second charge transfer device is a capacitor.
5. The method of claim 1 wherein said second generating step includes a step of transferring charge from said second charge transfer device to a first charge storage device and said third generating step includes the step of transferring charge from said second charge transfer device to a second charge storage device.
6. The method of claim 5 wherein said third and fourth charge storage devices are capacitors.
7. The method of claim 5 wherein the steps of charging a first charge transfer device, generating a second voltage source, charging a second charge transfer de-



vice, generating a third voltage source and generating a fourth voltage source are performed repetitively.

8. The method of claim 1 wherein said unipolar input voltage is of a positive polarity with respect to said voltage reference connection, said third voltage source has a negative polarity with respect to said voltage reference connection, and said fourth voltage source has a positive polarity with respect to said voltage reference connection.

9. The method of claim 1 wherein said unipolar input voltage is of a positive polarity with respect to said voltage reference connection, said third voltage source has a positive polarity with respect to said voltage reference connection, and said fourth voltage source has a negative polarity with respect to said voltage reference connection.

10. A method for generating, from a first voltage source providing a unipolar input voltage of first polarity having a voltage reference connection, bipolar output voltages of magnitude approximately twice the unipolar input voltage comprising the steps of:

in a first reconfiguring step, switchably connecting a first capacitor having first and second connection ends such that the second connection end is electrically connected to the unipolar input voltage and the first connection end is electrically connected to the voltage reference connection to charge the first capacitor to a voltage approximating the unipolar input voltage;

in a second reconfiguring step, switchably reconfiguring the first capacitor to generate a second voltage source at the first connection end of the first capacitor of magnitude substantially equal to the unipolar input voltage with respect to the voltage reference connection but of a second polarity opposite to the first polarity;

in a third reconfiguring step, switchably connecting a second capacitor having first and second connection ends between the unipolar input voltage source of first polarity and the second voltage source of second polarity;

in a fourth reconfiguring step, switchably reconfiguring the second capacitor to generate a third voltage source with respect to the voltage reference connection having a magnitude approximately twice the magnitude of the unipolar input voltage and having a selected polarity; and

in a fifth reconfiguring step, switchably reconfiguring the second capacitor to generate a fourth voltage source with respect to the voltage reference connection having a magnitude approximately twice the magnitude of the unipolar input voltage of polarity opposite to the selected polarity of the third voltage source.

11. The method of claim 10 further including between the fourth and fifth reconfiguring steps, the step of recharging the second capacitor between the unipolar input voltage of first polarity and the second voltage source of second polarity.

12. The method of claim 11 wherein the second reconfiguring step includes the step of switchably disconnecting the first connection end of the first capacitor from the voltage reference connection and switchably connecting the second connection end of the first capacitor to the voltage reference connection.

13. The method of claim 10 wherein the third reconfiguring step includes the step of switchably connecting the first end of the second capacitor to the second volt-

age source and switchably connecting the second end of the second capacitor to the unipolar input voltage.

14. A method for generating a bipolar output voltage from a unipolar input supply voltage having a voltage reference, said method comprising the steps of:

charging a first charge transfer device to a first voltage approximately equal to said unipolar input supply voltage;

inverting said first voltage to provide a second voltage of a magnitude approximately equal to and a polarity opposite to said first voltage and providing a third voltage between said unipolar input supply voltage and said second voltage;

transferring said third voltage to a first charge storage device of a selected polarity; and

transferring said third voltage to a second charge storage device of polarity opposite to said selected polarity.

15. The method of claim 14 further including the step of storing said third voltage on a second charge transfer device and alternately connecting said second charge transfer device in parallel with each of said first and second charge storage devices to effect the transfer of said third voltage in said transferring steps.

16. The method of claim 14 wherein said selected polarity is negative with respect to said voltage reference.

17. The method of claim 15 further including a step of recharging said second charge transfer device after transferring said third voltage to said first charge storage device and prior to transferring said third voltage to said second charge storage device.

18. An apparatus for generating a bipolar output voltage from a first voltage providing a unipolar input supply voltage having a voltage reference, comprising:

at least two first switching devices operative upon activation to charge a first charge transfer storage device to a first voltage approximately equal to said unipolar input supply voltage;

at least two second switching devices operative upon activation to invert said first voltage to provide a second voltage of a magnitude approximately equal to and a polarity opposite to said first voltage and to couple said second voltage and said unipolar input supply voltage to provide a third voltage between said unipolar input supply voltage and said second voltage;

at least two third switching devices operative upon activation to transfer said third voltage to a first charge storage device of a selected polarity; and at least two fourth switching devices operative upon activation to transfer said third voltage to a second charge storage device of polarity opposite said selected polarity.

19. The apparatus of claim 18 further including an oscillator for generating a plurality of signals to activate said first, second, third and fourth switching devices.

20. The apparatus of claim 18 further including a second charge transfer device for storing said third voltage prior to transferring said third voltage.

21. The apparatus of claim 18 wherein said selected polarity is negative with respect to said voltage reference.

22. The apparatus of claim 20 wherein said second charge storage transfer device is recharged after transferring said third voltage to said first charge storage device and prior to transferring said third voltage to said second charge storage device.

23. The apparatus of claim 18 wherein at least one of said first charge transfer device, said first charge storage device and said second charge storage device is a capacitor.

24. The apparatus of claim 18 wherein at least one of said first, second, third and fourth switching devices is a field effect transistor.

25. The apparatus of claim 24 wherein at least one of

said first, second, third, and fourth switching devices is an n-channel metal oxide semiconductor field effect transistor and at least one of said first, second, third, and fourth switching devices is a p-channel metal oxide semiconductor field effect transistor.

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US005193198A

**United States Patent** [19]

Yokouchi

[11] Patent Number: **5,193,198**[45] Date of Patent: **Mar. 9, 1993****[54] METHOD AND APPARATUS FOR  
REDUCED POWER INTEGRATED CIRCUIT  
OPERATION**[75] Inventor: **Hideaki Yokouchi, Suwa, Japan**[73] Assignee: **Seiko Epson Corporation, Tokyo,  
Japan**[21] Appl. No.: **696,460**[22] Filed: **May 6, 1991****[30] Foreign Application Priority Data**

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Aug. 10, 1990 [JP]	Japan	2-213221
Mar. 15, 1991 [JP]	Japan	3-51381

[51] Int. Cl.<sup>5</sup> ..... **H03K 3/01; H02M 3/07**[52] U.S. Cl. .... **395/750; 363/60;  
365/226; 365/227**[58] Field of Search ..... **323/313, 314, 317;  
364/707; 307/29, 48, 80, 85, 86, 28, 38, 142,  
143; 363/60; 395/725, 750; 365/228, 229, 226,  
227****[56] References Cited****U.S. PATENT DOCUMENTS**

3,757,795	9/1973	Anderson	307/48
3,941,989	3/1976	McLaughlin et al.	395/750
3,980,935	9/1976	Worst	365/229
4,236,199	11/1980	Stewart	363/60
4,565,960	1/1986	Takata et al.	323/317
4,794,317	12/1988	van Tran	323/316
4,806,789	2/1989	Sakihama et al.	365/228
4,875,188	10/1989	Jungroth	307/29
4,890,051	12/1989	Kim et al.	323/313

4,990,847	2/1991	Ishimaru et al.	323/317
5,012,132	4/1991	Wang	365/226

**OTHER PUBLICATIONS**

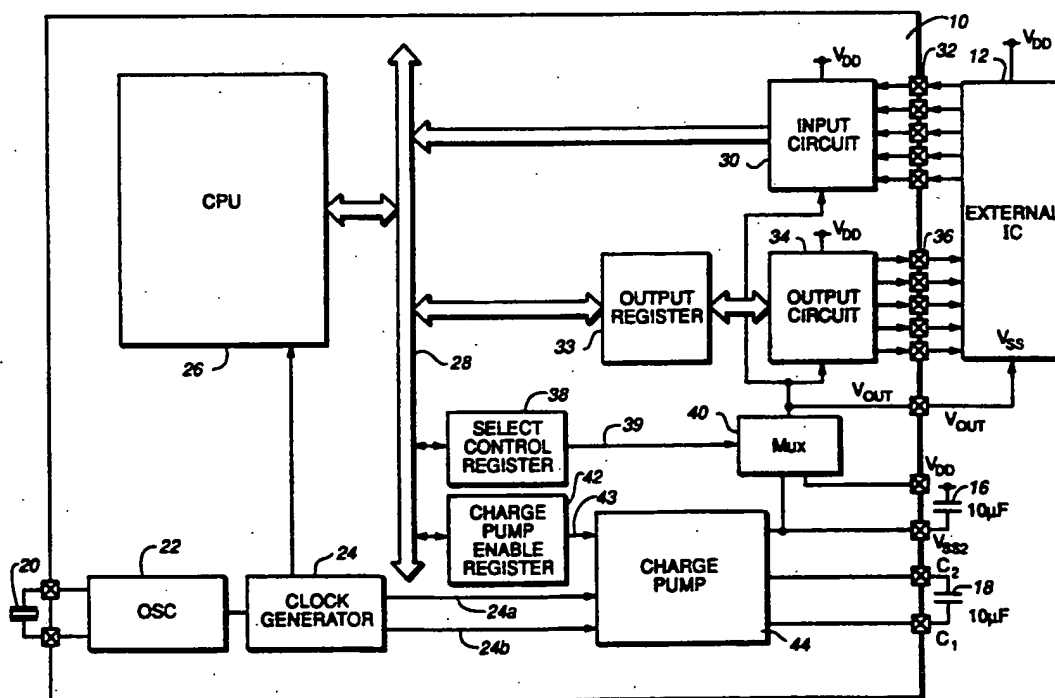
Owen, "Voltage Generator for EPROMs", Electronic Product Design (G.B.) p. 28, Oct. 1981.

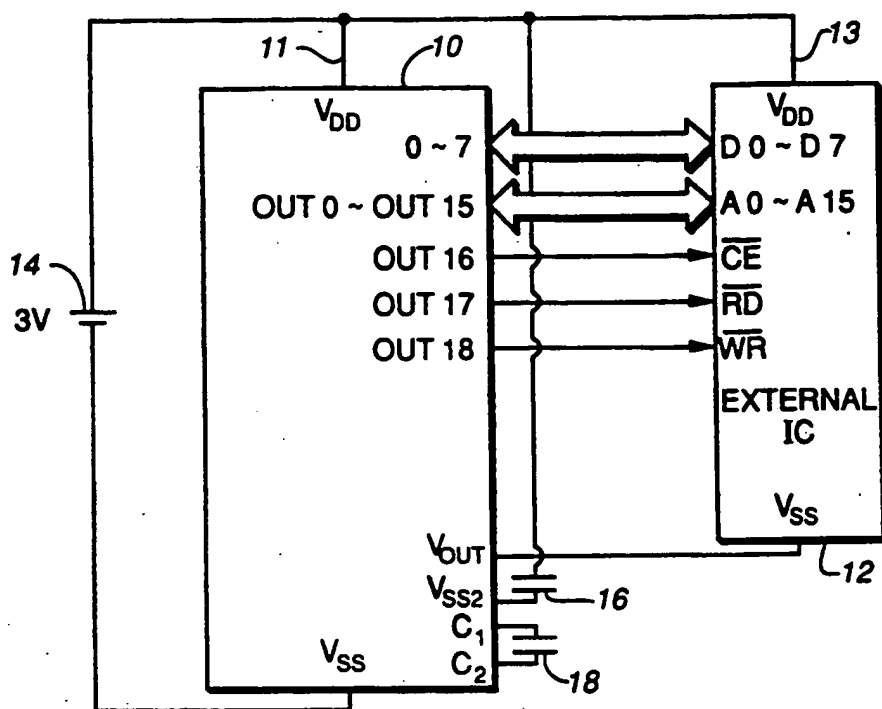
Primary Examiner—William H. Beha, Jr

Attorney, Agent, or Firm—Raymond J. Werner

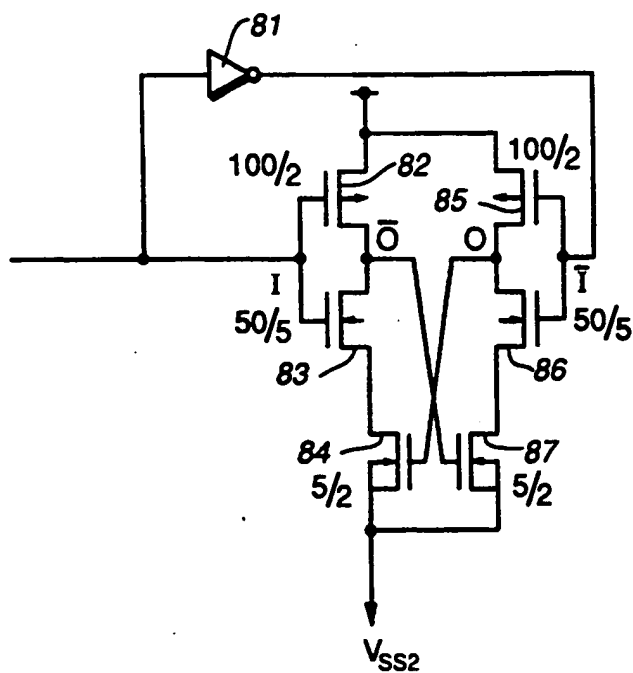
**[57] ABSTRACT**

A battery-powered electronic system in which ICs of low and high voltage specifications can be operated simultaneously by a single low voltage power supply, wherein prolongation of battery life, miniaturization of the housing size and reduction of manufacturing costs are achieved. The present invention comprises a monolithically integrated charge pump circuit for boosting a power supply voltage so as to output a voltage greater than that of the power supply voltage, and a power supply multiplexor for selecting between the output of the charge pump circuit and the power supply voltage in accordance with a power supply select control signal. The output of the multiplexor is used as a supply voltage, for at least one other IC in the system. The voltage selection process is dynamically determined based on the time-varying requirements of system operation. A voltage regulation circuit may be used to provide control over the charge pump circuit output. Circuitry is disclosed for disabling charge pump operation, when such operation is unnecessary, to reduce power consumption.

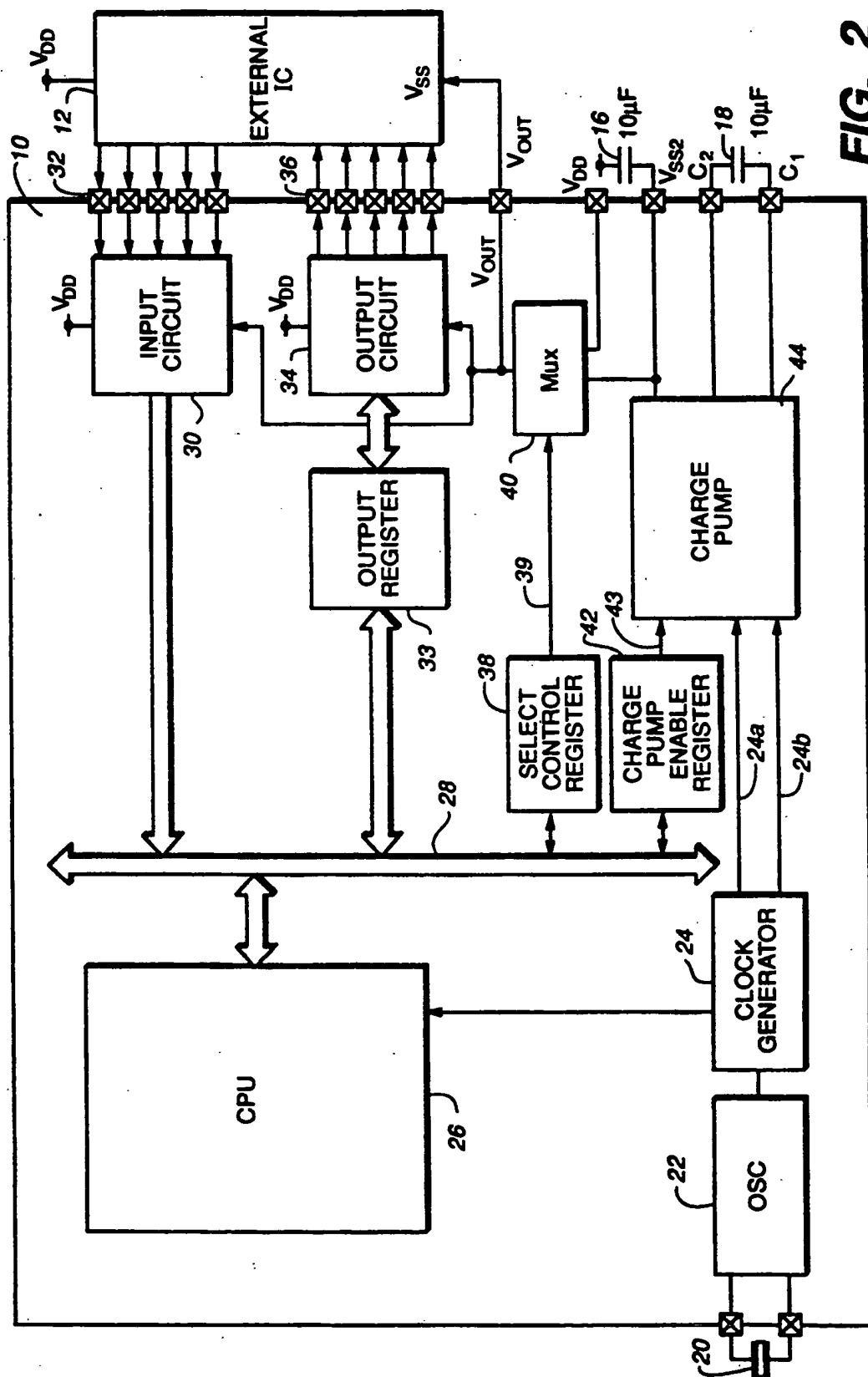
**18 Claims, 6 Drawing Sheets**



**FIG. 1**



**FIG. 4**



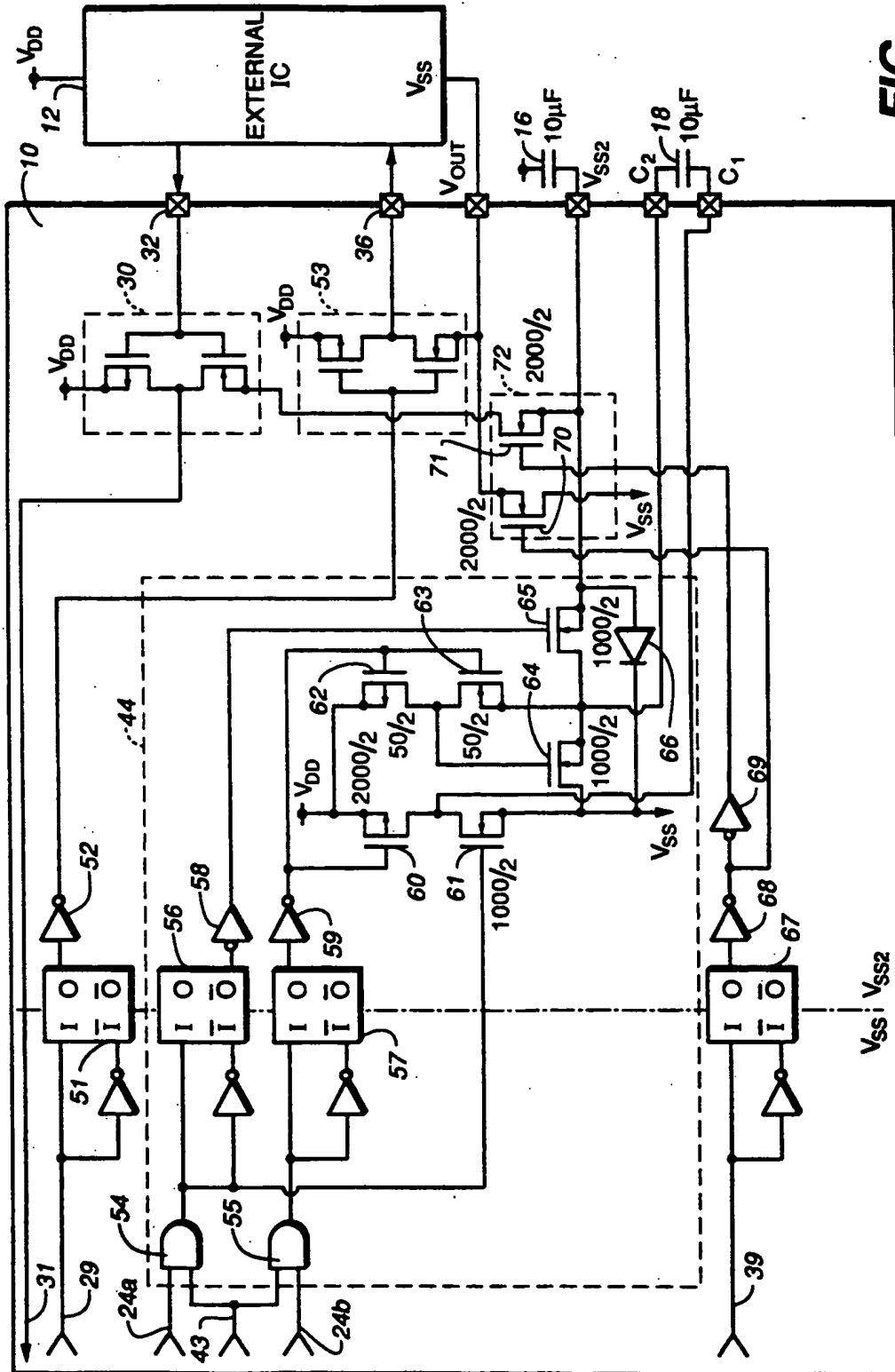
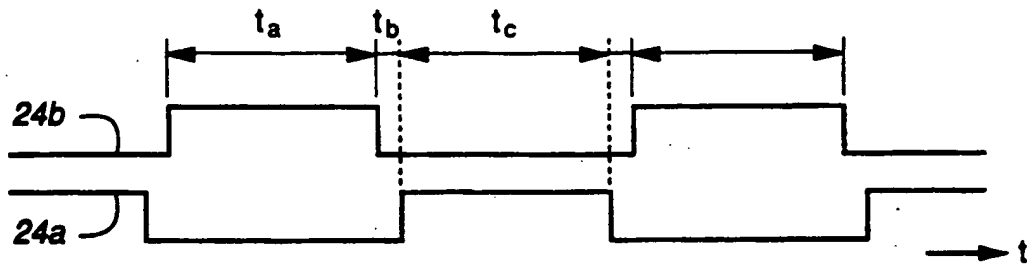
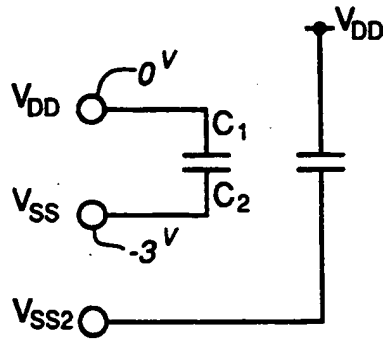


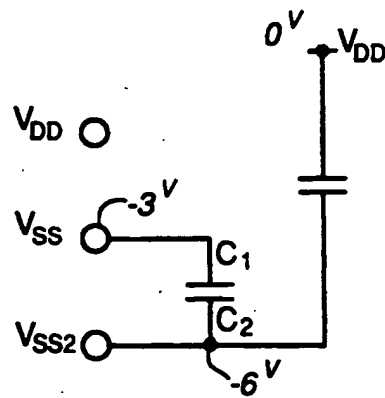
FIG. 3



**FIG.\_5**



**FIG.\_6**



**FIG.\_7**

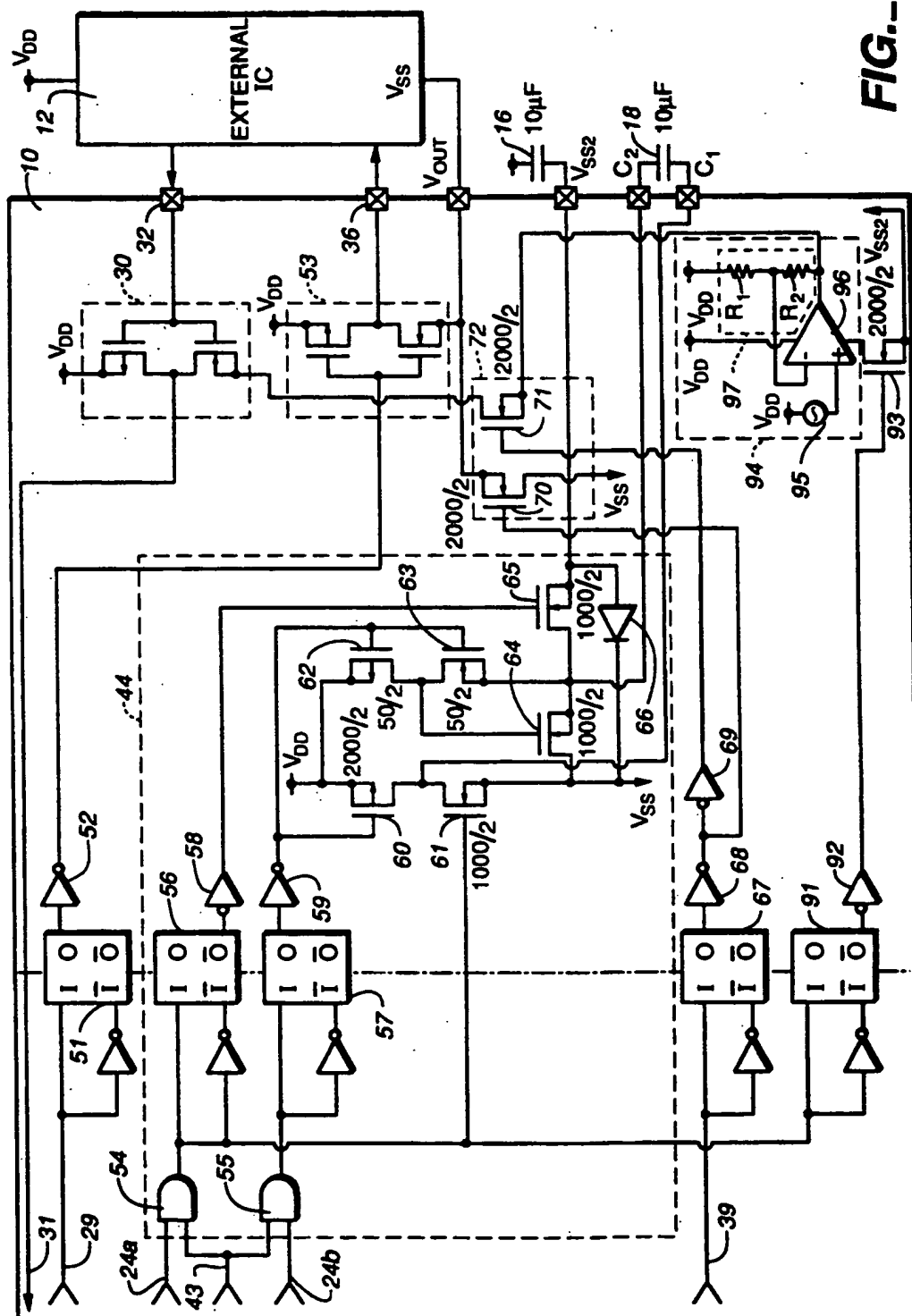
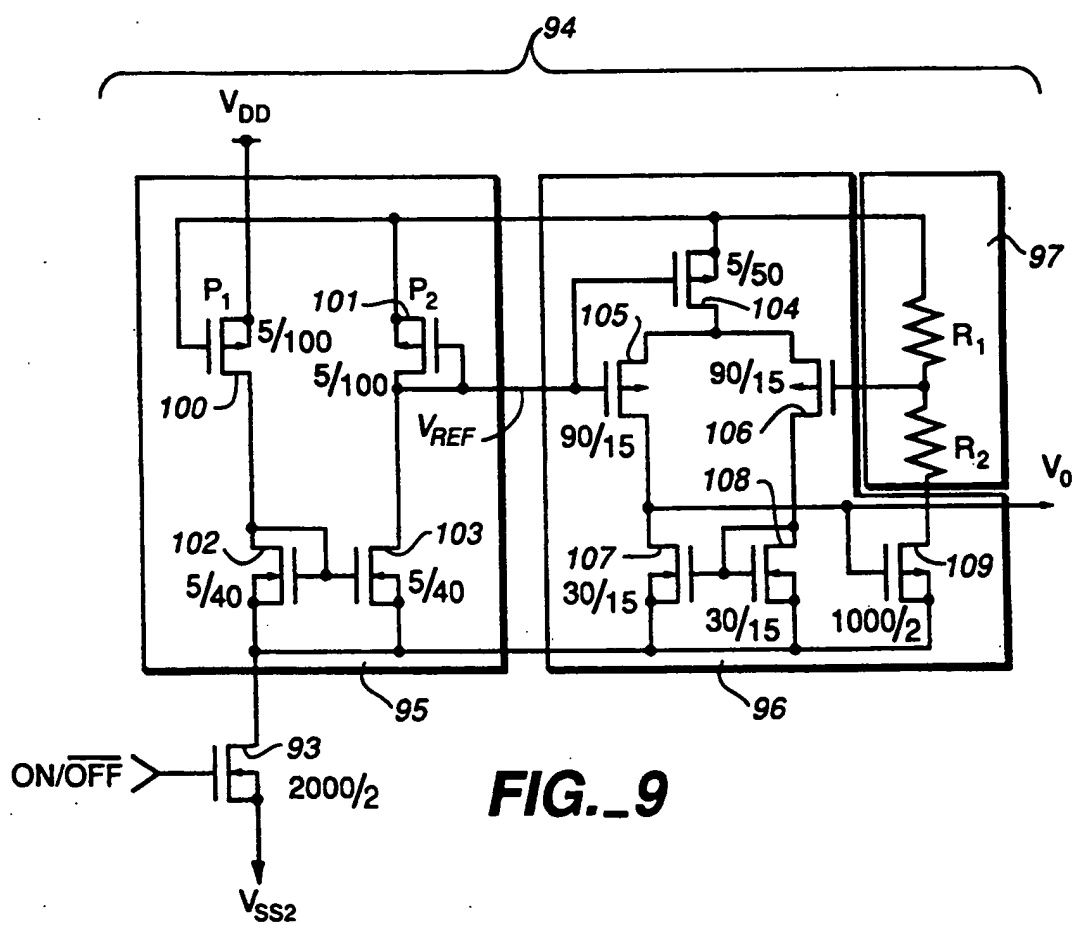


FIG. 8





## METHOD AND APPARATUS FOR REDUCED POWER INTEGRATED CIRCUIT OPERATION

### BACKGROUND OF THE INVENTION

The present invention relates to integrated circuit power supply techniques for minimizing power consumption. More particularly, the present invention relates to generating a voltage supply by means of a circuit resident within a first integrated circuit, for powering additional peripheral chips, such as memory devices that operate at both high and low voltages.

In conventional electronic systems using a plurality of integrated circuits (ICs) it is typical to use a common voltage supply for each IC. For example these systems are typically built by grouping together and using only ICs of the 5 V or the 3 V type. This is done in order to simplify the system by reducing the power supply and wiring requirements inherent in a multiple supply design.

However, in low-power microcomputer systems, a problem exists with respect to segregating ICs by their power supply requirements. Many low-power microcomputers are designed to operate with a 3 V power supply so that they can be driven by one lithium cell, but generally available memory devices are typically designed for operation with a 5 V power supply. In a low-power electronic apparatus such as a battery-powered electronic notebook in which a microcomputer and an external memory device are combined, a power supply comprised of a pair of lithium cells connected in series is needed to provide the greater than 3 V power supply required by the memory. Therefore, in such an apparatus, current consumption is larger than that in a similar apparatus operated from a 3 V supply since the current used is a function of the voltage supply magnitude. As a consequence of higher power operation the life of batteries are shortened.

Additionally, most ICs of the 5 V type have an operating voltage specification of  $5\text{ V} \pm 10\%$ . When using a pair of lithium batteries in series it is possible to produce a supply voltage of up to 7 V. Therefore, it has been necessary to provide a circuit for regulating the supply voltage, in a two battery system, to a value within the operating voltage range of these ICs. This regulator circuit is typically a separate IC. Use of a separate regulator IC is burdensome because the system becomes larger, and more costly to manufacture.

One approach to providing appropriate voltages without using a second battery cell has been to add a DC-DC converter IC to the system. The DC-DC converter can provide the voltage required by peripherals such as RAMs. However there are several problems with this approach. First, the additional DC-DC converter IC limits miniaturization of the system housing. Second, this additional chip increases manufacturing costs. Third, when the DC-DC converter output is used to power a peripheral chip, interfacing between chips with different supply voltages leads to a mismatch in logic levels. Fourth, there is a diode leakage pathway between the two voltage supply nodes which gives rise to battery-draining parasitic currents.

Any approach that requires more battery cells or more ICs means that miniaturization of the housing becomes difficult.

Therefore a need exists in low-power systems, for a means to combine ICs having different power supply requirements, with only one low voltage supply, such as

a battery, in the system, while simultaneously eliminating the need for costly additional components that consume space and power. There further exists a need for a means to interface circuits having different logic level voltages while still ensuring noise margin.

### SUMMARY OF THE INVENTION

It is an object of the present invention to provide circuitry, for battery-powered electronic systems in which ICs of low and high voltage specifications can be operated simultaneously by a single low voltage power supply, wherein prolongation of battery life, miniaturization of housing size and reduction of manufacturing costs are achieved.

Accordingly, the present invention comprises on a first IC, a monolithically integrated charge pump circuit for boosting an external supply voltage so as to output a voltage greater than that of the external supply, and a power supply multiplexor for selecting between the charge pump output and the external supply in accordance with a power supply select control signal. The output of the multiplexor is used as a supply voltage, to at least one other IC in the system, and also to those internal input and output circuits that interface with the other IC. The external IC(s) gain access to the multiplexor output voltage through an output terminal.

A voltage regulation circuit may be used to provide control over the charge pump circuit output. In this case, the external power supply is regulated into a constant voltage by the voltage regulator circuit and the regulator output becomes the input to the charge pump circuit. By using a regulator between the external supply and the charge pump input, the output voltage of the charge pump circuit is made stable. Alternatively, a voltage regulation circuit may be used on the output side of the charge pump. There is no particular advantage or disadvantage in choosing either configuration. Of, course, when this circuit is added, total current consumption is increased.

The voltage selection process is dynamically determined based on the time-varying requirements of system operation. For example, a low voltage will be selected to power an external memory IC when that IC is merely maintaining information, and a high voltage will be selected when the memory IC is being accessed for a read or a write cycle. More specifically, in a memory device such as a static RAM, a low voltage is required for holding data, while a high voltage is required for reading/writing data. When the static RAM is standing by, the low voltage power supply voltage, is connected to the power supply terminal through the power supply multiplexor circuit, but when reading or writing data, the high voltage output of the charge pump or the voltage regulator, is connected to the power supply terminal. The power supply multiplexor is switched according to need, thus realizing low current consumption.

An advantage of the present invention is the elimination of components used in previous approaches. For example, utilizing the present invention, only one battery is needed to operate a system that previously required either two batteries and a voltage regulator, or one battery and a DC-DC converter IC. Elimination of these components reduces manufacturing costs and permits miniaturization of the apparatus.

A further advantage of the present invention is the reduction in power consumption achieved by operating at high voltage only those circuit elements that require

high voltage and only for the short periods of time when necessary for proper operation of those circuit elements.

According to a further aspect of the present invention, the charge pump circuit includes an enable/disable circuit for stopping the charge pump clocks. Therefore, the charge pumping operation can be stopped when it is not needed for proper system operation (e.g. high voltage operations will not be undertaken). In this way it is possible to realize additional reductions in current consumption.

According to another aspect of the present invention, the first IC further comprises an input circuit and/or an output circuit to which the driving voltage is supplied from the power supply multiplexor circuit. An interface between the first IC and the external IC is provided which has improved noise margin because the I/O circuits of the first IC operate from the same supply voltage as the external IC.

According to a still further aspect of the present invention, the system comprises a single-chip microcomputer and at least one memory device. The single-chip microcomputer includes a CPU, a charge pump circuit, an external accumulating capacitor and an external boosting capacitor, for boosting a power supply voltage, a power supply multiplexor circuit for selecting between the charge pump output and the power supply voltage in accordance with a voltage select control signal, at least one of an input circuit supplied with the multiplexor output voltage for supplying an input signal to the CPU and an output circuit supplied with the multiplexor output voltage for sending out a signal from the CPU, and a power supply terminal to which the multiplexor output voltage is supplied.

The external IC, which may be a memory device, is connected to at least one input and one output circuit of the single-chip microcomputer, and uses the selectable supply voltage output via the power supply terminal. When the external device is in stand-by mode the selectable supply voltage output provides a low voltage to the external IC as well as to the internal input and output circuits. However, when the external device is in active mode the selectable supply voltage output provides a high voltage to the external IC as well as to the internal input and output circuits.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the connectivity between ICs in one embodiment of the present invention.

FIG. 2 is a block diagram illustrating some of the details of a low-power single-chip microcomputer embodying the charge pumping and voltage selection aspects of the present invention.

FIG. 3 is a circuit diagram, including transistor sizes, illustrating details of the charge pumping (boosting) circuit in the low-power microcomputer of FIG. 2.

FIG. 4 is a circuit diagram, including transistor sizes, illustrating the voltage level converter circuit.

FIG. 5 is a timing diagram illustrating the timing of the boosting clock signals used to drive the charge pump circuit.

FIG. 6 is a circuit diagram illustrating how the accumulating capacitor and boosting capacitor are electrically connected at time  $t_c$  shown in FIG. 5.

FIG. 7 is a circuit diagram illustrating how the accumulating capacitor and boosting capacitor are electrically connected at time  $t_c$  shown in FIG. 5.

FIG. 8 is a circuit diagram illustrating in detail the boosting circuit in the low-power microcomputer along with the voltage regulation aspect of the present invention.

FIG. 9 is a circuit diagram, including transistor sizes, illustrating the constant voltage circuit in the embodiment of FIG. 8.

#### DETAILED DESCRIPTION OF THE INVENTION

A system embodying the present invention is now described with reference to the drawings wherein like reference numerals refer to like parts throughout the drawings.

##### I. Circuit Connections

FIG. 1 shows a low-power single-chip microcomputer 10 and a 64K RAM (hereinafter referred to as "external IC") 12 connected to each other by means of data lines and control lines. A DC power supply 14, having a first and second terminal wherein the first terminal is positive with respect to the second terminal, is included in the system such that the positive supply terminal is connected to the respective  $V_{DD}$  power supply terminals 11, 13 of single-chip microcomputer 10 and external IC 12. The negative terminal of DC power supply 14 is connected to power supply terminal  $V_{SS}$  of single-chip microcomputer 10.

Accumulating capacitor 16 is connected between the positive terminal of DC power supply 14 and the power supply terminal  $V_{SS}$  of single-chip microcomputer 10, and boosting capacitor 18 is connected between terminals C1 and C2. In the preferred embodiment both capacitors are approximately 10 microFarad. Microcomputer output terminal VOUT, is connected to power supply terminal  $V_{SS}$  of external IC 12.

FIG. 2 illustrates further detail of single-chip microcomputer 10 wherein oscillator circuit 22 in conjunction with crystal 20 supplies an output oscillation signal to clock generator 24. Clock generator 24 generates timing signals in accordance with the oscillation signal, and supplies one of those timing signals to CPU 26. CPU 26 receives input data from input circuit 30 through data bus 28. Input circuit 30 is connected to input terminal 32, and input terminal 32 is connected to external IC 12. In other words, input circuit 30 receives data from external IC 12 through input terminal 32.

Operation results from CPU 26 are transferred to output register 33 by means of data bus 28 so as to make output register 33 supply the operation result stored therein to output circuit 34 at a predetermined time. Output circuit 34 is connected to output terminal 36 so as to supply data to external IC 12.

Power supply select control register 38 receives and stores power supply signal 39 supplied from CPU 26 through data bus 28, and outputs power supply select control signal 39 to power supply multiplexor circuit 40 to control the operation of multiplexor circuit 40.

Charge pump enable register 42 receives and stores boost control signal 43 supplied from CPU 26 through data bus 28.

Charge pump circuit 44 is connected to accumulating capacitor 16 through terminal  $V_{SS2}$ , and connected to boosting capacitor 18 through terminals C1 and C2. Charge pump circuit 44 is supplied with charge pump

enable signal 43 from charge pump enable register 42 and boosting clock signals 24a, 24b from clock generator 24. Charge pump circuit 44 boosts the power supply voltage and supplies the boosted voltage to power supply multiplexor circuit 40.

Power supply multiplexor 40 receives a select control signal 39, and two power supplies as inputs, one power supply is the voltage applied to terminal  $V_{SS}$ , and the second is the boosted voltage from charge pump circuit 44. Power supply multiplexor 40 produces as its output (the driving voltage), a selected one of its two inputs based on the state of select control signal 39. The output of power supply multiplexor 40 is connected to terminal  $V_{OUT}$ . The output of power supply multiplexor 40 is also connected to interface input and output circuits 30, 34.

The details of output circuit 34, are shown in FIG. 3. Output circuit 34 is comprised of voltage level conversion circuit 51, inverter 52 and output transistor circuit 53 which is comprised of a pair of FETs.

Charge pump circuit 44, shown in FIG. 3, is comprised of AND gates 54, 55, voltage level conversion circuits 56, 57, inverters 58, 59, MOSFETs 60, 61, 62, 63, 64, 65 and diode 66.

Multiplexor circuit 40, shown in FIG. 3, is comprised of a voltage level conversion circuit 67, inverters 68, 69 and a switching circuit 72 which itself is comprised of a pair of MOSFETs 70, 71.

FIG. 4 shows configuration details of the voltage level conversion circuits 51, 56, 57 and 67. Each voltage level conversion circuit is comprised of an inverter 81 and MOSFETs 82, 83, 84, 85, 86, 87. The source of MOSFET 84 is connected to a charge pump output terminal  $V_{SS2}$ . For example, in voltage level conversion circuit 56, if a clock signal of  $-3$  V is supplied to an input terminal I thereof, a clock signal of  $-6$  V is extracted from an output terminal thereof.

## II. Circuit Operation

### Charge Pump/Voltage Boosting Circuit

The present invention includes a monolithically integrated means of producing a DC power supply voltage greater in magnitude than the external power supply. In one embodiment of the present invention a charge pumping type circuit is used to produce this new DC power supply voltage, which is typically about twice the magnitude of the external supply.

This new voltage is used when required to interface with other system elements. External RAM chips, for example, may require a higher voltage to read and write than they do simply to maintain data. Since lower power consumption, and hence longer battery life are achieved via the use of lower supply voltages, it is advantageous to equip the system with one low voltage supply and generate a higher voltage low current supply for those occasions that warrant higher voltage operation.

FIG. 5, shows the timing of boosting clocks 24a, 24b which are output from clock generator 24. Boosting clocks 24a, 24b are generated so as to be non-overlapping. Three distinct timing regions,  $t_a$ ,  $t_b$ , and  $t_c$ , can be seen in FIG. 5. In time region  $t_a$ , boosting clock 24a is low, and 24b is high. In time region  $t_b$ , boosting clock 24a is low, and 24b is low. In time region  $t_c$ , boosting clock 24a is high, and 24b is low. If both clocks 24a, 24b were allowed to go high simultaneously, boosting capacitor 18 would be effectively shorted out.

To enable charge pump circuit operation, charge pump enable signal 43, which is output from charge pump enable register 42, should be logically high. Table I shows the ON/OFF state of the transistors in the charge pump circuit at the times  $t_a$ ,  $t_b$ , and  $t_c$ .

TABLE I

TIME = $t_a$	TIME = $t_b$	TIME = $t_c$
MOSFET 60- ON	MOSFET 60- OFF	MOSFET 60- OFF
MOSFET 61- OFF	MOSFET 61- OFF	MOSFET 61- ON
MOSFET 62- ON	MOSFET 62- OFF	MOSFET 62- OFF
MOSFET 63- OFF	MOSFET 63- ON	MOSFET 63- ON
MOSFET 64- ON	MOSFET 64- OFF	MOSFET 64- OFF
MOSFET 65- OFF	MOSFET 65- OFF	MOSFET 65- ON

At time  $t_a$  boosting clocks 24a, 24b are supplied to voltage level conversion circuits 56, 57 through AND gates 54, 55 respectively, and the output of AND gate 54 also drives the gate of MOSFET 61. Clock signal 24a, after being level-converted by voltage level conversion circuit 56, is supplied to the gate of MOSFET 65 through inverter 58. Clock signal 24b, after being level-converted by voltage level conversion circuit 57, is supplied through inverter 59 to the respective gates of MOSFETs 60, 62, 63.

With clock signals 24a, 24b in the time= $t_a$  state, MOSFETs 61, 63, 65 are turned OFF, and MOSFETs 60, 62, 64 are turned ON. As a result, a closed circuit is formed through the power supply terminal  $V_{DD}$ , MOSFET 60, terminal C1, boosting capacitor 18, MOSFET 64, and power supply terminal  $V_{SS}$ . By the formation of this closed circuit, a charging current is supplied from DC power supply 14 to boosting capacitor 18.

FIG. 6 shows the state of connection of accumulating capacitor 16 and boosting capacitor 18 at time  $t_a$ . Boosting capacitor 18 is charged so that the voltage across it is equal to the voltage of DC power supply 14. At this time, the boosting power supply terminal  $V_{SS2}$  of accumulating capacitor 16 is opened to DC power supply 14.

At time  $t_b$ , as shown in FIG. 5, the potential of boosting clock 24a is changed, so that MOSFETs 60, 61, 62, 64, 65 are turned OFF leaving only MOSFET 63 turned ON. Under such conditions both accumulating capacitor 16 and boosting capacitor 18 are opened to DC power supply 14.

At time  $t_c$ , as shown in FIG. 5, the respective potentials of boosting clocks 24a, 24b are reversed from their values at time  $t_a$ . This results in MOSFETs 60, 62, 64 being OFF, and MOSFETs 61, 63, 65 being ON. Consequently, a closed circuit is formed through power supply terminal  $V_{DD}$ , accumulating capacitor 16, boosting output terminal  $V_{SS2}$ , MOSFET 65, terminal C2, boosting capacitor 18, terminal C1, MOSFET 61, and power supply terminal  $V_{SS}$ . FIG. 7 shows how accumulating capacitor 16 and boosting capacitor 18 are electrically connected at time  $t_c$ . When the electrical connections described herein are made, charge stored in boosting capacitor 18 is discharged to  $V_{SS}$ , thus creating a short-lived charging current in accumulating capacitor 16.

By repeating the cycle described above, the potential of boosting output terminal  $V_{SS2}$  becomes approximately twice the potential difference between  $V_{SS}$  and  $V_{DD}$  or about  $-6$  V in this example. The voltage available at boosting output terminal  $V_{SS2}$  can be supplied through MOSFET 71 to input circuit 30, output transistor circuit 53 and external IC power supply terminal  $V_{OUT}$ . This is accomplished when power supply select

control signal 39, which originates from power supply select control register 38, is level-converted by means of voltage level conversion circuit 67, and the level-converted voltage select control signal is supplied to the gates of MOSFETs 70, 71 by means of inverters 68, 69 so that MOSFET 71 is in an ON state. It follows that input circuit 30, output circuit 34 and external IC 12 can be driven by the 6 V power supply.

The interface-level-matching between a 3 V system ( $V_{SS}$  system) and a 6 V system ( $V_{SS2}$  system) in charge pump circuit 44, output circuit 34 and power supply multiplexor circuit 40 is performed by voltage level conversion circuits 51, 56, 57 and 67 shown in FIG. 3. The purpose of the voltage level conversion circuits is to convert low voltage amplitude signals, (e.g. 3 V), to high voltage amplitude signals (e.g. 5 V). No level conversion circuit is provided in input circuit 30. The 6 V input signal amplitude presented to input circuit 30 from the external IC is connected to the gate of a MOSFET (not-shown) which itself is connected across the low voltage supply of the 3 V  $V_{SS}$  system. Typically, a voltage in the neighborhood of 6 V poses no problem, such as dielectric breakdown, for the MOSFET and therefore no reason exists to level shift the input voltage to a lower value. However, if any gate in this circuit cannot tolerate an applied voltage in the neighborhood of 6 V, then it would be necessary to provide the voltage level conversion circuit of FIG. 4, in input circuit 30.

When charge pump enable signal 43 and power supply select control signal 39 become logically low signals (OFF signals), charge pump circuit 44 stops its charge pumping operation, and MOSFETs 70, 71 become ON and OFF respectively, so that the nominal 3 V supply is connected to input circuit 30, output transistor circuit 53 and external IC power supply terminal  $V_{OUT}$ .

Input noise margin is assured because input circuit 30 and output circuit 34 operate with the same voltage as the external IC 12. That is, not only is the voltage level optimized to operate the external IC 12 with low power consumption, but an improved interface with respect to noise margin is provided.

In the above-described embodiment, charge pump enable signal 43 and power supply select control signal 39 are produced independently of each other so that charge pump enable signal 43 can be produced first. This provides for the stabilization of the charge pump circuit 44 output prior to its use.

If the operating time until the stabilization is established is very short, then charge pump enable signal 43 and power supply select control signal 39 may be one and the same signal.

In this case, MOSFET 93 is not necessary, and the source of MOSFET 102 is connected to power supply terminal  $V_{SS}$ .

### III. The Present Invention with a Constant Voltage Source

The present invention may also include the use of a voltage regulation circuit, for example the constant voltage circuit shown in FIG. 9 and described in detail below, to provide a stable output voltage. In this case, a substantially constant output voltage can be obtained by a constant voltage (voltage regulation) circuit even if the external power supply varies over a broad range. Therefore, the voltage supplied to the external IC power supply terminal  $V_{OUT}$  is stable. This feature is

particularly important if the operating voltage range specification of the external IC is narrow.

Another embodiment of the present invention, which includes a constant voltage circuit, is shown in FIG. 8. This IC includes voltage level conversion circuit 91, which receives the output of AND gate 54 as its input. The output of voltage level conversion circuit 91 is supplied through inverter 92 to the gate of MOSFET 93. The drain of MOSFET 93 is connected to constant voltage circuit 94, and the source of MOSFET 93 is connected to terminal  $V_{SS2}$ .

FIG. 9 shows the detailed configuration of constant voltage circuit 94. Constant voltage circuit 94 is comprised of reference voltage generation circuit 95, differential amplifier 96 and feedback amplifier resistor 97.

Reference voltage generation circuit 95 is comprised of MOSFETs 100, 101, 102, 103 of which MOSFETs 100, 101 are depletion type MOSFETs. The threshold voltage of the depletion type MOSFETs is preferably about  $-0.55$  V.

Differential amplifier 96 is comprised of MOSFETs 104, 105, 106, 107, 108. Feedback amplifier resistor 97 is comprised of resistors R1 and R2 so that a signal related to the output voltage of differential amplifier 96 is fed back to differential amplifier 96.

In one embodiment, the gate materials of MOSFETs 100 and 101 are P-type Poly-Si and N-type Poly-Si respectively, and MOSFETs 100, 101 are the same in their transistor size, substrate density (i.e. substrate doping concentration), and the like. The work function difference between the P-type Poly-Si and the N-type Poly-Si,  $V_{ref}$  (about 1.05 V), is output from reference voltage generation circuit 95 as  $(V_{DD} - V_{ref})$ . Differential amplifier 96 receives the output of reference voltage generation circuit 95 as a reference signal to thereby perform differential amplification, so that differential amplifier 96 outputs a constant voltage output  $V_0 = V_{ref}(R_1 + R_2)/R_1$ .

Therefore, by setting this constant voltage output  $V_0$  to, for example, 5 V, the voltage  $-5$  V is applied through a MOSFET 71 to input circuit 30, output transistor circuit 53 and external IC 12 respectively, so that they are driven by this regulated voltage.

It will be readily apparent to those skilled in the art that provision of a constant voltage circuit 94, will enhance system operation when the external power supply varies over a broad range. Particularly when the operating voltage range specification of an external IC is narrow, it is possible to make it operate stably by providing to the external IC power supply terminal  $V_{OUT}$  a well-regulated supply voltage.

Although, an input terminal and an output terminal are provided in the above embodiment, the present invention can be applied to situations in which only one terminal is provided for common use as an input and an output.

Integration of the present invention into a microcomputer is particularly effective because control means for a charge pump circuit, a power supply multiplexor circuit and so on can be easily realized in the form of software.

While the invention has been described in conjunction with several specific embodiments, it will be evident to those of ordinary skill in the art that many further alternatives, modifications and variations will be apparent in light of the foregoing description. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and varia-

tions that may fall within the spirit and scope of the appended claims.

What is claimed is:

1. An integrated circuit comprising:
  - a) a charge pump circuit, connected to a first power supply voltage node, for producing a boosted power supply voltage as an output; and
  - b) a power supply multiplexer circuit, having said charge pump output and said first power supply voltage node connected as inputs, for selecting between said charge pump output and said first power supply voltage node to thereby output a selected one of said inputs;
  - c) a power supply terminal for supplying said power supply multiplexer output to other integrated circuits provided externally; and
  - d) at least one input circuit having power supply terminals wherein said multiplexer output voltage is connected to supply power to said input circuit.
2. The integrated circuit of claim 1 further comprising at least one output circuit having power supply terminals wherein said multiplexer output voltage is connected to supply power to said output circuit power supply terminals.
3. The integrated circuit of claim 1 wherein said charge pump circuit includes an enable/disable circuit for discontinuing operation of said charge pump circuit.
4. An integrated circuit comprising:
  - a) a constant voltage circuit connected to an external power supply for outputting an internal power supply voltage of a substantially constant value;
  - b) a charge pump circuit connected to said internal power supply voltage to thereby output a voltage higher than said internal power supply voltage; and
  - c) a power supply multiplexer circuit, having said charge pump output and said power supply voltage connected as inputs, for selecting between said charge pump output and said power supply voltage to thereby output a selected one of said inputs.
5. An integrated circuit comprising:
  - a) a charge pump circuit connected to a power supply voltage to thereby output a voltage higher than said power supply voltage;
  - b) a constant voltage circuit connected to said charge pump output for outputting a substantially constant voltage higher than said power supply voltage; and
  - c) a power supply multiplexer circuit for selecting between the output of said constant voltage circuit and said power supply voltage in accordance with a voltage select control signal supplied thereto to thereby output, a selected one of the output voltage of said constant voltage circuit and said power supply voltage.
6. The integrated circuit of claim 5 further comprising a power supply terminal for supplying said driving voltage from said power supply multiplexer circuit to external integrated circuits.
7. The integrated circuit of claim 6 further comprising at least one input circuit to which said driving voltage is supplied from said power supply multiplexer circuit.
8. The integrated circuit of claim 6 further comprising at least one output circuit to which said driving voltage is supplied from said power supply multiplexer circuit.
9. The integrated circuit of claim 5 wherein said charge pump circuit includes an enable/disable circuit for discontinuing charge pump operation.

10. A low-power electronic system comprising:
  - a) a single-chip microcomputer having a CPU, a charge pump circuit connected to a power supply voltage for producing a voltage greater than said power supply voltage, a power supply multiplexer circuit for selecting between the output voltage of said charge pump circuit and said power supply voltage in accordance with a voltage select control signal supplied thereto to thereby output, as a driving voltage, a selected one of said charge pump output and said power supply voltage, at least one of an input circuit supplied with the driving voltage from said power supply multiplexer circuit for supplying an input signal to said CPU and an output circuit supplied with the driving voltage from said power supply multiplexer circuit for sending out an output signal from said CPU, and a power supply terminal to which said power supply multiplexer output is supplied; and
  - b) a memory device connected to said input and output circuits of said single-chip microcomputer, and supplied with said driving voltage from said power supply terminal.
11. The system of claim 10 wherein said single-chip microcomputer further comprises a power supply control multiplexer register for storing said voltage select control signal supplied from said CPU and for supplying said voltage select control signal to said power supply multiplexer circuit.
12. The system of claim 10 in which said single-chip microcomputer further includes a power supply control multiplexer register for storing a charge pump enable signal supplied from said CPU and for supplying said charge pump enable signal to said charge pump circuit.
13. The system of claim 10 wherein said single-chip microcomputer further includes voltage level conversion circuits connected between said single-chip microcomputer and a lower voltage circuit system and between said single-chip microcomputer and a high voltage circuit system.
14. A method of reducing power consumption in an electronic system having a low voltage power supply and at least two integrated circuits, portions of which are operable at low voltage for certain functions and require high voltage for other functions, comprising the steps of:
  - a) generating a high voltage power supply from said low voltage power supply within a first one of said at least two integrated circuits;
  - b) determining, within said first integrated circuit when said high voltage is required for proper system operation;
  - c) switching a power supply multiplexer circuit output from said low voltage power supply to said high voltage power supply; and
  - d) supplying said high voltage power supply to a second one of said at least two integrated circuits and to a first portion of said first integrated circuit; wherein said first portion comprises interface circuitry for communicating with said second integrated circuit, and said interface circuitry is electrically connected to said second integrated circuit.
15. The method of claim 14, further comprising the steps of:
  - a) determining when low voltage operation will result in power consumption savings; and

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b) switching from said high voltage power supply to said low voltage power supply to drive said circuit elements.

16. A method of reducing power consumption in an electronic system having a low voltage power supply and at least two integrated circuits, portions of which are operable at low voltage for certain functions and require high voltage for other functions, comprising the steps of:

- a) regulating said low voltage supply to produce a substantially constant voltage output;
  - b) generating a high voltage power supply from said substantially constant voltage output within a first one of said at least two integrated circuits;
  - c) determining, within said first integrated circuit when said high voltage is required for proper system operation;
  - d) switching a power supply multiplexer circuit output from said low voltage power supply to said high voltage power supply; and
  - e) supplying said high voltage power supply to a second one of said at least two integrated circuits and to an interface circuit within said first integrated circuit;
- wherein said interface circuit communicates with said second integrated circuit, and said interface circuit is electrically connected to said second integrated circuit.

17. A method of reducing power consumption in an electronic system having a low voltage power supply

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and at least two integrated circuits, portions of which are operable at low voltage for certain functions and require high voltage for other functions, comprising the steps of:

- a) generating a high voltage power supply from said low voltage power supply within a first one of said at least two integrated circuits;
- a) regulating said high voltage supply to produce a substantially constant high voltage output;
- c) determining, within said first integrated circuit when said substantially constant high voltage is required for proper system operation;
- d) switching a power supply multiplexer circuit output from said low voltage power supply to said substantially constant high voltage power supply; and
- e) supplying said high voltage power supply to a second one of said at least two integrated circuits and to a first portion of said first integrated circuit; wherein said first portion comprises interface circuitry for communicating with said second integrated circuit, and said interface circuitry is electrically connected to said second integrated circuit.

18. The method of claim 17 further comprising the step of disabling operation of high voltage generation circuitry when said operation is not required for proper system operation and cessation will result in power savings.

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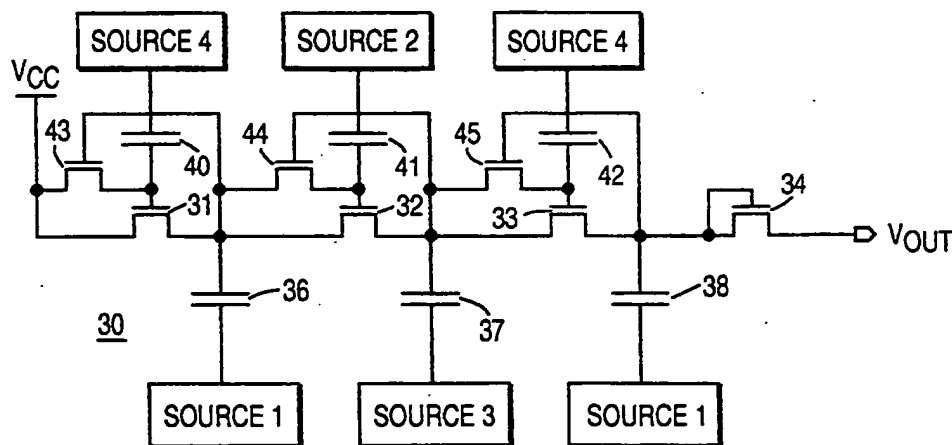
**United States Patent** [19]

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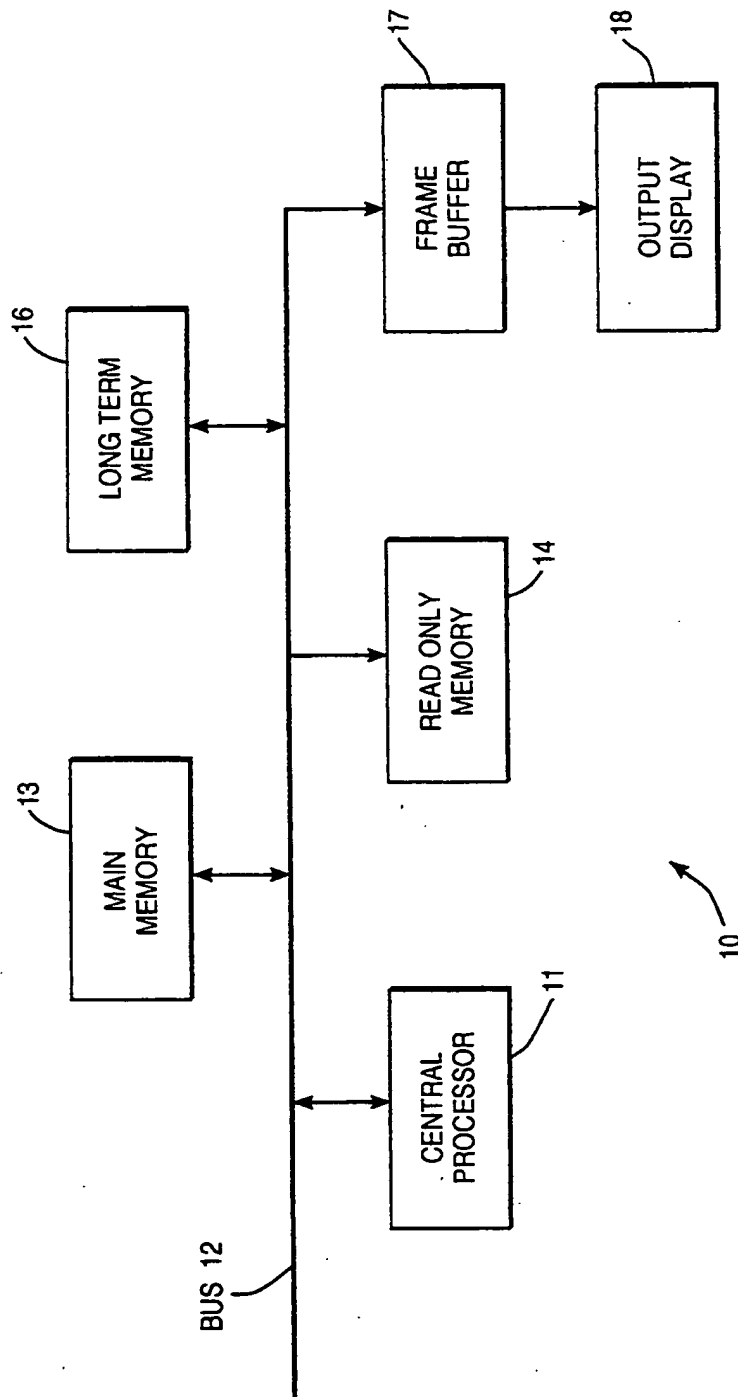
[11] **Patent Number:** 5,422,586[45] **Date of Patent:** Jun. 6, 1995[54] **APPARATUS FOR A TWO PHASE  
BOOTSTRAP CHARGE PUMP**[75] **Inventors:** Kerry D. Tedrow, Orangevale;  
Jahanshir J. Javanifard, Sacramento;  
Cesar Galindo, Stockton, all of Calif.[73] **Assignee:** Intel Corporation, Santa Clara, Calif.[21] **Appl. No.:** 119,423[22] **Filed:** Sep. 10, 1993[51] **Int. Cl.<sup>6</sup>** ..... G11C 7/00; G11C 16/02[52] **U.S. Cl.** ..... 327/306; 327/261;  
327/141; 327/100; 327/185[58] **Field of Search** ..... 327/306, 261, 141, 100,  
327/185; 365/226[56] **References Cited****U.S. PATENT DOCUMENTS**5,153,854 10/1992 Herold .  
5,157,278 10/1992 Min et al. .  
5,243,561 9/1993 Yamauchi .  
5,245,572 9/1993 Kosonocky et al. .  
5,276,646 1/1994 Kim .  
5,313,429 5/1994 Chevallier et al. .**OTHER PUBLICATIONS**1992 IEEE International Solid-State Circuits Conference, ISSCC 92 Session 9/Non-Volatile and Dynamic Rams/Paper 9.3, "TP9.3: A 5V-Only 0.6  $\mu$ m Flash EEPROM with Row Decoder Scheme in Triple-Well Structure", Masao Kuriyama, Shigeru Atsumi, Akira Umezawa, Hironori Banba, Ken-ichi Imamiya, Kiyomi Naruke, Seiji Yamada, Etsushi Obi, Masamitsu Oshikiri, Tomoko Suzuki, Sumio Tanaka, pp. 152, 153.*Primary Examiner*—William L. Sikes*Assistant Examiner*—Fetsum Abraham*Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman[57] **ABSTRACT**

An integrated circuit charge pump circuit including a plurality of stages, each stage including a first N type field effect switching transistor device having source and drain terminals connected in series with the source and drain terminals of all other stages, a second N type field effect control transistor device having drain and source terminals connecting the drain terminal and the gate terminal of the first switching transistor device, and a storage capacitor joined to the source terminal of the first device; a source of voltage to be pumped is connected to the drain terminal of the first device of the first stage. A first series of clock pulses is applied to the gate terminals of the first switching transistor devices in every other stage of the charge pump and to the gate terminals of the second control transistor devices in stages between; and a second series of clock pulses which do not overlap the first series of clock pulses is applied to the gate terminals of the first switching transistor devices in alternate stages of the charge pump and to the gate terminals of the second control transistor devices in stages between the alternate stages. These pulses cause the switching transistor to switch on and off in alternate stages in a manner that the gate terminal goes higher than the drain terminal so that charge is transferred without threshold drop between stages and high current as well as high voltage is pumped to the output terminal.

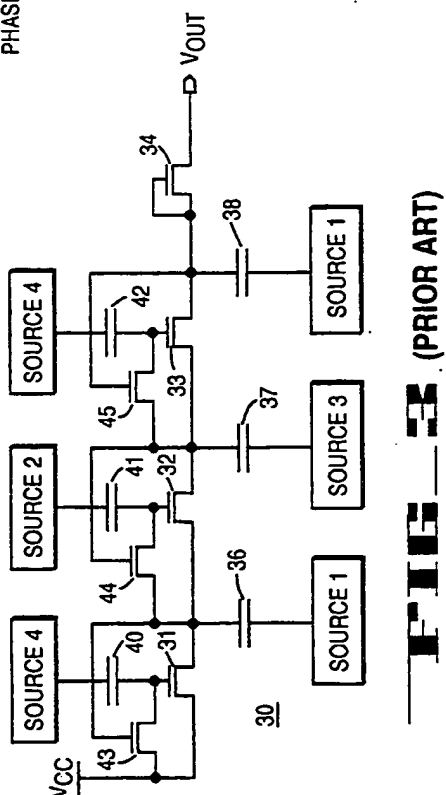
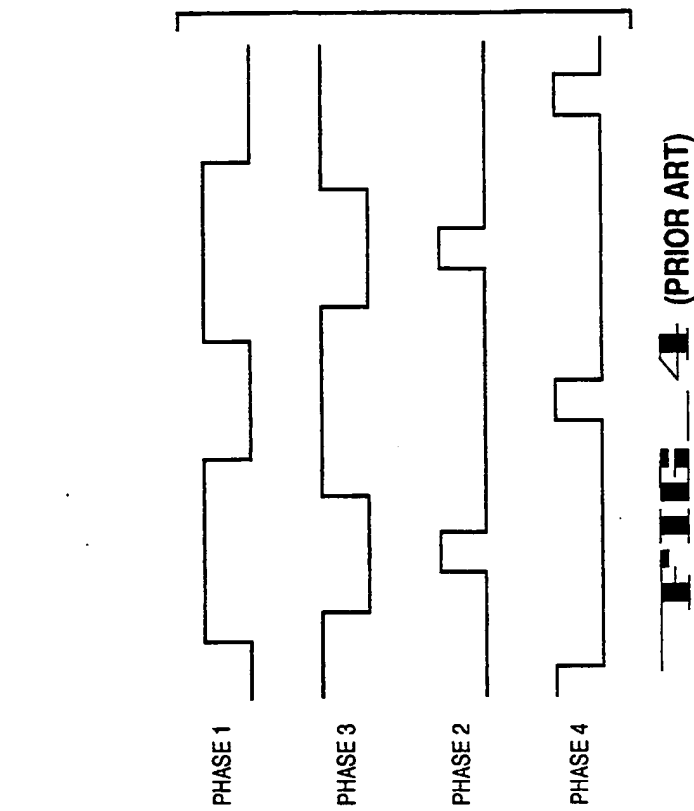
9 Claims, 4 Drawing Sheets







**FIG. 1**



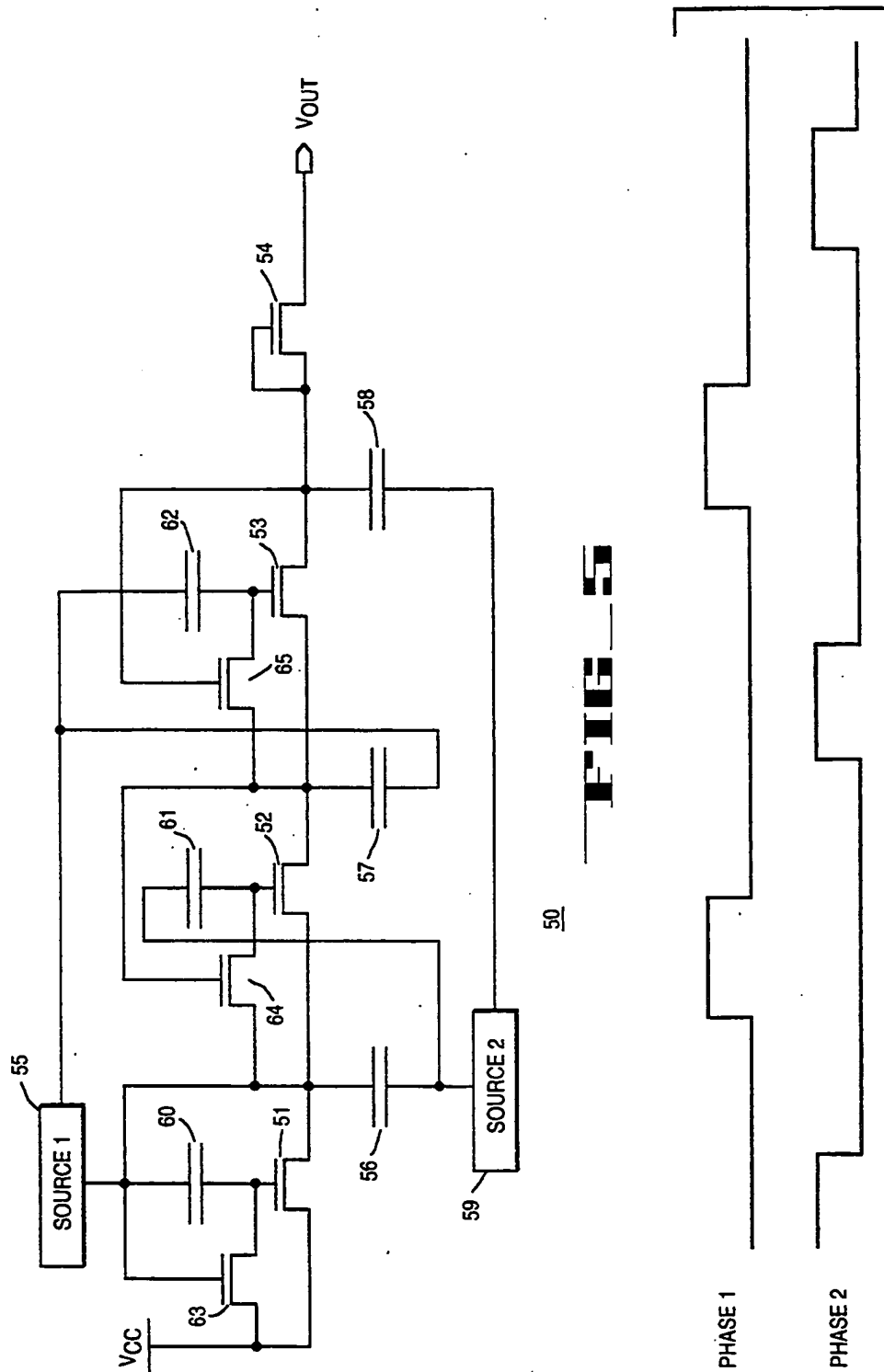
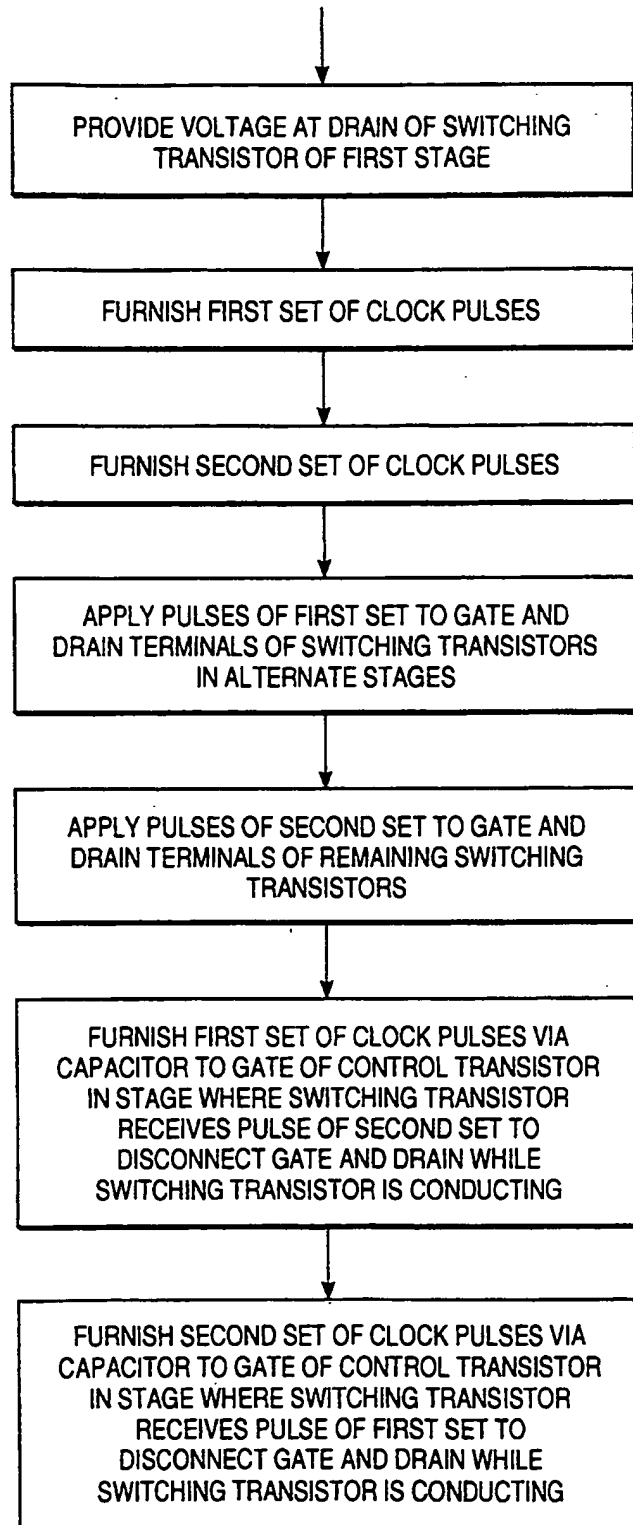


FIG 5

FIG 6

**FIG. 7**

## APPARATUS FOR A TWO PHASE BOOTSTRAP CHARGE PUMP

### BACKGROUND OF THE INVENTION

#### 1. Field Of The Invention

This invention relates to computer systems and, more particularly, to methods and apparatus for providing a charge pump for generating high voltages and high currents for erasing and programming flash electrically-erasable programmable read only memory arrays (flash EEPROMs).

#### 2. History of the Prior Art

It has been found that the use of computers has grown so extensive that the power used by these computers has become significant. In order to reduce the cost of operation as well as the consequent use of energy resources, a substantial move is underway to reduce this power usage. A major trend in the manufacture of personal computers is toward the reduction in the voltage level required to operate the integrated circuits which are used in the various components of those computers. A simultaneous trend is the desire to provide portable computers which are able to provide most of the abilities of desktop computers but are assembled in very small and light packages. This has led to attempts to reduce the power used by portable computers so that their battery life will be extended.

In order to reduce power consumption and extend battery life, much of the integrated circuitry used in personal computers is being redesigned to run at low voltage levels. This reduces the power usage and allows more components to be placed closer to one another in the circuitry. The circuitry and components used in portable computers are being designed to operate at voltages levels such as 5 volts and 3.3 volts. This helps a great deal to reduce the power needs of personal computers.

However, at the same time, the desire to offer more features in portable computers opposes this salutary result. Many of the features require higher voltages to function. For example, one real convenience is the ability to change the basic input/output and startup (BIOS) processes as improvements in a computer or its peripherals occur. Historically, this has been accomplished by removing the electrically programmable read only memory (EPROM) or similar circuitry providing the read only memory for storing the BIOS processes and replacing it with new circuitry at additional cost. This is a complicated operation beyond the abilities of many computer users. Recently, flash electrically-erasable programmable read only memory (flash EEPROM memory) has been used to store BIOS processes. This memory may be reprogrammed without removing the BIOS circuitry from the computer by running a small update program when the BIOS processes are changed. However, reprogramming flash EEPROM memory requires approximately twelve volts to accomplish effectively; and the lower voltage batteries provided in personal computers are not capable of programming and erasing flash EEPROM memory.

Another form of flash EEPROM memory array provides another example of high voltage requirements in portable computers. Recently, a new form of long term random access storage has been devised using flash EEPROM memory arrays. An example of a flash EEPROM memory array which may be used in place of a hard disk drive is given in U.S. patent application Ser.

No. 07/969,131, entitled *A Method and Circuitry For A Solid State Memory Disk*, S. Wells, filed Oct. 31, 1992, and assigned to the assignee of the present invention. These arrays provide a smaller lighter functional equivalent of a hard disk drive which operates more rapidly and is not as sensitive to physical damage. Such memory arrays are especially useful in portable computers where space is at a premium and weight is extremely important. However, these flash EEPROM memory arrays also require much higher voltages for writing and erasing data than can be provided directly by the batteries of portable computers. In situations in which batteries do not provide sufficient voltages, it has been typical to provide charge pumps to generate higher voltage from the lower voltages available. However, although such voltage pumps are able to increase the voltage to an appropriate level, prior art charge pumps do not provide sufficient current to generate the power for effectively erasing and programming flash EEPROM memory without the use of very large capacitors which utilize an inordinate amount of die space.

### SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide integrated circuitry charge pumps capable of providing sufficient power to effectively erase and program flash EEPROM memory arrays.

It is another, more specific, object of the present invention to provide a highly efficient bootstrap charge pump circuit for generating the high voltages and currents necessary to program and erase flash EEPROM memory arrays.

These and other objects of the present invention are realized in an integrated circuit which includes an integrated circuit charge pump circuit. The charge pump circuit includes a plurality of stages, each stage including a first N type field effect transistor device having gate, source, and drain terminals, a second N type field effect transistor device controlling the voltage at the gate terminal of the first device. The circuit includes means for applying a first series of clock pulses to the gate of the first device in every odd numbered stage of the charge pump and to the gate of the second device in every even numbered stage, and means for applying a second series of clock pulses which do not overlap the first series of clock pulses to the gates of the first devices in every even numbered stage of the charge pump and to the gates of the second devices in every odd numbered stage which causes the gate of the first device of each stage to tie precharged so that the first device is switched on by a higher gate voltage than drain voltage to charge the next stage of the charge pump with essentially no threshold voltage drop.

These and other objects and features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a computer system including the present invention.

FIG. 2 is a circuit diagram illustrating a first circuit functioning in accordance with the prior art.

FIG. 3 is a circuit diagram illustrating a four phase charge pump circuit.

FIG. 4 is a timing diagram useful in understanding the operation of the circuit of FIG. 3.

FIG. 5 is a circuit diagram illustrating a circuit functioning in accordance with the present invention.

FIG. 6 is a timing diagram useful in understanding the operation of the circuit of FIG. 5.

FIG. 7 is a flow chart describing a method in accordance with the present invention.

#### NOTATION AND NOMENCLATURE

Some portions of the detailed descriptions which follow are presented in terms of symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. The operations are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary or desirable in most cases in any of the operations described herein which form part of the present invention; the operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases the distinction between the method operations in operating a computer and the method of computation itself should be borne in mind. The present invention relates to a method and apparatus for operating a computer in processing electrical or other (e.g. mechanical, chemical) physical signals to generate other desired physical signals.

#### DETAILED DESCRIPTION

Referring now to FIG. 1, there is illustrated a computer system 10. The system 10 includes a central processor 11 which carries out the various instructions provided to the computer 10 for its operations. The central processor 11 is joined to a bus 12 adapted to carry information to various components of the system 10. Joined to the bus 12 is main memory 13 which is typically constructed of dynamic random access memory arranged in a manner well known to those skilled in the prior art to store information during a period in which power is provided to the system 10. Also joined to the bus 12 is read only memory 14 which may include various memory devices well known to those skilled in the art each of which is adapted to retain a particular memory condition in the absence of power to the system 10. The read only memory 14 typically stores various basic functions used by the processor 11 such as basic input/output processes and startup processes typically referred to as BIOS processes. Such memory 14 may be constructed of flash EEPROM memory cells

adapted to be modified as various ones of the BIOS processes used by a particular computer are changed. Typically, such flash EEPROM memory will include circuitry for programming and erasing the memory array. If the memory 14 is constructed of flash EEPROM memory cells, it may be modified by running an update process on the computer system 10 itself to reprogram the values stored in the memory 14.

Also connected to the bus 12 are various peripheral components such as long term memory 16 and circuitry such as a frame buffer 17 to which data may be written which is to be transferred to an output device such as a monitor 18 for display. The construction and operation of long term memory 16 (typically electro-mechanical hard disk drives) is well known to those skilled in the art. However, rather than the typical electro-mechanical hard disk drive, a flash EEPROM memory array may be used as the long term memory 16. Such flash EEPROM memory arrays are programmed and erased through techniques which utilize voltages greater than that typically available to the integrated circuits of more advanced portable computers. Such flash EEPROM memory arrays typically include circuitry for programming and erasing the memory array. Consequently, such long term memory arrays as well as memory 14 may provide circuitry in accordance with this invention for generating high voltages from the lower voltages available from their batteries.

FIG. 2 illustrates a typical prior art charge pump circuit 20. The circuit 20 includes some number of N channel field effect transistors devices (21, 22, and 23 are shown) connected with their drain and source terminals in series between a source of potential  $V_{cc}$  and an output terminal indicated at  $V_{out}$ . Capacitors 25 and 26 are utilized to provide two non-overlapping clock signals (phase 1 and phase 2) from sources not shown in the figure which vary between a low value of ground and a high value of  $V_{cc}$  in the sequence illustrated. Following the timing diagram of FIG. 2, since the gate terminal of the N device 21 is connected to its drain, the gate terminal is substantially higher than the source terminal so the N device 21 is initially on, allowing the capacitor 25 to charge to the value  $V_{cc}$  less the threshold voltage drop  $V_t$  across the device 21. The device 22 is off at this time because both input phases are low. When the phase 1 clock goes high, the high voltage at the source of the device 21 transferred by the capacitor 25 causes the device 21 to turn off. This same voltage raises the voltage at the drain and gate terminals of the device 22 so that the device 22 turns on and begins charging the capacitor 26. When the phase 1 clock goes low again, the device 22 begins to cease conducting charge to the capacitor 26; and the device 21 turns back on and begins to charge the capacitor 25.

When the phase 2 clock pulse goes high, the device 23 comes on and furnishes charge to the output terminal  $V_{out}$ . This pattern of charging continues with the voltage at the output terminal  $V_{out}$ . The voltage at this terminal will ultimately approach a value which is just less than the number of stages of the charge pump plus one multiplied by the value of the source voltage  $V_{cc}$  minus the threshold drop of each stage  $[(N+1) \times (V_{cc} - V_t)]$ .

Typically, the output terminal  $V_{out}$  furnishes the charge to a circuit which may be represented as a capacitor and which does not draw any appreciable amount of current. It may be shown that the amount of current which is transferred by this conventional

charge pump is directly related to the voltage at the output terminal Vout. The higher the voltage at the output terminal, the less current is transferred. Consequently, if the voltage at the output terminal is regulated and remains relatively high from pulse to pulse of the input clocks, once the circuit has been running for any time, then though the voltage at the output may be raised to a high value, the average current is relatively small.

If it is desired to erase or program flash EEPROM memory arrays, both high voltage and high current are required to be delivered by the charge pump. This is true because the flash EEPROM cells provide a resistive load when they are being erased. Consequently, a conventional charge pump cannot be used to provide erase or program currents to flash EEPROM memory arrays without requiring very large capacitors which occupy an inordinate amount of die space. One way in which a more efficient pump capable of furnishing a greater amount of current may be designed is to use a bootstrap type of pump. FIG. 3 illustrates a prior art first type of bootstrap pump arrangement. As is shown in FIG. 3, the pump 30 includes a number of stages of N type field effect transistors 31, 32, 33, and 34 connected in series between a source of voltage Vcc and an output terminal Vout. Phase 1 and 3 input clock signals are furnished to the circuit 30 from sources 1 and 3, respectively, via capacitors 36, 37, and 38. Phase 2 and 4 input clock signals are furnished from sources 2 and 4, respectively, by capacitors 40, 41, and 42. Each stage of the circuit 30 includes an N channel field effect transistor device 43, 44, or 45 used to control the voltage at the gate terminal of the device 31, 32, or 33 of that stage.

The four individual clock signals referred to as phase 1, phase 2, phase 3, and phase 4 are shown in FIG. 4. In order to understand the operation of the circuit 30, the operation of a single stage including the switching transistor 32 will be discussed. Following the prior art timing diagram of FIG. 4, the phase 3 and phase 4 clocks are initially high. Since the phase 3 clock is high, the control device 44 is initially on. When the phase 1 clock signal goes high, the voltage pulse applied through the capacitor 36 charges the capacitor 41 at the gate terminal of the device 32 through the device 44 to the voltage level of the drain terminal of the device 32. When the phase 3 clock then goes low, the device 44 turns off, isolating the gate of the device 32 and leaving the capacitor 41 charged. This also lowers the voltage at the source of the device 32 so that the device 32 begins to conduct. When the phase 2 clock then goes high, the voltage at the gate is appreciably higher than at the drain because of the precharging of the capacitor 41. This turns the device 32 on in the region in which it experiences no threshold voltage (Vt) drop. The elimination of the Vt drop means that the circuit can provide increased current from the capacitor 36 to the next stage. The high voltage at the capacitor 36 begins to charge the capacitor 37 and to the capacitor 42 through the device 45 very rapidly.

When the phase 2 clock then goes low, the device 32 begins to go off. When the phase 3 clock goes high, the device 44 turns on discharging the gate of the device 32 and bringing it toward the voltage of the drain so that the device 32 turns off rapidly. When the phase 1 clock then goes low, the device 32 stays off and the device 44 stays on so that the charge at the drain and gate are equalized.

Viewing the circuit as a whole, when the device 31 comes on in response to the high phase 4 clock, its gate has been charged through the device 43 which has gone off. Thus, the device 31 comes on without a Vt drop and charges the capacitor 36 and the capacitor 41 very rapidly. Then the device 31 begins to turn off as the phase 4 clock goes low. The rising phase 1 pulse completes the turnoff of the device 31 by discharging the capacitor 40 through the device 43. The high phase 1 clock continues the charging of the capacitor 41 until the drop of the phase 3 clock turns off the device 44 leaving the gate of the device 32 charged. As explained above, the lowering of the phase 3 clock begins turning on the device 32 which comes on completely without a Vt drop when the phase 2 clock goes high and the gate of the device 32 goes above the drain. This allows the rapid charge of the capacitors 37 and 42. The same sequence continues through whatever number of stages are present until the charge on the capacitor 38 is sufficient to turn on the device 34 to provide a pumped voltage level at the output of the circuit 30. It should be noted that the last stage operates in a range in which it exhibits a Vt drop.

This basic operation continues in the manner explained. The three stage pump circuit 30 illustrated in FIG. 3 furnishes approximately N (where N is the number of stages) plus one times the voltage of the source Vcc at the output terminal less the Vt drop of the device 34. For example, with Vcc equal to 4.4 volts, an output voltage of 17.1 volts is furnished at the output of the pump circuit 30. More importantly, the circuit 30 provides a more efficient operation than does the conventional pump illustrated in FIG. 2 because the circuit 30 does not have the threshold voltage drops of the circuit 20 except for the last stage. This allows it to provide more current at the output terminal. This efficiency is a result of the bootstrapping operation by which the capacitors 40, 41, and 42 are charged and then the charging path is cut off so that the charge cannot dissipate before the devices 31, 32, and 33 are turned on. The charged gate terminal forces a higher voltage on the gate terminal than the drain terminal of each switching transistor when that switching transistor is turned on causing the transistor to function without a threshold voltage drop. This increased efficiency allows the charge pump to use smaller capacitors and thus be implemented in a smaller die area on an integrated circuit.

As those skilled in the art will recognize, the four individual clock phases needed to operate the circuit 30 are very difficult to generate. The clocks are of different lengths and must be accurately overlapped in order to provide the appropriate operation of the circuit to obtain its advantageous results. In practice, it appears that such circuitry cannot be produced economically with real expectation of success. This is especially true when operating at frequencies which produce 50 ns. clock periods.

The circuit 50 illustrated in FIG. 5 may be produced economically and will provide essentially the same results as that produced by the circuit 30 of FIG. 3. The basic circuitry of FIG. 5 is similar to that utilized in FIG. 3. However, in contrast to the circuit 30 of FIG. 3, the circuit 50 includes only two sources of clock pulses. The clock pulses produced by these sources are shown in FIG. 6. These clock pulses are applied in a unique manner in order to allow the operation of the circuit 50 to produce the desired output voltages and currents. The flow chart of FIG. 7 describes this opera-

tion. The circuit 50 includes a number of stages of N type field effect transistors 51, 52, 53, and 54 connected in series between a source of voltage  $V_{cc}$  and an output terminal  $V_{out}$ . In the preferred embodiment of the circuit, the transistors 51, 52, and 53 as well as the other 5 transistors are special N type devices referred to as S type devices. S type devices are basically N type devices having a very low threshold voltage level. The use and manufacture of S type devices are described in detail in U.S. Pat. Nos. 4,052,229; 4,096,584; 4,103,189; and 5,057,715. Two phases of input clock signals (phase 1 and phase 2) are furnished to the circuit 50 from sources 55 and 59 via capacitors 56, 57, and 58. The same two phases of input clock signals are furnished from sources 55 and 59 by capacitors 60, 61, and 62. 10 Each stage of the circuit 50 includes an N channel field effect transistor device 63, 64, or 65 connected to the gate terminal of the device 51, 52, or 53 of that stage.

In contrast to the circuit 30 of FIG. 3, the two phase clock signals do not overlap and the capacitors 60, 61, 20 and 62 are not precharged by the devices 63, 64, and 65. Referring the FIG. 6, it may be seen that the phase 2 clock is illustrated as high initially. When this clock is high, enabling signals are applied to the gate terminals of the control devices 63 and 65; and to the gate of 25 switching device 52. These pulses turn the control devices 63 and 65 on. The high voltage from the source 2 is also applied at the drain of The device 52, and the high voltages at both the drain and gate of the device 52 cause it to turn on. When the device 52 goes on, its drain 30 and gate are initially at the same value. However, since the phase 1 clock is low, the control device 64 joining the drain and gate of the device 52 is off. Thus, after the device 52 has been on for any period, the high voltage at the drain transfers charge from the capacitor 56 to the capacitor 57, reducing the voltage level at the drain of the device 52. This causes the voltage at the gate of the device 52 to be higher than either the drain or the source; and the device 52 switches completely on without any threshold voltage drop, increasing the current 40 furnished to the next stage.

As the voltage at the drain and source of the device begin to equalize, the voltage at the gate of the control device is raised so that the control device is nearly on. 45 When the phase 2 clock pulse goes low, the device 64 turns on. The lowering of the voltage at the gate of the device 52 when the phase 2 pulse goes low causes the device 52 to begin to turn off. Simultaneously, the gate terminals of each of the control devices 63 and 65 are lowered turning off the devices 63 and 65 so that the drain and gate terminals of the devices 51 and 53 are isolated from each other. When the phase 1 clock pulse goes high, the device 64 switches completely on and equalizes the gate and drain of the device 52. At the same time, the gate terminals of the devices 51 and 53 55 are raised by the value  $V_{cc}$  while the drain of the device 53 is raised by the value  $V_{cc}$ .

The devices 51 and 53 function similarly to the device 52 in transferring charge to the capacitors 56 and 58. The gate and drain terminals of these devices are initially equal, but then the drain voltage drops as charge is transferred to the capacitors 56 and 58 of the next stages so that the devices are switched completely on and experience no threshold voltage drop.

Thus, when the phase 1 clock goes high, the device 65 51 turns on; and current provided by the source  $V_{cc}$  charges the capacitor 56. When the phase 1 pulse goes low the device 51 switches off. Then the phase 2 clock

pulse turns on the device 52; and the capacitor 56 provides stored charge and charge due to the phase 2 pulse to the capacitor 57. The device 52 switches off when the phase 2 pulse goes low. When the phase 1 pulse again goes high, the source  $V_{cc}$  again charges the capacitor 56. Simultaneously, the device 53 goes on and the capacitor 57 provides stored charge as well as the pulse from the phase 1 clock to charge a capacitor 58. When the phase 1 clock goes low, the device 53 turns off. When the phase 2 clock later goes high, the output device 54 turns on and furnishes a pumped voltage at  $V_{out}$  equal approximately to the number of stages plus one multiplied by the value of  $V_{cc}$  less the  $V_t$  drop of the output device 54.

Ultimately, the charging of the capacitor 58 and the positive swing of the phase 2 clock pulse raise the voltage level on the capacitor 58 sufficiently above the level  $V_{out}$  to cause the conduction of the switching device 54. This provides the desired output voltage while furnishing the high level of current necessary to erase and program flash EEPROM memory arrays.

Thus, as may be seen, the arrangement of FIG. 5 provides a reliable charge pump circuit capable of producing high levels of current efficiently with a substantial reduction in the circuitry and die space necessary in the prior art. The circuit of FIG. 5 also offers the advantage that it requires substantially less delay in various voltage regulation circuitry utilized with the circuit in its usual arrangement.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

What is claimed is:

1. An integrated circuit charge pump circuit comprising a plurality of stages, each stage including
  - a first N type field effect switching transistor device having gate, source and drain terminals, each switching transistor device of each stage being connected in series with switching transistor devices of other stages,
  - a second N type field effect control transistor device having gate, source and drain terminals, the drain and source terminals connecting the drain terminal and the gate terminal of the first switching transistor device, and
  - a storage capacitor joined to the source terminal of the first switching transistor device;
  - a voltage source providing voltage to be pumped and connected to the drain terminal of the first switching transistor device of the first stage;
  - a first clock source providing a first series of clock pulses;
  - circuitry connecting the first series of clock pulses to the gate terminals of the first switching transistor devices in odd stages of the charge pump and to the gate terminals of the second control transistor devices in even stages;
  - a second clock source providing a second series of clock pulses which do not overlap the first series of clock pulses; and
  - circuitry connecting the second series of clock pulses to the gate terminals of the first switching transistor devices which do not receive the first series of clock pulses and to the gate terminals of the second



control transistor devices which do not receive the first series of clock pulses such that the first switching transistor devices are switched on to charge the next stage of the charge pump.

2. An integrated circuit charge pump circuit as claimed in claim 1 further comprising an output stage comprising a first N type field effect switching transistor device having gate, source and drain terminals, the drain terminal being connected in series with a last stage of the circuit, and the gate terminal being connected to the drain terminal.

3. An integrated circuit charge pump circuit as claimed in claim 2 in which each of the switching transistor devices and each of the control transistor devices is an S type field effect transistor device.

4. An integrated circuit charge pump circuit comprising a plurality of stages, each stage including

a switching transistor device having gate, source, and drain terminals, the source and drain terminals of each stage being connected in series with the source and drain terminals of all other stages, means for connecting in series the switching transistor device, switching transistor devices in adjacent stages and

first storage means joined to the source terminal of the switching device;

second storage means joined to the gate terminal of the switching device;

means for providing a voltage to be pumped at the drain terminal of the first switching transistor device of a first stage of the charge pump circuit;

means for furnishing a first set of clock pulses;

means for furnishing a second set of clock pulses which do not overlap the first set of clock pulses;

means for applying pulses of the first series of clock pulses to the gate and drain terminals of the switching transistor devices in alternate stages of the charge pump circuit;

means for applying pulses of the second series of clock pulses to the gate and drain terminals of the switching transistor devices in stages of the charge pump circuit which switching transistor devices do not receive the first series of clock pulses at gate terminals;

means responsive to the first and second series of clock pulses for disabling the means for connecting the drain terminal and the gate terminal of the switching transistor device of each stage of the charge pump circuit during a period beginning with the turn on of the switching transistor of that stage and continuing until the storage means of that stage has charged to a voltage level equal to a voltage level at the drain of the switching transistor device of that stage, whereby the gate of the switching transistor of each stage is held at a voltage level during conduction sufficient to eliminate threshold voltage drop.

5. An integrated circuit charge pump circuit as claimed in claim 4 further comprising an output stage comprising a switching transistor device having gate, source and drain terminals, the output stage connected in series to a last stage of the plurality of stages, and gate terminal being connected to the drain terminal.

6. An integrated circuit charge pump circuit as claimed in claim 4 in which the means for connecting the the switching transistor device comprises a control transistor device having gate, source, and drain terminals, the source and drain terminals being connected in a path between the gate and drain terminals of the switching transistor device of that stage.

7. An integrated circuit charge pump circuit as claimed in claim 6 in which the means responsive to the first and second series of clock pulses for disabling the means for connecting the drain terminal and the gate terminal of the switching transistor device of each stage of the charge pump circuit during a period beginning with the turn on of the switching transistor of that stage and continuing until the storage means of that stage has charged to a voltage level equal to a voltage level at the drain of the switching transistor device of that stage, comprises:

means for furnishing the first set of clock pulses to the gate terminals of control transistor devices in stages in which the second set of clock pulses is applied to the gate of the switching transistor device, and

means for furnishing the second set of clock pulses to the gate terminals of control transistor devices in stages in which the first set of clock pulses is applied to the gate of the switching transistor device.

8. An integrated circuit charge pump circuit as claimed in claim 7 in which the first storage means joined to the source terminal of the switching device and the second storage means joined to the gate terminal of the switching device each comprises a capacitor, in which the means for furnishing the first set of clock pulses to the gate terminals of control transistor devices in stages in which the second set of clock pulses is applied to the gate of the switching transistor device, comprises means furnishing the first set of clock pulses to the capacitor and means joining the capacitor to the gate terminal of the control transistor device of that stage; and

in which the means for furnishing the second set of clock pulses to the gate terminals of control transistor devices in stages in which the first set of clock pulses is applied to the gate of the switching transistor device comprises means furnishing the second set of clock pulses to the capacitor and means joining the capacitor to the gate terminal of the control transistor device of that stage.

9. An integrated circuit charge pump circuit as claimed in claim 8 in which each of the switching transistor devices and each of the control transistor devices is an S type field effect transistor device.

\* \* \* \* \*

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

**PATENT NO.** : 5,422,586  
**DATED** : June 6, 1995  
**INVENTOR(S)** : Tedrow et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 2 at line 52 delete "tie" and insert --be--

In column 7 at line 28 delete "The" and insert --the--

In column 10 at line 5 insert --the-- following "and" and prior to "gate"

Signed and Sealed this  
Fifth Day of November, 1996

*Attest:*



**BRUCE LEHMAN**

*Attesting Officer*

*Commissioner of Patents and Trademarks*

# United States Patent [19]

Kojima et al.

[11] Patent Number: 4,839,787

[45] Date of Patent: Jun. 13, 1989

## [54] INTEGRATED HIGH VOLTAGE GENERATING SYSTEM

[75] Inventors: Makoto Kojima, Suita; Hirozumi Misaki, Takatsuki; Yasuyuki Okada, Takatsuki, all of Japan

[73] Assignee: Matsushita Electric Industrial Co., Ltd., Osaka, Japan

[21] Appl. No.: 197,448

[22] Filed: May 20, 1988

### [30] Foreign Application Priority Data

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[51] Int. Cl.<sup>4</sup> ..... H02J 11/00; H02M 3/18

[52] U.S. Cl. .... 363/60; 307/110

[58] Field of Search ..... 363/59, 60, 61; 320/1; 307/110

### [56] References Cited

#### U.S. PATENT DOCUMENTS

3,824,447	7/1974	Kuwabara	363/60
4,186,436	1/1980	Ishiwatari	363/60
4,636,930	1/1987	Bingham et al.	363/60
4,734,599	3/1988	Bohac, Jr.	307/110

#### FOREIGN PATENT DOCUMENTS

2058502A 8/1980 United Kingdom .

Primary Examiner—Peter S. Wong

Attorney, Agent, or Firm—Wenderoth, Lind & Ponack

### [57] ABSTRACT

This invention relates to an integrated high voltage generating system provided with a charge pump for raising the input power supply voltage sequentially while transferring the electric charges of the capacitors on a stage by stage basis, by serially connecting unit circuits composed of diode elements and capacitors, and supplying clock signals of mutually opposite phases to adjacent capacitors. Source and drain electrodes of a MOS transistor are connected between the first power supply output terminal and a second power supply output terminal, and the gate electrode of this MOS transistor is connected to the input end of any one of the unit circuits of the charge pump, wherein the voltage of the first power supply output terminal is stepped down depending on the voltage applied to the gate electrode of the MOS transistor, and is delivered to the second power supply output terminal. In this way, since the voltage is not stepped down using a dividing circuit, a potential between input power supply voltage and the first input power supply voltage can be obtained from the second power supply output terminal, without consuming unnecessary current and without causing the chip area to be increased.

9 Claims, 4 Drawing Sheets

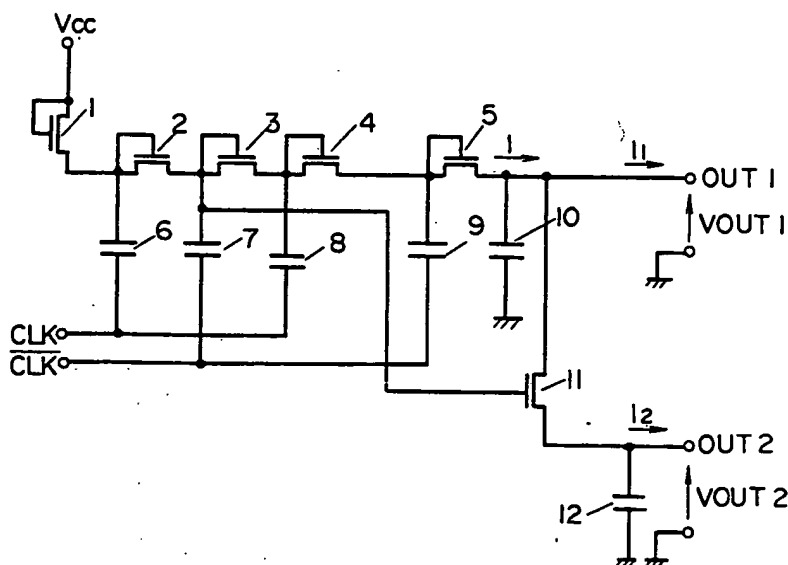


FIG. 1

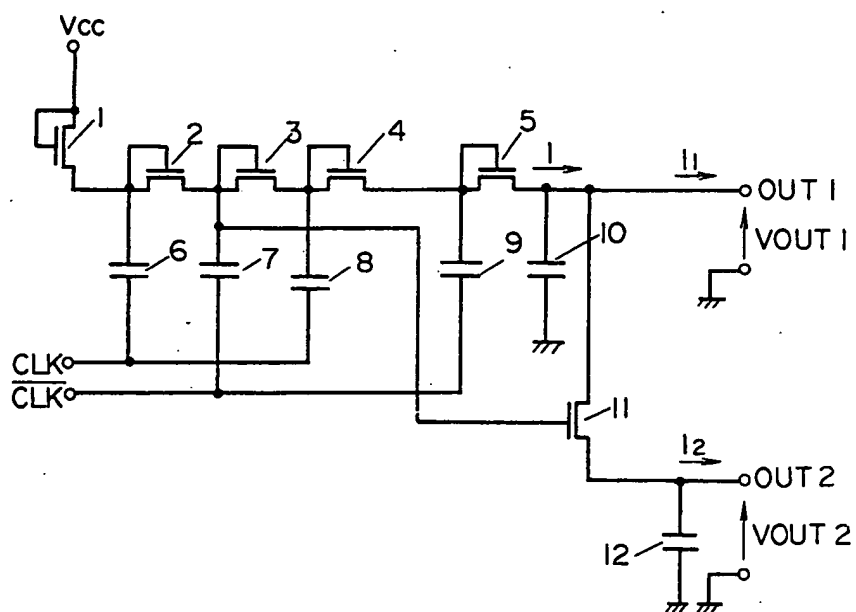


FIG. 2

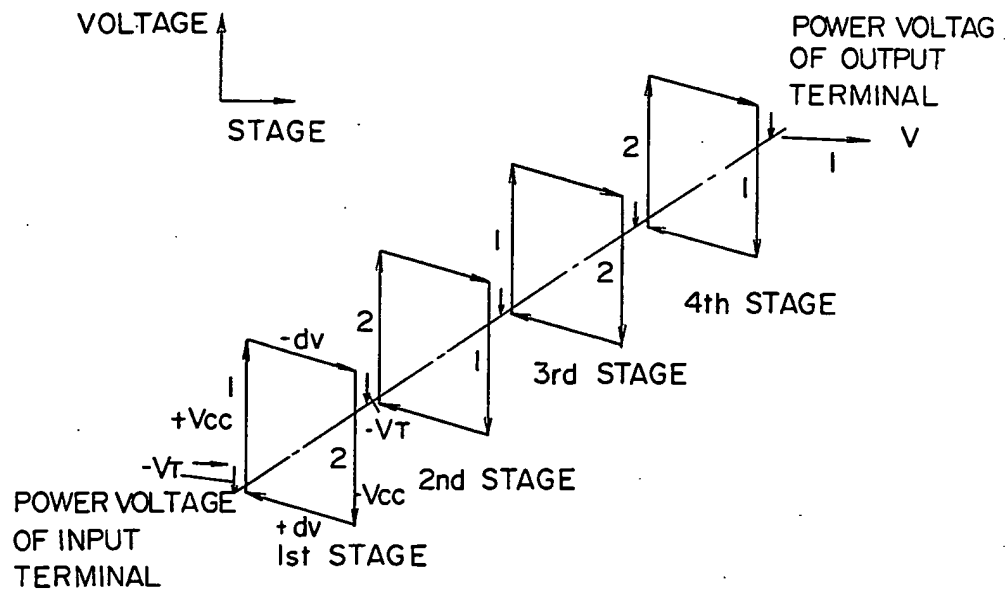


FIG. 3

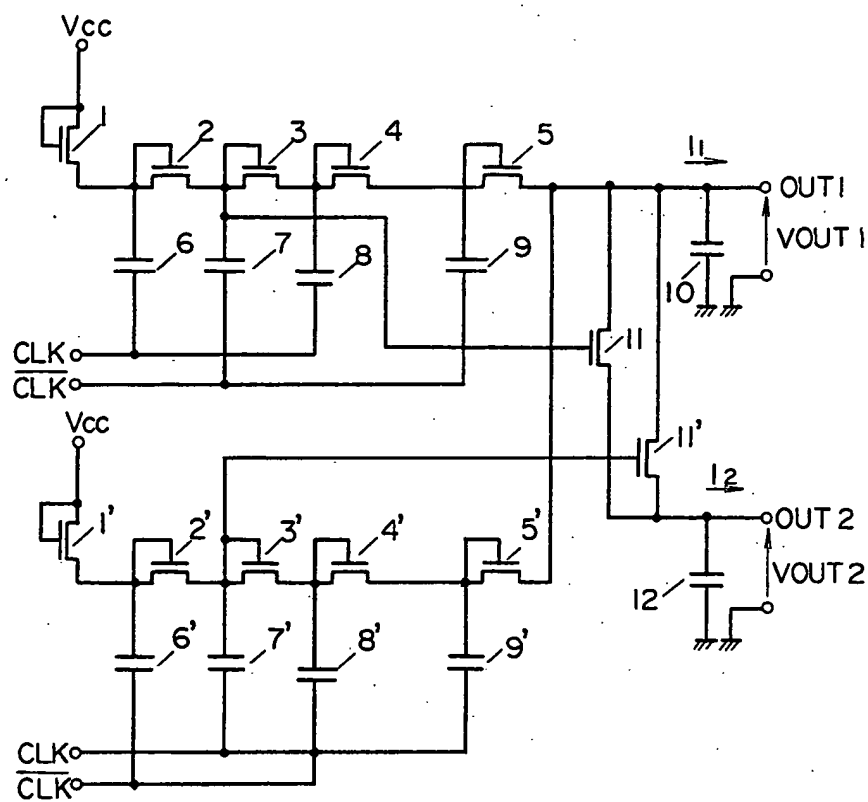


FIG. 4

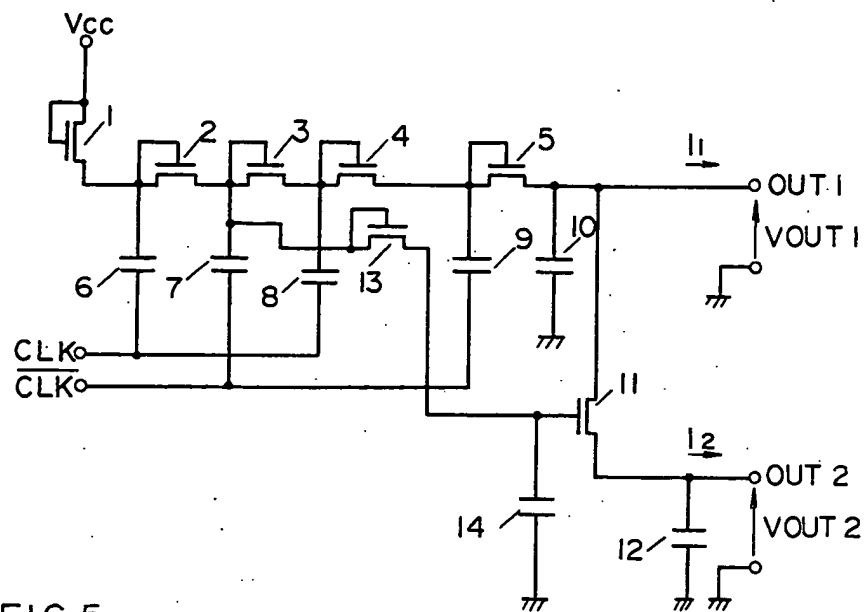
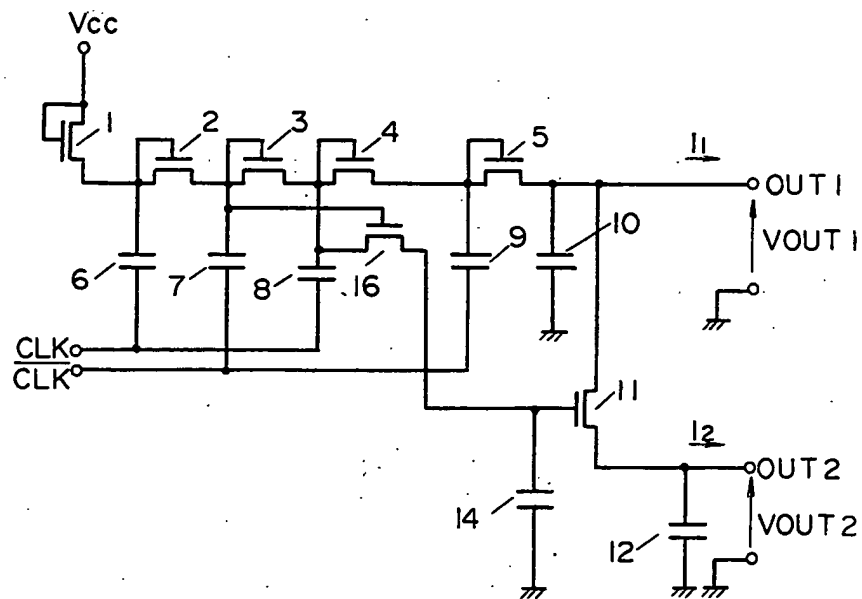


FIG.5





## INTEGRATED HIGH VOLTAGE GENERATING SYSTEM

### BACKGROUND OF THE INVENTION

This invention relates to an integrated high voltage generating system, and more particularly to an integrated high voltage generating system having a charge pump.

Various products have recently been developed which are portable and compact, and, as a result, they tend to have a lower supply voltage obtained from a single power source. For example, the power voltage of portable radio or portable tape recorder is about 1.5 to 3.0 V. When a high power voltage is required for a product, a high voltage generating system is incorporated in the product or a semiconductor device used in the product. When an integrated high voltage generating system is incorporated in a semiconductor device, the high voltage is generated by using a charge pump. Furthermore, if a high voltage power source having different potentials is needed, a high voltage is first generated by the charge pump, and this high voltage is divided and stepped down. The output is controlled using this divided voltage, thereby creating another high voltage source different from the original high voltage source. However, since the current supply capacity of the charge pump in the device is smaller in relation to its area, the electric power consumed in this dividing circuit cannot be ignored.

A conventional integrated high voltage generating system using a charge pump is described below.

FIG. 7 shows a conventional example of an integrated high voltage generating system using a charge pump for delivering two different power voltages. It comprises a charge pump having four unit circuits connected in series composed of diode-connected N-channel MOS transistors 1 to 5 and capacitors 6 to 9, a dividing circuit composed of two MOS transistors 17, 18, and a step-down control part composed of a MOS transistor 11 gated by the divided voltage of the dividing circuit.

The operation of the conventional integrated high voltage generating system is explained by referring to FIG. 7.

The electric charge coming in through the MOS transistor 1 from power source  $V_{cc}$  connected to the power source input terminal is sequentially transferred among four stages of unit circuit controlled by clock signals CLK,  $\overline{\text{CLK}}$  of normal and reverse phases with an amplitude of  $V_{cc}$ , and is sequentially boosted in this process. The boosted power supply voltage is delivered to a first power supply output terminal OUT 1. Part of this power supply voltage is delivered to a second power supply output terminal OUT 2 as another power supply voltage, by way of a step-down MOS transistor 11 which is gated by the divided output of the dividing circuit composed of two MOS transistors 17, 18. However, when a dividing circuit is used within the integrated high voltage generating system, the stability and response of this circuit and the current consumption are in conflict with each other, and accordingly the current consumption cannot be significantly decreased. The reason is as follows. Usually, at the first power supply output terminal OUT 1, a current flows of about several microamperes. On the other hand, when the MOS transistors 17, 18 are fabricated according to the design rule of about 3 microns, the gate width (W) and gate length (L) of the gate electrode are usually about 60 microns

and 3.0 microns respectively and their ratio W/L is about 20. At this time, the current IL flowing in the MOS transistors 17, 18 is about 5 mA. That is, when such MOS transistors 17, 18 are used, the majority of the current of several milliamperes delivered from the charge pump is consumed in the dividing circuit, and the function as the integrated high voltage generating system is sacrificed. Hence, as one of the methods of decreasing the current consumption in the dividing circuit to, for example about 5  $\mu\text{A}$ , it may be considered to design the gate width (W) at about 3 microns and the gate length (L) about 1500 microns, that is, the W/L of about 0.002. In turn, however, when the gate of MOS transistors 17, 18 is fabricated in such a size, since the gate width (W) itself is only about 3 microns, if its dimension varies about  $\pm 0.3$  micron, the effect of fluctuation is significant, and the stability of the device is impaired. Or when the gate is reduced to such a size, the stray capacitance of the gate increases. As a result, the response of the circuit is worsened. Thus, in the conventional integrated high voltage generating system using a dividing circuit, it was extremely difficult to lower the current consumption without spoiling the stability and response of the circuit.

Additionally, as another method of decreasing the current consumption, it may be considered to raise the dividing resistance. For example, when dividing 20 V into 15 V, in a 3-micron process, by using a MOS transistor of about 3  $\text{mm}^2$ , the current consumption becomes about 100  $\mu\text{A}$ . To reduce this current consumption, additional MOS transistors as the dividing resistances should be inserted between the power supply terminals of the dividing circuit (more than a dozen in the above example). Thus, the value of the current flowing in the dividing circuit may be reduced to several microamperes, and the current consumption can be decreased. This method however, becomes sensitive to fluctuations of the threshold voltages of the MOS transistors. Accordingly the circuit stability is poor.

On the other hand, the charge pump power supply is extremely small in the supply electric power per unit area, as compared with the power supplied by merely dividing the external power source. Therefore, if the capacity of the charge pump is increased in order to compensate for the slight power consumption in the dividing circuit, the area occupied by the charge pump within the semiconductor device becomes extremely large, and the chip size itself becomes larger.

It is hence a first object of this invention to present an integrated high voltage generating system capable of obtaining a potential between the input power supply voltage and the output power supply voltage without consuming unnecessary current.

It is a second object of this invention to present an integrated high voltage generating system capable of obtaining a potential between the input power supply potential and the output power supply potential without causing the chip area to be increased.

This invention may be briefly summarized as an integrated high voltage generating system including a charge pump having a plurality of unit circuits composed of diodes or diode-connected MOS transistors and capacitors of which one end is connected to the input side of the diodes or the MOS transistors and the other end to the clock signal source, connected in series so that the diode polarities may be in a same direction and clock phases applied to adjacent capacitors may be



mutually reverse, wherein an intermediate potential is taken out from the intermediate node between the power supply input terminal of the charge pump and the first power supply output terminal, and this intermediate potential is applied to the gate of the MOS transistor connected between the first power supply output terminal and the second power supply output terminal.

In this constitution, without consuming the unnecessary current as experienced in the dividing circuit, and without causing the chip area to be increased, a potential between the input power supply potential and the first power supply output potential may be obtained from the second power supply output terminal.

Other features and objects of the present invention will be apparent from the following description taken in connection with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of one embodiment of an integrated high voltage generating system of this invention;

FIG. 2 is a conceptual diagram modeling the voltage changes at each stage of the charge pump in FIG. 1;

FIG. 3 is a circuit diagram of a second embodiment of this invention;

FIG. 4 is a circuit diagram of third embodiment of this invention;

FIG. 5 is a circuit diagram of a fourth embodiment of this invention;

FIG. 6 is a circuit diagram of a fifth embodiment of this invention; and

FIG. 7 is a circuit diagram of a conventional integrated high voltage generating system.

### DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings, this invention is described relating to some of the embodiments in detail below.

FIG. 1 is a circuit diagram showing one of the embodiments of this invention. In this diagram, the charge pump constructed by the series connection of four stages of a unit circuit composed of diode-connected N-channel MOS transistor 1 to 5 and capacitors 6 to 9 is same as in the prior art. However, in this charge pump an intermediate potential is taken out from the intermediate node (the second stage in the case of the embodiment in FIG. 1) between the power supply input terminal and power supply output terminal. This intermediate potential gates MOS transistor 11 which couples a first power supply output terminal OUT 1 and a second power supply output terminal OUT 2. The first power supply voltage  $V_{OUT1}$  is supplied into a voltage detector circuit (not shown), while the second power supply voltage  $V_{OUT2}$  is supplied into a load (not shown). Capacitors 10, 12 are smoothing capacitors to lessen the reple of the first and second power supply output voltage  $V_{OUT1}$ ,  $V_{OUT2}$ . At each stage of the charge pump, clock signals CLK,  $\overline{\text{CLK}}$  of mutually opposite phases are applied to adjacent pumps, and their amplitude is  $V_{cc}$ , equal to that of the power supply voltage.

In this constitution, the electric charge running in through the MOS transistor 1 by way of the power supply  $V_{cc}$  connected to the power supply input terminal is sequentially transferred among four stages of the charge pump being controlled by the clock signals CLK,  $\overline{\text{CLK}}$  of normal and reverse phases having an amplitude of  $V_{cc}$ .

The conceptual drawing of the voltage waveform of each node of the charge pump at this time is shown in FIG. 2, in which the output of the first power supply output terminal OUT 1 is  $V_{OUT}$ , the sum of the currents flowing out is  $I$ , and the threshold voltage of the MOS transistors is  $V_T$ .

The first stage of the charge pump is explained as follows. For the sake of simplicity, the clock signal is suppose to have no transient time and phases of the clock signals CLK and  $\overline{\text{CLK}}$  are accurately reverse and the capacity of the capacitors 6 to 8 for the charge pump is supposed to be sufficiently larger than the stray capacitance. When the clock signal CLK connected to the capacitor 6 is LOW, the potential of this capacitor 6 is  $V_{cc} - V_T$ . At phase 1, the clock signal CLK rises, and the capacitor potential at the first stage instantly goes up to  $V_{cc} - V_T + V_{cc}$  to reach the peak voltage. At this moment, the clock signal  $\overline{\text{CLK}}$  for the capacitor of the next stage (second stage) falls, so that the electric charge stored in the capacitor 6 of the first stage is transferred to the capacitor 7 of the next stage via the MOS transistor 2. As a result, the potential of the capacitor 6 changes by  $-dV$ . At phase 2, since the clock signal CLK of the capacitor 6 falls, the potential of the capacitor 6 changes by  $-V_{cc}$ . Accordingly, the potential is decreased to the bottom voltage in a moment and then receiving electric charges from the preceding stage, the potential changes by  $+dV$ , and the node potential becomes  $V_{cc} - V_T$ . Here, assuming the frequency of the clock signals CLK and  $\overline{\text{CLK}}$  to be  $f$  [Hz] and the capacitance of the capacitor in the charge pump to be  $C$  [F], in the stationary state, the electric charge  $C \cdot dV$  transferred once from the capacitor 6 to 7 is equal to the sum of the current  $I/f$  flowing out per one clock time. Hence,  $dV = I/fC$ . Such a cycle occurs in each charge pump.

This operation may be also explained as follows. In the actual charge pump, the ON resistance of the transistors 2 to 5 are inserted in series to the input side of the diode-connected MOS transistors 2 to 5. Accordingly, each stage of the charge pump possesses some time constant due to capacitors 6 to 9 and the ON resistances. Therefore, when clock signals CLK,  $\overline{\text{CLK}}$  are applied to each stage, the potential of each intermediate node momentarily reaches the peak voltage (or the bottom voltage) when the clock signal rises (or falls), and then changes to a stationary voltage of a high level (or low level) according to the time constant. If rise and fall of clock signals CLK,  $\overline{\text{CLK}}$  are sufficiently steep, the peak voltage at the  $n$ -th stage, the stationary voltage of a high level, the stationary voltage of a low level and the bottom voltage are respectively expressed in equations (1) to (4).

Peak voltage at the  $n$ -th stage:

$$VHP_n = n(V_{cc} - V_T) + V_{cc} - (n-1) \cdot I \cdot R_s \quad (1)$$

High level stationary voltage at the  $n$ -th stage:

$$VHN = n(V_{cc} - V_T) + V_{cc} - n \cdot I \cdot R_s \quad (2)$$

Low level stationary voltage at the  $n$ -th stage:

$$VL_n = n(V_{cc} - V_T) - (n-1) \cdot I \cdot R_s \quad (3)$$

Bottom voltage at the  $n$ -th stage:

$$VLP_n = n(V_{cc} - V_T) - n \cdot I \cdot R_s \quad (4)$$

where  $R_s$  is an equivalent resistance per stage,  $R_s = 1/fC$ . Incidentally, equations (1) to (4) may be also expressed as in equations (5) to (8) respectively, in terms of the first power supply output voltage  $V_{OUT1}$  and the power supply voltage  $V_{cc}$ . In these equations,  $N$  denotes the total number of stages of the unit circuit in the charge pump.

$$V_{Hn} = n \cdot V_{OUT1} / N + (N-n)(V_{cc} - V_T) / N + V_T \quad (5)$$

$$V_{HPn} = V_{Hn} + I \cdot R_s \quad (6)$$

$$V_{Ln} = (n-1) \cdot V_{OUT1} / N + (N-n+1)(V_{cc} - V_T) / N \quad (7)$$

$$V_{LPn} = V_{Ln} - I \cdot R_s \quad (8)$$

From equation (7) it is known that the low level stationary potential of the potential of the intermediate node obtained from the  $n$ -th stage is equal to the potential of interior division between the voltage  $V_{OUT1}$  of the first power supply output terminal OUT 1 and the value lower by  $V_T$  than the voltage  $V_{cc}$  of the power supply input terminal into  $N-n+1$ ;  $n-1$ , that is, a divided voltage.

In the embodiment shown in FIG. 1, an intermediate potential is obtained from the intermediate node at the second stage, which corresponds to the case where  $n=2$ . In this circuit, from the second power supply output terminal OUT 2, a voltage lower than the maximum voltage applied to the gate of the MOS transistor 11 by  $V_T$  (threshold voltage of the MOS transistor 11) is taken out as the second power supply output voltage  $V_{OUT2}$ . That is, the second power supply voltage  $V_{OUT2}$  is

$$V_{OUT2} = n \cdot V_{OUT1} / N + (N-n)(V_{cc} - V_T) / N + I \cdot R_s \quad (9)$$

As clearly understood from this embodiment, by selecting the intermediate node (that is, in this case, setting  $n$  to any one of 1 to 4), the value of the second power supply voltage  $V_{OUT2}$  can be changed. Furthermore, in this circuit, since the dividing circuit as used in the conventional example shown in FIG. 7 is not used, a potential between the input power supply voltage and the second power supply output voltage  $V_{OUT2}$  may be obtained without consuming any unnecessary current.

FIG. 3 shows a second embodiment of this invention, combining two pieces of the embodiments shown in FIG. 1, and the parts indicated by reference numbers 1' to 11' are identical in function with 1 to 11 in FIG. 1, respectively. At the power supply input terminal of each charge pump, power supply  $V_{cc}$  is connected, and the power supply output terminals are commonly connected. Furthermore, clock signals CLK,  $\overline{CLK}$  are applied to each stage of two charge pumps so that the phase may be reverse to each other. Accordingly, the output voltages are same as in the first embodiment in FIG. 1, but the phase of operation of each charge pump is reverse to each other, so that the operation is effected in such a manner as to reduce the ripple of the first and second power supply output voltage  $V_{OUT1}$ ,  $V_{OUT2}$  of the first and second power supply output terminals OUT 1, OUT 2. That is, in the case using one line of a charge pump as in FIG. 1, pulsating currents similar to when a half-wave rectifying voltage is smoothed are caused, and the ripple content increases. However, when two lines of charge pump are driven alternately in reverse phases as shown in FIG. 3, the pulsating cur-

rents become as if full-wave rectifying voltage were being smoothed, so that the ripple content is decreased correspondingly.

FIG. 4 shows a third embodiment of this invention, in which a diode-connected MOS transistor 13 and a smoothing capacitor 14 are inserted between the intermediate node and the step-down MOS transistor 11 in FIG. 1. By constructing the circuit in this way, the gate voltage of the step-down MOS transistor 11 is stabilized, and the second power supply output voltage  $V_{OUT2}$  is also stabilized. The reason for this is as follows. As stated above, from the second power supply output terminal OUT 2, voltage lower than the maximum voltage applied to the gate of the MOS transistor 11 by  $V_T$  (the threshold voltage of the MOS transistor 11) is taken out as the second power supply output voltage  $V_{OUT2}$ . Since the voltage applied to the gate of the MOS transistor 11 is a voltage from the intermediate node, it fluctuates periodically in synchronism with the clock signals, CLK,  $\overline{CLK}$ . Therefore, for instance, if the gate voltage fluctuates between 11 V and 16 V and the threshold voltage  $V_T$  of the MOS transistor 11 is 1 V, the second power supply output voltage  $V_{OUT2}$  has a possibility of varying between 10 V and 15 V. Accordingly, by connecting the diode-connected MOS transistor 13 and the smoothing capacitor 14 between the intermediate node and the MOS transistor 11, the voltage applied to the gate of the step-down MOS transistor 11 can be flattened by the rectifying and smoothing action of the MOS transistor 13 and smoothing capacitor 14. As a result, the second power supply output voltage  $V_{OUT2}$  is lower than the flattened gate voltage by the portion of threshold voltage  $V_T$ , and an extremely stabilized voltage is obtained. In this circuit, the second power supply output voltage  $V_{OUT2}$  is expressed as follows:

$$V_{OUT2} = n \cdot V_{OUT1} / N + (N+n)(V_{cc} - V_T) / N + I \cdot R_s - V_T \quad (10)$$

Incidentally, a similar effect will be obtained by using an ordinary diode instead of the diode-connected MOS transistor 13.

In the above embodiments, meanwhile, the gate potential of the step-down MOS transistor 11 is determined by the peak voltage of the intermediate node, or, in other words, the top value of the transient response at the moment of rise (or fall) of clock signals CLK,  $\overline{CLK}$ . This top value of transient response suffers extremely by fluctuations of the ON resistances of MOS transistors 2 to 5 and the phase deviations between the two clock signals CLK,  $\overline{CLK}$ . Therefore, it is not wise to determine the gate potential of the step-down MOS transistor using the top value.

Accordingly, FIG. 5 shows a fourth embodiment of this invention which makes design easier and more precise than the foregoing embodiments. In this embodiment, the intermediate potential is taken out from the intermediate node through a MOS transistor 16 which is gated by the node signal in the previous stage. In this case, in the newly added MOS transistor 16, the gate potential and the charge pump side potential of the source drain are driven in opposite phases, and since the gate side is connected to the node of the previous stage (i.e. to one-stage lower voltage point), the maximum value of the intermediate potential is a low level stationary value (not the top value) of the  $n$ -th stage. There-

fore, designing becomes easier and more precise. At this time, the second power supply voltage  $V_{OUT2}$  is

$$V_{OUT2} = (n-1) \cdot V_{OUT1} / N + (N-n+1)(V_{CC} - V_T) / N - V_T \quad (11)$$

As clear from equation (11), in this embodiment, the second power supply output voltage  $V_{OUT2}$  is determined only by two elements, that is, the first power supply voltage  $V_{OUT1}$  and  $V_{CC} - V_T$ . (In all foregoing embodiments, the element of current  $I$  was contained.)

FIG. 6 shows a fifth embodiment, in which the charge pump 19 contains the elements 1 to 10, 13, 14 or 16 shown in FIG. 1, 3, 4 and 5. A voltage detection circuit 20 is composed of a transistor 21 for detection of voltage, a load transistor 22 and an inverter 23. The output of the voltage detection circuit 20 controls the clock signal source 24.

The input power supply voltage  $V_{CC}$  is boosted by the charge pump 19, and when the voltage  $V_{OUT1}$  of the first power supply output terminal OUT 1 exceeds a predetermined value, the voltage detection transistor 21 is turned on, and the output of the inverter 23 becomes a high level signal. In consequence, the frequency of the clock signal source 24 decreases, and the first power supply output voltage  $V_{OUT1}$  is lowered. As a result, when the first power supply output voltage  $V_{OUT1}$  becomes lower than the predetermined voltage, the voltage detection transistor 21 is turned off, and the output of the inverter 23 becomes a low level. Hence, the frequency of the clock signal source 24 increases, and the first power supply output voltage  $V_{OUT1}$  rises. By repeating such an operation, the first power supply output voltage  $V_{OUT1}$  is maintained at a predetermined voltage. When the first power supply output voltage  $V_{OUT1}$  is maintained at a predetermined voltage, the second power supply output voltage  $V_{OUT2}$  is also maintained at a voltage lower by  $V_T$  (threshold voltage of the MOS transistor 11). Therefore, the second power supply current voltage applied to the load can be stabilized.

Particularly, as with the charge pump 19 is FIG. 6, when the charge pump shown in the embodiment in FIG. 5 is used, the second power supply output voltage  $V_{OUT2}$  is determined only by the two elements of the first supply output voltage  $V_{OUT1}$  and  $V_{CC} - V_T$ , and the element of current  $I$  is not contained, so that the stabilization of the second power supply output voltage  $V_{OUT2}$  becomes extremely easy.

In the foregoing embodiments, meanwhile, the unit circuits of the charge pump were composed of diode-connected MOS transistors, but the same effects will be obtained if composed of ordinary diodes.

Thus, by using the integrated high voltage generating system of this invention, since an intermediate potential between the output end potential and input end potential is taken out from the intermediate node of the charge pump, there is no extra current consumption due to the dividing circuit, and the layout area is not to increased due to the dividing circuit, so that excellent effects may be obtained.

We claim:

1. An integrated high voltage generating system comprising:

a charge pump composed of plural unit circuits, each of said plural unit circuits having a capacitor and a diode element, wherein one end of said capacitor is connected to an input end of said diode element in each of said plural unit circuits, and wherein each

of said plural unit circuits represents a stage of said charge pump, and wherein said plural unit circuits are uniformly arranged according to a polarity of each diode element, and wherein an output end of said diode element of each preceding stage is sequentially connected to the input end of said diode element of each succeeding stage, whereby, when clock signals of mutually opposite phases are respectively applied to the other end of each capacitor of adjacent said plural unit circuits, an electric charge stored in said capacitor of each preceding stage is sequentially transferred to said capacitor of each succeeding stage, thereby raising a voltage level on a stage by stage basis;

- a power supply input terminal connected to a first stage of said charge pump at said input end of said diode element of a first unit circuit;
  - a first power supply output terminal connected to a final stage of said charge pump at said output end of said diode element of a final unit circuit;
  - a second power supply output terminal; and
  - a first MOS transistor having source and drain electrodes connected between said first and second power supply output terminals, and having a gate electrode connected at the input end of any one of said plural unit circuits of said charge pump, wherein a voltage of said first power supply output terminal is stepped down according to a voltage applied to said gate electrode, and wherein said stepped down voltage is delivered to said second power supply output terminal.
2. An integrated high voltage generating system according to claim 1, further comprising:
- an additional diode element connected between the input end of any one of said plural unit circuits of said charge pump and said gate electrode of said first MOS transistor.
3. An integrated high voltage generating system according to claim 2, further comprising:
- a smoothing capacitor connected between said gate electrode of said first MOS transistor and a reference potential point.
4. An integrated high voltage generating system according to claim 1, further comprising:
- a second MOS transistor having drain and source electrodes connected between the input end of any one of said plural unit circuits of said charge pump and said gate electrode of said first MOS transistor, and having a gate electrode connected to the input terminal of a unit circuit that is preceeding said any one of said plural unit circuits.
5. An integrated high voltage generating system according to claim 4, further comprising:
- a smoothing capacitor connected between said gate electrode of said first MOS transistor and a reference potential point.
6. An integrated high voltage generating system according to claim 1 further comprising:
- a voltage detection circuit connected to said first power supply output terminal of said charge pump in order to detect if the voltage of said first power supply output terminal has exceeded a predetermined value; and
- means for maintaining the voltage of said first power supply output terminal of the charge pump at said predetermined value.

7. An integrated high voltage generating system according to claim 4, further comprising:

- a voltage detection circuit connected to said first power supply output terminal of said charge pump in order to detect if the voltage of said first power supply output terminal has exceeded a predetermined value; and

means for maintaining the voltage of said first power supply output terminal of the charge pump at said predetermined value.

8. Integrated high voltage generating system comprising:

first and second charge pumps individually composed of plural unit circuits, each of said plural unit circuits having a capacitor and a diode element, wherein one end of said capacitor is connected to an input end of said diode element in each of said plural unit circuits, and wherein each of said plural unit circuits represents a stage of each charge pump, and wherein said plural unit circuits are uniformly arranged according to a polarity of said diode elements, and wherein an output end of said diode element of each preceding stage is sequentially connected to the input end of said diode element of each succeeding stage, whereby, when clock signals having mutually opposite phases are respectively applied to the other end of each capacitor of adjacent said plural unit circuits, an electric charge stored in said capacitor of each preceding stage is sequentially transferred to said capacitor of each succeeding stage, thereby raising a voltage level on a stage by stage basis, and wherein said clock signals having mutually opposite phases are

respectively supplied to said first and second charge pumps;

- a power supply input terminal connected to a first stage of said first and second charge pumps at the input end of said diode element of a first unit circuit;

- a first power supply output terminal connected to a final stage of said first and second charge pumps at the output end of said diode element of a final unit circuit;

- a second power supply output terminal;

- a first MOS transistor having drain and source electrodes respectively connected between said first and second power supply output terminals, and having a gate electrode connected to the input end of any one of the unit circuits of said first charge pump; and

- a second MOS transistor having drain and source electrodes respectively connected between said first and second power supply output terminals, and having a gate electrode connected to the input end of any one of the unit circuits of said second charge pump.

9. An integrated high voltage generating system of claim 8, further comprising:

- a voltage detection circuit connected to said first power supply output terminal in order to detect if the voltage of said first power supply output terminal has exceeded a predetermined value; and
- means for maintaining the voltage of said first power supply output terminal at said predetermined value.

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[54] **INTEGRATED, HIGH SPEED, ZERO HOLD CURRENT AND DELAY COMPENSATED CHARGE PUMP**

[75] Inventors: Jerry R. Wahl, Lakeville; Richard E. Hester, Eden Prairie, both of Minn.

[73] Assignee: VTC Incorporated, Bloomington, Minn.

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[51] Int. Cl.<sup>4</sup> ..... H03K 3/01; H03K 17/60; H03K 5/22; H03F 3/45

[52] U.S. Cl. .... 307/296.2; 307/296.4; 307/296.6; 307/255; 307/355; 307/270; 330/257

[58] Field of Search ..... 307/296.2, 296.4, 296.6, 307/270, 317 A, 255, 355, 356, 254; 330/257

[56] References Cited

## U.S. PATENT DOCUMENTS

4,074,205	2/1978	Robe	330/257
4,259,599	3/1981	Takada	307/270
4,331,887	5/1982	Jadus et al.	307/270
4,363,978	11/1982	Heimbigner	307/473
4,403,158	9/1983	Slemmer	307/296.2
4,409,496	10/1983	Baba	307/296.2
4,410,858	10/1983	Kusakabe	307/355
4,464,632	8/1984	Yoshihisa et al.	330/257 X
4,570,244	2/1986	Sud et al.	365/230

4,577,121	3/1986	Sano et al.	307/355
4,633,106	12/1986	Backes et al.	307/578
4,668,918	5/1987	Adams	307/511
4,748,346	5/1988	Emori	307/270
4,760,286	7/1988	Pigott	307/355 X

Primary Examiner—Stanley D. Miller

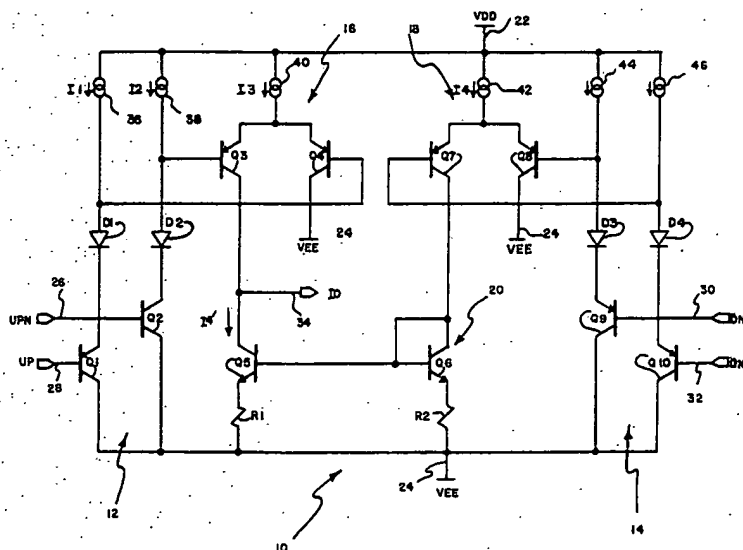
Assistant Examiner—Huy Kim Mai

Attorney, Agent, or Firm—Kinney & Lange

## [57] ABSTRACT

An integrated, high speed, zero hold current and delay compensated charge pump operable at one of two different selectable pumping currents. The charge pump includes first and second supply terminals, a first input terminal for receiving digital charge-up control signals, a second input terminal for receiving digital charge-down control signals, and an output terminal. A first transistorized differential amplifier controls a first current flow of a first polarity between the first supply terminal and the output terminal as a function of the charge-up control signals. A second differential amplifier controls a second current flow between the first and second supply terminals as a function of the charge-down control signals. A pump current mirror produces a mirrored second current flow of a second polarity between the output terminal and the second supply terminal as a function of the second current flow.

15 Claims, 3 Drawing Sheets



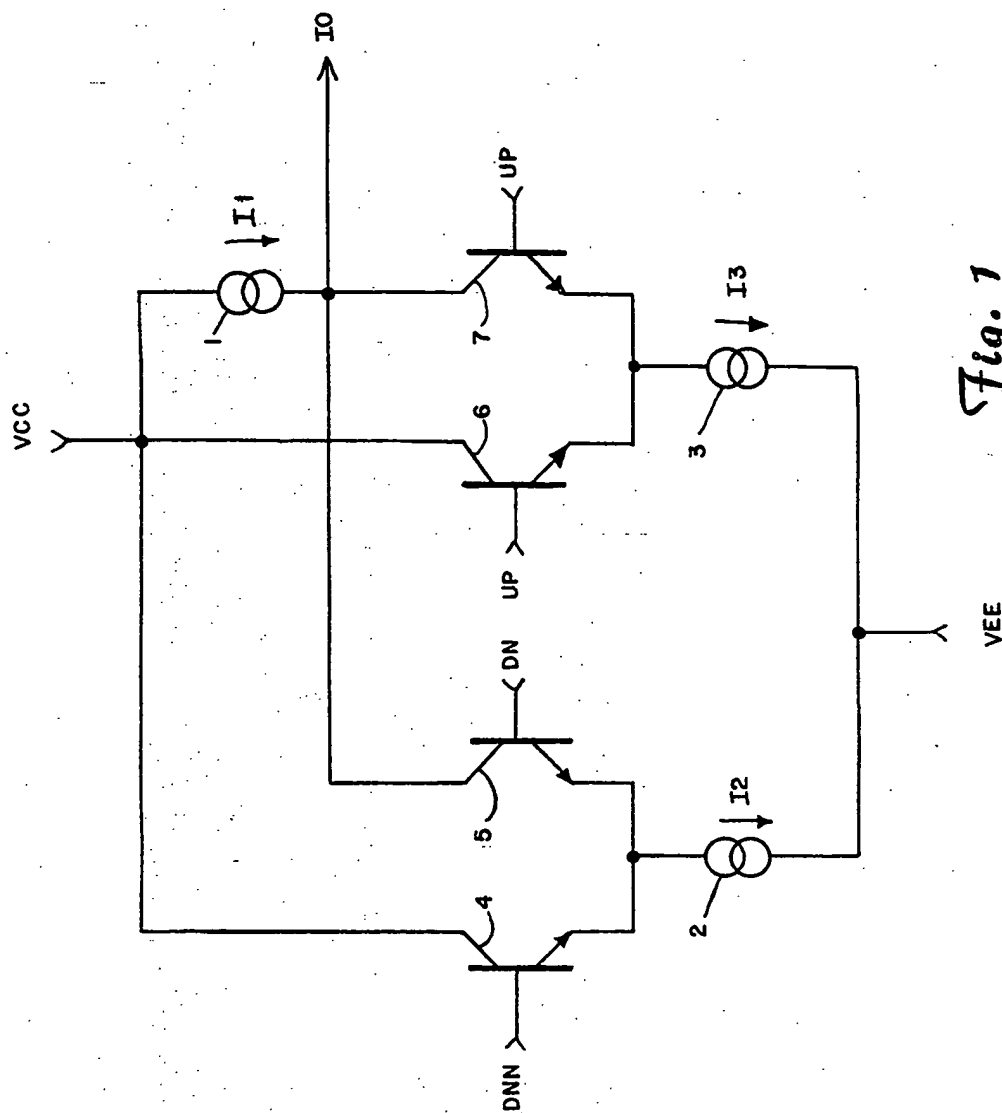


Fig. 1

PRIOR ART

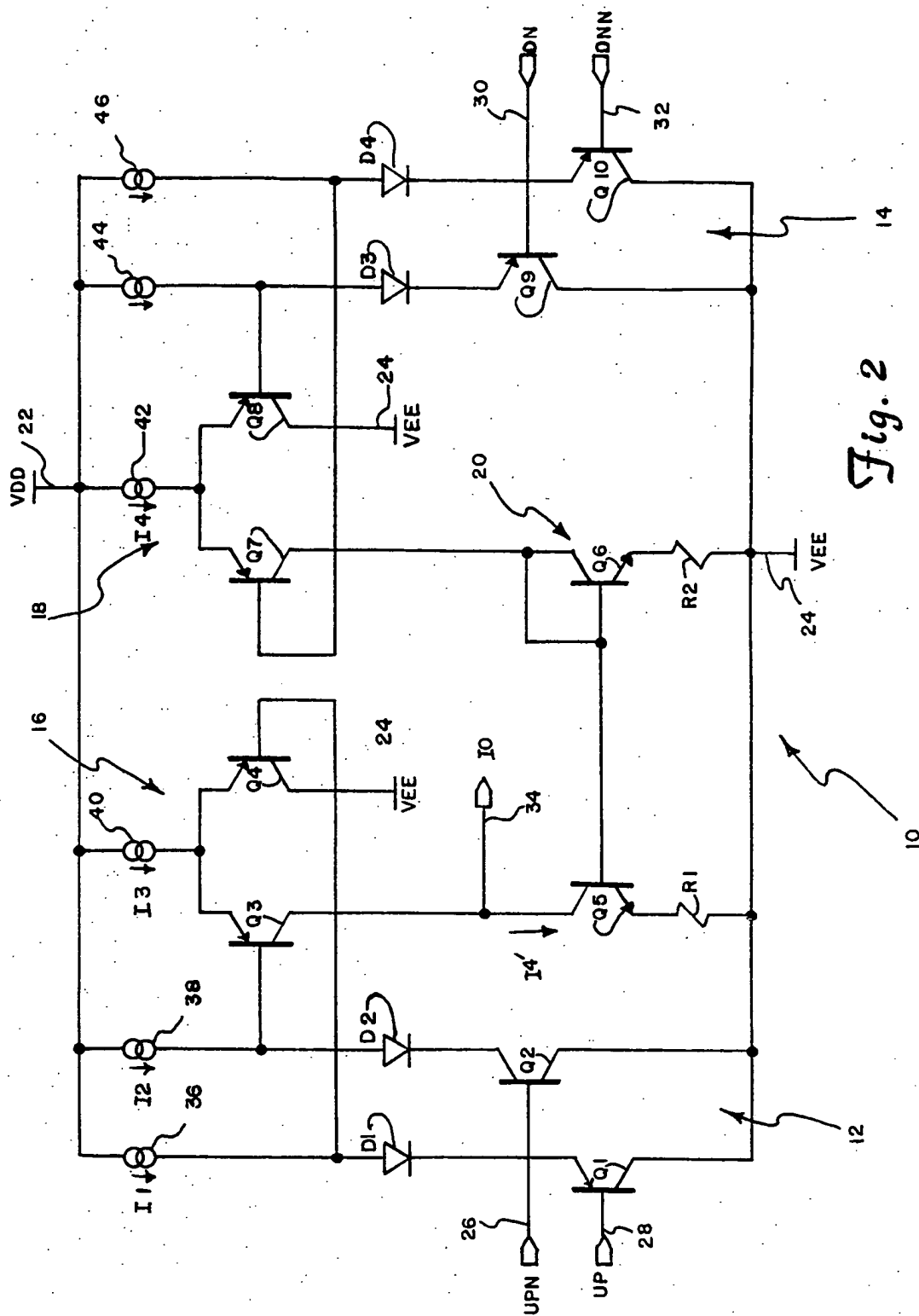


Fig. 2

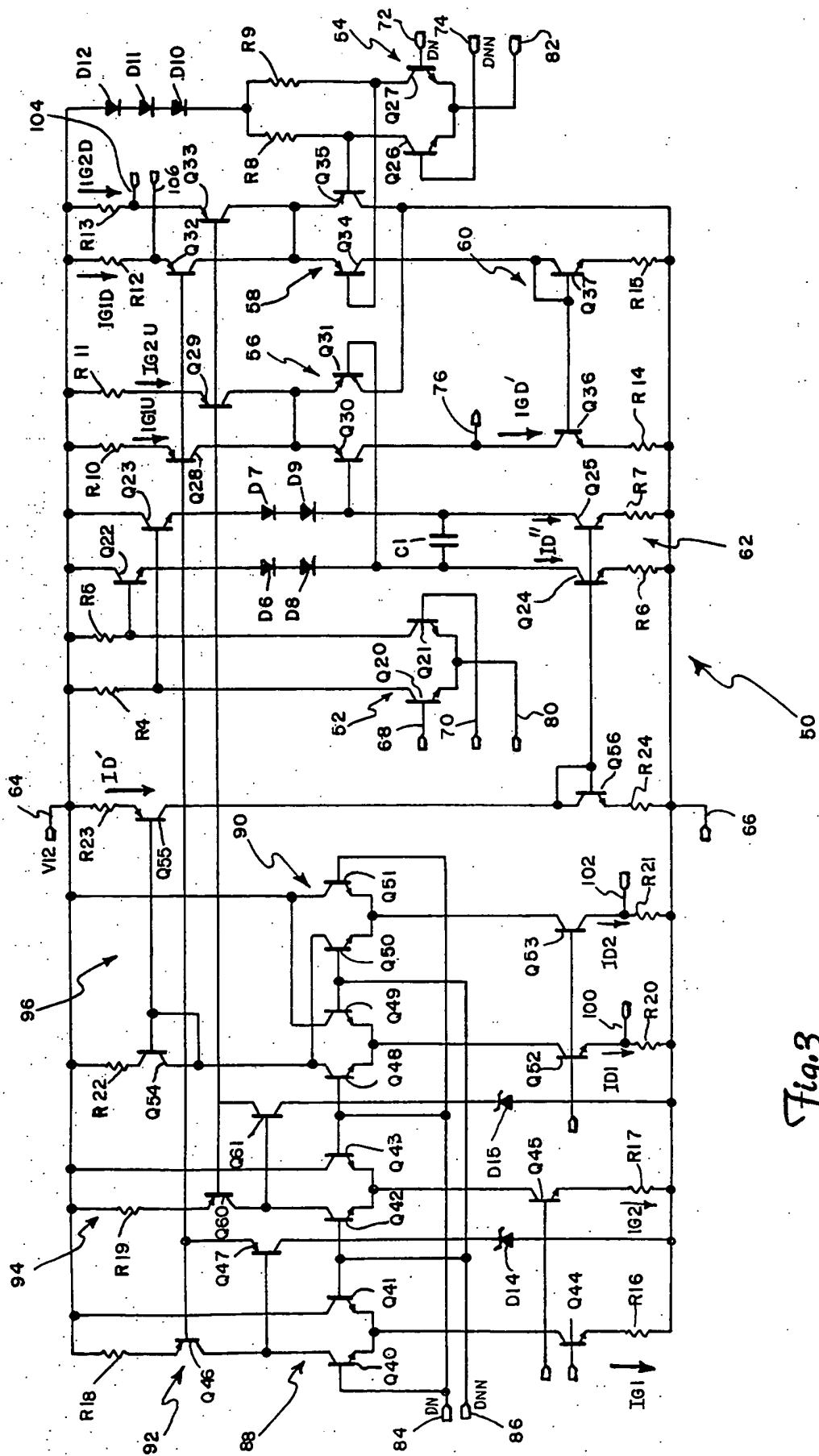


Fig. 3



# INTEGRATED, HIGH SPEED, ZERO HOLD CURRENT AND DELAY COMPENSATED CHARGE PUMP

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to charge pump circuits. In particular, the present invention is an integrated, zero hold current and delay compensated charge pump.

### 2. Description of the Prior Art

Charge pumps are commonly used circuits for controlling current flow. Digitally controlled charge pumps are often found in phase locked loops where they are used to control the sourcing of current into and sinking current from a filter coupled to the control input terminal of the voltage controlled oscillator. When operated in its charge-up mode, the charge pump will provide current to the filter thereby increasing the voltage on the filter and the frequency of the voltage controlled oscillator. When operated in its charge-down mode, the charge pump will draw current from the filter, thereby decreasing its voltage and the frequency of the voltage controlled oscillator. In its hold mode, the charge pump is essentially isolated from the filter. With current being neither drawn from nor supplied to the filter, its voltage and therefore the frequency of the voltage controlled oscillator are maintained at a steady state.

FIG. 1 is a schematic illustration of a known charge pump. The charge pump shown in FIG. 1 includes current sources 1, 2, and 3, and two emitter coupled pairs of transistors 4 and 5, and 6 and 7. Currents I1-I3 of the same magnitude are provided by current sources 1-3. This prior art charge pump is operated in a charge-up mode when logic HIGH, LOW charge-up signals are applied to the UP and UPN terminals and logic LOW, HIGH charge-down signals are applied to the DN and DNN terminals, respectively. Transistor 4 will be turned ON and conduct current I2, while transistor 6 will be turned ON and conduct current I3. Since transistors 5 and 7 are turned OFF, current I1 is supplied or sourced to output terminal I<sub>0</sub>. When the logic states of the signals are reversed (i.e. logic LOW, HIGH charge-up signals are applied to terminals UP and UPN, and logic HIGH, LOW charge-down signals are applied to terminals DN and DNN, respectively), transistors 4 and 6 are turned OFF while transistors 5 and 7 are turned ON. Both currents I2 and I3 will thereby be drawn from the node joining current source 1 to the collectors of transistors 5 and 7, while only current I1 is supplied to this node. Since the magnitude of currents I1, I2, and I3 are equal, an additional current will be sunk or drawn from output terminal I<sub>0</sub>.

The charge pump shown in FIG. 1 is operated in its hold mode when the UP and UPN terminals receive charge-up signals having logic LOW and HIGH states, while the charge-down signals have logic LOW and HIGH states applied to the DN and DNN terminals, respectively. Transistors 5 and 6 are turned OFF, while transistors 4 and 7 are switched ON by these signals. Current I1 is thereby conducted through transistor 7, while current I2 is conducted through transistor 4. In theory current will be neither sourced to nor sunk from output terminal I<sub>0</sub> since currents I1 and I2 are of equal magnitude. When the charge-up and charge-down control signals are synchronized in time, no cur-

rent will be output from the charge pump since the switching is very symmetrical, being performed differentially using NPN transistors 4-7.

In practice, however, the hold current is not zero when the charge pump is operated in its hold mode. A small amount of current will either flow to or be drawn from the output terminal of the charge pump. This can be a problem when the charge pump is used to control a phase lock loop, since it will lead to large amounts of steady-state error. Typically, the values of currents I1 and I2 are laser trimmed so that when the pump is in a hold state, very little current comes from the output terminal. The accuracy of this trimming operation can be to within plus or minus 0.1 percent. However, in many applications this will not result in a low enough hold current. Additionally, as supply voltages VCC and VEE vary, the hold current will get larger due to the mismatch of currents caused by the Early effect of the transistors. This effect is unavoidable with this type of pump.

Other current switching circuits are also known. The Jadus et al. U.S. Pat. No. 4,331,887 discloses current switch driving circuitry for supplying current to an output terminal. The output terminal is connected between a driving transistor and a sinking transistor. The driving and sinking transistors are coupled by logic signals applied to an ON control terminal, and an OFF control terminal. When both the ON and OFF control terminals are switched to a HIGH logic state, both driving and sinking transistors are switched OFF, preventing the output terminal from either sourcing or sinking current. The current will be sourced out of the output terminal when the ON control terminal is switched to a LOW logic state, and the OFF control terminal is switched to a HIGH logic state. When the OFF terminal is switched to a LOW logic state and the ON terminal is switched to a HIGH logic state, the sinking transistor is turned ON, and will draw current through the output terminal.

The Heimbigner U.S. Pat. No. 4,363,978 discloses a tristate driver circuit. The driver includes an output driver formed by two FETs having their source and drain terminals connected in series between a relatively positive potential V<sub>DD</sub> and a relatively negative potential V<sub>SS</sub>. An output terminal is connected between the two transistors. The output driver is controlled by two NOR gates formed by several FETs, as well as by other FETs. A buffer is driven to its float mode, or tristated, when the F terminal and F(bar) terminal receive logic 1 and logic 0 signals, respectively. The transistors of the output driver are then turned OFF.

The Takada U.S. Pat. No. 4,259,599 discloses a complementary transistor switching circuit. Either one or the other of two complementary transistors is turned OFF regardless of the state of the drive transistor. The other transistor will be turned ON.

The Backes et al. U.S. Pat. No. 4,633,106 discloses an MOS bootstrap push-pull stage which uses a diode capacitor charge pump.

The Sud et al. U.S. Pat. No. 4,570,244 discloses a transistor capacitor charge pump which is turned ON and OFF with clock pulses.

It is evident that there is a continuing need for improved charge pumps. A charge pump having a zero hold current as well as symmetrical switching characteristics is desired. A charge pump having these characteristics which can operate at several different pumping

currents would also be useful. The circuit must of course be relatively simple if it is to be commercially viable.

### SUMMARY OF THE INVENTION

A digitally controlled charge pump in accordance with the present invention includes first and second supply terminals, first input terminal means for receiving first digital charge control signals, second input terminal means for receiving second digital charge control signals, and an output terminal. First differential means coupled to the first input terminal means control a first current flow of a first polarity between the first supply terminal and the output terminal as a function of the first input signal. Second differential means coupled to the second input terminal means control a second current flow between the first and second supply terminals as a function of the second input signal. Pump current mirror means coupled to the second differential means and between the output terminal and the second supply terminal control a mirrored second current flow of a second polarity between the output terminal and the second supply terminal as a function of the second current flow.

In response to first and second charge control signals causing the charge pump to operate in a first (e.g. charge-up) mode, the first differential means permits a first current having a first polarity to flow between the first supply terminal and the output terminal. The second differential means causes the pump current mirror means to prohibit the flow of current between the output terminal and second supply terminal. In response to first and second digital charge control signals causing the charge pump to operate in a second (e.g. charge-down) mode, the first differential means prohibits the first current flow between the first supply terminal and the output terminal, while the second differential means causes the mirrored second current having the second polarity to flow between the output terminal and the second supply terminal. In response to first and second digital charge control signals causing the charge pump to operate in a third (e.g. hold) mode, the first differential means prohibits the first current flow between the first supply terminal and the output terminal, and the second differential means prohibits the mirrored second current flow between the output terminal and second supply terminal. The charge pump thereby has a zero hold current when operated in its hold mode.

The pump current mirror means is characterized by an inherent delay period. In preferred embodiments, the charge pump also includes delay circuit means coupled between the first input terminal means and the output terminal, for delaying response of the first current to the first charge control signals by a delay period equal to the delay period inherent in the pump current mirror means. Charge-up and charge-down pumping can thereby be symmetrically performed.

In still other embodiments, the charge pump includes gain control terminal means for receiving pumping gain control signals. Pumping gain control circuit means coupled between the pumping current gain control terminal means and a first current source means of the first differential means and a second current source means of the second differential means cause the first current source means to produce a first current flow having one of a plurality of different magnitudes, and cause the second current source means to produce a second current flow having one of a plurality of differ-

ent magnitudes, in response to the pumping current gain control signals. The charge pump can thereby be selectively operable at one of a plurality of different pumping currents. Controllable delay circuit means coupled between the first input terminal means and the output terminal, and coupled to the pumping current gain control terminal means delay response of the first current to the first charge control signals by selected delay periods equal to inherent delay periods of the pump current mirror means, in response to the gain control signals.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic illustration of a prior art digitally controlled charge pump.

FIG. 2 is a schematic illustration of a high speed, zero hold current charge pump in accordance with the present invention.

FIG. 3 is a schematic illustration of a high speed, zero hold current and delay compensated charge pump in accordance with the present invention, which can operate at one of two different pumping currents.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment to the present invention, integrated, high speed, zero hold current charge pump 10, is schematically illustrated in FIG. 2. Charge pump 10 includes first or charge-up input circuit 12, second or charge-down input circuit 14, first or charge-up differential amplifier 16, second or charge-down differential amplifier 18, and pump current mirror 20, all of which are interconnected between a first supply terminal 22 and a second supply terminal 24. Supply terminal 22 is connected to receive a relatively positive supply potential  $V_{DD}$ , while supply terminal 24 is connected to receive a relatively negative supply potential VEE. Charge-up input circuit 12 is connected to receive complementary digital charge-up control signals UP and UPN through charge-up input terminals 26 and 28. Charge-down input circuit 14 is connected to receive digital charge-down control signals DN and DNN over charge-down input terminals 30 and 32. An output terminal 34 is connected between charge-up differential amplifier 16 and current mirror 20.

Charge-up input circuit 12 is formed by PNP bipolar transistors Q1 and Q2, diodes D1 and D2, and current sources 36 and 38. The base of transistor Q1 is connected to input terminal 28, while the base of transistor Q2 is connected to input terminal 26. The collectors of transistors Q1 and Q2 are both coupled to second supply terminal 24. The emitter of transistor Q1 is connected to the cathode of diode D1, while the emitter of transistor Q2 is connected to the cathode of diode D2. Current sources 36 and 38 are connected between first supply terminal 22 and the anode of diodes D1 and D2, respectively. Current sources 36 and 38 provide currents I1 and I2, respectively. In one embodiment, currents I1 and I2 are both one milliamperes in magnitude.

Charge-up differential amplifier 16 is formed by PNP transistors Q3 and Q4, and current source 40. Current source 40 is connected between first supply terminal 22 and the emitters of transistors Q3 and Q4. The collector of transistor Q3 is connected to output terminal 34, while the collector of transistor Q4 is connected to second supply terminal 24. The bases of transistors Q3 and Q4 function as an input to amplifier 16, and are connected to receive a differential signal present between the anodes of diodes D2 and D1, respectively.

Current source 40 provides a two milliamper current in one embodiment.

Current mirror 20 is formed by NPN transistors Q5 and Q6, and resistors R1 and R2. Resistor R1 is connected between second supply terminal 24 and the emitter of transistor Q5. The collector of transistor Q5 is coupled to output terminal 34. The base of transistor Q5 is connected to the base and collector of transistor Q6. The emitter of transistor Q6 is connected to second supply terminal 24 through resistor R2.

Charge-down differential amplifier 18 is formed by PNP transistors Q7 and Q8, and current source 42. Current source 42 is connected between first supply terminal 22 and the emitters of transistors Q7 and Q8. In preferred embodiments, current source 42 produces a current I4 of two milliamperes. The collector of transistor Q7 is connected to the collector of transistor Q6 of current mirror 20. The collector of transistor Q8 is connected to the second supply terminal 24. The bases of transistors Q7 and Q8 function as an input to differential amplifier 18, and are connected to receive a differential signal from charge-down input circuit 14.

Charge-down input circuit 14 is formed by PNP bipolar transistors Q9 and Q10, diodes D3 and D4, and current sources 44 and 46. The collectors of transistors Q9 and Q10 are connected to second supply terminal 24. The bases of transistors Q9 and Q10 are connected to input terminals 30 and 32, respectively. Transistor Q9 has its emitter connected to the cathode of diode D3, while the emitter of transistor Q10 is connected to the cathode of diode D4. Current source 44 is connected between first supply terminal 22 and the anode of diode D3. Current source 46 is connected between first supply terminal 22 and the anode of diode D4. The anode of diode D3 is also connected to the base of transistor Q8, while the anode of diode D4 is connected to the base of transistor Q7.

To operate charge pump 10 in its charge-up mode, UP and UPN signals having logic HIGH and LO states are applied to input terminals 28 and 26, respectively. DN and DNN signals having logic LOW and HIGH states are simultaneously applied to input terminals 30 and 32, respectively. Input circuits 12 and 14 shift the level of the input signals and provide differential control signals to their respective charge-up differential amplifier 16 and charge-down differential amplifier 18. The potential applied to the base of transistor Q3 will therefore be at a relatively negative value compared to the potential applied to the base of transistor Q4, causing transistor Q3 to be switched ON, and transistor Q4 to be switched OFF. As a result, current I3 provided by current source 40 flows through transistor Q3.

During this period the differential signal provided by charge-down input circuit 14 is such that a relatively negative potential is applied to the base of transistor Q8, as compared to the potential applied to the base of transistor Q7. Transistor Q8 is thereby switched ON while transistor Q7 is switched OFF, causing current I4 from current source 42 to flow through transistor Q8. Since no current is flowing through transistor Q7, transistor Q5 of current mirror 20 will be switched to its OFF state, effectively isolating output terminal 34 from second supply terminal 24. Current I3 flowing through transistor Q3 thereby functions as a charge-up pumping current which is sourced to and flows out output terminal 34 (i.e. has a first polarity).

To operate charge pump 10 in its charge-down mode, logic states of the charge-up input signals and charge-

down input signals are reversed. UP and UPN signals having logic LOW and HIGH states are applied to terminals 28 and 26, respectively, while signals DN and DNN having logic HIGH and LOW states are applied to terminals 30 and 32, respectively. In response to these signals, charge-up input circuitry 12 provides a differential signal to charge-up differential amplifier 16 which forces the base of transistor Q3 to a relatively positive potential with respect to the potential applied to the base of transistor Q4. Transistor Q4 is thereby turned ON and shunts current I3 to second supply terminal 24, while transistor Q3 is turned OFF. Output terminal 34 is thereby electrically isolated from first supply terminal 22.

In response to the charge-down input signals, charge down input circuitry 14 provides a differential signal causing the base of transistor Q7 to be at a relatively negative potential compared to the potential at the base of transistor Q8. Transistor Q8 is thereby switched OFF, while transistor Q7 is switched ON. Current I4 provided by current source 42 thereby flows through transistor Q7, and transistor Q6 of current mirror 20. Current mirror 20 mirrors current I4, and produces a mirror current I4' through transistor Q5. This current is a charge-down pumping current which is sunk from output terminal 34 (i.e. has a second polarity) to second supply potential 24.

In the preferred embodiment described above in which currents I3 and I4 were two milliamperes, both the charge-up and charge-down pumping currents can be two milliamperes in magnitude. To operate charge pump 10 in its hold mode, input signals UP and UPN having logic LOW and HIGH states, and input signals DN and DNN having logic LOW and HIGH states, are applied to input terminals 28, 26, 30 and 32, respectively. The response of charge-up differential amplifier 16 and charge-down differential amplifier 18 to these input signals is identical to that described above. Transistor Q3 is switched OFF, isolating output terminal 34 from first supply terminal 22. Transistor Q7 is also switched OFF, thereby causing transistor Q5 to be turned OFF and isolating output terminal 34 from second supply terminal 24. Since transistors Q3 and Q5 are OFF, the hold current is inherently zero. The only current flowing from output terminal 34 will be the leakage current of transistor Q3, which is extremely small. The output impedance of transistors Q3 and Q5 in their OFF state is extremely high, so the effect of Early voltages is negligible.

Since current mirror 20 is used between charge-down differential amplifier 18 and output terminal 34, switching delay between charge-down input terminals 30 and 32 and output terminal 34 can be greater than that between charge-up input terminals 26 and 28 and the output terminal. This switching delay is due to the finite propagation delay of current mirror 20, which is fabricated of NPN transistors. If this delay is not compensated, charge pump 10 may generate steady-state error when used in a phase lock loop.

Charge pump 50, a second embodiment of the present invention, is schematically illustrated in FIG. 3. Charge pump 50 includes delay circuitry for compensating for the difference in delay between the charge-up and charge-down current paths created by the asymmetrical use of current mirrors. Furthermore, charge pump 50 is capable of operating at two different and selectable pumping currents.

Charge pump 50 includes charge-up input circuit 52, charge-down input circuit 54, charge-up differential amplifier 56, charge-down differential amplifier 58, pump current mirror 60 and selectable delay circuit 62, all of which are coupled between a first supply terminal 64 and a second supply terminal 66. Supply terminal 64 is connected to receive a first supply potential V12, while second supply terminal 66 is connected to receive a second supply potential VN1. Digital charge-up control signals U and UN are applied to charge-up input circuit 52 through terminals 68 and 70, respectively. Digital charge-down control signals DN and DNN are applied to charge-down input circuit 54 through terminals 72 and 74, respectively. Output terminal 76 is connected between current mirror 60 and charge-up differential amplifier 56.

Charge-up input circuit 52 includes NPN bipolar transistors Q20 and Q21 and resistors R4 and R5. The emitter of transistors Q20 and Q21 are coupled to receive a second bias potential BIAS2 from terminal 80. The base of transistor Q20 is connected to receive the U input signal from terminal 68, while the base of transistor Q21 is connected to receive the UN input signal from terminal 70. Resistor R4 couples the collector of transistor Q20 to supply terminal 64. Resistor R5 couples the collector of transistor Q21 to supply terminal 64.

Delay circuit 62 includes NPN transistors Q22, Q23, Q24, and Q25, resistors R6 and R7, capacitor C1 and diodes D6, D7, D8, and D9. Transistors Q24 and Q25 have their bases interconnected. The emitter of transistor Q24 is coupled to supply terminal 66 through resistor R6. The emitter of transistor Q25 is coupled to terminal 66 through resistor R7. The collector of transistor Q24 is connected to a first terminal of capacitor C1 and to a cathode of diode DS. The collector of transistor Q25 is connected to a second terminal of capacitor C1, and to a cathode of diode D9. The anode of diode D8 is coupled to the cathode of diode D6, while the anode of diode D9 is coupled to the cathode of diode D7. Transistor Q22 has its collector connected to supply terminal 64 and its emitter connected to the anode of diode D6. Transistor Q23 has its collector connected to supply terminal 64 and its emitter connected to the anode of diode D7. The base of transistor Q22 is coupled to charge-up input circuitry 52 at the collector of transistor Q21, while the base of transistor Q23 is coupled to the charge-up input circuit at the collector of transistor Q20.

Charge-down input circuit 54 includes NPN bipolar transistors Q26 and Q27, resistors R8 and R9, and diodes D10, D11, and D12. The emitters of transistors Q26 and Q27 are connected to receive a first bias potential BIAS1 from terminal S2. The base of transistor Q26 is connected to receive the DNN input signal from input terminal 74, while the base of transistor Q27 is connected to receive the DN signal from terminal 72. Diodes D10-D11 are connected in series between supply terminal 64 and a first terminal of resistors R8 and R9. A second terminal of resistor R8 is connected to a collector of transistor Q26, while a second terminal of resistor R9 is connected to a collector of transistor Q27.

Charge-up differential amplifier 56 is formed by PNP bipolar transistors Q28, Q29, Q30, and Q31 and resistors R10 and R11. The emitters of transistors Q30 and Q31 are connected together and to the collectors of transistors Q28 and Q29. The bases of transistors Q30 and Q31 are connected to the cathodes of diodes D9 and DS,

respectively, to receive a differential input signal. The collector of transistor Q30 is connected to output terminal 76, while the collector of transistor Q31 is connected to second supply terminal 66. The emitter of transistor Q28 is connected to first supply terminal 64 through resistor R10, while the emitter of transistor Q29 is connected to the first supply terminal through resistor R11.

Charge-down differential amplifier 58 includes PNP bipolar transistors Q32, Q33, Q34, and Q35 and resistors R12 and R13. The collector of transistor Q34 is coupled to current mirror 60, while the collector of transistor Q35 is coupled to second supply terminal 66. The bases of transistors Q34 and Q35 receive a differential signal from charge-down input circuit 54, the base of transistor Q34 being coupled to the collector of transistor Q27, and the base of transistor Q35 being coupled to the collector of transistor Q26. The emitters of transistors Q34 and Q35 are coupled together and to the collectors of transistors Q32 and Q33. First supply terminal 64 is coupled to the emitter of transistor Q32 through resistor R12, while the first supply terminal is coupled to the emitter of transistor Q33 through resistor R13.

Current mirror 60 is formed by NPN bipolar transistors Q36 and Q37 and resistors R14 and R15. The collector of transistor Q36 is connected to output terminal 76. Second supply terminal 66 is coupled to the emitter of transistor Q36 through resistor R14. Second supply terminal 66 is coupled to the emitter of transistor Q37 through resistor R15. The base and collector of transistor Q37 are connected to the collector of transistor Q34, and to the base of transistor Q36.

Charge pump 50 can operate at two different and independently selectable pumping currents. This operation is facilitated by the use of two different current sources in each of charge-up differential amplifier 56 and charge-down differential amplifier 58. Transistors Q28 and Q32 function as current sources in conjunction with current mirror circuitry yet to be described and provide a first gain charge-up current IG1U and a first gain charge-down current IG1D, respectively, when selected. Transistors Q29 and Q33 function as current sources in conjunction with still other current mirror circuitry yet to be described and provide a second gain charge-up current IG2U and a second gain charge-down current IG2D to charge-up differential amplifier 56 and charge-down differential amplifier 58, respectively.

The delay inherent within current mirror 60 is functionally related to the magnitude of the selected charge-down current IG1D or IG2D provided through charge-down differential amplifier 58. The delay of delay circuitry 62 which is used to compensate for the delay of current mirror 60 must therefore be selected as a function of the selected pumping current. Accordingly, transistors Q24 and Q25 function as current sources in conjunction with current mirror circuitry yet to be described and produce a delay current ID" having one of two magnitudes which cause the delay imposed by delay stage 62 to correspond to the delay of current mirror 60 with the selected pumping current.

To perform the pumping current gain and associated delay selection, charge pump 50 includes a pumping gain control current multiplexer 88 and a delay control current multiplexer 90. Multiplexer 88 is formed by a first emitter coupled pair of NPN bipolar transistors Q40 and Q41, and a second emitter coupled pair of NPN bipolar transistors Q42 and Q43. Multiplexer 88 also includes NPN bipolar transistors Q44 and Q45 and

resistors R16-R17. The bases of transistors Q40 and Q43 are connected to receive gain control signals GN on terminal 84. The bases of transistors Q41 and Q42 are connected to receive gain control signals GNN on terminal 86. The emitters of transistors Q40 and Q41 are coupled to the collector of transistor Q44. The collector of transistor Q41 is coupled to supply terminal 64. The emitter of transistor Q44 is connected to second supply terminal 66 through resistor R16. The base of transistor Q44 is connected to receive a bias potential VAHG. Transistor Q44 and resistor R16 function as a current source, and produce a first or high gain control current IG1. The emitters of transistors Q42 and Q43 are coupled to the collector of transistor Q45. The collector of transistor Q43 is connected to supply terminal 64. The emitter of transistor Q45 is connected to second supply terminal 66 through resistor R17. The base of transistor Q45 is connected to receive a second bias voltage VALG. Transistor Q45 and resistor R17 function as a current source and generate a second or low gain control current IG2.

Transistor Q40 of multiplexer 88 is coupled to transistors Q28 and Q32 of charge-up differential amplifier 56 and charge-down differential amplifier 58, respectively, by means of first gain current mirror 92. Current mirror 92 is formed by PNP bipolar transistors Q46 and Q47, zener diode D14 and resistor R18. The collector of transistor Q46 is coupled to the collector of transistor Q40 and to the base of transistor Q47. The emitter of transistor Q46 is connected to first supply terminal 64 through resistor R18. Transistor Q47 has its collector connected to the cathode of diode D14, while the anode of the diode is connected to second supply terminal 66. The base of transistor Q46 is connected to the emitter of transistor Q47 and to the bases of transistors Q28 and Q32.

Transistor Q42 of the second emitter coupled pair of multiplexer 88 is coupled to transistors Q29 and Q33 of charge-up differential amplifier 56 and charge-down differential amplifier 58, respectively, by means of second gain current mirror 94. Current mirror 94 includes PNP transistors Q60 and Q61, zener diode D15 and resistor R19. The collector of transistor Q60 is coupled to the collector of transistor Q42 and to the base of transistor Q61. The emitter of transistor Q60 is connected to first supply terminal 64 through resistor R19. The collector of transistor Q61 is connected to the cathode of diode D15 while the anode of the diode is connected to second supply terminal 66. The base of transistor Q60 and emitter of transistor Q61 are connected to the bases of transistors Q29 and Q33.

Delay control current multiplexer 90 includes a first emitter coupled pair of transistors Q48 and Q49, a second emitter coupled pair of transistors Q50 and Q51, and a pair of current sources formed by transistors Q52, Q53, and resistors R20 and R21. The emitters of transistors Q48 and Q49 are coupled to the collector of transistor Q52. The bases of transistors Q48 and Q49 are connected to receive the GN and GNN gain control signals applied to terminals 84 and 86, respectively. The base of transistor Q52 is connected to receive a current source bias voltage CURS2, while the emitter of this transistor is coupled to second supply terminal 66 through resistor R20.

The emitters of transistors Q50 and Q51 are connected to the collector of transistor Q53. The bases of transistors Q50 and Q51 are connected to receive the GNN and GN gain control signals applied to terminals

86 and 84, respectively. The collector of transistor Q51 is connected to first supply terminal 64. The base of transistor Q53 is connected to receive the second current source bias potential CURS2, while the emitter of this transistor is coupled to second supply terminal 66 through resistor R21.

Delay control current multiplexer 90 is coupled to transistors Q24 and Q25 of delay circuit 62 by means of delay control current mirror 96. Current mirror 96 includes transistors Q54, Q55, and Q56, and resistors R22, R23, and R24. The collector and base of transistor Q54 is connected to the collector of transistor Q48, while the emitter of this transistor is connected to first supply terminal 64 through resistor R22. The collector of transistor Q55 is coupled to the collector and base of transistor Q56. The base of transistor Q55 is connected to the base of transistor Q54. The emitter of transistor Q53 is connected to first supply terminal 64 through resistor R23. The emitter of transistor Q56 is connected to second supply terminal 66 through resistor R24. The base of transistor Q54 is connected to the base of transistors Q24 and Q25 of delay circuit 62.

The current source formed by transistor Q44 and resistor R16 is configured to produce a first gain pumping control current IG1. The current source formed by transistor Q45 and resistor R17 is configured to produce a second gain pumping control current IG2. In one preferred embodiment, second gain pumping control current IG2 is twenty times greater than first gain pumping control current IG1. The current source formed by transistor Q52 and resistor R20 is configured to provide a first gain delay control current ID1, while the current source formed by transistor Q53 and resistor R21 is configured to produce a second gain delay control current ID2.

When it is desired to operate charge pump 50 with its first or high gain pumping current, GN and GNN signals having logic HIGH and LOW logic states are applied to terminals 84 and 86, respectively. Current multiplexer 88 thereby selects first gain pumping control current IG1 since transistor Q40 will be turned ON, while transistor Q42 will be turned OFF. Current IG1 will flow through transistors Q46 and Q40, and is mirrored into current source transistors Q28 and Q32 of charge-up differential amplifier 56 and charge-down differential amplifier 58, respectively. First gain charge-up current IG1U and first gain charge-down current IG1D are thereby produced as a function of current IG1, and preferably have the same magnitude.

Delay current multiplexer 90 simultaneously selects first gain delay control current ID1 since transistor Q48 is turned ON, and transistor Q50 is turned OFF. Current ID1 will flow through transistors Q55 and Q56, is mirrored into transistors Q53 and Q54 as delay current ID', and is from there mirrored into current source transistors Q24 and Q25 which produce delay currents ID''. Currents ID'' are thereby provided as a function of current ID1. Characteristics of transistor Q52 and resistor R20 which form the current source, and/or the various resistors and transistors of current mirror 96, are selected to produce currents ID'' of a magnitude which will cause delay circuit 62 to delay switching response of charge-up differential amplifier 56 in response to charge-up control signals applied to charge-up input circuit 52 by a time delay corresponding to the inherent delay in current mirror 60 when operating with first gain charge-down current IG1D.

Should it be desired to operate charge pump 50 with its second gain pumping current, GN and GNN signals having logic LOW and HIGH states, respectively, are applied to terminals 84 and 86. Gain current multiplexer thereby selects second gain control current IG2 since transistor Q40 is switched OFF, and transistor Q42 is switched ON. Current IG2 flows through transistors Q60 and Q42, and is mirrored by current mirror 94 into transistors Q29 and Q33 of charge-up differential amplifier 56 and charge-down differential amplifier 58, respectively. Second gain charge-up pumping current IG2U and second gain charge-down pumping current IG2D are thereby applied to differential amplifiers 56 and 58, respectively, as a function of second gain control current IG2.

Concurrently, delay current multiplexer 90 will select second gain delay control current ID2 since transistor QS is switched OFF, and transistor Q50 is switched ON. Current ID2 will flow through transistors Q54 and Q50, be mirrored into transistors Q55 and Q56 as delay current ID', and is from there mirrored into current source transistors Q24 and Q25. Transistors Q24 and Q25 will product currents ID'' as a function of current ID2 so as to have a magnitude which causes delay circuit 62 to impose a delay between the switching of charge-up control signals UN and UNN and charge-up differential amplifier 56 which corresponds to the delay of current mirror 60 when operating with second gain charge-down current IG2D.

Having selected the desired pumping current or gain and its associated charge-up switching delay in the manner described above, charge pump 50 operates in a manner similar to that of charge pump 10 already described. Charge pump 50 operates in a charge-up mode sourcing either first gain charge-up current IG1U or second gain charge-up current IG2U to terminal 76 when charge-up signals U and UN have logic HIGH and LOW states, respectively, and charge-down control signals DN and DNN have logic LOW, and HIGH states, respectively. Charge pump 50 operates in its charge-down mode sinking one of either charge-down current IG1D' or IG2D' from output terminal 76 when control signals U and UN have logic LOW, HIGH states and control signals DN and DNN have logic HIGH, LOW states, respectively. When charge-up control signals U and UN have logic LOW, HIGH states and charge-down control signals DN and DNN have logic LOW, HIGH states, respectively, charge pump 50 is operated in its hold mode with both transistors Q30 and Q36 switched OFF. Output terminal 76 is thereby isolated from supply terminals 64 and 66.

The delay exhibited by delay circuitry 62 can be externally adjusted through the application of DADJH and DADJL signals applied to terminals 100 and 102, respectively. Terminal 100 is coupled to the emitter of transistor Q52, while terminal 102 is coupled to the emitter of transistor Q53. Signals DADJH and DADJL are used to adjust the magnitude of currents ID1 and ID2, and therefore the magnitude of currents ID'' and the delay of delay circuit 62.

External signals GADJL and GADJH can be applied to the emitters of transistors Q32 and Q33 through terminals 104 and 106, respectively. Signals GADJL and GADJH are used to adjust the magnitude of currents IG1DN and IG2D, and thereby the cancellation of the pump-up and pump-down currents at output terminal 76 when charge pump 50 is trying to pump up and down at the same time. This cancellation is generally of mini-

mal importance since the period of time that this situation occurs is typically very short.

Although the present invention has been described with reference to the preferred embodiments, those skilled in the art will realize that changes may be made in form and detail without departing from the spirit and scope of the invention.

What is claimed is:

1. A digitally controlled charge pump, including:
  - first and second supply terminals;
  - first input terminal means for receiving first digital charge control signals;
  - second input terminal means for receiving second digital charge control signals;
  - an output terminal;
  - first transistorized differential amplifier means including first control input terminal means coupled to the first input terminal means and second and third terminal means defining a first main current flow path and coupled between the first supply terminal and the output terminal, for controlling a first current flow of a first polarity between the first supply terminal and the output terminal through the first main current flow path as a function of the first control signals;
  - second transistorized differential amplifier means including a first control input terminal means coupled to the second input terminal means and second and third terminal means defining a second main current flow path and coupled between the first and second supply terminals, for controlling a second current flow between the first and second supply terminals through the second main current flow path as a function of the second control signals; and
  - transistorized pump current mirror means including first and second terminal means connected in series with the record main current flow path of the second differential means and third and fourth terminal means coupled between the output terminal and the second supply terminal, for producing and controlling a mirrored second current flow of a second polarity between the output terminal and the second supply terminal as a function of the second current flow.
2. The charge pump of claim 1 wherein:
  - the first differential amplifier means includes first current source means coupled between the first supply terminal and the output terminal, for producing the first current flow; and
  - the second differential amplifier means includes second current source means coupled between the first and second supply terminals, for producing the second current flow.
3. The charge pump of claim 2 wherein:
  - the first differential amplifier means includes:
    - a first transistor having first and second terminals connected in series with the first current source means and between the first supply terminal and the output terminal, and a control terminal coupled to the first input terminal means; and
    - a second transistor having first and second terminals coupled in series with the first current source means and between the first and second supply terminal means, and a control terminal coupled to the first input terminal means; and
  - the second differential means includes:



- a third transistor having first and second terminals coupled in series with the second current source means and between the first and second supply terminals, and a control terminal coupled to the second input terminal means; and
- a fourth transistor having first and second terminals coupled in series with the second current source means and between the first and second supply terminals, and a control terminal coupled to the second input terminal means.
4. The charge pump of claim 3 wherein the pump current mirror means includes:
- a fifth transistor having first and second terminals coupled in series with the first and second terminals of the third transistor and between the first and second supply terminals, and a control terminal; and
- a sixth transistor having first and second terminals coupled between the output terminal and the second supply terminal, and a control terminal coupled to the control terminal of the fifth transistor.
5. The charge pump of claim 4 wherein the pump current mirror means further includes:
- a first resistor coupled between the first or second terminal of the fifth transistor and the second supply terminal; and
- a second resistor coupled between the first or second terminal of the sixth transistor and the second supply terminal.
6. The charge pump of claim 4 wherein:
- the first and second transistors of the first differential means and the third and fourth transistors of the second differential means are transistors of a first conductivity type; and
- the fifth and sixth transistors of the pump current mirror means are transistors of a second conductivity type.
7. The charge pump of claim 6 wherein:
- the first, second, third and fourth transistors are PNP bipolar transistors; and
- the fifth and sixth transistors are NPN bipolar transistors.
8. The charge pump of claim 2 and further including:
- pumping current gain control terminal means for receiving pumping current gain control signals; and
- pumping current gain control transistorized circuit means coupled between the pumping current gain control terminal means and the first and second current source means, for causing the first current source means to produce a first current flow having one of a plurality of different magnitudes, and for causing the second current source means to produce a second current flow having one of a plurality of different magnitudes, in response to the pumping current gain control signals.
9. The charge pump of claim 8 wherein:
- the pump current mirror means is characterized by inherent delay periods functionally related to the magnitude of the second current flow; and
- the charge pump further includes controllable delay circuit means coupled between the first input terminal means and the output terminal and coupled to the pumping current gain control terminal means, for delaying response of the first current flow to the first charge control signals by delay periods equal to the inherent delay periods of the

- pump current mirror means; in response to the gain control signals.
10. The charge pump of claim 9 wherein the pumping current gain control circuit means includes:
- first gain control current source means for producing a first gain control current having a first magnitude;
- second gain control current source means for producing a second gain control current having a second magnitude;
- gain control current multiplexer means coupled to the gain control terminal means and to the first and second gain control current source means, for selecting one of the first and second gain control currents as a function of the gain control signals; and
- gain control current mirror means coupled between the gain control current multiplexer means and the first and second current source means, for mirroring the selected gain control current to the first and second current source means and causing the magnitude of the first and second currents to be produced as a function of the magnitude of the selected gain control current.
11. The charge pump of claim 10 wherein:
- the first current source means of the first differential amplifier means includes:
- a first gain first current source; and
- a second gain first current source;
- the second current source means includes:
- a first gain second current source; and
- a second gain second current source; and
- the gain control current mirror means includes:
- a first gain current mirror coupled to the gain control current multiplexer means, the first gain first current source and the first gain second current source, for mirroring the first gain control current to the first gain first current source and to the first gain second current source when the first gain control current is selected by the gain control current multiplexer means; and
- a second gain current mirror coupled to the gain control current multiplexer means, the second gain first current source and the second gain second current source, for mirroring the second gain control current to the second gain first current source and to the second gain second current source when the second gain control current is selected by the gain control current multiplexer means.
12. The charge pump of claim 9 wherein the controllable delay circuit means includes:
- a current responsive delay circuit coupled between the first input terminal means and the first differential means, and including a delay circuit current source;
- first delay control current source means for producing a first delay control current having a first magnitude;
- second delay control current source means for producing a second delay control current having a second magnitude;
- delay control current multiplexer means coupled to the gain control terminal means and to the first and second delay control current source means, for selecting one of the first and second delay control currents as a function of the gain control signals; and

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delay control mirror means for mirroring the selected delay control current to the delay circuit current source and causing the magnitude of the current produced by the delay current source to be produced as a function of the magnitude of the selected delay control current.

13. The charge pump of claim 1 and further including:

first transistorized input circuit means coupled between the first input terminal means and the first control input terminal means of the first differential amplifier means, for level shifting the first digital charge control signals; and

second transistorized input circuit means coupled between the second input terminal means and the first control input terminal means of the second

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differential amplifier means, for level shifting the second digital charge control signals.

14. The charge pump of claim 1 wherein:

the pump current mirror means is characterized by an inherent delay period, between the response of the mirrored second current flow to the second current flow; and

the charge pump further includes delay circuit means coupled between the first input terminal means and the output terminal, for delaying the response of the first current flow to the first charge control signals by a delay period equal to the inherent delay period of the pump current mirror means.

15. The charge pump of claim 14 wherein the delay circuit means includes circuit means connected between the first differential amplifier means and the pump current mirror means.

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**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 4,847,519

DATED : July 11, 1989

INVENTOR(S) : Jerry R. Wahl et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12, line 38, delete "record" and insert  
--second--.

**Signed and Sealed this**  
**Twenty-first Day of November, 1989**

*Attest:*

JEFFREY M. SAMUELS

*Attesting Officer*

*Acting Commissioner of Patents and Trademarks*

[54] VOLTAGE REGULATOR CIRCUIT

[75] Inventor: Makoto Ito, Yokohama, Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

[21] Appl. No.: 450,569

[22] Filed: Dec. 14, 1989

[30] Foreign Application Priority Data

Feb. 16, 1989 [JP] Japan ..... 1-36479

[51] Int. Cl.<sup>5</sup> ..... H03L 1/00; H03K 3/354

[52] U.S. Cl. .... 307/296.8; 307/296.2

[58] Field of Search ..... 307/296.8, 296.7, 296.2, 307/296.1, 491, 494, 304

[56] References Cited

U.S. PATENT DOCUMENTS

4,439,692 3/1984 Beekmans et al. .... 307/304  
4,553,047 11/1985 Dillinger et al. .... 307/296.8  
4,631,421 12/1986 Inoue et al. .... 307/296.2  
4,961,167 10/1990 Kumanoya et al. .... 307/296.2  
4,964,082 10/1990 Sato et al. .... 307/296.2

FOREIGN PATENT DOCUMENTS

24903 3/1981 European Pat. Off. .  
301184 2/1989 European Pat. Off. .  
3704609 8/1987 Fed. Rep. of Germany .  
3814667 11/1988 Fed. Rep. of Germany .

OTHER PUBLICATIONS

Pathak et al, "A 19-ns 250-MW CMOS Erasable Pro-

grammable Logic Device", IEEE Journal of Solid-State Circuits, vol. SC-21, No. 5, Oct. 1986, pp. 775-784. Patent Abstracts of Japan, vol. 10, No. 347 [E-457] [2403] Oct. 21, 1986.

Oto et al, "High-Voltage Regulation and Process Considerations for High-Density 5V-Only E<sup>2</sup>PROM's", IEEE Journal of Solid-State Circuits, vol. SC-18, No. 5, Oct. 1983, pp. 532-538.

McCreary et al, "Techniques for a 5-V-Only 64K EPROM Based Upon Substrate Hot-Electron Injection", IEEE Journal of Solid-State Circuits, vol. SC-19, No. 1, Feb. 1984, pp. 135-143.

Primary Examiner—Stanley D. Miller

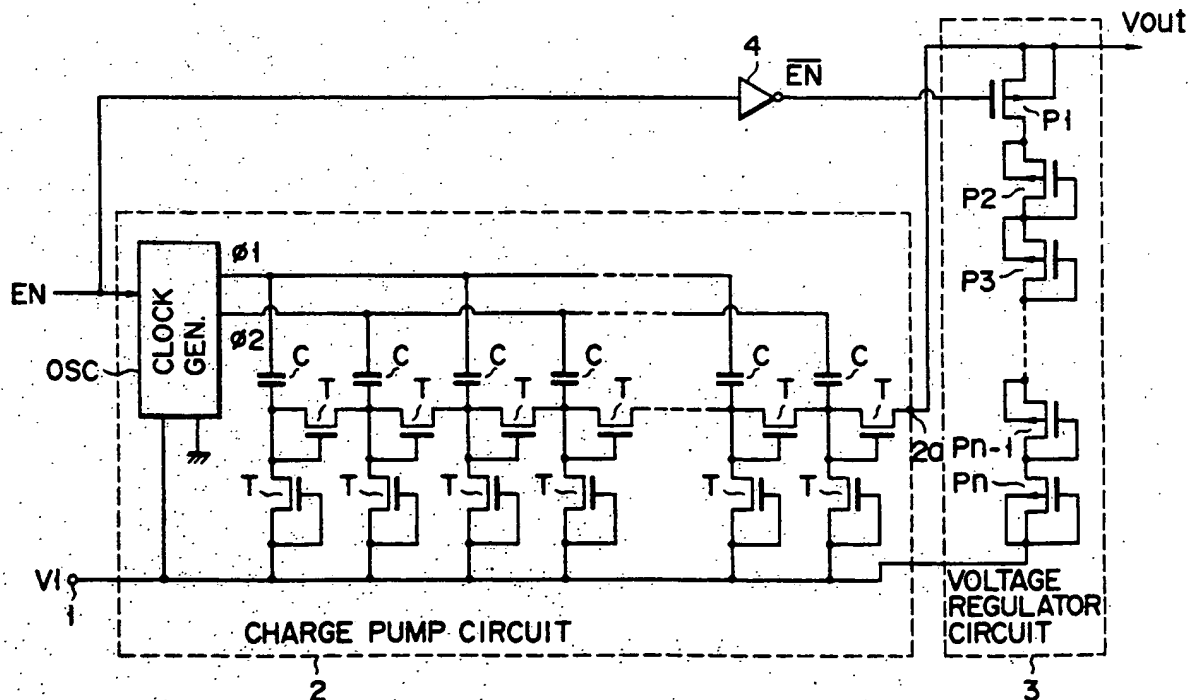
Assistant Examiner—Richard Roseen

Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett and Dunner

[57] ABSTRACT

A voltage regulator circuit for use with an integrated circuit with a charge pump circuit having a voltage output terminal and a voltage input terminal in which a plurality of voltage regulating P-channel MOS transistors, each of which has its source and substrate connected together and its gate and drain connected together, are connected in series between the voltage output and input terminals of the charge pump circuit.

8 Claims, 4 Drawing Sheets



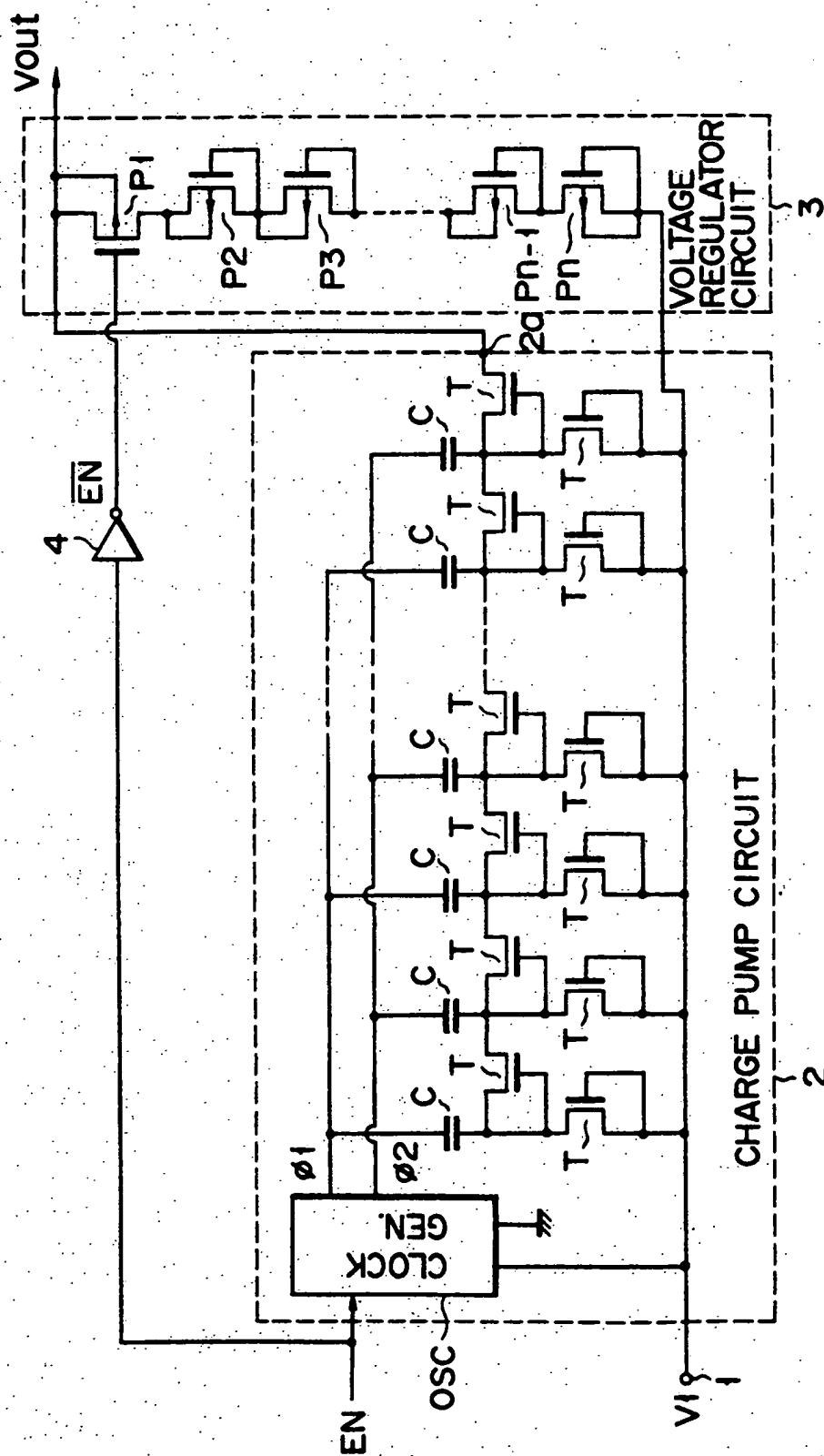


FIG. 1

FIG. 2

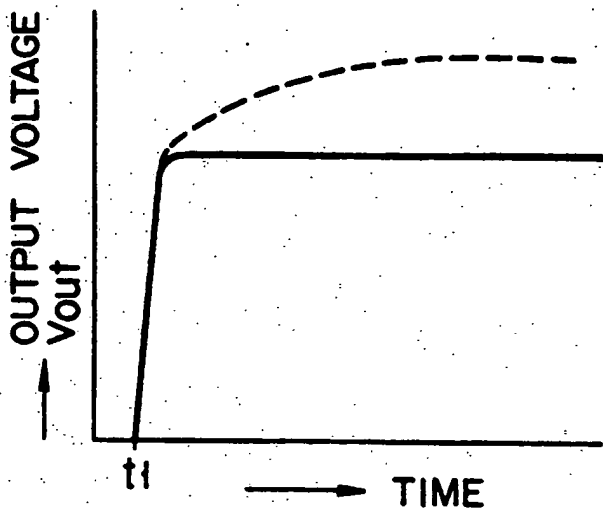


FIG. 3

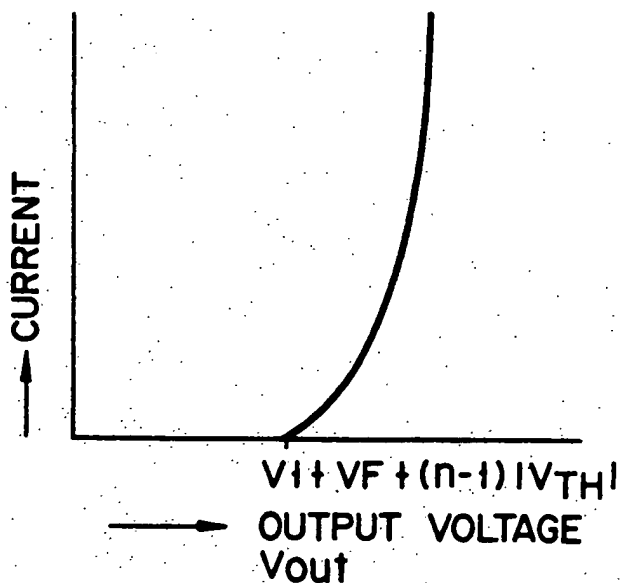
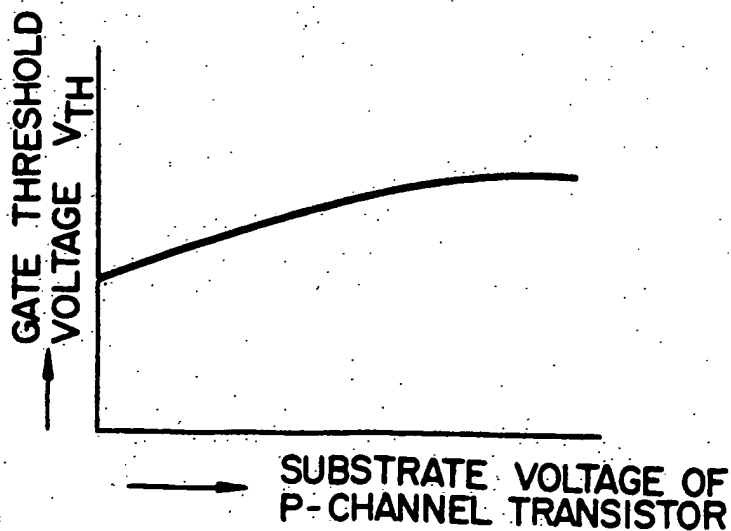


FIG. 4



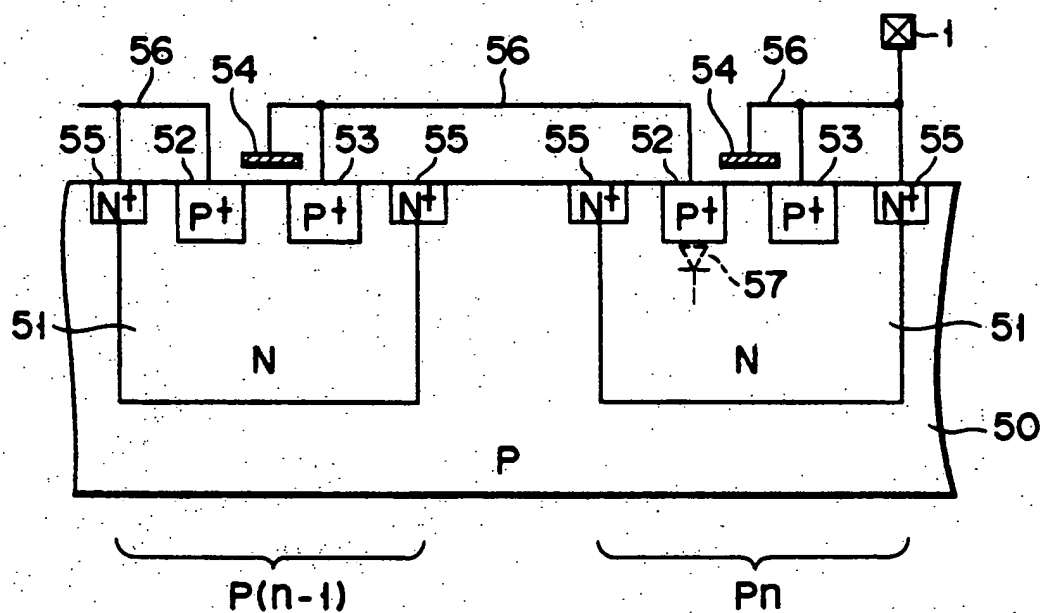


FIG. 5

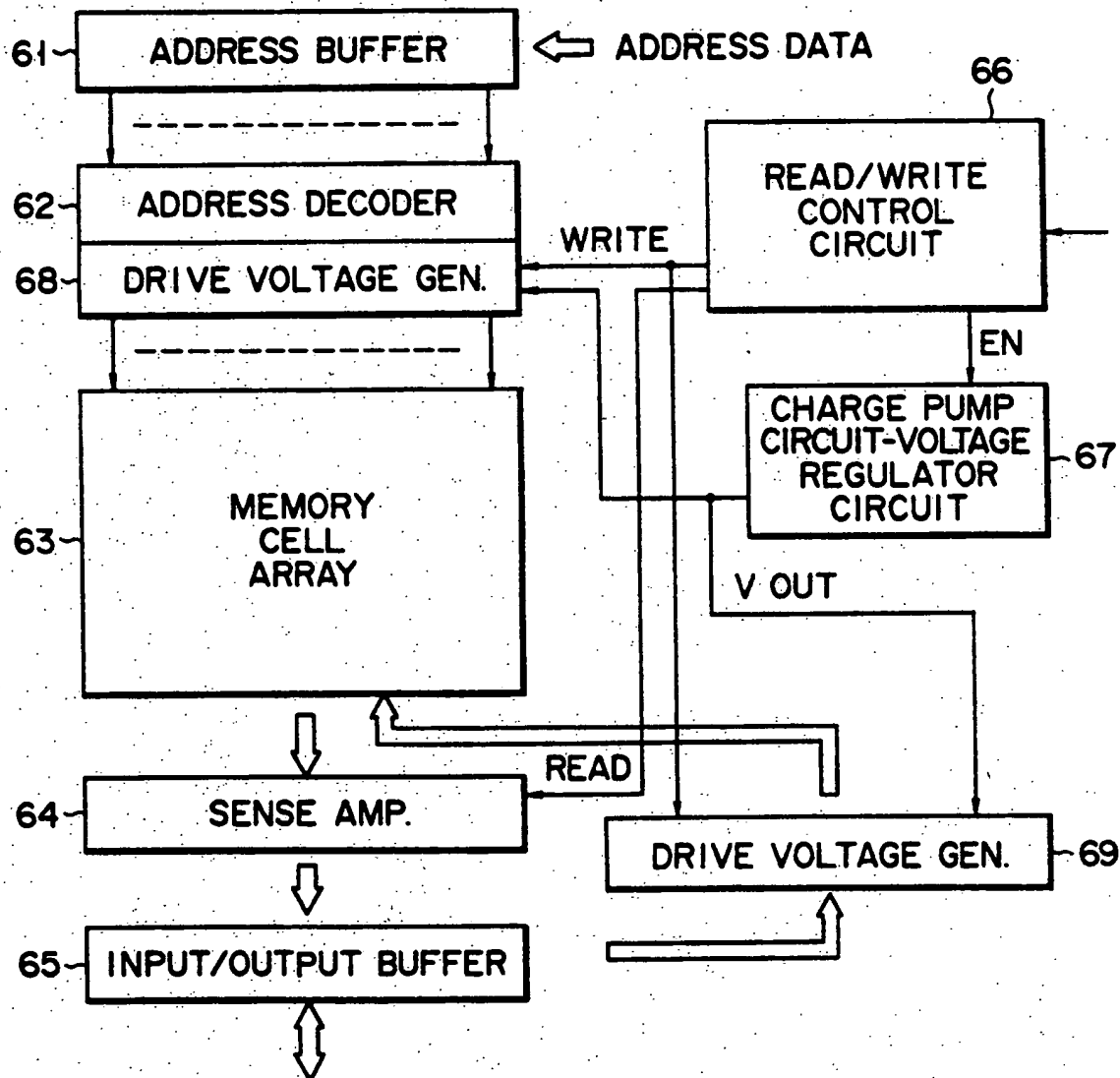


FIG. 6

## VOLTAGE REGULATOR CIRCUIT

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a voltage regulator circuit for holding an output voltage of a charge pump circuit in a semiconductor integrated circuit substantially constant.

#### 2. Description of the Related Art

Typical examples of voltage regulators adapted to hold output voltages of charge pump circuits in semiconductor integrated circuits substantially constant are described in the following articles (1)-(3).

(1) In the article entitled "High-Voltage Regulation and Process Considerations for High-Density 5 V-only EPROM's" by DUANE H. OTO et al., IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 5, Oct. 1983, pp 532-538, the output voltage of the charge pump circuit is compared with a reference voltage to control a clock signal for the charge pump circuit.

(2) In the article entitled "Techniques for a 5-V-Only 64K EPROM Based Upon Substrate Hot-Electron Injection" by JAMES L. MCGREARY et al., IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 1, Feb. 1984, pp 135-143, the output voltage of the charge pump circuit is applied to a plurality of MOS transistors to produce a control voltage which, in turn, is applied to the gate of a MOS transistor connected between the output node of the charge pump circuit and the supply voltage node so as to cause it to conduct. The output voltage is clamped by the MOS transistor.

(3) In the article entitled "A 19-ns 250-mW CMOS Erasable Programmable Logic Device" by JAGDISH PATHAK, IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, Oct. 1986, pp 775-784, two N-channel MOS transistors, each of which has its gate and drain connected together, are connected in series between the output node and input node of the charge pump circuit to produce an output voltage of  $V_{pp} + 2 V_{tn}$  ( $V_{pp}$  stands for a input voltage and  $V_{tn}$  stands for the threshold voltage of an N-channel MOS transistor).

However, the voltage-regulating N-channel MOS transistors used in the third article have a wide variability of threshold voltage because of the effect of back-gate bias. Thus, for a desired voltage regulating property it is difficult to determine the number of N-channel transistors to be connected in series. In addition, in case where a high voltage is abruptly output from the charge pump circuit and applied across the drain-source path of the N-channel MOS transistor, the transistor may be short-circuited. In such case, the voltage-regulating property of the voltage regulator circuit would be deteriorated because of the N-channel MOS transistor. In the worst case, the voltage regulation would become impossible. An integrated circuit incorporating the voltage-regulating N-channel MOS transistors is thus low in reliability.

### SUMMARY OF THE INVENTION

It is accordingly an object of the present invention to provide a voltage regulator circuit which solves the problem of low reliability of the voltage regulating property, which arises from difficulty in determining the number of N-channel MOS transistors used as voltage-regulating MOS transistors for obtaining a desired voltage-regulating property.

It is another object of the present invention to provide a voltage regulator circuit which solves the problem of deterioration of the voltage regulating property of MOS transistors when they are abruptly supplied with a high voltage from a charge pump circuit, which might cause incapability of the voltage regulation in the worst case, and which avoids the flow of unnecessary dc current through the MOS transistors when no input voltage is applied thereto from the charge pump circuit.

It is still another object of the present invention to provide a voltage regulator circuit which permits the avoidance of the flow of unnecessary dc current through voltage-regulating MOS transistors in case where a reference voltage becomes higher than an output voltage of the charge pump circuit at such a time when a test is made.

To attain the above objects, according to the present invention, a plurality of voltage-regulating P-channel MOS transistors, each of which has its source and substrate connected together and its gate and drain connected together, are connected in series between an voltage output terminal and an voltage input terminal of a charge pump circuit in a semiconductor integrated circuit. Such a P-channel MOS transistor having its source and substrate connected together and its gate and drain connected together is not very subject to the effect of back-gate bias. It is therefore easy to determine the number of P-channel MOS transistors to be connected in series for a desired voltage regulating property, improving the reliability of voltage regulating property.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a voltage regulator circuit embodying the present invention;

FIG. 2 is a graph illustrating an exemplary voltage regulating property of the voltage regulator circuit of FIG. 1;

FIG. 3 is a graph illustrating an exemplary output voltage-current characteristic of the voltage regulator circuit of FIG. 1;

FIG. 4 is a graph illustrating the effect of back-gate bias of P-channel MOS transistors in the voltage regulator circuit of FIG. 1;

FIG. 5 is a sectional view of part of P-channel MOS transistors in the voltage regulator circuit of FIG. 1; and

FIG. 6 is a block diagram of a nonvolatile memory integrated circuit in which the present invention finds application.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to a charge pump circuit-voltage regulator circuit formed in a semiconductor integrated circuit according to the present invention comprises a voltage input terminal 1 for receiving a input voltage  $V_1$ , a charge pump circuit 2 for producing a high output voltage  $V_{out}$  from the input voltage  $V_1$  at input terminal 1, a voltage regulator circuit 3 for regulating the output voltage  $V_{out}$  of charge pump circuit 2 to a substantially constant level and an inverter 4 for inverting an enable signal EN to apply an inverted enable signal  $\overline{EN}$  to voltage regulator circuit 3.

Charge pump circuit 2 comprises a clock generator OSC for producing nonoverlapping two-phase clock signals  $\phi_1$  and  $\phi_2$  when the enable signal EN is active (at a "High" level), boosting capacitors C each of which

receives at one end the clock signal  $\phi 1$  or  $\phi 2$  and MOS transistors T connected to the other end of each of capacitors C, thereby to produce output voltage  $V_{out}$  boosted relative to input voltage  $V_1$ .

In voltage regulator circuit 3, a plurality of P-channel enhancement MOS transistors  $P2-P(n-1)$ , each of which has its source and substrate connected together and its gate and drain connected together, are connected in series between voltage output terminal 2a and voltage input terminal 1 of charge pump circuit 2. In addition, the source-drain path of a P-channel MOS transistor P1 with its source and substrate connected together and its gate supplied with inverted signal  $\overline{EN}$  of enable signal EN is connected between voltage output terminal 2a of charge pump circuit 2 and one end of the series connection of P-channel MOS transistors P2 to  $P(n-1)$  (namely, the connection point of the source and substrate of P-channel MOS transistor P2). Moreover, between the other end of the series connection of P-channel MOS transistors P2 to  $P(n-1)$  (namely, the connection point of the gate and drain of P-channel MOS transistor  $P(n-1)$ ) and voltage input terminal 1 is connected a P-channel MOS transistor  $P_n$  having its gate, drain and substrate connected together. The MOS transistor  $P_n$  may be replaced with a diode.

Next, the operation of voltage regulator 3 will be described with reference to FIGS. 2 and 3 which illustrate the voltage regulating property and the voltage vs. current characteristic, respectively.

When the enable signal EN is inactive (at a "Low" level) and thus inverted signal  $\overline{EN}$  is at a "H" level, charge pump circuit 2 is disabled, and P-channel MOS transistor P1 is in the off state so that voltage regulator circuit 3 is disabled. When enable signal EN is rendered active (goes to a "H" level) at a time  $t_1$ , charge pump circuit 2 is enabled and P-channel MOS transistor P1 is rendered on. Consequently the output voltage of charge pump circuit 2 rises and increases gradually as indicated in dotted line in FIG. 2, but output voltage  $V_{out}$  is regulated to a substantially constant level by means of voltage regulator circuit 3. It is to be noted here that the output voltage  $V_{out}$  is given by

$$V_{out} = V_1 + VF + (n-1)V_{th}$$

where VF stands for the forward voltage of the PN junction diode of P-channel MOS transistor  $P_n$  and  $V_{th}$  stands for the threshold voltage of each of P-channel MOS transistors P1 to  $P(N-1)$ .

According to voltage regulator circuit 3 described above, as voltage regulating MOS transistors are used P-channel transistors P2 to  $P(n-1)$  each of which has its source and substrate connected together and its gate and drain connected together. P-channel transistors P2 to  $P(n-1)$  suffers such an effect of back-gate bias as shown in FIG. 4, which is not very serious. It is therefore easy to determine the number of P-channel MOS transistors for obtaining a desired voltage regulating property. The reliability of the voltage regulating property thus increases.

Even if a high voltage is abruptly applied to the source of P-channel MOS transistor P1 from charge pump circuit 2 when enable signal EN is rendered active ("H" level), transistor P1 is turned on by inverted signal  $\overline{EN}$  applied to its gate at the same time charge pump circuit 2 starts operating. Thus, the reliability of P-channel MOS transistor P1 will not be degraded. The problems of degradation of the voltage regulating property and incapability of voltage regulation will not arise.

The reliability of an integrated circuit incorporating voltage regulator 3 will not be degraded.

Moreover, when a boosted voltage is not applied to voltage regulator circuit 3 from charge pump circuit 2, that is, when the enable signal EN is inactive (at a "L" level), no dc current will flow through voltage regulator circuit 3 and thus unnecessary current dissipation is not produced because P-channel MOS transistor P1 is turned off by the inverted enable signal  $\overline{EN}$ .

Also, with such a voltage regulator 3 as described above, even when the potential at voltage input terminal 1 becomes higher than that at voltage output terminal 2a at a time of testing, for example, unnecessary dc current flow in the opposite direction from voltage input terminal 1 to voltage output terminal 2a will be avoided because of the existence of the PN junction diode of P-channel MOS transistor  $P_n$ .

FIG. 5 illustrates a sectional structure of P-channel MOS transistors  $P_n$  and  $P(n-1)$  which constitute part of voltage regulator circuit 3. That is, reference numeral 50 denotes a P-type semiconductor substrate, 51 an N well, 52 a P+ impurity region for the source, 53 a P+ type impurity region for the drain, 54 a gate electrode, 55 an N+ type well electrode and 56 wiring. As can be seen from the figure, because a PN junction diode 57 is formed between the source and the substrate in P-channel MOS transistor  $P_n$  which has its substrate (N well), gate and drain connected together, reverse current flow from voltage input terminal 1 can be avoided.

It is to be noted that, if P-channel MOS transistor P1 is omitted in the above embodiment, the effect of improved reliability of the voltage-regulating property from the existence of P-channel MOS transistors P2-P(n-1) and the effect resulting from the existence of P-channel MOS transistor  $P_n$  will be obtained.

FIG. 6 is a block diagram of a nonvolatile memory integrated circuit, for example, an EPROM integrated circuit, to which the present invention is applied.

In the EPROM integrated circuit, reference numeral 61 denotes an address buffer to which address data is applied, 62 an address decoder, 63 a memory cell array, 64 a sense amplifier, 65 an input/output buffer, 66 a read/write control circuit, 67 such a charge pump circuit-voltage regulator circuit as shown in FIG. 1, 68 a row drive voltage generator, and 69 a column drive voltage generator. Sense amplifier 64 is enabled by a read control signal READ from read/write control circuit 66. When supplied with the enable signal EN from read/write control circuit 66, charge pump circuit-voltage regulator circuit 67 produces a boosted voltage  $V_{out}$  regulated to a substantially constant level. Row drive voltage generator 68 applies the boosted voltage  $V_{out}$  from charge pump circuit-voltage regulator circuit 67 to a selected word line of memory cell array 63 in a write mode in which the generator 68 receives a write control signal WRITE from read/write control circuit 66. In the write mode, column drive voltage generator 69 is responsive to the write control signal WRITE from read/write control circuit 66 to apply the boosted voltage  $V_{out}$  from charge pump circuit-voltage regulator circuit 67 to a selected column line of memory cell array 63 according to input data from input/output buffer 65.

In the above EPROM integrated circuit, the high boosted voltage  $V_{out}$  is applied to the gate and drain of a memory cell connected to the selected word line and



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column line of memory cell array 63 so that input data is written into the selected memory cell.

It is to be noted that the voltage regulator circuit of the present invention may be applied to E<sup>2</sup>PROM integrated circuits and logic integrated circuits incorporating nonvolatile memory cells.

Although only one embodiment of the invention has been disclosed and described, it is apparent that other embodiments and modifications of the invention are possible.

What is claimed is:

1. A voltage regulator circuit for use with a semiconductor integrated circuit having a charge pump circuit with a voltage output terminal and a voltage input terminal, including a plurality of P-channel MOS transistors connected in series between said voltage output terminal and said voltage input terminal of said charge pump circuit, each of said P-channel MOS transistors having its source and substrate connected together and its gate and drain connected together.

2. A voltage regulator circuit according to claim 1, in which between one end of the series connection of said P-channel MOS transistors and said voltage output terminal of said charge pump circuit is connected a P-channel MOS transistor which has its source and substrate connected together and is supplied at its gate with an enable signal synchronized with an enable signal for said charge pump circuit.

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3. A voltage regulator circuit according to claim 1, in which between the other end of the series connection of said P-channel MOS transistors and said voltage input terminal of said charge pump circuit is connected a P-channel MOS transistor having its substrate, gate and drain connected together or a diode.

4. A voltage regulator circuit according to claim 2, in which a P-channel MOS transistor having its substrate, gate and drain connected together or a diode is connected between the other end of the series connection of said P-channel MOS transistors and said voltage input terminal of said charge pump circuit.

5. A voltage regulator circuit according to claim 1, in which said voltage regulator circuit regulates a boosted voltage to be applied to memory cells of a nonvolatile memory integrated circuit.

6. A voltage regulator circuit according to claim 2, in which said voltage regulator circuit regulates a boosted voltage to be applied to memory cells of a nonvolatile memory integrated circuit.

7. A voltage regulator circuit according to claim 3, in which said voltage regulator circuit regulates a boosted voltage to be applied to memory cells of a nonvolatile memory integrated circuit.

8. A voltage regulator circuit according to claim 4, in which said voltage regulator circuit regulates a boosted voltage to be applied to memory cells of a nonvolatile memory integrated circuit.

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US006788130B2

(12) **United States Patent**  
**Pauletti et al.**

(10) **Patent No.:** **US 6,788,130 B2**  
(45) **Date of Patent:** **Sep. 7, 2004**

(54) **EFFICIENT CHARGE PUMP CAPABLE OF HIGH VOLTAGE OPERATION**

(75) Inventors: **Timothy P. Pauletti**, Plano, TX (US);  
**David Baldwin**, Allen, TX (US); **John H. Carpenter, Jr.**, Rowlett, TX (US)

(73) Assignee: **Texas Instruments Incorporated**,  
Dallas, TX (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/254,336**

(22) Filed: **Sep. 25, 2002**

(65) **Prior Publication Data**

US 2004/0056707 A1 Mar. 25, 2004

(51) Int. Cl.<sup>7</sup> ..... **G05F 03/02**

(52) U.S. Cl. .... **327/536; 327/537; 363/59**

(58) Field of Search ..... **327/536, 537; 363/59**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,029,282 A \* 7/1991 Ito ..... 327/536

5,561,385 A \* 10/1996 Choi ..... 327/536  
5,672,992 A \* 9/1997 Nadd ..... 327/390  
6,157,242 A 12/2000 Fukui  
6,194,954 B1 \* 2/2001 Kim et al. .... 327/535  
6,215,708 B1 \* 4/2001 Lien et al. .... 365/189.09  
6,456,151 B1 \* 9/2002 Pontarollo ..... 327/536  
6,525,595 B2 \* 2/2003 Oku ..... 327/536  
2002/0130701 A1 \* 9/2002 Kleveland ..... 327/536

\* cited by examiner

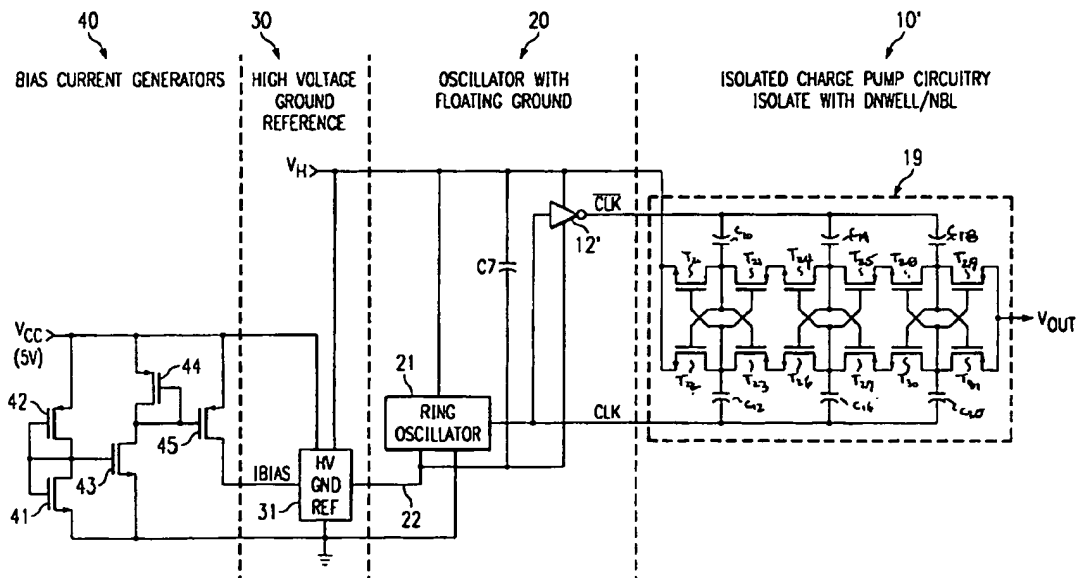
*Primary Examiner*—Terry D. Cunningham

(74) *Attorney, Agent, or Firm*—April M. Mosby; Wade James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

A high voltage integrated circuit operable in a system having a low voltage reference, a high voltage reference, and a ground, for providing an output voltage higher than the high voltage reference. The integrated circuit includes a high voltage ground reference circuit, operable to provide a high voltage ground reference node. Also included is an oscillator, operable to provide a clock signal, the oscillator being connected to the high voltage reference and to the high voltage ground reference node. An isolated charge pump circuit is provided, operable to generate the output voltage and isolated in the integrated circuit from other circuitry.

**6 Claims, 3 Drawing Sheets**



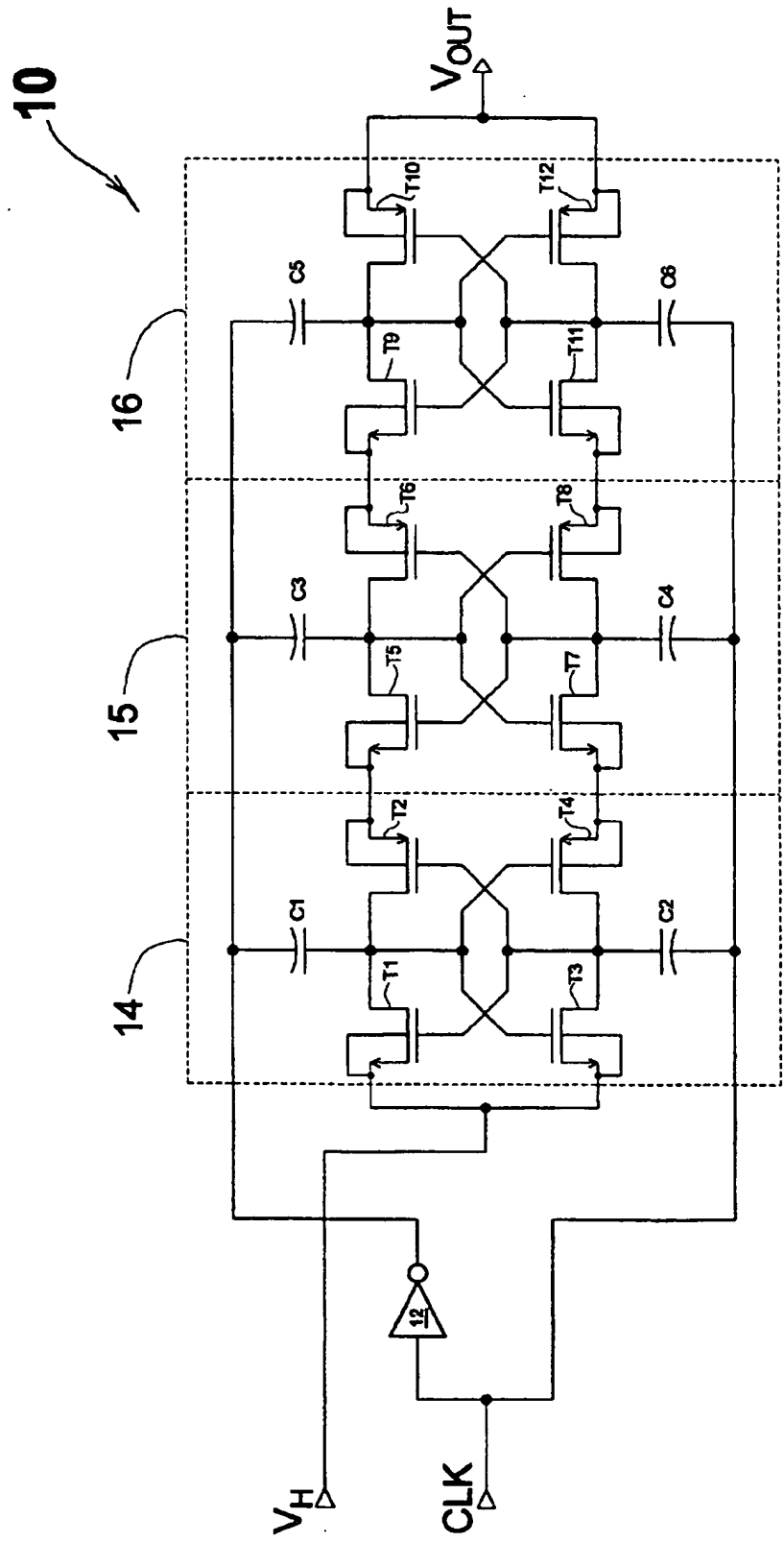
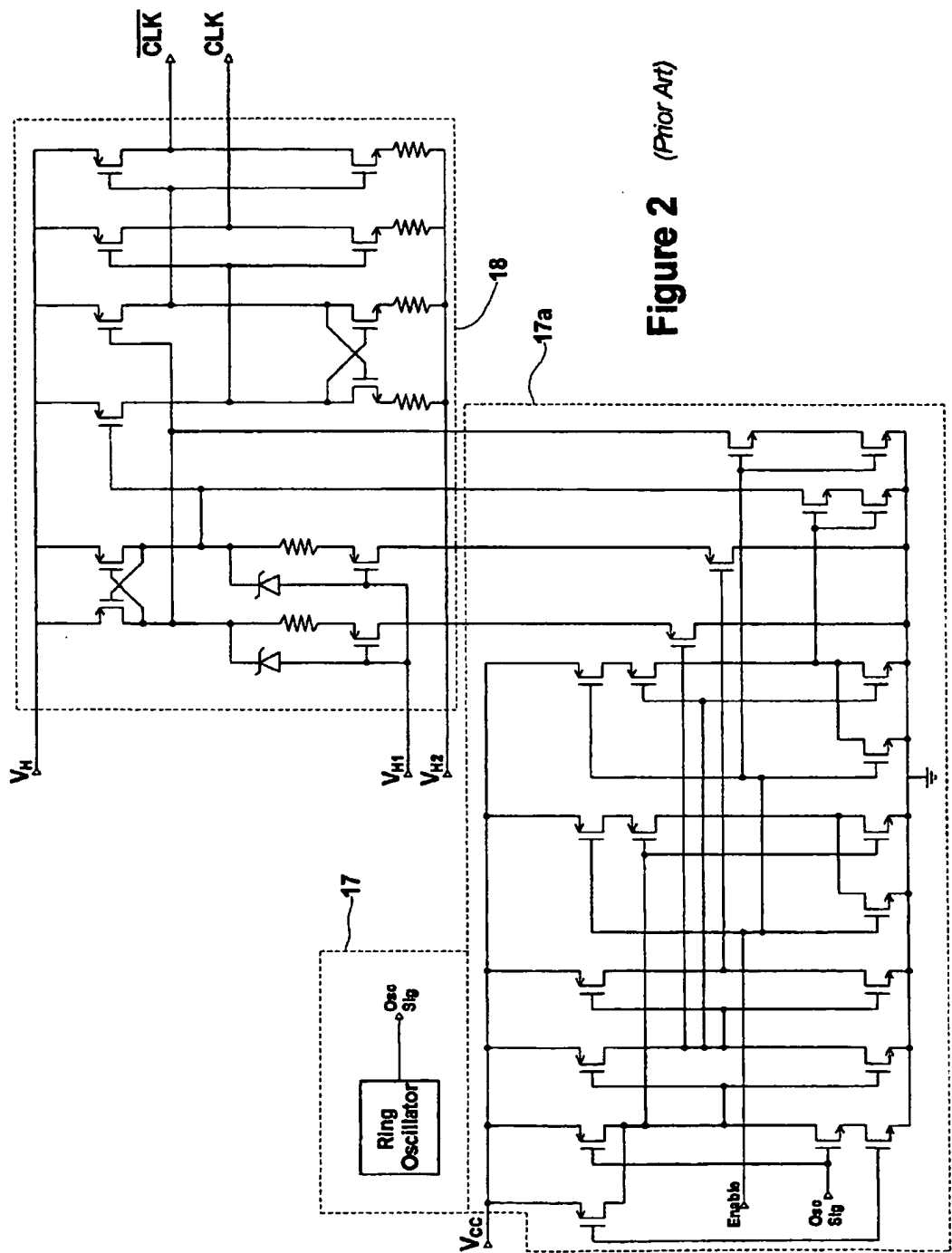


Figure 1 (Prior Art)



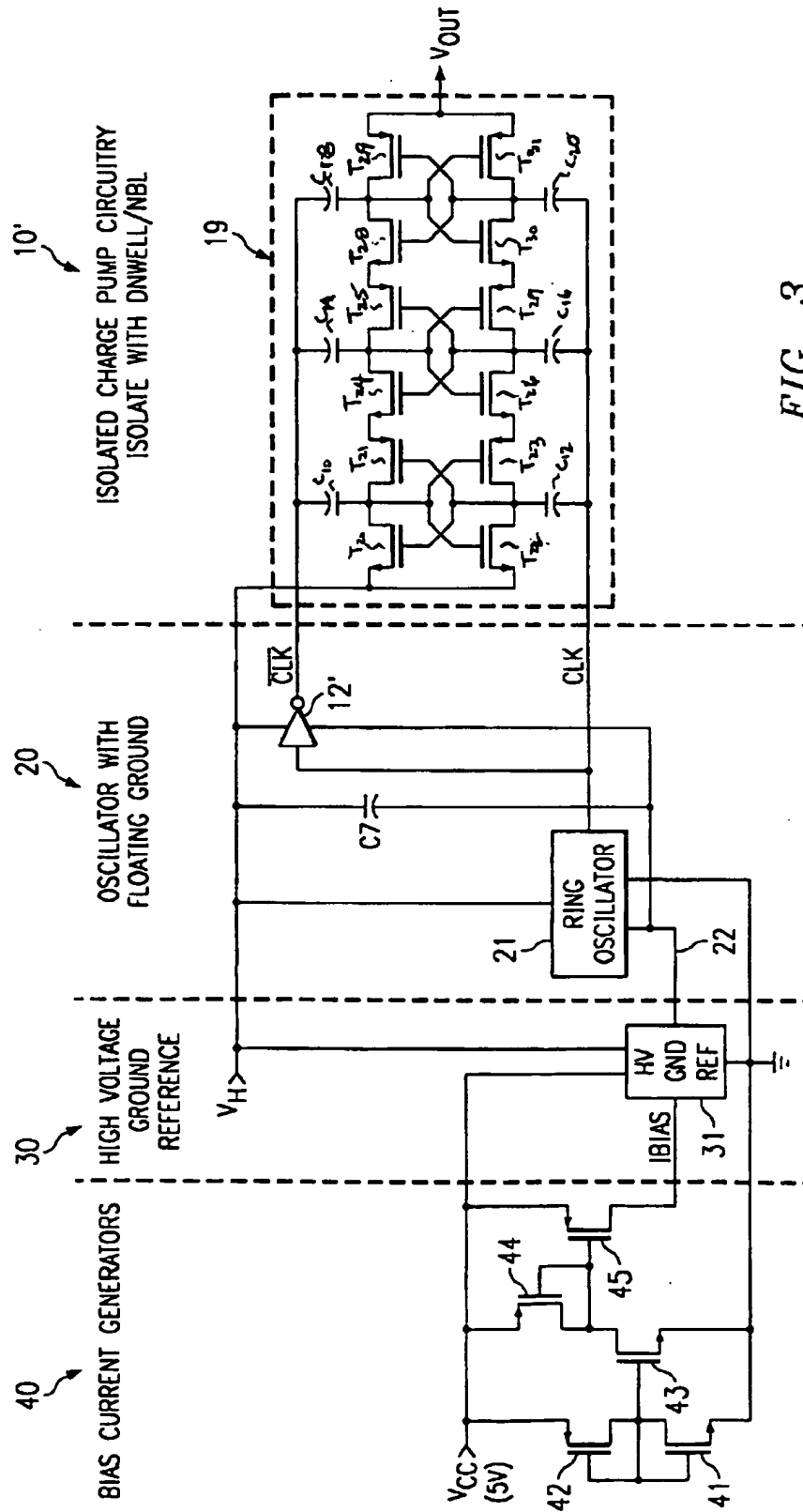


FIG. 3

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# EFFICIENT CHARGE PUMP CAPABLE OF HIGH VOLTAGE OPERATION

## TECHNICAL FIELD OF THE INVENTION

This invention relates to charge pump circuits, and more particularly relates to charge pump circuits capable of high voltage operation.

## BACKGROUND OF THE INVENTION

The charge pump is a type of DC-DC voltage converter circuit that uses capacitors to store and transfer energy, typically in order to generate a higher voltage than that supplied to the circuit. They are used in a variety of applications. They are commonly used, for example, to generate the higher voltages required for the writing and erasing operations of non-volatile memories such as flash memories. They are also used to achieve higher gate drive voltages ( $V_{gs}$ ) on MOSFETs to obtain a lower resistance from drain-to-source while the device is on ( $R_{dson}$ ) for a same size device. They are also used as a supply in low voltage applications. The foregoing list of applications is not exhaustive.

A charge pump is typically constructed in a series of stages that step up the voltage created by the charge stored in one stage to a higher voltage in the next. FIG. 1 is a circuit diagram of an exemplary prior art two-phase charge pump circuit 10. The circuit includes metal oxide semiconductor field effect transistors ("MOSFETs," or, simply "FETs") T1-T12, capacitors C1-C6, and an inverter, connected as shown. The circuit has three identical stages 14, 15, 16, each stage including four FETs (T1-T4, T5-T8 and T9-T12, respectively), and two capacitors (C1 & C2, C3 & C4 and C5 & C6, respectively), connected as shown. A high voltage  $V_H$  is provided to the first stage 14, while a square wave clock signal CLK is provided to one side of all stages, and its inverse, generated by inverter 12, is provided to the other side of all stages, as shown.

Each stage operates in similar manner, with increasing voltage being provided successively at the output of each stage, in a manner well known in the art. Thus, in successive half cycles of CLK, FETs T1-T12 operate in complementary fashion to pump charge onto the plates of capacitors C1-C6, creating a voltage across the capacitors, and then to use that voltage, which is raised during the transfer cycle by the voltage of the clock signal, to elevate the voltage across a capacitor in a next stage that is on the same side of the circuit by that voltage, less the threshold voltage of a connecting FET. The last stage provides an output voltage  $V_{OUT}$ .

However, as the voltage generated by each stage increases, the threshold voltages of the transferring FETs can increase, due to the well-known backgating effect. This causes a successively lower voltage increase from one stage to the next. In fact, the threshold voltage of a transferring FET can become the same as the voltages of the clock signals driving the pump, at which point no further boosting is possible. To avoid this, in the charge pump circuit 10 the backgate is tied to the source on each FET, as shown. Thus,  $V_{sb}=0$ . This requires isolation of the circuit.

In addition, there is a significant challenge in designing a charge pump that can work over a large voltage range. One reason for this is that the charge pump voltage is usually referenced to the supply in some way, and as the supply voltage increases so too does  $V_{OUT}$ . However, the capacitors are typically diffusion capacitors, which have a specific voltage tolerance. When the clock signal switches from the

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supply voltage in its high phase to a low voltage in its low phase, the voltage tolerance of a capacitor can be exceeded, causing breakdown of the capacitor. Thus, in designing a high voltage charge pump that can work over a very wide supply range, one must solve the problem of how to clock it, but not exceed the voltage tolerance of the capacitors.

U.S. Pat. No. 6,157,242, which issued on Dec. 5, 2000, to Haruyasu Fukui, et al., and was assigned to Sharp Kabushiki Kaisha, proposes a charge pump circuit arrangement to allow operation at a wide range of power supply voltages. In their scheme, normal clock signals are provided to early stages of a charge pump, but in order to overcome the problem associated with increasing transferring FET threshold voltage, and thus allow a higher output voltage to be generated, a clock signal boost circuit is provided for boosting voltages of the clock signals of later stages. In order to address the problem of having the charge pump work over a very wide range and still stay within the tolerances of the capacitors, they propose having their clock boosting capable of being enabled and disabled. For lower supply voltages, clock boosting would be enabled, while for higher supply voltages clock boosting would be disabled, to protect the capacitors against breakdown. However, this proposed solution provides a limited output voltage.

Another prior art solution, shown in FIG. 2, utilizes a conventional ring oscillator 17, with transfer circuitry 17a providing the oscillator signal to high voltage level shifters 18 to raise both the high and low voltage levels of the clock signals CLK and  $\overline{CLK}$ , in order to provide a higher output voltage, and using high voltage components in the charge pump (not shown). In this solution, high voltage references  $V_{H1}$  and  $V_{H2}$  are referenced linearly to supply, and provided to the level shifters, as shown. For example,  $V_{H1}$  could be at supply voltage,  $V_{supply}$ , such as 5 volts, and  $V_{H2}$  at some specified voltage below  $V_{supply}$ , with both rising and falling with  $V_{supply}$ , but holding the difference in their voltages to close tolerance. While this solution does not limit the output voltage, as in the arrangement disclosed in U.S. Pat. No. 6,157,242, it does require a relatively large integrated circuit area to implement, as it requires the additional area for the level shifters, and for high voltage components used in the design. In addition, the approach shown in FIG. 2 is limited in clocking frequency because of the high voltage level shifters 18. The FET devices in that circuit are, of necessity, large and have high intrinsic capacitance, and so do not switch rapidly.

## SUMMARY OF THE INVENTION

In accordance with the present invention there is provided a high voltage integrated circuit operable in a system having a low voltage reference, a high voltage reference, and a ground, for providing an output voltage higher than the high voltage reference. The integrated circuit includes a high voltage ground reference circuit, operable to provide a high voltage ground reference node. Also included is an oscillator, operable to provide a clock signal, the oscillator being connected to the high voltage reference and to the high voltage ground reference node. An isolated charge pump circuit is provided, operable to generate the output voltage and isolated in the integrated circuit from other circuitry.

These and other features of the invention will be apparent to those skilled in the art from the following detailed description of the invention, taken together with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a prior art charge pump.

FIG. 2 is a circuit diagram of a prior art circuit that generates a clock signals for a charge pump, at elevated voltages.

FIG. 3 is a diagram of a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The numerous innovative teachings of the present invention will be described with particular reference to the presently preferred exemplary embodiments. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses and innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit the invention, as set forth in different aspects in the various claims appended hereto. Moreover, some statements may apply to some inventive aspects, but not to others.

FIG. 3 is diagram of a preferred embodiment of the present invention. In general, to solve the problems described above, a ring oscillator circuit 21 providing the CLK signal has its "ground," or, reference voltage regulated so that it is always a constant and operational voltage between the supply voltage and the actual circuit ground. In order to protect the circuitry of the charge pump, it is placed in a deep N-well ring ("DNWELL") 19 over an N-type buried layer ("NBL"), using known fabrication techniques, resulting in an isolated charge pump circuit 10'. By providing a ring oscillator with floating ground and isolated charge pump circuit, the circuit area required is significantly reduced as compared with prior art solution described above, since no high voltage components are required, and no level shifters are required. In addition, there is significantly reduced current consumption, as compared with prior art solutions. Further, from a product design standpoint, less risk is involved with implementations of the present invention, since the circuit is simpler, compared with prior art solutions achieving the same or similar result.

Specifically, the circuit of FIG. 3 includes the isolated charge pump circuit 10', an oscillator stage with floating ground 20, a high voltage ground reference stage 30, and a bias generator stage 40. The bias generator stage 40 uses FETs 41 and 42 to establish a voltage reference with respect to  $V_{CC}$  ( $V_{CC}$  being, for example, 5 volts), and then uses that voltage to establish a reference current through FET 43, which is mirrored using a current mirror constructed of FETs 44 and 45, to generate a current bias,  $I_{bias}$ .

The high voltage ground reference stage 30 comprises a block of circuitry 31 that takes an integrated circuit high voltage source  $V_H$ , and generates a floating ground on node 22, which is provided to ring oscillator circuit 21 and to inverter 12'. The high voltage  $V_H$  is typically a readily available high voltage supply, for example a car battery voltage of approximately 12-14 volts, for applications intended for use in an automobile. Another example is in applications intended for use in a printer. Printers typically transform and regulate a 30 volt supply to control the motors that move the print heads. Other supply sources exist, depending on the application. In any event,  $V_H$  is higher than normal supply voltage.

Preferably, circuit 31 is an operational amplifier configured as a voltage regulator, that outputs a voltage that stays

within a range of the supply voltage, for example 5 volts. It will be appreciated that the invention is not limited to the use of circuitry 31, but that any circuit that provides a node, such as node 22, that has a constant and operational voltage between  $V_H$  and ground may be used to provide this function.

The oscillator circuit that is used in oscillator stage 20 is a conventional ring oscillator 21. It will be appreciated that the invention is not limited to the use of ring oscillator 21, but that any circuit that generates a suitable clock signal may be used to provide this function. Preferably, however, the ring oscillator 21 is constructed of PMOS type FET devices such that they are self-isolating. That is, in a p-type substrate technology they are designed to reside in an n-type tank that, in turn, resides in a p-epi layer. The purpose of the ground connection to the ring oscillator 21 is to provide the substrate connection of the PMOS devices in such an implementation. The use of  $V_H$  and the floating ground voltage on node 22 result in a CLK signal that changes essentially between those two voltages.

Inverter 12' is essentially the same construction as prior art inverter 12, but it has the floating ground connection 22 for its ground connections. It takes the high voltage CLK signal as an input and provides the inverse  $\overline{\text{CLK}}$  signal as an output, again changing between  $V_H$  and the floating ground voltage on node 22.

Now, the high voltage ground reference circuitry 31 preferably has high gain, in order to sink the switching current of the ring oscillator circuit 21 and still maintain solid regulation. Therefore, as a practical matter, node 22 will have some ripple on it. Capacitor C7 is provided to filter that ripple. In the preferred embodiment, capacitor C7 is provided between  $V_H$  and node 22, rather than, for example, between node 22 and ground. This is because as so connected, capacitor C7 forms a high frequency bypass for the oscillator supply. This supply is comprised of the  $V_H$  rail and the virtual reference ground node 22. In addition, the voltage between  $V_H$  and node 22 is a regulated low voltage, and as such it allows a higher density capacitor to be placed there, as compared with a connection between node 22 and ground. Finally, any supply transients coupled to  $V_H$  will be transferred to node 22 by way of capacitor C7, so that the transient appears as a common-mode signal. Hence, the differential supply voltage across the oscillator will remain constant, reducing the likelihood of damage to that component. If capacitor C7 is connected between node 22 and ground it would actually increase the likelihood that damage would occur due to transients induced on  $V_H$ .

In this way, ring oscillator circuit 21 and inverter 12' operate between the floating ground on line 22 and the high voltage reference  $V_H$ . Thus, the CLK signal and its inverse  $\overline{\text{CLK}}$  are provided to the isolated charge pump circuit 10' at a higher voltage, allowing a higher  $V_{OUT}$ , while by the DNWELL/NBL isolation, the low voltage components in isolated charge pump circuit 10' are protected against breakdown.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A high voltage integrated circuit operable in a system having a low voltage reference, a high voltage reference, and a ground, for providing an output voltage higher than the high voltage reference, comprising:

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- a bias current generator stage coupled to receive the low voltage reference to generate a bias current;
- a high voltage ground reference circuit coupled to receive the bias current, the low voltage reference, the high voltage reference and ground, the high voltage ground reference circuit operable to provide a high voltage ground reference node;
- an oscillator, operable to provide a clock signal, the oscillator being connected to the high voltage reference and to the high voltage ground reference node; and
- an isolated charge pump circuit coupled to receive the clock signal, the high voltage reference and an inverted clock signal, the isolated charge pump circuit operable to generate the output voltage.
2. A high voltage integrated circuit as in claim 1, wherein the high voltage ground reference circuit comprises an operational amplifier.
3. A high voltage integrated circuit as in claim 1, wherein the oscillator comprises a ring oscillator including PMOS FET devices in an n-type tank residing in a p-epi layer.
4. A high voltage integrated circuit as in claim 1, wherein the bias current generator stage, comprises:
- a first transistor, having a gate node, a source node and a drain node, the source node coupled to receive the low voltage reference;
- a second transistor, having a gate node, a source node and a drain node, the gate node coupled to the gate node of the first transistor, the drain node coupled to the drain node of the first transistor, the source node coupled to the ground;
- a third transistor, having a gate node, a source node and a drain node, the gate node coupled to the gate node of the first transistor, the source node coupled to the ground; and
- a current mirror coupled between the drain node of the third transistor and the low voltage reference.

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5. A high voltage integrated circuit as in claim 1, wherein the oscillator, comprises:
- a ring oscillator coupled to receive the high ground voltage reference, ground, and the high voltage reference to provide a clock signal;
- a capacitor coupled across the high voltage reference and the high ground voltage reference; and
- an inverter coupled to the ring oscillator to provide an inverted clock signal, wherein the inverter having a first and second control input coupled to receive the high ground voltage reference and the high voltage reference.
6. A high voltage integrated circuit as in claim 1, wherein the isolated charge pump circuit, comprises:
- at least one stage that comprises,
- a first transistor, having a control node, a drain node and a source node, the source node coupled to receive the high voltage reference,
- a second transistor, having a control node, a drain node and a source node, the control node of the first transistor coupled to the control node of the second transistor, the drain node of the first transistor coupled to the drain node of the second transistor,
- a third transistor, having a control node, a drain node and a source node, the source node coupled to receive the high voltage reference, the drain node coupled to the control node of the first transistor, the drain node of the first transistor coupled to the control node of the third transistor, and
- a fourth transistor, having a control node, a drain node and a source node, the control node of the third transistor coupled to the control node of the fourth transistor, the drain node of the third transistor coupled to the drain node of the fourth transistor,
- a first capacitor coupled between the drain node of the first transistor and the inverted clock signal node,
- a second capacitor coupled between the drain node of the third transistor and the clock signal node
- wherein each of the at least one stages couples to one preceding stage.

\* \* \* \* \*





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**Hausmann et al.**

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(45) Date of Patent: **Dec. 21, 2004**

(54) **SIGNAL GENERATOR FOR CHARGE PUMP  
IN AN INTEGRATED CIRCUIT**

5,999,009 A \* 12/1999 Mitsui ..... 324/765

\* cited by examiner

(75) Inventors: **Michael Hausmann, Unterhaching  
(DE); Joachim Schnabel, Munich (DE)**

*Primary Examiner*—Linh My Nguyen

(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(73) Assignee: **Infineon Technologies AG, Munich  
(DE)**

(57) **ABSTRACT**

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

The invention relates to a signal generating device (10) for a charge pump for an integrated circuit, comprising:

N signal outputs  $D_1, \dots, D_N$  and a signal setting input (12) for setting a frequency f, in which case the signal generating device (10) is designed in such a way that a periodic signal  $S_x(t)$  can be output via the signal output  $D_x$ , all the signals  $S_1(t), \dots, S_N(t)$  have the same settable frequency f, in which case the following holds true for the signal  $S_x(t)$ , where  $2 \leq x \leq N$ ,

$$S_x(t) = S_1(t - (x-1) \Delta T_x - k_x / (2f)),$$

in which case

$\Delta T_x$  is the delay duration of the signal  $S_x(t)$  with respect to  $S_{x-1}(t)$ , and

$$k_x \in \{0; 1\},$$

the delay duration  $\Delta T_x$  is dependent on the frequency f.

Furthermore, the invention relates to an integrated circuit.

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(51) Int. Cl.<sup>7</sup> ..... **H03H 11/26**

(52) U.S. Cl. .... **327/261; 331/57**

(58) Field of Search ..... **327/261, 269,  
327/270, 276; 331/57, 108 C, DIG. 3; 365/222**

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,689,213 A \* 11/1997 Sher ..... 331/57

**12 Claims, 4 Drawing Sheets**

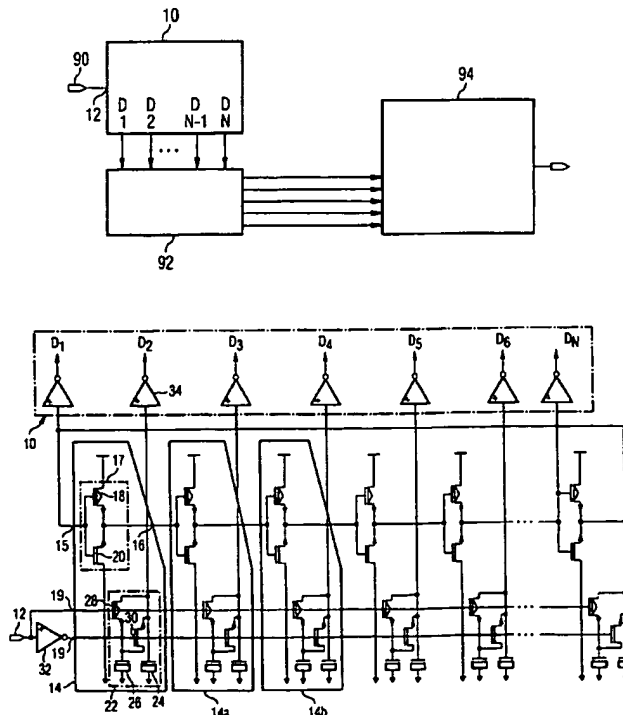


FIG 1

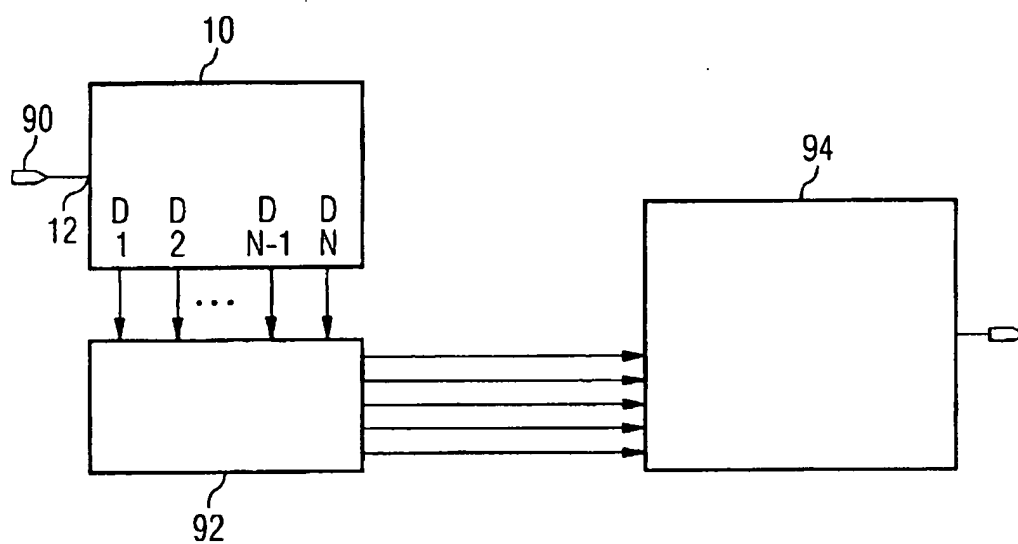


FIG 2

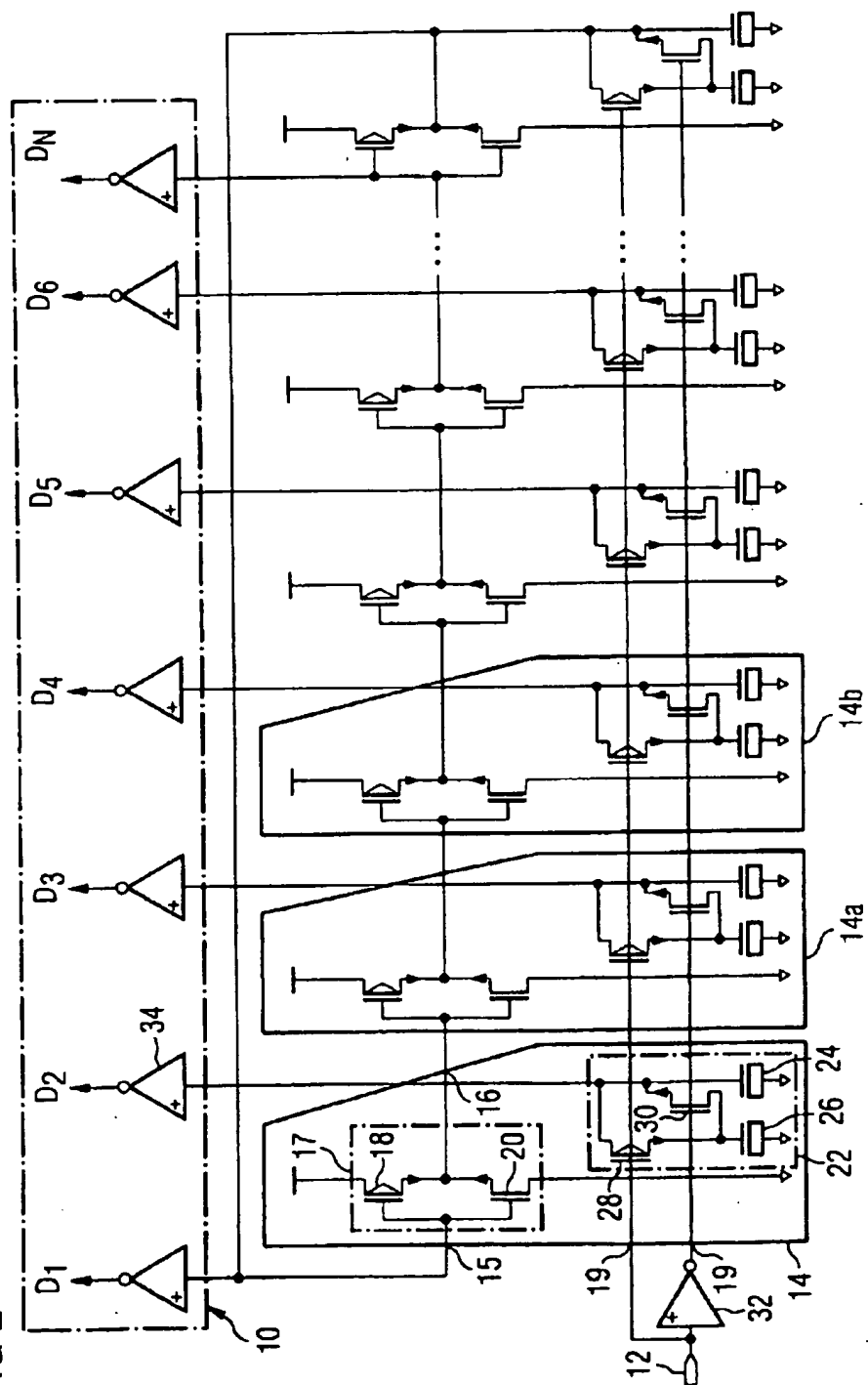


FIG 3

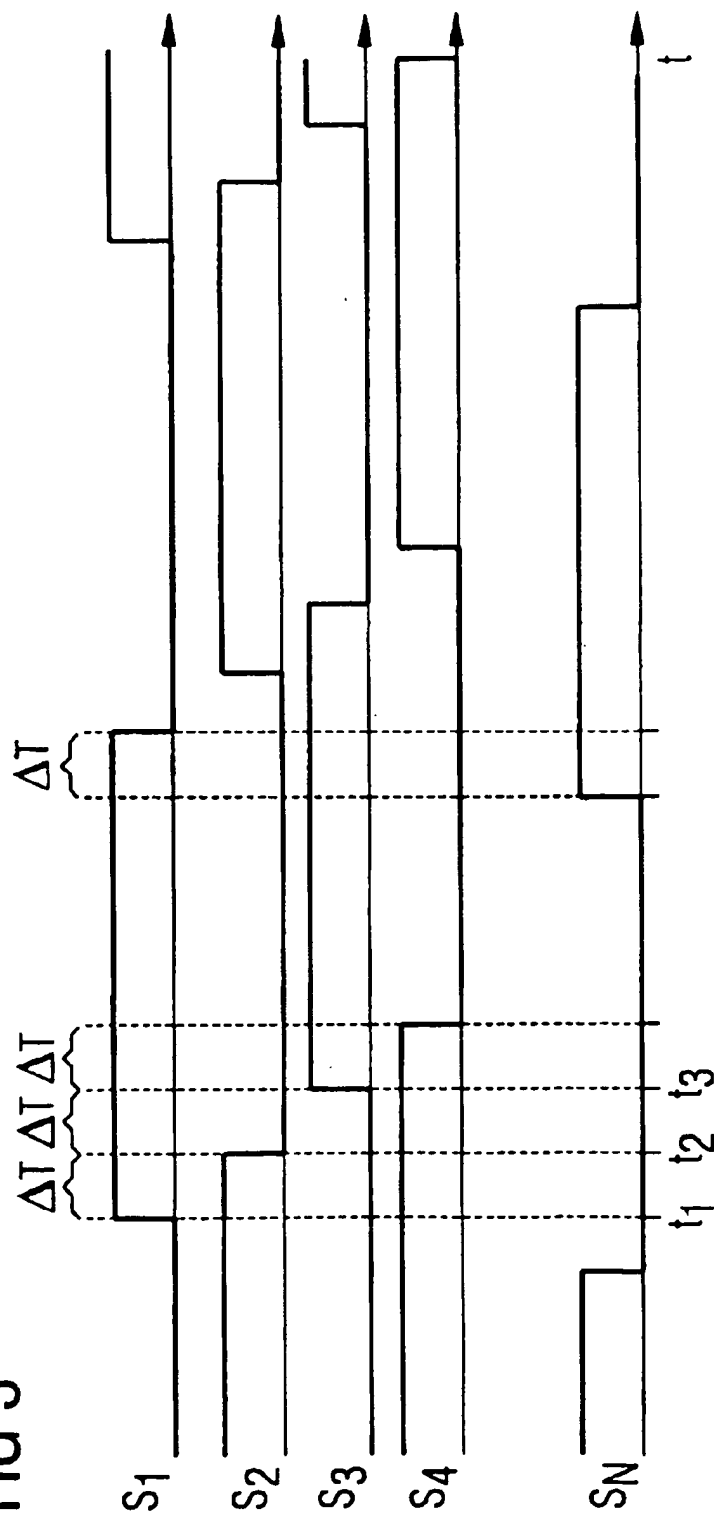
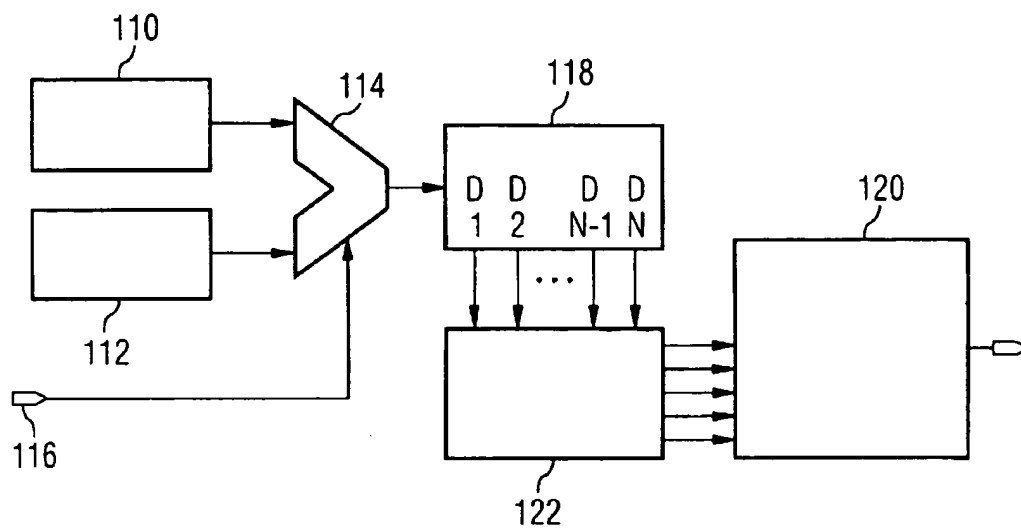


FIG 4 Prior art



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## SIGNAL GENERATOR FOR CHARGE PUMP IN AN INTEGRATED CIRCUIT

### RELATED APPLICATIONS

This application claims the benefit of the April 30, 2002 filing date of German application DE 102.19.371.1, the contents of which are herein incorporated by reference.

### FIELD OF INVENTION

The present invention relates to a signal generating device for a charge pump for an integrated circuit and to an integrated circuit which comprises such a signal generating device.

### BACKGROUND

In order, in an integrated circuit and, in particular, a semiconductor memory device or DRAM, to generate voltages which, in respect of magnitude, are higher than the supply voltage or are negative, so-called charge pumps are integrated. Charge pumps make it possible to generate multiples and sums of internal voltages. For this purpose, it is necessary to connect the charge pumps to ring oscillators which provide corresponding frequencies from which are derived control signals which are co-ordinated precisely with respect to time. In certain ranges, the maximum possible output current of the charge pumps is proportional to the oscillator frequency. This means that, in standby operation, i.e. with only a low current requirement, it becomes possible, for power loss reasons, to operate the pumps with lower frequencies than in the active operating mode, in which there is a higher current requirement.

Oscillator devices or arrangements which can generate the required control signals for a charge pump are known.

Such an oscillator arrangement according to the prior art is shown in FIG. 4. A signal with a first frequency  $f_1$  is generated in a first ring oscillator 110. A second signal with a frequency  $f_2$  is generated in a second ring oscillator 112. In this case, the frequency  $f_2$  is different from the frequency  $f_1$ . The two signals generated are fed to a multiplexer 114, by means of which a selection device 116 can select which of the two signals is output by the multiplexer 114.

The signal output by the multiplexer is fed to a delay chain 118, which generates the control signals for a charge pump 120.

In the delay chain 118, the signal received from the multiplexer 114 is delayed by a predetermined delay duration. The delayed signal is in turn delayed by the predetermined delay duration. This process is repeated until the required number of control signals has been obtained. The signals thus obtained are output to a control signal generating unit 122, which generates control signals for the charge pump 120.

This oscillator arrangement of the prior art has the disadvantage, however, that the control signals are inadequately adapted for the charge pump, which leads to an impairment of the efficiency.

### SUMMARY

Consequently, it is an object of the present invention to provide a signal generating device for a charge pump for an integrated circuit and an integrated circuit which enable an improved efficiency during the operation of the charge pump.

The invention provides a signal generating device for a charge pump for an integrated circuit, in which case the

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signal generating device has  $N$  signal outputs  $D_1, \dots, D_N$  and a signal setting input for setting a frequency  $f$  and is designed in such a way that

a periodic signal  $S_x(t)$  can be output via the signal output  $D_x$ ,

all the signals  $S_1(t), \dots, S_N(t)$  have the same settable frequency  $f$ , in which case

the following holds true for the signal  $S_x(t)$ , where  $2 \leq x \leq N$ ,

$$S_x(t) = S_1(t - (x-1) \Delta T_x - k_x / (2f)),$$

in which case

$\Delta T_x$  is the delay duration of the signal  $S_x(t)$  with respect to  $S_{x-1}(t)$ , and

$$k_x \in \{0; 1\},$$

the delay duration  $\Delta T_x$  is dependent on the frequency  $f$ .

The frequency  $f$  is preferably the inverse of the period duration of the periodic signal  $S_x(t)$ . Furthermore, the signal generating device is preferably designed in such a way that all the signals  $S_x(t)$  for  $2 \leq x \leq N$  satisfy the equation specified above. The delay duration  $\Delta T_x$  is preferably inversely proportional to the frequency  $f$ . In particular, it is preferred for the delay duration  $\Delta T_x$  to increase, the lower the frequency  $f$  is.

By virtue of the fact that the delay duration  $\Delta T_x$  is dependent on the frequency  $f$ , it is possible to ensure that the control signals for the charge pump are in an optimal temporal relationship with one another and the charge pump can thus be operated in an advantageous state for all frequencies.

The signals  $S_x(t)$  output all have the same frequency  $f$ . Consequently, the temporal sequence of the pulse signals output is the same; in particular, the edges of the signals are spaced apart from one another by the same delay time. However, in a preferred embodiment, it may be provided that the amplitude and/or an offset or a shift of one or more signals is provided.

Preferably,  $k_x = (1 + (-1)^x) / 2$ . Consequently, in each case successive signals are inverted with respect to one another.

The delay duration  $\Delta T_x$  is preferably essentially identical, to be precise equal to  $\Delta T_1$ , for all the signals  $S_2(t), \dots, S_N(t)$ .

In a preferred embodiment, the signal generating device comprises a multiplicity of oscillator stages connected in ring form, in which case

the oscillator stages each have an oscillator stage input and an oscillator stage output;

in which case the oscillator stage output is respectively signal-connected to the oscillator stage input of the downstream oscillator stage; and

the signal outputs  $D_1, \dots, D_N$  are signal-connected to a respective oscillator stage output of the oscillator stages.

Each oscillator stage preferably has a setting input which is signal-connected to the signal setting input.

By tapping off the signals  $S_1, \dots, S_N$  directly at the oscillator stage outputs, it is possible to obtain the delayed signals directly from the ring oscillator which is used for generating the signal. Consequently, the delay chain which was provided in the prior art can be dispensed with. Furthermore, the multiplexer can likewise be dispensed with since the frequency of the signal generating device according to the invention is variable, and, consequently, only one ring oscillator is required.

Preferably, the oscillator stages each comprise a settable delay element for setting a delay element duration  $\tau_{VG}$ .

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The delay element duration  $\tau_{VG}$  forms part of the delay duration  $\Delta T$ .

Preferably, the settable delay element is of capacitive design. It is further preferred that the delay element can be set by means of a setting signal which can be input via the signal setting input.

Preferably, the settable delay element is formed by at least one capacitor, one of whose electrodes is electrically connected to the oscillator stage output and whose other electrode is electrically connected to a fixed potential. The fixed potential is preferably  $V_{SS}$ , i.e. the potential on the integrated circuit which is provided for "earthing". It is further preferred that the settable delay element may comprise a further capacitor, which can be connected in parallel with the first capacitor by means of the setting signal. The delay element duration  $\tau_{VG}$  can be influenced by the size of the capacitance of the delay element.

It is further preferred that the oscillator stages each comprise an inverting element.

The signal generating device preferably comprises  $N$  oscillator stages.

In a preferred embodiment, the following holds true for the delay duration  $\Delta T = 1/(2 \cdot N \cdot f)$ , and the following preferably holds true for the signal  $S_1(t) = S_N(t - \Delta T) - k_1/(2f)$ , where  $k_1 \in \{0, 1\}$ . Preferably,  $k_1 = 1$ .

It is thus particularly preferred that the first signal  $S_1$  again follows the last signal  $S_N$  and the same delay duration is provided between all the signals.

The invention furthermore provides an integrated circuit which comprises a signal generating device according to the present invention or a preferred embodiment thereof.

#### BRIEF DESCRIPTION OF THE DRAWING

Further objects, features and advantages of the present invention will become apparent from a detailed description of a preferred embodiment of the present invention with reference to the drawings, in which:

FIG. 1 shows a schematic view of an arrangement of a charge pump and a signal generating device in accordance with a preferred embodiment of the present invention;

FIG. 2 shows a circuit diagram of a signal generating device in accordance with a preferred embodiment of the present invention;

FIG. 3 shows a timing diagram showing signals which have been generated by a signal generating device in accordance with a preferred embodiment of the present invention; and

FIG. 4 shows an oscillator arrangement of the prior art.

#### DETAILED DESCRIPTION

FIG. 1 shows a schematic view of a charge pump and a signal generating device in accordance with a preferred embodiment of the invention. The signal generating device 10 according to the invention comprises  $N$  signal outputs  $D_1, \dots, D_N$ . Furthermore, the signal generating device 10 comprises a signal setting input 12 for setting a frequency  $f$  of the signals to be generated. The frequency  $f$  may preferably be selected or set by means of a selection device 90, which is provided in the integrated circuit and is signal-connected to the signal setting input 12. As an alternative, the operating mode may be selected by the signal setting input 12. By way of example, a standby mode and a normal mode may be provided. This case is provided in the preferred embodiment of the present invention which is described below.

The outputs  $D_1$  to  $D_N$  of the signal generating device 10 are preferably connected to a control signal generating unit

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92. From the signals output by the signal generating device 10, the control signal generating unit 92 generates signals which are related temporally to one another such that they have an optimum arrangement of the operation of the charge pump 94.

FIG. 2 shows a circuit diagram of a signal generating device in accordance with a preferred embodiment of the present invention.

The signal generating device in accordance with a preferred embodiment of the present invention comprises a ring oscillator comprising a multiplicity of oscillator stages 14, 14a, 14b, . . . . An odd number of oscillator stages is preferably provided. The oscillator stages 14, 14a, 14b, . . . shown in the embodiment illustrated are preferably all identical. Therefore, only the oscillator stage 14 is described in detail in the description below.

The oscillator stage 14 has an oscillator stage input 15 and an oscillator stage output 16. The oscillator stage output 16 of the oscillator stage 14 is connected to the oscillator stage input 15 of the next oscillator stage; this is the oscillator stage 14a in the embodiment illustrated in FIG. 2. The oscillator stage output 16 of the last oscillator stage 14 (oscillator stage 14 on the far right in FIG. 2) is connected to the oscillator stage input 15 of the first oscillator stage 14 (oscillator stage 14 on the far left in FIG. 2). Furthermore, the oscillator stage 14 has a setting input 19, which is signal-connected to the signal setting input 12.

The oscillator stage 14 comprises an inverting element or an inverter 17, which comprises a p-channel field-effect transistor 18 and an n-channel field-effect transistor 20. During operation, the inverter 17 requires a certain time duration until it has switched. This is the inverter delay duration  $\tau_{inv}$ .

Furthermore, the oscillator stage 14 comprises a settable delay element 22 with a settable delay element duration  $\tau_{VG}$ . In accordance with the preferred embodiment of the present invention, the delay element 22 comprises a first capacitor 24, whose first electrode is electrically connected to the oscillator stage output 16 and whose second electrode is electrically connected to a fixed potential, preferably  $V_{SS}$ , i.e. the potential on the integrated circuit which is provided for earthing. Furthermore, a second capacitor 26 is provided, whose first electrode is electrically connected to the first electrode of the first capacitor 24 via a p-channel field-effect transistor 28 and an n-channel field-effect transistor 30. The field-effect transistors 28 and 30 can be driven via the signal setting input in such a way that the second capacitor 26 can be connected in parallel with the first capacitor 24. For this purpose, an inverter 32 is furthermore provided. The second electrode of the second capacitor 26 is likewise connected to a fixed potential, preferably the same as the second electrode of the first capacitor. It is furthermore conceivable to design the delay element 22 in any other way as long as the delay element duration  $\tau_{VG}$  can be set.

The total delay duration  $\Delta T$  of the oscillator stage 14 results from the sum of the inverter delay duration  $\tau_{inv}$  and the delay element duration  $\tau_{VG}$  as  $\Delta T = \tau_{VG} + \tau_{inv}$ . In accordance with the present embodiment, the delay duration  $\Delta T$  of the oscillator stage 14 is identical for all the oscillator stages 14, 14a, 14b, . . . for a specific frequency  $f$ . Preferably,  $\Delta T = 1/(2 \cdot N \cdot f)$ . However, it may also be provided that the delay duration  $\Delta T$  is different in different oscillator stages for the same frequency  $f$ .

A signal output  $D_x$  is connected to the oscillator stage output 16 via an inverter 34. As an alternative to the inverter, it is possible to provide a threshold value detector which

switches at a predeterminable threshold value, without inverting the incoming signal. However, each oscillator stage output 16 need not necessarily be connected to a signal output  $D_x$ .

The operation of the signal generating device according to the invention in accordance with a preferred embodiment of the invention is described below with reference to FIGS. 2 and 3. It is assumed here that the ring oscillator is in the steady-state condition, i.e. that a high or low signal is alternately present in each case at the oscillator stage outputs.

A signal generation cycle is described by way of example below. Firstly, it is assumed that a high signal is present at the oscillator stage input 15 of the first oscillator stage 14 and, consequently, as shown in FIG. 3, the signal  $S_1$ , which is a low signal, is present at the signal output  $D_1$ . A low signal is then fed to the oscillator stage input 15 of the oscillator stage 14 from the oscillator output of the last oscillator stage of the ring at the instant  $t_1$ . As a result, the p-channel field-effect transistor 18 is turned on and the n-channel field-effect transistor 20 is turned off. A low signal is still present at the oscillator stage output 16 at this point in time. The capacitor 24 then starts to be charged. The time duration required for the charging state of the capacitor to exceed a predetermined threshold value is the delay element duration  $\tau_{VG}$ .

If the charging state of the capacitor 24 has exceeded a predetermined threshold value, the inverter 34 outputs a signal  $S_2$  with an opposite polarity, i.e. a low signal. This is the instant  $t_2$  in FIG. 3. The high signal of the oscillator stage output 16 of the oscillator stage 14 is then also present at the oscillator stage input 17 of the next oscillator stage 14a. Here, the n-channel field-effect transistor 20 is then turned on and the p-channel field-effect transistor 18 is turned off, so that the charged capacitor 24 of the oscillator stage 14a starts to discharge. After the charging state of the capacitor 24 has fallen below a predetermined threshold value, the inverter 34 of the signal output  $D_3$  switches and a high signal is output as signal  $S_3$ . This is the instant  $t_3$  in FIG. 3.

This process is carried out until the end of the oscillator stage chain shown in FIG. 3. At the end of the oscillator stage chain, a signal is output which is opposite to the signal present at the input of the oscillator stage chain. Consequently, the above process is initiated anew.

A signal  $S_x(t)$  where  $2 \leq x \leq N$  can thus be expressed as a function of the signal  $S_1$  as follows:

$$S_x(t) = S_1(t - (x-1) \cdot \Delta T_x - k_x / (2f)),$$

in which case

$\Delta T_x$  is the delay duration of the signal  $S_x(t)$  with respect to  $S_{x-1}(t)$ , and

$k_x \in \{0; 1\}$ .

In the preferred embodiment of the present invention,  $T_x = \Delta T = 1/(2 \cdot N \cdot f)$  and  $k_x = (1 + (-1)^x)/2$ . Consequently,  $k_x$  alternately becomes 0 and 1 and two successive signals  $S_x(t)$  output are inverted with respect to one another, as shown in FIG. 3. However, it is likewise conceivable to choose  $k_x$  in such a way that the signals  $S_x$  output are not inverted with respect to one another or only respectively selected signals  $S_x$  are inverted. The signal  $S_1(t)$  may furthermore be expressed as a function of the signal  $S_N$  as follows:  $S_1(t) = S_N(t - \Delta T - k_1 / (2f))$ , where  $k_1 \in \{0; 1\}$ . Preferably,  $k_1 = 1$ , so that the signal  $S_1(t)$  is shifted by  $\Delta T$  with regard to the signal  $S_N(t)$  and is inverted with respect to the latter.

The period duration of the signals output is equal to the time required to run through the ring twice, i.e. to generate a high signal and a low signal for a signal  $S_x$ .

The frequency  $f$  can be varied by varying the duration of the charging process and/or discharging process of the capacitor of the delay element 22. For this purpose, the second capacitor 26 can be connected in parallel with the first capacitor 24. In this case, a low signal is fed via the signal setting input 12. The p-channel field-effect transistor 28 is thus turned on. Furthermore, a high signal output by the inverter 32 is present at the n-channel field-effect transistor 26, so that the latter is likewise turned on. This results in a parallel circuit of the capacitors 24 and 26.

The resulting capacitance is the sum of the capacitances of the two capacitors 24, 26. The time required to charge this resulting capacitance, and hence the delay time  $\tau_{VG}$ , is greater than the charging time with only one capacitor. As a consequence, the time required to run through all the oscillator stages of the ring oscillator once is longer, and thus so is the period duration  $1/f$  of the signals output.

#### List of Reference Symbols

10	Signal generating device
12	Signal setting input
14	Oscillator stages
15	Oscillator stage input
16	Oscillator stage output
17	Inverter
18	p-Channel field-effect transistor
19	Setting input
20	n-Channel field-effect transistor
22	Delay element
24	First capacitor
26	Second capacitor
28	p-Channel field-effect transistor
30	n-Channel field-effect transistor
32	Inverter
34	Inverter
90	Selection device
92	Control signal generating unit
94	Charge pump
110	Ring oscillator
112	Ring oscillator
114	Multiplexer
116	Selection device
118	Delay chain
120	Charge pump
122	Control signal generating unit
$D_1, \dots, D_N$	Signal outputs

What is claimed is:

1. A signal generating device for a charge pump for an integrated circuit, the signal generating device having  $N$  signal outputs  $D_1, \dots, D_N$  and a signal setting input for setting a frequency  $f$  such that:

a periodic signal  $S_x(t)$  can be output via the signal output  $D_x$ ;

all the signals  $S_1(t), \dots, S_N(t)$  have the same settable frequency  $f$ ; and

for  $x$  within an interval  $2 \leq x \leq N$ ,

$$S_x(t) = S_1(t - (x-1) \cdot \Delta T_x - k_x / (2f))$$

wherein  $\Delta T_x$  is a frequency-dependent delay duration of the signal  $S_x(t)$  with respect to  $S_{x-1}(t)$ , and  $k_x \in \{0; 1\}$ .

2. The signal generating device according to claim 1, wherein  $k_x = (1 + (-1)^x)/2$ .

3. The signal generating device according to claim 1, wherein the delay duration  $\Delta T_x$  is equal to  $\Delta T$  for all the signals  $S_2(t), \dots, S_N(t)$ .

4. The signal generating device according to claim 1, further comprising a multiplicity of oscillator stages connected in a ring, the oscillator stages each having an oscillator stage input and an oscillator stage output;



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each oscillator stage output being respectively signal-connected to an oscillator stage input of a downstream oscillator stage; and

the signal outputs  $D_1, \dots, D_N$  being signal-connected to a respective oscillator stage output of the oscillator stages.

5. The signal generating device according to claim 4, wherein the oscillator stages each comprise a settable delay element for setting a delay element duration  $\tau_{VG}$ .

6. The signal generating device according to claim 5, wherein the settable delay element is of capacitive design.

7. The signal generating device according to claim 5, wherein the delay element is set by a setting signal that is input via the signal setting input.

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8. The signal generating device according to claim 4, wherein the oscillator stages each comprise an inverting element.

9. The signal generating device according to claim 4, wherein the number of oscillator stages is equal to the number of signal outputs.

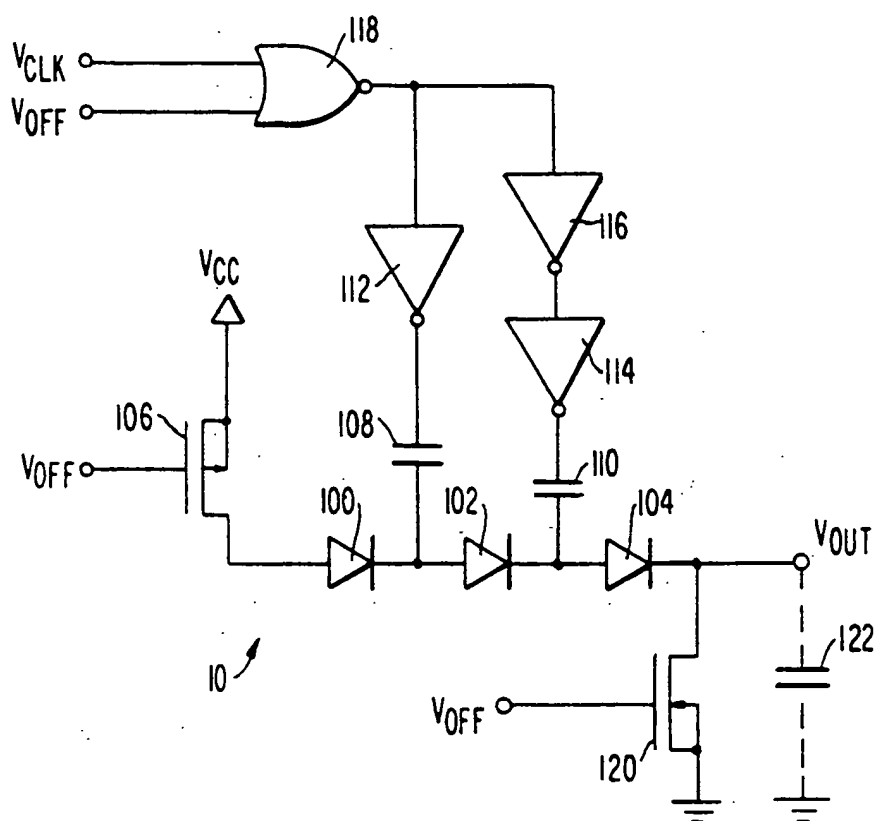
10. The signal generating device according to claim 3, wherein the delay duration  $\Delta T$  is given by  $\Delta T = 1/(2 \cdot N \cdot f)$ .

11. The signal generating device according to claim 10, wherein the signal  $S_1(t)$  is given by  $S_1(t) = S_N(t - \Delta t - k_1/(2f))$ , where  $k_1 \in \{0; 1\}$ .

12. An integrated circuit comprising a signal generating device according to claim 1.

\* \* \* \* \*





**FIG. 1**  
**PRIOR ART**

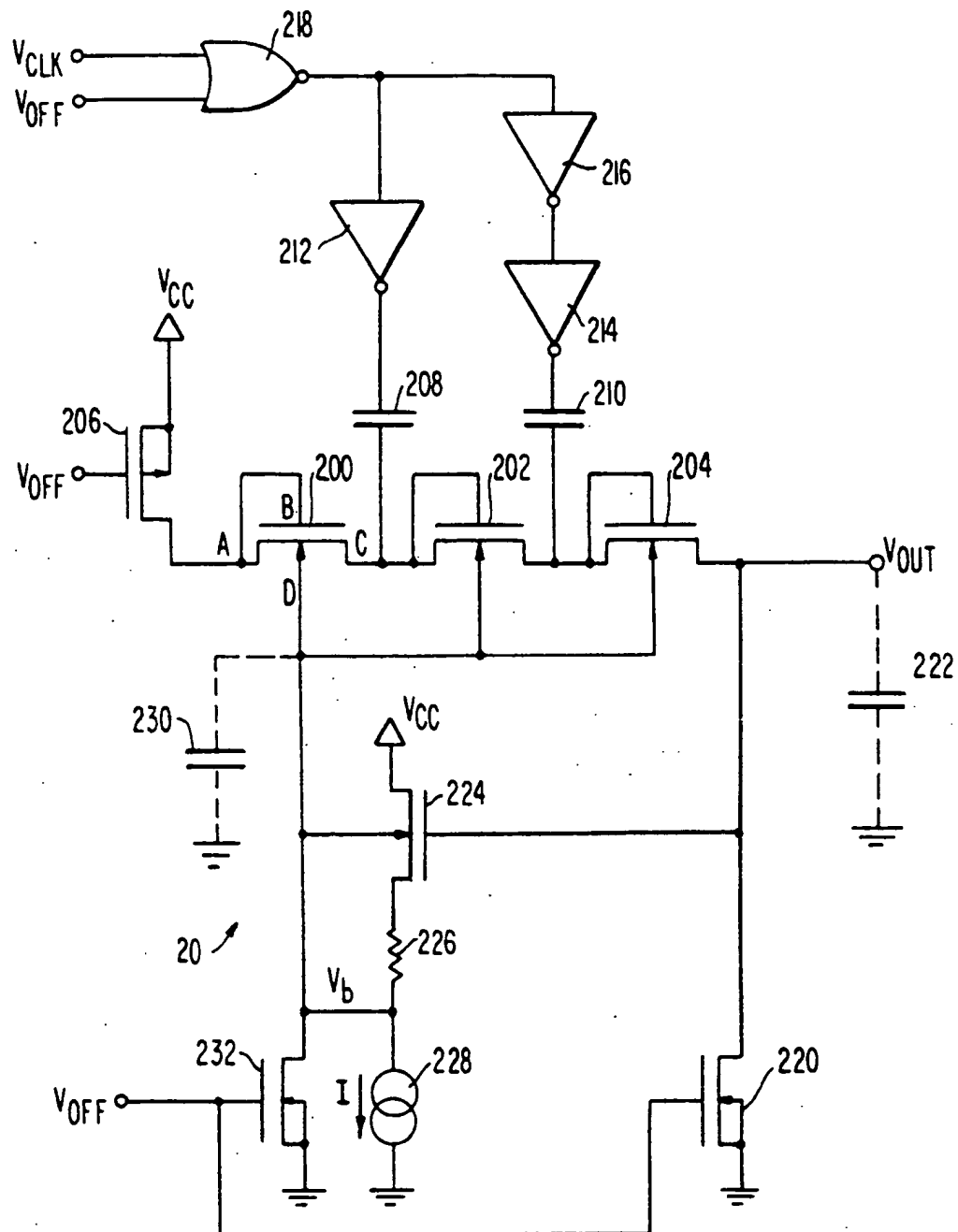


FIG. 2

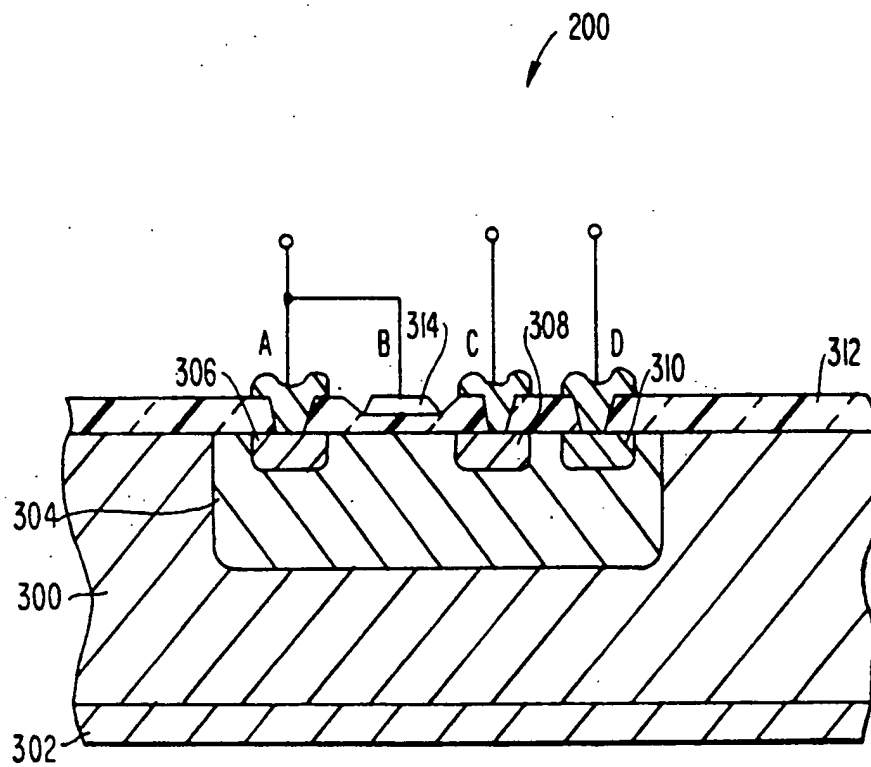


FIG. 3

# INTEGRATED CHARGE PUMP CIRCUIT WITH BACK BIAS VOLTAGE REDUCTION

## BACKGROUND OF THE INVENTION

The invention relates generally to voltage multiplier circuits, and relates more specifically to an integrated charge pump circuit with back bias voltage reduction.

Conventional charge pump circuits, such as those shown, for example, in FIG. 1 of this application or in FIG. 1 of U.S. Pat. No. 4,439,692, typically employ a plurality of series-connected diodes having an input terminal, an output terminal and one or more intermediate terminals, with each intermediate terminal being fed by a capacitively-coupled driver. Since the purpose of this circuit is to provide a voltage multiplication, the series-connected diodes in the charge-pump circuit must withstand voltages which exceed the normal power supply voltage range. When a charge pump circuit is required in MOS devices fabricated using standard MOS process technology, it becomes difficult to isolate the relatively high-voltage p-n junctions of these diodes, and additional process steps are usually necessary.

One possible solution to this problem, as shown in U.S. Pat. No. 4,439,692, is to use MOS-configured diodes (MOS transistors connected as diodes) for the conventional diodes of the prior art charge pump circuit. However, because these MOS-configured diodes typically have a larger diode drop (several volts as compared with the 0.7 volt of a conventional p-n junction), the voltage-multiplying capability of the charge pump is substantially degraded. In other words, to achieve a given output voltage level from the charge pump, the number of cascaded stages in an all-MOS charge pump would be greater than the number of stages in the conventional p-n junction diode circuit. This results in a slower, more complex circuit which occupies additional silicon area. Thus, using prior-art technology, there are substantial drawbacks connected with the otherwise-desirable use of MOS technology in fabricating charge pump circuits.

There are two basic reasons for the relatively large diode drops in MOS-configured diodes. First, in MOS process technology, it is conventional to use a threshold-implant step to force the threshold voltage to between about 1 and 2 volts. Thus, for example, in U.S. Pat. No. 4,439,692, all of the transistors in the charge pump circuit 18 in FIG. 3 are designated as "H" (hard) transistors. In this context, a "hard" transistor is deemed to be one which has a substantially larger positive or negative threshold voltage than that of a so-called "soft" transistor. Thus, as shown in FIG. 4 of U.S. Pat. No. 4,439,692, so-called "hard" transistors may have a threshold voltage of about +1 volt for enhancement mode FET's and a threshold voltage of about -3 volts for depletion-mode FET's. In no case will these "hard" transistors have a relatively low threshold voltage, as the "hard" transistors are by definition those which have a more negative or more positive threshold voltage value.

Secondly, the threshold voltage is further increased by a large body effect caused by large source-to-substrate voltages in integrated circuits employing MOS transistors in the charge pump circuit. This effect occurs because the sources of the MOS transistors cannot be tied to the P-well substrate in which the transistors (typically NMOS devices) are fabricated because the

sources must be allowed to rise above the supply voltage to permit the device to function as intended.

In order to create a relatively simple, efficient, fast and compact all-MOS charge pump circuit in an integrated circuit, these problem inherent in the prior-art structures must be overcome.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an integrated charge pump circuit which improves efficiency, speed, simplicity and compactness as compared to existing circuits.

In accordance with the invention, this object is achieved by a new integrated charge pump circuit having at least one diode type voltage-multiplier stage incorporating a diode-configured NMOS transistor fabricated in a P-type well which surrounds the NMOS transistor and forms its back gate. The improved physical and operational characteristics of the invention are achieved by making the NMOS transistor a relatively low-threshold transistor, and by using a bias circuit to generate a bias voltage which is less than the back bias voltage generated by the charge pump circuit. This bias circuit is advantageous in that it allows the P-type well to be biased at its highest possible potential without forward biasing any P-type well to bulk or P-type well to source junction. In this manner, the voltage difference between the source of the NMOS transistors and the P-type well can be minimized. This reduces the back bias voltage which further reduces the threshold of the NMOS transistors to result in a structure which offers performance in an all-MOS charge pump which approaches that of prior-art p-n junction diode circuits.

In a preferred embodiment of the invention, the threshold of the diode-configured transistors is selected to be relatively low (less than one voltage at zero back-body bias).

The bias circuit used to generate the bias voltage in the charge pump circuit may advantageously be composed of a further NMOS transistor connected as a source follower, with its gate being connected to an output terminal of the charge pump circuit and its source being coupled, through a resistor, to the P-type well in which the back gates of the diode-connected MOS transistors are formed. This configuration allows the P-well to always be biased one gate-to-source voltage plus one resistor drop below the output terminal voltage of the charge pump when the output is less than the supply voltage, and biased just one resistor drop below the supply voltage when the output is above the supply voltage. The value of the resistor drop can be selected to secure the desired output voltage value. This bias circuit serves to minimize the back bias when the charge pump is ON, and prevents forward conduction from the P-well to the bulk junction when the charge pump is OFF. The invention may be more completely understood with reference to the following detailed description, to be read in conjunction with the accompanying drawing.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows a schematic circuit diagram of a prior-art charge pump circuit;

FIG. 2 shows a schematic circuit diagram of an all-MOS charge pump circuit in accordance with the invention; and

FIG. 3 shows a simplified cross section of a semiconductor device that is used in the integrated charge pump circuit in accordance with the invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a conventional prior-art charge pump circuit 10 employing series-connected p-n junction diodes 100, 102 and 104. Power supply voltage  $V_{cc}$  is fed to the anode of diode 100 through switching transistor 106 and the output voltage of the charge pump is generated at the cathode of diode 104, as shown by the symbol  $V_{out}$ . The intermediate points in the diode string are connected to capacitors 108 and 110, which are in turn driven by inverters 112, 114 and 116, and NOR gate 118 having inputs  $V_{off}$  and  $V_{clk}$ . The circuit is turned ON and OFF by MOS transistors 106 and 120, which serve respectively to connect the anode of diode 100 to the power supply and disconnect the output terminal  $V_{out}$  when the circuit is OFF, with the switching being accomplished as a function of the signal  $V_{off}$  applied to the gates of transistors 106 and 120. The capacitance of the load connected to the terminal  $V_{out}$  is shown schematically by a capacitor 122 connected between the output terminal and ground by a dotted line.

The prior-art circuit of FIG. 1 operates in a conventional manner similar to that of charge pump 18 in FIG. 1 of U.S. Pat. No. 4,439,692, and accordingly will not be described in detail. Briefly, however, the circuit operates as follows.

$V_{clk}$  is a high frequency clock signal (about 1 MHz) that feeds the input of inverters 112 and 116.  $V_{off}$  is a control signal which, when high, disables the charge pump by blocking the  $V_{clk}$  signal and by discharging the load capacitor 122. When  $V_{off}$  is low, the  $V_{clk}$  signal is allowed to pass through gate 118; transistor 106 turns on, and 120 turns off. In this state, the charge pump is on: node  $V_{out}$  is first pulled to a value 3 diode drops below  $V_{cc}$ ; alternating pulses that drive capacitors 108 and 110 at the  $V_{clk}$  frequency effectively deliver charge packets that further drive up the voltage  $V_{out}$  across capacitor 122. The unidirectional connection of the diodes (100, 102, 104) forms a voltage multiplying circuit that forces charged to flow only in the direction of the output.

With this scheme, it can be shown that the achievable steady state value of  $V_{out}$  is

$$V_{out} = V_{cc} + 2V_p - 3V_d$$

where  $V_p$  is the output swing of inverting drivers 112 and 114, and  $V_d$  is the diode drop across diode 100, 102, or 104. Thus it can be seen that  $V_{out}$  is maximized if the diode drops are minimized.

In conventional charge pump circuits such as the one shown in FIG. 1, the node voltages at p-n junction diodes 100, 102 and 104 will exceed the supply voltage  $V_{cc}$ . When this type of circuit is implemented in an MOS structure, using standard MOS processed technology, it becomes difficult to isolate these high-voltage p-n junctions and additional process steps are usually required. One way to overcome these problems is to substitute MOS-configured diodes for the p-n junction diodes in the charge pump circuit, as shown for example in U.S. Pat. No. 4,439,692. However, because MOS transistors typically have larger diode drops (several volts as compared to 0.7 volts for a typical p-n junction), the voltage-multiplying capability of the charge pump circuit is substantially degraded. To achieve a

given output voltage from the charge pump, the number of cascaded stages would have to be increased when using MOS transistors instead of p-n junction diodes. This has a very adverse affect on the speed of operation of the circuit, and requires additional silicon area as well.

The main reason for this relatively large MOS diode drop, and the resulting degradation in performance, is that the source of the MOS devices in the charge pump cannot be tied to the P-well substrate because the source must be allowed to rise above the supply voltage during operation. This problem, present in prior-art MOS charge pump circuits such as those disclosed in U.S. Pat. No. 4,439,692, results in larger, slower and less efficient implementation of charge pump circuitry.

FIG. 2 shows an improved charge pump circuit 20 in accordance with the invention, in which the aforementioned problem is largely eliminated, thus resulting in a faster, smaller and thus more efficient all-MOS charge pump circuit implementation. It should be noted that while a two-stage charge pump circuit is shown in FIG. 2, charge pump circuits in accordance with the invention can also be fabricated with only one stage, or with more than two stages. Also, for clarity, components in FIG. 2 having counterparts in FIG. 1 are provided with reference numerals having the last two digits the same as those of the corresponding components in FIG. 1.

In FIG. 2, the basic charge-pump circuit with its capacitively-coupled drivers (shown in the top portion of the figure) is the same as that of FIG. 1, except that the p-n junction diodes 100, 102 and 104 have been replaced by diode-connected MOS transistors 200, 202 and 204, respectively. In accordance with the invention, and contrary to the teaching of the prior art, these transistors can advantageously be low threshold unimplanted NMOS transistors, with a threshold voltage of less than one volt. Such transistors can be easily fabricated without using additional masks, in a double-poly process, by forming the gates of the transistors with a poly-layer that is provided before the threshold implant, thereby effectively shielding the implant from the channel.

Additionally, a new bias circuit, shown in the lower portion of FIG. 2, provides a reduced back-bias voltage for the P-well in which the diode-connected MOS transistors 200, 202 and 204 are fabricated, when the charge pump is ON. Additionally, this bias circuit prevents forward conduction in the P-well to bulk junction when the charge pump is OFF. Physically, the back gate terminals of the diodes can be either the individual p-wells of the diodes, as shown in FIG. 3, electrically tied together, or they can be one common p-well surrounding all three diodes. By way of example, FIG. 3 shows a simplified cross-section of a representative diode-connected transistor, here transistor 200 of FIG. 2. In transistor 200, a substrate 300, here of n-type conductivity, is provided with a highly-doped n type contact layer 302 and a p type well 304. Drain and source regions 306 and 308 of n type conductivity are provided in the well 304, along with a p type back-gate contact 310. An insulating layer 312, typically of silicon dioxide, is provided over the top surface of the device, and is provided with apertures for contacting the drain, source and back gate contact. A gate electrode 314 is provided over a portion of the insulating layer 312 having reduced thickness, and the gate electrode is connected to drain region 306. For clarity, corresponding

terminals A, B, C and D of transistor 200 are shown in both FIG. 2 and FIG. 3. Alternatively, as noted above, all of the diode-connected transistors can be fabricated in a single p type well.

In the circuit of FIG. 2, the output voltage  $V_{out}$  is taken from the output region of the device and is provided to the gate of an additional MOS transistor 224 which is connected in a source follower configuration with its channel connected between the supply voltage  $V_{cc}$  and one end of a resistor 226. The other end of resistor 226 is connected to one terminal of a current source 228, the other terminal of which is connected to ground. The output of the bias circuit is taken at the junction between the resistor 226 and the current source 228, and the bias voltage developed at this point is designated as  $V_b$ . The bias voltage  $V_b$  is then applied to the back gates of transistors 200, 202, 204, and 224 within the P-well, with capacitor 230, shown in dotted lines in FIG. 2, representing the capacitance of the P-well. Finally, an additional transistor 232 is provided to discharge the bias voltage to ground when the charge pump is turned OFF, while the charge pump output voltage  $V_{out}$  is discharged to ground by transistor 220.

In each phase of operation, it is important that the p-well potential of the MOS diodes remain below the  $V_{cc}$  potential, and always be lower than the lowest source of drain node potential of these transistors, because otherwise parasitic p-n junctions can be activated that can result in destructive latch-up of the circuit. At the same time, it is important that the p-well potential be as high as possible in order to minimize the back body effect, and thus the threshold voltages, of these diodes. The bias circuit shown in FIG. 2 allows the p-well potential to be biased at least one gate-to-source voltage below the lowest source potential of the diodes when  $V_{out}$  is still below  $V_{cc}$  (during the transient charging phase of the output), and be biased at about  $V_{cc}$  when  $V_{out}$  is above  $V_{cc}$  (during steady state).

The bias voltages can be further reduced by adding an optional resistive drop via resistor 22 so that the amount of body effect, and thus the threshold voltage, of the MOS diode can be tailored to realize an exact value of the output at steady state.

The bias circuit receives a voltage  $V_{out}$  at the gate of source-follower transistor 224, and generates a bias voltage  $V_b$  which is roughly equal to  $V_{cc} - I_{228} \times R_{226}$ . Thus, the bias voltage can be precisely controlled in order to optimize the diode drops across the MOS-connected transistors 200, 202 and 204. When the charge pump is turned OFF, transistors 220 and 232 are activated by the voltage  $V_{off}$ , thereby discharging both  $V_{out}$  and  $V_b$  to ground. It should be noted that if the

particular circuit application does not require the bias voltage to be well controlled, then the value of resistor 226 can be set to zero without sacrificing the benefit to be derived from the invention.

In order to insure that  $V_{out}$  will not discharge faster than  $V_b$ , which might forward bias the P-well to the output region junction of transistor 204, the width-to-length ratio W/L of transistors 220 and 232 can be proportioned in accordance with the ratio of the load capacitance 222 to the P-well capacitance 230.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail, such as using a charge pump with a different number of stages, or using different polarity devices may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An integrated charge pump circuit comprising an output terminal for outputting a back bias voltage and at least one diode-type voltage-multiplier stage having a diode-configured NMOS transistor, a P-type well surrounding said NMOS transistor and forming the back gate thereof, said NMOS transistor being a low-threshold transistor, and a bias circuit for continuously generating a bias voltage as a function of and less than said back bias voltage to be applied to said P-type well and having an input connected to and having an input signal derived continuously from said output terminal and an output connected to and providing an output signal continuously to said P-type well.

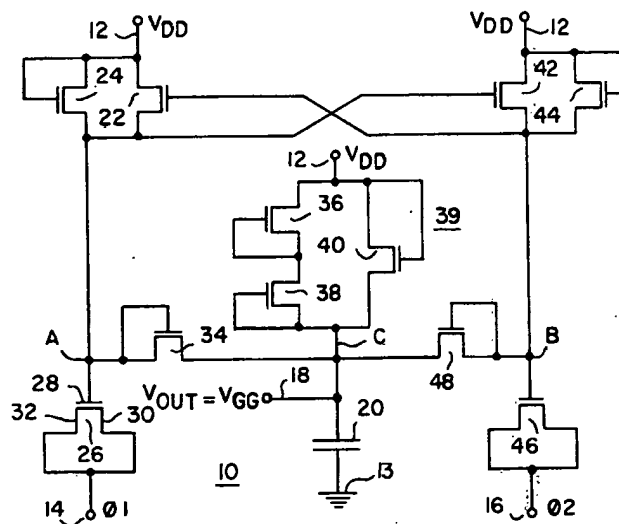
2. An integrated charge pump circuit a claimed in claim 1, wherein the threshold voltage of said diode-configured transistor is less than about one volt at zero back gate bias.

3. An integrated charge pump circuit as claimed in claim 1, wherein said bias circuit comprises a further NMOS transistor connected as a source-follower, the input of said source follower being connected to said output terminal and the output of said source follower being coupled to said P-type well.

4. An integrated charge pump circuit as claimed in claim 3, further comprising a resistor and a current source connected in series, a first terminal of said resistor being connected to the source of said further NMOS transistor, a second terminal of said resistor being connected to a first terminal of said current source and forming the output of said source follower, a second terminal of said current source being connected to ground, and the drain of said further NMOS transistor being connected in operation to a source of voltage.

\* \* \* \* \*





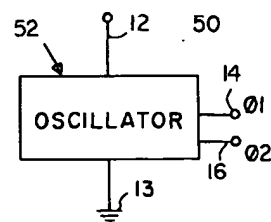


Fig 1b

Fig 1a

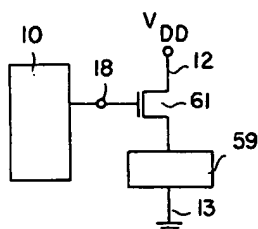


Fig 1c

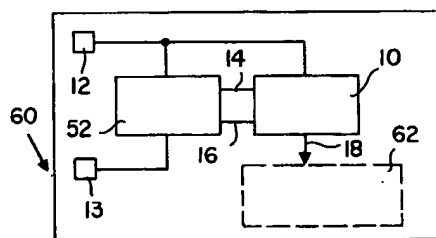


Fig 1b

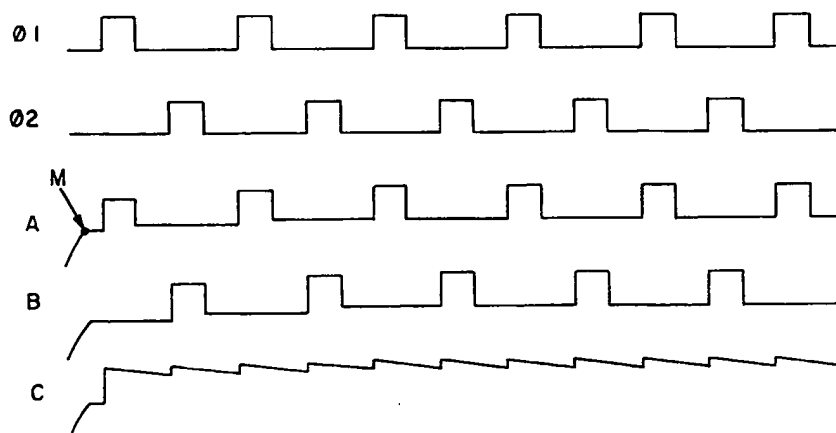


Fig 2

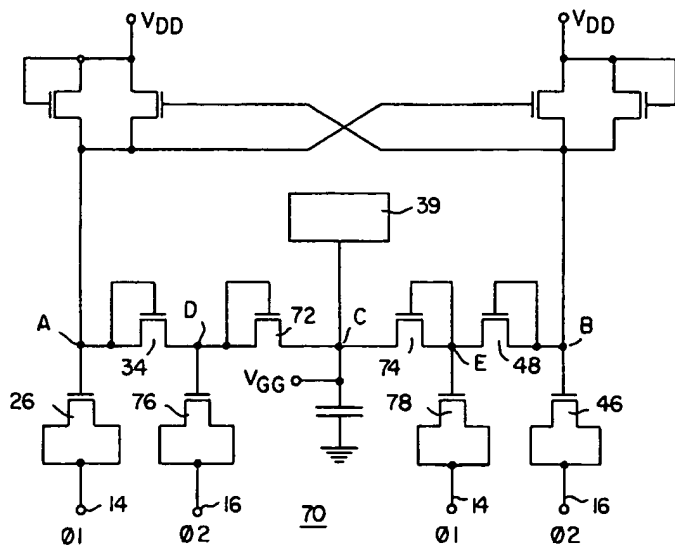


Fig 3

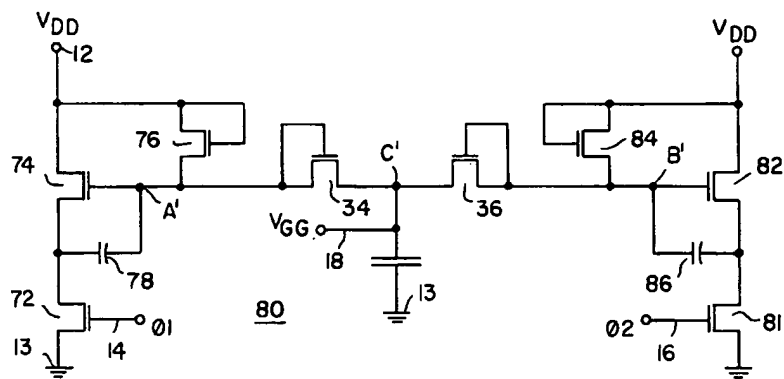


Fig 4

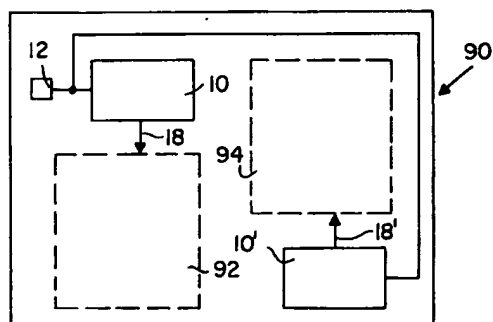


Fig 5

## MOS DC VOLTAGE BOOSTER CIRCUIT

### BACKGROUND OF THE INVENTION

MOS large scale integrated circuits have become increasingly popular in the electronics market because of their ability to provide high component densities at low cost per function at moderate speeds and relatively low power dissipation. However, for optimum performance, a plurality of relatively high power supply lines, commonly designated VDD and VGG as well as the ground conductor have been required. Improvements in the state-of-the-art MOSFET processing techniques have been developed to provide MOS chips which operate from the same relatively low voltage, for example, 5 volts, as popular bipolar integrated circuit logic families, for example, TTL, etc. However, it has been difficult to obtain the required circuit speeds for MOS LSI circuits at such low power supplies. Further, with the very high component density on MOS LSI integrated circuit chips, a large number of circuit functions per chip are obtainable, and a serious problem exists in providing enough leads and bonding pads for the semiconductor package and chip to provide the necessary signals for operation of the complex logic functions. Further, at such low power supply voltages, variations in the MOS processing parameters, especially the MOS threshold voltage  $V_t$  to become more significant, making far more difficult the design of certain logic circuits on the chip under worst-case conditions. Further, at such low power supply voltages, the voltage drops across the long metallization lines on the chip which distribute the supply voltage become significant and make more difficult design of logic elements located distant from the power supply bonding pad. In some cases, bootstrap inverter circuits and drivers have been used to produce high voltage pulses which provide the additional required drive to particular MOSFETs, usually MOSFET load devices, which need to generate a large magnitude signal with a fast rise time. But the variation and the magnitude of such pulses with processing variations has usually been in the opposite sense required for optimum circuit design. Further, race conditions normally associated with digital pulse generating circuitry further compound the problem of getting adequate high voltage signals to particular MOSFETs for the required period of time.

It is an object of the invention to provide an improved voltage booster circuit.

It is a further object of the invention to provide a voltage booster circuit fabricated with metal oxide semiconductor field effect transistors (MOSFETs).

It is a further object of the invention to provide an integrated circuit chip with at least one internal circuit which generates a DC voltage greater in magnitude than any voltage externally applied to the integrated circuit chip.

It is a further object of the invention to provide an integrated circuit chip with a plurality of internal voltage booster circuits which are located so as to distribute the stepped up DC voltage to nearby portions of the circuit requiring such stepped up voltage.

### SUMMARY OF THE INVENTION

Briefly described, the invention provides a voltage booster circuit for producing a stepped up voltage at an output node thereof and includes, in one embodiment, a field effect transistor load device coupled between

the supply voltage conductor and a capacitor, the opposite node of which is coupled to a periodic signal or clock signal. From the junction between the load field effect transistor and the capacitor is a diode-connected field effect transistor, the source of which is connected to the output node. In one embodiment of the invention, a voltage regulator circuit is connected to the output node, and includes at least one diode-connected field effect transistor coupled between a power supply and the output node; the source being connected to the output node, and in parallel contains at least one diode-connected field effect transistor coupled in the opposite sense between the output node and the power supply conductor. In another embodiment, a second load field effect transistor and capacitor are coupled in series between the power supply conductor and a second clock signal conductor, and a second diode-connected field effect transistor is coupled between the output node and the junction between the second load field effect transistor and the second capacitor. In another embodiment, a first feedback transistor is coupled in parallel with the first load field effect transistor and has its gate connected to the second junction, and a second feedback field effect transistor is coupled in parallel with the second load field effect transistor and has its gate connected to the first junction. In another embodiment of the invention, the above-described voltage boosters are provided on an integrated circuit chip to provide a stepped up bias voltage to a portion of the circuitry on the chip. In another embodiment, a free-running oscillator on the chip provides the required periodic clock input signal. In another embodiment, back-to-back bootstrap inverters have a capacitor terminal of the feedback capacitance thereof connected to a diode-connected field effect transistor which charges the output capacitance associated with the output node. This reduces the capacitive loading on the clock signals.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic diagram of a preferred embodiment of the invention.

FIG. 1B is a clock diagram representing a free-running oscillator which generates the periodic signals required by the embodiment of FIG. 1A.

FIG. 1C is a diagram illustrating a typical application of the voltage booster circuit of FIG. 1A.

FIG. 1D is a diagram representative of an integrated circuit chip incorporating the oscillator of FIG. 1B and the voltage booster circuit of FIG. 1A to provide a stepped up voltage on the integrated circuit chip.

FIG. 2 is a timing diagram useful in describing the operation of the embodiment of FIG. 1A.

FIG. 3 is a schematic diagram of another embodiment of the invention which produces a stepped up voltage higher in magnitude than the embodiment of FIG. 1A.

FIG. 4 is a schematic diagram of an alternative embodiment of the invention which produces less capacitive loading on the clock signal lines than the embodiments of FIG. 1A and FIG. 3.

FIG. 5 is a diagram representative of an integrated circuit chip having a plurality of voltage booster circuits as in FIGS. 1A, 3, or 4 which generate separate stepped up voltages which are distributed to separate appropriate portions of circuitry on the integrated circuit chip.

## DESCRIPTION OF THE INVENTION

FIG. 1A is a schematic diagram of a preferred embodiment of the invention. In FIG. 1A, voltage booster circuit 10 includes a first section including capacitor 26 coupled between input signal conductor 14 and node A and MOSFETs (metal oxide semiconductor field effect transistors) 22 and 24 coupled between supply voltage conductor 12 and node A, and diode-connected MOSFET 34 coupled between node A and output node C. (A diode-connected MOSFET is one in which the gate and drain electrodes are connected together). Output node C is connected to output conductor 18. An output capacitor 20 represents a capacitance associated with conductor 18 and is coupled between conductor 18 and ground supply conductor 13.

The MOSFETs described herein may be, in a preferred embodiment, N-channel MOSFETs. A supply voltage commonly designated VDD, may be applied to conductor 12, and may be approximately 5 volts. It is frequently required that a bias voltage greater in magnitude than VDD be available to certain portions of an MOS LSI (large scale integrated) circuit and a separate bonding pad is commonly provided on an integrated circuit chip to allow such a voltage, commonly designated VGG, to be distributed on the semiconductor chip where it is needed. However, this requires an extra pin on the package and an extra bonding pad which could advantageously be used to provide a functional input or output signal to the circuit if the VGG bias voltage could be generated internally.

If a periodic signal 01 is applied to clock signal conductor 14, a boosted, rectified signal will appear at output conductor 18, as will be described hereinafter with reference to the timing diagram of FIG. 2. However, it is important to note that a boosted, rectified signal can be achieved only with the elements thus far described, exclusive of MOSFET 22. However, parasitic leakage currents may result in undesired "ripple" on the output voltage on node C, and variations in processing parameters may result in an output voltage which varies in the wrong direction as a function of such processing parameters. The amount of ripple can be decreased, a desirable amount of regulation achieved, and a higher magnitude of output voltage may be accomplished by addition of the components next to be described.

A regulating circuit 39 is coupled between output node C and conductor 12 in FIG. 1A, and includes diode-connected MOSFET 40 having its gate and drain connected to conductor 12 and its source connected to output node C. Regulating circuit 39 also includes diode-connected MOSFETs 36 and 38 connected in series between conductor 12 and output node C, the source of MOSFET 36 being connected to conductor 12 and the gate and drain thereof connected to the source of MOSFET 38, the gate and drain of the latter being connected to output node C. As is explained hereinafter, additional diode-connected MOSFETs may be connected in series with MOSFETs 36 and 38 to achieve the type of regulation desired.

A second section of voltage booster circuit 10, symmetrical to the first section, includes MOSFETs 42 and 44 coupled between supply voltage conductor 12 and node B, and also includes diode-connected MOSFET 48 coupled between node B and output node C and further includes capacitor 46 coupled between node B

and clock signal conductor 16. Capacitors 26 and 46 may be MOS enhancement capacitors, as schematically illustrated in FIG. 1A. An enhancement capacitor consists of a gate conductor, such as conductor 28, overlying a thin gate oxide layer, which in turn overlies a channel region. The gate conductor overlaps a source region 32 and a drain region 30 which are separated by the channel region. The source and drain regions can be shorted together as shown to form one terminal of the capacitor while the gate electrode forms the other terminal. The main advantage to using enhancement capacitors is their compatibility with conventional MOS manufacturing processes.

Utilization of the symmetrical circuit configuration as shown in FIG. 1A and use of a phase-separated input signals 01 and 02 allows advantageous use of the illustrated cross-coupling technique between MOSFETs 22 and 42, which are referred to herein as feedback devices. The gate of MOSFET 22 is connected to node B and the gate of MOSFET 42 is connected to node A. Those skilled in the art will recognize that in the absence of MOSFETs 22 and 42, load MOSFETs 24 and 44, respectively, are capable of charging nodes A and B, respectively, only to the voltage which is a threshold voltage drop less in magnitude than VDD. However, as explained subsequently herein, feedback MOSFETs 22 and 42 permit nodes A and B, respectively, to be charged all the way to VDD volts.

The operation of the embodiment of FIG. 1A is explained with reference to FIG. 2; the operation of additional embodiments subsequently described herein is in essential respects entirely similar. The input signals 01 and 02 of FIG. 2 may be applied to clock signal conductors 14 and 16, respectively, and as shown, are non-overlapping signals. Waveform A appears at node A of FIG. 1A. Initially, if node A is at zero volts, node A is charged up through MOSFET 24 to  $V_{DD} - V_{th}$  volts, where  $V_{th}$  is the threshold voltage of MOSFET 24; this transition is indicated by point M on waveform A. When the first  $\phi_1$  pulse occurs, the charge on capacitor 26 tends to cause the voltage across capacitor 26 to be constant during the leading edge of the first  $\phi_1$  pulse. This causes the voltage at node A to be boosted. The charge on capacitor 26 is redistributed between the parasitic capacitance of node A (not shown) and capacitor 20 through unidirectional diode-connected MOSFET 34, thereby causing node C to be further charged up. The waveform at node C is shown by waveform C of FIG. 2. When the initial pulse of signal 01 disappears, node A falls back to  $V_{DD} - V_{th}$  volts, and is maintained at that level by MOSFET 24, which charges enhancement capacitor 26 up again. However, node C remains essentially at the voltage it was charged up to, since diode-connected MOSFET 34 prevents any loss of charge on capacitor 20 to node A. When the first 02 pulse occurs, the waveform B, which appears at node B, responds in an entirely similar fashion, further charging up output capacitor 20. The resulting waveform on output node C, which is at the same potential as output conductor 18 is shown in FIG. 2 as waveform C. The slight ripple effect on waveform C would occur if any parasitic leakage currents existed which would tend to discharge the potential at output node C between clock pulses. Of course, there is no requirement that the relationship between clock signals 01 and 02 be as illustrated in FIG. 2. In fact, they may be in phase or at different frequencies, and overlap. But if overlapping clock pulses are used, MOSFETs 22 and 42 must

be eliminated. The intermediate levels of waveform A (and B), as previously mentioned, are  $V_{DD} - V_{th}$  volts in the absence of MOSFETs 22 and 42. However, if node A is at  $V_{DD} - V_{th}$  volts, and 02 pulse occurs and boosts the voltage at node B to approximately  $V_{DD} - V_{th}$  plus 02 volts, MOSFET 22 will be sufficiently overdriven to further charge node A up to  $V_{DD}$  volts. Similarly, the intermediate level of node waveform B is boosted to  $V_{DD}$  volts by the action of MOSFET 42 when a 01 pulse occurs. Therefore, the boosted output voltage  $V_{OUT}$  at output node C, in absence of clamping regulator circuit 39, is then equal to the peak voltages at nodes A and B. That is, the voltage at output node C is equal to  $V_{DD}$  plus the magnitude of the 01 and 02 (assuming they are of the same magnitude) minus  $V_{th}$ , the threshold voltage of MOSFETs 34 and 48. In other words, the boosted output voltage  $V_{OUT}$  is given by the equation  $V_{OUT} = V_{DD} + \phi / -V_{th}$ , where  $\phi /$  is the magnitude of 01 and 02.

The operation of the regulator circuit 39 acts to limit the voltage at output node C in two ways. First, MOSFET 40 prevents  $V_{OUT}$  from falling below  $V_{DD} - V_{th}$  volts. Secondly, MOSFETs 36 and 38 prevent  $V_{OUT}$  from being boosted to more than  $V_{DD}$  plus 2  $V_{th}$  volts. Of course, additional MOSFETs may be placed in series with either MOSFETs 36 or 38 or MOSFET 40 to provide the desired limits. This regulating scheme provides a great advantage in worst case design of MOS circuits in that the VGG bias voltage required for biasing load devices of MOS logic gates and inverters and the like is preferably regulated in such a way that for large MOS threshold voltages VGG is large in magnitude, while for small MOS thresholds VGG is relatively less in magnitude. For a more complete discussion of the considerations of worst case design conditions for MOSFET load devices, see copending application, Ser. No. 475,376, by the same inventor and filed on even date herewith. FIG. 1c schematically depicts the arrangement thus suggested, in which voltage booster circuit 10 has its output terminal 18 connected to the gate of MOSFET 61, which is the load device of an MOS logic gate including MOSFET 61 and additional MOSFET circuitry 59 coupled between the source of MOSFET 61 and ground conductor 13. Improved power dissipation, circuit speed, and noise margin performance results from the suggested combination, wherein regulator 10 is the device shown in FIG. 1A including the regulator 39.

As previously suggested, the clocking input signals 01 and 02 do not have to be square wave signals as in FIG. 2, but rather may be signals generated by an oscillator coupled between voltage supply conductor 12 and ground conductor 13. As shown in FIG. 1D, free-running oscillator 52 may be provided on integrated circuit chip 60, which may in turn drive voltage booster circuit 10, as in FIG. 1A, which in turn provides a bias voltage which is distributed to various load devices and the like in MOSFET circuitry on a portion 62 of integrated circuit chip 60.

The following table lists typical values for the devices in FIG. 1A which have been used in a successful implementation of the circuit.

MOSFET	CHANNEL WIDTH	CHANNEL LENGTH (Mils)
	(Mils)	
22	1.0	.3
24	1.0	.3
34	1.0	.3
36, 38, 40	1.0	.3

MOSFET	-continued	
	CHANNEL WIDTH	CHANNEL LENGTH (Mils)
	(Mils)	
48	1.0	.3
42, 44	1.0	.3

Enhanced capacitors 26 and 46 may have an area of approximately 12 square mils.

FIG. 3 schematically depicts another embodiment of the invention which is entirely similar in operation to that of FIG. 1A, and where applicable the same reference numerals have been used. It differs from the embodiment of FIG. 1A mainly in the addition of diode-connected MOSFETs 72 and 74 coupled, respectively, between the source of MOSFET 34 and node C and the source of MOSFET 48 and node C. Further, enhanced capacitor 76 has been coupled between the source of MOSFET 34 and clock signal conductor 16, and enhancement capacitor 78 has been coupled between the source of MOSFET 48 and clock signal conductor 14. In this embodiment, the intermediate level at waveform A is boosted by the action of a 01 pulse and enhanced capacitor 26 so that the charge on capacitor 26 is redistributed through MOSFET 34 and is trapped on node D. If the magnitude of 01 is approximately equal to  $V_{DD}$ , the magnitude of the DC voltage on node D is approximately twice that of the intermediate level at node A. The currents of a 02 pulse further boosts the DC voltage at node D by the action of capacitor 76, as charges distributed through MOSFET 72 to node C thus, the voltage of node C is approximately equal to  $V_{DD}$  plus the magnitude of 01 plus magnitude of 02 plus the magnitude of 02 minus 2  $V_{th}$ .

The embodiment of FIG. 4 illustrates a voltage booster circuit in which the capacitive loading on clock signal conductors 14 and 16 may be reduced somewhat. The circuit includes a first MOS bootstrap inverter circuit including MOSFETs 74, 76, 72, and feedback capacitor 78. The voltage at A' has an intermediate level of approximately  $V_{DD} - V_{th}$  volts, and is boosted to approximately twice this value when MOSFET 72 is off at a combined action of feedback capacitor 78 and the pullup action of MOSFET 74. This voltage diminished by the threshold voltage of MOSFET 34 appears as a DC voltage trapped on node C'. The symmetrically connected bootstrap inverter including the MOSFETs 82, 84, and 81 and feedback capacitor 86 and diode-connected MOSFET 36 provide increased efficiency by reducing the ripple voltage magnitude if substantial leakage currents at node C exists. The gate capacitance of MOSFETs 72 and 81 can be substantially less than the capacitance of enhanced capacitors 26 and 46 of FIG. 1A, so that the capacitive loading to be charged up by the signals 01 and 02 is substantially reduced. In some cases this may offer advantages.

FIG. 5 illustrates an integrated circuit chip 90 which includes several voltage booster circuits 10 and 10', which may be any of the voltage booster circuits described herein. In FIG. 5, voltage booster circuit 10 and 10' are coupled between supply voltage conductor 12 and the ground conductor 13 (not shown in FIG. 5). The output voltages VGG and VGG' appear, respectively, at output nodes 18 and 18' and independently supply a bias voltage to MOS circuits 92 and 94, respectively, on different portions of the surface of integrated chip 90. As mentioned previously, this scheme of providing a plurality of voltage boosters where re-

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quired on an integrated circuit chip makes an additional bonding pad and package lead available for signal processing purposes, and allows provision of boosted input voltages of different magnitudes to suit different requirements on the chip, and provides an independent degree of voltage regulation for each which, as described earlier, may offer substantial design advantages in accomplishing optimum worst case circuit design with respect to manufacturing processing parameters such as MOS device threshold voltage.

I claim:

1. A voltage booster circuit coupled to a supply voltage conductor including a first MOSFET coupled between said supply voltage conductor and a first node for charging capacitance associated with the first node, a capacitor coupled between the first node and a first clock signal conductor, and a first diode-connected MOSFET coupled between the first node and a second node, the voltage booster circuit comprising:

a second diode-connected MOSFET having its gate and drain coupled to said supply voltage conductor and its source coupled to said second node, and third and fourth diode-connected MOSFETs coupled in series between said second node and said supply voltage conductor, the source of said fourth diode-connected MOSFET being coupled to said supply voltage conductor, the gate and the drain of said third diode-connected MOSFET being coupled to said second node.

2. A voltage booster circuit, coupled to a supply voltage conductor, for producing a stepped up voltage comprising:

first field effect transistor load means coupled between said supply voltage conductor and a first node for charging capacitance associated with said first node;

capacitive voltage boosting means coupled to said first node and a first clock signal conductor for boosting a voltage on said first node;

diode-connected field effect transistor circuit means coupled between said first node and a second node for transferring charge from said first node to said second node to charge up the capacitance associated with said second node;

second field effect transistor load means for charging a third node coupled between said supply voltage conductor and said third node;

second capacitive voltage boosting means for boosting a voltage on said third node coupled between a second clock signal conductor and said third node; and

second diode-connected field effect transistor circuit means for transferring charge from said third node to said second node coupled between said third node and said second node.

3. The voltage booster circuit as recited in claim 2 further including first field effect transistor feedback load means for charging the voltage on said first node to the voltage on said supply voltage conductor means

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coupled between said supply voltage conductor means and said first node and also coupled to said third node and being responsive to the voltage on said third node, and second field effect transistor feedback load means for charging the voltage on said third node to the voltage on said supply voltage conductor means coupled between said supply voltage conductor means and said third node and also coupled to said first node and being responsive to the voltage on said first node.

4. A voltage booster circuit for producing a stepped up voltage at an output voltage node comprising:

first MOSFET load means for charging a first node coupled between supply voltage conductor means and said first node;

second MOSFET load means for charging a second node coupled between said supply voltage conductor means and said second node;

a first diode-connected MOSFET transistor coupled between said first node and said output voltage node;

a second diode-connected MOSFET transistor coupled between said second node and said output voltage node; and

first and second capacitors coupled, respectively, between said first node and a first clock signal conductor and said second node and a second clock signal conductor.

5. The voltage booster circuit as recited in claim 4 further including MOSFET regulator clamping circuit means coupled to said output voltage node for regulating the voltage at said output voltage node.

6. An integrated chip including at least one voltage booster circuit as recited in claim 1 coupled to supply voltage conductor means and distributing a stepped up voltage to a first portion of said integrated circuit chip.

7. The integrated circuit chip as recited in claim 6 further including another said voltage booster circuit coupled to said supply voltage conductor means for producing a second stepped up voltage to a second portion of said integrated circuit chip.

8. A voltage booster circuit as recited in claim 1 wherein said capacitor is an enhancement capacitor having its gate electrode coupled to said first node.

9. A voltage booster circuit for producing a stepped up voltage at an output voltage node comprising:

a load MOSFET coupled between supply voltage conductor means and a first node;

a second diode-connected MOSFET coupled between said supply voltage conductor means and the gate of said load MOSFET;

a bootstrap capacitor coupled between said first node and the gate of said load MOSFET;

a switching MOSFET coupled between said supply voltage conductor means and said first node having its gate coupled to clock signal conductor means;

a second diode-connected MOSFET coupled between the gate of said load MOSFET and said output voltage node.

\* \* \* \* \*

# United States Patent [19]

Whidden

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[45] Mar. 9, 1976

## [54] DC TO DC VOLTAGE CONVERTER

[75] Inventor: James R. Whidden, Baldwinsville, N.Y.

[73] Assignee: General Electric Company, Syracuse, N.Y.

[22] Filed: Dec. 13, 1974

[21] Appl. No.: 532,367

### Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 418,236, Nov. 23, 1973, abandoned.

[52] U.S. Cl. .... 321/15; 320/1; 307/111

[51] Int. Cl.<sup>2</sup> ..... H02M 7/00

[58] Field of Search ..... 307/1, 2, 110; 320/1; 321/2, 15

### [56] References Cited

#### UNITED STATES PATENTS

3,240,958	3/1966	Kerios et al.	307/110
3,432,738	3/1969	Jensen	321/15
3,478,258	11/1969	Nagai	321/15
3,820,004	6/1974	Sugiura et al.	321/15
3,821,627	6/1974	Milovancevic	321/2

3,824,447 7/1974 Kuwabara ..... 321/15

### OTHER PUBLICATIONS

Electronic Design, "Transformerless Voltage Doubler has Good Output Regulation," Vol. 26, p. 64, Dec. 21, 1972.

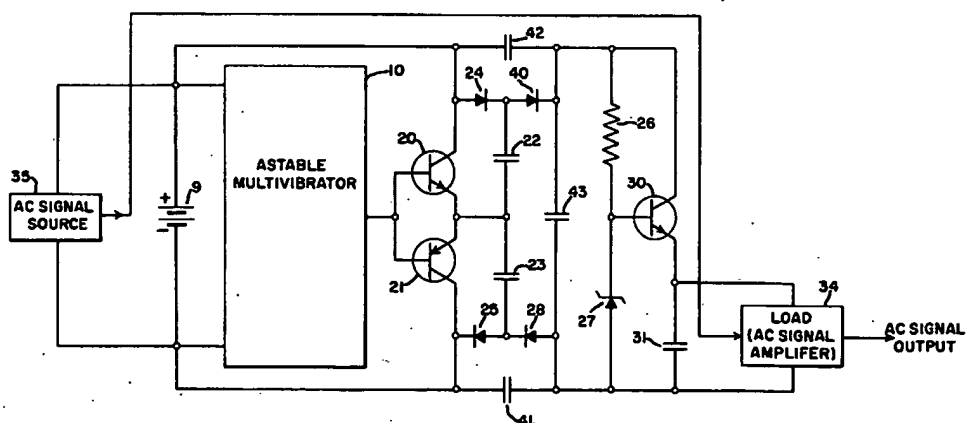
Scientific & Technical Aerospace Reports (Star), Issue No. 9, p. 1430, Figure 14, May 8, 1965.

Primary Examiner—William M. Shoop

### [57] ABSTRACT

A DC voltage source of amplitude below the DC voltage requirement of a load to be energized drives a pair of complementary transistors which are alternately turned on and off to apply supply voltage alternately to each of two capacitors connected in series. The sum voltage of the two capacitors is applied, in one embodiment, directly to a voltage regulator and filtered and, in another embodiment, is added to the DC source voltage prior to being regulated and filtered. The converter output is capacitively coupled to the DC supply voltage, thus furnishing a common AC connection.

14 Claims, 2 Drawing Figures





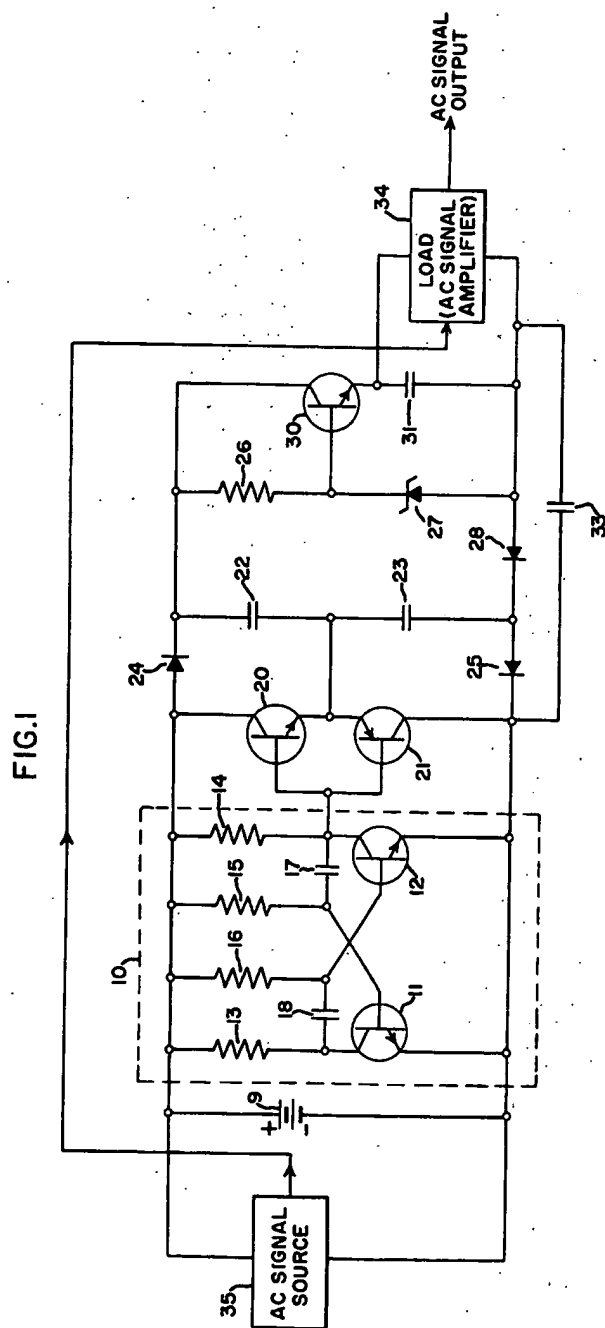
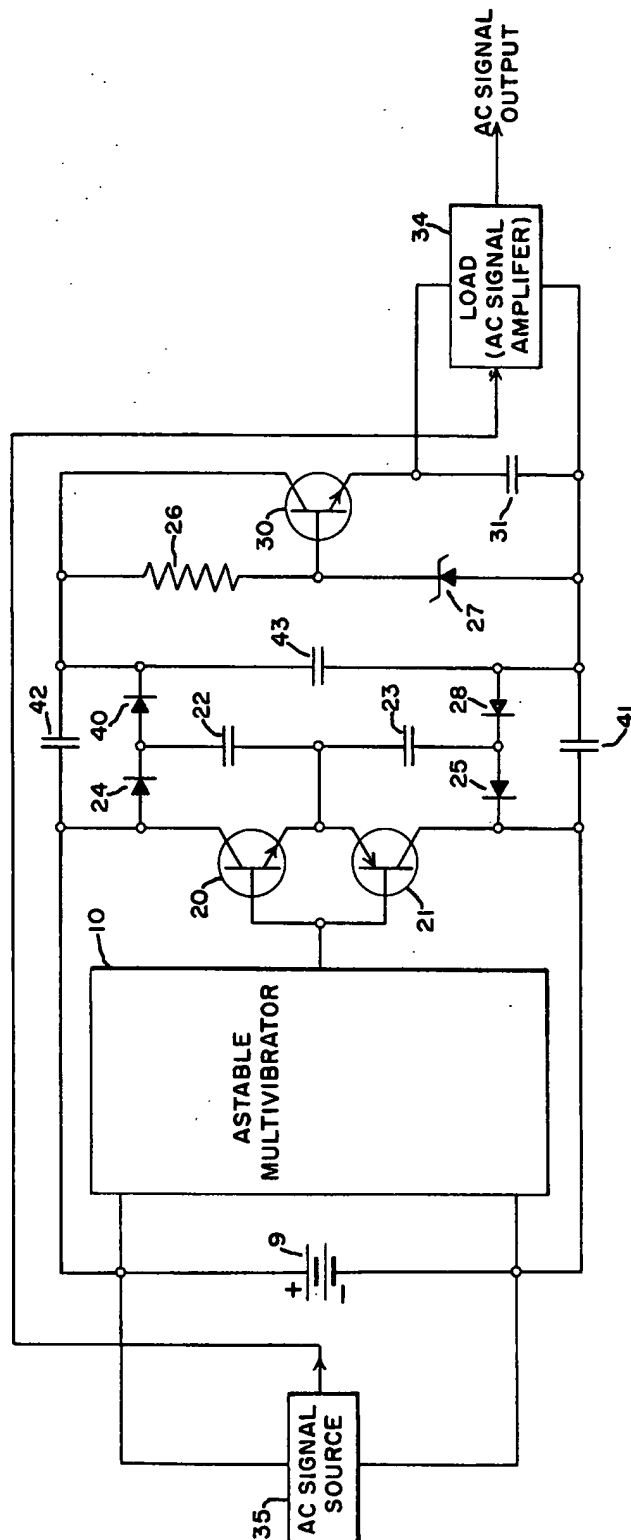


FIG. 2



## DC TO DC VOLTAGE CONVERTER

This is a continuation-in-part of application Ser. No. 418,236 filed Nov. 23, 1973, and now abandoned.

## INTRODUCTION

This invention relates to DC voltage amplitude converters, and more particularly to DC voltage doublers and triplers having well-regulated output voltage.

Portable battery-operated devices, of which many types are commonly used throughout the world, have never been standardized to operate from a single power supply voltage. Different types of apparatus usually require different power supply voltage levels, and different manufacturers of similar apparatus frequently establish different power supply voltage levels for their products.

Often the need to employ a power supply of higher voltage level may be met by increasing the total number of battery cells to be used with the product. Since the cells that are used in portable devices requiring sufficient current to drive a motor are usually rated at 1.5 volts each, the number of cells required to furnish rated DC voltage to some portable battery-operated devices may become so great as to detract from the portability or small size of the device. It is under such circumstances that DC to DC voltage converters may advantageously be incorporated into these devices to step up the DC level furnished by the power supply without requiring additional battery cells.

Because some portable battery-operated devices require rather precise levels of voltage for proper operation, it heretofore has often been unfeasible to employ converters in such apparatus because of their inadequate voltage regulation characteristics. The present invention, however, is directed to a DC to DC voltage converter which exhibits close regulation of its output voltage.

Accordingly, one object of the invention is to provide a DC to DC voltage converter that maintains a well-regulated level of output voltage.

Another object is to provide a DC voltage doubler capable of conducting alternating current between the voltage source and the load.

Another object is to provide a DC voltage tripler capable of conducting alternating current between the voltage source and the load.

Another object is to provide a transformless DC to DC converter employing complementary transistors to charge each one of a pair of capacitors in alternate manner.

Briefly, in accordance with a preferred embodiment of the invention, a DC to DC voltage converter comprises pulse generator means, and gating means coupled to the pulse generator means. First and second charge storage means are coupled to the gating means. The gating means furnishes a current path to the first charge storage means in response to a positive-going change in voltage produced by the pulse generator means and furnishes a current path to the second charge storage means in response to a negative-going change in voltage produced by the pulse generator means. Output circuit means are connected in series with the first and second charge storage means, the first and second charge storage means being connected in series-aiding relationship.

## BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawing in which:

FIG. 1 is a schematic diagram of one embodiment of a DC to DC voltage converter constructed in accordance with the instant invention; and

FIG. 2 is a schematic diagram of another embodiment of a DC to DC voltage converter constructed in accordance with the instant invention.

## DESCRIPTION OF TYPICAL EMBODIMENTS

FIG. 1 illustrates a DC to DC voltage converter including an astable multivibrator 10 of conventional configuration. Thus the multivibrator comprises first and second active elements 11 and 12 respectively, such as NPN transistors, each with its emitter electrode connected to the negative side of a power supply 9, its collector electrode connected through a load resistance 13 and 14, respectively, to the positive side of the power supply, and its base electrode connected through a bias resistance 15 and 16, respectively, to the positive side of the power supply. In addition, a coupling capacitor 17 is connected between the collector of transistor 12 and the junction of the base of transistor 11 and resistance 15, and a coupling capacitor 18 is connected between the collector of transistor 11 and the junction of the base of transistor 12 and resistance 16. An AC signal source 35 may be connected so as to be energized by power supply 9.

The collector of transistor 12, representing the output of multivibrator 10, is connected to the base electrode of each of transistors 20 and 21. Transistors 20 and 21 are of complementary configuration, transistor 20 being of the NPN type and transistor 21 being of the PNP type. The collector electrode of transistor 20 is connected to the positive side of power supply 9 while the collector electrode of transistor 21 is connected to the negative side of the power supply. The emitter electrodes of transistors 20 and 21 are connected in common to one side of each of a pair of capacitances 22 and 23. A diode 24 is connected in the forward-biased direction between the collector of transistor 20 and the other side of capacitance 22, while a diode 25 is connected in the forward-biased direction between the collector of transistor 21 and the other side of capacitance 23.

Connected in series across the series combination of capacitances 22 and 23 are a resistance 26, a zener diode 27, and a diode 28, the cathode of diode 28 being connected to the anode of diode 25 and the anode of diode 28 being connected to the anode of zener diode 27. The base electrode of an NPN transistor 30 is connected to the junction of resistance 26 and the cathode of zener diode 27, while the collector electrode of transistor 30 is connected to the cathode of diode 24. A filter capacitance 31 is connected between the emitter electrode of transistor 30 and the junction of the anodes of diodes 27 and 28. DC output voltage is provided across capacitance 31 from transistor 30, operated in an emitter follower configuration, to a load 34. If load 34 is a signal processor, such as an AC signal amplifier energized by the voltage across capacitance 31, output

signals from AC signal source 35 are supplied to the input of amplifier 34. A coupling capacitance 33 is connected between the cathode of diode 25 and the anode of diode 28.

During operation of the DC to DC converter of FIG. 1, multivibrator 10 produces pulses at the collector of transistor 12 in a well-known manner. Assuming transistor 11 is nonconductive and transistor 12 is conductive at any given instant of time, the collector-to-emitter voltage on transistor 12 is approximately zero and the collector-to-emitter voltage on transistor 11 is approximately equal to the voltage of power supply 9. Under these conditions, collector current drawn by transistor 12 causes current to flow through resistances 14 and 15, in turn causing a charge buildup on capacitance 17 tending to bias the base of transistor 11 positive.

When capacitance 17 has charged through resistance 15 to a sufficiently high voltage, transistor 11 becomes conductive and draws collector current through resistances 13 and 16. Base voltage on transistor 12 thus drops to a low value, switching the transistor into its nonconductive condition. Collector voltage thereupon rises sharply on transistor 12, producing a positive-going voltage thereon. Subsequently, capacitance 18 acquires a charge tending to bias the base of transistor 12 positive.

When capacitance 18 has charged through resistance 16 to a sufficiently high voltage, transistor 12 again becomes conductive, drawing current through resistance 14 so that collector voltage abruptly drops to approximately zero. At that time, a negative-going voltage is produced on the collector of transistor 12, and transistor 11 is driven into nonconduction. These cycles repeatedly continue as long as multivibrator 10 remains energized, producing a series of positive pulses on the collector of transistor 12 of amplitude approximately equal to that of power supply 9.

Transistor 20 is rendered conductive whenever a positive voltage is applied to its base, while transistor 21 is rendered conductive whenever its base voltage is approximately zero. Conduction of transistor 20 causes current flow through capacitance 23 and diode 25, while conduction of transistor 21 causes current flow through capacitance 22 and diode 24. Thus it is evident that the voltages which build up across capacitances 22 and 23 are in series-aiding relationship. Moreover, the amplitude of voltage on each of capacitances 22 and 23 approaches that of the power supply due to the low series voltage drop across either of transistors 20 and 21, when in the conductive state, and the associated forward-biased diode 25 or 24, respectively. When capacitances 22 and 23 are charged so that their total voltage amplitude exceeds that of power supply 9, diodes 24 and 25 prevent them from discharging back to the power supply. Diodes 24 and 25 also prevent capacitances 22 and 23, respectively, from discharging through transistors 20 and 21, respectively, when the transistor is in a conductive condition.

The total voltage across capacitances 22 and 23, which is approximately double the voltage of power supply 9, is applied across the series combination of resistance 26, zener diode 27, and forward-biased diode 28. The size of resistance 26 is selected to cause diode 27 to operate in its reverse breakdown state so as to maintain a constant voltage on the base of transistor 30 irrespective of the amount of current flow through resistance 26. Because the voltage across the base to

emitter junction of a transistor is approximately constant when the transistor is energized, it follows that even though the resistance of load 34 may vary within a given range, the voltage across the load is maintained essentially constant in accordance with the base to emitter voltage on transistor 30 which remains essentially constant.

Filter capacitance 31, typically of the electrolytic type, serves to filter transient currents produced by multivibrator 10, from the output of the circuit. This keeps multivibrator-produced transient currents from adversely affecting operation of the load. Additionally, capacitance 31 filters pulses that would otherwise appear at the load as a result of repetitively charging and discharging capacitances 22 and 23.

Coupling capacitance 33 is preferably of relatively large size in order to produce a low impedance alternating current path between voltage source 9 and load 34 if and when desired, bypassing diodes 25 and 28. This AC path allows alternating current, separately applied directly to load 34 from AC signal source 35, to return to AC source 35 from the load. Capacitance 31 filters pulses created by the on-and-off switching of diode 28, along with any transients associated with such pulses. Those skilled in the art will recognize that, as an alternative embodiment, an AC signal source may be substituted for load 34 and supply AC signals to a signal processing circuit substituted for AC signal source 35, where circumstances warrant.

Diode 28 prevents capacitance 33 from discharging therethrough when transistor 20 becomes conductive. This production occurs because, when transistor 21 becomes conductive, the cathode voltage of diode 25 remains unchanged, while the anode voltage on diode 25 and cathode voltage on diode 28 drops by an amount equal to the voltage across capacitance 23 (neglecting the collector-to-emitter voltage drop across transistor 21), which is almost equal to the voltage of power supply 9. Diode 25 is thus reverse-biased. At the same time, the anode voltage of diode 28 is driven negative as capacitance 33 acquires a charge caused by discharge of capacitance 23 through transistor 21 and diode 28 in series. When transistor 21 is next driven into nonconduction and transistor 20 into conduction, diode 24 becomes reverse-biased and the anode voltage on diode 25 and cathode voltage on diode 28 rises by an amount equal to the voltage across capacitance 22 (neglecting the collector-to-emitter voltage drop across transistor 20), which is almost equal to the voltage of power supply 9. Diode 25 is thus once again forward-biased. At the same time, the anode of diode 28 is maintained at a negative voltage by virtue of the charge acquired by capacitance 33 during the conduction interval of transistor 21. Thus diode 28 is maintained reverse-biased during the conduction interval of transistor 20 and thereby substantially prevents capacitance 33 from discharging therethrough during the conduction interval of transistor 20. Hence when transistor 21 is next driven into conduction, the voltage stored on capacitance 33 prevents any substantial discharge therethrough from capacitance 23, insuring that the voltage stored on capacitance 23 will remain sufficient high to drive the load with proper voltage amplitude at all times.

It should be noted that load 34 need not be responsive to signals from an AC signal source 35. In such case, AC signal source 35 is not employed, and there would be no need for capacitance 33, while a conduc-

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tive connection would be substituted for diode 28.

In the voltage converter of FIG. 2, astable multivibrator 10, of circuit configuration as illustrated in FIG. 1, is energized by power supply 9. AC signal source 35 may also be connected for energization by power supply 9.

The output of multivibrator 10 is connected to the base electrode of each of complementary transistors 20 and 21. The collector electrode of transistor 20 is connected to the positive side of power supply 9 while the collector electrode of transistor 21 is connected to the negative side of the power supply. The emitter electrodes of transistors 20 and 21 are connected in common to one side of each of capacitances 22 and 23. Diode 24 is connected in the forward-biased direction between the collector of transistor 20 and the other side of capacitance 22, while diode 25 is connected in the forward-biased direction between the collector of transistor 21 and the other side of capacitance 23. Thus far described, the circuitry of FIG. 2 is substantially identical to that of FIG. 1.

The cathode of diode 28 is connected to the anode of diode 25 as in the embodiment of FIG. 1, while the anode of a diode 40 is connected to the cathode of diode 24. A first storage capacitance 41 is connected between the anode of diode 28 and the cathode of diode 25, while a second storage capacitance 42 is connected between the anode of diode 24 and the cathode of diode 40. A third storage capacitance 43 is connected between the anode of diode 28 and the cathode of diode 40. Resistance 26 and zener diode 27 are connected in series between the anode of diode 28 and the cathode of diode 40, the anode of zener diode 27 being connected to the anode of diode 28. The base electrode of transistor 30 is connected to the junction of resistance 26 and the cathode of zener diode 27, while the collector electrode of transistor 30 is connected to the cathode of diode 40. Filter capacitance 31 is connected between the emitter electrode of transistor 30 and the anode of diode 28. DC output voltage is provided across capacitance 31 from transistor 30, operated in an emitter follower configuration, to load 34. Since load 34 is typically a signal processor, such as an AC signal amplifier energized by the voltage across capacitance 31, output signals from signal source 35 are supplied to the input of amplifier 34.

During operation of the DC to DC converter of FIG. 2, multivibrator 10 produces positive pulses as described in conjunction with the circuit of FIG. 1, NPN transistor 20 being rendered conductive whenever a positive voltage is applied to its base and PNP transistor 21 being rendered conductive whenever its base voltage is approximately zero. When transistor 21 becomes conductive, drawing collector-to-emitter current through diode 24 and capacitance 22 in series, the cathode voltage of diode 25 remains unchanged, while the anode voltage on diode 25 and cathode voltage on diode 28 drops by an amount equal to the voltage across capacitance 23 (neglecting the emitter-to-collector voltage drop across transistor 21), which is almost equal to the voltage of power supply 9. Diode 25 is thus reverse-biased. At the same time, the anode voltage of diode 28 is driven negative as capacitance 41 acquires a charge from capacitance 23 discharging through transistor 21 and diode 28 in series. In this fashion, capacitance 41 acquires a DC voltage substantially equal in amplitude to the voltage of power supply 9.

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When transistor 21 is next driven into nonconduction and transistor 20 into conduction drawing emitter-to-collector current through capacitance 23 and diode 25 in series, diode 24 becomes reverse-biased since the anode voltage of diode 24 remains unchanged, while the cathode voltage on diode 24 and anode voltage on diode 40 is increased by an amount equal to the voltage across capacitance 22 (neglecting the collector-to-emitter voltage drop across transistor 20), which is almost equal to the voltage of power supply 9 after but a few cycles of operation of multivibrator 10. At the same time, the cathode voltage of diode 40 is driven positive as capacitance 42 acquires a charge from capacitance 22 discharging through transistor 20 and diode 40 in series. In this fashion, capacitance 42 acquires a DC voltage substantially equal in amplitude to the voltage of power supply 9.

When transistor 20 is again driven into nonconduction and transistor 21 into conduction, diode 25 again becomes reverse-biased and the cathode voltage on diode 24 and anode voltage on diode 40 drops by an amount equal to the voltage across capacitance 23 (neglecting the emitter-to-collector voltage drop across transistor 21), which is almost equal to the voltage of power supply 9. Diode 24 is thus once again forward-biased. Consequently, capacitance 43 becomes charged with a DC voltage equal to the sum of the voltages on capacitances 41 and 42 and the voltage of power supply 9, all of which are connected in series-aiding relationship, thereby reaching substantially three times the amplitude of voltage furnished by power supply 9. The polarity of voltage on capacitance 43 is such that diodes 40 and 28 prevent discharge through capacitances 22 and 23, respectively, and, in conjunction with diodes 24 and 25, respectively, also prevent discharge of capacitance 43 back through power supply 9.

The tripled voltage of power supply 9, appearing across capacitance 43, is applied across the series combination of resistance 26 and zener diode 27. The size of resistance 26 is selected to cause diode 27 to operate in its reverse breakdown state so as to maintain a constant voltage on the base of transistor 30 irrespective of the amount of current flow through resistance 26. Because the voltage across the base to emitter junction of transistor 30 is thus approximately constant, the voltage across load 34 is maintained essentially constant.

Filter capacitance 31 serves to filter transient currents produced by multivibrator 10, from the output of the circuit so as to keep such currents from adversely affecting operation of the load. Capacitance 31 also filters pulse that would otherwise appear at the load as a result of repetitively charging and discharging capacitances 22 and 23 and storage capacitances 41, 42 and 43, including pulses created by the on-and-off switching of diodes 28 and 40 along with any transients associated with such pulses.

Storage capacitances 41 and 42 are preferably of relatively large size in order to produce a low impedance alternating current path between voltage source 9 and load 34 if and when desired, bypassing diodes 25 and 28. This AC path allows alternating current, separately applied directly to load 34 from AC signal source 35, to return to AC source 35 from the load. Storage capacitance 43 adds filtering to the circuit. As an alternative embodiment, an AC signal source may be substituted for load 34 and supply AC signals to a signal processing circuit substituted for AC signal source 35,

where circumstances warrant.

When diode 25 is forward-biased during conduction of transistor 20, the anode of diode 28 is maintained at a negative potential by virtue of the charge previously acquired by capacitance 41 during the conduction interval of transistor 21. Thus diode 28 is maintained reverse-biased during the conduction interval of transistor 20. When transistor 21 is next driven into conduction, the voltage stored on capacitance 41 prevents any appreciable discharge therethrough from capacitance 23, insuring that the voltage stored on capacitance 23 will remain sufficiently high to maintain proper voltage amplitude at all times on capacitance 41. Similarly, when diode 24 is forward-biased, the cathode of diode 40 is maintained at a positive potential by virtue of the charge previously acquired by capacitance 42 during the conduction interval of transistor 20. Thus diode 40 is maintained reverse-biased during the conduction interval of transistor 21. When transistor 20 is next driven into conduction, the voltage stored on capacitance 42 prevents any appreciable discharge therethrough from capacitance 22, insuring that the voltage stored on capacitance 22 will remain sufficiently high to maintain proper voltage amplitude at all times on capacitance 42. Thus the voltage stored across capacitances 22 and 23 in series is not directly applied to the load since diodes 40 and 28 conduct on alternate half cycles, respectively, of the multivibrator output voltage.

The foregoing describes a DC to DC voltage converter that maintains a well-regulated level of output voltage. The converter, which may be operated as either a doubler or tripler of DC voltage, capable of conducting alternating current between the voltage source and the load, is transformerless and employs complementary transistors to charge each one of a pair of capacitances in alternate manner.

While only certain preferred features of the invention have been shown by way of illustration, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

I claim:

1. A DC to DC voltage converter for use with a load which is also responsive to an AC source comprising: pulse generator means; gating means coupled to said pulse generator means; first and second charge storage means coupled to said gating means, said gating means furnishing a current path to said first charge storage means in response to a positive-going change in voltage produced by said pulse generator means and furnishing a current path to said second charge storage means in response to a negative-going change in voltage produced by said pulse generator means; output circuit means connected in series with said first and second charge storage means, said output circuit means including voltage regulator means, said first and second charge storage means being connected in series-aiding relationship; capacitance means coupling said output circuit means to said pulse generating means; and unidirectional conducting means coupling said first charge storage means to said voltage regulator means and poled so as to be reverse-biased each time said gating means furnishes a current path to said first charge storage means and thereby prevent

said capacitance means from discharging through said unidirectional conducting means at said time.

2. The apparatus of claim 1 wherein said gating means comprises first and second transistors each having a base electrode, an emitter electrode, and a collector electrode, each of said collector electrodes being coupled to one side of each of said first and second charge storage means, respectively, each of said base electrodes being connected to said pulse generator means, and each of said emitter electrodes being connected in common to the other side of each of said first and second charge storage means.

3. The apparatus of claim 2 wherein said pulse generator means comprises an astable multivibrator having first and second active elements, and first transistor being rendered conductive and said second transistor nonconductive in response to a rise in voltage across said first active element and said second transistor being rendered conductive and said first transistor nonconductive in response to a rise in voltage across said second active element.

4. The apparatus of claim 2 wherein said first and second transistors are of complementary configuration and said base electrodes are connected in common.

5. The apparatus of claim 3 wherein said first and second transistors are of complementary configuration and each of said base electrodes is connected to said first active element.

6. A converter for increasing voltage amplitude furnished from a DC power supply, said converter comprising:

pulse generator means;

gating means coupled to said pulse generator means;

first and second charge storage means coupled to

said gating means, said gating means furnishing a

charging current path to said first charge storage

means in response to a change in voltage of one

polarity direction produced by said pulse generator

means and furnishing a charging current path to

said second charge storage means in response to a

change in voltage of opposite polarity direction

produced by said pulse generator means;

third charge storage means coupled to said gating

means, said gating means furnishing a current path

from said first charge storage means to said third

charge storage means in response to said change in

voltage of opposite polarity direction produced by

said pulse generator means; and

output circuit means connected in series with said

third charge storage means, said third charge stor-

age means being connected in series-aiding rela-

tionship with said power supply.

7. The apparatus of claim 6 wherein said output circuit means includes voltage regulator means.

8. The apparatus of claim 6 wherein said gating means comprises first and second transistors each having a base electrode, an emitter electrode, and a collector electrode, each of said collector electrodes being coupled to one side of each of said first and second charge storage means, respectively, each of said base electrodes being connected to said pulse generator means, and each of said emitter electrodes being connected in common to the other side of each of said first and second charge storage means.

9. The apparatus of claim 6 including fourth charge storage means coupled to said gating means, said gating means further furnishing a current path from said second charge storage means to said fourth charge storage

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means in response to said change in voltage of one polarity direction produced by said pulse generator means, said fourth charge storage means being connected in series with said output circuit means and in series-aiding relationship with said power supply and said third charge storage means.

10. The apparatus of claim 9 wherein said output circuit means includes voltage regulator means.

11. The apparatus of claim 9 wherein said gating means comprises first and second transistors each having a base electrode, an emitter electrode, and a collector electrode, each of said collector electrodes being coupled to one side of each of said first and second charge storage means, respectively, each of said base

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electrodes being connected to said pulse generator means, and each of said emitter electrodes being connected in common to the other side of each of said first and second charge storage means.

12. The apparatus of claim 9 including fifth charge storage means connected in parallel with said output circuit means.

13. The apparatus of claim 10 including fifth charge storage means connected in parallel with said output circuit means.

14. The apparatus of claim 11 including fifth charge storage means connected in parallel with said output circuit means.

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[54] **CAPACITIVE VOLTAGE CONVERTER  
EMPLOYING CMOS SWITCHES**

[75] Inventor: Peter A. Stoll, Santa Clara, Calif.

[73] Assignee: Intel Corporation, Santa Clara, Calif.

[22] Filed: Feb. 24, 1975

[21] Appl. No.: 552,439

[52] U.S. Cl. .... 321/15; 307/110;  
357/42; 357/59

[51] Int. Cl.<sup>2</sup> ..... H02M 3/06

[58] Field of Search ..... 321/15; 307/109, 110;  
357/42, 59

[56] **References Cited**

**UNITED STATES PATENTS**

3,818,484 6/1974 Nakamura et al. .... 321/15  
3,824,447 7/1974 Kuwabara ..... 321/15

3,878,450 4/1975 Greatbatch ..... 321/15

**OTHER PUBLICATIONS**

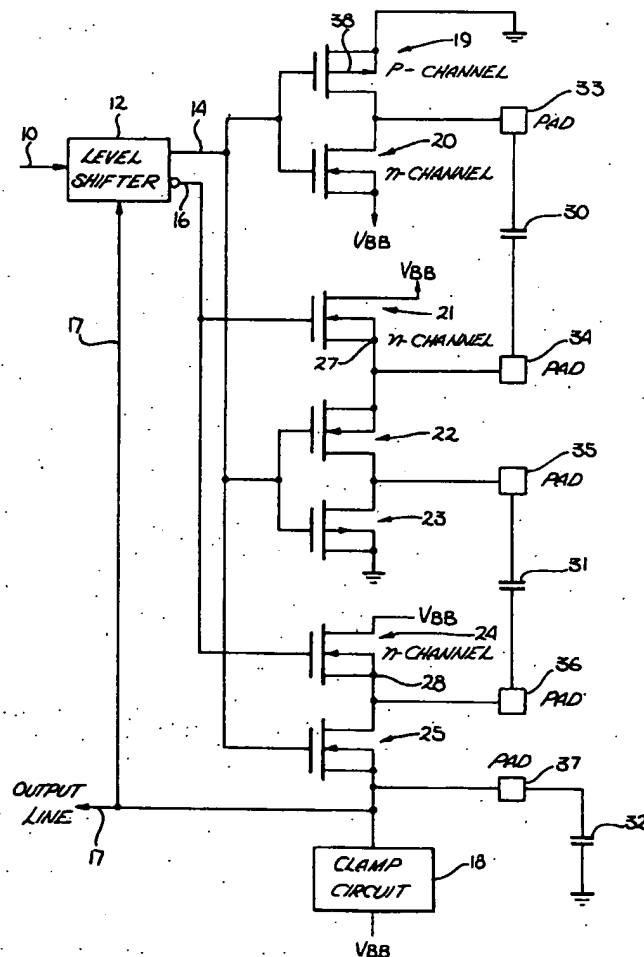
"Fundamentals of COS/MOS Integrated Ckts." by Bishop et al.; *Solid State Tech.*, Apr., 1974, pp. 85-89.  
"Production of C-IGFETS" by Kroel et al.; *IBM Tech. Disc. Bull.* vol. 15, No. 5, Oct., 1972, pp. 1623-1624.

Primary Examiner—Gerald Goldberg  
Attorney, Agent, or Firm—Spensley, Horn, & Lubitz

[57] **ABSTRACT**

A CMOS circuit for approximately tripling battery voltage particularly adaptable for use with liquid crystal displays such as used in watches. P-wells of the CMOS circuit are coupled to active circuit nodes rather than to battery potentials. In the presently preferred embodiment a hybrid circuit with external capacitors is used to increase overall efficiency.

7 Claims, 2 Drawing Figures





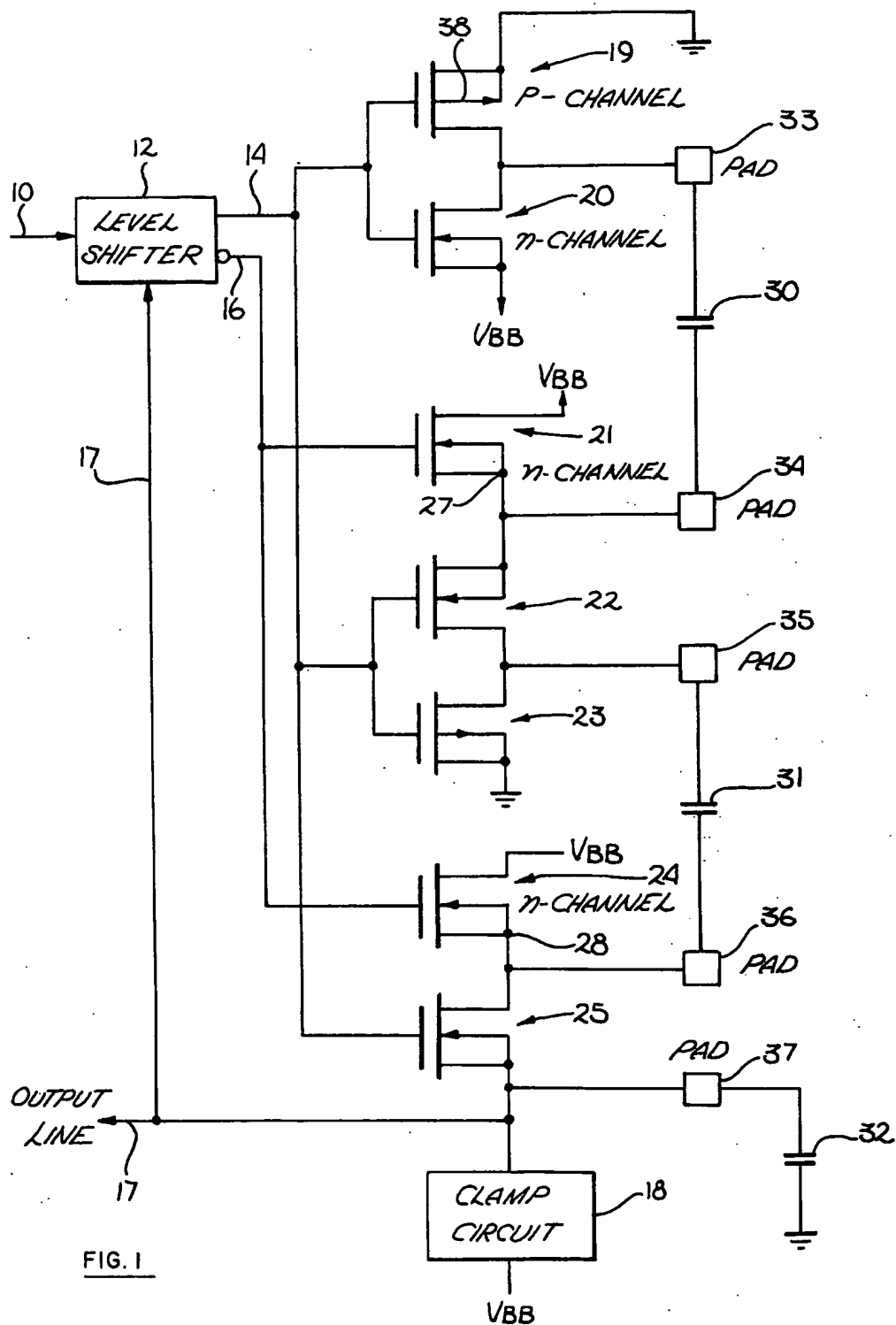
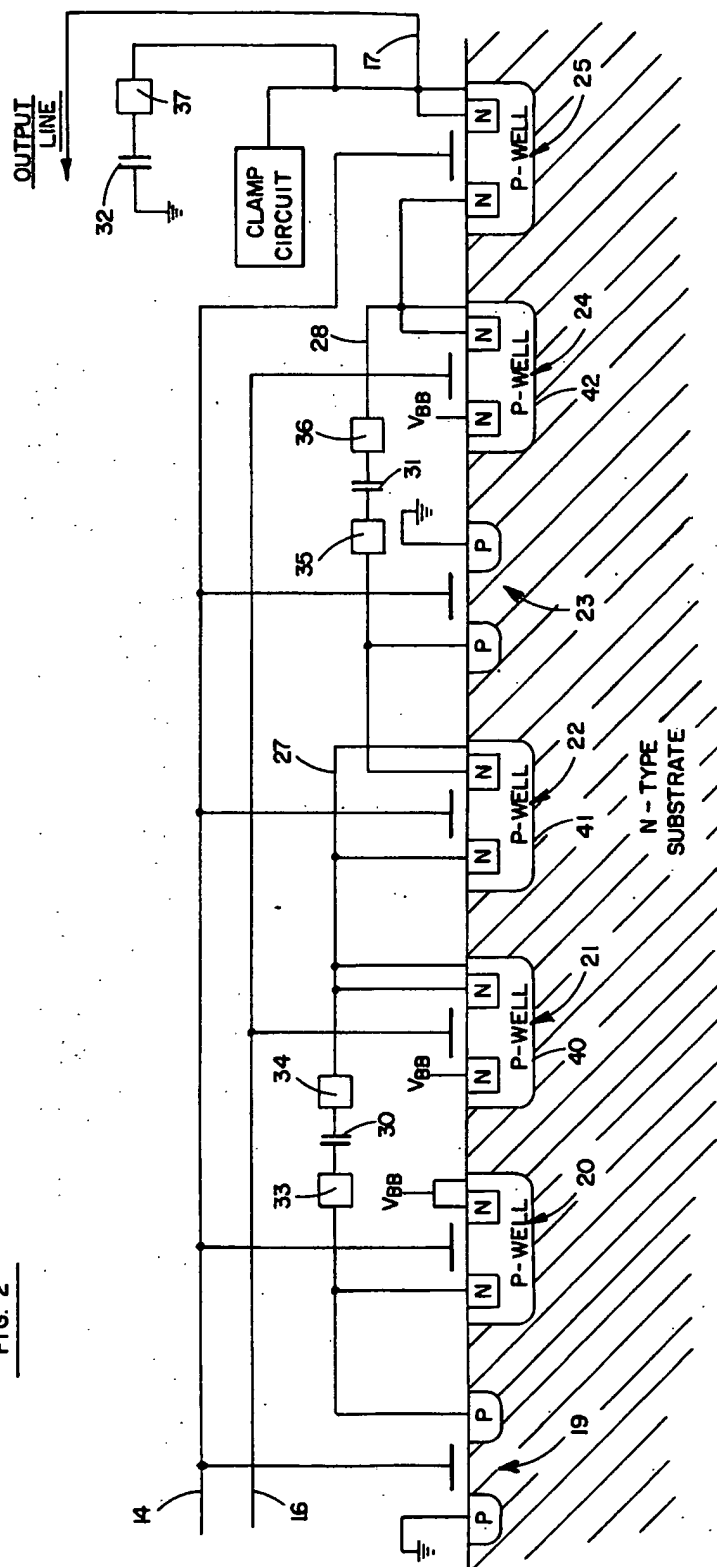


FIG. 2



## CAPACITIVE VOLTAGE CONVERTER EMPLOYING CMOS SWITCHES

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The invention relates to the field of voltage converters employing CMOS devices.

#### 2. Prior Art

Complementary metal-oxide-silicon (CMOS) devices have been utilized in applications where low power consumption is required, such as in electronic watches. In such watches and in other applications voltages higher than those economically available from batteries are required for displays, particularly for liquid crystal displays. In the prior art numerous circuits are known for raising a battery potential, for example, of 1.5 volts, to a higher potential such as 4.5 volts for activating displays.

Generally, the prior art voltage converting circuits employ resistors, diodes, inductors and bipolar transistors in a resonant transfer circuit. These components cannot be integrated into the CMOS circuit used for the remainder of the watch circuitry. Moreover, such components are relatively expensive when compared to the remainder of the watch electronics.

As will be seen, the present invention provides a voltage converter employing only CMOS active devices although external capacitors are utilized in the presently preferred embodiment. The presently disclosed circuit provides a less expensive, and more efficient, converter than known in the prior art.

### SUMMARY OF THE INVENTION

A circuit is disclosed for charging a capacitance means and for then coupling the capacitance means in series with another potential means. The capacitance means is coupled between a first and a second connection means. A first transistor is disposed on a substrate of a first conductivity type. This transistor selectively couples the capacitance means so that the capacitance means may be charged. The first transistor includes a channel which is disposed in a well in said substrate, the well being of an opposite conductivity type to the substrate. The capacitance means is coupled to the well. A second transistor is used for coupling the capacitance means and potential means in series. The circuit includes control means which is coupled to the first and second transistors for causing the capacitance means to be alternately charged and coupled in series with the potential means. The potential of the well of the first transistor changes as the capacitance means and potential means are coupled and decoupled, thereby allowing the first transistor to operate as a switch.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of the presently preferred embodiment of the voltage converter.

FIG. 2 is a cross-sectional elevation view of a substrate which includes the transistors of FIG. 1.

### DETAILED DESCRIPTION OF THE INVENTION

In the presently preferred embodiment the voltage converter converts a first potential or battery potential to a higher level which is approximately three times the battery potential. As will be appreciated, the principle of the present invention may be utilized for other than voltage tripling. Also in the presently preferred em-

bodiment the CMOS devices are deployed on an n-type substrate where p-type wells are used to define n-channel devices. As will be obvious to one skilled in the art, the invention may be utilized on a p-type substrate.

In FIG. 1, an input line 10 which is coupled to a level shifter 12 is supplied with a signal such as a 1 khz square wave. The input square wave, or other signal, in the case of a watch may be derived from a crystal source, although such accuracy is not required. The level shifter 12 provides two complementary outputs, one on line 14, and the other on line 16. The output from the circuit of the figure, line 17, is coupled to level shifter and provides a potential greater in magnitude than  $V_{BB}$  for powering the level shifter 12. By way of example, assume an input square wave to level shifter 12 varies between zero and -1.5 volts and that the output on line 17 is approximately -4.5 volts. The output of level shifter 12 would be two square waves varying between zero and approximately -4.5 volts. Any one of a number of known prior art circuits may be utilized for level shifter 12.

In the presently preferred embodiment all the transistors employ polycrystalline silicon gates. The convention used for the transistors in the figure is as follows: an arrow pointing away from the gate signifies a p-channel transistor, an arrow pointing into the gate signifies an n-channel transistor, and the connection between the center line (such as line 38 of transistor 19) and one of the other two terminals of the transistors signifies the biasing of the substrate in the case of p-channel transistors and the p-well in the case of n-channel transistors. For example, transistor 20 has one of its n-type regions and its p-well connected to  $V_{BB}$ . The other terminal of transistor 20 is coupled to one terminal of transistor 19 and to one terminal of capacitor 30. The other terminal of transistor 19 and the substrate are coupled to the negative potential  $V_{BB}$ .

Transistors 19 and 20 are coupled in series between ground and  $V_{BB}$ , the gate of both these transistors are coupled to line 14. Transistors 21, 22 and 23 are coupled in series between  $V_{BB}$  and ground. An n-type region of both transistors 21 and 22 along with the p-type wells 40 and 41 (FIG. 2) of transistors 21 and 22, respectively, are coupled to a node 27 defined between transistors 21 and 22; this node being also coupled to the other terminal of capacitor 30. Note that the p-wells of transistors 21 and 22 are coupled to an active signal node in the circuit rather than to a power supply potential. The common node between transistors 22 and 23 is coupled to one terminal of capacitor 31. This node includes an n-type region of transistor 22 and a p-type region of transistor 23. The gate of transistor 21 is coupled to line 16; the gates of transistors 22 and 23 are coupled to line 14.

Transistors 24 and 25 are coupled in series between  $V_{BB}$  and a clamp circuit 18. The gate of transistor 24 is coupled to line 16; the gate of transistor 25 is coupled to line 14. The common junction between transistors 24 and 25, node 28, is coupled to the other terminal of capacitor 31. This node includes the p-well 42 of transistor 24, thereby coupling this p-well to an active circuit node. An n-type region of transistor 25, defining one terminal of the transistor, is coupled to one terminal of capacitor 32, the clamp circuit 18 and to the output line 17.

In the presently preferred embodiment capacitors 30, 31 and 32 are external capacitors, that is, they are not part of the common substrate upon which the remain-

der of the circuit is fabricated. Since the transistors, level shifter 12 and clamp circuit 18 are formed on the same substrate, the external capacitors are coupled to the substrate through "pads". For example, capacitor 30 is coupled between pads 33 and 34, capacitor 31 is coupled between pads 35 and 36 and capacitor 37 is coupled to pad 37, the other terminal of this capacitor being coupled to ground. "On chip" capacitors may be utilized although it has been found that a more efficient circuit is possible where external capacitors are utilized. In the presently preferred embodiment 0.01 microfarads capacitors are utilized.

The clamp circuit 18 is used to clamp line 17 to  $V_{BB}$  to activate or start the circuit. Note that the line 17 provides power for level shifter 12; thus to activate the circuit, line 17 is held at the  $V_{BB}$  potential through the clamp circuit 18. Once an output is produced on lines 14 and 16, line 17 is released from  $V_{BB}$  and allowed to rise (in the negative direction) in potential. In applications where the circuit is utilized as part of a watch, clamp circuit 18 may be a manual switch momentarily closed upon assembly of the watch or when a battery is replaced. Any one of numerous clamping circuits may be utilized for clamp circuit 18 including automatically activated circuits.

In operation capacitors 30 and 31 are charged to the potential  $V_{BB}$ , in parallel, and then coupled in series with the potential  $V_{BB}$  to provide an output on line 17 of approximately  $3V_{BB}$ . Capacitor 32 which is coupled to line 17 provides filtering of the output signal. Capacitor 30 is charged through transistors 19 and 21; capacitor 31 is charged through transistors 23 and 24. Transistor 20 couples one terminal of capacitor 30 to  $V_{BB}$  (for the series connection of the capacitors) while transistors 22 and 25 couple capacitors 30 and 31 in series to line 17.

Assume for the sake of examining the operation of the circuit, that a negative potential equal to approximately  $3V_{BB}$  is present on line 14, while simultaneously, a zero potential exists on line 16. The negative potential on the gates of transistors 19 and 23 cause these transistors to conduct while the same negative potential of the gates of transistors 20, 22 and 25 prevent these transistors from conducting. The zero potential (line 16) on the gates of the pull-down transistors 21 and 24 cause these transistors to conduct. Thus, when a negative potential is present on line 14, and a zero potential on line 16, capacitor 30 charges through transistors 19 and 21 and capacitor 31 charges through transistors 23 and 24.

When the output from level shifter 12 changes and a negative potential equal to approximately  $3V_{BB}$  is present on line 16 and a zero potential on line 14, transistor 19 ceases to conduct and transistor 20 conducts. Similarly, transistors 21 and 23 cease to conduct while transistor 22 conducts. Also transistor 24 ceases to conduct and transistor 25 conducts. Since the capacitors are assumed to have been previously charged, the potential present on line 17 is equal to  $V_{BB}$  plus the sum of the voltages to which capacitors 30 and 31 have been charged. In actual tests the potential on line 17 approaches  $3V_{BB}$ .

In FIG. 2 transistors 19, 20, 21, 22, 23, 24 and 25 are shown on an n-type substrate. The connections between these transistors and particularly the capacitors 30 and 31 are again shown. From this figure the p-well connections are readily seen, note that the p-wells 40 and 41 for transistors 21 and 22, respectively are cou-

pled to pad 34, and that the p-well 42 for transistor 24 is coupled to pad 36. Thus the potential of these wells may vary as will be explained. (Note the pads 33, 34, 35, 36 and 37 are shown above the substrate for purposes of illustration in FIG. 2).

An important aspect of the present invention is the fact that the p-well 40 of the transistor 21 is coupled to an active node, node 27. If this p-well were coupled to line 17, transistor 21 would fail to turn on when a zero potential was present on line 16. On the other hand, if the p-well 40 of transistor 21 was coupled to  $V_{BB}$ , transistor 21 would turn on and charge capacitor 30, however, when capacitor 30 is coupled in series with  $V_{BB}$ , the potential on node 27 rises above  $V_{BB}$  (in the negative sense) providing a forward biased junction with transistor 21. Since the p-well 40 of transistor 21 is coupled to the active node 27, transistor 21 turns on at the appropriate potential, and also remains off when the capacitors are coupled in series. The same is true for pull-down transistor 24 in that its p-well 24 is coupled to an active node 28.

Thus, a voltage converter has been disclosed in the form of a voltage tripler which utilizes CMOS circuits in which external capacitors are first charged in parallel and then coupled in series to provide a higher potential. The circuit is made feasible in part by coupling p-wells of the pull-down transistors to active nodes.

I claim:

1. An MOS integrated circuit disposed on a substrate of a first conductivity type, for coupling a capacitance means to a source of potential such that said capacitance means may be charged from said source of potential, and for coupling said capacitance means to a connection means comprising:

a first well of a second conductivity type disposed on said substrate; said well being coupled to said capacitance means;

a first transistor disposed in said first well, said first transistor including a pair of regions of said first conductivity type, one of said regions coupled to said source of potential and the other of said regions coupled to said capacitance means; and,

a second transistor, said second transistor including a pair of regions of said first conductivity type, one of said regions coupled to said capacitance means and the other region coupled to said connection means;

whereby said capacitance means may be charged from said source of potential then coupled in series with said source of potential or other capacitance means to provide a higher output potential.

2. The circuit defined by claim 1 wherein said second transistor is disposed in a well of said second conductivity type.

3. The circuit defined by claim 2 wherein said first conductivity type is n-type.

4. A CMOS integrated circuit disposed on a substrate of a first conductivity type for charging a capacitor from a source of potential, and for coupling said capacitor in series with said source of potential to provide a higher potential than said source of potential; said source of potential including a first and second potential terminal and said capacitor including a first and second capacitor terminal, comprising:

a first transistor disposed on said substrate, said first transistor including a pair of regions of a second conductivity type, one of said regions coupled to

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said first potential terminals and the other of said regions coupled to said first capacitor terminal;

a first p-well, said first p-well coupled to said second potential terminal;

a second transistor disposed in said first p-well said second transistor including a pair of regions of said first conductivity type, one of said regions coupled to said first capacitor terminal and the other of said regions coupled to said second potential terminal;

a second p-well disposed in said substrate, said second p-well coupled to said second capacitor terminal;

a third transistor disposed in said second p-well, said third transistor including a pair of regions of said first conductivity type, one of said regions coupled to said second potential terminal and the other of said regions coupled to said second capacitor terminal;

a fourth transistor disposed on said substrate, said fourth transistor including a pair of regions of said

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first conductivity type, one of said regions coupled to said second capacitor terminal;

a fifth transistor disposed on said substrate, said fifth transistor including a pair of regions of said second conductivity type, one of said regions coupled to said first potential terminal and the other of said regions providing a common terminal with said other region of said fourth transistor;

whereby said capacitor may be charged from said source of potential and then coupled in series with said source of potential to provide a higher potential at said common terminal.

5. The circuit defined by claim 4 wherein said fourth transistor is disposed within a p-well.

6. The circuit defined by claim 5 wherein said p-well of said fourth transistor is coupled to said second capacitor terminal.

7. The circuit defined by claim 4 wherein said first conductivity type is n-type.

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## [54] CAPACITIVE VOLTAGE MULTIPLIER

[75] Inventors: Jimmy L. Hutchines, San Jose; John E. Meyer, Saratoga, both of Calif.

[73] Assignee: National Semiconductor Corporation, Santa Clara, Calif.

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[51] Int. Cl.<sup>2</sup> ..... H02M 7/00

[52] U.S. Cl. .... 363/59; 357/51

[58] Field of Search ..... 321/15; 357/41, 51

## [56] References Cited

### U.S. PATENT DOCUMENTS

3,824,447	7/1974	Kuwabara	321/15
3,942,047	3/1976	Buchanan	321/15 X
3,955,353	5/1976	Astle	321/15 X
3,975,671	8/1976	Stoll	321/15

### OTHER PUBLICATIONS

"Electronics," Capacitors Add Up in Voltage Multiplier, H. R. Mallory, Mar. 2, 1970, p. 104.

"Scientific & Technical Aerospace Report," NASA, Issue No. 9, p. 1430, N65-18948, p. 8.

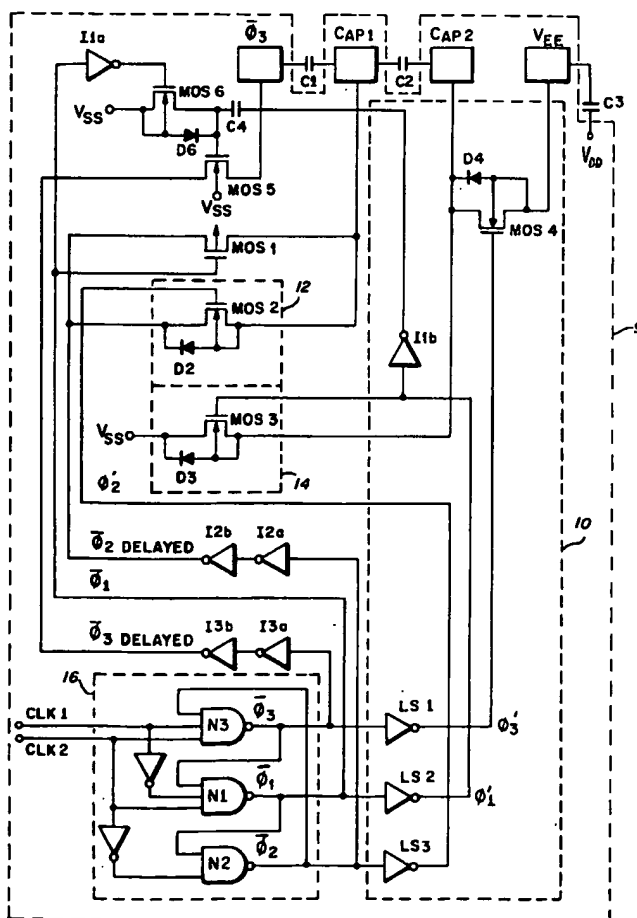
Primary Examiner—William M. Shoop

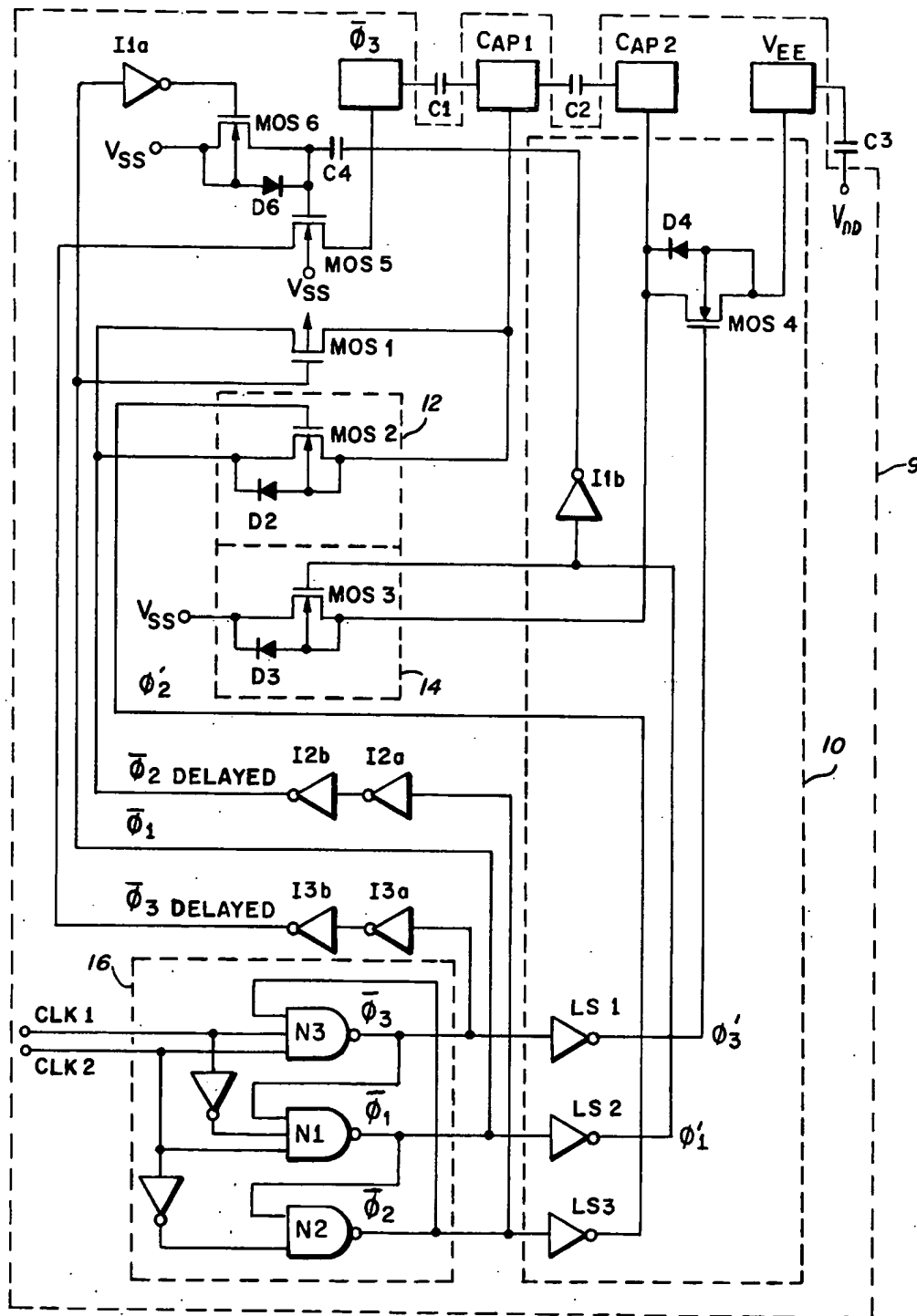
Attorney, Agent, or Firm—Gail W. Woodward; Willis E. Higgins

## [57] ABSTRACT

A voltage multiplier in which an n-phase circuit charges n-1 capacitors during the separate phases, then during the last or nth phase the capacitors are put in series to create n times the input voltage. MOS transistor devices are used to act as switches to charge a number of series connected capacitors. During a first phase of operation, the first in the series of capacitors is charged to a specific voltage to be multiplied by closing the MOS switches to place the voltage across the capacitor. During a next phase of operation, the first capacitor is disconnected by the switches and the next capacitor in series is charged to the input voltage. During successive phases of operation, successive capacitors are similarly charged. During the last phase of operation, the capacitors are connected in series with the voltage to be multiplied and are connected to an output capacitor. This places a total charge on the output capacitor which is equal to the sum of all the charges on the respective series connected capacitors plus the voltage to be multiplied. This results in an n+1 voltage multiplication wherein n is the number of series connected capacitors.

3 Claims, 1 Drawing Figure





## CAPACITIVE VOLTAGE MULTIPLIER

## BACKGROUND OF THE INVENTION

The present invention relates in general to voltage multiplier circuits and, more particularly, to an MOS voltage multiplier circuit.

## DESCRIPTION OF THE PRIOR ART

Integrated circuit technology is utilized in low voltage applications where space is at a premium, such as in digital watches using low power batteries. In such an application, a higher voltage than that supplied by the battery is necessary to drive the time indicating display. Thus, a voltage multiplier circuit is necessary using a minimum number of components external to the integrated circuit, a minimum number of external connecting pins, and a minimum amount of interconnection circuitry within the integrated circuit.

In the past, an n-time-voltage multiplier required 2n pin connections.

Furthermore, in prior voltage multipliers the output voltage is a multiple of the input voltage minus the voltage drop across the transistor or diode circuits utilized. This voltage drop cannot be tolerated in a low voltage system, and since MOS transistor switches can have enough gain to minimize such voltage drops, they are particularly suitable in a voltage multiplier.

## SUMMARY OF THE PRESENT INVENTION

It is a primary object of the present invention to provide an MOS voltage multiplier.

It is also an object of the invention to provide a voltage multiplier which simplifies the interconnecting circuitry and reduces the number of components which are external to the integrated circuit chip.

Briefly, the above objects are accomplished in accordance with the invention by providing a circuit made up of external capacitors connected in series across the pins of an integrated circuit chip. The pins of the chip are connected internally to MOS transistor switches which are operated by a clocking circuit to provide for a multiphase circuit operation.

During successive phases of operation, MOS switches are closed in such a manner that the series connected capacitors are charged successively during each phase to the input voltage. During the final phase of operation, the last capacitor charged is connected to the input voltage and the first capacitor charged is connected to an output capacitor, such that the voltage developed across the output capacitor is the sum of all the voltages across the series connected capacitors plus the input voltage.

The circuit has the advantage that it results in output pin efficiency. In the past, an n-times voltage multiplier needed 2n pin connections. With the present invention, only n+1 connections are required for the n-1 capacitors across which charges are developed.

The invention has the further advantage that since it uses MOS transistors, the multiplied voltage will not be degraded by diode drops generally caused when transistor circuits are used.

## DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following detailed description of a preferred embodiment of the invention, as illustrated in the accompanying draw-

ings wherein the single FIGURE is a schematic diagram of a voltage multiplier incorporating features of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawing, an MOS voltage multiplier circuit is shown wherein the output voltage across the capacitor  $C_3$  is a multiple of the input voltage  $V_{SS}$ . The integrated circuit chip itself is designated by dashed line 9. Capacitors  $C_1$ ,  $C_2$ , and  $C_3$  are off-chip devices connected by conventional pads indicated by the rectangular elements labeled 3, CAP1, CAP2, and  $V_{EE}$ .

The dotted lines 10 indicate a p-channel tub which is common to the most negative supply voltage ( $V_{EE}$ ) that is created. Devices  $I_{1B}$ ,  $L_{S1}$ ,  $L_{S2}$  and  $L_{S3}$  contain n-channel devices connected such that their sources and substrates are the  $V_{EE}$  supply. All other n-channel devices, not within dotted lines, have their substrates connected to the  $V_{SS}$  supply.

MOS 2 and MOS 3 are each in their own individual tubs as indicated by dotted lines 12 and 14. The substrate connections through diodes  $D_2$  and  $D_3$ , respectively, prevent the substrate diodes of MOS 2 and MOS 3 from clamping the generated voltages at CAP 1 and CAP 2 back to  $V_{SS}$ . With the substrate connections as shown, the back gate bias effect (body effect) on MOS 2 and MOS 3 is minimal.

A three phase circuit is shown within dotted lines 16. Clock lines CLK 1 and CLK 2 from an external source are combined in NAND circuits  $N_1$ ,  $N_2$  and  $N_3$  to produce signals  $\Phi_1$ ,  $\Phi_2$ , and  $\Phi_3$ . These signals are powered by level shifters  $L_{S1}$ ,  $L_{S2}$  and  $L_{S3}$  to produce the basic timing signals for the circuitry  $\Phi_1'$ ,  $\Phi_2'$  and  $\Phi_3'$ , respectively. Only one of these outputs is energized at a time, and  $\Phi_2'$  may be longer than  $\Phi_1'$  or  $\Phi_3'$ , for reasons set forth below.

The voltage across capacitor  $C_3$  is multiplied by successively charging capacitors  $C_1$  and  $C_2$  to the voltage  $V_{DD}$  minus  $V_{SS}$ . During phase two and phase three, the gate of MOS 1 is held at  $V_{DD}$  level by NAND gate  $N_1$ , thus turning MOS 1 off.

MOS 2 is an n-channel device with its substrate connected to CAP1 to reverse bias diode  $D_2$  allowing CAP1 to become more negative than  $V_{SS}$ . The substrate of MOS 2 is not connected to  $V_{EE}$  as this would increase the body effect (M factor), thus requiring a larger device to transfer the same amount of charge.

During phase 1, the gate of MOS 2 is held at  $V_{EE}$  by level shifter  $LS3$  thereby turning MOS 2 off.

During phase 2, MOS transfers the voltage  $V_{SS}$  provided by inverter  $I2b$  to the CAP1 pad. This causes the capacitor  $C_1$  to be charged to the voltage  $V_{DD}$  by the action MOS 5.

Since the gate of MOS 3 is held at  $V_{EE}$  level by the level shifter  $LS2$ , MOS 3 is held off during phase 2 and phase 3. With MOS 3 off, shifting CAP1 from the  $V_{DD}$  level to the  $V_{SS}$  level will cause CAP2 to be shifted from the  $V_{SS}$  level to the  $V_{DD}$  minus  $V_{SS}$  level below  $V_{SS}$ .

During phase 3, the gate of MOS 2 is held at  $V_{EE}$  level by level shifter  $LS3$  thereby turning MOS 2 off.

MOS 3 is an n-channel device with its substrate connected to CAP2 to reverse bias diode  $D_3$  which allows CAP2 to be more negative than CAP1. The substrate is not connected to  $V_{EE}$  as this would increase the body effect (M factor) thereby requiring a larger device to transfer the same amount of charge.



During phase 1 of the operation, MOS 3 transfers the  $V_{SS}$  voltage level to CAP2 which, since CAP1 is held at  $V_{DD}$  by the operation of MOS 1, charges capacitor  $C_2$  to the voltage  $V_{DD}$  minus  $V_{SS}$ . During phase 2 and phase 3, the gate of MOS 3 is held at the  $V_{EE}$  voltage level by level shifter LS2, thus turning MOS 3 off.

MOS 4 is an  $n$ -channel device with its substrate connected to  $V_{EE}$  which reverse biases diode  $D_4$ , thus allowing  $V_{EE}$  to become more negative than CAP2.

During both phases 1 and 2, the gate of MOS 4 is held at the  $V_{EE}$  voltage level by level shifter LS1, therefore turning MOS 4 off.

During phase 3, MOS 4 turns on, closing a path between CAP 2 and  $V_{EE}$  to thereby transfer charge from capacitors  $C_1$  and  $C_2$  in series to capacitor  $C_3$ .

MOS 5 is an  $n$ -channel device with its substrate connected to  $V_{SS}$ .

During phase 1, the gate of MOS 5 is held at the  $V_{SS}$  voltage level through MOS 6, which allows the not phase 3 pad to float. Since MOS 5 is an  $n$ -channel device, phase 3 can be driven more positive than  $V_{DD}$ . This allows the charge stored on capacitor  $C_1$  to be maintained during phase 1 when CAP1 is driven to the voltage  $V_{DD}$  by inverter I2b through MOS 1 as explained above.

During phase 2, MOS 5 transfers the  $V_{DD}$  voltage level provided by inverter I3b to the not phase 3 pad. Since CAP1 is held at the  $V_{SS}$  level by MOS 2 during phase 2, capacitor  $C_1$  will charge to the voltage  $V_{DD}$  minus  $V_{SS}$ .

During phase 3, MOS 5 transfers the  $V_{SS}$  level provided by inverter I3b to the not phase 3 pad. Since during phase 3 devices MOS 1, MOS 2 and MOS 3 are all turned off, the CAP1 pad shifts to the  $V_{DD}$  minus  $V_{SS}$  level below  $V_{SS}$ , i.e.  $(2V_{SS}-V_{DD})$ . This shift from the  $V_{SS}$  level of phase 2 to the  $V_{SS}$  minus  $V_{DD}$  level of phase 3 on the CAP1 pad will shift the  $V_{SS}$  minus  $V_{DD}$  level of CAP2 pad of phase 2 to the  $3V_{SS}$  minus  $V_{DD}$  level during phase 3. As described above, MOS 4 transfers the charge from capacitors  $C_1$  and  $C_2$  in series to capacitor  $C_3$  during phase 3. The charges on  $C_1$  and  $C_2$  in series will balance with the charge on  $C_3$  until the  $V_{EE}$  level and the CAP2 level are equal.

MOS 6 is an  $n$ -channel device with its substrate connected to  $V_{SS}$ .

During phase 2 MOS 6 transfers the  $V_{SS}$  voltage level to the gate of MOS 5, which turns MOS 5 off. During phase 1, the output of inverter I1b is at the  $V_{EE}$  level and capacitor  $C_4$  is charged to the voltage  $V_{SS}$  minus  $V_{EE}$ .

During phase 2 and phase 3, the output of inverter I1a applies the voltage  $V_{SS}$  to the gate of MOS 6 turning it off. This allows the gate of MOS 5 to float. During phase 2, the output of inverter I1b swings from the voltage  $V_{EE}$  to  $V_{DD}$  forcing the gate of MOS 6 to the voltage  $V_{SS}$  plus  $V_{DD}$  minus  $V_{EE}$ . This allows MOS 5 to pull the not phase 3 pad to the voltage level  $V_{DD}$  which is provided by inverter I3B. Level shifter LS1 provides a delay which insures that the inverter I1a will turn MOS 6 off before the inverter I1b will begin to swing positive. MOS 1 and MOS 6 have their gates driven from the voltage  $V_{SS}$  to insure correct power of operation regardless of the initial conditions of the output not phase 3, CAP1, CAP2 or  $V_{EE}$ . MOS 2, MOS 3 and MOS 4 have their gates driven from the voltage  $V_{EE}$  in order to provide gate drive negative enough to completely turn the transistors off at the appropriate time. It should be understood that it may be desirable to make phase 2 longer than phase 1 or phase 3 to thereby give

MOS 5 more time to refresh the charge on capacitor  $C_1$  during the phase 2 operation described above.

It should further be understood that the source and drain of MOS 5 may be shorted together connecting the output of I3b directly to the not phase 3 pad. Thus, with capacitor  $C_2$  eliminated and with capacitor  $C_1$  connected between the not phase 3 pad and the CAP 2 pad, the circuit will perform as a voltage doubler capable of forcing  $V_{EE}$  to the voltage  $V_{DD}$  minus  $V_{SS}$  below  $V_{SS}$  ( $2V_{SS}-V_{DD}$ ).

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail which may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A voltage multiplier comprising:

a plurality of capacitors connected in series across the output pads of an integrated circuit chip;  
a clock circuit providing multiphase voltage output;  
means connecting the pads of said chip to MOS transistor switches;

means interconnecting said MOS switches to said clocking circuit such that during successive phases of operation said switches are closed in such a manner that the series connected capacitors are separately charged to the input voltage successively during each phase of said clock circuit; and

means operable during the final phase of operation of said clock for connecting an output capacitor to said input voltage and said series connected capacitors such that the voltage developed across the output capacitors is the sum of all the voltages across the series connected capacitors plus the input voltage.

2. A voltage multiplier comprising:

an integrated circuit chip having a first pad, a second pad, a third pad, and a fourth pad;

a clock circuit providing three outputs, a first phase, a second phase, and a third phase, wherein during each phase the respective output rises from a first voltage level to a second voltage level;

a first capacitor connected across said first and second pads;

a second capacitor connected across said second pad and said third pad;

a first and second MOS transistor connected source to drain between said second pad and said second phase output including means for energizing said first transistor during said first phase and said second transistor during said second phase whereby said first voltage level is applied to said second pad during said first phase and said second voltage level is applied to said second pad during said second phase;

a third MOS transistor connected between said third pad and said second voltage level including means for energizing said third transistor during said first phase for transferring said second voltage level to said third pad;

a fourth MOS transistor connected between said third and fourth pad operable during said third phase for connecting said third and fourth pads together;

a fifth MOS transistor connected between said first pad and said third phase output energizable during said second phase for transferring said first voltage level to said first pad;

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whereby during said first phase of operation said second capacitor is charged to a voltage which is the difference between said first and second voltages applied to said second and third pads, respectively, through said first and third MOS transistors and whereby during said second phase said first capacitor is charged to a voltage which is the difference between said second and first voltages supplied by said second and fifth transistors, respectively, and whereby during said third phase of operation

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said third and fourth pads are connected together through said fourth MOS transistor to thereby apply the voltage on said capacitors to said fourth pad.

3. The combination according to claim 2 further comprising an output capacitor connected to said fourth pad and returned to said first voltage level to thereby provide for the transfer of the charge across said first and second capacitors to said output capacitor.

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[54] **CIRCUIT FOR OBTAINING DC VOLTAGE HIGHER THAN POWER SOURCE VOLTAGE**

[75] Inventor: Kazuhiro Asano, Tokyo, Japan

[73] Assignee: Kabushiki Kaisha Daini Selkoshu, Japan

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[22] Filed: Sept. 21, 1976

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Sept. 23, 1975 Japan ..... 50-115210

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[52] U.S. Cl.: 307/246; 58/23 BA; 307/264; 307/296 A; 307/DIG. 1; 307/DIG. 4; 363/60

[58] Field of Search 307/296, 221 C, 224 C, 307/225 C, 246, 251, 270, 264, DIG. 1, DIG. 4; 58/23 A, 23 BA, 23 D, 50 R; 321/15; 328/176

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

3,639,787	2/1972	Lee	307/DIG. 1 X
3,900,743	8/1975	Weimer	307/DIG. 1 X
3,900,747	8/1975	Yamazaki et al.	307/221 C X
3,955,353	5/1975	Astle	58/23 BA
3,988,617	10/1976	Price	307/DIG. 4 X

**OTHER PUBLICATIONS**

Cassani, "Low-Voltage to High-Voltage Translator"; *IBM Tech. Disc. Bull.*, vol. 17, No. 12, pp. 3541-3542; May, 1975.

*Primary Examiner*—John S. Heyman

*Assistant Examiner*—Larry N. Anagnos

*Attorney, Agent, or Firm*—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A voltage boosting circuit comprises a plurality of units connected in sequence and each composed of a condenser and a plurality of MOS-FETs without any transformer or diode. The boosting circuit lends itself to miniaturization by integrated circuit technique.

7 Claims, 8 Drawing Figures

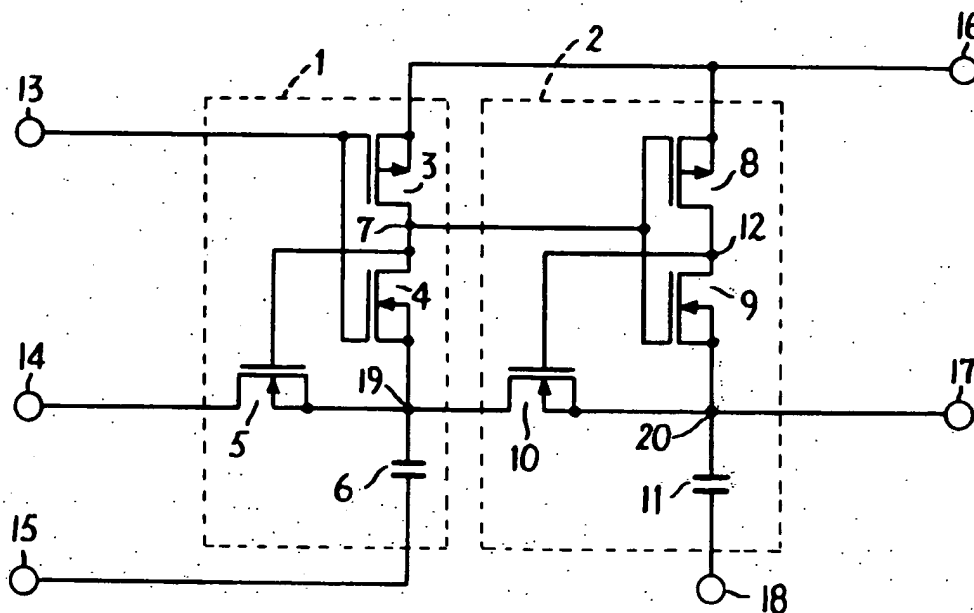


FIG. 1

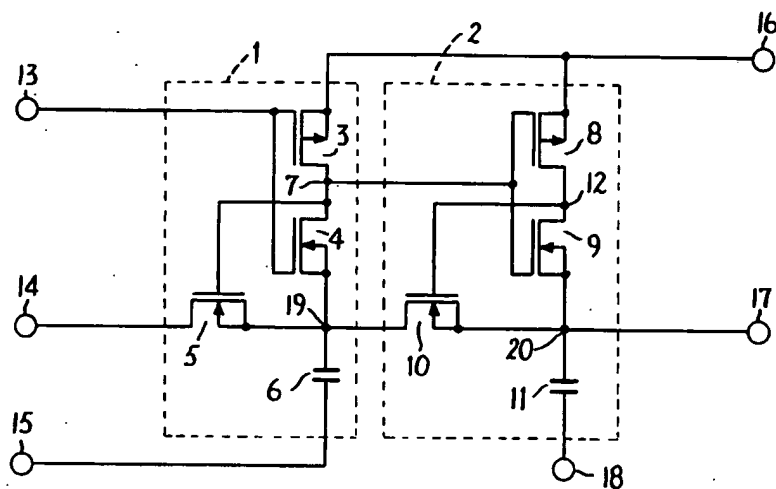
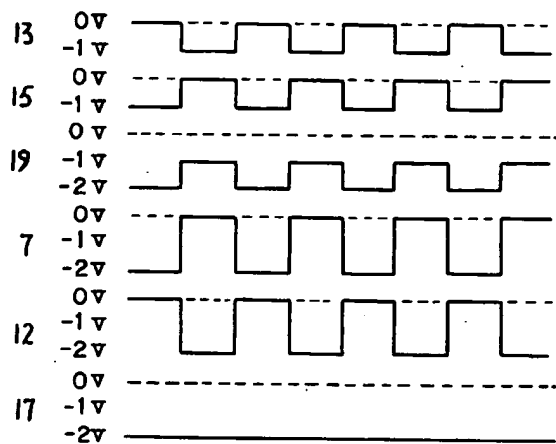


FIG. 2



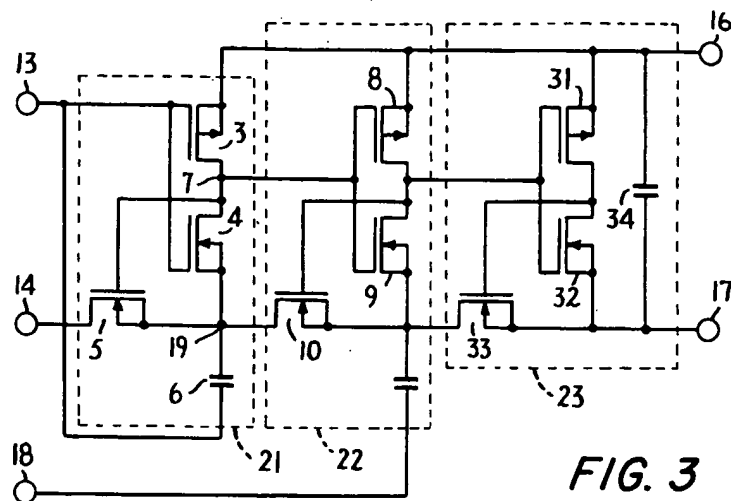


FIG. 3

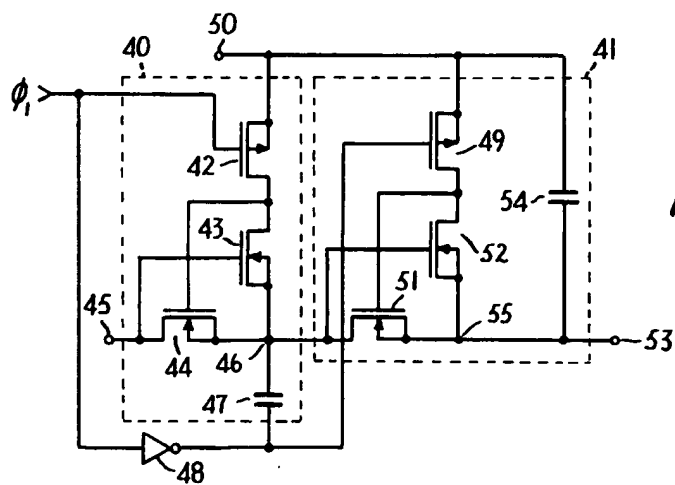


FIG. 4

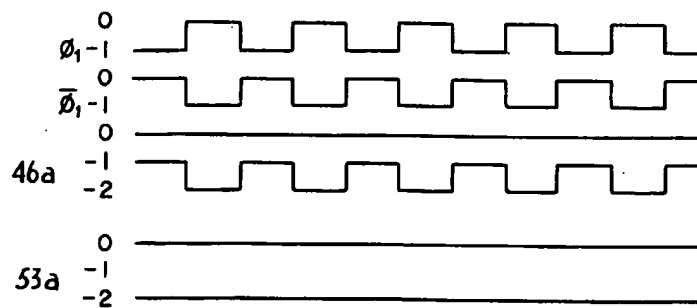


FIG. 5



## CIRCUIT FOR OBTAINING DC VOLTAGE HIGHER THAN POWER SOURCE VOLTAGE

### FIELD OF INVENTION

The present invention relates to a voltage boosting circuit and particularly a circuit that can be miniaturized by integrated circuit techniques.

### BACKGROUND OF INVENTION

The conventional voltage boosting circuit employing a transformer, diode and condenser is very difficult to miniaturize by integrated circuit techniques. Therefore, the space requirements of the conventional voltage boosting circuit make it unsuitable for use where small size is required, for example in a wristwatch or hand held calculator. Furthermore, the cost of the circuit elements comprising a transformer and diode is high so that the cost of an electronic watch or calculator utilizing the voltage boosting circuit is correspondingly high.

### SUMMARY OF INVENTION

The present invention aims to eliminate the above noted disadvantages by providing a voltage boosting circuit which can readily be miniaturized by integrated circuit techniques. In accordance with the invention, the voltage boosting circuit comprises a plurality of units which are connected in sequence and each comprises a condenser and a plurality of MOS-FETs. As the voltage boosting circuit in accordance with the invention does not require any transformers or diodes it can be incorporated in integrated circuitry so as to be suitable for use in a small sized electronic watch or calculator. The desired boosting magnification is attained by employing a plurality of the boosting units connected in sequence with the output voltage of one unit applied as the input voltage of the next unit.

### BRIEF DESCRIPTION OF DRAWINGS

The above mentioned and further objects, features and advantages of the present invention will become more apparent from the following description when taken in connection with the accompanying drawings in which:

FIG. 1 is a circuit diagram of a voltage boosting circuit in accordance with the invention having two voltage boosting units;

FIG. 2 shows diagrammatically the voltage forms of each portion of the circuit of FIG. 1;

FIG. 3 is a circuit diagram of a voltage boosting circuit having three voltage boosting units;

FIG. 4 is a circuit diagram of a voltage boosting circuit having two voltage boosting units;

FIG. 5 shows waveforms for explaining the operation of the circuit of FIG. 4;

FIG. 6 is a circuit diagram of a voltage boosting circuit having three voltage boosting units;

FIG. 7 shows waveforms for explaining the operation of the circuit of FIG. 6; and

FIG. 8 is a block diagram of the circuitry of an electronic watch using a boosting circuit in accordance with the present invention.

### DESCRIPTION OF PREFERRED EMBODIMENTS:

The present invention relates to a voltage boosting circuit suitable for use in an electronic watch or hand

held calculator and especially to a boosting circuit which is suitable for incorporation integrated circuitry.

FIG. 1 illustrates a two stage voltage boosting circuit in accordance with the invention comprising two boosting units 1 and 2 connected in series. Unit 1 comprises a P type MOS-FET 3 and an N type MOS-FET 4 connected so as to constitute an inverter. The gates of both of the MOS-FETs are connected to an input terminal 13. The source of MOS-FET 3 is connected to a power supply terminal 16. The source of MOS-FET 4 is connected through a connecting point 19 to one terminal of a condenser 6, the other terminal of which is connected to an input terminal 15. The source of the MOS-FET 4 is also connected through the connecting point 19 to the source of an N type MOS-FET 5, the gate of which is connected to the drains of MOS-FETs 3 and 4. The drain of MOS-FET 5 is connected to a voltage supply terminal 14.

The unit 2 comprises a P type MOS-FET 8 and an N type MOS-FET 9 which are connected so as to constitute an inverter. The gates of MOS-FETs 8 and 9 are connected through a connecting point 7 to the drains of MOS-FETs 3 and 4. The source of MOS-FET 8 is connected to the power supply terminal 16. The source of MOS-FET 9 is connected through a connecting point 20 to one terminal of a condenser 11, the other terminal of which is connected to a terminal 18. The source of MOS-FET 9 is also connected through the connecting point 20 to the source of an N type MOS-FET 10, the gate of which is connected through a connecting point 12 to the drains both of MOS-FETs 8 and 9. The drain of MOS-FET 10 is connected to the connecting point 19 of the first boosting unit 1.

Referring now to the connections of each of the terminals 13, 14, 15, 16, 17 and 18, the terminal 13 is a terminal to which an input signal is applied for driving the voltage boosting circuit. Such signal may for example be a divided signal from an oscillating circuit such as is available in a timepiece. Terminal 14 is connected to the low voltage point of a power source while terminals 16 and 18 are connected to the high voltage point of the power source. Terminal 15 is a terminal to which is applied a signal which is 180° out of phase with the signal applied to terminal 13. Terminal 17 is the output terminal of the voltage boosting circuit.

The operation of the voltage boosting circuit shown in FIG. 1 will now be described with reference to FIG. 2 in which the waveforms are designated by the same reference numerals as the respective points of the circuit in FIG. 1.

Assuming that the power source is negative and has a voltage of 1 volt, the voltage of terminals 16 and 18 will be 0 volt and the voltage of terminal 14 will be -1 volt. The voltage of the terminal 17 will be about -1 volt by the charge of condenser 11 through the parasitic diode of N type MOS-FETs 5 and 10. Similarly, the voltage of connecting point 19 will be about -1 volt.

In this condition, when the voltage of input terminal 13 becomes -1 volt and the voltage of input terminal 15 becomes 0 volt, the P type MOS-FET 3 becomes to ON condition provided that its threshold voltage VTP is lower than 1 volt and N type MOS-FET 4 becomes to OFF condition as its source voltage is equal to the gate voltage. Therefore, the voltage of the connecting point 7 common to the drains of MOS-FETs 3 and 4 becomes 0 volt and N type MOS-FET 5 becomes to ON condition provided that its threshold voltage VTN is lower than 1 volt. Moreover, as the voltage of the connecting

point 7 is 0 volt, P type MOS-FET 8 becomes to OFF condition and N type MOS-FET 9 becomes to ON condition. The source and gate voltages of N type MOS-FET 10 are equal to one another whereby MOS-FET 10 becomes to OFF condition.

As the voltage of terminal 15 is 0 volt, the condenser 6 is charged through the N type MOS-FET 5 which is in ON condition. The voltage of the connecting point 19 becomes -1 volt whereby the condenser 6 is given a charge corresponding to a drop of potential of 1 volt.

When the input signals are inverted so that the voltage of terminal 13 becomes 0 volt and the voltage of terminal 15 becomes -1 volt, P type MOS-FET 3 is changed to OFF condition and N type MOS-FET 4 is changed to ON condition. Therefore, the source and gate voltages of N type MOS-FET 5 are equal to one another whereby MOS-FET 5 becomes to OFF condition.

However, the condenser 6 does not suddenly discharge so that the voltage of terminal 19 is dropped to -2 volts when the voltage of terminal 15 is changed to 1 volt. Since MOS-FET 4 is in ON condition, the voltage of the terminal 7 of the first booster unit likewise becomes -2 volts. This causes P type MOS-FET 8 to change to ON condition and N type MOS-FET 9 to change to OFF condition. Therefore, the voltage of the connecting point 12 becomes 0 volt whereby N type MOS-FET 10 becomes to ON condition. Hence, the condenser 11 is charged through N type MOS-FET 10 so that the voltage of connecting point 20 and hence the voltage of terminal 17 becomes lower than -1 volt. At this time the first condenser 6 discharges.

When the input signals are again inverted so that the voltage of the input terminal 13 is -1 volt and the voltage of terminal 15 is 0 volt, the first condenser 6 is again charged and the stored charge is transferred to the second condenser 11.

Upon repetition of the described operations the condenser 11 is solely charged so that a voltage which is twice that of the power source is generated at the output terminal 17. Furthermore, if a load is connected between the terminals 16 and 17, the second condenser 11 is charged by the repeated switching operation in spite of discharge of the condenser 11 by the load so that an output voltage is maintained at a constant level.

According to the present invention, the MOS-FETs of the voltage boosting circuit are easily incorporated in the logic of an integrated circuit employed in an electronic timepiece or a hand held calculator whereby only the condensers need be provided as independent additional elements. Accordingly, the space required by the voltage boosting circuit for an electronic watch or calculator is remarkably reduced as is also the cost. Furthermore, it is possible to obtain more than twice the voltage of the power source by using additional boosting units.

Thus, for example FIG. 3 shows an embodiment of the invention having three voltage boosting units 21, 22 and 23 connected in series with one another. In units 21 and 22 corresponding parts have been designated by the same reference numerals as in FIG. 1. The third voltage boosting unit 23 in like manner comprises MOS-FETs 31, 32 and 33 and a condenser 34. The operation of the embodiment shown in FIG. 3 will be understood from the foregoing explanation of the operation of the embodiment of FIG. 1.

FIG. 4 shows another embodiment of the invention comprising two voltage boosting units 40 and 41. The

first boosting unit 40 comprises a P type MOS-FET 42 as a switching element. The source of P type MOS-FET 42 is connected to a high voltage point 50 of a standard voltage power source. An input pulse  $\phi_1$  is applied to the gate of the P type MOS-FET 42. The gate of an N type MOS-FET 43 is connected to a low voltage point 45 of the standard voltage power source. The drains of MOS-FETs 42 and 43 are connected together and to the gate of an N type MOS-FET 44, the drain of which is connected to the low voltage terminal 45 of the standard voltage power source. The source of N type MOS-FET 43 is connected through a connection point 46 to the source of N type MOS-FET 44 and to one terminal of a condenser 47, the other terminal of which is connected through an inverter 48 to the input of pulse  $\phi_1$ . Thus, an inverted signal of the input pulse  $\phi_1$  is applied to the connecting point 46 through the inverter 48 and the condenser 47.

The second boosting unit 41 has a P type MOS-FET 49 of which the source is connected to the high voltage point 50 of the standard voltage power source. An inverted signal of the input pulse  $\phi_1$  is applied to the gate of P type MOS-FET 49 through the inverter 48. The second boosting unit further comprises an N type MOS-FET 52, the gate of which is connected to the connection point 46 of the first boosting unit. The drains of MOS-FETs 49 and 52 are connected together and to the gate of an N type MOS-FET 51, the drain of which is connected to the connection point 46 of the first boosting unit. The source of N type MOS-FET 52 is connected through a connecting point 55 to the source of N type MOS-FET 51 and to one terminal of a condenser 54, the other terminal of which is connected to the high voltage point 50 of the standard power source. The connecting point 55 is also connected to an output terminal 53.

The operation of the voltage boosting circuit shown in FIG. 4 will now be described with reference to the accompanying waveforms shown in FIG. 5.

An input pulse  $\phi_1$  of the waveform shown in FIG. 5 is applied to the gate electrode of the P type MOS-FET 42 of the first boosting unit 40 and an inverted signal  $\bar{\phi}_1$  is applied by the inverter 48 to the gate of the P type MOS-FET 49 of the second boosting unit 41 and also to the condenser 47. In this condition, if the voltage of high voltage point 50 of the standard power source is 0 volt and the voltage of the low voltage point 45 is -1 volt, the P type MOS-FET 42 becomes to ON condition when the voltage of input pulse  $\phi_1$  is -1 volt. Further, N type MOS-FET 44 becomes to ON condition whereby the voltage of the connecting point 46 becomes -1 volt. At this time, the voltage of the condenser 47 in the output side of the inverter 48 is 0 volt. Thereafter, when the voltage of input pulse  $\phi_1$  is changed to 0 volt, P type MOS-FET 42 changes to OFF condition, the voltage of the connecting point 46 is lowered to -2 volts according to a changed voltage of -1 volt of condenser 47 in the output side of inverter 48. N type MOS-FET 44 becomes to OFF condition and N type MOS-FET 43 becomes to ON condition.

When the voltage of input pulse  $\phi_1$  is changed to -1 volt, P type MOS-FET 42 and N type MOS-FET 44 become to ON condition whereby the voltage of connecting point 46 is changed to -1 volt according to the OFF condition of N type MOS-FET 43. FIG. 5 shows the change of voltage of the connecting point 46 by waveform 46a.



In the second boosting unit 41 when the voltage of the inverted input pulse  $\phi_1$  applied to the gate electrode of P type MOS-FET 49 is -1 volt, P type MOS-FET 49 becomes to ON condition and N type MOS-FET 51 also becomes to ON condition. Therefore, the voltage of the output terminal 53 becomes -2 volts (at this time the voltage of the connecting point 46 is -2 volts). Thereafter, when the voltage of the inverted input pulse  $\phi_1$  becomes 0 volt, P type MOS-FET 49 and N type MOS-FET 51 become to OFF condition and N type MOS-FET 52 becomes to ON condition.

In this condition, no electric power is applied to the output terminal 53. However, the voltage of the output terminal 53 is maintained at -2 volts by the charge of the charged condenser 54. FIG. 5 shows a waveform 53a which represents the voltage of the output terminal 53. It will thus be seen that the voltage is boosted by a factor of 2 by connecting the first boosting unit 40 and the second boosting unit 41 in series.

FIG. 6 shows a further embodiment of a boosting circuit in accordance with the present invention for obtaining a voltage boosted by the factor of 3. The embodiment illustrated in FIG. 6 comprises a first boosting unit 60, a second boosting unit 61 and a third boosting unit 62. The first boosting unit 60 has a P type MOS-FET 63 as a switching element of which the source is connected to a high voltage point 59 of a standard voltage power source. An input pulse  $\phi_1$  is applied to the gate electrode of the P type MOS-FET 63. The first boosting unit 60 further comprises an N type MOS-FET 64, the gate of which is connected to a low voltage point 69 of the standard power source. The drains of MOS-FETs 63 and 64 are connected together and to the gate of an N type MOS-FET 65, the drain of which is connected to the low voltage point 69 of the standard voltage power source. The source of N type MOS-FET 64 is connected through a connecting point 67 to the source of N type MOS-FET 65 and to one terminal of a condenser 66, the other terminal of which is connected through an inverter 68 to the input of the input pulse  $\phi_2$ .

The second voltage boosting unit 61 has a P type MOS-FET 70 as a switching element, the source of which is connected to the high voltage point 59 of the standard voltage power source. The input pulse  $\phi_2$  is applied to the gate electrode of the P type MOS-FET 70 through the inverter 68. The second boosting unit 61 further comprises an N type MOS-FET 72, the gate of which is connected to the connecting point 67 of the first boosting unit 60. The drains of MOS-FETs 70 and 72 are connected together and to the gate of an N type MOS-FET 71, the drain of which is connected to the connecting point 67 of the first boosting unit. The source of N type MOS-FET 72 is connected through a connecting point 73 to the source of the N type MOS-FET 71 and to one terminal of a condenser 76, the other terminal of which is connected through inverters 74 and 75 to the input of input signal  $\phi_2$ . Thus, the input pulse  $\phi_2$  is applied to the connecting point 73 through inverters 74 and 75 and condenser 76.

The third boosting unit 62 similarly to the second boosting unit 61 has a P type MOS-FET 77 as a switching element the source of which is connected to the high voltage point 59 of the standard voltage power source. A pulse signal generated by the inverter 75 is applied to the gate of the P type MOS-FET 77. The third boosting unit 62 further comprises an N type MOS-FET 79, the gate of which is connected to the

connecting point 73 of the second boosting unit. The drains of MOS-FETs 77 and 79 are connected to the gate of an N type MOS-FET 78, the drain of which is connected to the connecting point 73 of the second boosting unit 61. The source of N type MOS-FET 79 is connected through a connecting point 82 to the source of N type MOS-FET 78 and to one terminal of a condenser 81, the other terminal of which is connected to the high voltage point 59 of the standard voltage power source. The connecting point 82 and hence one terminal of the condenser 81 are connected to an output terminal 80.

The operation of the embodiment of the present invention shown in FIG. 6 will now be explained with reference to the accompanying waveforms shown in FIG. 7.

An input pulse  $\phi_2$  as indicated by the waveform  $\phi_2$  in FIG. 7 is applied to the gate of the P type MOS-FET 63 of the first boosting unit 60. A pulse having the same phase as the waveform  $\phi_2$  is applied to the gate electrode of the P type MOS-FET 77 of the third boosting unit 62 and to the condenser 76 of the second boosting unit. An inverted input pulse  $\phi_2$  which is 180° out of phase with the input pulse  $\phi_2$  as indicated by the waveform  $\phi_2$  is applied through the inverter 68 to the gate of P type MOS-FET 70 of the second boosting unit and to the condenser 66 of the first boosting unit.

In this condition, if the voltage of the high voltage point 59 of the standard voltage power source is 0 volt, and if the voltage of the low voltage point 69 of the power source is -1 volt, a signal as indicated by the waveform 67a is generated at the connecting point 67 by the input pulse  $\phi_2$  which is sequentially operated to 0 volt and -1 volt. This signal is applied to the drain electrode of N type MOS-FET 71 and to the gate of N type MOS-FET 72 in the second boosting unit 61. If the voltage of the inverted input pulse  $\phi_2$  is -1 volt, P type MOS-FET 70 becomes to ON condition and N type MOS-FET 71 also becomes to ON condition. At this time, the voltage of the connecting point 67 is -2 volts, whereby the voltage of the connecting point 73 of the second boosting unit is also -2 volts since N type MOS-FET 71 is in ON condition.

When the voltage of the inverted impulse pulse  $\phi_2$  is changed to 0 volt, the P type MOS-FET 70 and N type MOS-FET 71 become to OFF condition and N type MOS-FET 72 changes to ON condition. At this time the voltage of the output of the inverter 75 changes from 0 volt to -1 volt whereby the voltage of the terminal 73 through the condenser 76 changes from -2 volts to -3 volts. The change of voltage of the connecting point 73 is indicated by the waveform 73a in FIG. 7. The voltage change of the connecting point 73 is applied to the drain electrode of N type MOS-FET 78 and to the gate of N type MOS-FET 79 in the third boosting unit 62. If the input pulse  $\phi_2$  applied to the gate electrode of P type MOS-FET 77 is -1 volt, P type MOS-FET 77 becomes to ON condition and N type MOS-FET 78 also becomes to ON condition. A voltage of -3 volts is then generated at the connecting point 73 and is applied to the output terminal 80 through the N type MOS-FET 78 which is in ON condition. The voltage at the output terminal 80 is maintained by the charge on the condenser 81.

Further, when the voltage of the input pulse applied to the P type MOS-FET 77 changes to 0 volt and P type MOS-FET 77 and N type MOS-FET 78 thereby change to OFF condition, the voltage at the output

terminal 80 is maintained at -3 volts, as indicated by the waveform 80a. It is thus possible to obtain a voltage boosted by the factor 3 by connecting the first, second and third boosting units 60, 61 and 62 respectively in series with one another.

FIG. 8 is a block diagram showing the circuitry of an electronic watch having a boosting circuit in accordance with the present invention. The signal produced by an oscillating circuit 90 having a quartz element is divided by a dividing circuit 91 to obtain a 1 Hz standard pulse which is applied to a level shifter 92. A divided signal generated from a selected one of the dividing steps of the dividing circuit 91 is applied to a boosting circuit 96 as an input pulse. The boosting circuit 96 generates a voltage which is three times the standard voltage. This boosted voltage is applied to the level shifter 92, a time measuring device 93, a driving circuit 94 and a display device 95. The level shifter 92 shifts the level of the standard pulse from the dividing circuit 91 and applies it to the time measuring device 93. The time measuring device 93 generates a counting signal corresponding to the time and applies the counting signal to the driving circuit 94 after changing the counting signal to a selected code for operating the display device 95, for example a digital display device in which the digits are composed in known manner of seven segments. The driving circuit 94 amplifies the signal and applies it to the display device 95.

As will be understood by those skilled in the art, many variations and modifications of the embodiments illustrated by way of example in the drawings may be made and hence the invention is in no way limited to these embodiments.

According to the invention, the boosting circuit is composed of a plurality of boosting units, each comprised of MOS-FETs and a condenser, whereby it is possible to obtain a smaller boosting unit than with a conventional boosting unit having diodes. Furthermore, it is possible to mount the boosting unit on the same chip with other circuitry. As the voltage of the commonly connected source electrodes of the first and second MOS-FETs of one unit is employed as the standard voltage of the next boosting unit, it is possible easily to obtain a desired boosting magnification by connecting a plurality of the boosting units in sequence with each other.

What I claim is:

1. A voltage boosting circuit comprising a plurality of boosting units connected in series, each of said units comprising a condenser and an MOS-FET, said MOS-FET of a first unit being connected between one terminal of said condenser and one terminal of a power source so as to connect said terminal with said power source when said MOS-FET is conductive and said MOS-FET of a succeeding unit being connected between said terminal of said condenser of the preceding unit and one terminal of said condenser of said succeeding unit so as to connect said terminals of said condenser when said MOS-FET is conductive, and means for switching said MOS-FET, said switching means of each said unit comprising a second MOS-FET having a source connected to the opposite terminal of said power source, a third MOS-FET having a source connected to the source of said first mentioned MOS-FET and to one terminal of said condenser, means connecting the drains of said second and third MOS-FETs to the gate of said first mentioned MOS-FET and means for applying a

pulse signal to the gates of said second and third MOS-FETs.

2. A voltage boosting circuit according to claim 1, further comprising means for applying to the other terminal of said condenser a pulse signal which is 180° out of phase with said first mentioned pulse signal.

3. A voltage boosting circuit comprising a plurality of boosting units connected in series, each of said units comprising a condenser and an N type MOS-FET,

said MOS-FET of a first unit being connected between one terminal of said condenser and the low voltage point of a power source so as to connect said terminal with said power source when said MOS-FET is conductive, and

said MOS-FET of a succeeding unit being connected between said terminal of said condenser of the preceding unit and one terminal of said condenser of said succeeding unit so as to connect said terminals of said condenser when said MOS-FET is conductive, and

means for switching said MOS-FET of each unit, said switching means comprises a second MOS-FET having a source connected with the high voltage point of said power source, a third MOS-FET having a source connected to the source of said first mentioned MOS-FET and to one terminal of said condenser, means connecting the drains of said second and third MOS-FETs to the gate of said first mentioned MOS-FET, means for applying a signal pulse to the gate of said second MOS-FET, and means for connecting the gate of said third MOS-FET and the drain of said first mentioned MOS-FET to the low voltage point of said power source.

4. A voltage boosting circuit according to claim 3, in which said signal pulse applying means includes means for applying signals of opposite phase to the gates of said second MOS-FETs of successive units in said series.

5. A voltage boosting circuit according to claim 4, which comprises three of said units connected in series.

6. A voltage boosting circuit for an electric watch comprising in combination:

a first voltage boosting unit comprising a first switching means composed of P and N types FETs, a second switching means controlled by an output of said first switching means, a first condenser having one terminal connected to at least said second switching means, a first input terminal connected to said first switching means and having a first clock signal applied thereto, a second input terminal connected to said second switching means and having a DC power source applied thereto, and a third input terminal connected to the other terminal of said condenser and having a second clock signal with a phase difference of 180° from said first clock signal applied thereto,

a second voltage boosting unit comprising a third switching means composed of P and N types, FETs, a fourth switching means controlled by an output of said third switching means, a second condenser having one terminal connected to at least said fourth switching means, means for applying a third clock signal to said third switching means, means connecting said fourth switching means with a connecting point between said second switching means and said one terminal of said first condenser, means connecting the other terminal of

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said second condenser and a booster output terminal connected with a connecting point between said fourth switching means and said second condenser,

an electric charge kept in said first condenser of said first voltage boosting unit being transferred to said second condenser when said second switching means is turned OFF and said fourth switching means is turned ON, whereby a DC voltage is obtained at said output terminal which is at least twice that of the input DC power source.

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7. A voltage boosting circuit according to claim 6, in which one terminal of said first switching means in said first voltage boosting unit is connected to a connecting point between said first condenser and said second switching means, one terminal of said third switching means in said second voltage boosting unit is connected to one terminal of said first switching means, and another terminal of said third switching means is connected to a connecting point between said fourth switching means and said second condenser.

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## [54] VOLTAGE MULTIPLIER FOR AN ELECTRONIC TIME APPARATUS

[75] Inventor: Hubert Portmann, Colombier, Switzerland

[73] Assignee: Ebauches S.A., Neuchâgel, Switzerland

[21] Appl. No.: 702,490

[22] Filed: July 6, 1976

### [30] Foreign Application Priority Data

Aug. 14, 1975 Switzerland ..... 10575/75

[51] Int. Cl.<sup>2</sup> ..... H02M 7/25; G04C 3/00

[52] U.S. Cl. .... 363/60; 58/23 BA; 363/147

[58] Field of Search ..... 321/15; 58/23 R, 23 BA, 58/50 A; 307/110; 363/60, 61, 147

### [56] References Cited

#### U.S. PATENT DOCUMENTS

3,790,812	2/1974	Fry	321/15
3,824,447	7/1974	Kuwabara	307/110
3,944,908	3/1976	Oki	321/15
4,001,664	1/1977	Hyltin	321/15
4,015,420	4/1977	Walker	58/23 BA

#### FOREIGN PATENT DOCUMENTS

2,530,870 2/1976 Germany ..... 58/23 BA

### OTHER PUBLICATIONS

IEEE Journal of Solid-State Circuits, vol. SC-11, No. 3, pp. 374-378, June 1976.

Primary Examiner—William H. Beha, Jr.  
Attorney, Agent, or Firm—Imirie, Smiley & Guay

### [57] ABSTRACT

A voltage multiplier for an electronic time-measuring apparatus comprising cells, each of which including two capacitors, a pair of complementary field-effect transistors (FET'S) acting as switches, and an inverter comprising a pair of FET'S. The elements of the cells are such that they are capable of being integrated together with the rest of the circuit of the time-measuring apparatus.

The voltage to be increased is fed via a first capacitor to the first pair of FET'S and at the same time to the input of the inverter whose output drives with the correct phase the first pair of FET'S, which alternatively switches the input signal to a common point of the cell and to an output terminal of the cell, thus charging a second capacitor with the opposite polarity than that of the input signal respective to the common point of the cell. In order for the input voltage to be further increased, the cells can be cascaded in a chain, the common point of one cell being connected to the output terminal of the preceding cell. Each cell will add to the preceding one an amount of voltage equal to that of the input voltage.

5 Claims, 9 Drawing Figures

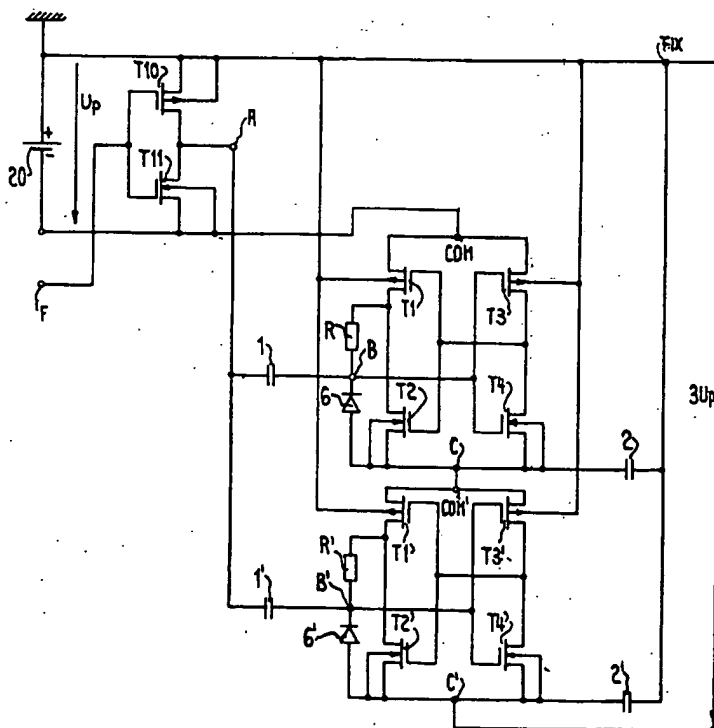


FIG. 1 PRIOR ART

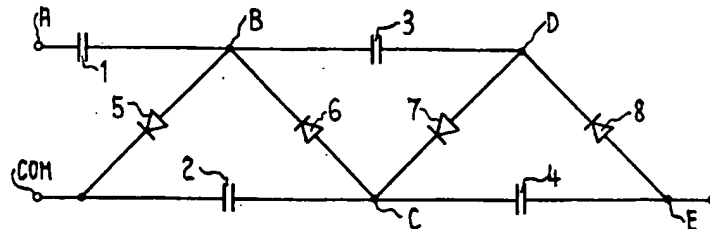


FIG. 2

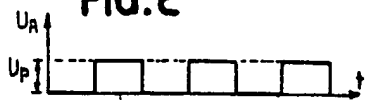


FIG. 3



FIG. 4

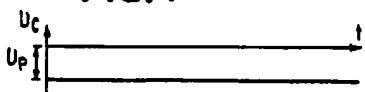


FIG. 5

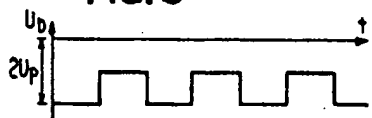


FIG. 6

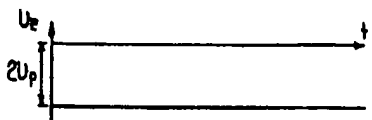


FIG. 7

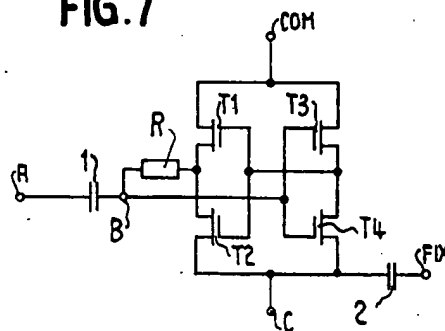


FIG. 8

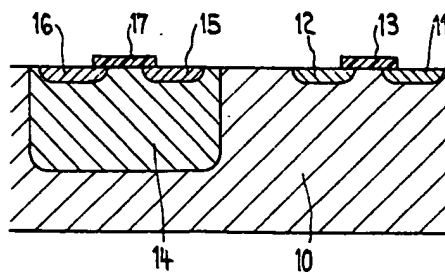
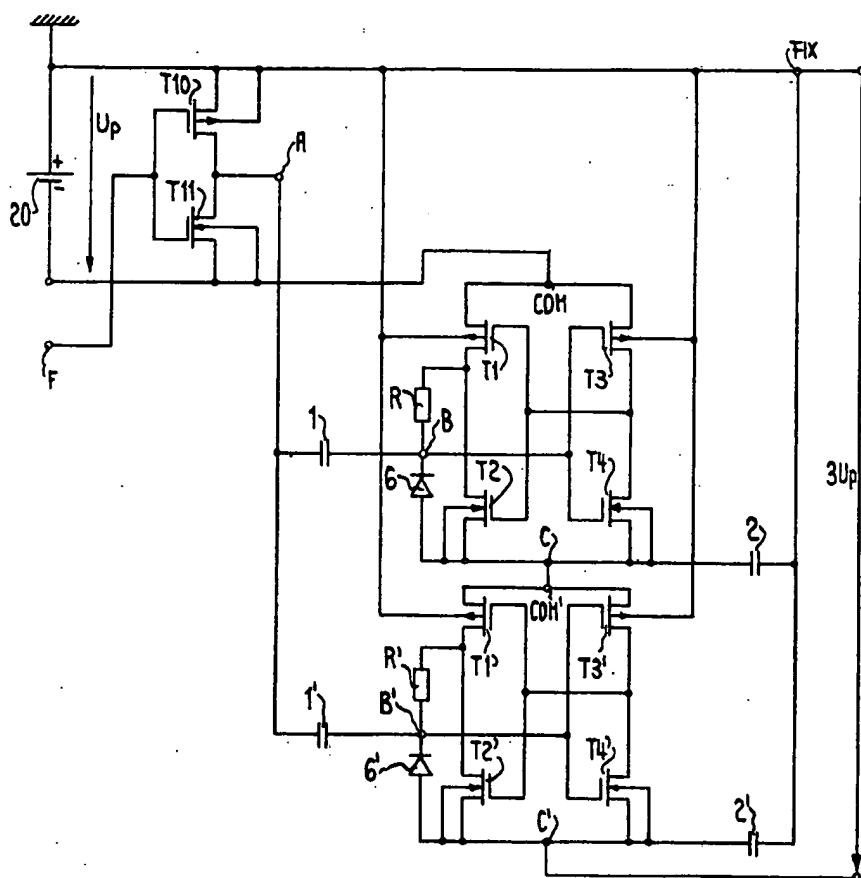


FIG. 9



# VOLTAGE MULTIPLIER FOR AN ELECTRONIC TIME APPARATUS

The present invention relates to a voltage multiplier for electronic time apparatus.

Entirely electronic watches (called "solid-state") need, for feeding their display, a voltage which is greater than the cell voltage. There are known and presently used voltage converters in the form of transformers or of simple inductances. The use of these elements presents certain disadvantages the transformer is a relatively large and particularly expensive element, the number of its outputs is high and its magnetic circuit must be well shielded so as not to disturb the rest of the circuit. The use of an inductance, on the other hand, necessitates an adjustment of the output voltage and it is then necessary to find a Zener diode having the correct characteristics or alternatively it is necessary to adjust a resistance.

The invention has for its object to seek to provide a voltage multiplier device precluding the above-mentioned faults. Its power level must be of the order of microwatts, its output voltage must be very stable and little dependent of the charge at its output. The elements of which it is composed, finally, should be capable of being made by means of the same fabrication technique as the rest of the circuit of the time apparatus. The time circuit and the multiplier should thus be capable of being integrated together on the same base.

According to the present invention there is provided a voltage multiplier for an electronic time apparatus comprising at least one cell including a first capacitor transmitting an input signal to two complimentary field effect transistors which transmit the input signal alternatively to a common point of the cell and to an output terminal of the cell, the said transistors being controlled by a reverser also controlled by the signal transmitted to the transistors and fed by the voltage appearing at the common point and at the output terminal of the cell, a second capacitor being connected between the output terminal and a stable voltage point.

The present invention will be described further, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a diagram illustrating the configuration of a known voltage converter;

FIGS. 2-6 are diagrams illustrating the functioning of the device shown in FIG. 1;

FIG. 7 shows a cell of a voltage multiplier in accordance with the present invention;

FIG. 8 shows schematically, in section, the construction of the transistors used in the voltage multiplier of the invention; and

FIG. 9 is a diagram of a voltage multiplier in accordance with the present invention.

FIG. 1 shows a voltage converter using capacitors 1 to 4 and diodes 5 to 8. The particular connection of the capacitors and diodes enables a continuous voltage to be obtained at an output E which voltage has an amplitude greater than the amplitude of the pulses arriving at an input point A. FIGS. 2 to 6 show voltage waveforms  $U_A$ ,  $U_B$ ,  $U_C$ ,  $U_D$ , and  $U_E$  at the points A, B, C, D and E of the circuit of FIG. 1. The point COM is a reference point. At the input A of the circuit a series of pulses of amplitude  $U_p$  are supplied and at the points B and D situated to the right of capacitors 1 and 3, respectively, rectangular signals appear having an amplitude  $U_p$

displaced by a continuous voltage  $U_p$  with respect to the preceding point. At the points C and E situated on the right of capacitors 2 and 4 continuous voltages appear the size of which is a whole multiple of the value  $U_p$ .

The chain can be enlarged at will with cells formed by two capacitors and two diodes. This circuit however only has a real practical value when one can neglect the voltage drops across the diodes relative to the value  $U_p$ . In watches, the rectangular pulse signal has its amplitude limited by the feed voltage (battery voltage) which is in the region of 1.5 volts, whilst the voltage drop across a diode is of the order of 0.5 Volts, which is thus far from being negligible.

The diagrams of FIGS. 2 to 6 are only valid if the capacitors have capacitance values which are sufficiently high so that the charging and discharging currents to which they are subjected at the frequency of the input signal does not noticeably modify their state of charge and thus their voltage.

In this case the voltages at the points A, B and C are only distinguished from each other by their continuous levels. It is thus possible to connect in the capacitors 1 and 3 between the point A and the points B and D respectively. Similarly, the voltages at the points COM, C and E only differ by their continuous components and it is possible to connect their capacitors 2 and 4 between the point COM and the points C and E respectively. Since the point COM is at a constant voltage it is equally possible to connect the capacitors at any other point itself having a constant potential and only being displaced from the potential at point COM by a continuous component, in particular one or other terminal of the battery.

Considering the example of FIG. 1 and the first cell comprised of the capacitors 1 and 2 and diodes 5 and 6, the point C shows a continuous negative voltage of value  $U_p$  with respect to the point COM. If the point COM is connected to the negative terminal of the battery, the point C shows a continuous negative voltage of value  $2U_p$  with respect to the positive terminal of the battery (which is found to be generally the earth of the circuit). It is clear that one can reverse the polarity of the output voltage by changing the polarities of the diodes and by connecting the point COM to the positive terminal of the battery. On the other hand, it is not essential that the capacitor 2 be connected to the point COM, it can be connected to any point at all having a fixed voltage and a small impedance (FIX). During the positive half of the input signal ( $U_p$ ) the diode 5 conducts a current which charges the capacitor 1 (in FIG. 1, positive to the left, negative to the right). During the negative half (or zero), the capacitor 1 partially discharges across the diode 6, which charges the capacitor 2. After several cycles, if the capacitor 1 does not discharge too much, the potentials indicated in FIGS. 3 and 4 will have been attained. The voltage drops on the diodes will cause (voltage of battery: 1.5 Volts and a drop on the diodes: 0.5 Volts) a loss of more than 30% with respect to a theoretical value. To avoid this inconvenience, the diodes should be replaced by active elements controlled at the correct frequency.

In the active circuit of FIG. 7, the capacitors 1 and 2 remain; the diodes 5 and 6 of FIG. 1 on the other hand have been replaced by transistors T1 and T2 respectively. The transistor T1 must be conductive during the positive half of the input signal at A, whilst T2 must conduct during the negative half of the input signal  $U_p$ .

With regard to the voltages at the points B, C and COM, the transistor T1 must conduct when its source and its drain are found at the most positive voltage of the device. It is convenient thus to choose a p-channel field effect transistor (FET) for T1 because p-channel FET's conduct when their control electrodes are polarised negatively with respect to their two other electrodes. Thus one can work with the voltage levels available in the system, the voltage at the point C being sufficiently negative with respect to B and COM in the time interval considered. It is equally easy to block the transistor T1 with a potential corresponding to the point COM, no other electrode of T1 being connected to a more positive voltage, which ensures its blockage. A similar reasoning indicates that T2 is, preferably, an n-channel field effect transistor. It follows that the control electrodes of T1 and T2 can be controlled by the same signal, their complimentary character ensuring that conduction of only one transistor at a time. However, since the signal at the point B has correct voltage levels for controlling T1 and T2 but the incorrect phase, it is necessary to pass the signal through a reverser made with the complimentary transistors T3 and T4 for producing a control signal having the correct phase. This reverser must be fed by the levels of the points COM and C to function correctly.

Presuming that the input voltage at the point A passes from its most positive level to its most negative level, the transistor T1 will conduct until the voltage is sufficiently lowered so that the reverser T3, T4 changes state. From this moment only the transistor T1 will be blocked. Thus, the capacitor 1, which was charged, has a tendency to discharge, i.e. its charge will follow the input signal as long as the transistor T1 will conduct. In a similar manner, when the reverser switches over, the transistor T2 conducts and has a tendency to discharge the capacitor 2 into the capacitor 1, given that the voltage on the capacitor 2 is, at this moment, even greater than the sum of the input voltage and the voltage on the capacitor 1. Moreover, it is only when the input voltage has attained its ultimate most negative value that the transistor T2 should itself conduct. The problem is similar when the voltage at the input passes from its most negative level to its most positive level, the transistor T2 remains conductive too long and the transistor T1 starts to conduct too soon. The switching transistors T1 and T2 thus oppose the changing of the voltage controlled by the input. To palliate this inconvenience, the switching transistors T1, T2 are provided having small dimensions with respect to the transistors of the input stage (not shown) which furnishes the input signal  $U_A$ . The signal  $U_A$  then maintains very rigid pulse edges, in spite of the charge which represents the transistors T1 and T2. The earlier mentioned phenomenon is then of a sufficiently short duration to be of no consequence. One can also, as can be seen in FIG. 7, put a resistance R between the point B and the transistors T1 and T2 to largely reduce the influence of the transistors T1 and T2 during the switching over.

It is also sought to resolve the problem posed by the polarisation of the substrate and the cases containing the field effect transistors forming the circuit. The field effect transistor has four inputs, namely: the three conventional electrodes: drain, source and gate, and an electrode contacting the substrate, or the case in which they are located. In the "C-MOS" (complimentary-MOS) technique both types of transistors are provided on the same substrate. As shown in FIG. 8, in the nega-

tively doped sub-strate 10, there is provided a p-channel transistor by diffusing into this substrate two positively doped layers 11 and 12 adapted to form respectively the source and the drain and on the substrate between the two layers 11 and 12, an insulating layer of  $\text{SiO}_2$  13 is applied adapted to receive the control electrode of the transistor, i.e. the gate. To make an n-channel transistor, a positively doped region 14 is buried in the substrate 10 into which region 14 negatively doped layers 15 and 16 are diffused and an insulating layer 17 is applied which receive the drain, source and gate electrodes of the transistor. The negatively doped substrate 10 must be connected to a terminal having a voltage which is sufficiently positive with respect to the source and drain electrodes of the p-channel transistors. For the positively doped regions, their voltages must be sufficiently negative with respect to the respective electrodes of the n-channel transistors.

FIG. 9 shows a multiplier composed of two cells. There is shown the battery 20 with an indication of its polarity. There is also shown the final stage of the device controlling the converter and which is composed of two transistors T10, T11 forming a reverser fed by a signal F derived from a timer circuit. The transistors represented in this diagram include, additional to the three conventional electrodes, a fourth electrode which contacts either the substrate or the casing of the transistor. This electrode is shown with an arrow in the drawing, an ingoing arrow is indicative of an n-channel transistor, an outgoing arrow of a p-channel transistor. The substrate of all the p-channel transistors is connected to the positive terminal of the battery. The casings of the n-channel transistors are directly connected to the sources of their respective transistors. In effect, the substrate, common to all the p-channel transistors, must be placed at the most positive possible voltage, it is then easy to connect it to the positive terminal of the battery which, in this instance, is connected to earth for the whole circuit. For the casings of the n-channel transistors, each transistor can have its own casing if necessary and this must be at a sufficiently negative voltage with respect to the drain and source electrodes of the or each transistor which it houses. It suffices to connect the casing directly to the respective sources of the transistors. It is preferable not to connect all the casings to the most negative voltage of the circuit, as the threshold voltage of the n-channel transistors depends greatly on the polarisation of the casings, if this polarisation is too great, the threshold voltage increases uselessly. In the solution adopted and illustrated in FIG. 9, the polarisation of the casing being small, the threshold voltage becomes independent of the voltage level. Thus, the n-channel transistors are grouped in boxes which are just sufficiently polarised so that the source or drain are never negative with respect to the casing.

The first cell is composed of transistors T1, T2, T3, T4, a resistance R and two capacitors 1 and 2. It also includes a diode 6 connected between points C and B. The second cell is composed of transistors T1', T2', T3' and T4', a resistance R' and two capacitors 3 and 4, a diode 6' connected between points E (output) and D. The diodes 6 and 6' (similarly to FIG. 1) ensure a correct starting of the multiplier when the output voltage is nil.

The voltage of the battery being  $U_A$ , the output voltage is, theoretically,  $3 U_A$ . Two tables, shown below, give the results obtained with two types of multipliers, for different output currents and the following values:



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frequency of control pulses: 250 Hz  
voltage of battery  $U_p = 2.5$  V.

Doubling (a single cell) with $C_1 = C_2 = 0.15 \mu F^*$		
output voltage (V)	output current ( $\mu A$ )	yield (%)
5	0	0
4.97	0.5	90
4.7	5	93

\* $C_1, C_2$  = value of the capacitors 1,2

Quadrupling (three cells) with $C_1 = C_2 = \dots = 100$ nF		
output voltage (V)	output current ( $\mu A$ )	yield (%)
9.7	0	0
9	0.1	75
8	1	78

In the first case, the stability and the yield are very high, in the second, the two characteristics depend obviously on the quality of the transistors used.

In so far as concerns the value of the frequency of the input pulses, it is to be noted that this is a compromise dictated by the dimensions of the capacitors on the one hand (preferring a high frequency) and the losses due to the stray capacitances (preferring a low frequency).

One can see that the choice of MOS transistors presents appreciable advantages: there is a compatibility between the multiplier and the "C-MOS" logic of the time circuit, the losses of voltage are negligible in view of the lack of "offset" voltage of the field effect transistors, the problems of dissipation of energy in the control of the transistors do not exist, being given that the input impedance of these transistors is almost infinite.

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I claim:

1. A voltage multiplier for an electronic time apparatus comprising, at least one cell, including two complementary field effect transistors, a first capacitor, said first capacitor transmitting an input signal to said two complementary field effect transistors, said transistors transmitting the input signal alternatively to a common point of the cell and to an output terminal of the cell, a reverser, said transistors being controlled by said reverser, said reverser also being controlled by the signal transmitted to the transistors by said first capacitor and fed by voltages appearing at the common point and at the output terminal of the cell, a second capacitor being connected between the output terminal and a stable voltage point of the cell.

2. A multiplier in accordance with claim 1, in which the transistors of the multiplier are of small dimensions with respect to external transistors providing the input signal.

3. A multiplier in accordance with claim 1, in which a resistance is connected between the first capacitor and the two transistors of the cell.

4. A multiplier in accordance with claim 1, in which the stable voltage point of the cell is one of the terminals of a battery for supplying the time apparatus and the output voltage of the multiplier is taken between the output terminal of the cell and a terminal of the battery.

5. A multiplier in accordance with claim 1, in which several cells are connected in cascade, so that the common point of one cell is connected to the output terminal of the preceding cell, the inputs of each of the cells being common and the stable voltage points of each of the cells being common.

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# United States Patent [19]

Holbrook et al.

[11] 4,106,086

[45] Aug. 8, 1978

## [54] VOLTAGE MULTIPLIER CIRCUIT

[75] Inventors: Mark Denton Holbrook, Belle Mead;  
Richard Plumb Fillmore, Plainfield,  
both of N.J.

[73] Assignee: RCA Corporation, New York, N.Y.

[21] Appl. No.: 755,612

[22] Filed: Dec. 29, 1976

[51] Int. Cl.<sup>2</sup> ..... H02M 7/00

[52] U.S. Cl. .... 363/60

[58] Field of Search ..... 307/110; 363/59, 60,  
363/61

## [56] References Cited

### U.S. PATENT DOCUMENTS

3,942,047	3/1976	Buchanan	363/60 X
4,001,664	1/1977	Hyltin	363/59
4,053,821	10/1977	Hose, Jr. et al.	363/60

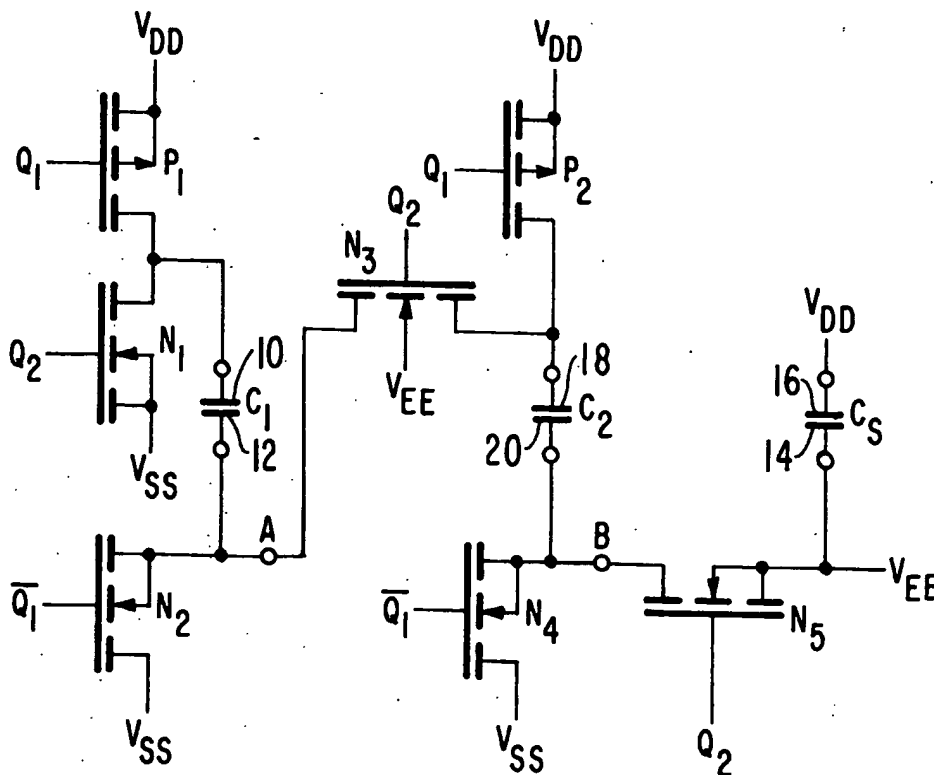
Primary Examiner—William M. Shoop

Attorney, Agent, or Firm—H. Christoffersen; A. L.  
Limberg

## [57] ABSTRACT

A voltage multiplying circuit comprising a plurality of booster capacitors and switch means for first connecting the capacitors in parallel with a voltage source to charge, then reconnecting the capacitors in series with the source and in parallel with a storage capacitor, to dump the cumulative voltage into the storage capacitor, is characterized in that control signals for actuating the switch means are phased to forestall the formation of a path for leakage current that undesirably discharges the capacitors and reduces the conversion efficiency of the voltage multiplying circuit.

1 Claim, 6 Drawing Figures



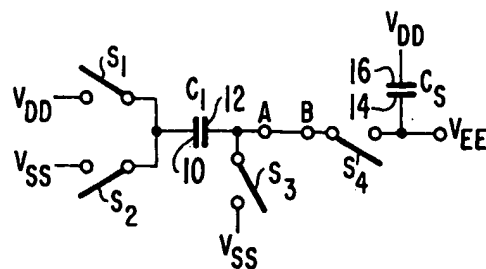


Fig. 1.

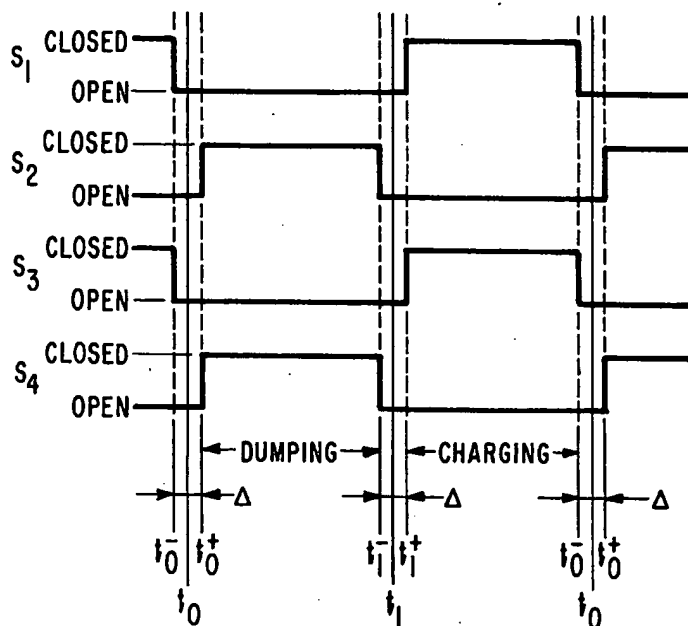


Fig. 2.

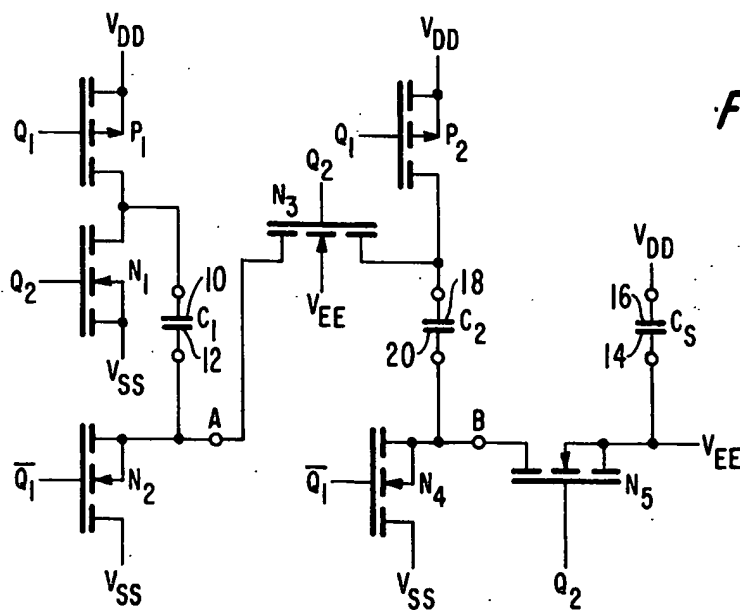


Fig. 3.

Fig. 4.

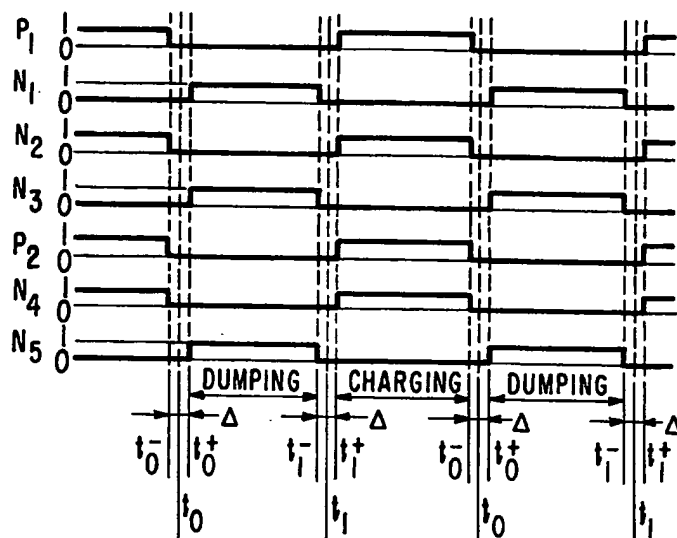


Fig. 5.

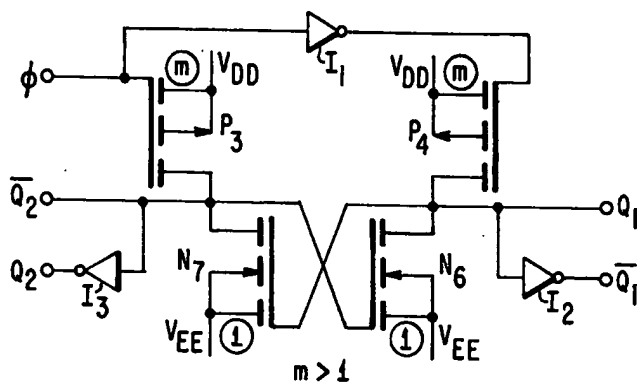
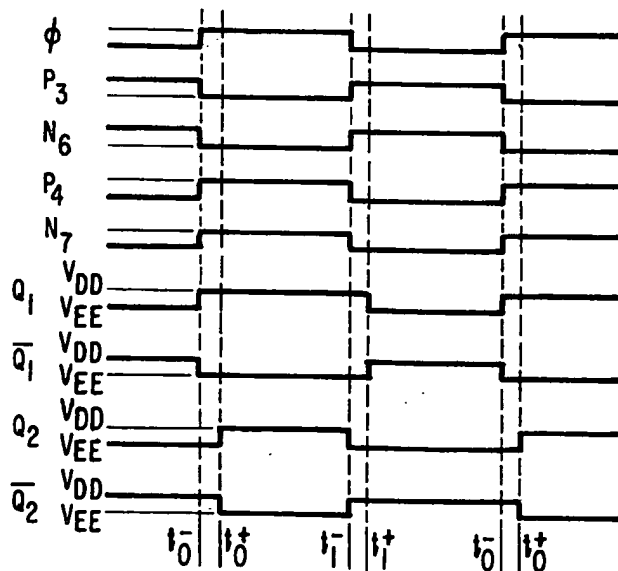


Fig. 6.



## VOLTAGE MULTIPLIER CIRCUIT

The present invention relates to an improvement in voltage multiplying circuits. The voltage multiplying circuits of concern are of the following type. At least one "booster" capacitor is cyclically connected in parallel with a voltage source for charging during a "charging" portion of the operating cycle, and then during a "dumping" portion of the operating cycle switched into a series connection with the input voltage source across a storage capacitor. Since the potential across each booster capacitor cannot change instantaneously after switching the booster capacitor serves as an additional voltage source in its serial connection with the original voltage source, augmenting or "boosting" the potential applied to the storage capacitor. Charge is transferred to the storage capacitor ideally to charge it to —neglecting losses and other voltages reducing effects to be described—a multiple of the potential supplied by the input voltage source and thereafter to keep it charged to that level. The storage capacitor continually supplies the multiplied potential to further circuitry and its charge must be replenished to make up for the current consumed by this further circuitry. This type of voltage multiplier has been described in U.S. Pat. No. 3,824,447 issued July 16, 1974 to T. Kuwabara and entitled "Booster Circuit"; U.S. Pat. No. 3,790,812 issued Feb. 5, 1974 to P. Fry and entitled "Device For Generating A High Voltage Supply" and in copending application Ser. No. 578,913 "Voltage Amplitude Multiplying Circuits" filed May 19, 1975 by B. D. Rosenthal and A. Dingwall and assigned like the present application to RCA Corporation.

Various prior art voltage multiplying circuits utilize unidirectionally conducting elements, such as diodes, or transistors connected like diodes, in the switching means. The forward potential drops across each unidirectional conducting element undesirably interferes with the charging of the capacitors to a full multiple of source potential and decreases the output voltage available from the voltage multiplying circuit to a value somewhat smaller than the desired multiple of input voltage. Such decreases become appreciable where the supply voltage is small, for example, on the order of 1.5 volts, in that the forward potential drops across the unidirectionally conductive elements are typically on the order of 0.5–0.7 volts.

To avoid this problem, circuits utilizing switch means consisting of transistors have been developed and are described, for example, by Rosenthal and Dingwall in the above-mentioned application Ser. No. 578,913. While such transistor circuits avoid the forward voltage drop problems associated with circuits utilizing unidirectional elements, the present inventors have noted that spurious discharge of capacitors can occur during the operation of the transistor switch means, decreasing the output voltage of the circuit below its ideal value.

The present invention provides a voltage multiplying circuit wherein suitably phasing the operation of the respective switches in the circuit forestalls the occurrence of a leakage path permitting discharge of the capacitor that undesirably lowers multiplied voltage output and reduces conversion efficiency of the voltage multiplied circuit.

In the drawing:

FIG. 1 is a schematic diagram of a voltage multiplying circuit;

FIG. 2 is a diagram of the conduction states of the various switches of the circuit of FIG. 1 in timed relation according to the teaching of the present invention;

FIG. 3 is a schematic diagram of a FET voltage tripler;

FIG. 4 is a diagram of the conduction states of the various transistors of FIG. 3 as controlled in accordance with the present invention;

FIG. 5 is a schematic diagram of one embodiment of a circuit for providing control signals in accordance with the present invention;

FIG. 6 is a diagram of the conduction states of the transistors of the circuit of FIG. 5 and waveforms of the control signals generated thereby.

Referring to FIG. 1, an input voltage source, not shown, supplies the relatively positive potential  $V_{DD}$  and the relatively negative potential  $V_{SS}$ . The voltage multiplying circuit shown in FIG. 1 generates a negative output voltage  $V_{EE}$  approximately twice as negative with respect to  $V_{DD}$  and  $V_{SS}$ . Switch means  $S_1$  and  $S_2$  selectively connect a first plate 10 of a booster capacitor  $C_1$  to the positive and negative potentials  $V_{DD}$  and  $V_{SS}$ , respectively. The second plate 12 of capacitor  $C_1$  is selectively connected through a switch means  $S_3$  to the negative potential  $V_{SS}$  and through a switch means  $S_4$  to one plate 14 of a storage capacitor  $C_S$ . The other plate 16 of capacitor  $C_S$  is connected to positive potential  $V_{DD}$ . The voltage at plate 14 of capacitor  $C_S$  is taken as the output voltage  $V_{EE}$ .

In general, the circuit of FIG. 1 operates in a cyclical fashion, alternating between a charging mode of operation and dumping mode. In the charging mode, switch means  $S_1$  and  $S_3$  are closed and switch means  $S_2$  and  $S_4$  are open, applying  $V_{DD}$  and  $V_{SS}$  to plates 10 and 12, respectively, of  $C_1$ —in effect paralleling  $C_1$  with the input signal source supplying  $V_{SS}$  and  $V_{DD}$ . Booster capacitor  $C_1$  is perforce charged such that a potential equal to  $V_{DD}$  appears at plate 10 and  $V_{SS}$  at plate 12. In the dumping mode, switch means  $S_1$  and  $S_3$  are open and switch means  $S_2$  and  $S_4$  are closed to connect plate 10 of capacitor  $C_1$  to the negative potential  $V_{SS}$  tending to boost the potential at plate 12 of capacitor  $C_1$  to  $2V_{SS}$ . The connection of plate 12 of  $C_1$  and of plate 14 of  $C_S$  permits charge to be transferred to  $C_S$  to bring both plates to a potential  $V_{EE}$  approaching  $2V_{SS}$ .

In the prior art, switch means  $S_1$  through  $S_4$  have been responsive to a single control signal, or to control signals having essentially simultaneous transitions. The present inventors have noted that such operation is disadvantageous in that all of the switch means may be momentarily conductive during the transitions providing a path for a leakage current that undesirably discharge the capacitors. For example, the output voltage of the FIG. 1 circuit is undesirably decreased by discharge of capacitors  $C_1$  and  $C_S$  through paths provided by concurrent conduction through switch means  $S_2$  and  $S_3$ , and switch means  $S_3$  and  $S_4$ , respectively. This flow of leakage current entails the consumption of energy, which is lost to the circuitry for utilizing  $V_{EE}$  and reduces the conversion efficiency of the voltage multiplying circuit. High conversion efficiency is of particular importance in applications demanding low power consumption such as battery powered liquid crystal display watches.

In accordance with one aspect of the present invention, the conversion efficiency of the voltage multiplier circuit is improved by controlling switch means  $S_1$  through  $S_4$  to effect two-step transitions between oper-

ational modes including an intermediate switching condition wherein all of the switch means are non-conductive. More specifically, in any operational mode transition, the following occurs: (1) all conductive switch means are rendered non-conductive to effect the intermediate switching condition; and (2) the initially non-conductive switch means are then rendered conductive. Referring to FIG. 2, in the prior art, transitions from the charging to dumping mode occur at repetitive times  $t_0$ , and transitions from the dumping mode to the charging mode occur at times  $t_1$ , with changes in the conductive states of the switch means occurring simultaneously at such times. However, in accordance with the present invention, assuming the circuit to initially be a charging mode with switch means  $S_1$  and  $S_3$  conductive and  $S_2$  and  $S_4$  non-conductive, control signals are generated to open switch means  $S_1$  and  $S_3$  at an instant  $t_0^-$  slightly before time  $t_0$ , and further control signals are generated to close switch means  $S_2$  and  $S_4$  at an instant  $t_0^+$  slightly after  $t_0$ . Thus, an intermediate switching condition  $\Delta$  wherein all the switch means  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  are non-conductive is interposed between the charging and dumping conditions. Similarly, in the transition from the dumping mode to the charging mode at time  $t_1$ , switch means  $S_2$  and  $S_4$  are opened at time  $t_1^-$  an instant before time  $t_1$ , and switch means  $S_1$  and  $S_3$  are closed at a time  $t_1^+$  an instant after  $t_1$ , to effect a two-step operational mode transition. Thus, switch means  $S_1$  and  $S_3$  are never concurrently closed with switch means  $S_2$  and  $S_4$ , which forestalls the establishment of a leakage path through which an unwanted discharge of capacitors  $C_1$  and  $C_2$  can take place.

Referring again to FIG. 1, output voltage  $V_{EF}$  can be made a larger multiple of  $V_{SS}$  by breaking the connection between points A and B in the circuit and inserting therebetween further stages. Such stages comprise switch means analogous to switch means  $S_1$ ,  $S_2$  and  $S_3$  and booster capacitors analogous to booster capacitor  $C_1$ , except with the switch means corresponding to  $S_2$  connecting the capacitor to point A of the preceeding stage, rather than to negative potential  $V_{SS}$ . The juncture between the further stage capacitor and the switch means corresponding to  $S_3$  is connected to point B, or is utilized as a "point A" and connected to the switch means corresponding to  $S_2$  in a succeeding further stage. The switch means of the additional stages are operated in synchronism with their respective corresponding switch means  $S_1$ ,  $S_2$  or  $S_3$  in the first stage.

Switch means  $S_1$  through  $S_4$  and any switches used in additional stages, may be any electronically controlled switch means such as, for example, insulated-gate-field-effect transistors (IGFET's) of the enhancement or depletion type formed in bulk silicon, bipolar transistors, or transistors formed on an insulator substrate. A voltage tripler utilizing enhancement type IGFET's is shown in FIG. 3. Like reference characters in FIG. 1 and 3 denote like components. Transistors of P-conductivity type are formed in an N substrate, and are identified in the drawing by the letter P followed by a reference numeral. Transistors of N conductivity type are formed in P-wells diffused into the N-substrate, and are identified by the letter N followed by a reference numeral. In general, the respective substrates of P-conductivity type and N-conductivity type transistors should be connected to potentials, greater than or equal to the most positive and less than or equal to the most negative potentials, respectively, applied to the source or drain of the particular transistor. As is well known, IGFET's

have first and second electrodes, termed source and drain, which define the ends of a conduction path, the conductivity of which is controlled by the potential applied to a control electrode, the gate. It should be appreciated that the respective first and second electrodes may exchange operations as the source or drain. The source electrode is defined as the first or second electrode having, in a P-type IGFET, the highest potential, and in an N-type IGFET the lowest potential, applied thereto. For conduction to occur the applied gate-to-source potential ( $V_{GS}$ ) must be in a direction to forward bias the gate with respect to the source and must be greater in magnitude than the threshold voltage ( $V_T$ ) of the transistor. In the circuit of FIG. 3, transistor  $P_1$  serves as switch means  $S_1$ , having source electrode connected to  $V_{DD}$  and drain connected to plate 10 of capacitor  $C_1$ . Transistor  $N_1$ , having source connected to  $V_{SS}$  and drain connected to plate 10 of capacitor  $C_1$ , serves as switch means  $S_2$ . Similarly, the function of switch means  $S_3$  is provided by transistor  $N_2$  having drain coupled to  $V_{SS}$  and source connected to plate 12 of capacitor  $C_1$ . A second stage comprising transistors  $P_2$ ,  $N_3$  and  $N_4$  and capacitor  $C_2$  is utilized in the tripler. The source and substrate of transistor  $P_2$  are connected to  $V_{DD}$ , and the drain thereof is connected to plate 18 of capacitor  $C_2$ . Transistor  $N_3$  has its drain connected to point A, whereby the first and second stages of the tripler are connected and has its source connected to plate 18 of capacitor  $C_2$ . The substrate of transistor  $N_3$  has  $V_{EF}$  applied thereto (from plate 14 of capacitor  $C_2$ ). The second plate 20 of capacitor  $C_2$  is connected to point B and to the source and substrate of transistor  $N_4$ , the drain of which is connected to  $V_{SS}$ . Transistor  $N_5$  serves as switch means  $S_4$ , the drain thereof being connected to point B and the substrate and source thereof being connected to plate 14 of capacitor  $C_2$ . Transistors  $P_1$  and  $P_2$  are controlled by the application at their respective gates of a control signal  $Q_1$ ; transistors  $N_1$ ,  $N_2$  and  $N_3$  by application at their gates of a control signal  $Q_2$ ; and transistors  $N_2$  and  $N_4$  are controlled by application at their gates of a control signal  $Q_1$ . The control signals  $Q_1$ ,  $\bar{Q}_1$  and  $Q_2$  are illustrated in FIG. 6, and are generated, for example, by a circuit such as that illustrated in FIG. 5, as will hereinafter be explained. The control signals alternate between relatively positive potential  $V_{DD}$  and relatively negative potential  $V_{EF}$ . Signal  $Q_1$  has positive-going and negative-going transitions at times  $t_0^-$  and  $t_1^+$  respectively. Signal  $Q_2$ , on the other hand, has positive-going and negative-going transitions at  $t_0^+$  and  $t_1^-$ , respectively. Signal  $\bar{Q}_1$  is the complement of signal  $Q_1$ .

Referring to FIGS. 3 and 4 and to the diagrams of control signals  $Q_1$ ,  $\bar{Q}_1$  and  $Q_2$  in FIG. 6, the operation of the voltage tripler in FIG. 3 will be explained. In FIG. 4, a conductive state is indicated by a level 1 and a non-conductive state indicated by level 0. Assuming the circuit to be initially in the charging mode,  $Q_1$  and  $Q_2$  are at low level, and accordingly, transistors  $P_1$ ,  $N_2$ ,  $P_2$  and  $N_4$  are conductive and transistors  $N_1$ ,  $N_3$  and  $N_5$  are non-conductive. Thus, during the charging mode, capacitor boosters  $C_1$  and  $C_2$  are, in effect, coupled in parallel between the positive potential  $V_{DD}$  and negative potential  $V_{SS}$  and are isolated from capacitor  $C_2$ . Capacitors  $C_1$  and  $C_2$  are thus charged such that potential  $V_{DD}$  appears at plates 10 and 18 and potential  $V_{SS}$  appears at plates 12 and 20. The time constants of the circuit are such that the capacitors have attained essentially full charge within the charging period. At instant

$t_0^-$  a two-step transition to the dumping mode is initiated. Control signal  $Q_1$  undergoes a positive-going transition, causing transistors  $P_1$ ,  $N_2$ ,  $P_2$  and  $N_4$  to become non-conductive. Thus, for a period beginning at  $t_0^-$  all of the transistors in the circuit are rendered non-conductive and the intermediate switching state is assumed. At time  $t_0^+$ , however, control signal  $Q_2$  undergoes a positive-going transition, causing transistors  $N_1$ ,  $N_3$  and  $N_5$  to become conductive. The dumping mode of operation is thereby effected wherein: plate 10 of capacitor  $C_1$  is connected to negative potential  $V_{SS}$ , plate 12 of capacitor  $C_1$  is connected to plate 18 of capacitor  $C_2$ , and plate 20 of capacitor  $C_2$  is connected to plate 14 of capacitor  $C_3$ . Since the voltage across a capacitor cannot change instantaneously, capacitors  $C_1$  and  $C_2$  each operate during transfer of charge to  $C_3$  in effect, as batteries supplying a potential ideally of value  $V_{DD} - V_{SS}$ . So the total potential, with respect to  $V_{DD}$  that appears across capacitor  $C_3$  is boosted to a potential approaching  $3V_{SS}$  as referred to  $V_{DD}$ .

At time  $t_1^-$  a two-step transition back to the charging mode is initiated. Control signal  $Q_2$  undergoes a negative-going transition, causing transistors  $N_1$ ,  $N_3$  and  $N_5$  to become non-conductive, thereby instituting the intermediate switching condition wherein all switch means are non-conductive. At time  $t_1^+$ , control signal  $Q_1$  undergoes a negative-going transition causing transistors  $P_1$ ,  $N_2$ ,  $P_2$  and  $N_4$  to become conductive, completing the transition to the charging mode. Controlling transistors  $P_1$ ,  $P_2$ ,  $N_1$ ,  $N_2$ ,  $N_3$ ,  $N_4$  and  $N_5$  in the manner described above prevents leakage paths permitting unwanted discharge of the capacitors.

A circuit for generating control signals  $Q_1$ ,  $\bar{Q}_1$  and  $Q_2$  is shown in FIG. 5 with the waveform of an input clock signal  $\phi$  applied thereto, and the conduction states of the transistors of the circuit being shown in FIG. 6 along with the waveforms of the control signals generated. Clock signal  $\phi$  is preferably a rectangular wave having positive-going transitions at times  $t_0^-$  and negative-going transitions at time  $t_1^-$ . Clock signal  $\phi$  is applied to the gate of a transistor  $P_3$  and through a conventional CMOS inverter  $I_1$  to the gate of transistor  $P_4$ . The respective sources and substrates of transistors  $P_3$  and  $P_4$  are connected to positive potential  $V_{DD}$ . The drains of transistors  $P_3$  and  $P_4$  are respectively coupled to the gates of transistors  $N_6$  and  $N_7$ , respectively. The respective sources and substrates of transistors  $N_6$  and  $N_7$  are connected to negative potential  $V_{EE}$ , that is, to plate 14 of capacitor  $C_3$  in FIG. 3. The drain of transistor  $N_6$  is connected to the interconnection of the drain of transistor  $P_4$  and gate of transistor  $N_7$ . Similarly, the drain of transistor  $N_7$  is connected to the interconnection of the drain of transistor  $P_3$  and the gate of transistor  $N_6$ . As will be hereinafter explained, control signals  $Q_1$  and  $\bar{Q}_1$  are developed at the interconnected drains of transistors  $P_4$  and  $N_6$  and  $\bar{Q}_2$  at the interconnected drains of transistors  $P_3$  and  $N_7$ . Control signals  $\bar{Q}_1$  and  $Q_2$  are respectively provided by inverting, via inverters  $I_2$  and  $I_3$ , the  $Q_1$  and  $\bar{Q}_2$  signals.

Transistors  $P_3$  and  $P_4$  have a transconductance that is  $m$  times as large as that of transistors  $N_6$  and  $N_7$ ,  $m$  being larger than 1, which is essential to the proper operation of the FIG. 5 control signal generator. (The encircled numerals near the source electrodes of  $P_3$ ,  $P_4$ ,  $N_6$  and  $N_7$  indicate the relative sizes of their transconductances.) The higher-transconductance transistor  $P_3$  can respond to a source-to-gate potential with amplitude equal to the difference between  $V_{SS}$  and  $V_{DD}$  to change

the charge on the interconnection of its drain electrode and that of lower-transconductance transistor  $N_7$  at a relatively rapid rate compared with the rate the lower-transconductance transistor  $N_7$  can change the charge when a source-to-gate potential of  $V_{DD} - V_{EE}$  amplitude is applied to it rather than to  $P_3$ . Similarly, higher-transconductance transistor  $P_4$  can respond to a source-to-gate potential with amplitude equal to the difference between  $V_{SS}$  and  $V_{DD}$  to change the charge on the interconnection of its drain electrode and that of lower-transconductance transistor  $N_6$  at a relatively rapid rate compared with the rate the lower-transconductance transistor  $N_6$  can when a source-to-gate potential of  $V_{DD} - V_{SS}$  amplitude is applied to it rather than to  $P_4$ .

Referring to FIGS. 5 and 6, the operation of the circuit of FIG. 5 will be explained. It is assumed that inverters  $I_1$ ,  $I_2$  or  $I_3$  exhibit no appreciable delay. The circuit is taken to be initially in the condition wherein  $\phi$  is low, transistors  $P_3$  and  $N_4$  conductive and  $P_4$  and  $N_7$  non-conductive. At time  $t_0^-$ , clock  $\phi$  undergoes a positive-going transition. Transistors  $P_3$  and  $P_4$  are thereby rendered conductive and non-conductive, respectively. When transistor  $P_4$  is rendered conductive, control signal  $Q_1$  undergoes a nearly instantaneous transition from  $V_{EE}$  to  $V_{DD}$ . With  $V_{DD}$  applied to its gate and transistor  $P_3$  non-conductive, transistor  $N_7$  becomes conductive, causing a slow transition in control signal  $\bar{Q}_2$  from  $V_{DD}$  to  $V_{EE}$ . Thus, the negative-going transition in control signal  $\bar{Q}_2$  does not, in effect, occur until time  $t_0^+$ .

At  $t_1^-$ , clock  $\phi$  undergoes a negative-going transition. Transistors  $P_3$  and  $P_4$  are thereby rendered conductive and non-conductive, respectively. With  $V_{DD}$  applied at its gate and  $P_4$  non-conductive,  $N_6$  becomes conductive, and  $N_7$ , with the positive potential removed from its gate, becomes non-conductive. Control signal  $\bar{Q}_2$ , therefore, undergoes a relatively instantaneous positive-going transition from  $V_{EE}$  to  $V_{DD}$ . The change in control signal  $Q_1$ , however, is effected by the conduction in high-impedance  $N_6$  and therefore the transition in  $Q_1$  is, in effect, delayed by a predetermined period to time  $t_1^+$ . Thus, control signal  $Q_1$  has positive-going transitions at times  $t_0^-$  and negative-going transitions at times  $t_1^+$  and control signal  $Q_2$  (complement of  $\bar{Q}_2$ ) has positive-going transitions at time  $t_0^+$  and negative-going transitions at time  $t_1^-$ .

While the voltage multiplying circuits shown in FIGS. 1 and 3 operate by generating a multiplied negative potential, the circuits can be modified to produce a multiplied positive potential. In the case of FIG. 1, the respective positive and negative potential sources can be interchanged to develop a multiplied positive potential relative to  $V_{DD}$  across capacitor  $C_3$ . In the case of FIG. 3, the interchanging of potentials can be effected by replacing the transistors with their respective complementary types and applying the complement of the respective control signals shown in FIG. 3.

What is claimed is:

1. In a voltage multiplier circuit comprising a source of input voltage, a storage capacitor across which output voltage that is a multiple of input voltage is made available, at least one booster capacitor, control signal generator means for cyclically generating a first control signal followed by a second control signal, said first and said second control signals for governing charging and dumping portion of an operating cycle respectively, a first set of electronically controlled switch means conductive responsive to said first control signal to connect each booster capacitor across said source of input volt-

age for charging and being otherwise non-conductive, and a second set of electronically controlled switch means conductive responsive to said second control signal to connect each booster capacitor in series with said source of input voltage across said storage capacitor for transferring charge to said storage capacitor and being otherwise non-conductive, the improvement

wherein said control signal generator is of a type for providing an interval between said first and second control signals in each cycle and for providing an interval between said second control signal in each cycle and the first control signal in the succeeding cycle.

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**Disclaimer**

4,106,086.—*Mark Denton Holbrook*, Belle Mead, and *Richard Plumb Fillmore*, Plainfield, N.J. VOLTAGE MULTIPLIER CIRCUIT. Patent dated Aug. 8, 1978. Disclaimer filed Apr. 20, 1979, by the assignee *RCA Corporation*.

Hereby enters this disclaimer to all claims of said patent.

[*Official Gazette June 19, 1979.*]

# United States Patent [19]

Ishiwatari

Reprint Available Copy

[11] 4,186,436

[45] Jan. 29, 1980

## [54] BOOSTER CIRCUIT

[75] Inventor: Masumi Ishiwatari, Zushi, Japan

[73] Assignee: Canon Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 871,746

[22] Filed: Jan. 23, 1978

### [30] Foreign Application Priority Data

Jan. 27, 1977 [JP] Japan ..... 52-8139

[51] Int. Cl.<sup>2</sup> ..... H02M 7/00

[52] U.S. Cl. .... 363/60

[58] Field of Search ..... 307/109, 110; 320/1; 363/59, 60

### [56] References Cited

#### U.S. PATENT DOCUMENTS

2,463,509	3/1949	Bird	307/110 X
2,631,249	3/1953	Smith	363/59 X
3,032,714	5/1962	Cohen	320/1X
3,943,428	3/1976	Whidden	363/60
3,955,353	5/1976	Astle	363/60 X

## FOREIGN PATENT DOCUMENTS

2035223 1/1972 Fed. Rep. of Germany ..... 363/59

Primary Examiner—William M. Shoop  
Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper & Scinto

### [57] ABSTRACT

A voltage step-up circuit, or booster circuit, wherein in response to a first signal a first switching element is enabled to charge a first capacitor with an input voltage while a second switching element is disabled, and in response to a second signal the second switching element is enabled to charge with the input voltage a second capacitor connected in series to the first capacitor while the first switching element is disabled. The sum of the voltages appearing across the first and second capacitors is derived as an output voltage. The "ON" and "OFF" times of the first and second signals may be varied, and the ratio between the "ON" time of the first signal to the "ON" time of the second signal may also be varied. The number of switching elements and capacitors may be increased as needed.

6 Claims, 6 Drawing Figures

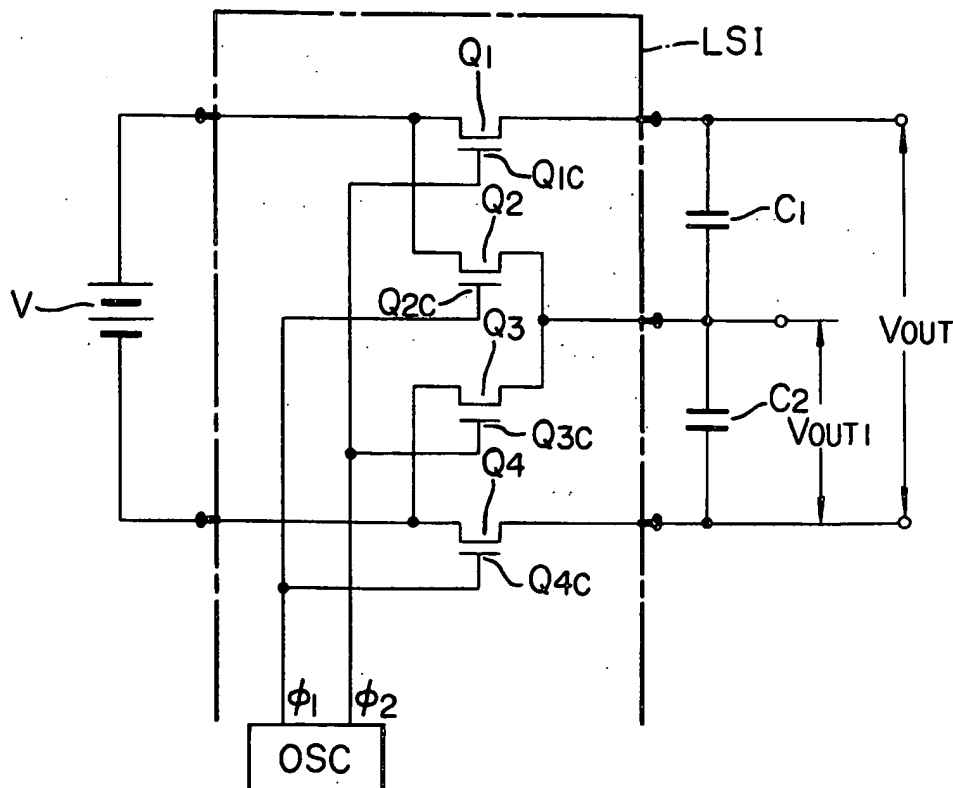




FIG. 3B

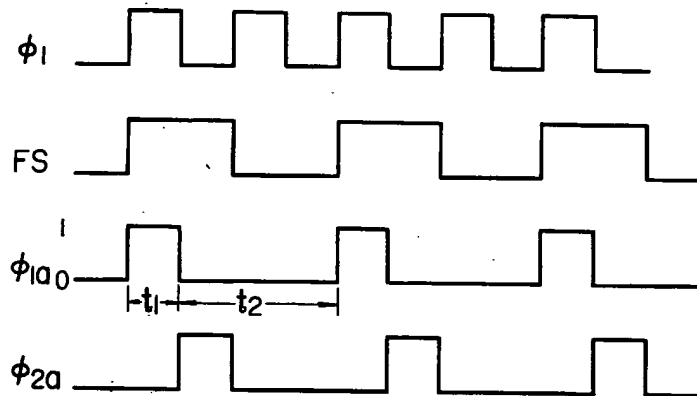


FIG. 4A

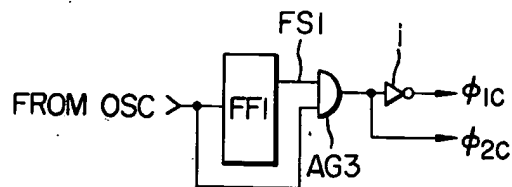
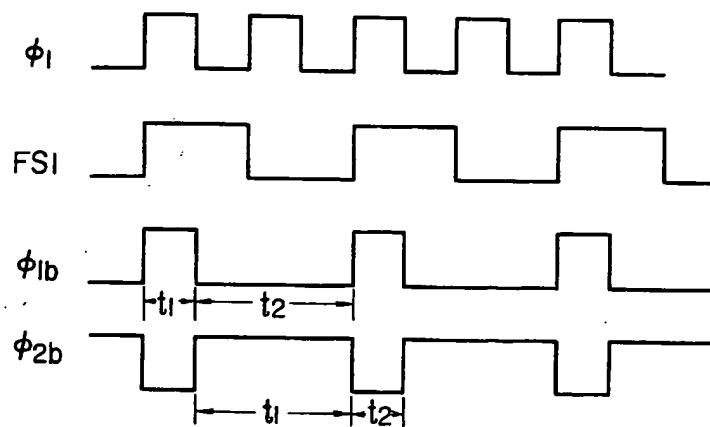


FIG. 4B



## BOOSTER CIRCUIT

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a booster circuit.

#### 2. Description of the Prior Art

In order to drive a liquid crystal display device incorporated in a desktop computer or in a pocket-size calculator, a power source must supply a voltage of the order of 4.5 to 10 V. In general the desktop computers and pocket-size calculators operate on one or two mercury or silver oxide batteries (1.5 V to 3.0 V) so that a booster or step-up circuit must be provided in order to drive the liquid crystal display device.

To this end DC-DC converters including a boosting transformer have been used, but their energy transfer efficiency is considerably low as their power consumption is as much as or exceeds the power consumption in a load or a liquid crystal display device. Furthermore the DC-DC converter represents a considerable part of the cost of the desktop computer or the pocket-size calculator so that the cost of the DC converter must be reduced in order to reduce the total cost of the calculator.

### SUMMARY OF THE INVENTION

In view of the above, one of the objects of the present invention is to provide a booster circuit with less power consumption.

Another object of the present invention is to provide a booster circuit best adapted to be implemented on an one-chip calculator.

The above and other objects, features and advantages of the present invention will become more apparent from the following description of preferred embodiments thereof taken in conjunction with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a booster circuit in accordance with the present invention;

FIG. 2 is a timing diagram of signals controlling the operation of the booster circuit shown in FIG. 1;

FIG. 3A is a block diagram of a signal generator;

FIG. 3B shows the waveforms of signals appearing at the points of the signal generator shown in FIG. 3A;

FIG. 4A is a block diagram of another signal generator; and

FIG. 4B shows the waveforms of signals appearing at the points of the signal generator shown in FIG. 4A.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1 there is shown a first embodiment of the booster or step-up circuit in accordance with the present invention. An input voltage  $V$  which is of a silver oxide battery of a voltage to be boosted is impressed across capacitors  $C1$  and  $C2$  through switching elements  $Q1$ - $Q4$  such as MOS transistors which are enabled or disabled in response to signals  $\phi1$  and  $\phi2$  applied to control terminals  $Q1c$ - $Q4c$  from a signal generator OSC. Fig. 2 shows the waveforms of these control signals  $\phi1$  and  $\phi2$ .

Next the mode of operation will be described. First it is assumed that no charge be stored in the capacitors  $C1$  and  $C2$ . Then when the signal  $\phi1$  is "1" and the signal  $\phi2$  is "0", the switching elements  $Q2$  and  $Q4$  are enabled

and the switching elements  $Q1$  and  $Q3$  are disabled. Therefore the input voltage  $V$  is applied across the capacitor  $C2$  through the switching elements  $Q2$  and  $Q4$ . The voltage  $V1$  across the capacitor  $C2$  is substantially equal to the input voltage  $V$ .

When the signal  $\phi1$  changes to "0" and the signal  $\phi2$  changed to "1", the switching elements  $Q2$  and  $Q4$  are disabled and the switching elements  $Q1$  and  $Q3$  are enabled. Therefore while the voltage across the capacitor  $C2$  remains unchanged, the capacitor  $C1$  is charged with the input voltage  $V$  through the enabled switching elements  $Q1$  and  $Q3$ . The voltage  $V2$  across the capacitor  $C1$  is substantially equal to the input voltage  $V$ .

Now the output voltage  $V_{out}$  of the booster or step-up circuit becomes  $V1 + V2$  which is higher than the input voltage  $V$ . This procedure is repeated in response to changes in signals  $\phi1$  and  $\phi2$  so that the output voltage  $V_{out}$  is repeatedly obtained.

The booster circuit may be implemented on the same chip as of arithmetic and logic circuits of digital equipment such as a pocket-size calculator.

In FIG. 3A there is shown a schematic diagram of a circuit for controlling the output voltage  $V_{out}$  of the booster circuit shown in FIG. 1, and FIG. 3B shows the waveforms of associated signals therewith. With this circuit, the ratio of the pulse duration of the "1" signal to the pulse duration of the "0" signal may be varied. That is, the output  $\phi1$  from the signal generator OSC is frequency divided in a flip-flop FF, and the output FS from the flip-flop FF and the output  $\phi1$  from the signal generator OSC are applied to AND gate AG1 to derive the control signal  $\phi1a$ . In a like manner, the output FS from the flip-flop FF and the output  $\phi2$  from the signal generator OSC are applied to AND gate AG2 to derive the output  $\phi2a$  which is applied to the switching elements  $Q1$  and  $Q3$ . Therefore the voltage appearing across the capacitor  $C1$  or  $C2$  may be varied.

In FIG. 4A there is shown a schematic diagram of another circuit for controlling the output voltage  $V_{out}$ , and FIG. 4B shows the waveforms of associated signals therewith. With this circuit, the ratio of the "1" state duration of the control signal  $\phi1$  to the "1" state duration of the control signal  $\phi2$  may be varied. That is, the output  $\phi1$  from the signal generator OSC is frequency divided in a flip-flop FF1, and the output FS1 from the flip-flop FF1 and the signal  $\phi1$  are applied to AND gate AG3 to derive the control signal  $\phi2c$  which is applied to the switching elements  $Q2$  and  $Q4$ . The output from AND gate AG3; that is, the control signal  $\phi2c$  is inverted by an inverter  $i$  to derive the control signal  $\phi1c$  which is applied to the switching elements  $Q1$  and  $Q3$ .

Therefore the voltage appearing across the capacitor  $C2$  is higher than the voltage across the capacitor  $C1$  so that when another output voltage  $V_{out2}$  is derived across the capacitor  $C2$ , the drop in output voltage  $V_{out}$  may be prevented.

Instead of the circuit shown in FIG. 4A, the capacitors  $C1$  and  $C2$  may have different capacitances to attain the same effects.

So far the number of capacitors has been described as being two, but it will be apparent to those skilled in the art that the number of capacitors may be increased based on the description above.

Thus according to the present invention the energy transfer efficiency may be considerably improved without the use of a transformer.

I claim:

1. Semiconductor unit for producing higher potential than input voltage by the use of electric energy storage means comprising:

first and second input terminals for supplying electric energy to said unit;

a first switching circuit for transmitting the electric energy applied to said first and second input terminals, said first switching circuit comprising a first electric switching element (Q1) and a second electric switching element (Q3);

a second switching circuit for transmitting the electric energy applied to said first and second input terminals, said second switching circuit comprising a third electric switching element (Q2) and a fourth electric switching element (Q4);

a first output terminal electrically connected through the first switching element of said first switching circuit to said first input terminal;

a second output terminal electrically connected through the second switching element of said first switching circuit to said second input terminal, and connected through the third switching element of said second switching circuit to said first input terminal;

a third output terminal electrically connected through the fourth switching element of said second switching circuit to said input terminal;

(a) first energy storage means coupled between said first output terminal and said second output terminal;

(b) second energy storage means coupled between said second output terminal and said third output terminal; and

a signal generating circuit for generating a first pulse signal train to be applied to said first switching circuit and a second pulse signal train to be applied to said second switching circuit, the pulses of the first and second pulse signal trains being different in phase from each other, and thus said first and second switching circuits being alternatively driven;

whereby electric energy is stored in said first and second energy storage means.

2. Semiconductor unit according to claim 1 wherein the pulses of the first and second pulse signal trains of said signal generating circuit are different in pulse width from each other.

3. Semiconductor unit according to claim 1 wherein said first and second switching circuits comprise MOS transistors.

4. Semiconductor unit according to claim 1, wherein said first and second energy storage means are capacitors.

5. Monolithic semiconductor unit according to claim 4 wherein the pulses of the first and second pulse signal trains of said signal generating circuit are different in the pulse width from each other.

6. Monolithic semiconductor unit according to claim 4 wherein said first and second switching circuits comprise MOS transistors.

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[54] APPARATUS FOR CHARGING A CAPACITOR

[75] Inventor: Jun-ichi Sano, Chelmsford, Mass.

[73] Assignee: GTE Laboratories Incorporated, Waltham, Mass.

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[22] Filed: Dec. 23, 1980

[51] Int. Cl.<sup>3</sup> ..... H02M 3/18

[52] U.S. Cl. .... 363/60; 307/110; 307/246

[58] Field of Search ..... 363/59-61; 320/1; 307/109, 110, 246, 264, 578, 581

[56] References Cited

U.S. PATENT DOCUMENTS

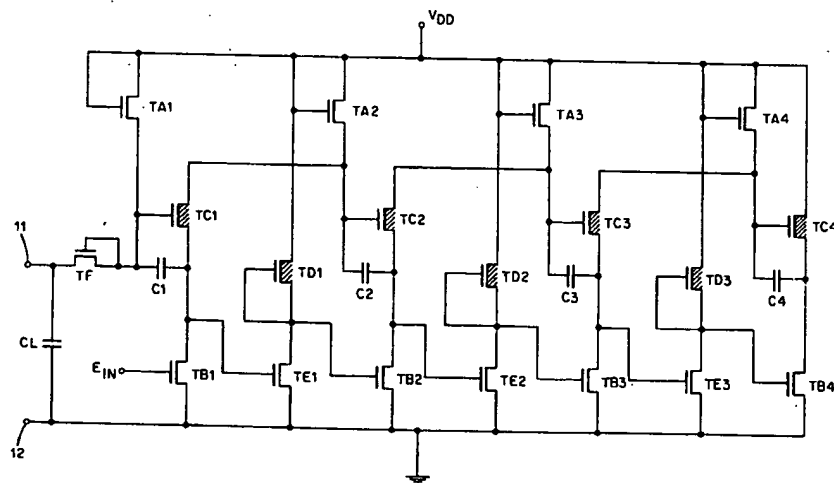
3,824,447	7/1974	Kuwabara	363/60
4,053,821	10/1977	Hose, Jr. et al.	363/60
4,199,806	4/1980	Patterson	363/60

Primary Examiner—William M. Shoop  
Assistant Examiner—Peter S. Wong  
Attorney, Agent, or Firm—David M. Keay

[57] ABSTRACT

An NMOS FET circuit for charging a storage capacitor to a voltage higher than the power supply voltage. The circuit includes several stages each including a capacitance and FET switches. In response to a high level control signal the FET's in effect connect each capacitance between the supply voltage and ground to charge the capacitances. Then, in response to a low level control signal the FET's in effect connect the capacitances in series between the supply voltage and the storage capacitor thus transferring a portion of the charges in the capacitances into the storage capacitor. The charge placed in the storage capacitor produces a voltage thereacross which is greater than the supply voltage.

10 Claims, 3 Drawing Figures



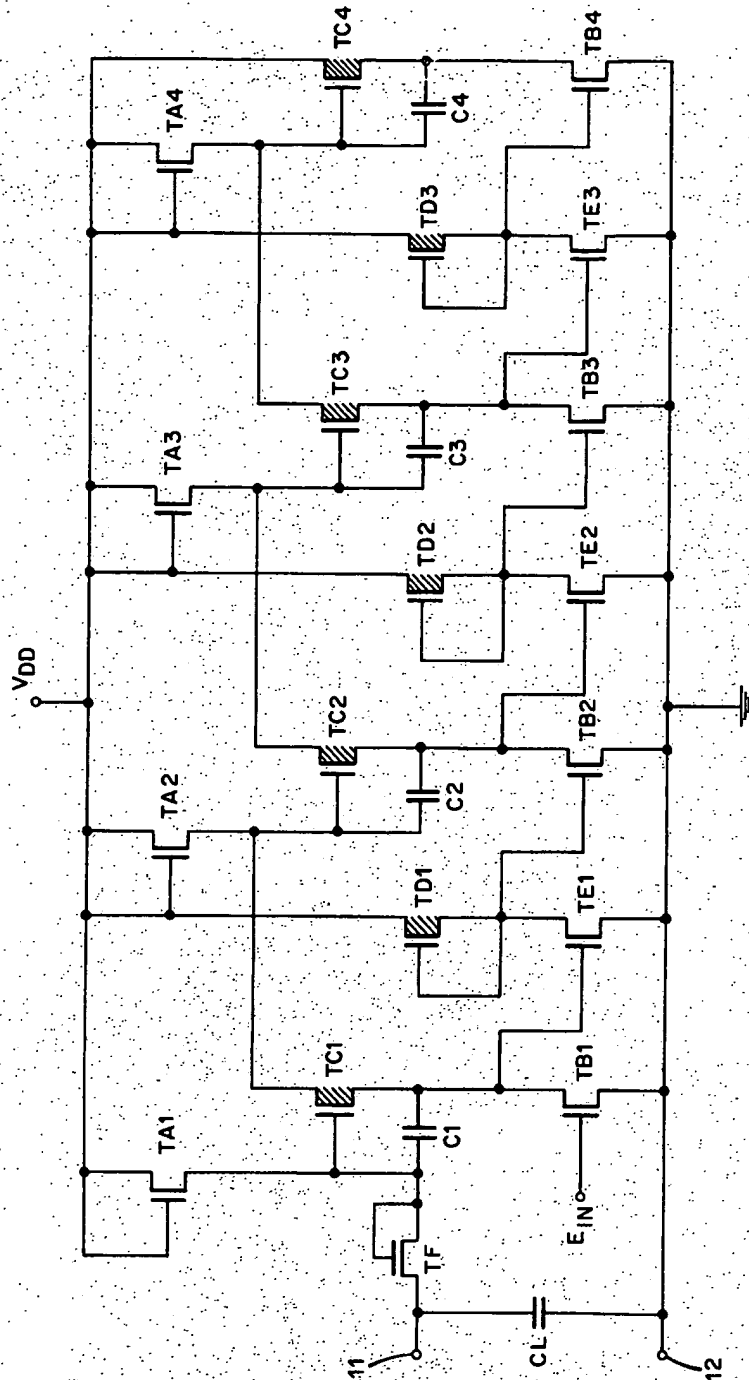


Fig. 1.



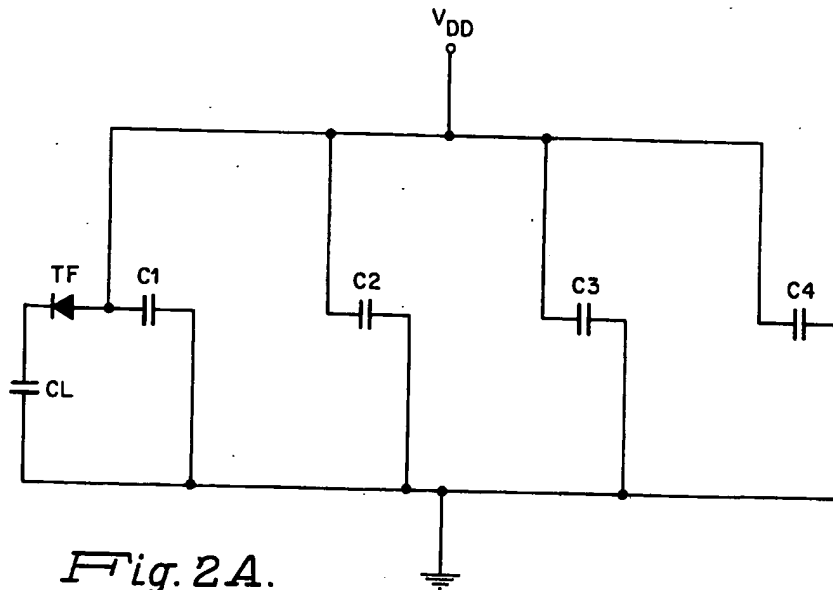


Fig. 2A.

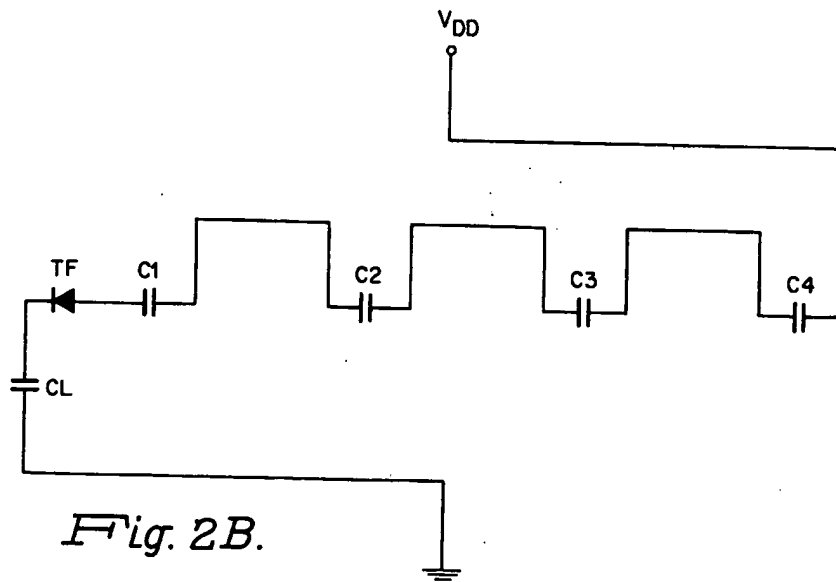


Fig. 2B.

## APPARATUS FOR CHARGING A CAPACITOR

### BACKGROUND OF THE INVENTION

This invention relates to apparatus for charging a capacitor. More particularly, it is concerned with apparatus for charging a capacitor to a voltage higher than the available supply voltage.

Under certain circumstances, particularly with metal-oxide-silicon (MOS) integrated circuits, it would be desirable to have available voltages which are higher than the operating voltages available from the power supplies typically employed. The availability of higher voltages would be particularly useful for DC biasing in order to provide improved switching speed and greater current driving capability.

### SUMMARY OF THE INVENTION

Voltages higher than the operating potential provided by the available power supply may be provided by charging a storage capacitor to a higher voltage by employing apparatus in accordance with the present invention. Apparatus in accordance with the present invention includes a source of operating potential and a point of reference potential. A plurality of stages are arranged in order. Each stage includes a capacitance means with first and second terminals, a first field effect transistor connected between the source of operating potential and the first terminal of the capacitance means, and a second field effect transistor connected between the second terminal of the capacitance means and the point of reference potential. Each stage except the last stage has a third field effect transistor which is connected between the second terminal of the capacitance means of the associated stage and the first terminal of the capacitance means of the following stage. The last stage also has a third field effect transistor which is connected between the second terminal of the capacitance means of the last stage and the source of operating potential. Means are provided for coupling the first terminal of the capacitance means of the first stage to one terminal of the storage capacitor, and means are provided for coupling the point of reference potential to the other terminal of the storage capacitor. The apparatus includes control means for applying first or second control signal conditions to the stages. In response to the first control signal condition all of the first and second field effect transistors are in a high conduction condition and the third field effect transistors are in a relatively low conduction condition whereby each of the capacitance means is connected between the source of operating potential and the point of reference potential and becomes charged. In response to the second control signal condition all of the first and second field effect transistors are in a low conduction condition and the third field effect transistors are in a relatively high conduction condition whereby the plurality of capacitance means are connected in series between the source of operating potential and the storage capacitor, thus transferring a portion of the charges in the capacitance means into the storage capacitor. The charge placed in the storage capacitor produces a voltage thereacross which is greater than the operating potential.

### BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a schematic circuit diagram of an exemplary apparatus in accordance with the present invention; and FIGS. 2A and 2B are diagrams illustrating equivalent circuits of the apparatus of FIG. 1 under two sets of operating conditions.

For a better understanding of the present invention, together with other and further objects, advantages, and capabilities thereof, reference is made to the following disclosure and appended claims in connection with the above-described drawings.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 of the drawings illustrates an exemplary metal-oxide-silicon (MOS) field effect transistor (FET) apparatus in accordance with the present invention. In the circuit illustrated all of the FET's are N channel enhancement and depletion type devices. The FET devices and other components of the apparatus as illustrated in FIG. 1 may be fabricated as an integrated circuit in a single body of semiconductor material. The storage capacitor CL which is to be charged may be fabricated in the same body of semiconductor material or may be external of the body and connected to the circuit.

The apparatus for charging the storage capacitor CL includes a terminal  $V_{DD}$  of a positive voltage source. The exemplary apparatus illustrated includes four stages. Each of the four stages has a capacitance C1-C4. A first enhancement type FET TA1-TA4 in each stage has one of its conduction path electrodes (source or drain) and its gate electrode connected to the voltage source  $V_{DD}$  and its other conduction path electrode connected to the first terminal of the associated capacitance C1-C4. A second enhancement type FET TB1-TB4 in each stage has one conduction path electrode connected to the second terminal of the associated capacitance C1-C4 and the other conduction path electrode connected to ground. Each stage also has a third FET TC1-TC4 of the depletion type with its gate electrode connected to the juncture of the associated first FET TA1-TA4 and the first terminal of the associated capacitance C1-C4. One of the conduction path electrodes of the third FET TC1-TC4 of each stage is connected to the juncture of the second terminal of the associated capacitance C1-C4 and the associated second FET TB1-TB4. The other conduction path electrode of the third FET TC1-TC4 of each stage except the last is connected to the first terminal of the capacitance C2-C4 of the following stage. The other conduction path electrode of the third FET TC4 of the last stage is connected directly to the voltage source  $V_{DD}$ .

The gate electrode of the second FET TB1 of the first stage is connected to a control input terminal  $E_{IN}$ . The gate electrodes of the second FET's TB1-TB4 of the other stages are indirectly coupled to the control input terminal  $E_{IN}$  by connections from the juncture of each of the second FET's TB1-TB3 and the second terminal of the associated capacitance C1-C3 except for the last stage by way of delay circuits. The delay circuit in each of the first three stages is an inverter circuit including an FET TD1-TD3 of the depletion type connected in series with an FET TE1-TE3 of the enhancement type between the voltage source  $V_{DD}$  and ground. The juncture of the conductive path electrodes of the two transistors of each inverter circuit is connected to the gate electrode of the associated depletion type FET TD1-TD3 and to the gate electrode of the

second FET TB2-TB4 of the following stage. The gate electrode of the enhancement type FET TE1-TE3 is connected to the juncture of the second FET TB1-TB3 and the second terminal of the capacitance C1-C3 of the preceding stage.

An FET TF of the enhancement type is connected in series between the first terminal of the capacitance C1 of the first stage and the first terminal of the storage capacitor CL. The gate electrode of FET TF is connected to the juncture of the FET TF and the capacitance C1 so that the FET TF functions as a unidirectional current flow device or diode. The storage capacitor CL is shown with its first terminal connected to a terminal 11 and its second terminal, which is connected to ground, connected to a second terminal 12. The charge stored in the storage capacitor CL is thus made available at terminals 11 and 12.

The apparatus illustrated in FIG. 1 operates in the following manner to store a charge in the storage capacitor CL. When the control signal  $E_{IN}$  becomes high, all of the second FET's TB1-TB4 become conductive. The capacitances C1-C4 of each stage become charged by current flow through the associated first FET's TA1-TA4, which are highly conductive, and the second FET's TB1-TB4. At the same time the third FET's TC1-TC4 are in a relatively low conduction condition. Although there is some conduction through the third FET's TC1-TC4, there is no significant interference with charging of the capacitances C1-C4. FIG. 2A illustrates the equivalent of the circuit of FIG. 1 under these conditions. In effect, each of the capacitances C1-C4 is connected between the voltage source  $V_{DD}$  and ground, and is charged to the supply voltage. The actual voltage across each capacitance C1-C4 is  $V_{DD} - V_{th} - K_{sub}\sqrt{V_{SB}}$ , where  $V_{th}$  is the threshold voltage,  $K_{sub}$  is the back bias constant, and  $V_{SB}$  is the source to substrate voltage of each of the first FET's TA1-TA4.

When the control signal  $E_{IN}$  becomes low, the second FET's TB1-TB4 are turned off. The action of the inverters of the FET's TD1-TD3 and TE1-TE3 in each stage except the fourth introduces a slight delay between each stage, thus insuring that the second FET of each stage is completely off before that of the following stage is turned off. This sequence of turning off the second FET's TB1-TB4 prevents the charge stored in a capacitance from leaking off through the second FET of the preceding stage.

With the second FET's TB1-TB4 off, the voltages at the junctures of the second FET's TB1-TB4 and the third FET's TC1-TC4 increase, pulled up by conduction through the third FET's TC1-TC4. At the same time, the voltages at the gate electrode of the third FET's TC1-TC4 also rise because of the charges in the associated capacitances C1-C4. When the voltages at the gate electrodes of each of the third FET's TC1-TC4 exceeds  $V_{DD} - V_{th} - K_{sub}\sqrt{V_{SB}}$  ( $V_{th}$ ,  $K_{sub}$ , and  $V_{SB}$  being parameters at the first FET's TA1-TA4), the first FET's TA1-TA4 become cut-off. The third FET's TC1-TC4 are in a relatively high conduction condition; and, therefore, in effect the capacitances C1-C4 are connected in series between the voltage source  $V_{DD}$  and the storage capacitor CL as illustrated in the diagram of FIG. 2B. As the charges stored in the capacitances C1-C4 are partially transferred into the storage capacitor CL, the voltages across the capacitances C1-C4 decrease and the currents through them are reduced.

The voltage  $V_{CL}$  produced across the storage capacitor CL by the transfer of charges from the capacitances C1-C4 may be calculated employing the law of conservation of charge as follows:

$$V_{CL} = \frac{N(V_{DD} - V_{TA}) + \frac{V_{DD} - V_{TF}}{N}}{CL + \frac{C_n}{N}} C_n$$

where  $C_n$  is the capacitance value of each capacitance C1-C4,  $N$  is the number of stages,  $V_{TA} = V_{th} + K_{sub}\sqrt{V_{SB}}$  of each first FET TA1-TA4, and  $V_{TF} = V_{th} + K_{sub}\sqrt{V_{SB}}$  of FET TF.

If the cycle of applying high and low control voltages  $E_{IN}$  is repeated, the voltage across the storage capacitor CL is increased up to a maximum. During cycling the FET TF acts as a diode as illustrated in FIGS. 2A and 2B permitting current to flow into the storage capacitor CL from the apparatus and preventing the flow of current out of the storage capacitor CL into the apparatus when the control signal  $E_{IN}$  is high. The final voltage which can be obtained across the storage capacitor CL may be expressed as

$$V_{CL(final)} = N(V_{DD} - V_{TA}) + V_{DD} - V_{TF}$$

For example, in an apparatus in accordance with the invention having a supply voltage  $V_{DD}$  of 5 volts,  $V_{TA}$  of 1.7 volts,  $V_{TF}$  of 2.3 volts, four stages, a capacitive value  $C_n$  of 1 picofarad for each capacitance C1-C4 and a storage capacitor CL of 1 picofarad, after a single cycle the storage capacitor CL is charged to a voltage  $V_{CL}$  of 11.1 volts. After a series of control input pulses, for example 5 volt squarewave pulses at a frequency of 500 KHz, the final voltage  $V_{CL(final)}$  across the storage capacitor is 15.9 volts.

The foregoing are calculated values which do not take into consideration the effects of parasitic capacitances between both terminals of the capacitances C1-C4 and ground. One consequence of the parasitic capacitances is that the incremental increase of voltage  $V_{CL}$  across the storage capacitor CL decreases with increasing number of stages. After a certain number of stages there is no further increase in the voltage  $V_{CL}$ . For example, in apparatus as described above, if the parasitic capacitance between each terminal of each capacitance C1-C4 is approximately 0.1 picofarads, more than four stages produces no significant result over that obtained with four stages.

In an exemplary apparatus as described above the dimensions of the channels of the FET's may be as follows: TA1-TA4 1.0 mil wide by 0.3 mil long; TB1-TB4 0.3 mil wide by 0.3 mil long; TC1-TC4 0.3 mil wide by 3.0 mils long; TD1-TD3 0.3 mil wide by 1.2 mils long; TE1-TE3 0.3 mil wide by 0.6 mil long; and TF 0.3 mil wide by 0.3 mil long.

While there has been shown and described what is considered a preferred embodiment of the present invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention as defined by the appended claims.

What is claimed is:

1. Apparatus for charging a storage capacitor including
  - a source of operating potential;
  - a point of reference potential;

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a plurality of stages arranged in order, each stage including capacitance means having first and second terminals,  
 a first field effect transistor connected between the source of operating potential and the first terminal of the capacitance means, and  
 a second field effect transistor connected between the second terminal of the capacitance means and the point of reference potential;  
 each of said stages except the last stage including a third field effect transistor connected between the second terminal of the capacitance means of the associated stage and the first terminal of the capacitance means of the following stage;  
 the last stage having a third field effect transistor connected between the second terminal of the capacitance means of the last stage and the source of operating potential;  
 means for coupling the first terminal of the capacitance means of the first stage to one terminal of the storage capacitor;  
 means for coupling the point of reference potential to the other terminal of the storage capacitor;  
 control means for applying first or second control signal conditions to said stages;  
 said first and second field effect transistors being operable in a high conduction condition and said third field effect transistors being operable in a relatively low conduction condition in response to said first control signal condition at said control means whereby each of said capacitance means is connected between said source of operating potential and said point of reference potential and becomes charged;  
 said first and second field effect transistors being operable in a low conduction condition and said third field effect transistors being operable in a relatively high conduction condition in response to said second control signal condition at said control means whereby the plurality of capacitance means are connected in series between said source of operating potential and said storage capacitor transferring a portion of the charges in the capacitance means into the storage capacitor;  
 said control means including  
 a control input terminal connected to the gate electrode of the second field effect transistor of the first stage for receiving said first or second control signal conditions, and  
 means coupling the gate electrode of the second field effect transistor of each of said stages except the first stage to the preceding stage.

2. Apparatus for charging a storage capacitor in accordance with claim 1 wherein  
 the gate electrode of each of said first field effect transistors is connected to the source of operating potential; and  
 the gate electrode of each of said third field effect transistors is connected to the juncture of the first

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terminal of the capacitance means and the first field effect transistor of the associated stage.

3. Apparatus for charging a storage capacitor in accordance with claim 2 wherein  
 each stage except the last stage includes a delay means connected between the juncture of the second terminal of the capacitance means and the second field effect transistor of the associated stage and the gate electrode of the second field effect transistor of the following stage.

4. Apparatus for charging a storage capacitor in accordance with claim 3 wherein  
 each of said second field effect transistors is of the enhancement type.

5. Apparatus for charging a storage capacitor in accordance with claim 4 wherein  
 each of said third field effect transistors is of the depletion type.

6. Apparatus for charging a storage capacitor in accordance with claim 5 wherein  
 each of said first field effect transistors is of the enhancement type.

7. Apparatus for charging a storage capacitor in accordance with claim 6 wherein  
 each of said delay means includes an inverter stage.

8. Apparatus for charging a storage capacitor in accordance with claim 7 wherein  
 said means for coupling the first terminal of the capacitance means of the first stage to said one terminal of the storage capacitor includes a unidirectional current flow device for permitting the flow of current into the storage capacitor and for preventing the flow of current out of the storage capacitor.

9. Apparatus for charging a storage capacitor in accordance with claim 8 wherein each of said delay means includes  
 a depletion type field effect transistor and an enhancement type field effect transistor connected in series between the source of operating potential and the point of reference potential;  
 the gate electrode of the depletion type field effect transistor being connected to the juncture of the depletion type field effect transistor and the enhancement type field effect transistor;  
 the gate electrode of the enhancement type field effect transistor being connected to the juncture of the second terminal of the capacitance means and the second field effect transistor of the associated stage; and  
 the juncture of the depletion type field effect transistor and the enhancement type field effect transistor being connected to the gate electrode of the second field effect transistor of the following stage.

10. Apparatus for charging a storage capacitor in accordance with claim 9 wherein  
 said field effect transistors are N channel metal-oxide-silicon field effect transistors.

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# United States Patent [19]

Risinger

[11] Patent Number: 4,460,952

[45] Date of Patent: Jul. 17, 1984

## [54] ELECTRONIC RECTIFIER/MULTIPLIER/LEVEL SHIFTER

[75] Inventor: Vance Risinger, Lubbock, Tex.

[73] Assignee: Texas Instruments Incorporated,  
Dallas, Tex.

[21] Appl. No.: 377,729

[22] Filed: May 13, 1982

[51] Int. Cl.<sup>3</sup> ..... H02M 7/08; H02M 7/10

[52] U.S. Cl. .... 363/61; 307/110;  
363/60

[58] Field of Search ..... 307/110; 363/59-61,  
363/62, 127

## [56] References Cited

### U.S. PATENT DOCUMENTS

3,731,179	5/1973	Rademaker	363/60
4,321,661	12/1982	Sano	363/60
4,340,931	7/1982	Endo et al.	363/124
4,398,099	8/1983	Benoit-Gonin	363/60

## FOREIGN PATENT DOCUMENTS

3115 1/1977 Japan ..... 307/110

## OTHER PUBLICATIONS

Accardi, "Diode-Switched FET's Rectify the Full Wave," Electronics, Aug. 3, 1970.

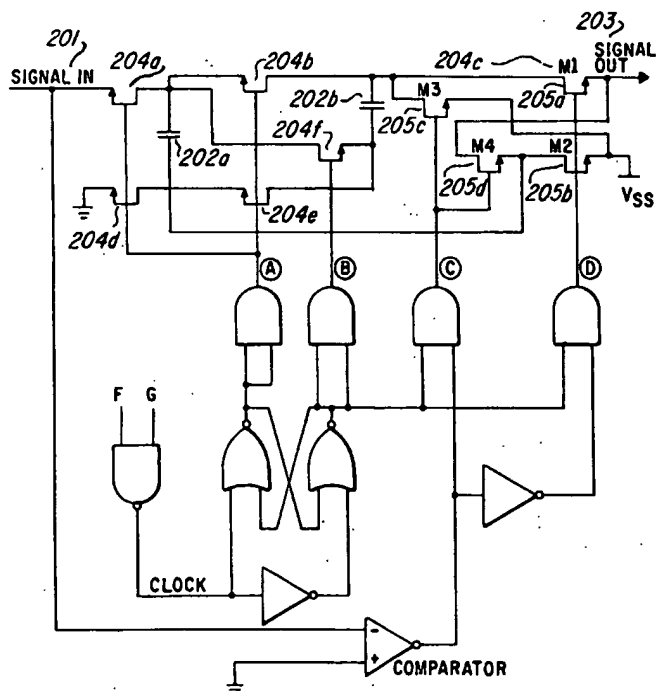
Primary Examiner—William H. Beha, Jr.

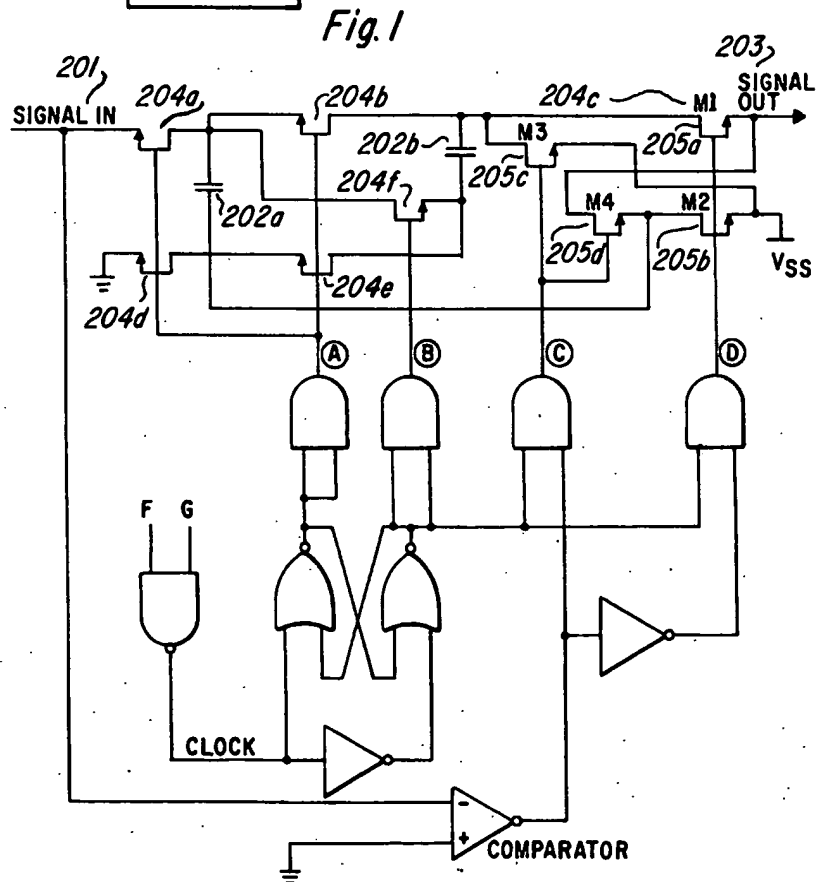
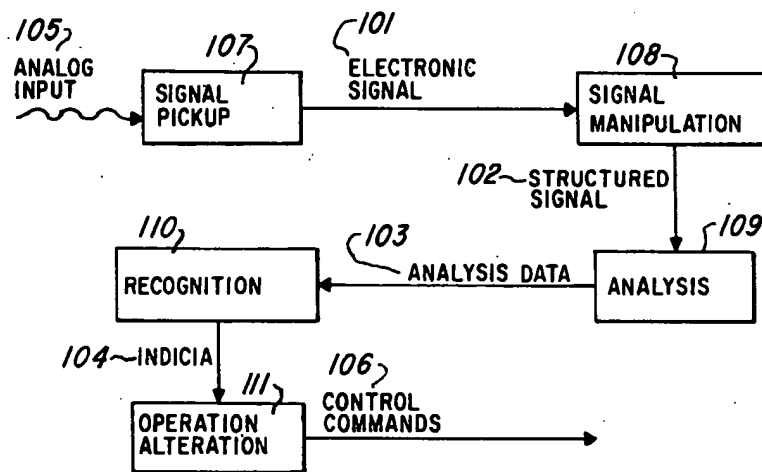
Attorney, Agent, or Firm—William E. Hiller; James T. Comfort; Melvin Sharp

## [57] ABSTRACT

A rectifier/multiplier/level shifter utilizing multiple capacitors which are switched from parallel to series or vice versa. An analog signal is communicated to a plurality of capacitors in parallel which are subsequently connected in series by selective switching. Depending upon the sign of the analog signal, taps are made on the capacitors so as to rectify the incoming analog signal. In a similar fashion a tap utilizes the serial multiplication of the capacitors so as to create a multiplier circuit. This particular architecture is particularly well suited for a metal-oxide-silicon (MOS) embodiment.

7 Claims, 3 Drawing Figures





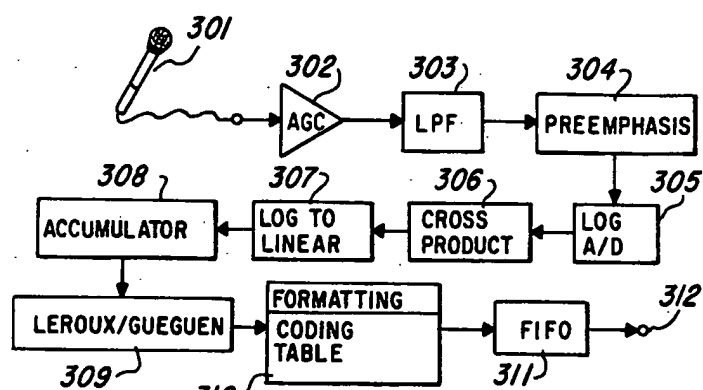


Fig. 3

# ELECTRONIC RECTIFIER/MULTIPLIER/LEVEL SHIFTER

## BACKGROUND

This invention relates to rectifiers or multipliers and more particularly to semiconductor rectifiers and multipliers.

The need to rectify input signals has long existed in the art. Generally the rectification of a signal is accomplished through the use of diodes and rectifier tubes. As discrete devices though, diodes and rectifier tubes require a minimum threshold before they allow the current to pass. This threshold level causes a clipping action which is highly undesirable in many circuits.

Analog signal multiplication is typically performed through the use of amplifiers. This operation as well requires a threshold voltage; therefore, low voltages are not multiplied whatsoever.

Little or no analog signal multiplication or rectification is done through an integrated circuit. This is due to the limitation on presently used rectification methods which prevent them from being amenable to integration.

## SUMMARY OF THE INVENTION

The present invention utilizes a capacitor means which is coupled to an incoming analog signal and additionally to ground. A switching means connects either the first or the second node of the capacitor means to the output depending upon the polarity of the incoming analog signal. In this fashion the incoming analog signal is rectified.

Additionally the present invention encompasses the architecture wherein the capacitor means contains a plurality of individual capacitors which are selectively coupled in parallel or in series so as to multiply the incoming analog signal accordingly.

The plurality of capacitors being selectively coupled either in parallel or in series is also advantageous because the capacitors when coupled in parallel may sample the incoming analog signal as referenced to one reference voltage and when switched to the output as series-connected capacitors may be referenced to another reference voltage, thereby allowing the incoming analog signal to be level shifted.

In the preferred embodiment of the invention two capacitors are used which are switchable from parallel to series interconnection. The incoming analog signal in the rectification operation is communicated to both capacitors being in parallel while the second node of the capacitors is connected to ground. The capacitors are then switched to series, being disconnected from the incoming analog signal, and either the first node of the series or the second node of the series is communicated as the rectified output signal depending upon the sign of the input analog signal. The decision as to the sign of the input analog signal is done by way of a comparator connected to ground which activates the appropriate switches.

In this fashion the input analog signal is multiplied (doubled) and rectified by the circuitry. This particular architecture is compatible with semiconductor implementation and particularly compatible with metal-oxide-silicon (MOS) applications.

The invention is further explained by the following description and its applicability.

## DESCRIPTION

In general the recognition of an analog or spoken signal entails the translation of the spoken signal into an electronic signal. This is typically done by way of a microphone or other such signal pick up device. This electronic signal is manipulated to be in the proper format for later use. The formatted signal is analyzed so as to develop appropriate data therefrom. This analysis data is used to determine or recognize which word or phrase has been spoken in the original analog input. The recognized word or phrase has an identifying indicia associated therewith which is used for storage, later reference, or control of an apparatus.

In this context the alteration or change of an operation is as simple as communicating the indicia to an operator or as complex as the control of some other electronic apparatus.

### Formatting:

The electronic signal from the microphone or other such pick up means is manipulated so that it is either rectified, multiplied or otherwise structured so as to place it in a better condition for the analysis. This formatting of the electronic signal speeds up the entire operation significantly.

Rectification of the signal is particularly important so as to allow reduced circuitry. In the preferred embodiment of rectification, the incoming signal is communicated to a plurality of capacitors. A sensing means, connected to ground, activates switches so as to tap the node of the capacitors which rectifies the incoming signal.

Multiplication is effected in the same circuitry by selectively connecting the capacitors in series (thereby multiplying the signal) or parallel (dividing the signal).

This switching operation maintains the signal between two bounds for ease in operating thereon.

The circuitry above is readily implementable on a semiconductor unit such as a metal-oxide-silicon (MOS) device.

### Analysis:

The preferred analysis operation passes the formatted electronic signal through an automatic gain control circuit (AGC) then through a low pass filter. In this context, it has been found that a low pass filter of 500 hertz (Hz) is suitable for this operation. The automatic gain control is used as an interface with the analog signal from the microphone. The AGC provides a more or less constant peak output level having a sufficient amplitude so as to drive the low pass filter and other components thereafter.

In this context, it has been found that an AGC having a peak signal level less than 80% of the full voltage and greater than 40% of full voltage provides satisfactory results. Additionally, a total 54 dB of gain reduction and a potential of better than 80 dB total gain is also desirable.

The low pass filter is used to roll off the high frequency components of the signal. The filter preferably provides an anti-aliasing for a signal so that no high frequency component of the signal overpowers the system sample rate of preferably 8 kHz so as to produce an interference signal. Preferably the cutoff frequency is 3.4 kHz.

The signal from the low pass filter is communicated to a pre-emphasis circuit so as to help eliminate any glottal waveform and lip radiation which may be included within the speech. It has been found that the



glottal waveform and lip radiation components of speech interfere dramatically with the vocal tract estimation when using linear predictive coding (LPC) analysis. In this context, it has been found that a pre-emphasis transformation of the formula:  $S(n) - uS(n-1)$ , where  $S(n)$  is the sample at time  $N$  and where preferably  $0.9 \leq u \leq 1.0$  performs suitably. This equation is preferably performed in an analog sample data domain.

The calculation of the autocorrelation terms in LPC analysis requires the computation of numerous multiplications and additions. So as to reduce the time necessary for these computations, a logarithmic analog to digital (Log A/D) converter is utilized which translates the analog signal from the pre-emphasis into its logarithmic digital equivalent. This allows the logarithmic digital equivalent sequence to be selectively added to other logarithmic digital equivalents so as to effectively perform a "logarithmic multiplication". The logarithmic multiplication product is thereafter transformed into its linear equivalent and selectively accumulated with other linear equivalents. In this fashion, the need to perform multiplications upon digital values is completely eliminated since only addition operations are necessary. This elimination of multiplication operations significantly accelerates the entire process allowing for "real time" operation.

The selective accumulation of the products generates autocorrelation terms which are utilized by the Le-Roux/Gueguen equations so as to develop reflection coefficients which are usable in an LPC synthesizer. The reflection coefficients are formatted and coded appropriately and then stored in a memory for later retrieval.

It is important to note that the reflection coefficients are particularly well suited for recognition and/or synthesis. Since they are already in proper format for synthesis, they are readily usable for matching to template data to determine the word, phrase, sentence, allophone, or sound.

#### Matching:

The preferred apparatus for matching the reflection coefficients derived from the spoken speech to template data involves dynamic programming which time warps the input to the template. Time warping is necessary since the same word takes a varying amount of time to be spoken by different people as well as by the same person. Time warping allows one frame of input to correspond to varying amounts of times within reference frames of the template.

For example, assume that  $N$  templates exist; that is,  $N$  words or phrases are independently recognizable. If template  $j$  has 50 frames associated therewith and each frame takes 25 milliseconds, then the speech input which takes 75 frames should not necessarily be discarded. A particular frame within the input is mapped to varying numbers of frames with the template.

In the computation, the minimal contour to a target frame of a particular template is determined. In this apparatus, only the past four columns of minimal distance or path data are kept. The preferred embodiment utilizes LPC-4 (linear predictive coding having a filter order of 4). The Euclidean distance between the input frame and each target frame of the template is computed. This generates, for time  $t$ , a distance column which is dynamically mapped to the minimal matrix for time,  $t-1$ ,  $t-2$ ,  $t-3$  and  $t-4$ . The minimal value between each value within the distance column and a prior minimum of the minimum matrix is derived. This generates

a minimum column. The minimum column replaces the oldest column within the minimum matrix.

Generally, this technique maps the minimum contour for a particular input frame being associated with a particular target frame within the template.

When the end of word is determined, whether by operator input or by sensing the amplitude of the speech, the most current upper value having the minimal value of all templates is chosen. The template associated therewith is the "best" match for the spoken word. The basic premise is to determine with which template does a sequence of input frames most closely align itself. The width of a frame is "warped" to allow an input frame to be associated with half, one, two, three, etc target frames.

In this manner the optimal match between the spoken word or phrase is made. The computation of the minimal value is performed continuously and only when the end of word or phrase is given is the minimal value of the templates determinative of the word having been spoken.

#### Recognition:

The preferred recognition apparatus utilizes a microphone with the LPC analysis already described together with the control means. The control means accepts the reflection coefficients developed through the analysis and compares these with template data. An indicia of the recognized template is communicated so as to communicate the word associated therewith.

Two semiconductor units are therefore all that is necessary so as to create a recognition device. Optionally, a read-only-memory (ROM) or other such memory device is usable for expansion of the vocabulary repertoire. An expansion of the template library is placed on the ROM.

Since two semiconductor units are all that is necessary, it is practical to make the recognition apparatus as a portable hand held device. Battery power, solar energy or other such means for portable power supply allows the device to be readily moved to remote areas for privacy or for a specific application.

This arrangement allows for the creation of a learning aid which accepts spoken words as well as tactile input data.

The following drawings with their accompanying descriptions and discussion more fully describe the present invention, its embodiment, and ramifications thereupon.

#### DRAWINGS IN BRIEF

FIG. 1 is a block diagram of a recognition apparatus.

FIG. 2 is an electrical schematic of the rectifier/multiplier electronic circuit device in accordance with the present invention.

FIG. 3 is a block diagram of the preferred embodiment of the analysis apparatus.

#### DRAWINGS IN DETAIL

FIG. 1 is a block diagram of an embodiment of the recognition operation. The analog input 105 from the operator is picked up by the signal pick up means 107. Signal pick up means 107 translates the analog input into an analog electronic signal 101 which is communicated to the signal manipulation means 108. The signal manipulation means 108 structures the analog electronic signal 101 into a form which is readily used by the analysis means 109. Manipulation includes rectification, multiplication, filtering, and the like.

The analysis means generates data and other indicia relative to the structured signal 102 so as to form a "fingerprint" of the original analog input 105. The analysis means 109 communicates this analysis data 103 to the recognition means 110. The recognition means 110 compares the analysis data to template data, not shown. Based upon this comparison, an indicia 104 is communicated to the operation alteration means 111 which generates control commands 106 thereupon.

In this fashion, the analog input is translated, matched to an appropriate template and is used to alter the operation of the present apparatus or some other device apparatus. This architectural arrangement allows for a spoken command to effectively control an apparatus.

FIG. 2 is a schematic of the rectifier/multiplier apparatus. The incoming signal 201 is selectively communicated to the capacitor 202. In this embodiment, two capacitors, 202a and 202b, are used which are matched as to their capacitive ability. In an alternative embodiment, multiple capacitors are used and their relative capacitance is varied selectively so as to provide more flexibility in signal manipulation.

Upon the input of the signal, the switch arrangement 204a and 204f is interconnected so that the incoming signal is communicated in parallel to both capacitors 202a and 202b. At the appropriate clocking pulse, capacitors 202a and 202b are switched to a serial arrangement so as to double the original incoming signal 201. This signal, through the use of the switch arrangement 205a-205d rectifies the signal to be of a particular polarity.

This arrangement is particularly adaptable to being placed upon a semiconductor device. Additionally, the architecture provides easy multiplication and rectification without the loss due to clipping or other inadequacies found in the prior art.

FIG. 3 is a block diagram of an embodiment of the analysis circuit. Microphone 301 receives the spoken analog signal which is communicated to an automatic gain control (AGC) 302.

The AGC 302 is used as an analog interface for the microphone 301. The AGC 302 provides a relatively constant peak output level having a sufficient amplitude so as to drive the low pass filter 303, the pre-emphasis 304, and the logarithmic analog to digital (Log A/D) 305. The AGC 302 in providing this peak output level, allows for low level input signals to be effectively utilized and thereby reduces clipping.

In this capacity it has been found that an AGC providing a peak signal of less than 80% of voltage rail and greater than 40% of the voltage rail is suitable. Additionally it has been found that a gain being incremented in six (6) dB steps is acceptable.

The signal from the AGC 302 is communicated to the low pass filter 303 which is used to withdraw high frequency components of the signal. The low pass filter 303 also gives an anti-aliasing of the signal so that a high component of the signal is not able to overpower the system sample rate of preferably 8 KHz. This significantly reduces the interference signal normally found in speech.

The signal from the low pass filter 303 is communicated to pre-emphasis 304. The pre-emphasis 304 is used to eliminate the glottal waveform and lip radiation components of speech. These components typically interfere with vocal tract estimation and therefore the pre-emphasis 304 provides for a more accurate linear predictive coding (LPC) analysis. The use of the pre-

emphasis 304 eliminates the variable frequency through a simple one pole differencing filter. In this context it has been found that a pre-emphasis being defined by the function:

$$\text{output} = S(n) - uS(n-1),$$

where  $S(n)$  is the sample at time  $n$  is acceptable.

The signal from the pre-emphasis 304 is communicated to the Log A/D 305 which translates the heretofore analog signal into its logarithmic digital equivalent. The translation to the logarithmic form allows for elimination of multiplication since logarithmic components, through their addition, effectively perform a multiplication.

The Log A/D 305 signal is communicated to a cross product means 306 which sums chosen elements from the Log A/D 305. These chosen sums are then translated to their linear equivalents 307 and subsequently accumulated selectively by an accumulator 308. In this process, the accumulator 308 generates reflection coefficients which are usable by the LeRoux/Gueguen formula 309 for the generation of autocorrelation terms.

The autocorrelation terms are preferably formatted/encoded so as to be usable in a speech synthesis device. The autocorrelation terms so formatted are stored in a memory 311 in a first-in-first-out (FIFO) arrangement so that they are retrievable upon demand at 312.

In this manner, the incoming signal is controlled and generates analysis data which is usable for recognition and/or synthesis of a mimic word.

What is claimed is:

1. An electronic circuit device for providing multiplication and rectification of an analog signal, said circuit device comprising:

an input for receiving the analog signal;

plural capacitor means operably coupled to said input and including at least first and second capacitors arranged to be alternatively coupled in parallel relationship in a first phase and in series relationship in a second phase;

a first switching network operably connected to said plural capacitor means and having first and second switching relationships with respect to said at least first and second capacitors interconnecting said at least first and second capacitors in parallel relationship and in series relationship respectively;

control means operably connected to said first switching network for determining the switching relationship of said first switching network with respect to said at least first and second capacitors; said first switching network initially being in said first switching relationship interconnecting said at least first and second capacitors in parallel relationship for reception of the analog signal from said input and being responsive to said control means for switching to said second switching relationship interconnecting said at least first and second capacitors in series relationship such that the original analog signal is multiplied; and

a second switching network operably connected to the output of said plural capacitor means and having first and second switching relationships with respect to said at least first and second capacitors depending upon the polarity of the analog signal received at said input for selectively providing as the output signal, the signal from one of said capac-

itors such that the output signal is rectified to be of a particular polarity.

2. An electronic circuit device as set forth in claim 1, further including comparator means coupled to said input and to a source providing a reference voltage for comparing the analog signal from said input with the reference voltage to derive a polarity indication of said analog signal; and

the output of said comparator means being operably coupled to said second switching network to communicate the polarity of said analog signal thereto.

3. An electronic circuit device as set forth in claim 1, wherein said control means comprises a timing clock for providing clocking pulses at predetermined time intervals to said first switching network to which said first switching network is responsive in switching between said first and second switching relationships.

4. An electronic circuit device as set forth in claim 3, wherein said first switching network comprises a plurality of MOS transistors operating in a switching mode.

5. An electronic circuit device as set forth in claim 4, wherein said second switching network comprises a second plurality of MOS transistors operating in a switching mode.

6. An electronic circuit device as set forth in claim 5, wherein said electronic circuit device has a single semiconductor substrate on which said plural capacitor means and said MOS transistors included in said first and second switching networks are integrated.

7. An electronic circuit device as set forth in claim 1, wherein said at least first and second capacitors as coupled in parallel relationship in said first phase are referenced to a first reference voltage; and

said at least first and second capacitors as coupled in series relationship in said second phase are referenced to a second reference voltage different from said first reference voltage such that level shifting of the original analog signal occurs.

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# United States Patent [19]

Topich

[11] Patent Number: 4,485,433

[45] Date of Patent: Nov. 27, 1984

[54] INTEGRATED CIRCUIT DUAL POLARITY  
HIGH VOLTAGE MULTIPLIER FOR  
EXTENDED OPERATING TEMPERATURE  
RANGE

[75] Inventor: James A. Topich, Centerville, Ohio

[73] Assignee: NCR Corporation, Dayton, Ohio

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[22] Filed: Dec. 22, 1982

[51] Int. Cl.<sup>3</sup> ..... H02M 3/18

[52] U.S. Cl. .... 363/60; 363/65;  
307/110

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307/110

Attorney, Agent, or Firm—J. T. Cavender; Casimer K. Salys; T. Rao Coca

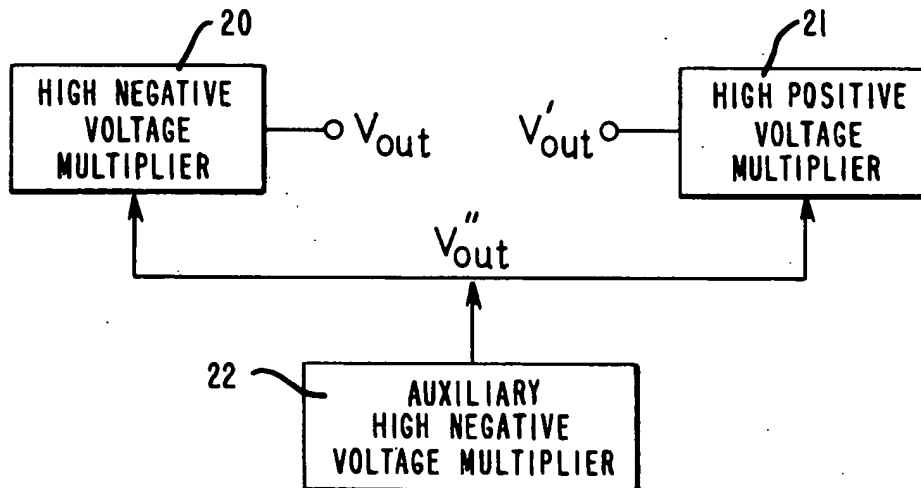
## [57] ABSTRACT

Disclosed is an on-chip, dual polarity high voltage multiplier circuit consisting of a main high positive voltage multiplier and high negative voltage multiplier and an auxiliary high negative voltage multiplier coupled to the main multipliers to prevent turning on of parasitic transistors associated with the MOS diodes of the main multipliers and thereby extend the operating temperature range to 150° C. and improve the fall time of the dual polarity multiplier. The auxiliary multiplier may be located in a common p-well with the main positive and negative multipliers or with the main negative multiplier and its output voltage is connected to this common well.

Primary Examiner—William M. Shoop

Assistant Examiner—Anita M. Ault

10 Claims, 7 Drawing Figures



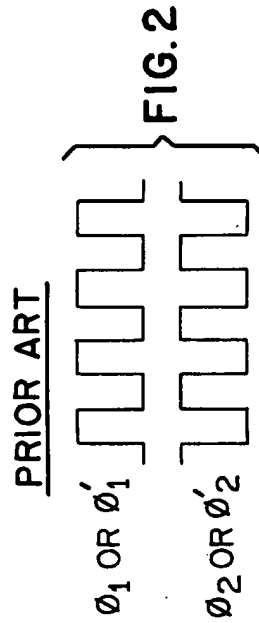
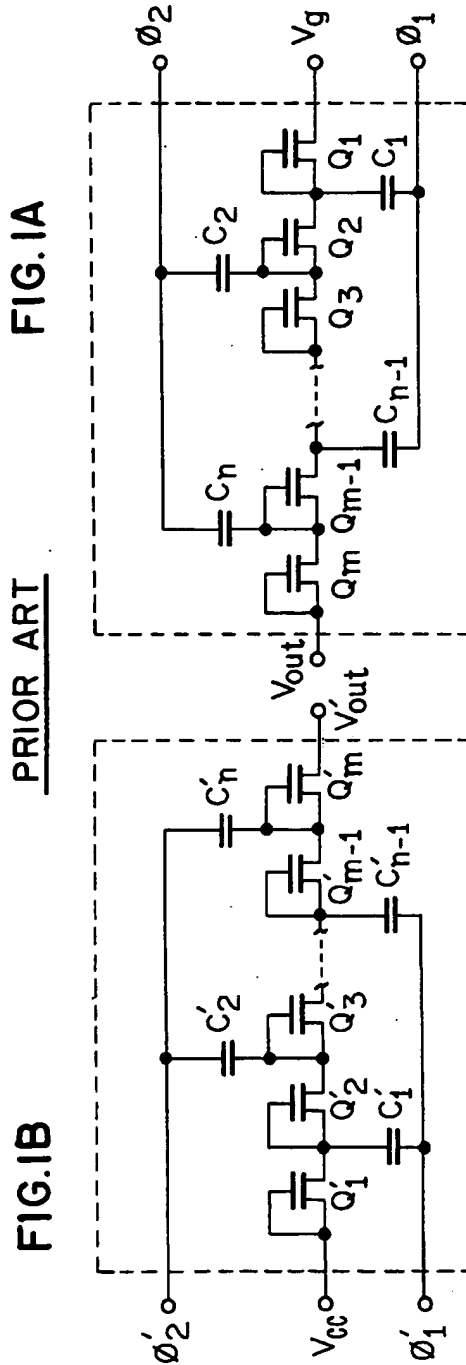


FIG. 3

PRIOR ART

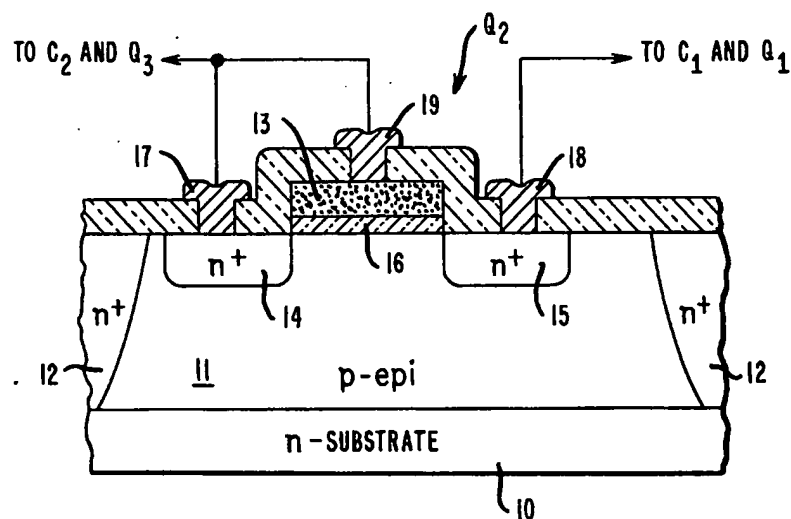
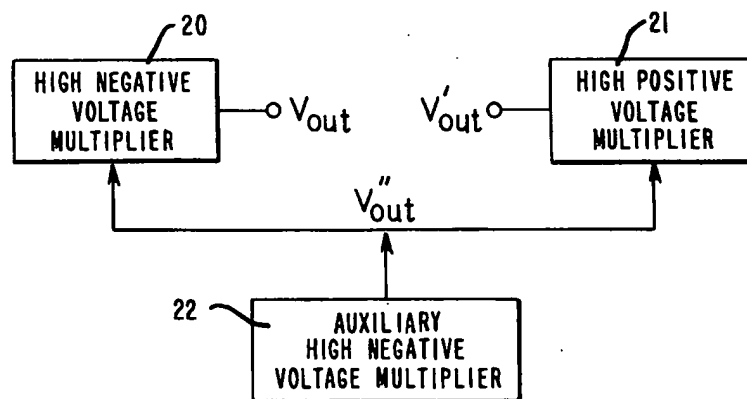


FIG. 4





# INTEGRATED CIRCUIT DUAL POLARITY HIGH VOLTAGE MULTIPLIER FOR EXTENDED OPERATING TEMPERATURE RANGE

## BACKGROUND OF THE INVENTION

This invention relates to an on-chip, dual polarity, high voltage multiplier and, more particularly, to a voltage multiplier having an extended operating temperature, as high as 150° C.

As used throughout, the following two definitions apply:

"Rise time" is the time taken by the positive voltage multiplier to increase its output voltage from approximately the 10% level to the 90% level of the final voltage.

"Fall time" is the time taken by the negative voltage multiplier to decrease its output voltage from approximately the 10% level to the 90% level of the final voltage.

To be competitive in the marketplace, a non-volatile memory device is now required to be a "5 volt only" device. This means that the memory device, for example a non-volatile random access memory (NVRAM), which typically requires multiple external power supplies (providing +5 volt, +22 volt and -22 volt voltages for read, write and erase operations, respectively) should have the capability to generate the high write and erase voltages, on chip, by utilizing a single 5 volt external power supply. One method of on-chip high-voltage generation is by means of the voltage multiplier technique. One such prior art voltage multiplier is shown in FIGS. 1A and 1B which represent circuits for generating a low negative voltage and a high positive voltage, respectively.

Referring to FIG. 1A,  $V_g$  represents the ground connection and  $V_{out}$  is the voltage output of the negative multiplier.  $V_{out} \ll V_g$ .  $C_1, C_2 \dots C_n$  are coupling capacitors and  $Q_1, Q_2 \dots Q_m$  are rectifying elements (or diodes). In this prior art voltage multiplier arrangement, the capacitors were permanent capacitors (i.e. their operation is not dependent on the polarity of the voltage applied across their plates) and the rectifying elements were diode-connected enhancement mode metal-oxide-semiconductor (MOS) transistors.

Referring to FIG. 1B,  $V_{cc}$  here represents the input power supply voltage, typically 5 volts and  $V'_{out}$  is the voltage output of the positive voltage multiplier.  $V'_{out} \gg V_{cc}$ . As in FIG. 1A,  $C'_1, C'_2 \dots C'_n$  and  $Q'_1, Q'_2 \dots Q'_m$  represent coupling capacitors and diodes, respectively.

$\phi_1$  and  $\phi_2$  shown in FIG. 1A and  $\phi'_1$  and  $\phi'_2$  shown in FIG. 1B designate two clock pulses, of the type shown in FIG. 2, having a fixed amplitude and in antiphase with each other. These pulses are applied to the successive nodes of the diode-chain via the coupling capacitors. The amplitude of these clock pulses is typically about 5 volts.

The output nodes  $V_{out}$  and  $V'_{out}$  of the negative and positive voltage multipliers shown in FIGS. 1A and 1B are connected together to generate high positive and low negative voltages at the same (output) node. This ability is essential for an on-chip voltage multiplier since devices on an integrated circuit chip, such as NVRAMs, invariably require that the same node of the voltage multiplier go both positive and negative for purposes of programming the device.

In actual construction of the on-chip dual polarity voltage multiplier, it is necessary that the MOS diode elements  $Q_1, Q_2 \dots Q_m$  of the negative multiplier be located in regions of the substrate isolated from the remainder of the chip. This is necessary because the negative voltage multiplier pulls the isolated region negative with its output voltage. If isolation was not used, turning on of the negative voltage multiplier would interfere with the functioning of the peripheral circuits. The isolated region may be either a diffused well or an isolated epitaxial region formed on the substrate. For example, if the diodes  $Q_1, Q_2 \dots Q_m$  are n-channel MOS devices, the diffused well approach will utilize an n-type substrate in which p-wells are formed. The corresponding isolated epitaxial region approach, which is disclosed in the copending application Ser. No. 410,674, entitled "Method of Fabricating An I.C. Voltage Multiplier" by the present inventor and assigned to the assignee of the present invention, is shown in FIG. 3. This approach involves using an n-type substrate 10 (typically, single crystal silicon) having thereon a p-type epitaxial silicon layer (hereafter, p-epi layer) 11 flanked by deep N<sup>+</sup> diffusions 12. The diffusions 12—12 isolate the p-type epitaxial layer 11 from the remainder of the integrated circuit.

Regardless of whether the diffused well or isolated epitaxial region approach is chosen, the dual polarity voltage multiplier suffers from (1) a slow response (i.e. long fall time) of the negative multiplier due to a large substrate to p-epi/p-well junction capacitance  $C_{\pi}$  and (2) rapid deterioration of the negative voltage multiplication scheme at elevated temperatures due to the turning on during the negative cycle of the clock pulses  $\phi_1$  and  $\phi_2$  of parasitic transistors associated with the MOS devices. To fully understand these problems, reference is made to FIG. 3 wherein is shown, in cross-sectional representation, the diode  $Q_2$  (of FIG. 1A). The diode  $Q_2$  shown in FIG. 3 is an n-channel MOS transistor and comprises a conductive polysilicon gate 13 and highly doped n<sup>+</sup> drain and source regions 14 and 15, respectively. A relatively thin silicon dioxide (gate oxide) 16 insulates the polysilicon gate 13 from the underlying p-epi region 11. Transistor  $Q_2$  further includes metal contacts 17, 18, and 19 making electrical contact, respectively, with drain 14, source 15 and gate 13. For consistency with FIG. 1A, gate 13 and drain 14 of transistor  $Q_2$  shown in FIG. 3 are connected together and this common point is connected to the (source of) transistor  $Q_3$  and one plate of coupling capacitor  $C_2$  and the source 15 of  $Q_2$  is connected to coupling capacitor  $C_1$  and transistor  $Q_1$ .

In operation, a nominal 5 volt potential is always applied to the substrate 10. For the low negative voltage multiplication to take place the p-epi layer 11 to n-substrate 10 junction capacitance  $C_{\pi}$  needs to be charged. However, because the parasitic bipolar transistor formed by the n<sup>+</sup> drain 14, the p-epi region 11 and the n-substrate 10 is turned on whenever the n<sup>+</sup> region 14 is pulled more negative than the p-epi region 11, the effective capacitance of the p-epi to substrate 10 junction  $C_{eff}$  will be increased by a factor equal to the current gain B of the parasitic transistor mentioned hereinabove. In other words,  $C_{eff}$  is equal to  $B \times C_{\pi}$ . The gain B is inversely proportional to the thickness of the p-epi layer 11 and typically is high, of the order of one hundred or more. As a result of this large effective capacitance, the p-epi to n-substrate capacitor will be charged



rather slowly and thereby the fall time of the negative voltage multiplier will be undesirably increased.

The deterioration in the performance of the negative voltage multiplier with increasing temperature referred to hereinabove is due to the relative ease of turning on of the parasitic bipolar transistor 14-11-10 (FIG. 3) during the negative cycle of the waveforms  $\phi_1$  and  $\phi_2$  which drive the multiplier. As temperature increases, the built-in potential of the parasitic bipolar transistor pn junctions will decrease, making this parasitic transistor turn on more easily. Consequently, the parasitic transistor will compete with the MOS transistor  $Q_2$  and will transfer off more and more voltage multiplier output current to the substrate 10 via the parasitic transistor rather than enabling the output current to be transferred to the successive stages of the negative voltage multiplier. As a result of this competition between the parasitic bipolar transistor and the MOS transistor, the negative voltage multiplication will deteriorate.

The positive voltage multiplier in the dual polarity voltage multiplier pair (shown in FIG. 1B) does not suffer from the above problems associated with the negative multiplier since the parasitic transistors associated with the MOS diodes that are utilized in the construction of the positive voltage multiplier are not turned on. This is because the p-epi region similar to 11 in this case is always at least 5 V more negative than any of the  $n^+$  regions similar to 14 (FIG. 3). Consequently, the waveforms  $\phi_1$  and  $\phi_2$  (which are  $\pm 5$  V) can never bring the  $n^+$  region to a more negative potential than the p-epi region. Since the parasitic transistors are not turned on, there is no shunting of current from the positive multiplier output node to the substrate. Also, since there is no need for charging up the p-epi layer to substrate 10 capacitance, the rise time of the positive voltage multiplier is not affected.

One way of solving the above problems associated with the negative voltage multiplier is to connect the output of the negative multiplier  $V_{out}$  (FIG. 1A) to the p-epi well region 11 and thereby reducing the current going to substrate 10 (FIG. 3). However, this is not practical, since the output node  $V_{out}$  of the negative multiplier is connected to the output node  $V'_{out}$  of the positive multiplier and this common node goes both positive and negative during the operation of the positive multiplier and negative multiplier respectively. As a result, whenever the positive output of this common node is applied to the p-epi well region 11, the pn junction (isolation diode) formed by the p-epi region 11 and the n-substrate 10 will be forward biased, thereby limiting the positive voltage to an isolation diode drop higher than the bias on the n-substrate 10. Consequently, the positive voltage multiplier operation will be severely inhibited.

### SUMMARY OF THE INVENTION

It is an object of the present invention to provide an on-chip, dual polarity voltage multiplier capable of operating in the wide temperature range of  $(-55$  to  $150)^\circ\text{C}$ .

It is another object of this invention to provide an on-chip, dual polarity voltage multiplier having an improved fall time.

These and other objects are accomplished by means of an auxiliary, on-chip, negative voltage multiplier which is located in the common p-well of the dual polarity voltage multiplier and whose low negative voltage output is connected to the common p-well. Alter-

nately, the auxiliary voltage multiplier may be located in a separate p-well and its output is connected to the p-well in which the main negative voltage multiplier is located. The voltage output of the auxiliary multiplier is lower (i.e. more negative) than the negative voltage output of the dual polarity voltage multiplier to ensure that parasitic transistors associated with the negative voltage multiplier are not turned on during operation of the dual polarity multiplier. Since the parasitic transistors associated with the negative multiplier are not turned on, it is possible to enhance the dual polarity multiplier operating temperature range and significantly reduce its fall time.

### BRIEF DESCRIPTION OF THE DRAWING

FIGS. 1A and 1B are schematic diagrams of prior art voltage multiplier circuits. FIG. 1A represents a negative voltage multiplier and FIG. 1B represents a positive voltage multiplier.

FIG. 2 is a schematic representation of the voltage waveforms (clock pulses) applied to the successive nodes of the voltage multiplier.

FIG. 3 is a partial sectional view of the transistor  $Q_2$  shown in FIG. 1A.

FIG. 4 is a block diagram illustrating the dual polarity voltage multiplier for extended operating temperatures in accordance with the principles of the present invention.

FIG. 5 is a partial sectional view of the auxiliary voltage multiplier output connection.

FIG. 6 is a graphical comparison of the output characteristics at different temperatures of a negative voltage multiplier constructed in accordance with the present invention and a conventional negative voltage multiplier.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In one illustrated embodiment, shown in block diagram representation in FIG. 4, the on-chip, dual polarity high voltage multiplier for extended operating temperature range comprises a high negative voltage multiplier 20 having an output designated as  $V_{out}$ , a high positive voltage multiplier 21 having an output  $V'_{out}$  and an auxiliary high negative voltage multiplier 22 having an output designated as  $V''_{out}$ . The outputs  $V_{out}$  and  $V'_{out}$  are connected together to generate the necessary high write and erase voltages at the same node. These voltages are typically about  $\pm(20-25)$  volts.

Multipliers 20 and 21 may be constructed by means of permanent coupling capacitors and n-channel MOS transistors (diodes) using the voltage multiplication scheme shown in FIGS. 1A and 1B, respectively. (The necessity for using permanent capacitors rather than depletion mode transistors arises from the need to generate at a common output node of multipliers 20 and 21 both positive and negative voltages. If depletion mode devices are used as coupling capacitors, then, many of the depletion devices in each multiplier scheme shown in FIGS. 1A and 1B will be turned off whenever the common output node goes to a polarity opposite to the output polarity of the individual multipliers 20 and 21, thus hampering the operation of these multipliers.) In the alternative, the coupling capacitors may be parallel plate capacitors using polysilicon as the plate material. The coupling capacitors  $C_1, C_2 \dots C_n$  and  $C'_1, C'_2 \dots C'_n$  and MOS transistors  $Q_1, Q_2 \dots Q_m$  and  $Q'_1, Q'_2 \dots Q'_m$  of multipliers 20 and 21, respectively, may be

located in a common p-well (whether it be a p-well diffused into an n-type substrate or a p-epi layer formed on an n-type substrate and flanked on all sides by deep  $n^+$  diffusions) or in individual p-wells (one p-well per multiplier) depending on the layout of the remainder of the I.C. on the chip. The number of voltage multiplication stages necessary for multipliers 20 and 21 is dictated by the required write and erase voltages of the devices on the chip, the higher the required voltage, the more are the number of stages. The output current requirements of multipliers 20 and 21 are also dictated by the requirements of the I.C. on the chip. Typically, for NVRAMs the positive and negative currents required are approximately 100 microamps.

Referring to FIG. 4, the output  $V''_{out}$  of the auxiliary multiplier 22 is connected to the p-well(s) in which the MOS transistors constituting the individual multipliers 20, 21 (and 22) are located to maintain the p-well(s) always (i.e. regardless of operating temperature) at a sufficiently low negative potential to prevent turning on of the parasitic bipolar transistors associated with the MOS transistors  $Q_1, Q_2 \dots Q_m$  of the negative voltage multiplier 20 (and the auxiliary multiplier 22). Since the parasitic transistors associated with the transistors  $Q_1, Q_2 \dots Q_m$  are not turned on even at high operating temperatures (of the order of  $150^\circ \text{C}$ .), the negative voltage multiplier output current transfer by these parasitic devices to the substrate, which is characteristic of prior art voltage multiplier circuits, is eliminated and an extended operating temperature capability for the dual polarity voltage multiplier is achieved.

The auxiliary negative voltage multiplier 22 may be constructed using the voltage multiplication scheme shown in FIG. 1A. For convenience, the capacitors and MOS transistors which constitute the auxiliary multiplier 22 are designated as  $C'_1, C'_2 \dots C'_n$  and  $Q''_1, Q''_2 \dots Q''_m$ , respectively. In this construction, the coupling capacitors  $C'_1, C'_2 \dots C'_n$  may be depletion mode transistors rather than permanent capacitors since the output node of the auxiliary multiplier 22 always remains at negative polarity and there is no possibility of the depletion mode devices being turned off and the auxiliary multiplier made non-functional. The transistors  $Q''_1, Q''_2 \dots Q''_m$  may be n-channel MOS devices of the type used in the construction of multiplier 20. One such MOS transistor  $Q''_m$  which corresponds to the final stage of the auxiliary multiplier 22, is shown in cross-sectional representation in FIG. 5.

In FIG. 5, the various parts of the transistor  $Q''_m$  structure designated by double primed numerals  $10''$  to  $19''$  correspond to like parts of transistor  $Q_2$  structure shown in FIG. 3 and designated by numerals 10 to 19 with the exception that p-epi region  $11''$  may be a common well in which the various components of all the three multipliers 20, 21 and 22 or at least the components of multipliers 20 and 22 (FIG. 4) are located. As shown in FIG. 5, the final voltage output  $V''_{out}$  of the auxiliary multiplier 22 which is generated at the drain  $14''$  is applied to the common p-well  $11''$  via the enhanced contact region  $23''$  which is formed to enhance the metal connection  $24''$  to the p-epi well  $11''$ . A method of accomplishing this enhanced metal-to-p-contact is disclosed in the copending U.S. patent application Ser. No. 409,193 entitled "Epitaxial Contact Fabrication Process" by John E. Dickman, Raymond A. Turi and the present inventor, and assigned to the assignee of the present invention.

Since the positive voltage multiplier 21 (FIG. 4) does not suffer from the turning on of parasitic transistors associated with the MOS diodes utilized in its construction (since the p-epi region 11 in this case is always at a potential more negative than any of the  $n^+$  regions, see FIG. 3), there is no requirement for the output  $V''_{out}$  of the auxiliary multiplier 22 to be applied to the p-epi region in which the MOS devices of multiplier 21 are located. Thus, if the MOS devices of multiplier 21 are located in a first p-epi region on the substrate and the MOS devices of multipliers 20 and 22 are located in a second and third p-epi regions (or a common p-epi region) on the substrate, then to extend the operating temperature of the dual voltage multiplier, the output  $V''_{out}$  of multiplier 22 needs to be connected only to the second and third p-epi regions (or the common p-epi region).

In designing the auxiliary negative multiplier 22, the voltage output  $V''_{out}$  should be at least (3-5) volts more negative than the maximum negative voltage generated on the chip (i.e. the output  $V_{out}$ ) to ensure that the parasitic transistors associated with the negative voltage multiplier 20 are not turned on. Referring to FIG. 3, by maintaining the p-epi well 11 at a more negative potential than the  $n^+$  region 14, the bipolar transistor 14-11-10 is prevented from turning on. In order to generate the above-mentioned low voltage, it is necessary that the auxiliary multiplier 22 be regulated at a voltage more negative than the negative voltage multiplier 20.

The auxiliary multiplier 22 need not have a shorter fall time than the multiplier 20 since the sole function of multiplier 22 is to generate a more negative voltage than  $V_{out}$  and continuously supply this voltage to the p-epi well region(s).

Referring to FIG. 4, although the voltage output  $V''_{out}$  of the auxiliary multiplier 22 is required to be more negative than the output  $V_{out}$  of multiplier 20, there is no such requirement with regard to the output current of the auxiliary multiplier 22. In fact, the auxiliary multiplier 22 need not generate a high current. The output current of multiplier 22 may be of a value which is sufficient to maintain the p-well(s) of multipliers 20 and 22 charged (i.e. maintain the p-epi to n-substrate capacitance charged) during operation of the dual polarity voltage multiplier shown in FIG. 4. In this connection, it is important to take into consideration the substrate current (i.e. the current that is shunted to the substrate  $10''$  (FIG. 5) on which the auxiliary multiplier is located due to the switching of the voltage waveforms  $\phi_1$  and  $\phi_2$  (FIG. 2) which are applied to drive the multiplier). The substrate current is a function of the current gain of the parasitic npn transistor formed between the  $n^+$  region 14, p-epi region  $11''$  and the substrate  $10''$  (FIG. 5). The substrate current will increase with the current gain of the parasitic transistor. If the current gain is too large, then all of the output current that the multiplier can generate will go to the substrate and the operation of the dual polarity voltage multiplier will be jeopardized since there will be no output current available at  $V''_{out}$  (FIG. 4) for driving (i.e. charging) the p-well(s) of other multipliers. Because the current gain of parasitic transistors is inversely proportional to the p-epi region  $11''$  thickness, one way of decreasing the current gain (and therefore decreasing the substrate current and increasing the output current) is to use a thick, of the order of (15-18) microns thickness, p-epi layer  $11''$ .

The auxiliary multiplier output current and substrate current are functions of temperature as well. At room temperature, the substrate current is typically about twice that of the output current. At a high temperature of about 150° C., the substrate current may be three times as large as the output current. The reason for the increase in substrate current at high temperatures is due to the parasitic npn transistors being easily turned on as temperature increases.

Since the auxiliary multiplier 22 should generate a more negative voltage output  $V'_{out}$  than the output  $V_{out}$  of negative multiplier 20 (FIG. 4) but need not provide a larger output current than that of multiplier 20 or have a smaller fall time than that of multiplier 20, the number of voltage multiplication stages needed to construct the multiplier 22 could be smaller than that of multiplier 20.

### CHARACTERIZATION

The performance of a voltage multiplier circuit in accordance with the present invention was evaluated by fabricating, testing at various temperatures and evaluating two negative multiplier circuits, one having the auxiliary voltage multiplier and the second without the auxiliary multiplier. The main negative multiplier circuits and the auxiliary multiplier circuit each consisted of eighteen stages, but they were regulated at different voltages. The negative multipliers were regulated at a voltage of -20 volts and the auxiliary multiplier was regulated at a more negative voltage of -25 volts. The coupling capacitors used in this construction were parallel polysilicon plate capacitors and the rectifying elements were n-channel MOS transistors. The multipliers were fabricated using the process disclosed in the previously-mentioned U.S. application Ser. No. 410,674, by the present inventor. In the case of the negative multiplier having the auxiliary multiplier, each multiplier was located in a separate p-epi well and the output of the auxiliary multiplier was tied to both p-epi wells. The p-epi layer thickness was approximately 15 microns.

The test results are illustrated in FIG. 6 showing the I-V characteristics of the negative multipliers with and without the use of the auxiliary multiplier at the room temperature of 25° C. and a high 150° C. temperature. The I-V characteristics of the multiplier paired with the auxiliary multiplier is shown by the continuous lines and those of the multiplier without the auxiliary multiplier are shown by the dashed lines. The voltage multiplier output current plotted on the vertical axis is negative in accordance with the convention that in a negative voltage multiplier circuit current flows into the multiplier output node.

It is quite apparent from FIG. 6 that the I-V characteristics of the negative voltage multiplier without the auxiliary multiplier degraded quite significantly at the high temperature as compared with its characteristics at room temperature. First, this voltage multiplier was able to generate an output current only in the low voltage range of 0 to -12 volts. Second, the output current of this multiplier was also low of approximately 0 to -50 microamps. Both of these results render this multiplier unsuitable at high temperatures for most, on-chip, voltage generation purposes.

In contrast with the poor results obtained with the single voltage multiplier, the negative multiplier paired with the auxiliary multiplier has excellent operational features. In this case, the I-V characteristics were essentially independent of temperatures in the range

(25-150)°C. The circuit generated high negative output voltages of more than about -20 volts. The output current of this multiplier was sufficiently high, in the range of about (-60 to -95) microamps.

Thus, there has been described a dual polarity, high voltage multiplier having the capability of operating at an extended temperature range of up to 150° C. by means of an, on-chip, auxiliary negative voltage multiplier whose output is continuously applied to the common p-well of all the multipliers that constitute the dual polarity multiplier or to the individual p-wells of each negative multiplier. Since the output voltage of the auxiliary multiplier is more negative than that of the main negative multiplier, the p-wells are always maintained at a low enough potential to prevent turning on of parasitic bipolar transistors associated with the MOS devices used for the individual multiplier construction. In this manner, the substrate current which jeopardizes the dual polarity voltage multiplier operation is eliminated. Since the p-wells are maintained at a low negative potential at all temperatures of up to 150° C., extended operating temperature capability of the dual voltage multiplier is achieved. Also, since the p-well is always maintained at a low potential, the need for charging the p-epi-to-substrate capacitance is eliminated. Consequently, the fall time of the dual voltage multiplier is significantly improved.

While the invention has been described in connection with the use of an on-chip auxiliary negative voltage multiplier to extend the operating temperature range of an on-chip dual polarity high voltage multiplier, the invention, however, is not so limited. Another application of the auxiliary multiplier involves its use with a back bias generator to extend the operating temperature range of the back bias generator circuit. The back bias generator typically comprises a negative voltage multiplier, having a low negative voltage (-2 volts to -5 volts) output and constructed using coupling capacitors and MOS diodes connected in the voltage multiplication scheme shown in FIG. 1A. The back bias generator suffers from loss of current to the substrate, particularly at high temperatures, due to the turning on of parasitic bipolar transistors associated with the various (n-channel) MOS diodes located on a p-epi/p-well region of the (n-type) substrate. One way of solving this problem is to connect the output node of the back bias generator to its own p-well/p-epi region. However, to compensate for the loss of current to the substrate, the back bias generator will then have to generate a current which is significantly larger than the required output current. For example, if the required output current is about 100 microamps, the back bias generator will have to generate a current of as much as 200 microamps. In order to generate this large current the coupling capacitors constituting the back bias generator will have to be large (in area). However, these large capacitors will consume a large area of valuable chip real estate thereby decreasing device density on the chip.

By using an auxiliary negative voltage multiplier whose output is connected to the p-well/p-epi region in which the MOS diodes of back bias generator are located the above problems associated with the conventional back bias generator are solved. The auxiliary voltage multiplier output voltages and current for this application are sufficiently small of about (-5 to -8) volts and (1-10) microamps, respectively. These outputs maintain the p-epi/p-well region of the back bias generator sufficiently more negative than the n<sup>30</sup> re-

gions associated with the MOS devices and prevent turning on of the parasitic bipolar devices associated therewith. Since the auxiliary voltage multiplier output current is small, the coupling capacitors constituting the auxiliary multiplier are small (in area). Thus, even though an additional, on-chip, (auxiliary) voltage multiplier is used with the back bias generator, a net savings in chip real estate is obtained.

Since, typically, the output voltage of the auxiliary multiplier for the back bias generation application need not be more than about -8 volts, the auxiliary multiplier in this case can be constructed with 2 or 3 voltage multiplication stages.

While the invention has been shown and described with respect to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

I claim:

1. A dual polarity voltage amplifier integrated circuit on a semiconductor substrate of a first conductivity type having an isolated region of an opposite conductivity type, said circuit comprising:

a positive voltage multiplier consisting of a plurality of coupling capacitors and metal-oxide-semiconductor (MOS) diodes connected together for generating a positive output voltage, said MOS diodes being located in said isolated region;

a negative voltage multiplier consisting of a plurality of coupling capacitors and MOS diodes for generating a negative output voltage, said negative multiplier MOS diodes being located in said isolated region; and

an auxiliary voltage multiplier consisting of a plurality of coupling capacitors and MOS diodes for generating a negative output voltage more negative than said negative multiplier output, said auxiliary multiplier MOS diodes being located in said isolated region and said auxiliary multiplier output applied to said isolated region.

2. A dual polarity voltage multiplier integrated circuit on a semiconductor substrate of a first conductivity type having a plurality of isolated regions of a conductivity type opposite to said first conductivity type, said circuit comprising:

a positive voltage multiplier having a plurality of coupling capacitors and metal-oxide-semiconductor (MOS) diodes connected together for generating a positive output voltage, said MOS diodes being located in a first isolated region;

a negative voltage multiplier having a plurality of coupling capacitors and MOS diodes connected together for generating a negative output voltage, said negative multiplier MOS diodes being located in a second isolated region; and

an auxiliary negative voltage multiplier having a plurality of coupling capacitors and MOS diodes connected together for generating a negative output voltage more negative than the output voltage of said negative multiplier, said auxiliary multiplier MOS diodes being located in a third isolated region

and said auxiliary multiplier output voltage applied to said second and third isolated regions.

3. The circuit as in claim 2 wherein the coupling capacitors are parallel polysilicon plate capacitors.

4. The circuit as in claim 2 wherein the coupling capacitors constituting said positive voltage multiplier and negative voltage multiplier are parallel polysilicon plate capacitors and the coupling capacitors constituting the auxiliary multiplier are depletion-mode devices.

5. The circuit as in claim 2 wherein said substrate is n-type single crystal silicon and said first and second regions are p-type epitaxial silicon.

6. A voltage multiplier circuit on an n-type semiconductor substrate having a first and second p-type isolated regions thereon, said circuit comprising:

a first voltage multiplier having a plurality of coupling capacitors and metal-oxide-semiconductor (MOS) diodes connected together for generating a negative voltage output, said first multiplier MOS diodes being located in said first p-type region; and a second voltage multiplier having a plurality of coupling capacitors and MOS diodes connected together for generating a negative voltage output more negative than said first multiplier output, said second multiplier MOS diodes being located in said second p-type region and said second multiplier output connected to said first and second p-type regions.

7. The circuit as in claim 6 further comprising a third voltage multiplier having a plurality of coupling capacitors and MOS diodes connected together for generating a positive voltage output, said third multiplier MOS devices being located in said first or second p-type region.

8. The circuit as in claim 7 wherein said substrate is single crystal silicon and said p-type regions are epitaxial silicon.

9. A dual polarity high voltage multiplier integrated circuit on an n-type semiconductor silicon substrate having an isolated p-type epitaxial silicon region thereon, said circuit comprising:

a first voltage multiplier having a plurality of coupling capacitors and n-channel MOS diodes connected together for generating a high positive voltage output, said MOS diodes being located on said epitaxial region;

a second voltage multiplier having a plurality of coupling capacitors and n-channel MOS diodes connected together for generating a low negative voltage output, said second multiplier MOS diodes being located in said epitaxial region; and

a third voltage multiplier having a plurality of coupling capacitors and n-channel MOS diodes connected together for generating a negative voltage output which is more negative than said second multiplier voltage output, said third multiplier MOS diodes being located in said epitaxial region and said third multiplier output applied to said epitaxial region.

10. The circuit as in claim 9 wherein said coupling capacitors are parallel polysilicon plate capacitors located on said substrate.

\* \* \* \* \*

# United States Patent [19]

Bingham et al.

[11] Patent Number: 4,679,134

[45] Date of Patent: Jul. 7, 1987

[54] **INTEGRATED DUAL CHARGE PUMP  
POWER SUPPLY AND RS-232  
TRANSMITTER/RECEIVER**

[75] Inventors: David Bingham, San Jose; Charles M. Allen, Sunnyvale, both of Calif.

[73] Assignee: Maxim Integrated Products, Inc., Sunnyvale, Calif.

[21] Appl. No.: 878,233

[22] Filed: Jun. 25, 1986

## Related U.S. Application Data

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[51] Int. Cl.<sup>4</sup> ..... H02M 3/18

[52] U.S. Cl. .... 363/61; 307/110;  
357/51

[58] Field of Search ..... 363/59, 60, 61;  
307/109, 110, 284, 305, 567; 357/51; 320/1

## [56] References Cited

### U.S. PATENT DOCUMENTS

4,047,091	9/1977	Hutchins et al.	357/51
4,050,004	9/1977	Greatbatch	363/59
4,186,436	1/1980	Ishiwatari	363/60
4,404,624	9/1983	Yamazaki	363/59
4,616,303	10/1986	Mauthe	307/110
4,621,315	11/1986	Vaughn et al.	363/60

Primary Examiner—Peter S. Wong

Assistant Examiner—Judson H. Jones

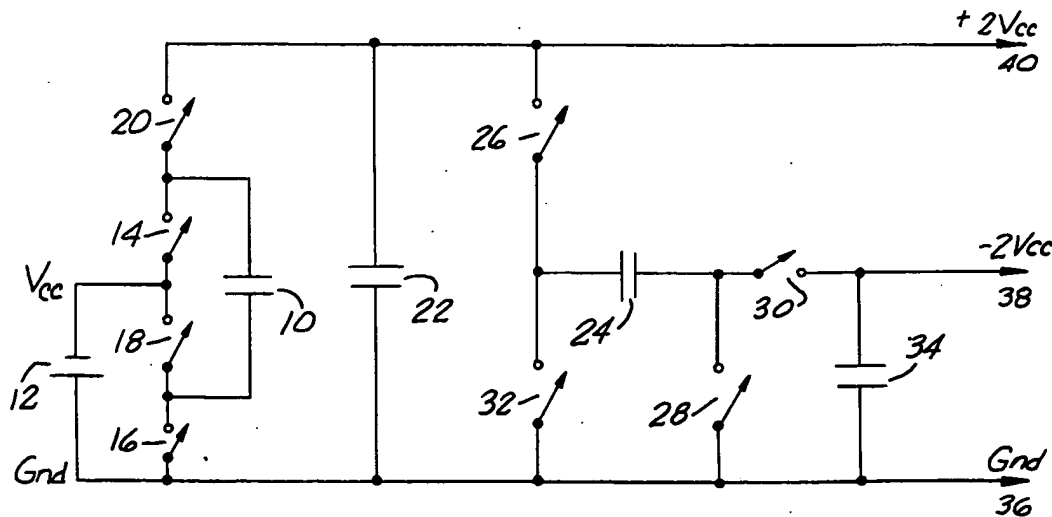
Attorney, Agent, or Firm—Lyon & Lyon

## [57] ABSTRACT

A monolithic integrated circuit containing an inver-

ting/non-inverting voltage doubler charge pump circuit is disclosed for converting a unipolar supply voltage to a bipolar supply voltage of a greater magnitude. The unipolar input voltage is placed across a first external transfer capacitor by a first set of MOS switches during a first time period. The unipolar input voltage source is placed in series with the first transfer capacitor and this series combination of voltages is placed across a first external reservoir capacitor by a second set of MOS switches during a second time period. The voltage appearing across the first external reservoir capacitor is placed on a second transfer capacitor during the first time period by a third set of MOS switches. The voltage across the second transfer capacitor is placed into a second external reservoir capacitor with its polarity inverted by a fourth set of MOS switches during the second time period. A dual-collector lateral junction transistor, formed during the conventional CMOS processing steps used to fabricate the MOS switches, is connected as a voltage clamp between a ground potential and the two bipolar DC output lines of the power supply circuit to assure correct start-up conditions for the circuit. Gain reduction devices are placed in the semiconductor substrate to collect minority carriers which would otherwise be injected into inherent parasitic four layer PNPJN junction devices created as a result of the architecture of the circuit, to prevent latch-up of the four layer devices. In a preferred embodiment, an RS-232 receiver and transmitter are contained on the same monolithic integrated circuit as the dual charge pump power supply.

2 Claims, 10 Drawing Figures



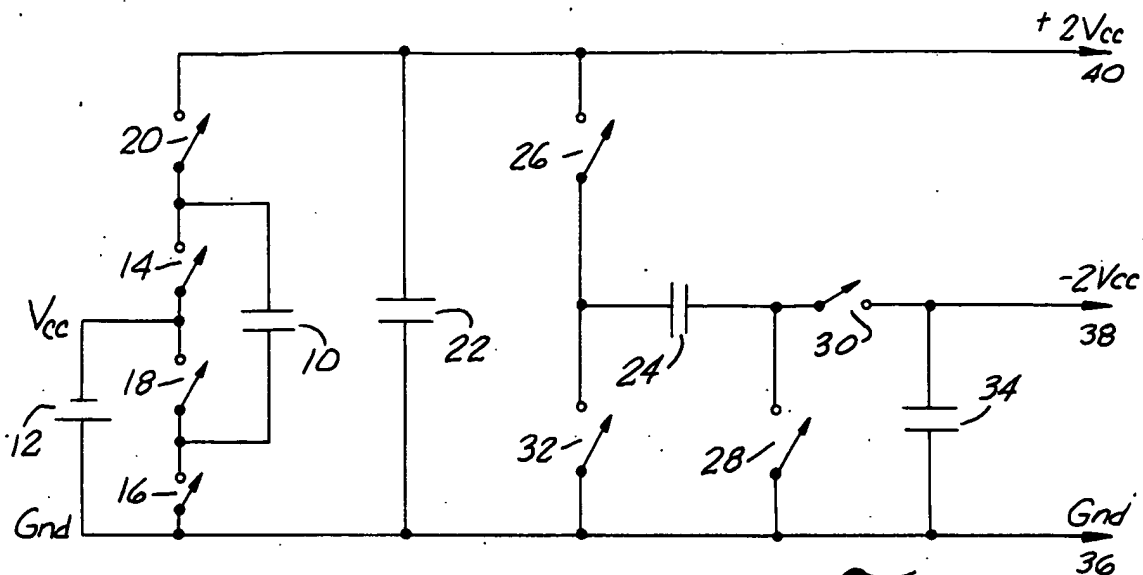


FIG. 1a.

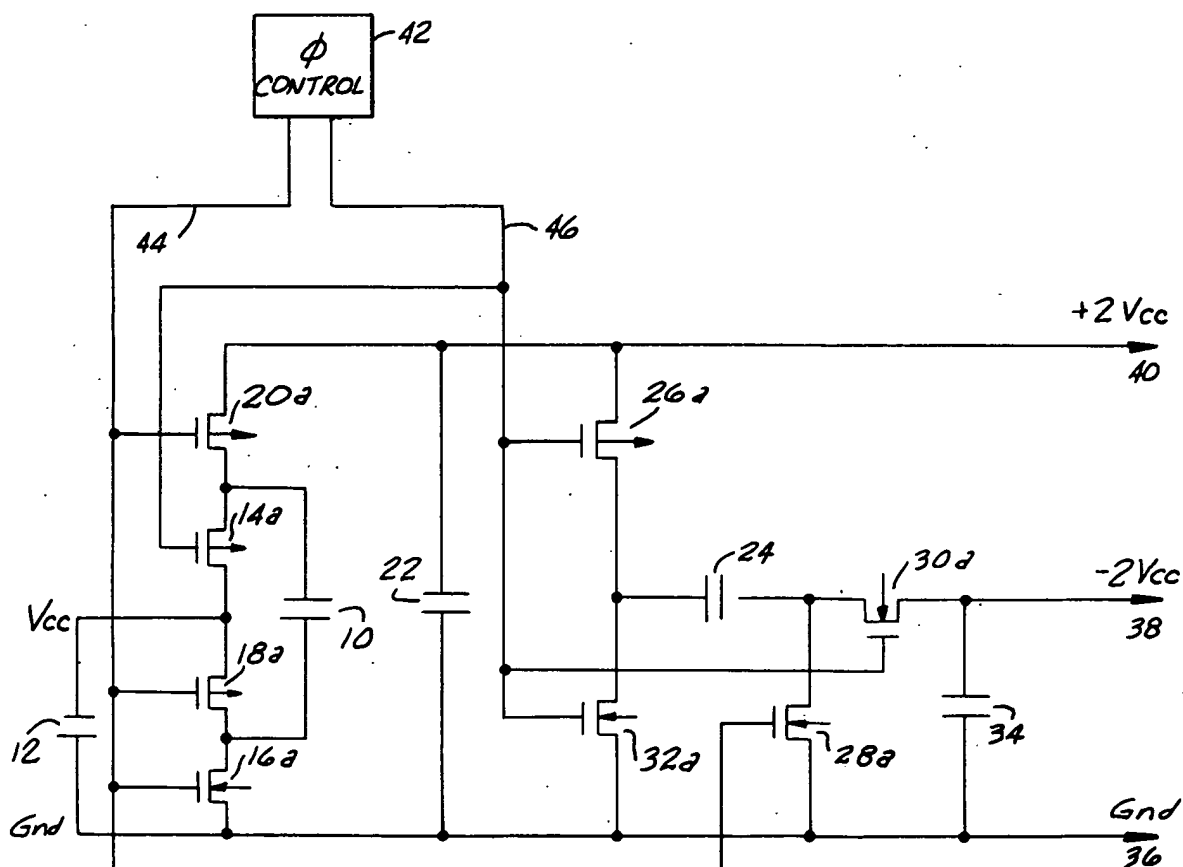
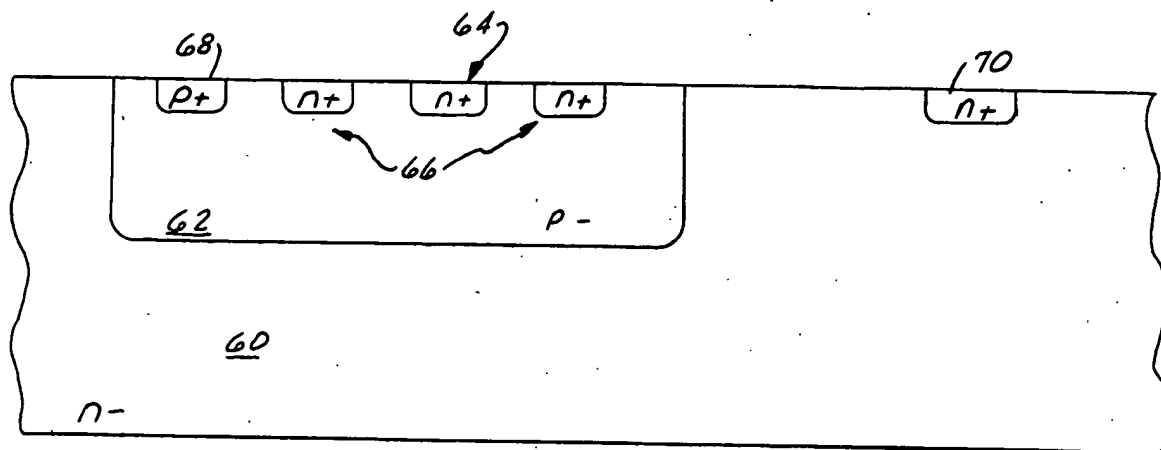


FIG. 1b.





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FIG. 4.

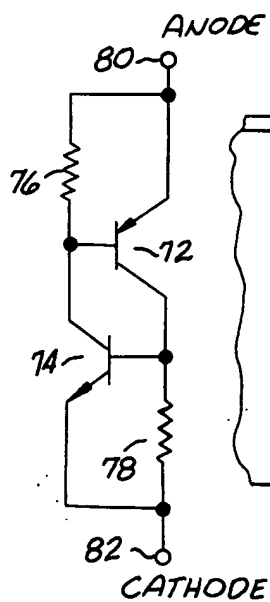


FIG. 5a.

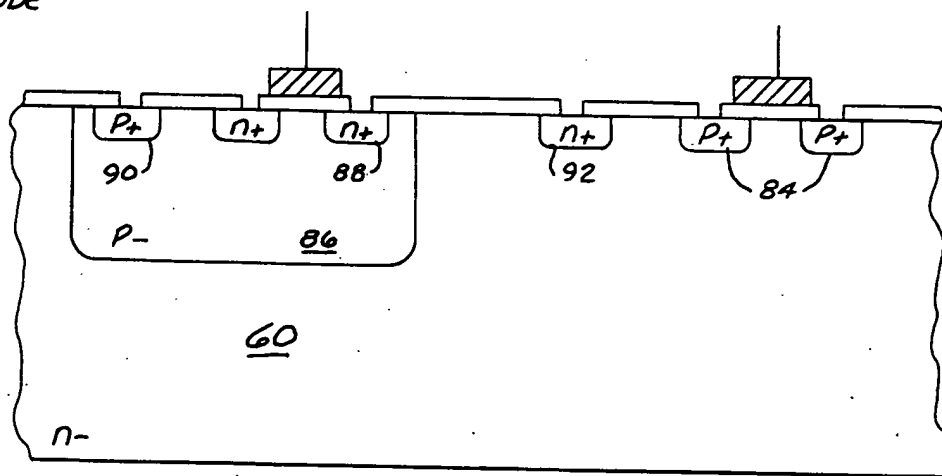


FIG. 5b.





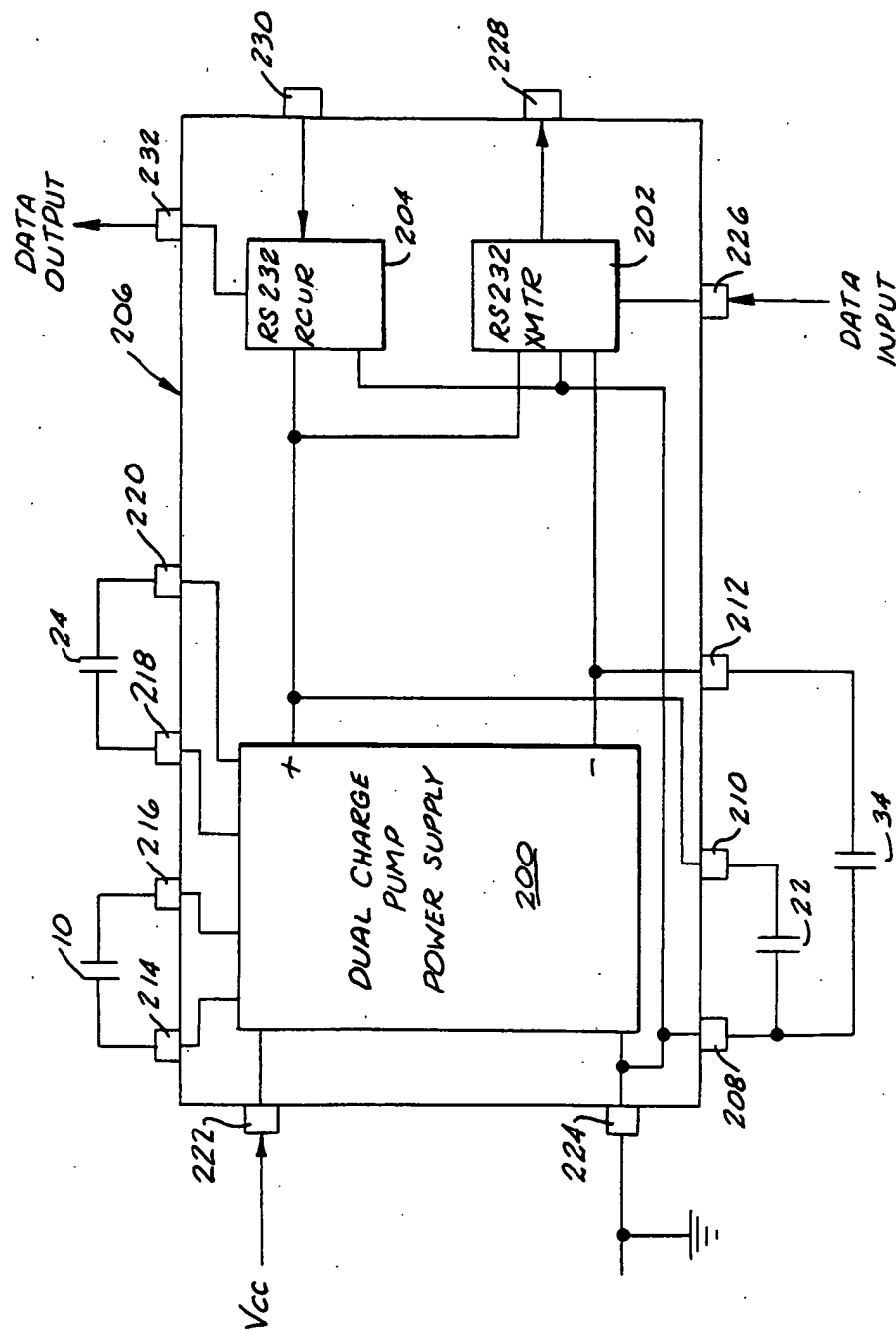


FIG. 7.

## INTEGRATED DUAL CHARGE PUMP POWER SUPPLY AND RS-232 TRANSMITTER/RECEIVER

This application is a continuation of application Ser. No. 782,953 filed Oct. 1, 1985.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention pertains to charge pump power supplies for generating bipolar output voltages greater in magnitude than a single unipolar input voltage. More particularly, the present invention pertains to the integration of such a circuit on a single piece of semiconductor substrate material. Further, the invention pertains to other circuitry integrable on a single piece of semiconductor substrate material along with such a power supply circuit.

#### 2. Prior Art

Discrete component voltage doubler and voltage inverter circuits are well known in the art. Such circuits are used in many electronic systems which require a multiplicity of DC voltages for operation. More recently, in the context of digital circuits and systems, it has become common to employ a single five volt unipolar voltage supply to power digital circuitry in modern data processing systems. For example, semiconductor microprocessors, memories, and logic all commonly operate from a single five volt power supply. There are, however, certain interface circuits and other special purpose circuits which require voltages other than five volts. More particularly, some circuits require voltages in the ranges of from five to fifteen volts. Additionally, requirements often exist for bipolar power supply voltages so that voltage power requirements of plus or minus 15 volts and plus or minus 12 volts are commonly encountered, for example in RS-232 communication loops.

For these communication circuits and other applications, bipolar DC power requirements are low when compared to the digital circuitry power requirements. In fact, it is common to encounter five volt unipolar power supplies for driving digital logic rated in tens or hundreds of watts whereas interface and other power requirements may be as low as tens or hundreds of milliwatts.

It is therefore often desirable to generate locally the various non-primary voltage sources, i.e., the bipolar voltage sources, if the power requirements are not high and if it can be done economically and with relatively high electrical power conversion efficiencies.

For an example, a minicomputer may have a 100 watt 5 volt power supply which supplies all of the requirements for a multiplicity of printed circuit boards holding logic integrated circuits. On one of those integrated circuit boards, there will often be an RS-232 digital interface circuit requiring a plus or minus 10 or plus or minus 15 volt power supply. This interface circuit may consume 50 milliwatts of power. Instead of generating the plus and minus 15 volt power supply from the main power supply and then bussing these voltages to the boards which require them, it is often more economical to generate these two voltages from the bussed five volt power supply locally on whatever board needs other voltages. However, generating such voltages by the use of discrete components is often disadvantageous because the additional components required to generate such voltages take up a relatively large amount of cir-

cuit board real estate, and often are power inefficient, i.e., heat producing.

The industry has recently turned its attention to attempts to furnish auxiliary power supplies of the nature herein described on a single semiconductor substrate. Such circuits have the obvious advantages of space saving, assembly labor savings, and relatively lower power dissipation. A form of such circuits known as charge pumps have been used in semiconductor memory chips to produce a crude back bias supply and for supplying the higher voltages needed to program such memory devices. Charge pump circuits have been used in the inverting mode to produce voltage polarities opposite to that of the supply voltage from which they are generated. An example of such a circuit is found in the product designated ICL 7660, a power supply circuit manufactured by the assignee of the present invention.

The efforts to design and implement a bipolar charge pump integrated circuit have met with several obstacles which result from the inherent nature of the integration process and the fabrication process which are used to manufacture these devices. It is well known to those in the art that when MOS or CMOS circuits are integrated onto a single semiconductor substrate, the chip layout geometry and architecture inherently produce parasitic junction devices. These devices include junction diodes, bipolar transistors, and PNP four layer diode devices, similar to silicon controlled rectifier (SCR) devices.

The existence of these parasitic devices has created difficulties in the design and fabrication of dual polarity charge pump power supply circuits. When forward biased, the aforementioned four layer diode device will cause a CMOS circuit to experience a phenomenon known as latch-up. Latch-up is a phenomenon common to CMOS circuits whereby the circuit can be triggered into a low impedance conducting state by forward biasing an inherent four layer diode device in the circuit. This four layer diode may be triggered by various means into a low voltage, low impedance state. When this occurs, operation of the circuit is inhibited and possible damage may occur to the circuit if there is no inherent current limiting designed into the circuit.

Another problem inherent in the design of dual polarity charge pump inverter circuits is the difficulty of assuring correct start-up of the circuit. The conditions existing in the semiconductor material at the time of start-up may randomly produce states which prevent such a circuit from ever starting up to produce the desired output voltages. In the past, elaborate systems and considerable extra circuitry has been designed into such circuits in an attempt to avoid this problem.

### BRIEF DESCRIPTION OF THE INVENTION

The present invention consists of a CMOS inverting and non-inverting charge pump power supply integrated into a single piece of semiconductor substrate material. An inherent lateral bipolar transistor formed during the CMOS fabrication process is utilized to always assure the correct operating conditions which will allow start-up of the circuit. In addition, the inherent four layer diode devices which are created during the fabrication of the circuit are identified during the geometry layout process which defines the locations on the semiconductor substrate where the various devices will be placed, and extra minority charge collector regions are placed in the semiconductor substrate to collect injected minority charge carriers and prevent the possi-

bility of triggering the inherent four layer PNPJ junction into a low impedance conducting or latch-up mode.

Another aspect of the present invention is the integration, on a single piece of semiconductor substrate material, of an inverting charge pump power supply, a non-inverting charge pump power supply, and a combination of RS-232C receivers and transmitters. Combination of RS-232C transmitters and receivers may consist of at least one transmitter together with either zero or any number of receivers.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a simplified schematic diagram of the charge pump circuit of a preferred embodiment of the present invention.

FIG. 1(b) is a schematic diagram of the charge pump circuit of FIG. 1(a) wherein the switches are replaced by MOS transistors.

FIG. 2 is a gate drive circuit suitable for operating driving the gates of the charge pump circuit of FIG. 1(b).

FIG. 3 is a schematic diagram of a preferred embodiment of the present invention further showing the substrate connections of the MOS devices and a PNP lateral junction device for assuring the correct start-up conditions of the charge pump circuit.

FIG. 4 is a semiconductor substrate profile drawing of NPN lateral transistor suitable for use in the present invention.

FIGS. 5(a) and 5(b) are respectively a schematic representation of a four layer device and a semiconductor substrate profile drawing of such a device showing the MOS geometry which inherently creates such a device.

FIG. 6(a) is a schematic diagram of a four layer device having extra P region collectors, suitable for use in the present invention.

FIG. 6(b) is a substrate profile drawing of a four layer device suitable for use in the present invention having extra minority charge carrier collectors for preventing latch-up showing the relative placement of such charge collectors.

FIG. 7 is a block diagram of an embodiment of the present invention including a dual integrated charge pump power supply and a RS-232C receiver and transmitter.

#### DESCRIPTION OF A PREFERRED EMBODIMENT

Referring first to FIG. 1(a), simplified conceptual schematic drawing of the basic charge pump circuit of the present invention, the circuit of the present invention operates by placing an input voltage upon one of two transfer capacitors via a series of switches. The charge in that capacitor is then transferred to one of two reservoir capacitors. The polarity of the voltage is established via the switch interconnecting scheme.

More specifically, the operation of the circuit of FIG. 1(a) is time-divided into two segments, or phases. In a first phase, voltage from a voltage source is placed on transfer capacitors. During a second phase the voltage on the transfer capacitors is transferred to the reservoir capacitors.

Referring first to the positive voltage doubler portion of the circuit, transfer capacitor 10 is charged from voltage source 12 (having a value Vcc) by closing switches 14 and 16 while switches 18 and 20 remain open during a first phase. During a second phase

switches 14 and 16 are open and switches 18 and 20 are closed.

As can be seen from FIG. 1(a), when switches 18 and 20 are closed during the second phase the voltage source 12 is effectively placed in series with the voltage stored across reservoir capacitor 10 and thus the sum of the voltage across voltage source 12 and capacitor 10 is placed across reservoir capacitor 22.

The inverting portion of the voltage doubler circuit operates as follows: transfer capacitor 24 is charged to the voltage across reservoir capacitor 22 via the switches 26 and 28 which are closed during the first phase of operation of the circuit while switches 30 and 32 remain open. During the second phase of circuit operation switches 26 and 28 are opened and the voltage across transfer capacitor 24 is placed on reservoir capacitor 34 via the closing of switches 30 and 32. Those of ordinary skill in the art will note that the circuit configuration is such that when the voltage across transfer capacitor 24 is placed across reservoir capacitor 34 the positive end of transfer capacitor 24 is connected to ground line 36 through switch 32 and the negative end of capacitor 24 is connected to the side of reservoir capacitor 34 connected to -2 Vcc output line 38. The polarity of the voltage across reservoir capacitor 34 with respect to ground line 36 is thus such that the voltage across reservoir capacitor 34 is negative. The output of reservoir capacitor 22 is connected to +2 Vcc output line 40.

The first and second phases of circuit operation described above are repeated at a frequency which may range from approximately 100 hertz to 100's of kilohertz or higher. It has been found that a frequency of approximately 15 KHz performs satisfactorily for the purposes of the present invention.

The foregoing represents an idealized characterization of the operation of the circuit of FIG. 1(a). Those of ordinary skill in the art will readily realize that it will take several first and second phase cycles before the resultant voltage between ground terminal 36 and +2 Vcc output terminal 40 actually reaches a voltage value of +2 Vcc. Likewise, it will be appreciated that several cycles are also needed for the voltage between ground terminal 36 and -2 Vcc output terminal 38 arrives at a voltage of -2 Vcc.

Those of ordinary skill in the art will also realize that the amount of current which may be drawn from the output of the circuit of FIG. 1(a) depends on the relative sizes of transfer capacitors 10 and 24 and reservoir capacitors 22 and 34, as well as the on impedance of switches 14, 16, 18, 20, 26, 28, 32 and 30.

It will also be apparent that the voltage appearing between output terminals 36 and 38 or 36 and 40 will be approximately twice the input voltage supplied by voltage source 12. Those of ordinary skill in the art will appreciate that other multiples of the input voltage Vcc at voltage source 12, are readily achievable using the concept of the present invention.

Turning now to FIG. 1(b), it is seen that in an actual embodiment of the present invention switches 14, 16, 18, 20, 26, 28, 30 and 32 have been replaced with MOS transistors. Thus, switch 14 is replaced by P-channel MOS transistor 14(a), switch 16 is replaced by N-channel MOS transistor 16(a), switch 18 is replaced by P-channel MOS transistor 18(a), switch 20 is replaced by P-channel MOS transistor 20(a), switch 26 is replaced by P-channel MOS transistor 26(a), switch 28 is replaced by N-channel MOS transistor 28(a), switch 30 is

replaced by N-channel MOS transistor 30(a), switch 32 is replaced by N-channel MOS transistor 32(a).

The time controlled operation of the circuit of FIG. 1(b) is implemented by phase control unit 42. Phase control unit 42 drives all of the gates of the MOS devices, 14(a), 16(a), 18(a), 20(a), 26(a), 28(a), 30(a), and 32(a) via gate control lines 44 and 46. Gate control lines 44 and 46 are connected to the gates of the P-channel MOS transistors and N-channel MOS transistors, used as MOS switches, such that the switches are turned on and off appropriately as described herein during the first and second phases of the circuit operation.

Those of ordinary skill in the art will readily appreciate that, in order to insure efficient power transfer, that switching of MOS switching devices should be accomplished on a break before make basis or, at worst case, on a simultaneous switching basis. Those of ordinary skill in the art will also realize that the order of phases could be reversed. Alternatively, a first clock could be used to control the sets of MOS switches controlling transfer capacitor 10 and reservoir capacitor 22, and a second clock could be used to control the sets of MOS switches controlling transfer capacitor 24 and reservoir capacitor 34.

It should be understood for purposes of this disclosure, that all of the capacitors shown in FIGS. 1(a) and 1(b) would be located outboard of the integrated circuit in an actual embodiment. That is, these capacitors are external components which connect to the integrated MOS switches on the semiconductor substrate via terminals provided on the semiconductor substrate for that purpose. For an operating frequency of 15 KHz, 20 microfarads is a sufficient size for all capacitors. Those of ordinary skill in the art will readily appreciate that as the switching frequency is increased the values of the capacitors will drop, but that switching losses will increase due to the charging to discharging at the clock rate of its parasitic nodal capacitances in the MOS devices. Conversely, as the switching frequency decreases, the size of the capacitors would increase, with the concomitant disadvantage that the increasing capacitor size is accompanied by increasing physical size of the capacitors.

For a current capacity of 10 milliampere at +10 volts and -10 volts, the MOS switching devices should have a channel width to channel length ratio of 5000 to 10,000, with channel lengths of approximately five microns. Those of ordinary skill in the art will recognize that the range of current output of the circuit described herein could be as large as approximately one ampere, however, the MOS devices would have to be scaled accordingly as is well known in the art.

Referring now to FIG. 2, an embodiment of the phase control unit 42 of the present invention, the operation of phase control unit 42 is disclosed. Those of ordinary skill in the art will recognize that phase control unit 42 may consist of three conventional CMOS inverter circuits each comprised of a P-channel and N-channel MOS transistor pair. The embodiment of FIG. 2 contains a first CMOS inverter comprised of P-channel MOS transistor 44 and N-channel MOS transistor 46, the inverter comprised of P-channel MOS transistor 48 and N-channel MOS transistor 50, and the inverter comprised of P-channel MOS transistor 52 and N-channel MOS transistor 54.

These three inverter pairs are driven by oscillator 56, which may be any conventional oscillator configured

from CMOS elements as is well known to those skilled in the art.

The circuit of FIG. 2 is powered by +2 Vcc and -2 Vcc lines 36 and 40. This assures that the voltage swing on gate lines 44 and 46 will span approximately the entire power supply range, thus ensuring that all of the gates of the P-channel and N-channel devices which they drive will be as fully turned on as possible and can be turned off since all transistors and enhancement types. This will guarantee as low an on-state impedance of the MOS switches as possible thus maximizing the efficiency and current drive capabilities of the present invention.

In the illustration of a preferred embodiment of the present invention depicted in FIG. 1(a), the substrate connections of the MOS devices are shown uncommitted. Those of ordinary skill in the art will realize that junction isolated MOS transistors such as used in FIG. 1(b) are four-terminal devices and that both the gate terminal and the substrate terminal are control terminals. The turn-on voltage of the gate terminal is affected by the reverse bias on the substrate to source junction. As that reverse bias is increased, the turn on voltage of the device also increases. The affect is significantly greater for an N-channel transistor than a P-channel transistor.

As the substrate-to-source voltage increases the gate turn voltage of the device also increases, thus potentially increasing the on resistance of the device to a point where circuit operation could be seriously effected. Since, in a circuit of this nature, the drain-source resistance in the on state should be as low as possible, it is desirable to connect each N-channel MOS transistor substrate to its source.

With respect to P-channel transistors the effect of this reverse substrate source biasing is about half of that for N-channel MOS transistors due to lighter channel impurity doping densities. The most practical solution in the case of the P-channel MOS transistors is to connect all P-channel substrates to the most positive voltage in the circuit. That voltage is, as seen from FIG. 1(a) +2 Vcc which appears on positive supply line 40. These connections are shown in respect to FIG. 3.

Prior to start-up, it is reasonable to assume that zero voltage exists on all capacitors. At start-up, reservoir capacitor 22 may be connected to ground line 36 or to -2 Vcc line 38. Reservoir capacitor 22 will be immediately charged with the source substrate diodes of P-channel MOS transistors 14(a) and 18(a) to a voltage of approximately Vcc -0.6 of a volt. The voltage on reservoir capacitor 34 could lie somewhere between ground line 36 and the voltage on reservoir capacitor 22; depending which of transistors 26(a), 28(a), 30(a) or 32(a) were conducting (if any). This results in a voltage on the -2 Vcc line that could be such that N-channel transistor 16(a) and other transistors being turned on. Under these conditions, a voltage between +2 Vcc and -2 Vcc drives the gates of all of the output transistors and is indeterminate. Thus both start-up and operation is not assured.

If the other possible start-up conditions of the capacitor and MOS device connections and off/on states are assumed, those of ordinary skill in the art will readily appreciate that the start-up and operation of the circuit of FIGS. 1 and 2 is not assured.

The solution to this dilemma is to place a clamp on the -2 Vcc line 38 to clamp that voltage line to assure that it will never assume a voltage substantially more

positive than that appearing on ground line 36. The +2 Vcc line 40 is also clamped so that it will never assume a voltage substantially more negative than the voltage Vcc on approximately Vcc - 0.6 volts.

While those of ordinary skill in the art will realize that, conceptually, a diode would be an ideal clamping means for the -2 Vcc line 38, it is not possible to fabricate a simple PN junction diode in a MOS process. A junction transistor will always be created by an attempt to fabricate a diode. The presence of such a transistor in the circuit of FIG. 1(b) would cause excess wasted current to flow in the circuit, because of its beta or current gain.

In a preferred embodiment of the present invention, this clamp is comprised of a lateral NPN transistor. This lateral NPN transistor is shown in FIG. 3. The lateral collector and base of this device are both connected to -2 Vcc line 38, its vertical collector connected to +2 Vcc. The lateral collector serves to minimize the effective current gain of the unwanted but inherent vertical collector of NPN transistor 58, which would otherwise cause excess current flow from the +2 Vcc line through ground. Unless the -2 Vcc line 38 exceeds ground by approximately 0.6 of a volt in the positive direction, this device will not conduct current. If the -2 Vcc line equals approximately 0.6 volts, the device turns on and current will flow in approximately equal portions through both collectors to maintain the -2 Vcc line at no greater than zero plus approximately 0.6 volts.

With respect to the clamp for +2 Vcc line 40, the action of the inherent junction diodes 59(a) and 59(b) present between the drain and substrate of devices 14(a) and 18(a) serve to clamp the +2 Vcc line to a voltage no more negative than the input positive supply voltage Vcc minus approximately 0.6 volts.

Consequently the voltages on +2 Vcc line and -2 Vcc line are both well defined. Additionally the voltage difference between +2 Vcc line 38 and -2 Vcc line 40 at start-up is (Vcc - 1.2) volts and is also well defined. This value of voltage is sufficiently large to guarantee operation of the drive circuitry for the gates of the output transistors until the charge pumps charge the lines +2 Vcc (40) and -2 Vcc (38) to those voltages.

The lateral NPN transistor used to clamp -2 Vcc line 38 is fabricated using conventional CMOS fabrication techniques. For a current drain of plus and minus 10 mA at 10 volts, the periphery of the emitter for the lateral NPN transistor can typically be 100 microns. Those of ordinary skill in the art will appreciate that the size of this device may be scaled to accommodate larger current carrying requirements, and its periphery need not be larger than 1000 microns.

Referring now to FIG. 4, a substrate profile drawing of a dual collector lateral NPN transistor 58, that transistor 58 is fabricated on a portion of the lightly doped N type substrate material 60 in a P-well 62. P-well 62 is placed into substrate 60 using common CMOS processing techniques. N region 64 serves as the emitter of the lateral NPN transistor, and is surrounded by N region 66 which serves as the lateral collector. P region 68 in P-well 62 serves as the base contact, it being understood by those skilled in the art that P-well 62 itself serves as the base of lateral NPN transistor 58. N-region 70 located in a region of substrate 60 outside of P-well 62 serves as the unwanted, but inherent vertical collector of NPN lateral transistor 58.

When the base emitter junction of lateral NPN transistor 58 is forward biased, minority carriers injected by the emitter into the base are collected by both the vertical and lateral collectors in roughly equal amounts. Connecting the lateral collectors to the common base reduces the vertical collector current to approximately 1/2 of the clamp current. If a vertical NPN transistor had been used alone, the clamp current (base current) would be multiplied by the beta (approximately 500 of the device) thereby wasting large amounts of current.

Referring now to FIGS. 1(b) and 3, during start-up reservoir capacitor 22 is charged by the forward biased condition of the source-substrate diodes 59(a) and 59(b) of P-channel device 14(a) and the drain substrate diode of P-channel device 18(a). The initial current surge through these diodes can be hundreds of milliamperes and thus be well above the holding current of the inherent SCR type four layer diode device which exists in the circuit.

Such a four layer device is schematically represented in FIG. 5(a). Referring to FIG. 5(a), it is seen that the four layer device is made up of PNP transistor 72, NPN transistor 74, resistor 76, and resistor 78. Resistor 76 is connected across the base-emitter junction of PNP transistor 72 while resistor 78 is connected across the base-emitter junction of PNP transistor 74. The base of NPN transistor 74 is connected to the collector of PNP transistor 72 and the base of PNP transistor 72 is connected to the collector of NPN transistor 74. The connection of the emitter junction of PNP transistor 72 and resistor 76 form the anode connection 78 of the four layer device and the intersection of resistor 78 and the emitter of NPN transistor 74 form the cathode connection 80 of the four layer device.

As will be appreciated by those of ordinary skill in the art, the four layer device shown in FIG. 5(a) will enter a low impedance state between its anode 80 and cathode 82 after suitable triggering if the product of the betas of the two equivalent transistors is greater than one and the anode current into the four layer device is greater than the turn on voltage of either transistor divided by its equivalent base emitter shunting resistor, whichever is greatest.

Referring now to FIGS. 3, 5(a) and 5(b), it will be apparent to those of ordinary skill in the art that such a four layer device occurs in the circuit of FIG. 3. The sources of either of P-channel devices 14(a) and 18(a) (shown diagrammatically as P region 84 in FIG. 5(b)) represent the emitter of PNP transistor 72 of FIG. 5. The semiconductor substrate 60 forms the base of PNP transistor 72 as well as the collector of NPN transistor 74. P-well 86 forms the collector of PNP transistor 72 as well as the base of NPN transistor 74. The source of either of N-channel transistors 16(a) and 32(a), one of which is shown as N region 88 of FIG. 5(b), forms the emitter of NPN transistor 74. Resistor 76 is formed by the bulk resistance of the P-well 86. Likewise, the resistor 78 is formed by the bulk resistance of the substrate material. Those skilled in the art will note that regions such as P region 90 in P-well 86 and N region 92 in substrate 60 serve as low resistance surface planes commonly used in CMOS technology to buss supply voltages to the surfaces of substrate and P-wells.

In order to trigger the four layer device into its low impedance state, currents must be injected into the base of either of transistors 72 or 74, either the P-well 86 or the substrate 60. These currents must be greater than the holding current required for the four layer device.

This condition can occur by various means. For example, a very rapid rate of increase in the anode-cathode voltage will force current into the bases of transistors 72 and 74 due to the charging of the collector-base junction capacitors inherent in those devices. Alternatively, forward biasing of a region in the substrate junction adjacent to the P-well 86 and P-region 84 forming the emitter of transistor 72 could induce base currents to flow in transistor 72 and 74 sufficient to exceed holding current values. Either of these conditions could occur at start-up of the circuit of FIG. 3.

In order for the inverting doubler charge pump circuit of the present invention to reliably operate, it is necessary to assure that this possible latch-up condition can never occur. One method which is used in some CMOS circuits to inhibit the possibility of latch-up would be to insert high value resistors in series with either or both of the emitters of NPN transistor 74 or PNP transistor 72. This method, however, in the present invention would result in an unacceptably high value of on impedance for the MOS switches.

Another method of assuring that the latch-up condition never occurs is disclosed as an aspect of the present invention. The product of the betas of PNP transistor 72 and NPN transistor 74 is made less than unity. Thus, the current flowing between the anode terminal 80 and cathode terminal 82 of the four layer device will never reach a value great enough to equal the holding current necessary to sustain that device in its low impedance state.

Referring now to FIG. 6(a), another four layer device 100 composed of equivalent NPN and PNP transistors is shown. However, unlike the circuit of FIG. 5(a) the four layer device depicted in FIG. 6(a), having anode terminal 102 and cathode terminal 104, a single collector NPN transistor 106 and a multiple collector PNP transistor 108 as well as resistors 110 and 112. The multiple PNP collectors (shown at 114) are tied back to the base of the PNP transistor 108. Only a single multiple collector is connected to the base of NPN transistor 106. These collectors 114 are fabricated on substrate 60 in a region located between the emitter of NPN transistor 106 and the base of PNP transistor 108.

The function of the serial collectors 114 is to guard the forward biased PN junction formed between P regions 128 or 138 and substrate 60 by collecting the minority carriers which are injected into the substrate 60. These carriers are thus prevented from reaching the base of the PNP transistor 108 and assure that the beta product of these two transistors is less than unity. Most of the minority carriers injected into the substrate are collected by these serial collectors before they can diffuse and be collected by the P-well which is also the base of the NPN transistor. This may be designed to reduce the PNP beta to a value of less than the reciprocal of the NPN beta thereby preventing latch-up.

Referring now to FIG. 6(b), a semiconductor profile drawing of four layer device 100 of FIG. 6(a), NPN transistor 106 is formed in P-well 120. Contact 122, contacting N region 124 in P-well 120, constitutes cathode 104 of four layer device 100. This N region may be the source of either N-channel MOS transistor 16(a) or N-channel MOS transistor 32(a) from FIGS. 1 and 3. N region 124 forms the emitter of NPN transistor 106 and P-well 120 forms the base of NPN transistor 106. Substrate 60 forms the collector of NPN transistor 106, as well as the base of PNP transistor 112.

Contact 126, contacting P region 128 is at  $V_{cc}$  potential. P region 128 may be either the source of P channel MOS transistor 14(a) or the drain of P-channel MOS transistor 18(a) from FIGS. 1 and 3. P region 128 forms the emitter of PNP transistor 108.

P regions 130(a) through 130(e), in substrate 60, form the multiple collectors of PNP transistor 108 (shown at 114 in FIG. 6(a)). Multiple collectors 130(a) through 130(e) are connected together at the surface of the semiconductor substrate 60 by layer 132 which may be made of aluminum and fabricated during the metalization step of a conventional CMOS fabrication process. N regions 134(a) through 134(d), disposed in between P regions 130(a) through 130(e) are used for the purpose of making a low impedance contact between the  $+2 V_{cc}$  line and the substrate. P-well 120, the base of NPN transistor 106, also serves as the single collector of PNP transistor 108, as shown in FIG. 6(a). The regions 135, shown adjacent to layer 132, are the gate oxide layer of the MOS structures.

As is shown in FIG. 6(b) the multiple collectors of PNP transistor 114 are interposed in between the N-channel MOS transistor 16(a) in the P-well formed of N regions 124 and 136. This device, for illustration, shown as 16(a) on FIG. 6(b), has drain region 138 and gate 140. This device, for illustration, shown as 18(a) on FIG. 6(b), has drain region 138 and gate region 142. P-channel MOS transistor 14(a) formed of P region 128 and P region 138. In this manner these multiple collectors 130(a) through 130(e) are in a position to collect most of the minority carriers which are injected into the semiconductor substrate as a result of forward biasing at start-up of the parasitic PN junctions formed during the CMOS fabrication process.

Depending on the CMOS process used, the number of multiple collectors 114 may range from 1 to approximately 10. Furthermore, the spacing between the injecting PN junction and the nearest P-well should be typically anywhere from 25 to 500 microns. Spacing may be reduced if the lifetime of the substrate minority carriers is particularly low and or the substrate resistivity is very low (less than one ohm-centimeter). In the presently preferred embodiment the spacing between the injecting PN junctions and the nearest P-well is approximately 150 microns and four multiple collectors 114 are used. This is based upon a process using a substrate having a substrate resistivity of approximately 2.5 ohm-cm.

Although the presently preferred embodiment has been disclosed as a P-well CMOS embodiment, those of ordinary skill in the art will recognize that N-well CMOS technology could also be used without departing from the spirit and scope of the present invention. Those of ordinary skill in the art will readily understand from the disclosure herein how to fabricate such an N-well embodiment.

Referring now to FIG. 7, a block diagram of a preferred embodiment of the present invention including dual charge pump power supply 200, previously described, RS-232C transmitter circuit 202, and RS-232 receiver circuit 204. These elements are shown diagrammatically as fabricated on a single piece of semiconductor substrate material 206. Positive reservoir capacitor 22 is shown connected to the semiconductor substrate via terminal pads 208 and 210. Negative reservoir capacitor 34 is shown connected to the substrate via terminal pads 208 and 212. Positive transfer capacitor 10 and negative transfer capacitor 24 are shown connected to

the substrate via terminal pads 214, 216, 218 and 220 respectively. An input voltage is provided to the circuit at Vcc input terminal pad 222 and ground input terminal pad 224. Those of ordinary skill in the art will readily realize that ground input terminal 224 and terminal pad 208 may in some embodiments be the same connection terminal pad. The data input to RS-232 transmitter 202 is provided at terminal pad 226 and the output of RS-232 transmitter 202 is provided at terminal pad 228. The data input to RS-232 receiver 204 is provided at terminal pad 230 and the data output of RS-232 receiver 204 so provided at terminal pad 232.

A monolithic integrated circuit containing the dual charge pump power supply 200 and RS-232 transmitter 202 and receiver 204 may be fabricated as a monolithic integrated circuit. The only outboard components required for operation of the circuit are positive and negative reservoir capacitors 22 and 34 and the positive and negative transfer capacitors 10 and 24.

While the preferred embodiment of FIG. 7 shows a single RS-232 transmitter 202 and a single RS-232 transmitter 204, those of ordinary skill in the art will readily recognize that other combinations of receivers and transmitters could be added without departing from the spirit of the invention. It is noted, however, that an embodiment of the circuit of FIG. 7 which contains only one or more RS-232 receivers 204, and no RS-232 transmitters 202, does not require a negative power supply connection. This is because the negative swing of the RS-232 format signal is usually disregarded by the receiver circuitry.

The RS-232 transmitter circuit 202, as well as the RS-232 receiver circuit 204 may be conventionally configured out of CMOS elements as is well known in the art. For example, RS-232 transmitter circuit 202 may be a CMOS inverter with a level shifter to translate TTL logic levels to the RS-232 format, as is known in the art. Alternatively, it may be configured similarly to the MC 1488 circuit, manufactured by Motorola. RS-232 receiver circuits 204 may be a CMOS inverter with a level shifter to translate the incoming RS-232 format signal to TTL logic levels as is known in the art. Alternatively, it may be configured similarly to the MC 1489 circuit, manufactured by Motorola.

A preferred embodiment of the present invention has been disclosed. Those of ordinary skill in the art will readily recognize that other embodiments are possible which do not differ in material respects. It is the intention of the inventors to include such embodiment within the scope of the appended claims.

We claim:

1. A circuit, integrable on a single piece of semiconductor substrate material, for providing a bipolar voltage output at substantially double the voltage of a unipolar voltage input source, including:
  - first and second voltage input terminals,
  - first and second positive transfer capacitor connection terminals,
  - a first set of MOS semiconductor switches for selectively connecting said first voltage input terminal to said first and second positive transfer capacitor connection terminal and said second voltage input terminal to said second positive transfer capacitor connection terminal,
  - first and second positive reservoir capacitor connection terminals,
  - a second set of MOS semiconductor switches for selectively connecting said first voltage input ter-

terminal to said second positive transfer capacitor connection terminal and for selectively connecting said second voltage input terminal to said first positive reservoir capacitor connection terminal and said first positive transfer capacitor connection terminal to said second positive reservoir capacitor connection terminal,

first and second negative transfer capacitor connection terminals,

a third set of MOS semiconductor switches for selectively connecting said first positive reservoir capacitor connection terminal to said first negative transfer capacitor connection terminal and said second positive reservoir capacitor connection terminal to said second negative transfer capacitor connection terminal,

first and second negative reservoir capacitor connection terminals, said first negative reservoir capacitor connection terminal connected to said first positive reservoir capacitor connection terminal,

a fourth set of MOS semiconductor switches for selectively connecting said first negative transfer capacitor connection terminal to said second negative reservoir capacitor connection terminal and second negative transfer capacitor connection terminal to said first negative reservoir capacitor connection terminal,

selection circuitry for selectively activating said first, second, third and fourth sets of MOS semiconductor switches,

means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal,

means for clamping said second negative reservoir capacitor to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal,

means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material,

at least one RS-232 transmitter circuit, disposed in said semiconductor substrate material, having positive, negative and ground potential power conductors connected to said second positive reservoir capacitor terminal, said second negative reservoir capacitor connection terminal, and said first positive reservoir capacitor terminal, respectively, a data input connection terminal connected to said transmitter circuit for providing data to said transmitter, and a data output terminal connection for providing an output from said transmitter.

2. A circuit, integrable on a single piece of semiconductor substrate material, for providing a bipolar voltage output at substantially double the voltage of a unipolar voltage input source, including:

- first and second voltage input terminals,
- first and second positive transfer capacitor connection terminals,

- a first set of MOS semiconductor switches for selectively connecting said first voltage input terminal to said first and second positive transfer capacitor connection terminal and said second voltage input terminal to said second positive transfer capacitor connection terminal,

- first and second positive reservoir capacitor connection terminals,



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a second set of MOS semiconductor switches for selectively connecting said first voltage input terminal to said second positive transfer capacitor connection terminal and for selectively connecting said second voltage input terminal to said first positive reservoir capacitor connection terminal and said first positive transfer capacitor connection terminal to said second positive reservoir capacitor connection terminal, 5

first and second negative transfer capacitor connection terminals, 10

a third set of MOS semiconductor switches for selectively connecting said first positive reservoir capacitor connection terminal to said first negative transfer capacitor connection terminal and said second positive reservoir capacitor connection terminal to said second negative transfer capacitor connection terminal, 15

first and second negative reservoir capacitor connection terminals, said first negative reservoir capacitor connection terminal connected to said first positive reservoir capacitor connection terminal, 20

a fourth set of MOS semiconductor switches for selectively connecting said first negative transfer capacitor connection terminal to said second negative reservoir capacitor connection terminal and 25

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second negative transfer capacitor connection terminal to said first negative reservoir capacitor connection terminal,

selection circuitry for selectively activating said first, second, third and fourth sets of MOS semiconductor switches,

means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal,

means for clamping said second negative reservoir capacitor to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal,

means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material,

at least one RS-232 receiver circuit disposed on said semiconductor substrate material, including positive and ground power connection terminals connected to said first and second voltage input terminals and having a data input connection terminal and a data output connection terminal.

\* \* \* \* \*

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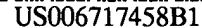
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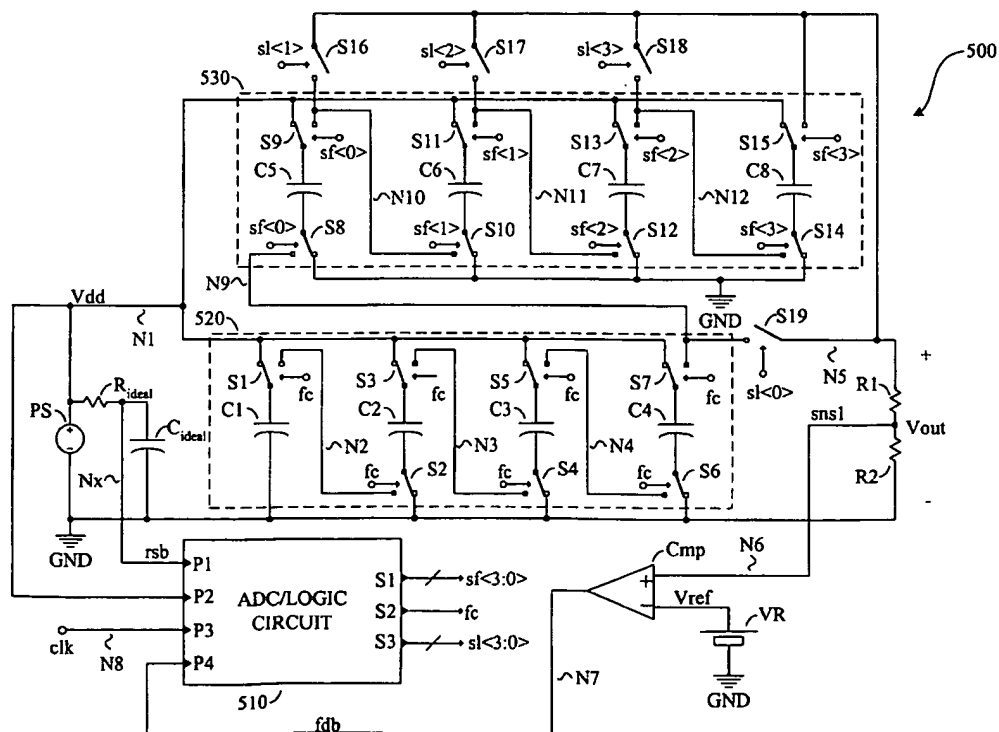
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(10) **Patent No.:** **US 6,717,458 B1**  
(45) **Date of Patent:** **Apr. 6, 2004**



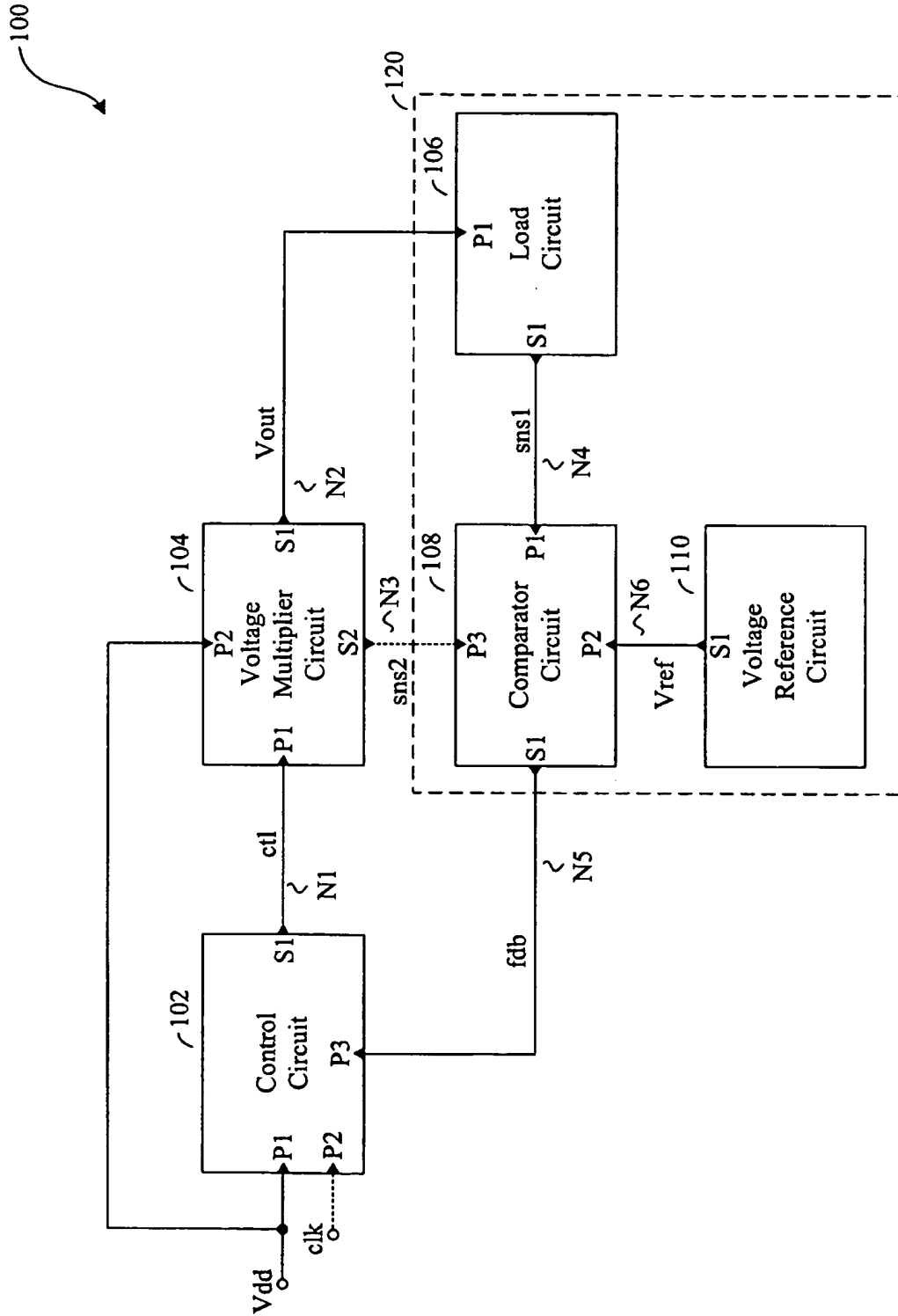


Fig.1

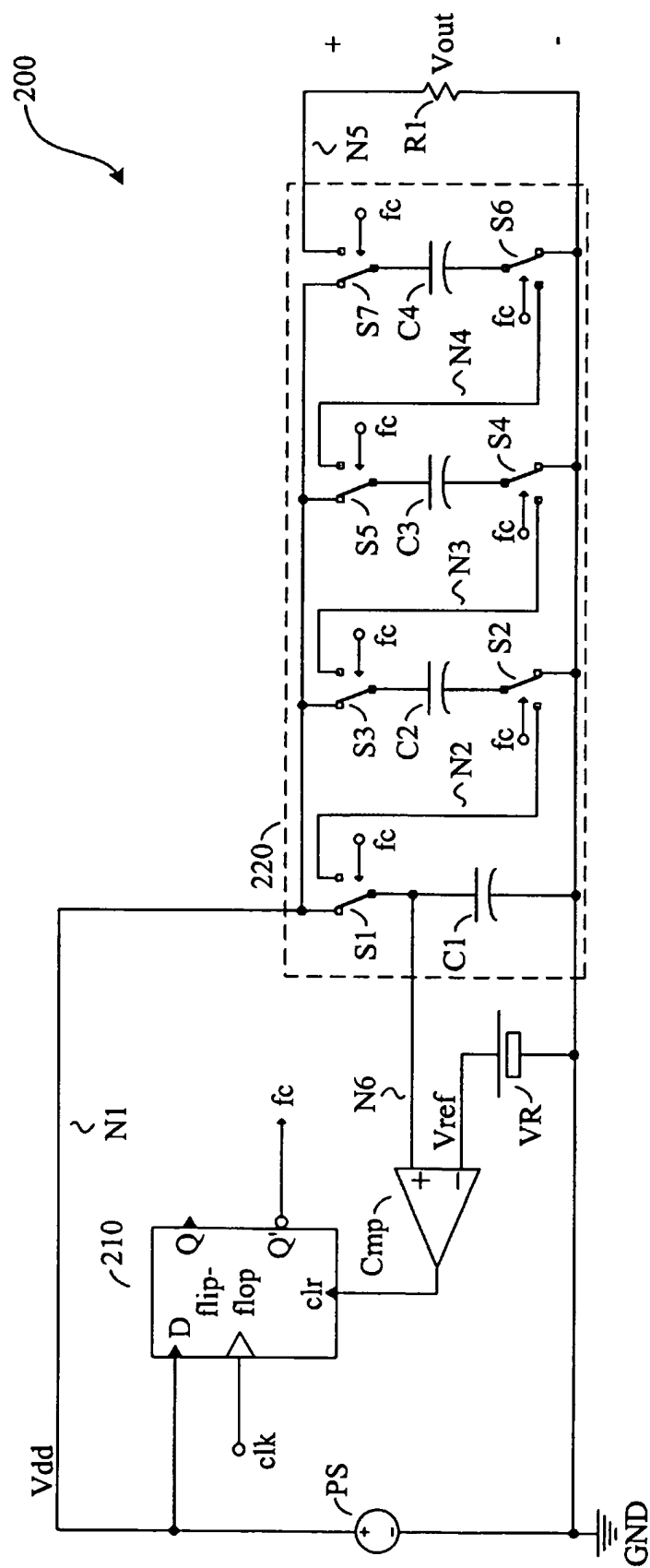


Fig.2

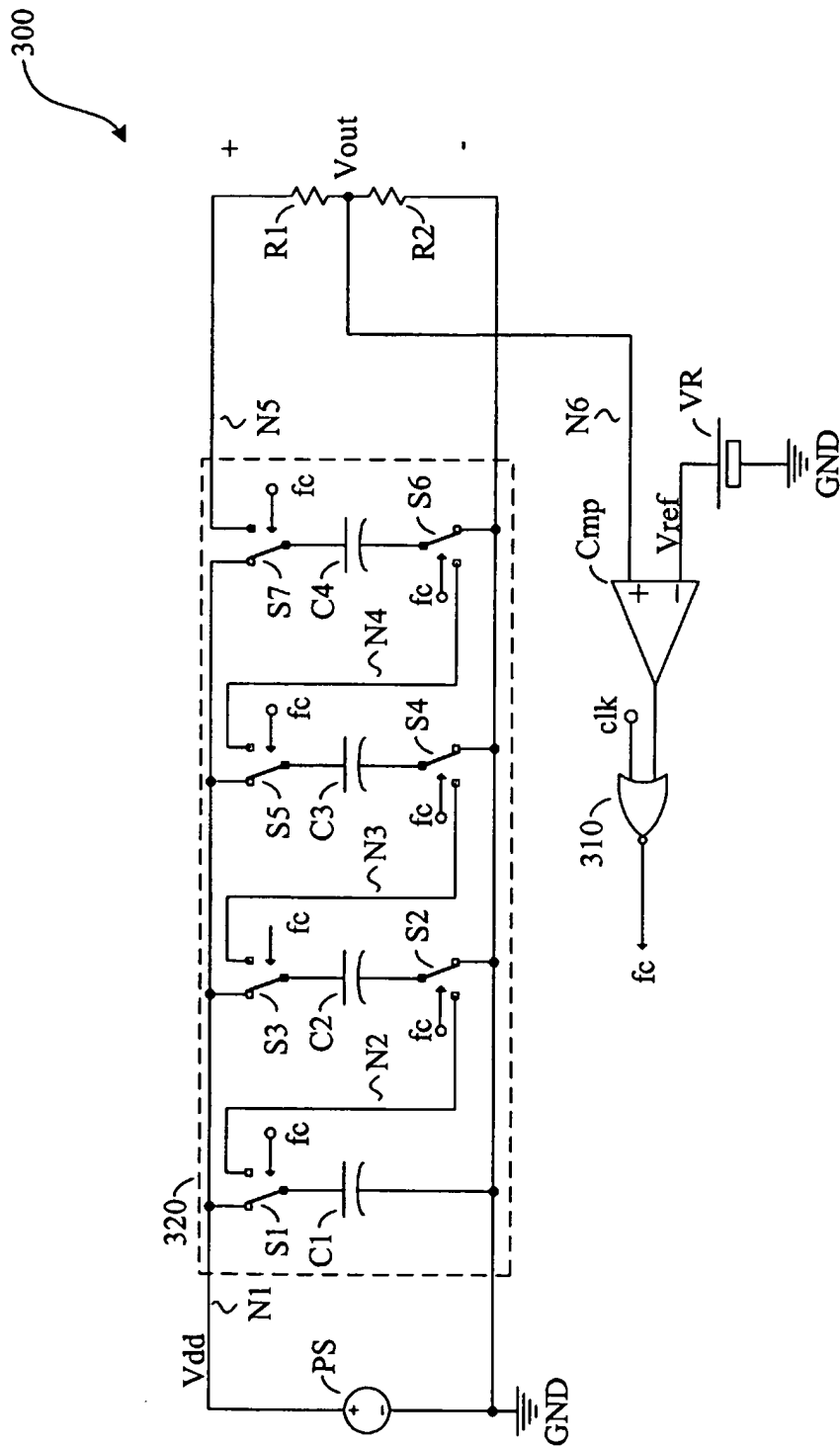


Fig.3

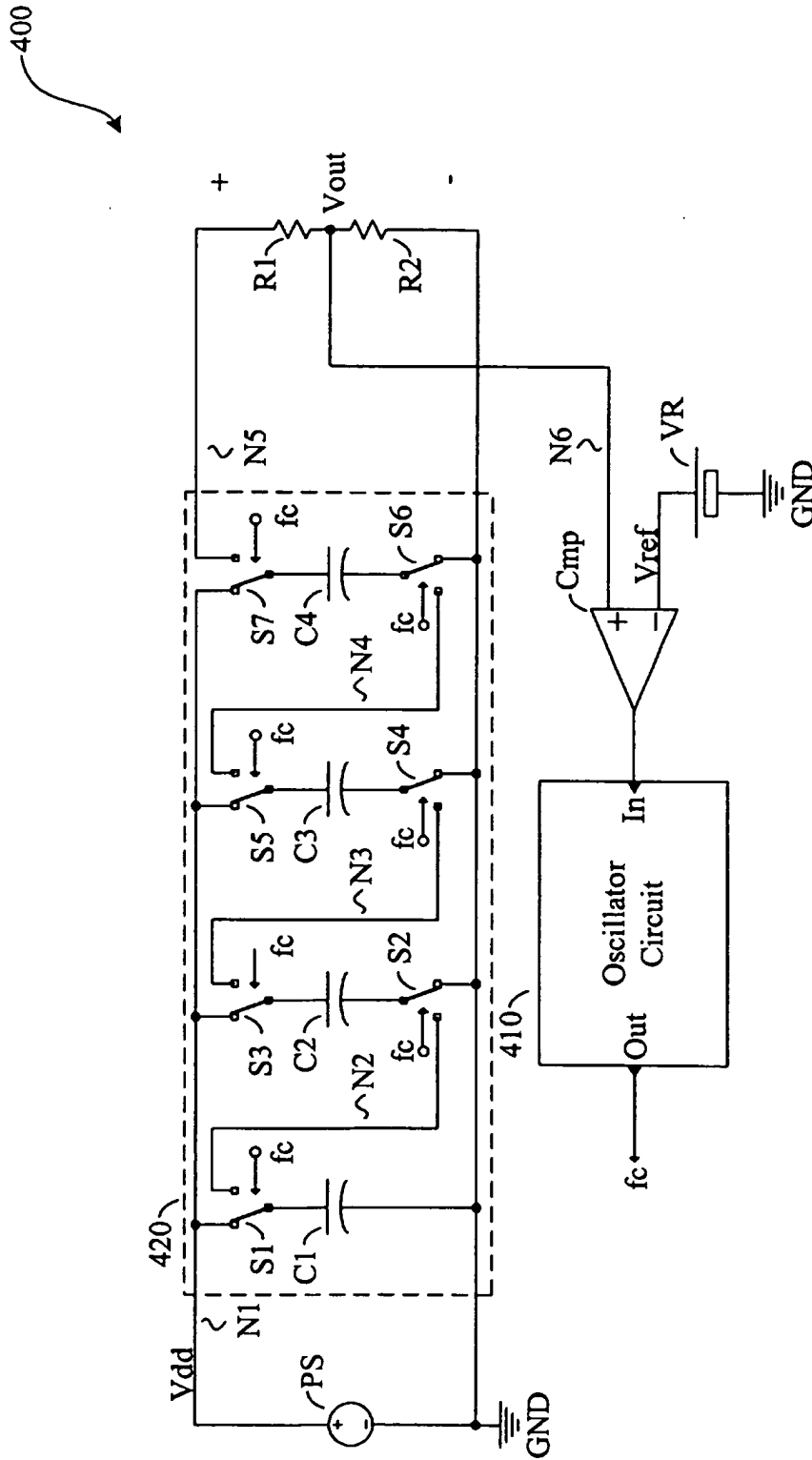
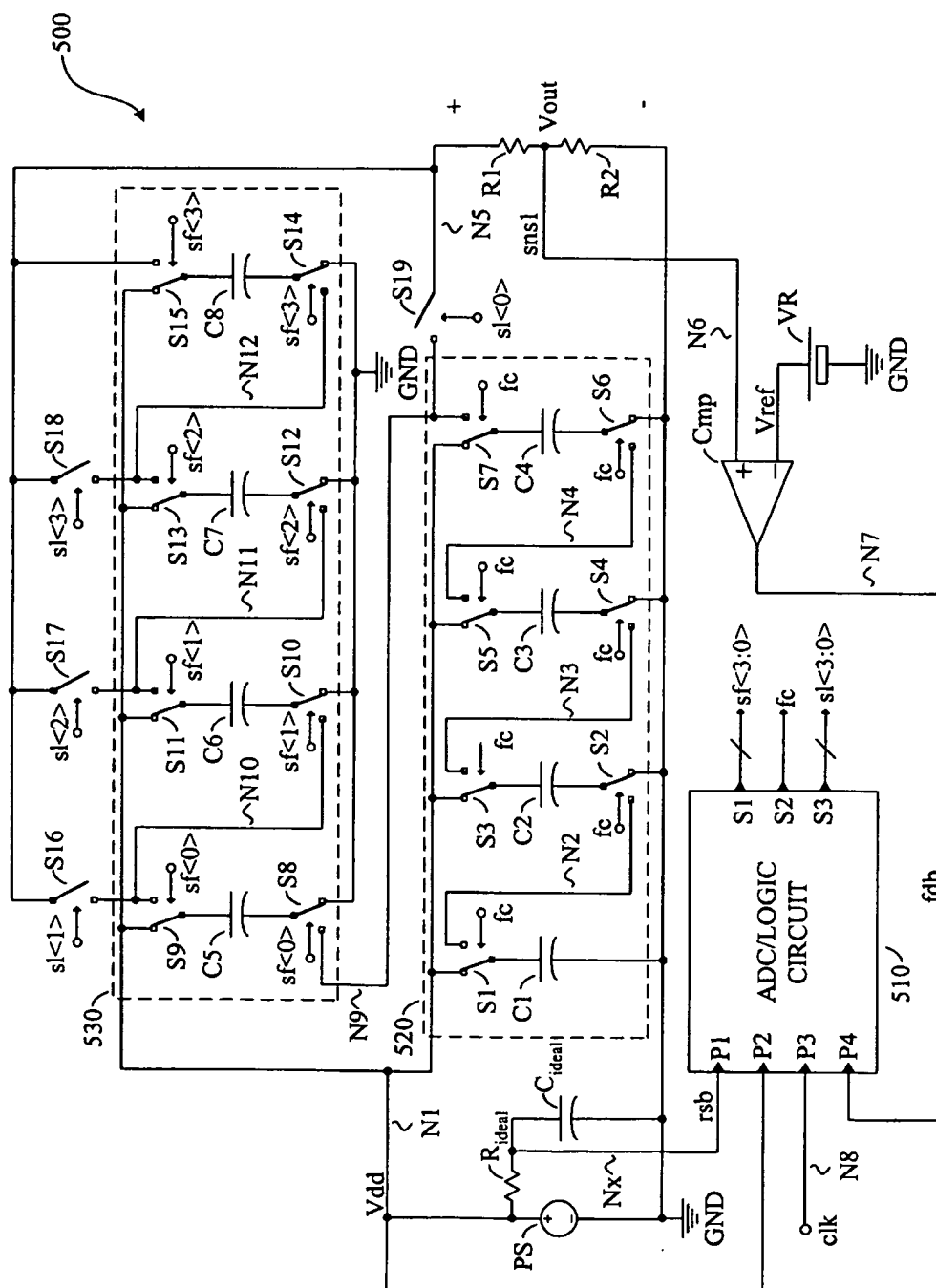


Fig.4



**Fig. 5**

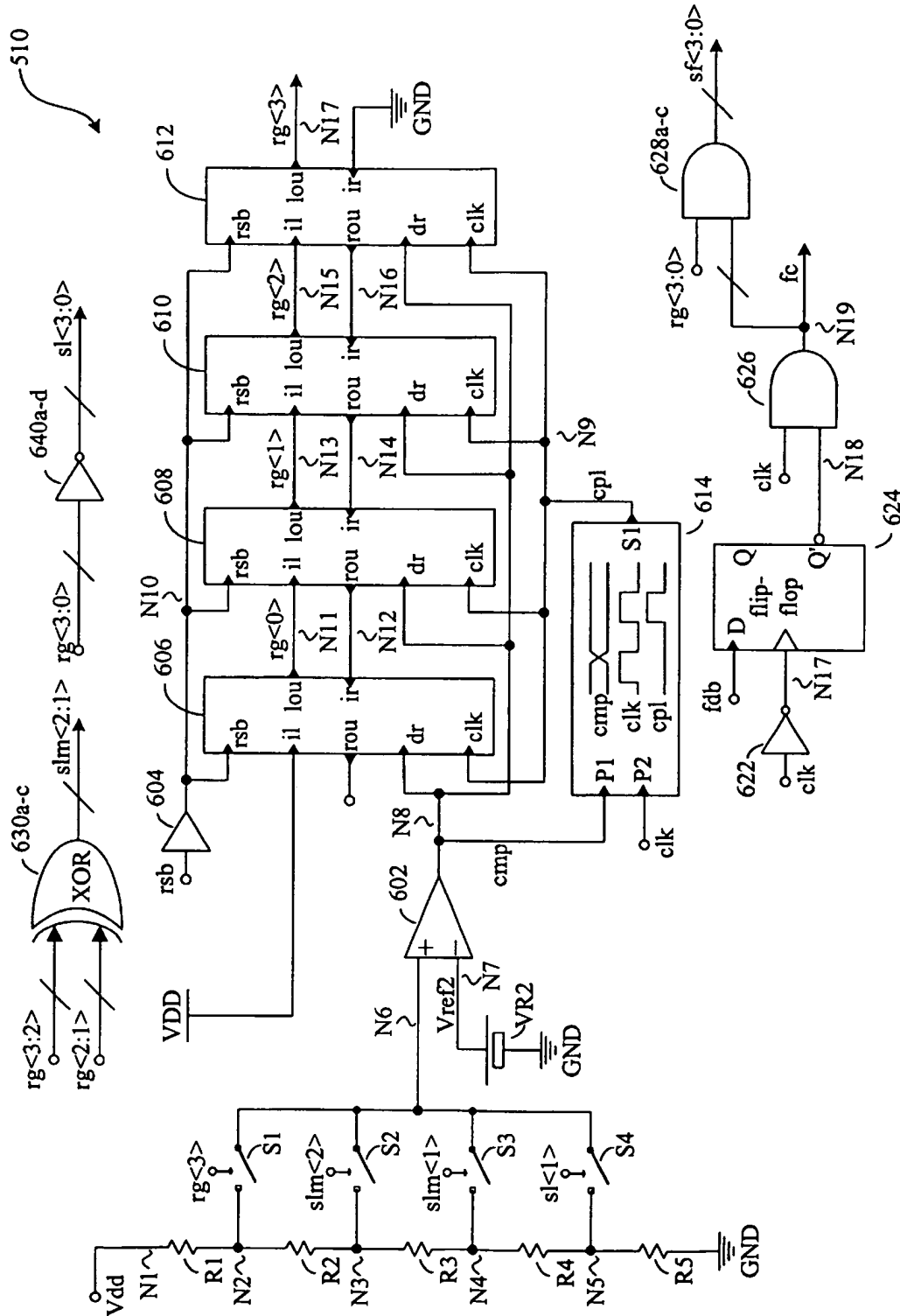


Fig.6



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## METHOD AND APPARATUS FOR A DC-DC CHARGE PUMP VOLTAGE CONVERTER-REGULATOR CIRCUIT

### FIELD OF THE INVENTION

The present invention relates generally to converter circuits. More particularly, the present invention relates to a DC-DC charge pump voltage converter-regulator circuit.

### BACKGROUND OF THE INVENTION

Many DC powered devices have subsystems that require a supply voltage higher than power supply can provide. For example, certain display devices that use liquid crystal technology require a relatively high voltage to operate. In these devices, the supply voltage is boosted in order to reach the required operating voltage. Various circuits may be used to do a DC-DC boost conversion of the supply voltage.

One method to obtain a regulated supply voltage for subsystems is to use switched capacitors voltage multipliers followed by a linear voltage regulator. The switched capacitors voltage multipliers multiply the supply voltage by a specified multiplication factor. For example, a supply voltage of 5 volts may be multiplied by a multiplication factor of 2 to achieve an output voltage of 10 volts. The linear regulator can then regulate the output voltage at any voltage level 10 volts or less.

### SUMMARY OF THE INVENTION

The present invention is directed to converter circuits. More particularly, the present invention relates to a DC-DC charge pump voltage converter-regulator. The converter-regulator of the present invention includes improved efficiency by providing other forms of regulation for the output voltage. In one embodiment, the converter-regulator includes charge level control implemented by a flip-flop circuit. In a second embodiment, the control of the output voltage is implemented by a logic circuit. In a third embodiment, the control of the output voltage is implemented by an oscillator circuit. In a fourth embodiment, the control of the output voltage is implemented by multiplying the supply voltage according to a multiplication factor dependent upon the level of the supply voltage.

Briefly stated, an apparatus and method for a DC-DC charge pump voltage converter-regulator circuit includes a control circuit, a multiplier circuit, and a feedback circuit. The feedback circuit includes a load circuit, a comparator circuit, and a voltage reference circuit. The multiplier circuit produces an output signal by multiplying a supply signal according to a multiplication factor. The output signal is communicated to the load circuit. The output signal is measured producing a sense signal. The voltage reference circuit produces a reference voltage. The control circuit regulates the output signal according to the result of a comparison between the sense signal and the reference voltage. In one embodiment, the multiplication factor is adjusted to compensate for a change in the supply signal. The multiplication factor may be increased to compensate for a decrease in the supply signal.

A more complete appreciation of the present invention and its improvements can be obtained by reference to the accompanying drawings, which are briefly summarized below, to the following detailed description of illustrative embodiments of the invention, and to the appended claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram illustrating an exemplary converter-regulator circuit;

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FIG. 2 is a schematic diagram illustrating another embodiment for the exemplary voltage converter-regulator circuit;

FIG. 3 is a schematic diagram illustrating yet another embodiment for the exemplary voltage converter-regulator circuit;

FIG. 4 is a schematic diagram illustrating yet another embodiment for the exemplary voltage converter-regulator circuit;

FIG. 5 is a schematic diagram illustrating yet another embodiment for the exemplary voltage converter-regulator circuit; and

FIG. 6 is a schematic diagram illustrating an exemplary logic circuit for the voltage converter-regulator circuit shown in FIG. 5, in accordance with the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following detailed description of exemplary embodiments of the invention, reference is made to the accompanied drawings, which form a part hereof, and which is shown by way of illustration, specific exemplary embodiments of which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Throughout the specification, and in the claims, the term "connected" means a direct electrical connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical connection between the things that are connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal or data signal. The meaning of "a", "an", and "the" include plural references. The meaning of "in" includes "in" and "on".

The present invention generally relates to a voltage converter-regulator for boosting and regulating an supply voltage. The regulated output voltage of the voltage converter-regulator may then be used with subsystems that require high supply voltages. The voltage converter-regulator has improved efficiency when used in conjunction with a battery cell. The voltage converter-regulator minimizes the use of additional circuitry for controlling a high voltage condition when the battery cell is fully charged.

For example, a typical supply voltage from a battery cell is in a range of 2 . . . 4.2V. The range depends on whether the battery cell is fully charged. If a subsystem requires a supply voltage 12V, then the supply voltage is boosted to supply the 12V. In previous configurations,  $\times 6$  voltage multiplier may be used to produce at least a 12V supply voltage for the range of supply voltages. The  $\times 6$  multiplier delivers 12 . . . 25.2V depending on the charge level of the battery cell. A linear regulator may then used to limit the output voltage to 12V for the full range of supply voltages. However, this results in 15.2V drop in the voltage when the battery cell is fully charged. Effectiveness of the configuration in this example is therefore  $(12/25.2)100=47.6\%$ . In

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addition, the circuitry involved in boosting and regulating the signal is required to handle high voltages of approximately 25.2V.

In the present invention, the supply voltage ( $V_{dd}$ ) is boosted to an output voltage ( $V_{out}$ ) that has a voltage level corresponding to a reference voltage ( $V_{ref}$ ). The supply voltage ( $V_{dd}$ ) is boosted until it is clamped to a target voltage level, minimizing the circuitry needed for high voltage conditions. The output voltage ( $V_{out}$ ) is then regulated at the target voltage, where the target voltage represents the desired supply voltage of a given subsystem.

FIG. 1 is a schematic diagram illustrating an exemplary voltage converter-regulator circuit in accordance with the present invention. The voltage converter-regulator circuit (100) includes a control circuit (102), a voltage multiplier circuit (104), and a feedback circuit (120). The feedback circuit (120) includes a load circuit (106), a comparator circuit (108), and a voltage reference circuit (110).

The control circuit (102) produces a control signal ( $ctl$ ) at node N1 in response to an supply voltage ( $V_{dd}$ ), a clock signal ( $clk$ ), and a feedback signal ( $fdb$ ). The voltage multiplier circuit (104) produces the output voltage ( $V_{out}$ ) at node N2 and an optional sense signal ( $sns2$ ) at node N3 in response to the supply voltage ( $V_{dd}$ ) and the control signal ( $ctl$ ). The load circuit (106) produces an output sense signal ( $sns1$ ) in response to the output voltage ( $V_{out}$ ). The voltage reference circuit (110) produces a voltage reference signal ( $V_{ref}$ ) at node N6. The comparator circuit (108) produces the feedback signal at node N5 in response to the reference signal ( $V_{ref}$ ) and the either an output sense signal ( $sns1$ ) or the optional sense signal ( $sns2$ ).

In operation, the voltage converter-regulator circuit (100) produces an output voltage ( $V_{out}$ ) that corresponds to the reference voltage ( $V_{ref}$ ). The output voltage ( $V_{out}$ ) may correspond to the reference voltage ( $V_{ref}$ ) through a multiplication factor "n", or another relationship. Also, the output voltage ( $V_{out}$ ) may be calculated from either the output sense signal ( $sns1$ ) or the optional sense signal ( $sns2$ ). The output sense signal ( $sns1$ ) or the optional sense signal ( $sns2$ ) indicates that the level of the output voltage ( $V_{out}$ ). A comparison of the output sense signal ( $sns1$ ) or the optional sense signal ( $sns2$ ) to the voltage reference signal ( $V_{ref}$ ) also indicates the level of the output voltage ( $V_{out}$ ) in comparison to its target voltage. (i.e.,  $V_{ref}=sns1$ , or  $V_{ref}=sns2$ , then  $V_{out}=target\ voltage$ ). Therefore, the feedback signal ( $fdb$ ) indicates whether the output voltage ( $V_{out}$ ) is substantially equal to its target voltage.

The voltage multiplier circuit (104) boosts the output voltage ( $V_{out}$ ) to reach its target voltage depending on the potential of the feedback signal ( $fdb$ ). When the feedback signal ( $fdb$ ) indicates that the output voltage ( $V_{out}$ ) is below its target voltage, the control circuit (102) actuates the voltage multiplier circuit (104). When actuated, the voltage multiplier circuit (104) begins to increase the output voltage ( $V_{out}$ ) at the next pulse of the clock signal ( $clk$ ) until it reaches its target voltage. The occurrence of the output voltage ( $V_{out}$ ) reaching its target voltage is reflected in the potential of the feedback signal ( $fdb$ ). When the output voltage ( $V_{out}$ ) reaches its target voltage, the control circuit (102) interrupts the voltage multiplier circuit (104) from continuing to increase the output voltage ( $V_{out}$ ) at the next clock pulse. Therefore, the output voltage ( $V_{out}$ ) is clamped to a target voltage and avoids a high voltage condition.

FIG. 2 is a schematic diagram illustrating another embodiment for the exemplary voltage converter-regulator circuit in accordance with the present invention. The voltage

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converter-regulator circuit (200) includes a flip-flop circuit (210), a comparator circuit (Cmp), a load circuit represented by a resistor ( $R1$ ), a multiplier circuit (220), and a voltage reference circuit (VR). The multiplier circuit (220) includes seven switch circuits (S1-S7) and four capacitance circuits (C1-C4). A power supply circuit (PS) represented by a voltage source, is also included in FIG. 2.

The voltage converter-regulator circuit (200) operates similarly to the voltage converter-regulator circuit (100) shown in FIG. 1. The power supply circuit (PS) produces a supply voltage ( $V_{dd}$ ) at node N1. In the present embodiment, the seven switch circuits (S1-S7) control the connection of the four capacitance circuits (C1-C4) in response to a control signal ( $fc$ ). Switch circuits S1, S3, S5, S7 change the connection of each capacitance circuit (C1-C4) between being coupled to node N1 and another node (N2-N5) respectively. Switch circuits S2, S4, S6 also change the connection of capacitance circuits C2-C4 between being coupled to a ground terminal (GND) and another node (N2-N4) respectively. The switch circuits (S1-S7) are in one of two possible positions: position 1 during a first interval and position 2 during a second interval.

When the switch circuits (S1-S7) are in position 1, the capacitance circuits (C1-C4) are coupled in parallel between node N1 and the ground terminal (GND). Each capacitance circuit (C1-C4) charges exponentially at a rate dependent upon the size of the capacitance circuits (C1-C4) and the type of power supply circuit (PS) used. A non-inverting input of the comparator circuit (Cmp) is coupled to node N6. The comparator circuit (Cmp) also includes an inverting input that is coupled to the voltage reference circuit (VR) and an output coupled to a clear input of the flip-flop circuit (210). The comparator circuit (Cmp) compares the voltage level at node N6 with a reference voltage ( $V_{ref}$ ) produced by the voltage reference circuit (VR). The comparator circuit (Cmp) produces a clear signal when the charge on the capacitance circuits (C1-C4) reaches a voltage level corresponding to the reference voltage ( $V_{ref}$ ). The flip-flop circuit (210) receives the clear signal at a clear input. The flip-flop circuit (210) includes the clear input, a D input, a clock input, and two outputs (Q, Q'). The D input is coupled to node N1. The flip-flop circuit (210) produces the control signal ( $fc$ ) with a high logic level (logic "1") at the Q' output in response to the clear signal at the next rising clock edge of the clock signal ( $clk$ ). The switch circuits (S1-S7) switch from position 1 to position 2 in response to the control signal ( $fc$ ).

When the switch circuits (S1-S7) are in position 2, the capacitance circuits (C1-C4) are coupled in series between the ground terminal (GND) and node N5. When series-connected, the capacitance circuits (C1-C4) produce a boosted output voltage ( $V_{out}$ ) across the resistor ( $R1$ ). The output voltage ( $V_{out}$ ) rises according a slope to reach an asymptotic voltage level that is approximately equal four-times the supply voltage ( $V_{dd}$ ). However, in the present embodiment, the output voltage ( $V_{out}$ ) is clamped to a voltage level that is approximately equal to four-times the reference voltage ( $V_{ref}$ ). The output voltage ( $V_{out}$ ) in the present embodiment is dependent upon the load. Therefore, output voltage ( $V_{out}$ ) is equal to four-times the reference voltage when the output current is approximately zero. In another embodiment, a greater or fewer number of capacitance circuits may be used. At the next clock edge of the clock signal ( $clk$ ), the flip-flop circuit (210) changes states, flipping the control signal ( $fc$ ) from a high logic level (logic "1") to a low logic level (logic "0"). When the control signal is at low logic level, the capacitance circuits (C1-C4) are

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connected in parallel and are charged by the power supply circuit (PS). The switching process repeats such that the output voltage (Vout) is substantially clamped to a predetermined voltage level based upon a multiple of the reference voltage.

FIG. 3 is a schematic diagram illustrating another embodiment for the exemplary voltage converter-regulator circuit in accordance with the present invention. The voltage converter-regulator circuit (300) includes a logic circuit (310), a comparator circuit (Cmp), a load circuit represented by two resistors (R1, R2), seven a multiplier circuit (320), and a voltage reference circuit (VR). The multiplier circuit (320) includes seven switch circuits (S1–S7) and four capacitance circuits (C1–C4). A power supply circuit (PS) represented by a voltage source, is also included in FIG. 3.

The voltage converter-regulator circuit (300) operates similarly to the voltage converter-regulator circuit (100) shown in FIG. 1. The power supply circuit (PS) produces a supply voltage at node N1. In the present embodiment, the seven switch circuits (S1–S7) control the connection of the four capacitance circuits (C1–C4) in response to a control signal (fc). Switch circuits S1, S3, S5, S7 change the connection of each capacitance circuit (C1–C4) between being coupled to node N1 and another node (N2–N5) respectively. Switch circuits S2, S4, S6 also change the connection of capacitance circuits C2–C4 between being coupled to a ground terminal (GND) and another node (N2–N4) respectively. The switch circuits (S1–S7) are in one of two possible positions: position 1 and position 2.

When the switch circuits (S1–S7) are in position 1, the capacitance circuits (C1–C4) are coupled in parallel between node N1 and the ground terminal (GND). Each capacitance circuit (C1–C4) charges exponentially at a rate dependent upon the size of the capacitance circuits (C1–C4) and the type of power supply circuit (PS) used. A non-inverting input of the comparator circuit (Cmp) is coupled to node N6. The comparator circuit (Cmp) also includes an inverting input that is coupled to the voltage reference circuit (VR) and an output coupled to a first input of the logic circuit (310). The comparator circuit (Cmp) compares the voltage level at node N6 with a reference voltage (Vref) produced by the voltage reference circuit (VR). The comparator circuit (Cmp) produces feedback signal when output voltage reaches a predetermined voltage level corresponding to the reference voltage (Vref). The logic circuit (310) receives the feedback signal at the first input. The logic circuit (310) includes the first input, a second input, and an output. The second input receives a clock signal (clk) from a clock signal generator (not shown). The logic circuit (310) produces the control signal (fc) with a high logic level (logic “1”) at the Q’ output in response to the clear signal at the next rising clock edge of the clock signal (clk). The switch circuits (S1–S7) switch from position 1 to position 2 in response to the control signal (fc).

When the switch circuits (S1–S7) are in position 2, the capacitance circuits (C1–C4) are coupled in series between the ground terminal (GND) and node N5. When series-connected, the capacitance circuits (C1–C4) produce a boosted output voltage (Vout) across the load circuit (RL). The output voltage (Vout) rises according a slope to reach an asymptotic voltage level that is approximately equal four-times the supply voltage (Vdd). However, in the present embodiment, the output voltage (Vout) is clamped to a voltage level that corresponds to the reference voltage (Vref). In this embodiment, the output voltage (Vout) of the voltage converter-regulator circuit (300) equals to  $V_{ref}(R1+R2)/R2$ . In another embodiment, another configuration may

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be used such that the output voltage (Vout) corresponds to the reference voltage (Vref) according to another relationship. When the output voltage (Vout) decreases below the predetermined voltage level, the logic circuit (310) flips the control signal (fc) from a high logic level (logic “1”) to a low logic level (logic “0”). When the control signal is at low logic level, the capacitance circuits (C1–C4) are connected in parallel and are charged by the power supply circuit (PS). The switching process repeats such that the output voltage (Vout) is substantially clamped to a predetermined voltage level based upon a multiple of the reference voltage. In this embodiment, the voltage converter-regulator circuit (300) controls the clock pulse width. The clock pulse width is dependent on the output voltage (Vout), wherein the output voltage operates as a control signal.

The advantage of the voltage converter-regulator circuit (300) is that it provides a stable output voltage (Vout) for certain range of output load current. In another embodiment, a switched capacitor voltage divider may be used instead of resistors R1 and R2 along with a clocked synchronous comparator to provide additional effectiveness. In yet another embodiment, control may be implemented by skipping clock pulses instead of pulse width modulation for better noise tolerance.

In this embodiment the logic circuit (310) is illustrated as a NOR gate. In another embodiment, a different logic circuit or combination of logic circuits may be used without departing from the purpose of the present invention.

FIG. 4 is a schematic diagram illustrating another embodiment for the exemplary voltage converter-regulator circuit in accordance with the present invention. The voltage converter-regulator circuit (400) includes an oscillator circuit (410), a comparator circuit (Cmp), a load circuit represented by two resistors (R1, R2), a multiplier circuit (420), and a voltage reference circuit (VR). The multiplier circuit (420) includes seven switch circuits (S1–S7) and four capacitance circuits (C1–C4). A power supply circuit (PS) represented by a voltage source, is also included in FIG. 4.

The voltage converter-regulator circuit (400) operates similarly to the voltage converter-regulator circuit (300) shown in FIG. 3. The voltage converter-regulator circuit (400) includes a controlled oscillator circuit (410) in place of the logic circuit (310) shown in FIG. 3. The voltage converter-regulator circuit (400) has a high efficiency and fast dynamic response to load current changes. The fast dynamic response results in a low output voltage ripple. Clock pulses used in other embodiments that require a clock signal are skipped when load current is low and the output voltage (Vout) decreases slowly in the present embodiment. The skipped pulses result in a low switching frequency and low circuit power consumption. The lower frequency and power consumption result in a high efficiency. The oscillator circuit (410) frequency may be selected at a maximum frequency according to the capacitors used and the switch resistance associated with each switch circuit (S1–S7) for better dynamic performance of the voltage converter-regulator circuit (400). In addition, the oscillator circuit (410) operates to track the frequency of power supply circuit (PS) and the ambient temperature, extending the operation of the voltage converter-regulator circuit (400).

FIG. 5 is a schematic diagram illustrating another embodiment for the exemplary voltage converter-regulator circuit in accordance with the present invention. The voltage converter-regulator circuit (500) includes an ADC/logic circuit (510), a comparator circuit (Cmp), a load circuit represented by two resistors (R1, R2), two multiplier circuits

(520, 530), four switch circuits (S16–S19), a voltage reference circuit (VR), a resistance circuit ( $R_{ideal}$ ), and capacitance circuit ( $C_{ideal}$ ). The multiplier circuits (520, 530) include fifteen switch circuits (S1–S15) and eight capacitance circuits (C1–C8).

The power supply circuit (PS) is coupled between a power supply node (N1) and a ground terminal (GND). The resistance circuit ( $R_{ideal}$ ) is coupled between the power supply node (N1) and node Nx. The capacitance circuit ( $C_{ideal}$ ) is coupled between node Nx and a ground terminal (GND). In multiplier circuit 520, capacitance circuits C1–C4 are coupled between the ground terminal (GND) and the power supply node (N1) when switch circuits S1–S7 are in a first position, hereinafter referred to as position 1. Capacitance circuits C1–C4 are coupled between the ground terminal (GND), node N2, node N3, node N4, and node N9 respectively (i.e., capacitance circuit C2 is coupled between node N2 and node N3) when switch circuits S1–S7 are in a second position, hereinafter referred to as position 2.

In multiplier circuit 530, capacitance circuits C5–C8 are coupled between the ground terminal (GND) and the power supply node (N1) when switch circuits S8–S15 are in position 1. Capacitance circuits C5–C8 are coupled between node N9, node N10, node N11, node N12, and node N5 respectively (i.e., capacitance circuit C7 is coupled between node N11 and node N12) when switch circuits S1–S7 are in position 2.

Switch circuits S16–S18 are coupled between node N5 and nodes N1 N12 respectively. Switch circuit S19 is coupled between the power supply node (N1) and node N5. Resistor R1 is coupled between node N5 and node N6. Resistor R2 is coupled between node N6 and the ground terminal (GND). The comparator circuit (Cmp) includes a non-inverting input coupled to node N6, an inverting input coupled to the voltage reference circuit (VR), and an output coupled to node N7. The ADC/logic circuit (510) includes a first input (P1) coupled to node Nx, a second input (P2) that is coupled to the power supply node (N1), a third input (P3) that is coupled to node N8, and a fourth input (P4) that is coupled to node N7. The ADC/logic circuit (510) includes three outputs (S1–S4) that control the positions of the switch circuits (S1–S19). The ADC/logic circuit (510) is described in greater detail in FIG. 6.

The voltage converter-regulator circuit (500) operates similarly to the voltage converter-regulator circuit (300) shown in FIG. 3. However, voltage converter-regulator circuit (500) includes a second multiplier circuit 530. The power supply circuit (PS) produces a supply voltage (Vdd) at node N1. Switch circuits S1–S15 switch between a first position, position 1, and a second position, position 2. Switch circuits S16–S19 are either open or closed. Switch circuits S1–S7 are actuated in response to a first control signal (fc). Switch circuits S8–S15 are actuated in response to control signals sf<3:0>. Switch circuits S8 and S9 are actuated in response to control signal sf<0>. Switch circuits S10 and S11 are actuated in response to control signal sf<1>. Switch circuits S12 and S13 are actuated in response to control signal sf<2>. Switch circuits S14 and S15 are actuated in response to control signal sf<3>. Switch circuits S16–S19 are actuated in response to control signals sl<3:0>. Switch circuit 16 is actuated in response to control signal sl<1>. Switch circuit 17 is actuated in response to control signal sl<2>. Switch circuit 18 is actuated in response to control signal sl<3>. Switch circuit 19 is actuated in response to control signal sl<0>.

The control signals (fc, sl<3:0>, sf<3:0>) are produced by the ADC/logic circuit (510) in response to a reset signal (rsb)

that is provided at node Nx, a supply signal (Vdd) that is provided at node N1, a clock signal (clk) produced at node N8, and a feedback signal (fdb) that is provided at node N7. The supply voltage (Vdd) is produced by the power supply circuit (PS). The clock signal (clk) is produced by a clock signal generator (not shown). The feedback signal (fdb) is produced by the comparator circuit (Cmp) in response to a comparison of a sense signal (sns1) to a reference signal (Vref). The sense signal (sns1) is a voltage level that corresponds to a measurement of the output voltage (Vout) of the voltage converter-regulator circuit (500). The reference signal (Vref) is produced by the voltage reference circuit (VR).

When switch circuits S1–S15 are in position 1, the capacitance circuits (C1–C8) are coupled in parallel between the power supply node (N1) and the ground terminal (GND). Switch circuits S1–S15 remain in position 1 until the capacitance circuits (C1–C8) charge to a predetermined voltage level. Once the capacitance circuits (C1–C8) are charged to the predetermined voltage level, a select number of the switch circuits (S1–S19) may be actuated to produce a predetermined output voltage (Vout) across the load circuit (R1, R2).

In one embodiment, the power supply circuit (PS) is a battery cell that produces different supply voltage (Vdd) levels depending upon the level of charge present in the battery cell. For instance, the supply voltage (Vdd) may be at a low voltage level when the battery cell is substantially discharged and a high voltage level when the battery cell is substantially charged. For example, the supply voltage (Vdd) may range from 2V to 4V, or over some other range of voltages associated with battery cells. The present embodiment compensates for the degradation of the supply voltage (Vdd) by multiplying the supply voltages by a range of multiplication factors (n). For supply voltages in the range from 2V to 4V, the following exemplary table (table 1) illustrates the affect of changing the multiplication factor on the output voltage (Vout).

TABLE 1

Vdd	<2.3 V	2.3–2.6 V	2.6–3.2 V	3.2–4 V	>4 V
n	8	7	6	5	4
Vout	<18.4 V	16–18.2 V	15.6–19.2 V	16–20 V	>16 V

From exemplary Table 1, it can be observed that the output voltage (Vout) does not reach a voltage level beyond 20V. The present invention operates to avoid a high voltage condition by limiting the output voltage (Vout) to lower voltages.

The multiplication factor (n) changes in response to a change in the supply voltage (Vdd) to maintain a predetermined voltage level for the output voltage (Vout). The multiplication factor (n) is dependent on the number and size of the capacitance circuits (C1–C8) that are coupled together in series when the capacitance circuits are discharged to the load circuit (R1, R2).

The first multiplier circuit (520) of the voltage converter-regulator (500) multiplies the supply voltage (Vdd) by a multiplication factor of 4 when capacitance circuits C1–C4 are coupled together in series. Each additional capacitance circuit (C5–C8) that is coupled in series with capacitance circuits C1–C4 of the second multiplier circuit (530) increases the multiplication factor (n) by 1. The switch circuits (S1–S19) are selectively actuated to either include or exclude the capacitance circuits (C5–C8) of the second multiplier circuit (530).

In a first example, the voltage converter-regulator circuit (500) is configured to multiply the supply voltage (Vdd) by a multiplication factor of 4. For this example, switch circuits S16–S18 are open, switch circuit S19 is closed, and switch circuits S1–S7 are switched from position 1 to position 2 in response to the clock signal (clk) (i.e., at the next rising edge). Switch circuits S8–S15 are maintained in position 1. When switch circuits are switched from position 1 to position 2, the sum of the voltage levels for capacitance circuits C1–C4 may be observed across the resistors R1 and R2. With equal-sized and sufficiently large capacitance circuits C1–C4, the output voltage (Vout) across resistors R1 and R2 is proportional to four times the supply voltage (Vdd).

In a second example, the voltage converter-regulator circuit (500) is configured to multiply the supply voltage (Vdd) by a multiplication factor of 5. For this example, switch circuit S16 is closed, switch circuits S17–S19 are open, and switch circuits S1–S9 are switched from position 1 to position 2 in response to the clock signal (clk). Switch circuits S10–S15 are maintained in position 1. When switch circuits S1–S9 are switched from position 1 to position 2, the sum of the voltage levels for capacitance circuits C1–C5 may be observed across the resistors R1 and R2.

In a third example, the voltage converter-regulator circuit (500) is configured to multiply the supply voltage (Vdd) by a multiplication factor of 6. For this example, switch circuit S17 is closed, switch circuits S16, S18, and S19 are open, and switch circuits S1–S11 are switched from position 1 to position 2 in response to the clock signal (clk). Switch circuits S12–S15 are maintained in position 1. When switch circuits S1–S11 are switched from position 1 to position 2, the sum of the voltage levels for capacitance circuits C1–C6 may be observed across the resistors R1 and R2.

In a fourth example, the voltage converter-regulator circuit (500) is configured to multiply the supply voltage (Vdd) by a multiplication factor of 7. For this example, switch circuit S18 is closed, switch circuits S16, S17, and S19 are open, and switch circuits S1–S13 are switched from position 1 to position 2 in response to the clock signal (clk). Switch circuits S14 and S15 are maintained in position 1. When switch circuits S1–S13 are switched from position 1 to position 2, the sum of the voltage levels for capacitance circuits C1–C7 may be observed across the resistors R1 and R2.

In a fifth example, the voltage converter-regulator circuit (500) is configured to multiply the supply voltage (Vdd) by a multiplication factor of 8. For this example, switch circuits S16–S19 are open, and switch circuits S1–S15 are switched from position 1 to position 2 in response to the clock signal (clk). When switch circuits S1–S15 are switched from position 1 to position 2, the sum of the voltage levels for capacitance circuits C1–C4 may be observed across the resistors R1 and R2.

In other embodiments, an increased or decreased number of multiplier circuits or capacitance circuits may be used to increase or decrease the multiplication factor (n) available to the voltage converter-regulator circuit (500).

FIG. 6 is a schematic diagram illustrating an exemplary logic circuit for the voltage converter-regulator circuit shown in FIG. 5. The logic circuit (510) includes five resistance circuits (R1–R5), four switch circuits (S1–S4), a comparator circuit (602), a voltage reference circuit (VR2), a buffer circuit (604), five flip-flop circuits (606, 608, 610, 612, 624), a clock generation circuit (614), five inverter circuits (622, 640a–d), four AND logic circuits (626, 628a–c), and three XOR logic circuits (630a–c).

The resistance circuits (R1–R5) are coupled in a resistance ladder separated by nodes (N1–N5), or voltage tap points. Resistance circuit R1 is coupled between node N1 and node N2. Resistance circuit R2 is coupled between node N2 and node N3. Resistance circuit R3 is coupled between node N3 and node N4. Resistance circuit R4 is coupled between node N4 and node N5. Resistance circuit R5 is coupled between node N5 and a ground terminal (GND).

The switch circuits (S1–S4) are coupled between node N6 nodes N2–N5 respectively. The comparator circuit (602) includes a non-inverting input that is coupled to node N6, an inverting input that is coupled to node N7, and an output that is coupled to node N8. The voltage reference circuit (VR2) is coupled between node N7 and the ground terminal (GND). The clock generation circuit (614) includes a first input (P1) that is coupled to node N8, a second input (P2) that is coupled to the clock signal (clk) that is illustrated in FIG. 5, and an output (S1) that is coupled to node N9. The buffer circuit (604) is coupled between node N10 and the reset signal (rsb) that is illustrated in FIG. 5.

In this embodiment, flip-flop circuits 606, 608, 610, and 612 are bi-directional flip-flops circuits. Flip-flop circuit 606 includes a first input (rsb) that is coupled to node N10, a second input (il) that is coupled to the power supply node (VDD), a third input (ir) that is coupled to node N12, a fourth input (dr) that is coupled to node N8, a fifth input (clk) that is coupled to node N9, a first output (lou) that is coupled to node N11, and a second output (rou) that is coupled to node N12. Flip-flop circuit 608 includes a first input (rsb) that is coupled to node N10, a second input (il) that is coupled to node N11, a third input (ir) that is coupled to node N14, a fourth input (dr) that is coupled to node N8, a fifth input (clk) that is coupled to node N9, a first output (lou) that is coupled to node N13, and a second output (rou) that is coupled to node N12. Flip-flop circuit 610 includes a first input (rsb) that is coupled to node N10, a second input (il) that is coupled to node N13, a third input (ir) that is coupled to node N16, a fourth input (dr) that is coupled to node N8, a fifth input (clk) that is coupled to node N9, a first output (lou) that is coupled to node N15, and a second output (rou) that is coupled to node N14. Flip-flop circuit 612 includes a first input (rsb) that is coupled to node N10, a second input (il) that is coupled to node N15, a third input (ir) that is coupled to the ground terminal (GND), a fourth input (dr) that is coupled to node N8, a fifth input (clk) that is coupled to node N9, a first output (lou) that is coupled to node N17, and a second output (rou) that is coupled to node N16.

Inverter circuit 622 is coupled between node N17 and the clock signal (clk) that is illustrated in FIG. 5. Flip-flop circuit 624 includes a first input (D) that is coupled to the feedback signal (fdb) that is illustrated in FIG. 5, a second input that is coupled to node N17, a first output (Q), and a second output (Q') that is coupled to node N18. AND logic circuit 626 includes a first input that is coupled to the clock signal (clk) that is illustrated in FIG. 5, a second input that is coupled to node N18, and an output that is coupled to node N19. AND logic circuits 628a–c each include a first input that is coupled to a corresponding one of signals rg<3:0> respectively, a second input that is coupled to node N19, and an output that corresponds to signals sf<3:0> that are illustrated in FIG. 5.

XOR logic circuits 630a–c each include a first input that is coupled to signals rg<3:2> respectively, a second input that is coupled to a corresponding one of signals rg<2: 1> respectively, and an output that corresponds to one of signals slm<2: 1>. Inverter circuits 640a–d each include an input that is coupled to a corresponding one of signals rg<3:0> and an output that corresponds to one of signals sl<3:0> that are illustrated in FIG. 5.

In operation, the resistance circuits (R1–R5) form a voltage divider with multiple tap points. Each voltage tap point corresponds to a particular potential related to the supply voltage (Vdd). A potential is provided at node N6 when one or more of the switch circuits (S1–S4) are closed. Switch circuits S1–S4 are actuated in response to signals rg<3>, slm<2>, slm<1>, and sl<1> respectively. The comparator circuit (602) produces a comparison signal (cmp) in response to the comparison of the potential at node N6 to the reference voltage (Vref2). Vref2 is produced by the reference voltage circuit (VR2). The clock generation circuit (614) is arranged to produce a clock pulse signal (cpl) in response to the comparison signal (cmp) and the clock signal (clk) that is illustrated in FIG. 5.

Flip-flop circuits 606, 608, 610, and 612 are arranged to operate as a shift register. Signal rsb operates as a reset signal for the shift register during power-up. The reset signal (rsb) ensures that the shift register remains in a reset state until a voltage determined by capacitance circuit Cideal is reached. As the clock pulse signal (cpl) is applied to each flip-flop circuit (606, 608, 610, 612), a low logic level (logic “0”) is shifted to the left or to the right in the shift register. The left input port (il) of the first flip-flop circuit (606) is coupled to the supply signal (VDD) such that a logic “0” is shifted from the right to the left when the clock pulse signal (cpl) is applied to the shift register. The right input port (ir) of the last flip-flop circuit (612) is coupled to the ground terminal (GND) such that the logic “0” may be shifted back from the left to the right when the clock pulse signal (cpl) is applied to the shift register. The comparison signal (cmp) is applied to an input port (dr) of each flip-flop circuit (606, 608, 610, 612). The shifting direction (right or left) of the shift register is determined by the comparison signal.

The source voltage (Vdd) may decrease over time due to voltage drain. A voltage drain may occur when the power source is a battery cell or some other voltage storing device. For example, the source voltage (Vdd) may reach a potential (e.g., 3.9V) that indicates the source voltage (Vdd) is decreasing below its original potential (e.g., 4V). In the present embodiment, switch circuit S4 is closed when the source voltage (Vdd) has decreased slightly below its original potential. When the source voltage (Vdd) further decreases (e.g., to 3.2V), the potential at node N6 decreases. The comparator circuit (602) detects when the potential at node N6 decreases below reference voltage Vref2. The comparison signal (cmp) transitions to a low logic level when the potential at node N6 decreases to a potential less than reference voltage Vref2.

The shift register pushes a low logic level to the right in response to the low logic level of the comparison signal (cmp) in response to the clock pulse signal (cpl) (i.e., at the next rising edge). As previously stated, switch S4 is closed, therefore control signal sl<1> is a high logic level. Control signal rg<1> is the inverse of control signal sl<1> and is therefore a low logic level. Correspondingly, the potential at node N13 is a low logic level. Control signal rg<2> transitions to a low logic level in response to a right directional push of the low logic level at node N13 in the shift register. As stated previously, inverter circuits 640a–d inverting control signals rg<3:0> to produce control signals sl<3:0>. Control signal sl<2> is a high logic level and control signals sl<0>, sl<1>, and sl<2> are low logic levels in response to inverting signals rg<3:0>. Switch circuit S17 closes in response to sl<2> and switch circuits S16, S18, and S19 are open. In the present embodiment, a multiplication factor of 6 results when switch circuit S17 is closed. The multiplication factor compensates for the decrease in the source voltage as described above.

Further, XOR logic circuits 630a–c produce control signals slm<2:1> in response to control signals rg<3:2> and control signals rg<2:1> respectively. Signal slm<1> actuates switch circuit S3, while signal slm<2> actuates switch circuit S2. In the example provided, rg<0>, rg<1>, and rg<3> are low logic levels and rg<2> is a high logic level, resulting in slm<1> being a high logic level. Accordingly, switch circuit S3 is actuated, changing the potential at node N6 to correspond to the reference voltage (Vref2) given the change in the supply voltage (Vdd). Switch circuits S1–S4 may be actuated to regulate the potential at node N6 as the supply voltage (Vdd) decreases. The multiplier may be adjusted as the supply voltage (Vdd) changes when the potential at node N6 changes in response to the next decrease in the supply voltage.

Flip-flop circuit 624 produces an output (Q') in response to the feedback signal (fdb) and the inverse of the clock signal (clk). The clock signal (clk) is inverted by inverter 622. When the feedback signal (fdb) is at a high logic level, the Q' output is a low logic level. The Q' output is a high logic level when the feedback signal (fdb) is at a low logic level. The feedback signal (fdb) corresponds to the output voltage of the voltage converter-regulator circuit (500) shown in FIG. 5. For example, the feedback signal (fdb) is a low logic level (logic “0”) when the sense signal (sns1) is less than reference voltage Vref shown in FIG. 5. The Q' output of flip-flop circuit 624 is set to a high logic level at the next rising edge of the inverse of the clock signal (clk) in response to the low logic level of the feedback signal (fdb). Control signal fc is produced by AND logic circuit 626 in response to the Q' output and the clock signal (clk). The control signal (fc) actuates switch circuits S1–S7 shown in FIG. 5 as described above. Control signals sf<3:0> are produced by AND logic circuits 628a–c in response to signals rg<3:0> respectively and control signal fc. Control signals sf<3:0> actuate switches S8–S14 that are illustrated in FIG. 5 as described above.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

I claim:

1. An apparatus for providing an output signal from a supply signal that has an associated voltage level, the apparatus comprising:

- a control circuit that is configured to produce a control signal in response to the supply signal and a feedback signal that is associated with the output signal;
- a first multiplier circuit receiving the control signal to produce the output signal by multiplying the supply signal according to a first multiplication factor, wherein the first multiplication factor is adjusted to compensate for a change in the supply signal;
- a second multiplier circuit that is selectively coupled to the first multiplier circuit such that the first and second multiplier circuits produce the output signal in response to multiplying the supply signal by a second multiplication factor when the second multiplier circuit is coupled to the first multiplier circuit, wherein the second multiplication factor is greater than the first multiplication factor when the supply signal decreases below a predetermined level;
- the feedback circuit that is configured to provide a feedback signal in response to receiving the output signal, wherein the control circuit provides regulation of the output signal in response to the feedback signal.

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2. An apparatus as in claim 1, wherein the control circuit further comprises a logic circuit that is configured to produce the control signal in response to the supply signal and the feedback signal.

3. An apparatus as in claim 2, wherein the logic circuit further comprises a flip-flop circuit.

4. An apparatus as in claim 1, wherein the control circuit further comprises an oscillator circuit that is configured to produce a clock signal in response to the feedback signal, wherein the control signal is responsive to the clock signal.

5. An apparatus as in claim 1, wherein the control circuit further comprises an ADC/logic circuit that is configured to produce at least the control signal in response to the supply signal and the feedback signal.

6. An apparatus as in claim 1, wherein the first and second multiplier circuits further comprising a multiplicity of capacitance circuits, wherein the multiplicity of capacitance circuits are coupled to the supply signal during a first interval, and a selected group of the multiplicity of capacitance circuits are coupled in series with one another during a second interval such that the second multiplication factor is related to the selected group of the multiplicity of capacitance circuits.

7. An apparatus as in claim 1, the first multiplier circuit further comprising a multiplicity of capacitance circuits that are coupled to the supply signal during a first interval, and a selected group of the multiplicity of capacitance circuits that are coupled in series with one another during a second interval such that a second multiplication factor is related to the selected group of the multiplicity of capacitance circuits.

8. An apparatus as in claim 1, the feedback circuit further comprising:

a load circuit that is arranged to produce a sense signal in response to the output signal;

a voltage reference circuit that is arranged to produce a reference voltage; and

a comparator circuit that is configured to produce the feedback signal in response to a comparison between the reference voltage and the sense signal.

9. An apparatus as in claim 1, wherein the output signal is regulated to a predetermined level that is related to a reference signal by comparing at least a portion of the output signal to the reference signal.

10. A method for providing an output signal in response to a supply signal comprising:

multiplying the supply signal according to a multiplication factor to produce the output signal, wherein the multiplication factor is adjusted according to a predetermined number of capacitance circuits that are selectively coupled in series to produce the output signal, and wherein the multiplication factor corresponds to first and second multiplication factors;

measuring a sense signal that has a potential that is related to the output voltage;

comparing the sense signal to a reference signal;

regulating the output signal using a control circuit, wherein the output signal is regulated in response to the comparison of the sense signal to the reference signal; and

adjusting the first and second multiplication factors to compensate for a change in the supply signal such that the second multiplication factor is greater than the first multiplication factor when the supply signal decreases below a predetermined level.

11. A method as in claim 10, further comprising adjusting the multiplication factor according to the potential of the supply signal.

12. A method as in claim 10, wherein multiplying the supply signal further comprises coupling the predetermined number of capacitance circuits to the supply signal during a

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first interval and coupling the predetermined number of capacitance circuits in series during a second interval.

13. A method as in claim 12, further comprising coupling additional capacitance circuits to the supply signal during the first interval and coupling additional capacitance circuits in series with the predetermined number of capacitance circuits during the second interval to adjust the multiplication factor.

14. A method as in claim 10, further comprising adjusting the multiplication factor in response to the supply signal, wherein the multiplication factor is increased when the supply voltage decreases below a predetermined voltage level.

15. A method as in claim 14, the step of adjusting the multiplication factor further comprising coupling capacitance circuits in parallel to the supply signal such that the capacitance circuits are charged during a first interval, coupling a selected number of the capacitance circuits in series with one another during a second interval such that an output signal is provided by the selected number of capacitance circuits.

16. A method as in claim 15, the step of regulating the output signal further comprising adjusting at least one of the first and second intervals such that the output signal is maintained above a predetermined threshold level.

17. An apparatus for providing an output signal in response to a supply signal, comprising:

a means for multiplying that is arranged to multiply the supply signal according to a multiplication factor to produce the output signal, wherein the multiplication factor is adjusted according to a predetermined number of capacitance circuits selectively coupled in series to produce the output signal, and wherein the multiplication factor corresponds to first and second multiplication factors;

a means for measuring that is arranged to measure a sense signal that has a potential related to the output voltage;

a means for comparing that is arranged to compare the sense signal to a reference signal;

a means for regulating coupled to the means for multiplying to regulate the output signal using a control circuit, wherein the output signal is regulated in response to the comparison of the sense signal to reference signal; and

a means for adjusting that is arranged to adjust the first and second multiplication factors to compensate for a change in the supply signal such that the second multiplication factor is greater than the first multiplication factor when the supply signal decreases below a predetermined level.

18. An apparatus for providing an output signal from a supply signal that has an associated voltage level, the apparatus comprising:

a control circuit comprising an ADC/logic circuit that is configured to produce a control signal in response to the supply signal and a feedback signal that is associated with the output signal;

a first multiplier circuit receiving the control signal to produce the output signal by multiplying the supply signal according to a first multiplication factor, wherein the first multiplication factor is adjusted to compensate for a change in the supply signal; and

a feedback circuit that is configured to provide a feedback signal in response to receiving the output signal, wherein the control circuit provides regulation of the output signal in response to the feedback signal.



UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,717,458 B1  
DATED : April 6, 2004  
INVENTOR(S) : Vladislav Y. Potanin

Page 1 of 1

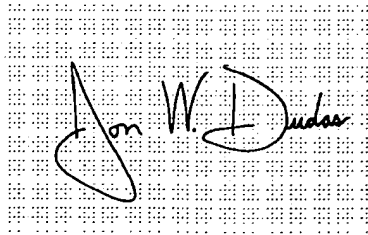
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,

Line 63, after "level;" please add -- and --.

Signed and Sealed this

Twenty-first Day of September, 2004



JON W. DUDAS  
*Director of the United States Patent and Trademark Office*





US006559689B1

(12) **United States Patent**  
**Clark**

(10) **Patent No.: US 6,559,689 B1**  
(45) **Date of Patent: May 6, 2003**

(54) **CIRCUIT PROVIDING A CONTROL VOLTAGE TO A SWITCH AND INCLUDING A CAPACITOR**

(75) **Inventor: Timothy A. Clark, Noblesville, IN (US)**

(73) **Assignee: Allegro Microsystems, Inc., Worcester, MA (US)**

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(52) **U.S. Cl. .... 327/97; 327/91; 327/390; 327/337**

(58) **Field of Search .... 327/91, 97, 94, 327/390, 589, 337**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,065,766 A	12/1977	Butler et al.
4,383,246 A	5/1983	Munt
4,703,407 A	10/1987	Fry et al.
4,853,563 A	8/1989	Hill et al.
4,873,408 A	10/1989	Smith et al.
4,940,906 A	7/1990	Gulczynski
4,965,578 A	10/1990	Poujois
5,172,019 A	12/1992	Naylor et al.
5,262,779 A	11/1993	Sauer
5,331,323 A	7/1994	Yamamoto
5,408,150 A	4/1995	Wilcox
5,442,218 A	8/1995	Seidel et al.
5,517,379 A	5/1996	Williams et al.
5,539,610 A	7/1996	Williams et al.
5,550,412 A	8/1996	Anneser
5,581,454 A	12/1996	Collins
5,598,118 A	1/1997	Koifman et al.
5,635,867 A	6/1997	Timm
5,666,035 A	9/1997	Basire et al.

5,691,870 A	11/1997	Gebara
5,726,594 A	3/1998	Williams
5,748,016 A	5/1998	Kurosawa
5,748,134 A	5/1998	Dent
5,790,063 A	8/1998	Koifman et al.
5,804,943 A	9/1998	Kollman et al.
5,905,404 A *	5/1999	Nagaraj ..... 327/390
5,933,034 A	8/1999	Hastings et al.
5,936,833 A	8/1999	Grossman et al.
5,943,227 A	8/1999	Bryson et al.
5,945,845 A	8/1999	Thomann et al.
5,945,872 A *	8/1999	Robertson et al. .... 327/390
5,949,271 A *	9/1999	Fujikura ..... 327/390
5,962,985 A	10/1999	Buij et al.
6,005,439 A *	12/1999	Fong ..... 330/253
6,052,000 A *	4/2000	Nagaraj ..... 327/91
6,072,355 A *	6/2000	Bledsoe ..... 327/390
6,118,326 A	9/2000	Singer et al. .... 327/390
6,215,329 B1 *	4/2001	Campardo et al. .... 327/390

\* cited by examiner

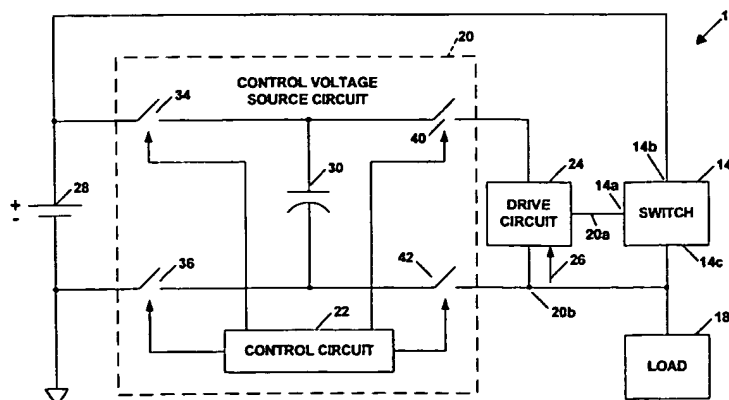
*Primary Examiner*—Terry D. Cunningham

(74) *Attorney, Agent, or Firm*—Daly, Crowley & Mofford, LLP

(57) **ABSTRACT**

A circuit for providing a control voltage to a switch includes a capacitor, a first pair of switches for coupling the capacitor to an input voltage source and a second pair of switches for coupling the capacitor to the switch. The first pair of switches is controlled by a control signal in response to the voltage across the capacitor in order to prevent overcharging the capacitor beyond a first predetermined level. The second pair of switches is controlled by a second control signal in response to the voltage across the switch in order to replenish the capacitor voltage when the capacitor voltage falls to a second predetermined level. The first and second pairs of switches are closed during non-overlapping time intervals in order to isolate the switch from the input voltage source, thereby preventing switching transients from affecting the input voltage source and permitting the circuit to be used to drive a variety of switch types arranged in a variety of configurations.

14 Claims, 9 Drawing Sheets



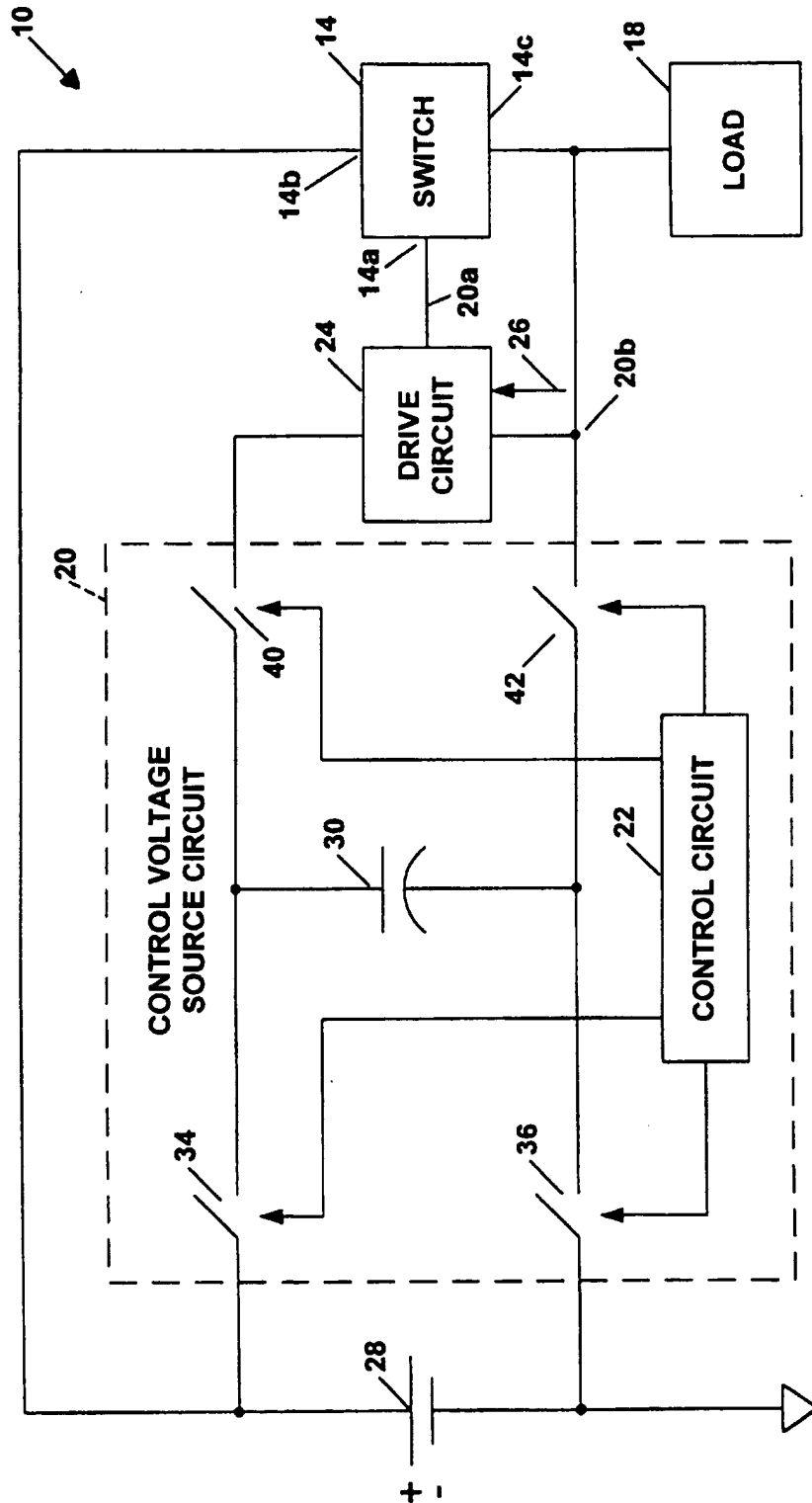
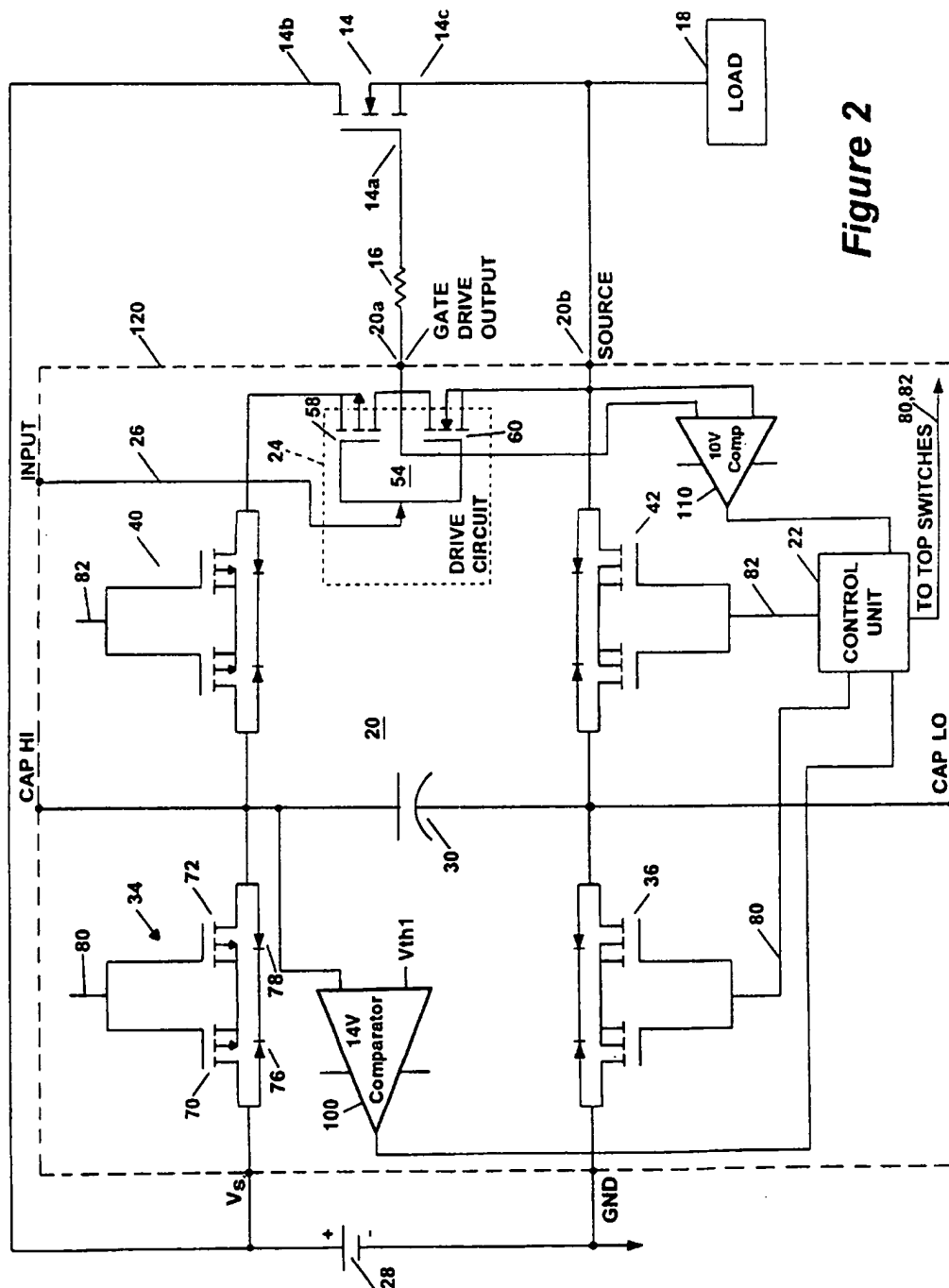
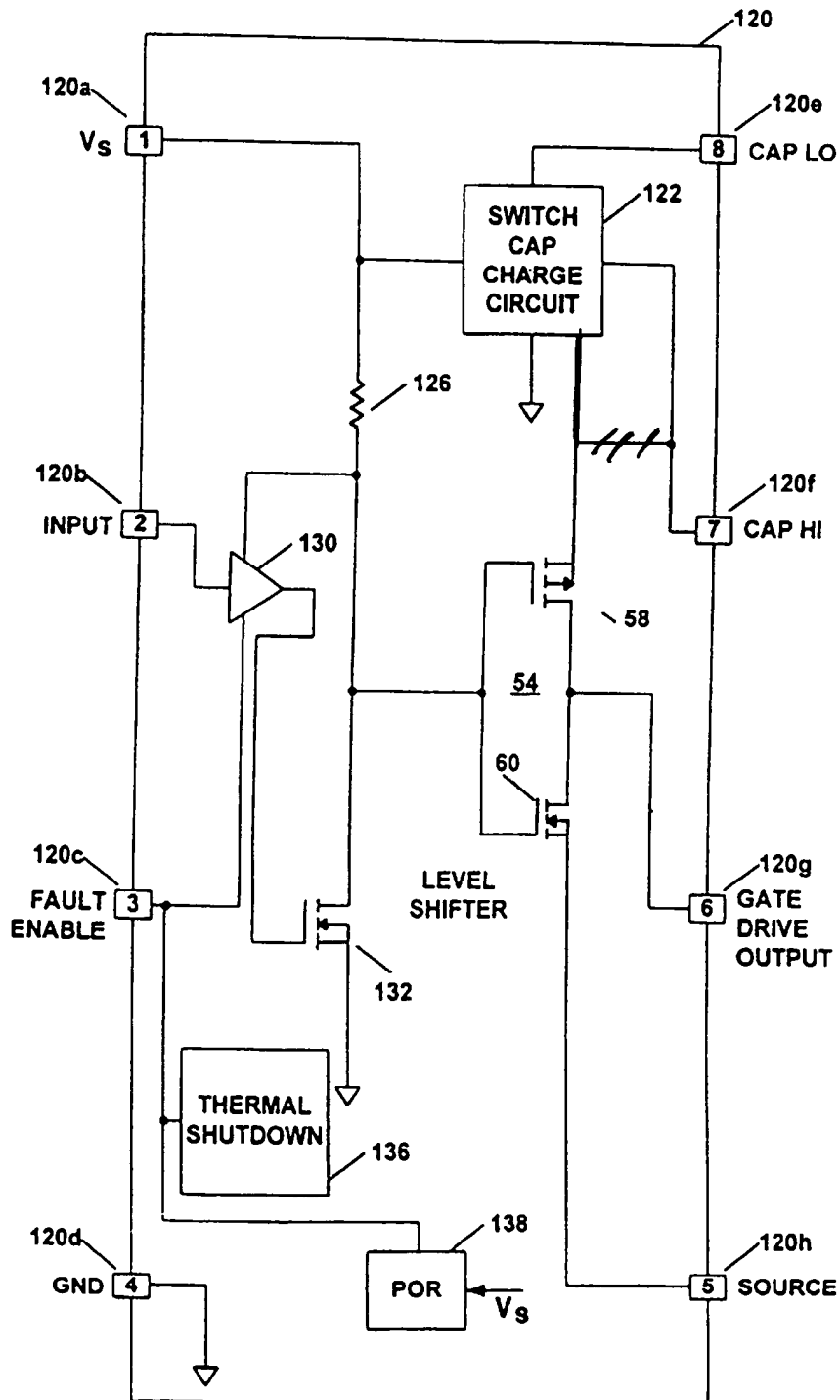


Figure 1



## Figure 2



### Figure 3

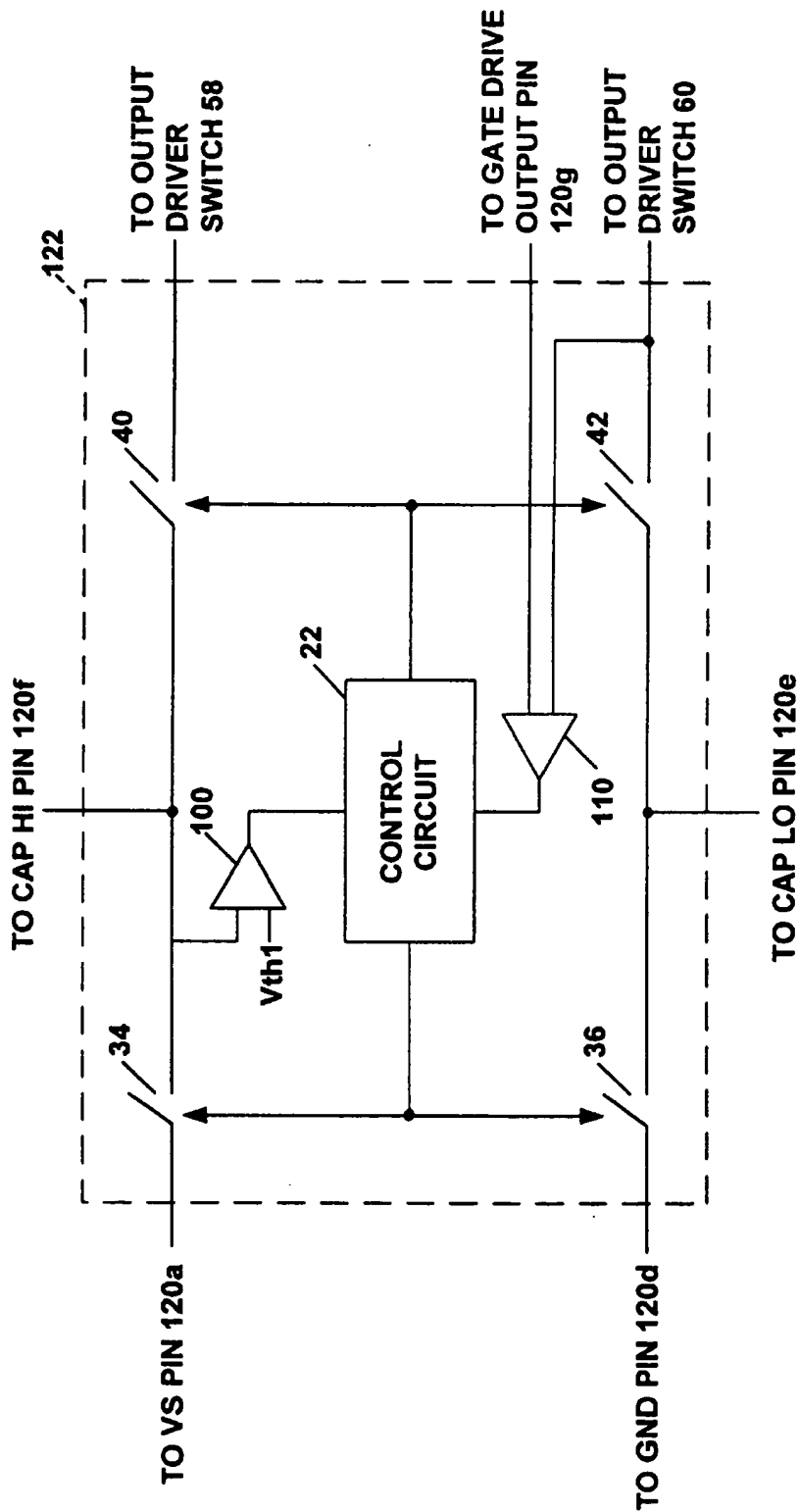


Figure 3A

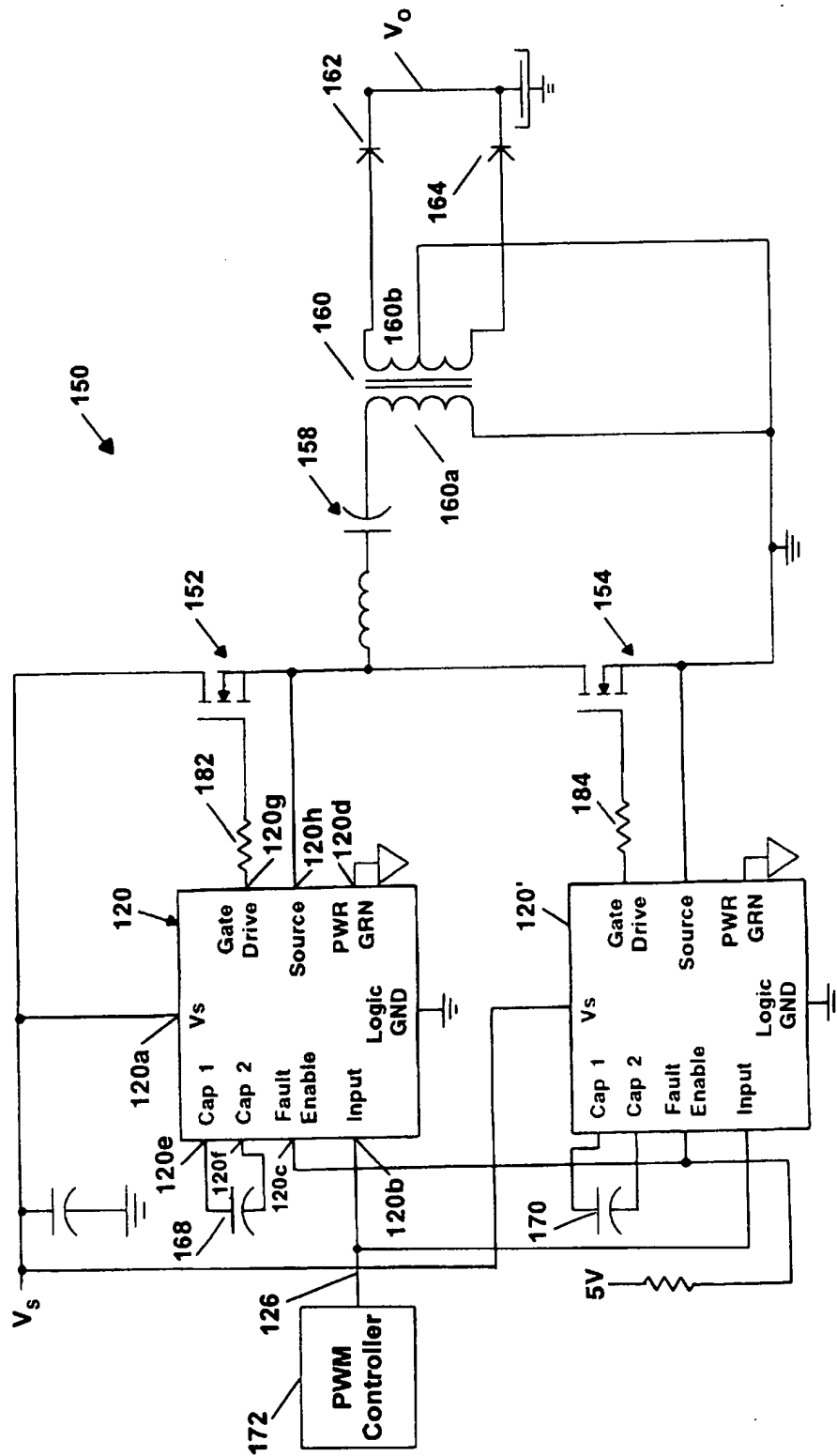
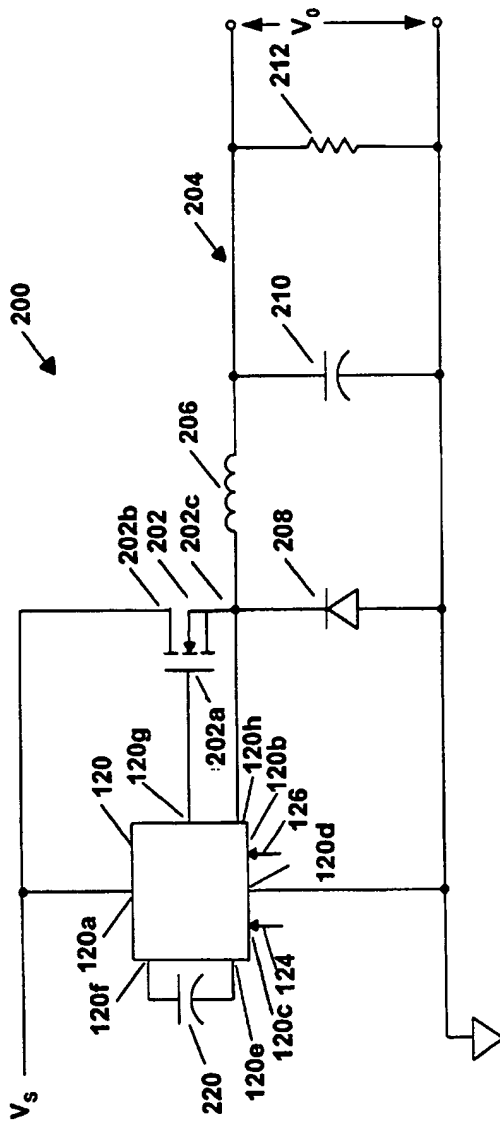
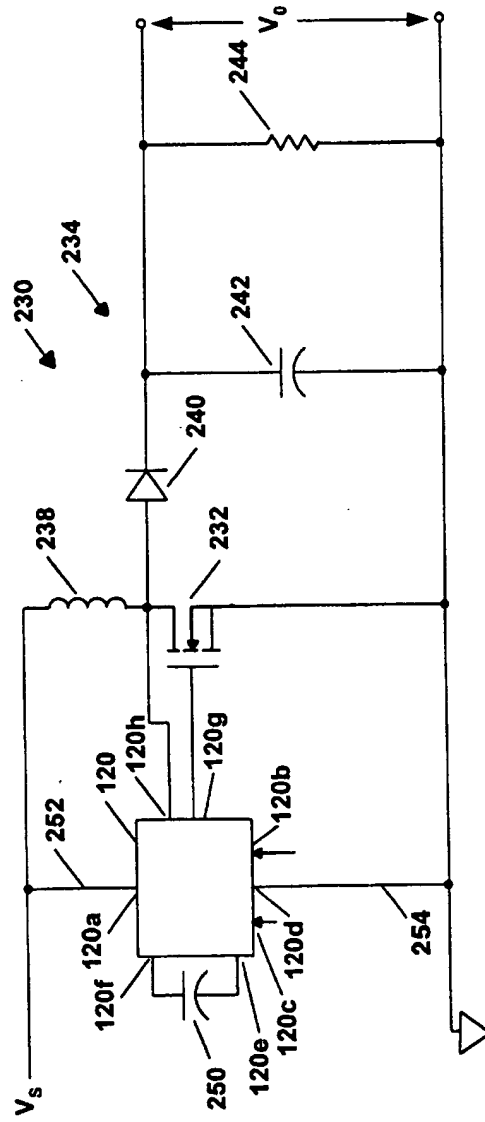


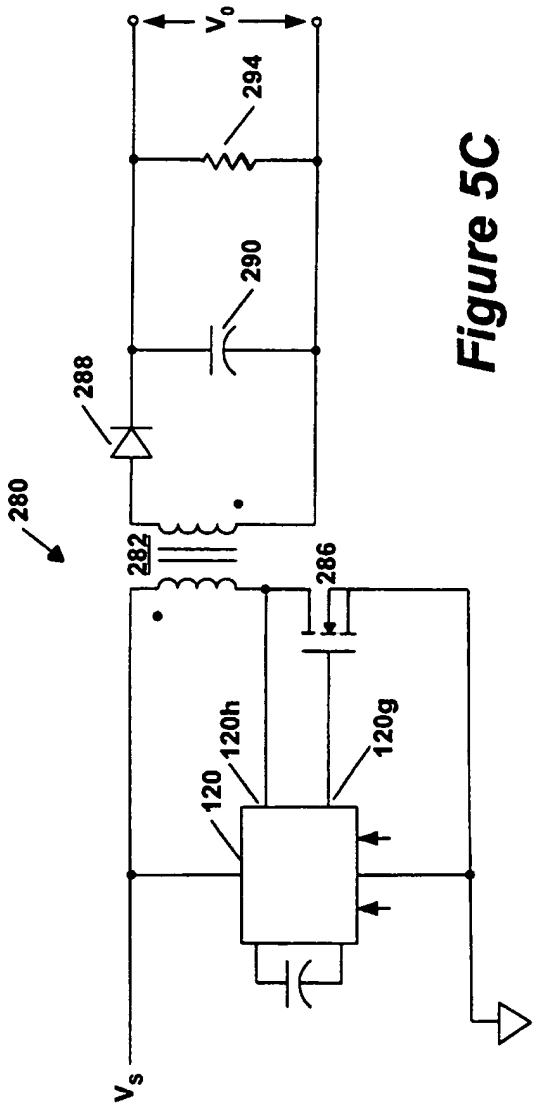
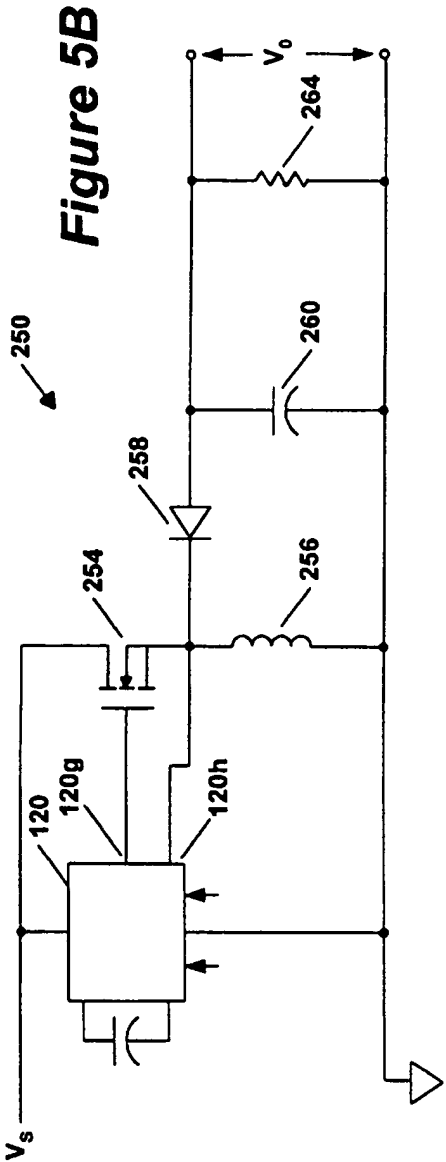
Figure 4

## Figure 5



**Figure 5A**







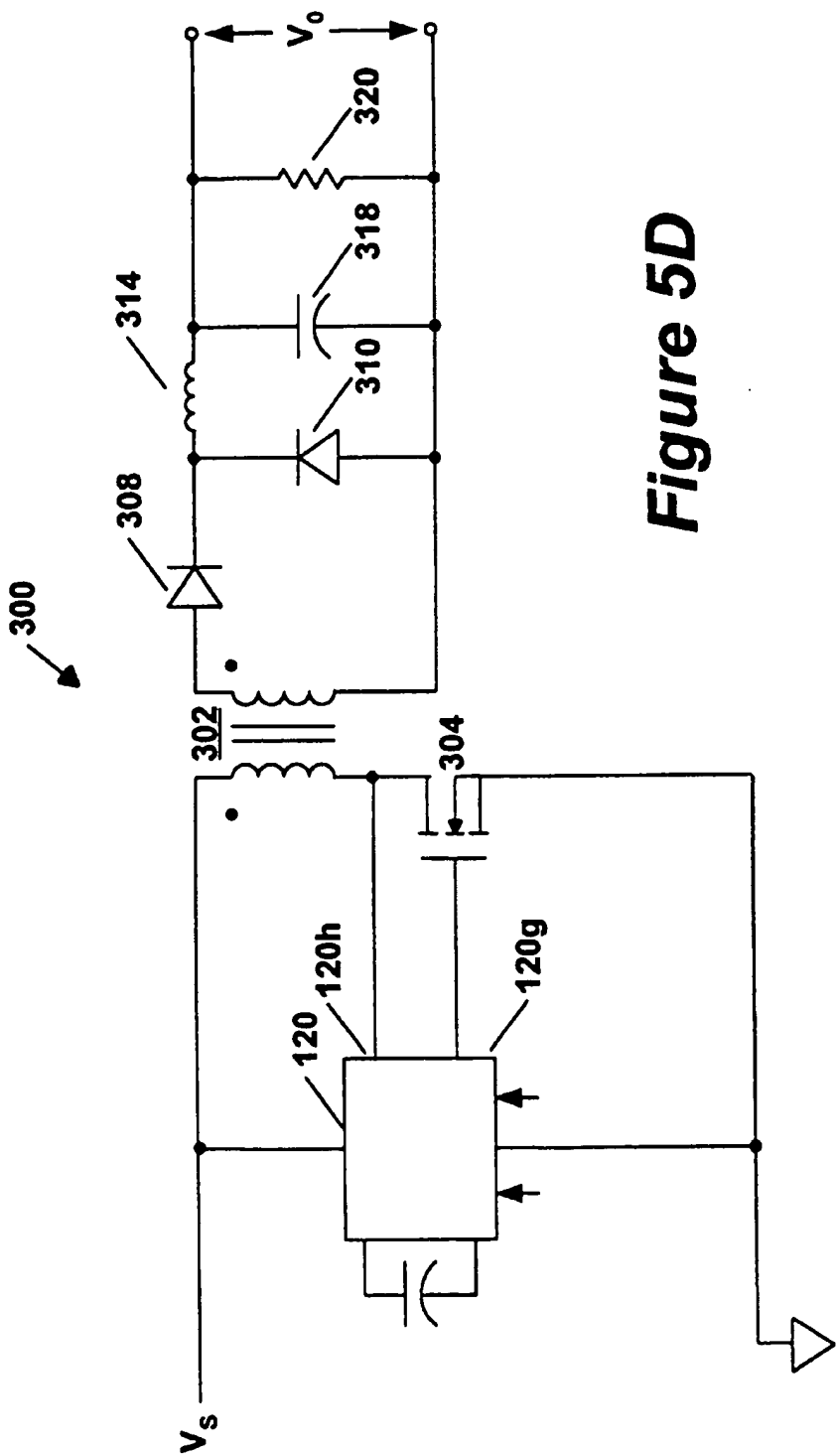


Figure 5D

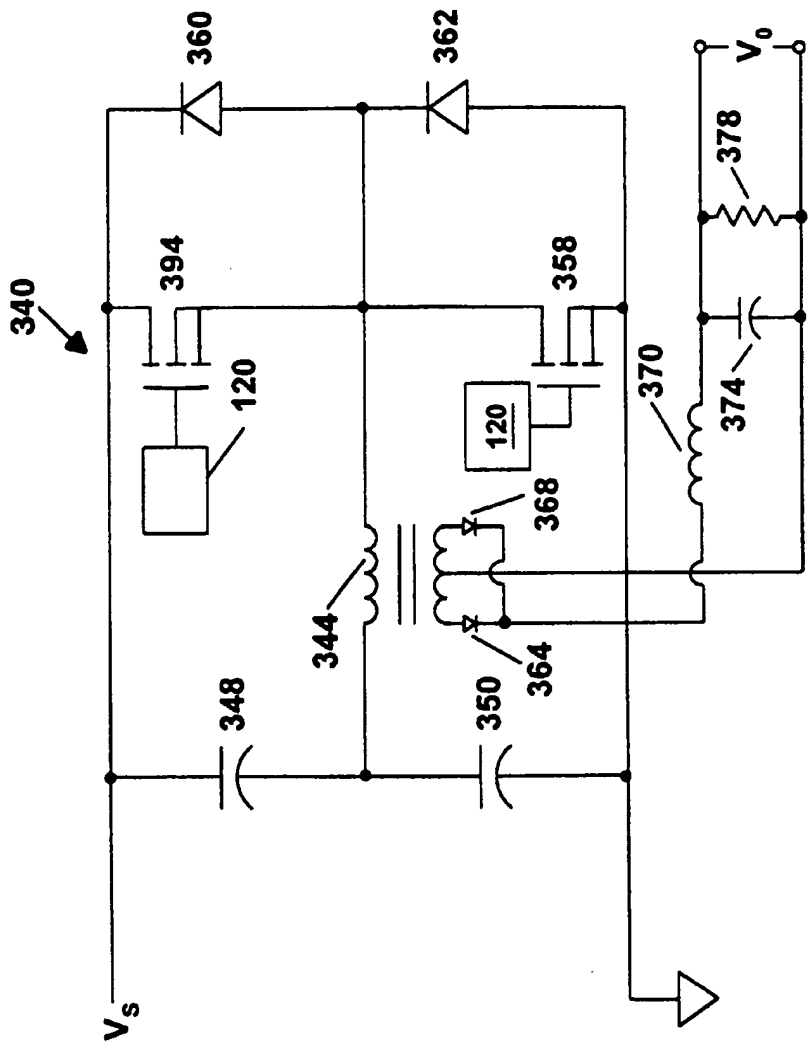


Figure 5E

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# **CIRCUIT PROVIDING A CONTROL VOLTAGE TO A SWITCH AND INCLUDING A CAPACITOR**

## **CROSS-REFERENCE TO RELATED APPLICATIONS**

Not applicable.

## **STATEMENT REGARDING FEDERALLY FUNDED RESEARCH**

Not applicable.

## **BACKGROUND OF THE INVENTION**

Transistors are commonly used as the switching device in circuits supplying a load which requires a switching source, such as power supplies, motor drivers, amplifiers, etc. Such circuits may utilize one or more transistors of various types, such as Metal Oxide Field Effect Transistors (MOSFETs, or simply FETs) or Insulated Gate Bipolar Transistors (IGBTs), arranged in various topologies. The voltage across the transistor may be fixed or unknown, depending on the particular topology.

The control voltage necessary to drive a particular switch is a function of the switch type and topology. For example, the control, or gate voltage necessary to drive a high current, power FET must present a predetermined differential voltage across the gate and source terminals of the FET, such as on the order of 10 volts. More particularly, in an N-channel FET, the gate voltage must be brought to approximately 10 volts higher than the source voltage and in a P-channel FET, the gate voltage must be brought to approximately 10 volts lower than the source voltage. The absolute value of the control voltage may be as low as 10 volts in the case of driving a "low side" FET in which the source terminal is coupled to ground or may be an unknown voltage in the case of driving a "high side" FET or floating low side FET in which the source terminal is at an unknown voltage.

Various circuits are used to provide switch control voltage. One such circuit is referred to as a "bootstrap" circuit and is most commonly used to drive FETs in applications in which the source voltage is unknown. The voltage across a bootstrap capacitor coupled between an input voltage source and the source terminal of the FET rises as the source voltage rises and thus, provides a voltage which is at a predetermined level higher than the source voltage. However, since the bootstrap circuit does not provide any isolation between the bootstrap voltage and the input voltage source, current and voltage transients caused by the switching FET can affect the input voltage source.

A charge pump, which generates an output voltage in response to a lower input voltage, is sometimes used to provide the necessary FET gate drive voltage. However, like the bootstrap circuit, the charge pump does not provide any isolation between the input voltage source and the power switch.

Pulse transformers can be used to provide isolation between the input voltage source and the power switch, in order to prevent transients from affecting the input voltage source. However, pulse transformers can be expensive and bulky.

## **SUMMARY OF THE INVENTION**

It is an object of the present invention to provide a circuit for generating a control voltage for switches arranged in various configurations.

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It is a further object to provide a circuit for generating a switch control voltage which provides isolation between an input voltage source and the switch without the use of a transformer.

These and other objects of the invention are achieved with a circuit including a capacitor, a first pair of switches adapted to couple the capacitor to an input voltage source during a first time interval, and a second pair of switches adapted to couple the capacitor to a control terminal of a switch during a second time interval which is nonoverlapping with respect to the first time interval. The voltage across the capacitor provides a predetermined differential voltage which is independent of the input voltage or any other fixed voltage.

With this arrangement, the circuit can be used to provide drive switches arranged in various configurations, including high side switches and floating low side switches, in which cases a terminal of the switch is at an unknown, or floating voltage. Also, the above-described circuit provides isolation between the input voltage source and the switch, thereby advantageously preventing current and voltage transients from affecting the input voltage source.

A control circuit provides a first control signal to each of the first pair of switches in response to the voltage across the capacitor and a second control signal to each of the second pair of switches in response to the voltage across the switch. In one embodiment, a first comparator has a first input terminal coupled to the capacitor, a second input terminal coupled to a threshold voltage, and an output terminal at which an output signal is provided to the control circuit. The output signal is indicative of whether or not the voltage across the capacitor is greater than a predetermined level and the first control signal causes the first pair of switches to open when the voltage across the capacitor is greater than the predetermined level. In this way, the first pair of switches is opened to prevent the capacitor from charging to a voltage that is too high to safely drive the switch.

A second comparator has a first input terminal coupled to the control terminal of the switch, a second input terminal coupled to the reference terminal of the switch, and an output terminal coupled to the control circuit at which an output signal is provided. The output signal of the second comparator is indicative of whether or not the voltage across the switch is less than a predetermined level and the second control signal provided by the control circuit causes the second pair of switches to open when the voltage across the control and reference terminals of the switch is less than the predetermined level. In this way, charge on the capacitor is replenished to keep the capacitor voltage above a minimum level necessary to fully enhance the switch.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following description of the drawings in which:

FIG. 1 is a block diagram of a circuit including a control voltage circuit for generating a control voltage for a switch according to the invention;

FIG. 2 is a more detailed block diagram of the circuit of FIG. 1;

FIG. 3 is a block diagram of an illustrative integrated circuit incorporating the control voltage circuit of FIG. 2;

FIG. 3A is a schematic of the switch capacitor charge circuit of FIG. 3;

FIG. 4 is a schematic of an illustrative resonant converter utilizing four integrated circuits of the type shown in FIG. 3;

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FIG. 5 is a schematic of a Buck converter utilizing the circuit of FIG. 3;

FIG. 5A is a schematic of a boost converter utilizing the circuit of FIG. 3;

FIG. 5B is a schematic of a Buck-boost converter utilizing the circuit of FIG. 3;

FIG. 5C is a schematic of a flyback converter utilizing the circuit of FIG. 3;

FIG. 5D is a schematic of a forward converter utilizing the circuit of FIG. 3; and

FIG. 5E is a schematic of a half-bridge converter utilizing the circuit of FIG. 3.

#### DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1, a circuit 10 includes a switch 14 having a control terminal 14a, an input terminal 14b, and a reference terminal 14c, a load 18 coupled to the switch, an input voltage source 28, and a control voltage circuit 20 for generating a control voltage for the switch. The control voltage generated by the circuit 20 is coupled to a drive circuit 24 which provides the necessary current to turn the switch 14 on and off.

The switch 14 and load 18 may take various forms for various applications. As examples, the switch 14 may be a power transistor, such as a FET or IGBT, and the load 18 may be the output section of a power supply or a motor. In the illustrative embodiment, the circuit 10 is a switch-mode power supply used in automotive applications and the input voltage source 28 is provided by a battery providing a voltage between 14 and 42 volts DC.

The control voltage circuit 20 of the present invention is suitable for driving switches arranged in various topologies, as will be described below in conjunction with FIGS. 4 and 5-5E. As examples, the control voltage circuit may be used to drive switches of a resonant converter as shown in FIG. 4, a Buck converter as shown in FIG. 5, a boost converter as shown in FIG. 5A, a Buck-boost converter as shown in FIG. 5B, a flyback converter as shown in FIG. 5C, or a forward converter as shown in FIG. 5D. Further, more than one control voltage circuit 20 may be used in a given application to drive respective switches, as in the case of the resonant converter of FIG. 4 and the half-bridge circuit of FIG. 5E. Thus, the control voltage circuit 20 can be considered "universal" in its suitability for driving switches arranged various topologies.

The controlled switch 14 may be a "high side" switch or a "low side" switch. A high side switch is one in which a terminal of the switch is coupled to the positive terminal of a voltage source. For example, switch 14 shown in FIG. 1 is a high side switch since its input terminal 14b is coupled to the positive terminal of the input voltage source 28. A low side switch is one in which a terminal of the switch is coupled to the negative terminal of a voltage source. For example, switch 286 of the flyback circuit 280 of FIG. 5C is a low side switch since its source terminal is coupled to the negative terminal of the input voltage source 28. When providing a control voltage to a high side switch, a predetermined voltage is required across the control and reference terminals; whereas, when providing a control voltage to a low side switch, a predetermined voltage is required across the input and control terminals.

In the illustrative embodiment of FIG. 1, the switch 14 is a power FET and, more particularly, is a N-type FET. Thus, the control terminal 14a of the switch is a gate terminal, the

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input terminal 14b is a drain terminal, the reference terminal 14c is a source terminal, and the gate terminal 14a must be brought to at least a predetermined voltage above the reference terminal 14c in order to turn on the switch. Alternatively however, the switch may be an P-type FET, in which case the gate terminal 14a must be brought to at least a predetermined voltage below the reference terminal 14c in order to turn on the switch. In applications in which the switch 14 is a FET, the control voltage circuit 20 may be referred to as a gate drive voltage circuit and the drive circuit 24 may be referred to as a gate drive circuit.

The control voltage source circuit 20 includes a capacitor 30, a first pair of switches 34, 36 adapted to couple the capacitor to the input voltage source 28 during a first time interval, and a second pair of switches 40, 42 adapted to couple the capacitor to the drive circuit 24 during a second time interval which is non-overlapping with respect to the first time interval. With this arrangement, the control voltage circuit 20 provides a voltage to the gate drive circuit 24 which is isolated from the input voltage source 28. Thus, current and voltage transients caused by the switching action of the switch 14 are prevented from affecting the input voltage source 28.

A control circuit 22 provides control signals to the switches 34, 36, 40, and 42 to open and close the switches, as will be discussed. In general, the first pair of switches 34, 36 is opened to de-couple the capacitor 30 from the input voltage source 28 when the voltage across the capacitor exceeds a predetermined level and the second pair of switches 40, 42 is opened to de-couple the capacitor from the drive circuit 24 when the voltage across the control and reference terminals 14a, 14c of the switch 14 falls below a second predetermined level. In this way, charge on the capacitor is replenished when the capacitor voltage falls below the second predetermined level in order to ensure full enhancement of the switch and the voltage applied to the switch is limited to the first predetermined level in order to prevent exceeding the Vgs rating of the switch.

Referring also to FIG. 2, a more detailed schematic of the circuit 10 of FIG. 1 is shown to include the switch 14, the input voltage source 28, the load 18, the drive circuit 24, and the control voltage source circuit 20. The drive circuit 24 includes an output driver 54 responsive to a control signal 26. The control signal 26 is provided by a controller 50 (not shown) which may take various forms, such as a conventional pulse-width modulation (PWM) controller. The control signal 26 is indicative of the output current or voltage of the load 18 and causes the duty cycle of the switch 14 to be adjusted so as to maintain the desired output current or voltage. The illustrative output driver 54 includes a pair of series-coupled FETs 58, 60 capable of providing the necessary source current to drive the gate terminal 14a of the FET 14, respectively, through a resistor 16. The resistor 16 is selected to control the slew rate of the FET 14.

Each of the switches 34, 36, 40, and 42 of the control voltage source circuit 20 may be implemented in various ways. In the illustrative embodiment, each such switch is comprised of a pair of series-coupled, commonly controlled FETs. Illustrative switch 34, for example, includes PMOS FET 70 coupled in series with PMOS FET 72. Each of the FETs 70, 72 has an intrinsic diode 76, 78, respectively, coupled as shown. The gate terminals of the FETs 70, 72 are responsive to a control signal 80 provided by the control circuit 22. Switches 36, 40, and 42 have like FETs 70, 72 with intrinsic diodes 76, 78, as shown. Each of the switches 34, 36 is responsive to a control signal 80 and each of the switches 40, 42 is responsive to a control signal 82, as shown.

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Alternatively, the switches 34 and 40 may be implemented with diodes and the switches 36, 42 with the illustrated series-coupled FETs. More particularly, switch 34 may be replaced by a diode having an anode coupled to the positive terminal of the input voltage source 28 and a cathode coupled to the positive terminal of the capacitor 30. Switch 40 may be replaced by a diode having an anode coupled to the positive terminal of the capacitor and a cathode coupled to the drive circuit 24.

The control circuit 22 is responsive to an output signal from a comparator 100 for providing the control signal 80 to switches 34 and 36 in order to open the switches 34, 36 and de-couple the capacitor 30 from the input voltage source 28 when the voltage across the capacitor exceeds a predetermined threshold level. The predetermined threshold level is set by the threshold voltage  $V_{th1}$  applied to an input terminal of the comparator 100. Thus, the comparator 100 has a first input terminal coupled to the capacitor 30, a second input terminal responsive to the threshold voltage  $V_{th1}$ , and an output terminal at which an output signal is provided to the control circuit 22. The output signal of the comparator is indicative of whether the voltage across the capacitor 30 is greater or less than the threshold voltage. In the illustrative embodiment, the threshold voltage  $V_{th1}$  is set to approximately 14 volts. With this arrangement, the capacitor 30 is prevented from charging to a voltage greater than approximately 14 volts. The threshold voltage is selected in order to protect the gate to source junction of the switch 14 by preventing application of a voltage of greater than the  $V_{gs}$  rating of the switch.

The control circuit 22 is further responsive to an output signal from a second comparator 110 for providing the control signal 82 to switches 40 and 42 in order to open the switches and de-couple the capacitor 30 from the gate and source terminals of the switch 14, via the drive circuit 24, when the voltage across the switch falls below a second predetermined threshold level  $V_{th2}$ . The comparator 110 has a first input terminal coupled to the gate terminal 14a of the switch 14, a second input terminal coupled to the source terminal 14c of the switch 14, and an output terminal at which an output signal is provided to the control circuit 22. The output signal of the comparator 110 is indicative of whether the voltage across the gate and source terminals of the switch is less than the second threshold voltage  $V_{th2}$ . The comparator 110 could be provided as a differential amplifier and comparator combination. In the illustrative embodiment, the threshold voltage  $V_{th2}$  is set to approximately 10 volts. With this arrangement, the drive circuit 24 and thus the gate and source terminals of the switch 14 are supplied with a predetermined minimum voltage necessary to fully enhance the switch 14.

The switching frequency of the switch 14 is a function of the particular components and application. Switches 34, 36, 40 and 42 may be operated synchronously or asynchronously with respect to the switch 14.

As noted above, the control signal 80 coupled to the first pair of switches 34, 36 and the control signal 82 coupled to the second pair of switches 40, 42 are non-overlapping. With this arrangement, the input voltage source 28 is isolated from the switch 14, thereby preventing switching transients from affecting the input voltage source. Further, it is because of this isolation that the circuit 20 is able to supply the necessary control voltage to switches arranged in various topologies. That is, since the supplied voltage is not referenced to any particular potential, it can be used to provide a control voltage to a high side switch or to a floating low side switch.

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There is a fixed time interval between opening the first pair of switches 34, 36 and closing the second pair of switches 40, 42. Likewise, there is a fixed time interval between opening the second pair of switches 40, 42 and closing the first pair of switches 34, 36. The manner in which the fixed dead times are selected as well as the relationship between the dead times and the charging and discharging rates of the capacitor depends upon the particular application. The flying capacitor value must be several times the gate capacity of the FET that flying capacitor drives. Ten times is a typical ratio, however other ratios may also be used.

Much of the control voltage circuit 20 may be incorporated into a monolithic integrated circuit. As one example, the components contained within the dotted line boundary 120 in FIG. 2 with the exception of the capacitor 30 may be provided on an integrated circuit, as will be described further in conjunction with FIG. 3. Of course, it will be appreciated by those of ordinary skill in the art that many variations to the integrated circuit 120 are possible, including which components are integrated and the connections that are provided at externally accessible pins.

Referring also to FIG. 3, one embodiment of a portion of an integrated circuit 120 to be used in a complete switch control voltage circuit is shown. For example, it should be appreciated that neither the connection to the pin 120h associated with the driver circuit 54 (FIG. 2) nor the connection to the gate drive output pin 120g (FIG. 3A) is explicitly shown in FIG. 3. Given the description provided herein, however, one of ordinary skill in the art would understand how to make such connections.

Integrated circuit 120 includes a  $V_s$  pin 120a coupled to a switch capacitor charge circuit 122 which is shown in FIG. 3A to include the first pair of switches 34, 36, the second pair of switches 40, 42, the comparators 100, 110 and control circuit 22. The  $V_s$  pin is further coupled to a resistor 126, as shown. External to the integrated circuit 120, the  $V_s$  pin is adapted for coupling to the positive terminal of the input voltage source 28 (FIG. 2). The resistor 126 couples power to an internal buffer 130 and to the interconnected gate terminals of the output driver switches 58 and 60, as shown.

An INPUT pin 120b to the integrated circuit 120 is adapted for coupling to an external controller which produces a feedback, or control signal, such as a PWM signal 26 (FIG. 2). The PWM signal is internally coupled to the buffer 130 having an output coupled to a level shifting transistor 132, as shown. The buffer 130 can be disabled in response to a logic low fault signal coupled to a FAULT/ENABLE pin 120c. Various fault conditions may be monitored external to the integrated circuit 120 and used to provide the fault signal to the FAULT/ENABLE pin. Alternatively or additionally, fault conditions may be monitored on the chip 120, for example with a thermal shutdown circuit 136 and/or with a power on/reset (POR) circuit 138. The POR circuit holds the chip output off until power to the chip is within a predetermined range. In operation, either a power on/reset, over temperature, or other fault indicating condition disables the buffer 130 thereby disabling the GATE DRIVE OUTPUT pin 120g of the chip. This is achieved by pulling the output signal of the buffer 130 low to turn off the level shifting transistor 132 and the output driver 54. When no fault or disable conditions exist, the output of the buffer 130 controls the output driver 54 through transistor 132.

A CAP LO pin 120e of the chip is adapted for coupling to the positive terminal of the external capacitor 30 (FIG. 2) and a CAP HI pin 120f is adapted for coupling to the

negative terminal of the capacitor 30. The voltage provided by the circuit 20 at terminals 20a and 20b (FIG. 1) is provided across the GATE DRIVE OUTPUT pin 120g and the SOURCE pin 120h of the chip 120.

Referring to FIG. 4, a resonant converter 150 is shown to include two integrated circuits 120 of the type shown in FIG. 3. The resonant converter 150 includes power transistors 152 and 154 coupled in series, with the interconnection between the power transistors coupled to the resonating capacitor 158 and transformer primary winding 160a, as shown. The transformer secondary 160b is coupled to synchronous rectifiers 162 and 164 having interconnected terminals at which the output voltage  $V_o$  of the converter 150 is provided. Each of the resonant switches 152 and 154 is controlled by an integrated circuit 120 of the type shown in FIG. 3. The illustrative resonant converter 150 is a 500 Watt, DC-DC converter having an input voltage  $V_s$  on the order of 42 volts and providing an output voltage  $V_o$  on the order of 12 volts with a switching frequency on the order of 500 KHz.

More particularly, each of the power switches 152 and 154 is controlled by an integrated circuit 120, 120', respectively, which is responsive to an input voltage source  $V_s$ , as shown. An input signal 126 provided by a pulse width modulator controller 172 is coupled to an INPUT pin 120b of the integrated circuits 120 and 120', as shown. The gate drive signal provided at pin 120g of integrated circuits 120 and 120' is coupled to the gate terminal of the respective power switch 152 and 154 through resistors 182 and 184, respectively, as shown.

In the illustrative resonant converter 150, both integrated circuits 120, and 120' (referred to collectively as integrated circuits 120) have interconnected FAULT/ENABLE pins 120c. With this arrangement, a fault condition detected by any of the integrated circuits 120 causes all of the integrated circuits 120 and thus, the entire circuit 150, to shut down.

In operation, power switches 152 and 154 operate asynchronously to generate the output voltage  $V_o$ . More particularly, during a first half cycle, power switch 152 is closed causing charge to be transferred directly through the transformer 160 to the converter output  $V_o$ ; whereas, during a second half cycle, the charge stored in the capacitor 158 and transformer winding 160a is transferred to the secondary 160b and also back through the primary 160a via conducting power switch 154.

As is apparent from consideration of the resonant converter 150 of FIG. 4, the control voltage circuit implemented by integrated circuits 120 is capable of generating an isolated control voltage for driving a high side switch 152, a low side switch 154, and output switches 162 and 164, as shown.

Referring also to FIG. 5, a Buck, or step-down converter 200 is shown to include a power transistor 202 and a load 204. The Buck converter 200 converts an input voltage  $V_s$  to a lower output voltage  $V_o$ . The load 204 includes an inductor 206, a diode 208, a capacitor 210, and a resistor 212 across which the output voltage  $V_o$  is provided.

An integrated circuit 120 of the type shown in FIG. 3 supplies the necessary gate drive signal to the power transistor 202. To this end, the circuit 120 has a  $V_s$  pin 120a coupled to the positive terminal of the input voltage source  $V_s$ , a GND pin 120d coupled to the negative terminal of the input voltage source, a CAP HI pin 120f for coupling to the positive terminal of an external capacitor 220 and a CAP LO pin 120e for coupling to the negative terminal of the external capacitor 220, as shown. A FAULT/ENABLE pin 120c is provided for receiving an external fault/enable signal 124

and the INPUT pin 120b is responsive to a feedback signal 126, such as from a PWM controller (not shown). The gate drive signal is coupled to the gate terminal 202a and source terminal 202c of the switch 202 via a GATE DRIVE OUTPUT pin 120g and a SOURCE pin 120h, respectively, as shown.

In operation, when the transistor 202 conducts, energy is transferred directly from the input voltage source  $V_s$  through the transistor 202 and inductor 206, to the output capacitor and resistor 220, 212, respectively. During non-conduction of the switch 202, current flows through the diode 208 and is thereby transferred from the inductor 206 to the output capacitor 210 and resistor 212. The conduction time intervals of the switch 202 are governed by the PWM control signal 126.

The transistor 202 is a high side transistor. Thus, the voltage at its source terminal 202c varies between the input voltage of  $V_s$  to near ground. The circuit 120 provides a predetermined voltage differential between the gate terminal 202a and the source terminal 202c which is isolated from any known or reference potential, such as ground.

FIG. 5A shows the integrated circuit 120 used in a boost converter 230. The boost converter 230 includes a low side switch 232. In this application, the circuit 120 provides the gate drive signal via pin 120g to the gate terminal of low side switch 232 and the SOURCE pin 120h of circuit 120 is coupled to the drain terminal of the low side switch, as shown, since it is the drain terminal of the switch 232 which "floats."

In operation, when the switch 232 does not conduct, energy is transferred through the inductor 238 and diode 240 to the output capacitor 242. During intervals of conduction of the switch 232, the charge on the output capacitor 242 supplies the converter output voltage  $V_o$ .

FIG. 5B shows the circuit 120 in use in a Buck-boost converter 250 having a power switch 254 responsive to a gate drive signal provided at pin 120g of the circuit 120. The SOURCE pin 120h of circuit 120 is connected to the source terminal of the high-side NMOS switch 254. Thus, similar to the converter of FIG. 1, in the Buck-boost converter of FIG. 5B, the circuit 120 controls a high-side switch having a floating source terminal.

In operation, charge is transferred to the inductor 256 during intervals of conduction of the power switch 254 and is transferred from the inductor 256 to the output capacitor 260 during intervals of non-conduction of the primary switch 254.

Referring also to FIG. 5C, the integrated circuit 120 is in use in a flyback converter 280 in which the gate drive signal provided at pin 120g of the chip 120 is coupled to the gate terminal of power switch 286 and the SOURCE pin 120h of the circuit 120 is coupled to the drain terminal of the power switch 286, as shown, since it is the drain terminal of the power switch which "floats."

In operation, charge is transferred from the primary winding of the transformer 282 to the output capacitor 290 during intervals of conduction of the power switch 286 and is transferred from the storage capacitor 290 to the output  $V_o$  during intervals of non-conduction of the primary switch.

Further examples of applications for the switch control voltage circuit of the present invention are shown in FIGS. 5D and 5E. In particular, FIG. 5D shows the circuit 120 in use in a forward converter 300 in which the primary switch 304 is an NMOS switch receiving a gate drive signal from pin 120g of the chip 120 and having the SOURCE pin 120h of the chip 120 coupled to the floating drain terminal of the

power switch 304. FIG. 5E shows two integrated circuits 120 in use in a half-bridge converter. Each of the circuits 120 provides a gate drive signal to a respective switch 354, 358 in order to implement asynchronous operation of the switches.

It will be appreciated by those of ordinary skill in the art that the converter topologies shown in FIGS. 4 and 5-5E are illustrative only and that the switch control voltage circuit 20 of FIG. 1 alone, or in an integrated circuit implementation 120 (FIG. 3), may be used in a variety of circuit topologies beyond those shown herein.

Having described the preferred embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may be used.

It is felt therefore that these embodiments should not be limited to disclosed embodiments but rather should be limited only by the spirit and scope of the appended claims. All publications and references cited herein are expressly incorporated herein by reference in their entirety.

What is claimed is:

1. A circuit for generating a control voltage across a pair of output terminals for controlling a switch having an input terminal, a reference terminal, and a control terminal, said circuit comprising:

a capacitor;

a first pair of switches adapted to couple said capacitor to an input voltage source during a first time interval;

a second pair of switches adapted to couple said capacitor to said pair of output terminals during a second time interval, non-overlapping with respect to said first time interval; and

a control circuit providing a first control signal to said first pair of switches in response to the voltage across said capacitor and providing a second control signal to said second pair of switches.

2. The circuit of claim 1 wherein said switch is a transistor.

3. The circuit of claim 2 wherein said transistor is one of a FET and an IGBT.

4. The circuit of claim 1 wherein said second control signal is provided in response to the voltage across terminals of said switch.

5. A circuit for generating a control voltage across a pair of output terminals for controlling a switch having an input terminal, a reference terminal, and a control terminal, said circuit comprising:

a capacitor;

a first pair of switches adapted to couple said capacitor to an input voltage source during a first time interval;

a second pair of switches adapted to couple said capacitor to said pair of output terminals during a second time interval, non-overlapping with respect to said first time interval;

a control circuit providing a first control signal to said first pair of switches in response to the voltage across said capacitor and providing a second control signal to said second pair of switches, wherein said second control signal is provided in response to the voltage across terminals of said switch; and

a first comparator having a first input terminal coupled to said capacitor, a second input terminal coupled to a threshold voltage, and an output terminal coupled to said control circuit at which an output signal is provided, wherein said output signal is indicative of

whether or not the voltage across said capacitor is greater than a predetermined level and wherein said first control signal provided by said control circuit causes said first pair of switches to open when said voltage across said capacitor is greater than said predetermined level.

6. The circuit of claim 5 further comprising a second comparator having a first input terminal coupled to said control terminal of said switch, a second input terminal coupled to said reference terminal of said switch, and an output terminal coupled to said control circuit at which an output signal is provided, wherein said output signal is indicative of whether or not the voltage across said control and reference terminals of said switch is less than a second predetermined level and wherein said second control signal provided by said control circuit causes said second pair of switches to open when said voltage across said control and reference terminals of said switch is less than the second predetermined level.

7. The circuit of claim 1 wherein each of said first and second pairs of switches comprises either a diode and a FET or a pair of FETs.

8. A circuit responsive to an input voltage source and for providing the gate drive voltage to a gate drive circuit, said gate drive circuit adapted for biasing the gate terminal of a transistor further having a source terminal and a drain terminal, said circuit comprising:

a capacitor having a first terminal and a second terminal;

a first switch coupled between a first terminal of said input voltage source and a first terminal of said capacitor;

a second switch coupled between a second terminal of said input voltage source and a second terminal of said capacitor, wherein said first and second switches are closed during a first time interval to charge said capacitor;

a third switch coupled between said first terminal of said capacitor and said gate drive circuit;

a fourth switch coupled between said second terminal of said capacitor and said gate drive circuit, wherein said third and fourth switches are closed during a second time interval to transfer charge from said capacitor to said gate drive circuit, and wherein said first and second time intervals do not overlap;

a control circuit for providing a first control signal to said first switch and a second control signal to said second switch in response to the voltage across said capacitor and for providing a third control signal to said third switch and a fourth control signal to said fourth switch in response to the voltage across the gate and source terminals of said transistor; and

a first comparator having a first input terminal coupled to said first terminal of said capacitor, a second input terminal coupled to a threshold voltage, and an output terminal coupled to said control circuit at which an output signal is provided, wherein said output signal is indicative of whether or not the voltage across said capacitor is greater than a predetermined level and wherein said first and second control signals provided by said control circuit cause said first and second switches to open when said voltage across said capacitor is greater than said predetermined level.

9. The circuit of claim 8 further comprising a second comparator having a first input terminal coupled to said gate terminal of said transistor, a second input terminal coupled to said source terminal of said transistor, and an output terminal coupled to said control circuit at which an output

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signal is provided, wherein said output signal is indicative of whether or not the voltage across said gate and source terminals of said transistor is less than a second predetermined level and wherein said third and fourth control signals provided by said control circuit cause said third and fourth switches to open when said voltage across said gate and source terminals of said transistor is less than the second predetermined level.

10. A circuit comprising:

- a transistor having a gate terminal receiving a control signal from a gate drive circuit, a source terminal, and a drain terminal;
- a load coupled to one of said source terminal and said drain terminal of said transistor, the other of said source terminal and said drain terminal coupled to an input voltage source; and
- a gate drive voltage circuit responsive to said input voltage source for providing a gate drive voltage to said gate drive circuit, said gate drive voltage circuit comprising:
  - a capacitor;

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- a first pair of switches adapted to couple said capacitor to said input to voltage source during a first time interval; and
- a second pair of switches adapted to couple said capacitor to said gate drive circuit during a second time interval, non-overlapping with respect to said first time interval.

11. The circuit of claim 10 wherein said load is one of a switch-mode power supply and a motor.

12. The circuit of claim 10 wherein said load has one of the following topologies: a Buck converter, a boost converter, a Buck-boost converter, a forward converter, a flyback converter, and a resonant converter.

13. The circuit of claim 10 wherein said transistor is a high-side switch having said drain terminal coupled to said input voltage source.

14. The circuit of claim 10 wherein said transistor is a low-side switch having said source terminal coupled to a predetermined reference voltage.

\* \* \* \* \*





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**Imamiya**

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 (45) **Date of Patent:** **Nov. 26, 2002**

(54) **POTENTIAL DETECTOR AND SEMICONDUCTOR INTEGRATED CIRCUIT**

(75) **Inventor:** Kenichi Imamiya, Tokyo-To (JP)

(73) **Assignee:** Kabushiki Kaisha Toshiba, Kanagawa (JP)

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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 May 18, 2001 (JP) ..... 2001-149496

(51) **Int. Cl.<sup>7</sup>** ..... G05F 3/02

(52) **U.S. Cl.** ..... 327/536; 327/537

(58) **Field of Search** ..... 327/539, 536, 327/537

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,970,409 A \* 11/1990 Wada et al. .... 307/110  
 5,532,640 A \* 7/1996 Okunaga ..... 327/536  
 5,812,001 A 9/1998 Imamiya  
 6,356,137 B1 \* 3/2002 Roohparvar et al. .... 327/390  
 6,356,469 B1 \* 3/2002 Roohparvar et al. .... 327/536

**OTHER PUBLICATIONS**

Kenichi Imamiya, "Potential Change Suppressing Circuit" U.S. application 09/725,726 filed Nov. 30, 2000.  
 Kanda et al., "Semiconductor Integrated Circuit" U.S. application 09/731,881 filed Dec. 8, 2000

\* cited by examiner

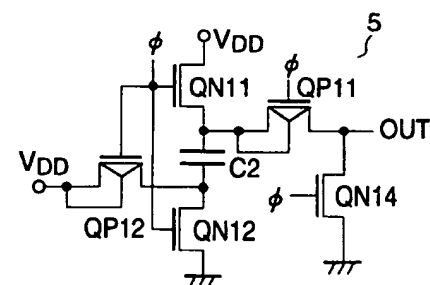
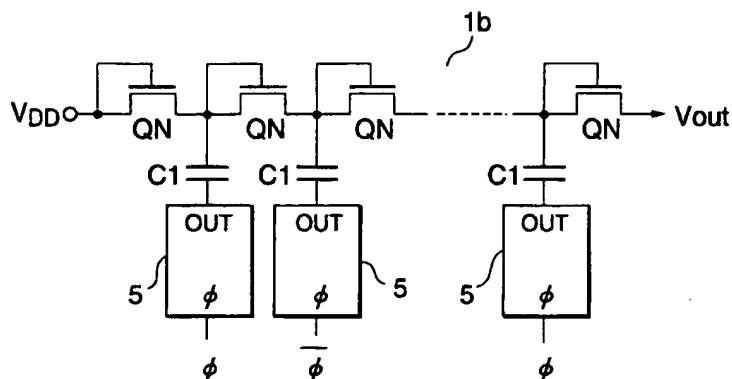
*Primary Examiner*—Terry D. Cunningham

(74) *Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.

(57) **ABSTRACT**

An integrated semiconductor circuit has a potential detector for detecting a potential boosted by a high voltage generator. One terminal of a first capacitor is connected to a potential detection terminal via a first switching device, the other terminal thereof being connected to a reference potential terminal. A terminal of a second capacitor is connected, via a second switching device, to a first node at which the first switching device and the first capacitor are connected, the other terminal thereof being connected to the reference potential terminal. A third switch is connected between a second node at which the second switching device and the second capacitor are connected and the reference potential terminal. A clock generator generates clock signals to simultaneously and periodically turn on the first and the third switching devices whereas turn on the second switch periodically in an opposite timing for the first and the third switching devices. A comparator compares a potential at the second node with a reference potential and outputs a detection signal when a potential at the potential detection terminal reaches a predetermined potential.

**3 Claims, 13 Drawing Sheets**



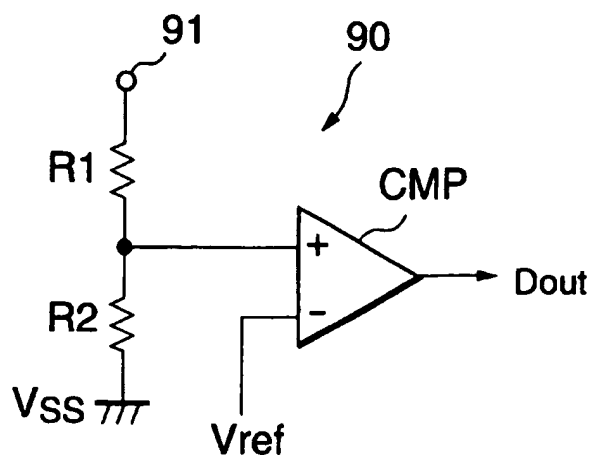


FIG. 1 (RELATED ART)

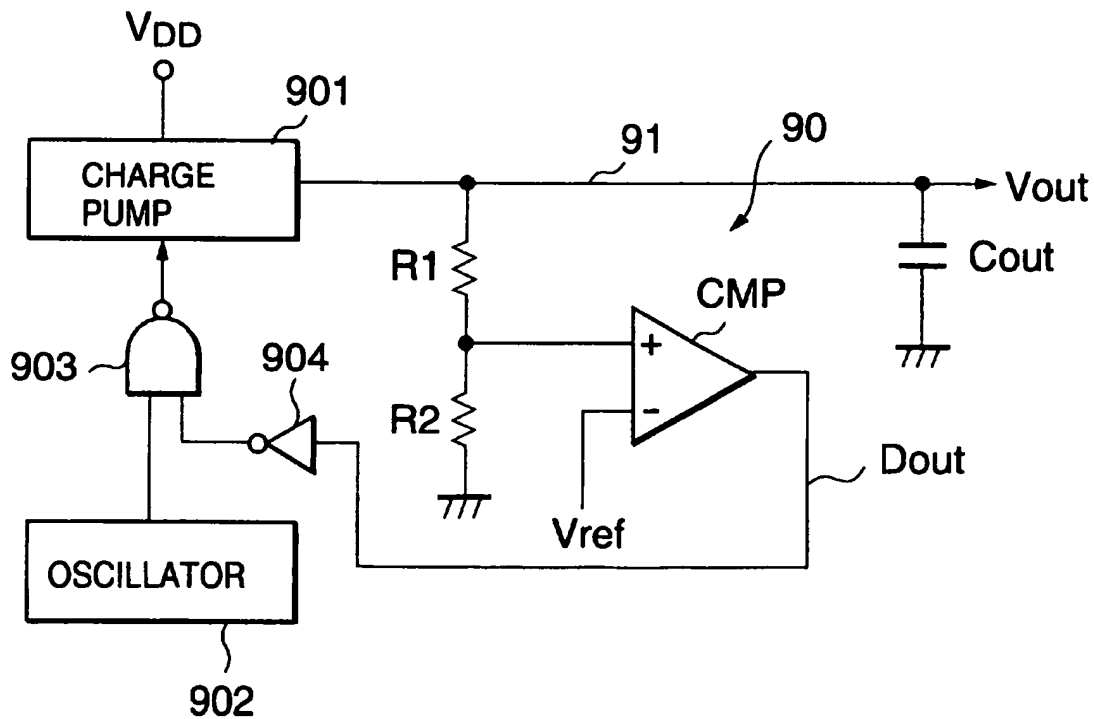


FIG. 2 (RELATED ART)

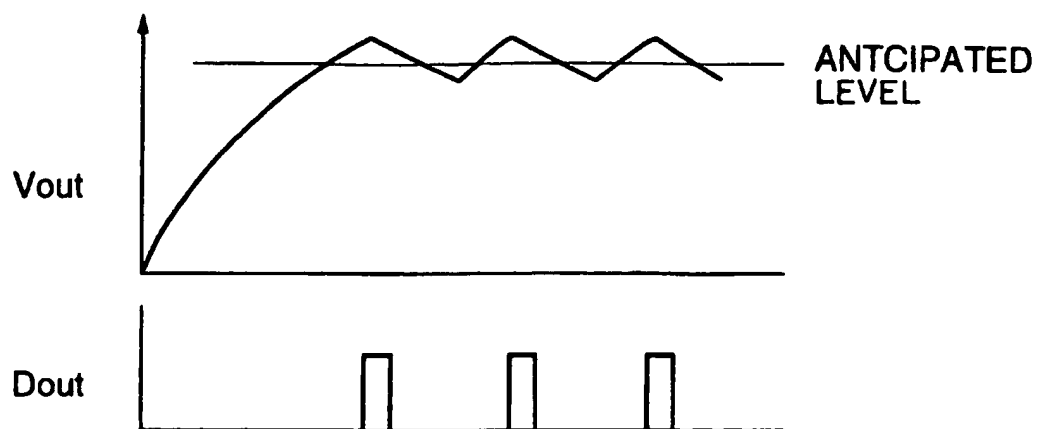


FIG. 3A

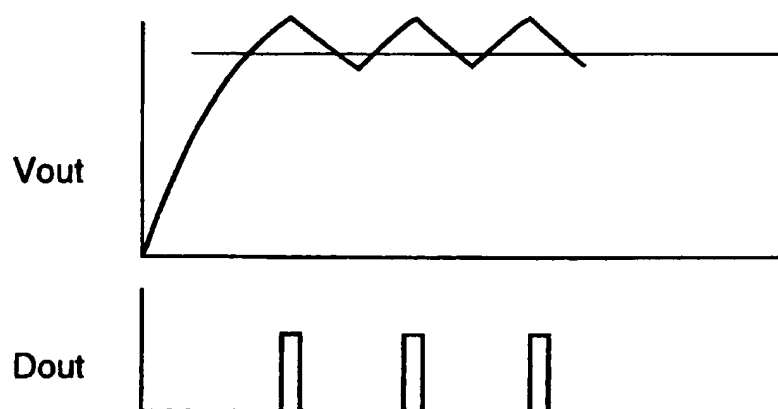


FIG. 3B

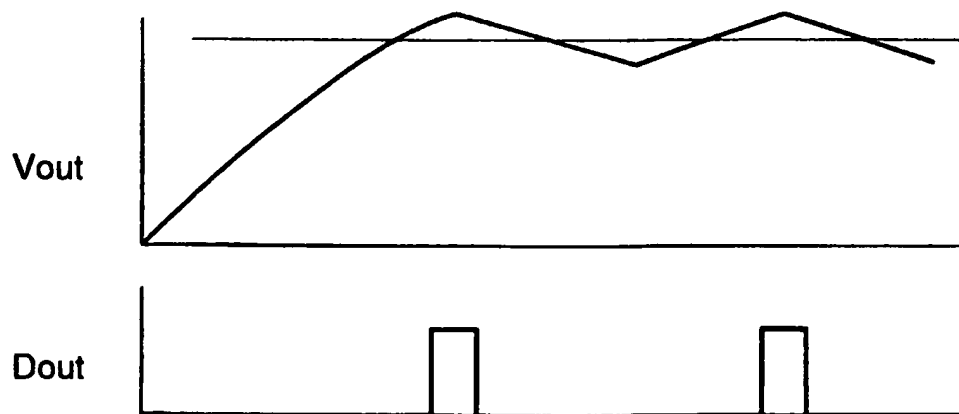


FIG. 3C

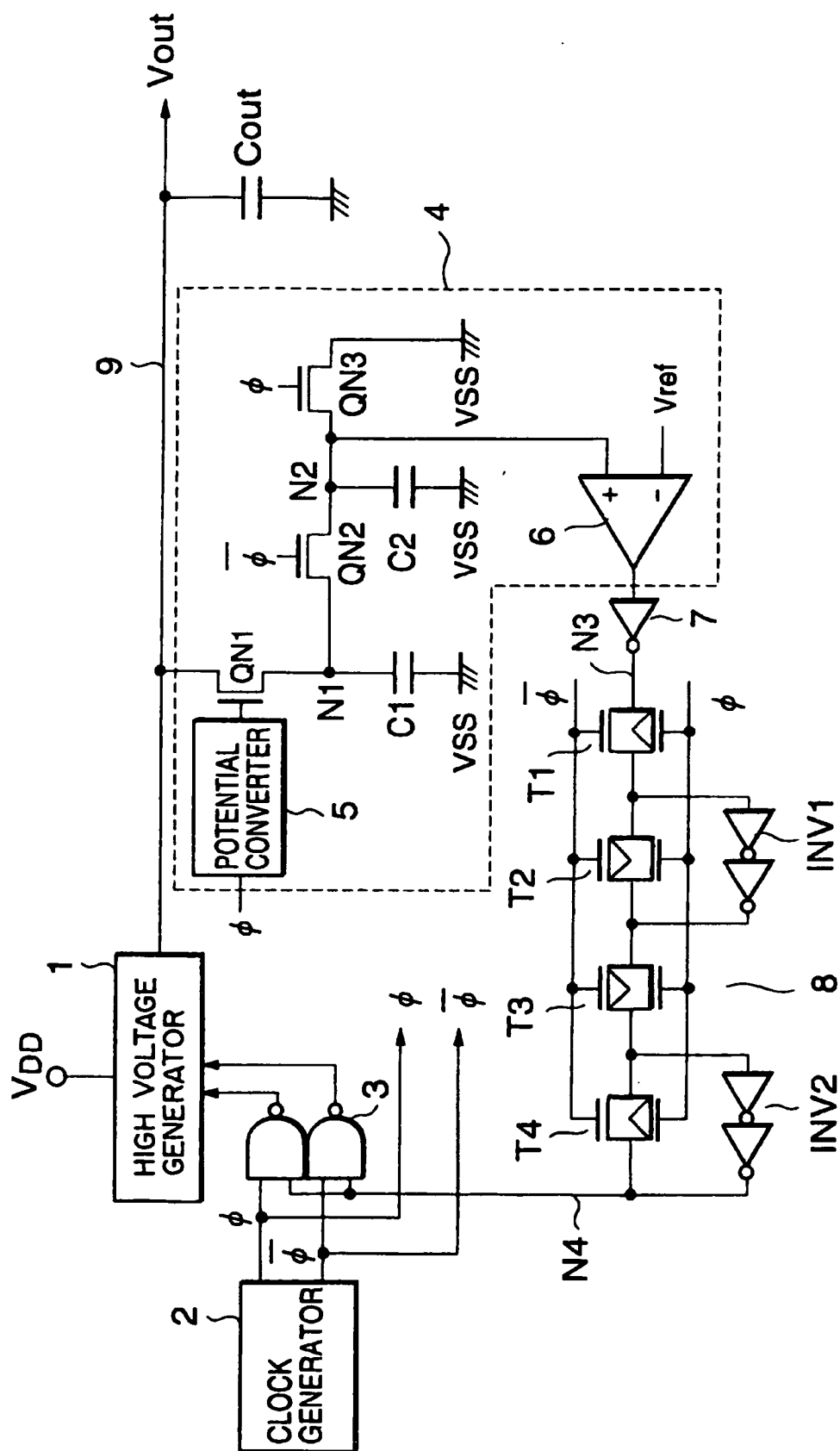


FIG. 4

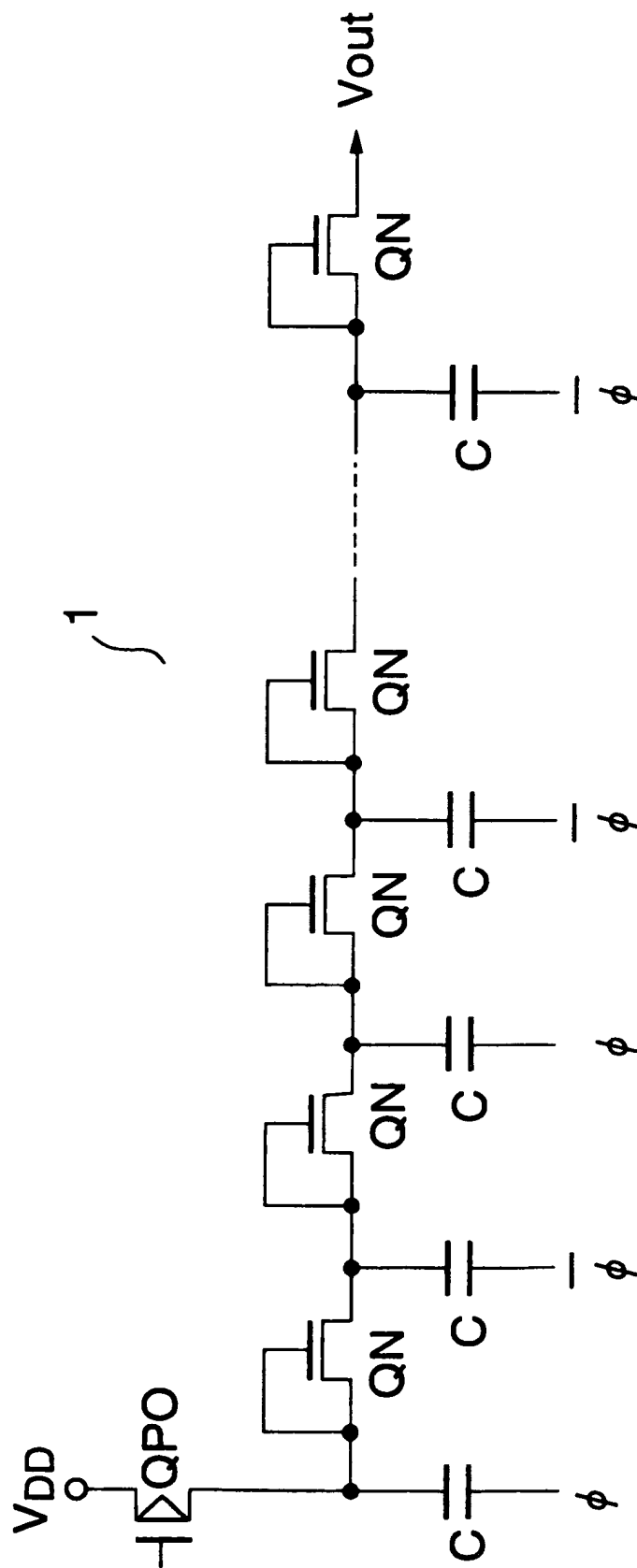


FIG. 5

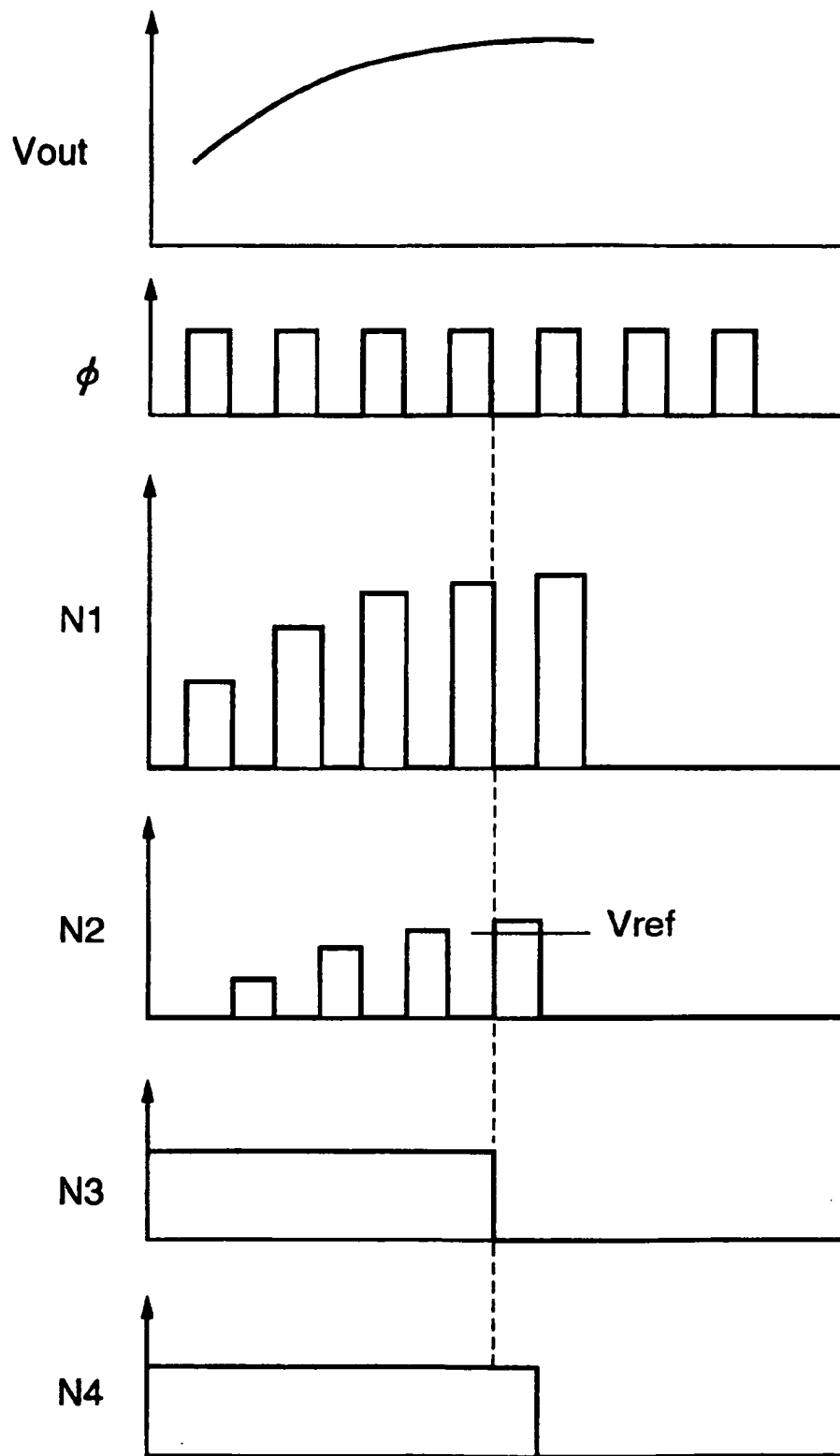


FIG. 6

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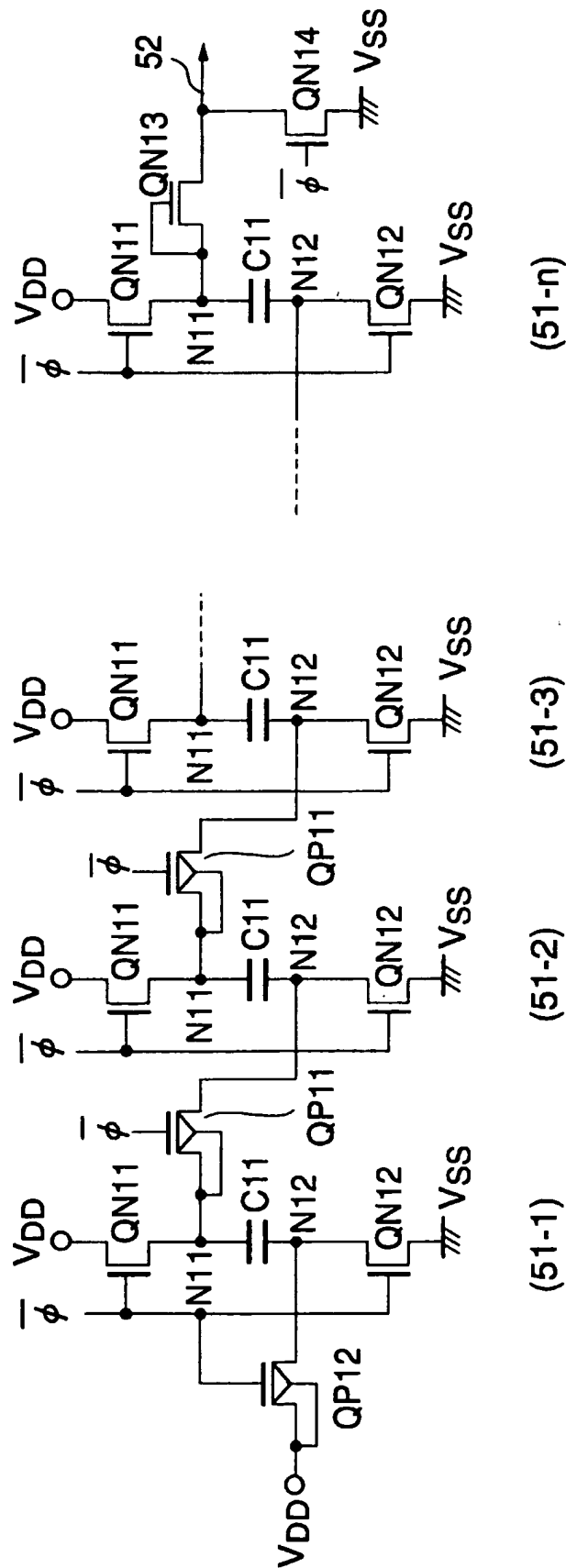


FIG. 7

5a

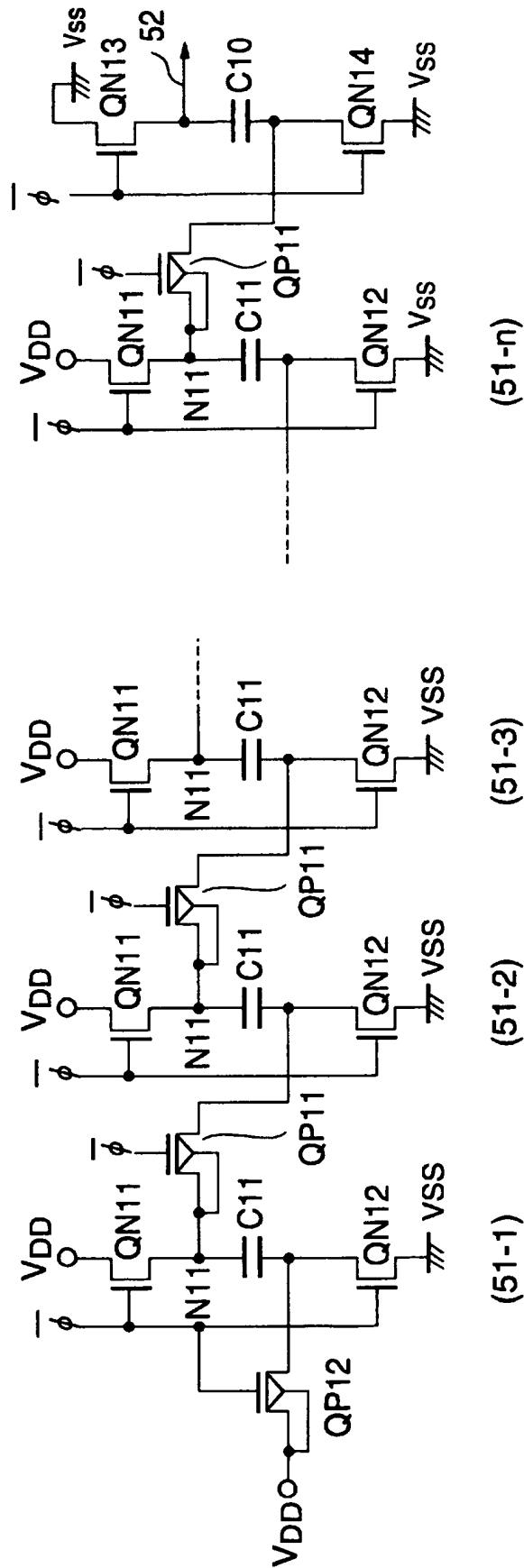


FIG.8



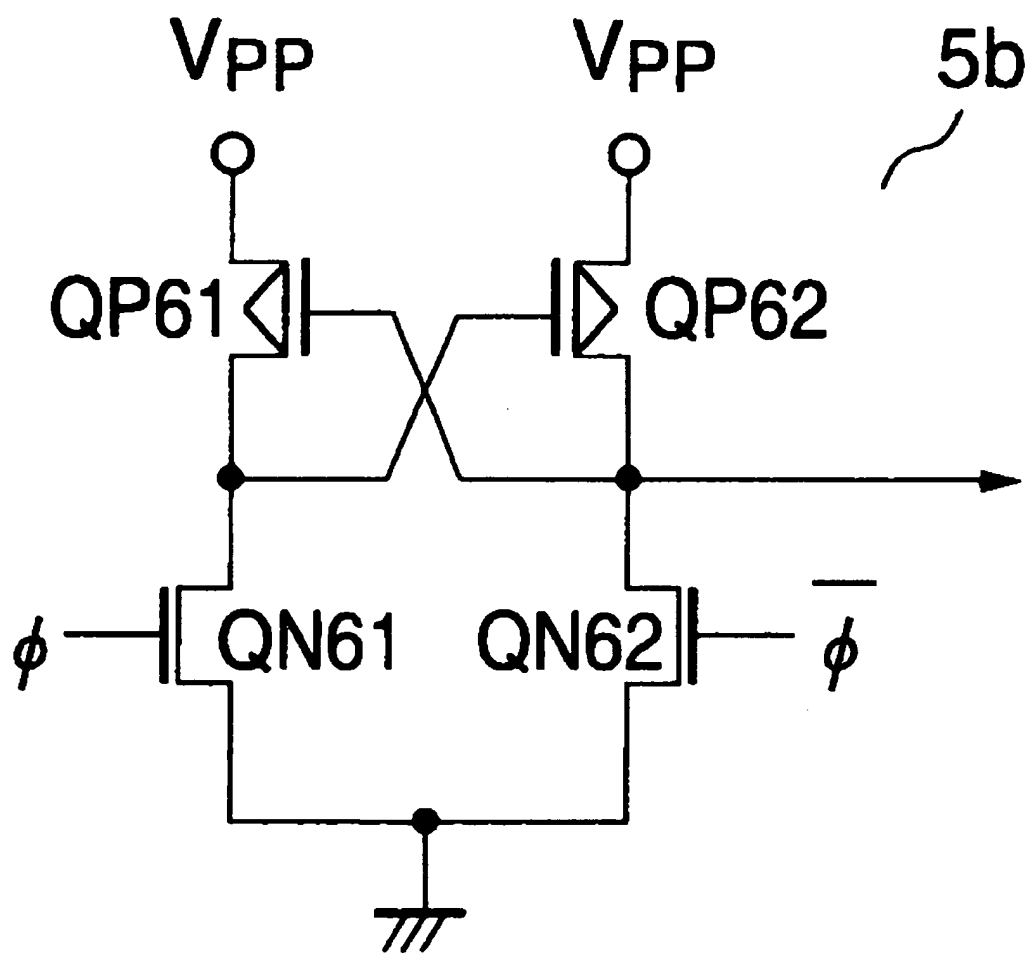
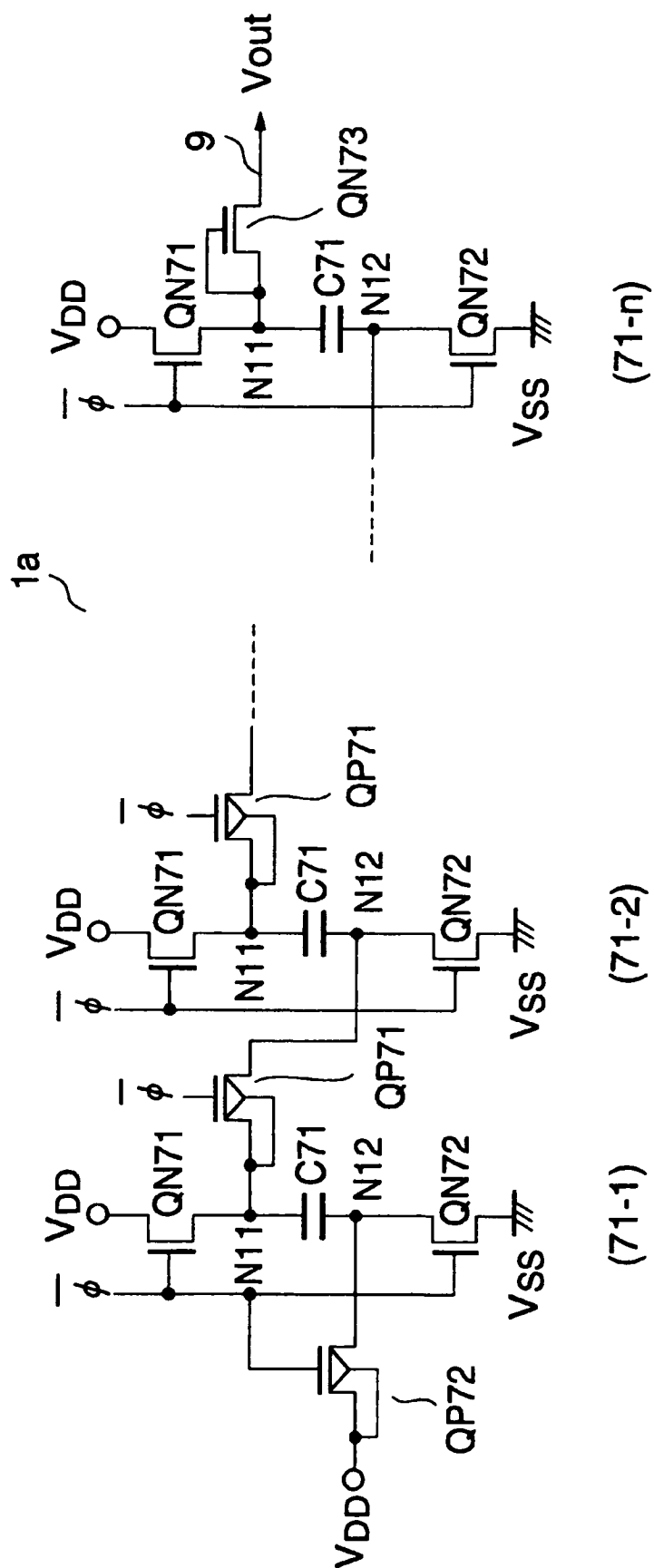
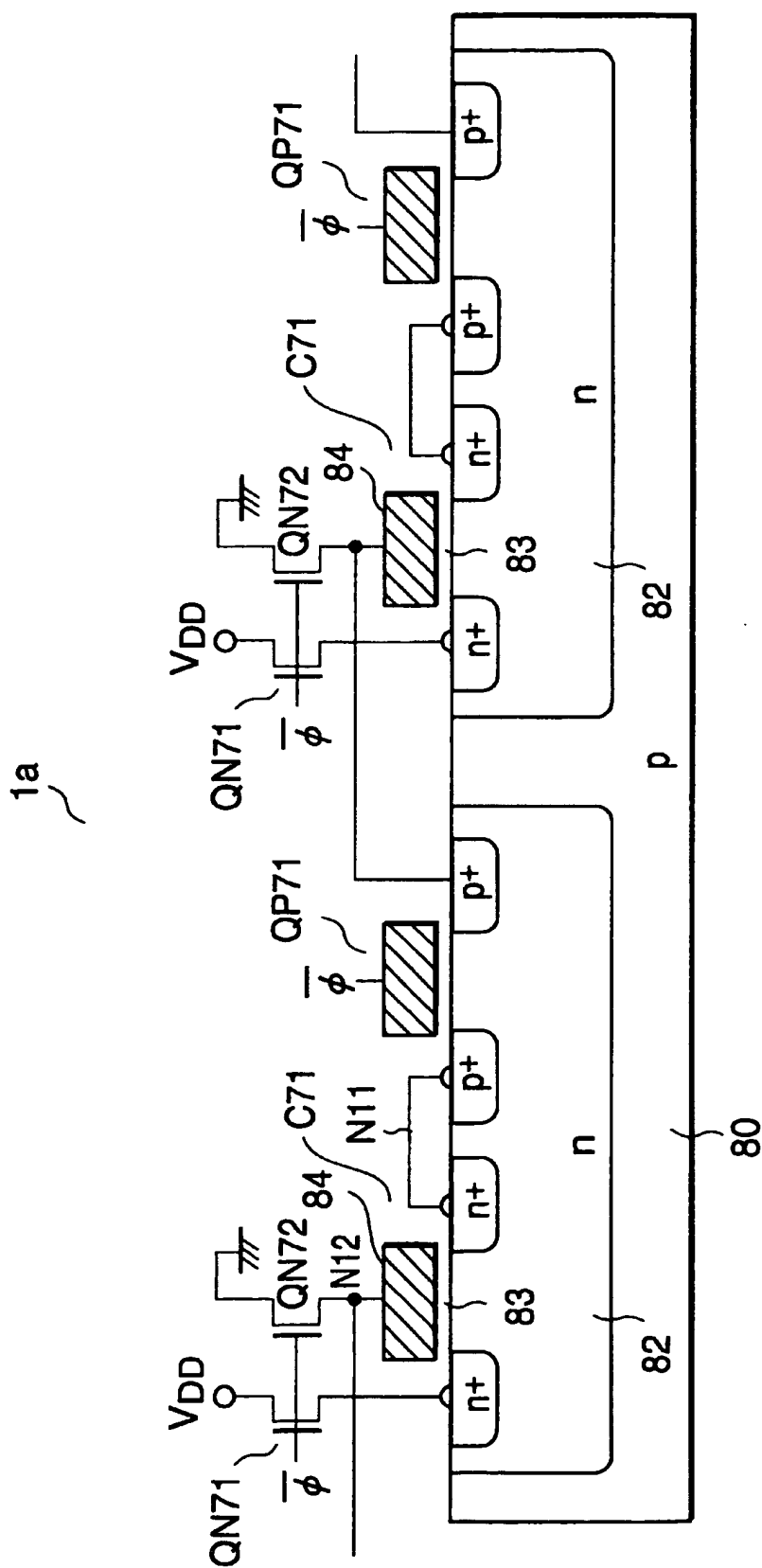


FIG. 9





**FIG. 11**

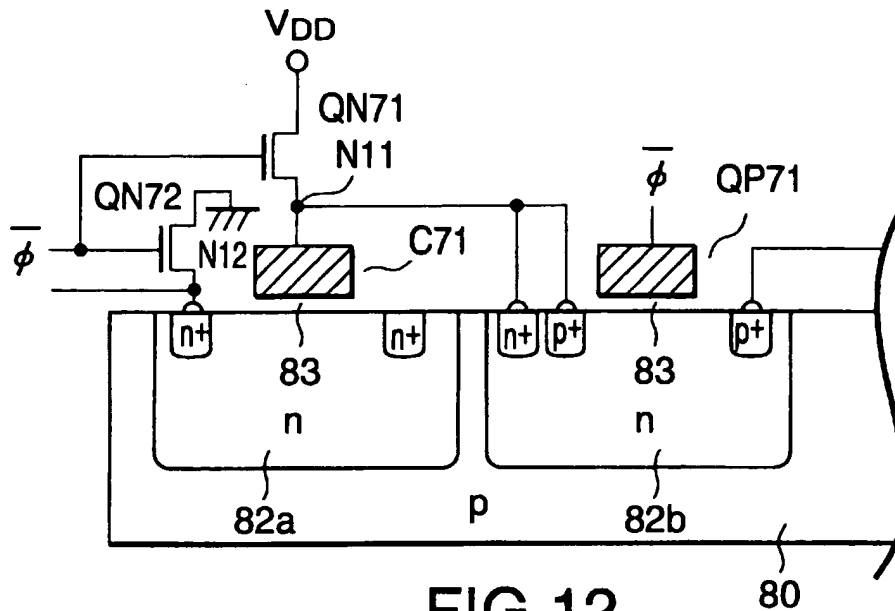


FIG. 12

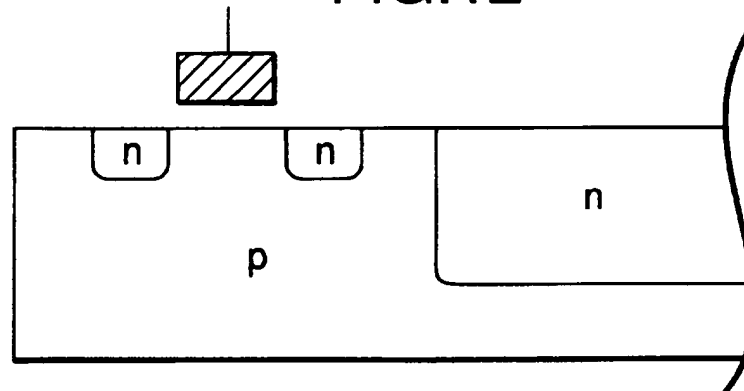


FIG. 13

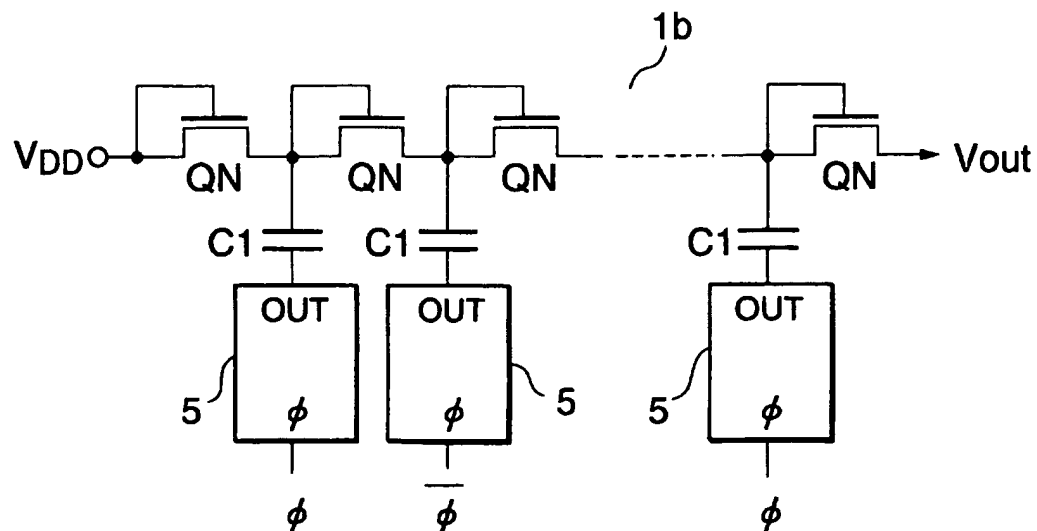


FIG.14

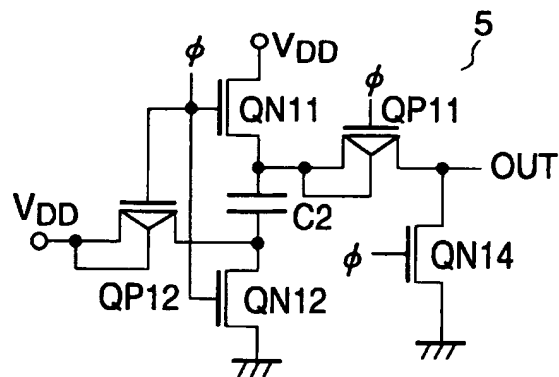


FIG. 15A

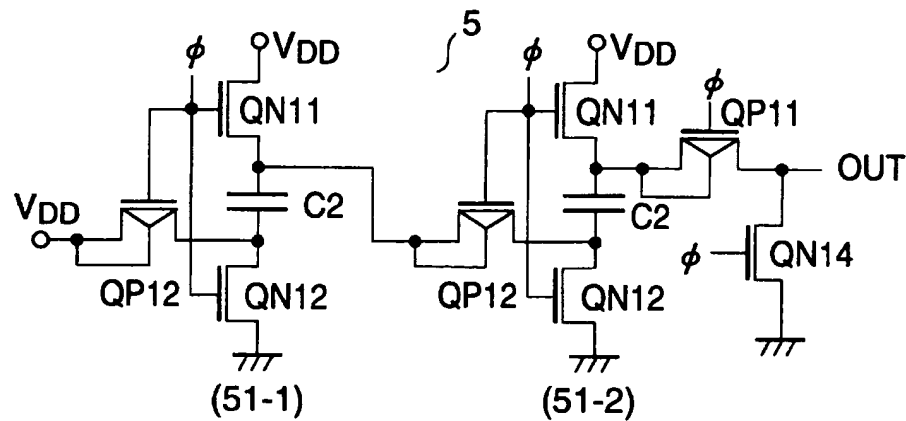


FIG. 15B

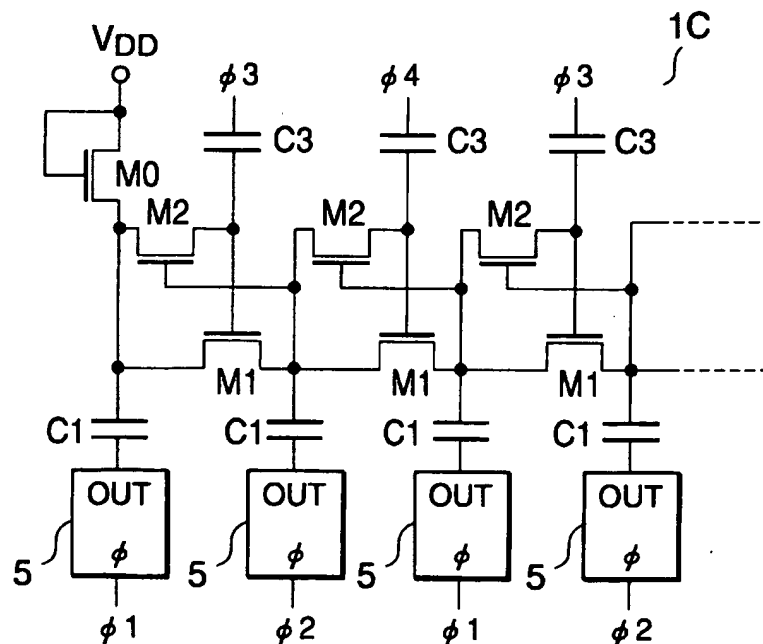


FIG. 16

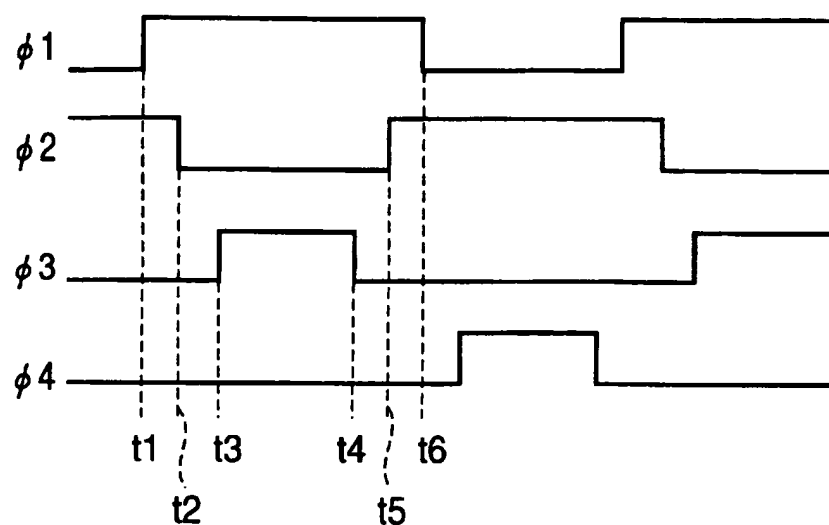


FIG.17

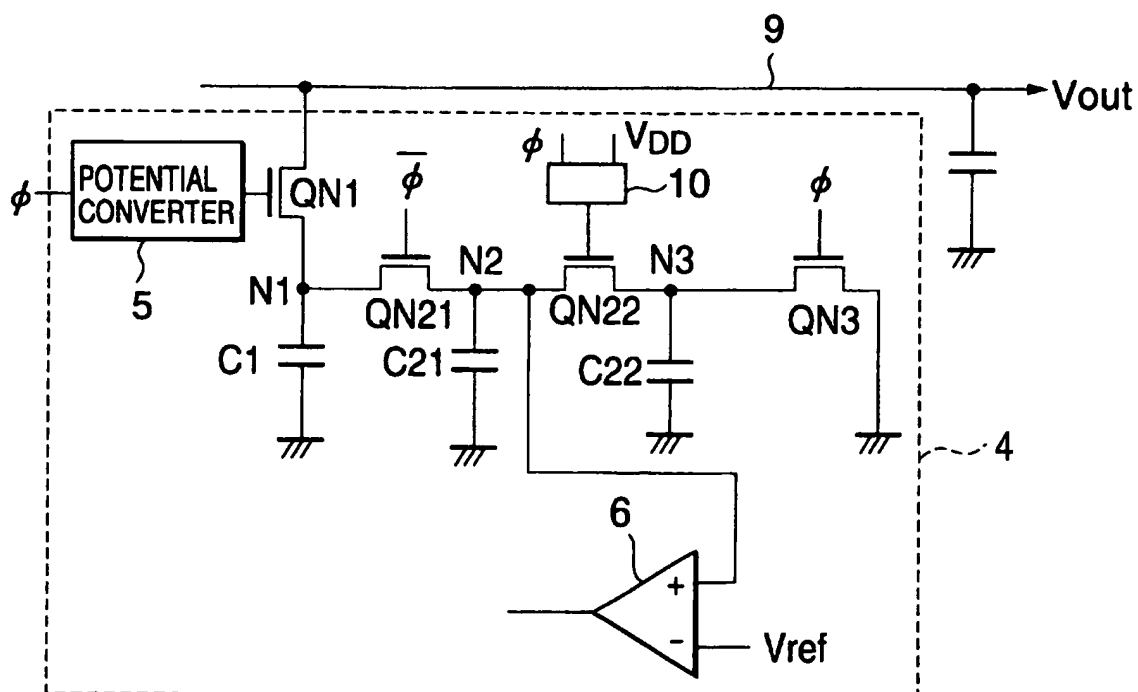


FIG.18

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## POTENTIAL DETECTOR AND SEMICONDUCTOR INTEGRATED CIRCUIT

### CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35 USC §119 to Japanese Patent Application No. 2000-153660 filed on May 24, 2000 in Japan and Japanese Patent Application No. 2001-149496 filed on May 18, 2001 in Japan, the entire contents of which are incorporated by reference herein.

### BACKGROUND OF THE INVENTION

The present invention relates to a potential detector to detect an electric potential output from a high voltage generator, etc., that has reached a certain level in a semiconductor integrated circuit.

FIG. 1 shows a known potential detector 90. The detector 90 consists of resistors R1 and R2 connected in series between a terminal 91 to be detected and a ground terminal Vss, and a comparator CMP to compare a potential at a node at which the resistors R1 and R2 are connected together with a reference potential Vref.

The potential at the node of the resistors R1 and R2 is obtained as  $V1 \cdot R2 / (R1 + R2)$  where V1 is a potential at the terminal 91. The comparator CMP outputs a high-level detection signal when the potential at the node exceeds the reference potential Vref.

The potential detector 90 is used, for example, for detecting an output potential Vout of a high voltage generator used in a semiconductor circuit such as a non-volatile semiconductor memory.

FIG. 2 shows an example where the potential detector 90 is used for detecting a potential Vout appearing at an output terminal 91 of a high voltage generator 910 such as a charge pump. The high voltage generator 901 is driven by clocks generated by an oscillator 902 such as a ring oscillator.

The potential detector 90 outputs a detection signal Dout when the potential Vout appearing at the output terminal 91 of the high voltage generator 901 reaches a certain potential to dis-activate a gate 903 that has fed clocks generated by the oscillator 902 to the high voltage generator 901. The high voltage generator 901 then stops, so that the boosted output Vout is kept at a constant level, as illustrated in FIG. 3A.

The known potential detector generates a potential by the series-connected resistors, which is compared with a reference potential. A current always flows through the resistors R1 and R2 for generating the potential. The high voltage generator 901 thus requires a drive performance high enough for accepting a current consumed by the resistors R1 and R2. The drive performance of the high voltage generator is decided according to the resistance of the resistors R1 and R2 when a load capacitance to be driven by the high voltage generator is relatively small. This requires drive performance for the high voltage generator higher than that for the high voltage generator to drive the load itself, which is not practical in view of power consumption and circuit integration.

A high voltage generator having unnecessarily high drive performance will generate a potential boosted to a high level during a response time of a potential detector. This results in a large variation in boosted output Vout against an anticipated level, as illustrated in FIG. 3B, with difficulty in obtaining a constantly boosted potential.

The larger the resistance of the resistors R1 and R2 for avoiding such potential variation, the larger the parasitic

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capacitance to the resistors. This results in a large delay of change in output potential of the high voltage generator, and further a large delay time required for the output potential to be transferred to the input terminal of the comparator CMP. Change in output potential of the high voltage generator illustrated in FIG. 3C does not have an abrupt potential increase such as shown in FIG. 3B, however, exhibits a slow response. This also results in unstably un-converted potential output.

### SUMMARY OF THE INVENTION

A purpose of the present invention is to provide a potential detector integrated on a small area and capable of stable potential detection while consuming a small power.

Another purpose of the present invention is to provide a semiconductor integrated circuit with the potential detector and having a high voltage generator for generating a constant potential output.

The present invention provides a potential detector comprising: a first capacitor, one terminal thereof being connected to a potential detection terminal via a first switching device, another terminal thereof being connected to a reference potential terminal; a second capacitor, a terminal thereof being connected, via a second switching device, to a first node at which the first switching device and the first capacitor are connected, another terminal thereof being connected to the reference potential terminal; a third switch connected between a second node at which the second switching device and the second capacitor are connected and the reference potential terminal; a clock generator for generating clock signals to simultaneously and periodically turn on the first and the third switching devices whereas turn on the second switch periodically in an opposite timing for the first and the third switching devices; and a comparator for comparing a potential at the second node with a reference potential and outputting a detection signal when a potential at the potential detection terminal reaches a predetermined potential.

Moreover, the present invention provides a semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential and a potential detector for controlling the high voltage generator by detecting a potential at an output terminal of the high voltage generator, the potential detector comprising: a first capacitor, one terminal thereof being connected to an output terminal of the high voltage generator via a first switching device, another terminal thereof being connected to a reference potential terminal; a second capacitor, one terminal thereof being connected, via a second switching device, to a first node at which the first switching device and the first capacitor are connected, another terminal thereof being connected to the reference potential terminal; a third switching device connected between a second node at which the second switching device and the second capacitor are connected and the reference potential terminal; a clock generator for generating clock signals to simultaneously and periodically turn on the first and the third switching devices whereas turn on the second switching device periodically in an opposite timing for the first and the third switching devices; and a comparator for comparing a potential at the second node with a reference potential and outputting a detection signal when a potential at the potential detection terminal reaches a predetermined potential.

Furthermore, the present invention provides a semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the

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high voltage generator comprising: a plurality of charging circuits, each having a capacitor, one terminal thereof being connected to a high-level side power terminal via a first switching device, another terminal thereof being connected to a low-level side power terminal via a second switching device; and a plurality of third switching devices each provided between adjacent two charging circuits so that a node at which the first switching device and the capacitor of each charging circuit are connected is connected to another node at which the second switching device and the capacitor of the succeeding charging circuit are connected, wherein the capacitor of each charging circuit is charged with a potential almost equal to a power supply potential when the first and the second switching devices are turned on whereas the third switching devices are turned off and the charged capacitors of the charging circuits are coupled in series when the first and the second switching devices are turned off whereas the third switching devices are turned on, thus outputting a boosted potential.

Moreover, the present invention provides a semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising: a charge pump having a plurality of first capacitors, adjacent two first capacitors being driven by clocks in opposite timing and a transfer device for transferring charges stored in each first capacitor to the succeeding first capacitor; and a potential converter for supplying a boosted clock to each first capacitor, wherein the potential converter includes: a second capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device; a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the second capacitor; a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the second capacitor to an output terminal; and a fifth switching device that is turned on simultaneously with the first switching device to reset a potential at the output terminal, wherein the second capacitor is charged while the first and the second switching devices are on and the charged second capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

Furthermore, the present invention provides a semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising: a plurality of first capacitors that are charged during a first period; a plurality of second capacitors provided alternately with the first capacitors, the second capacitors being charged during a second period that partially overlaps with the first period; a first transfer device for transferring charges stored in each first capacitor to the succeeding second capacitor during a third period that is delayed from the second period by a predetermined time; and a second transfer device for transferring charges stored in each second capacitor to the succeeding first capacitor during a fourth period that is delayed from the first period by the predetermined time.

#### BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 shows a circuit diagram of a known potential detector;

FIG. 2 shows an example circuit diagram to which the known potential detector is applied;

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FIGS. 3A to 3C illustrate waveforms in potential up-conversion by the known potential detector;

FIG. 4 shows a circuit diagram of a power supply according to the present invention;

FIG. 5 shows a circuit diagram of a high voltage generator used in the power supply;

FIG. 6 illustrates waveforms in potential detection by the power supply;

FIG. 7 shows a circuit diagram of a potential converter used in the power supply;

FIG. 8 shows a circuit diagram of a modification to the potential converter;

FIG. 9 shows a circuit diagram of another modification to the potential converter;

FIG. 10 shows a circuit diagram of a modification to the high voltage generator;

FIG. 11 illustrates a structure of the modification to the high voltage generator;

FIG. 12 illustrates another structure of the modification to the high voltage generator;

FIG. 13 illustrates another structure of the capacitor in the modification to the high voltage generator;

FIG. 14 shows a circuit diagram of another modification to the high voltage generator;

FIG. 15A shows a circuit diagram of still another modification to the potential converter;

FIG. 15B shows a circuit diagram of a further modification to the potential converter;

FIG. 16 shows a circuit diagram of still another modification to the high voltage generator;

FIG. 17 illustrates waveforms of clock signals in the high voltage generator shown in FIG. 16; and

FIG. 18 shows a circuit diagram of another embodiment of a potential detector.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments according to the present invention will be disclosed with reference to the attached drawings.

FIG. 4 shows a circuit diagram of a power supply used in a semiconductor circuit.

The main components of this circuit are a high voltage generator 1 for obtaining an internal power supply potential higher than a power supply potential  $V_{DD}$  and a clock generator 2 for driving the high voltage generator 1.

The high voltage generator 1 is a known charge pump shown in FIG. 5. The clock generator 2 is, for example, a ring oscillator, that generates clocks  $\phi$  and  $\bar{\phi}$  for controlling the charge pump.

The semiconductor circuit for which the present invention is applied is, for example, a non-volatile semiconductor memory. A boosted output potential  $V_{out}$  of the high voltage generator 1 is used for data programming and erasure.

The complementary clocks  $\phi$  and  $\bar{\phi}$  of the clock generator 2 are selectively supplied to the high voltage generator 1 via a NAND gate 3. The NAND gate 3 is controlled to turn on or off the high voltage generator 1. A potential detector 4 is provided to detect a potential appearing at an output terminal 9 for controlling the high voltage generator 1.

The area surrounded by a dashed line is a main section of the potential detector 4. The detector 4 is also controlled by the complementary clocks  $\phi$  and  $\bar{\phi}$  of the clock generator 2. Another clock generator may be provided only for controlling the potential detector 4.



The potential detector 4 has two capacitors C1 and C2, a terminal of each being connected to a ground terminal Vss. The other terminal N1 of the first capacitor C1 is connected to the output terminal 9 of the high voltage generator 1 via an NMOS transistor QN1. The other terminal N2 of the second capacitor C2 is connected to the terminal N1 via an NMOS transistor QN2.

The output (Vout) terminal 9 of the high voltage generator 1 has a large load capacitance Cout in this embodiment. The capacitors C1 and C2 used for the potential detector 4 have capacitance much smaller than the load capacitance Cout.

The NMOS transistor QN1 is a switching device for charging the capacitor C1 with the output Vout of the high voltage generator 1. The gate of the NMOS transistor QN1 is driven by the clock signal  $\phi$ .

The NMOS transistor QN2 is a switching device for supplying a certain amount of charges stored in the capacitor C1 to the capacitor C2 while short-circuiting the nodes N1 and the N2 of the two capacitors. The gate of the NMOS transistor QN2 is driven by the clock signal  $\phi$ .

The node N2 of the capacitor C2 and the NMOS transistor QN2 is connected to the ground terminal Vss via an NMOS transistor QN3 (a resetting-switching device). The gate of the NMOS transistor QN3 is driven by the clock signal  $\phi$ .

A potential converter 5 is connected to the gate of the NMOS transistor QN1 for up-converting the clock signal  $\phi$  to drive the transistor QN1 so that output Vout of the high voltage generator 1 boosted based on the power supply potential VDD is sufficiently transferred to the capacitor C1.

A potential higher than the power supply potential VDD is supplied to the gate of the charging NMOS transistor QN1. On the other hand, the power supply potential VDD is supplied to the gates of the charge-supplying NMOS transistor QN2 and the resetting NMOS transistor QN3. The gate oxide film of the NMOS transistor QN1 is thus formed as thicker than those of the NMOS transistors QN2 and QN3.

The node N2 of the capacitor C2 and the NMOS transistor QN2 is connected to an input terminal of a comparator 6 (a differential amplifier). A reference potential Vref is supplied to the other terminal of the comparator 6. When a potential at the node N2 exceeds the reference potential, the comparator outputs a high-level detection signal.

The detection signal is supplied to a flip-flop 8 via an inverter 7. The flip-flop 8 consists of series-connected four CMOS transfer gates T1 to T4 that are alternately turned on and off by the clock signals  $\phi$  and  $\phi$  and two inverter chains INV1 and INV2 connected in parallel to the second and the fourth gates T2 and T4, respectively. The output of the flip-flop 8 is used as a control signal for activating the NAND gate 3.

The operation of the high voltage generator 1 of the power supply circuit (FIG. 4) is disclosed with reference to FIG. 6 that illustrates waveforms in up-conversion and potential detection.

The high voltage generator 1 is controlled by the clock signals  $\phi$  and  $\phi$  so that the output potential Vout is gradually increased as shown in FIG. 6. In the potential detector 4, the NMOS transistors QN1 and QN3 are turned on whereas the NMOS transistor QN2 is turned off while the clock signal  $\phi$  is HIGH. The capacitor C1 is charged with the potential at the output terminal 9 of the high voltage generator 1 while the capacitor C2 is discharged to be reset.

When the clock signal  $\phi$  is turned into LOW, the NMOS transistors QN1 and QN3 are turned off whereas the NMOS

transistor QN2 is on. The nodes N1 and N2 are thus isolated from the output terminal 9 of the high voltage generator 1 and the ground terminal Vss, respectively, and short-circuited with each other. This initiates the supply of the charges that has been stored in the capacitor C1 when sampled at the high-level clock signal  $\phi$  to the capacitor C2.

The charge supply results in the same potential at the node N1 and N2. In detail, when the capacitor C1 has been charged with a potential V1, a potential V2 obtained by charge supply is expressed as  $V2 = V1 \cdot C1 / (C1 + C2)$  lower than the potential V1. The potential at the node N2 is thus increased from the ground potential Vss to the potential V2. The potential at the node N2 is compared with the reference potential Vref in the comparator 6.

When the potential at the node N2 has not reached the reference potential Vref, the node N2 is discharged at the next high-level clock signal  $\phi$  for another charging of the node N1 with the output of the high voltage generator 1. The charge supply is performed again at the next low-level clock signal  $\phi$ . These charging and supplying operations are repeated until the potential at the node N2 exceeds the reference potential Vref.

When the potential at the node N2 exceeds the reference potential Vref as the boosted potential Vout has been increased, as shown in FIG. 6, the output of the comparator 6 is inverted and hence a node N3 is turned into LOW. An output node N4 of the flip-flop 8 is then turned into LOW at the high-level clock signal  $\phi$ . The NAND gate 3 is thus turned off to stop the supply of clock signals to the high voltage generator 1 for halting the up-conversion operation.

The NMOS transistor QN1, a switching device for charging the capacitor C1, is driven by a potential boosted by the voltage converter 5 so that almost no potential drop occurs at the capacitor 1.

The capacitors C1 and C2 have very small capacitance compared to the capacitance Cout of the output terminal 9 of the high voltage generator 1 so that a potential drop that may otherwise occur at the output terminal 9 when the capacitor 1 is coupled to the output terminal 9 via the NMOS transistor QN1 can be disregarded.

A constant output potential Vout under ideal circuit response is expressed as

$$V_{ref}(C1+C2)/C1 \quad (1)$$

where C1 and C2 are the capacitance of the capacitors C1 and C2.

A ratio of the capacitance of the capacitors C1 and C2 to the load capacitance Cout of the output terminal 9 of the high voltage generator 1 is preferably  $1/10$  or lower. This capacitance ratio serves to disregard a potential drop that will occur at the output terminal 9 when the capacitor 1 is coupled to the output terminal 9 via the NMOS transistor QN1.

A constant point of the output potential Vout of the high voltage generator 1 is decided in accordance with the reference potential Vref and the capacitance of the capacitors C1 and C2 according to the expression (1). A ratio of the capacitance of the capacitor C1 to C2 can be set freely.

As described above, according to this embodiment, a boosted potential is detected with capacitor charging and charge supply at low power because of generation of no D. C. current which is generated in the known method using potential division by resistors.

The smaller the areas, or the capacitance of the capacitors C1 and C2, the larger the equivalent resistance thereof, and

hence the smaller the leak current. The high voltage generator 1 is thus free from leakage. Especially, the capacitors C1 and C2 having the capacitance  $\frac{1}{10}$  or lower of the load capacitance  $C_{out}$  of the output terminal 9 serve to disregard a potential drop occurring at the output terminal 9 when the capacitor C1 is coupled thereto via the NMOS transistor QN1.

Smaller areas for the capacitors C1 and C2 serve to decrease occurrence of leakage different from the known method using resistors, thus high circuit integration is achieved according to this embodiment.

Moreover, a large equivalent resistance to the capacitors C1 and C2 in this embodiment does not increase parasitic capacitance which may otherwise occur in the known method using resistors. The embodiment is thus excellent in circuit response for stable potential detection.

FIG. 7 shows a circuit diagram of the potential converter 5 for driving the charging NMOS transistor QN1 in FIG. 4.

The potential converter 5 shown in FIG. 7 has a plurality of charging circuits 51 (51-1 to 51-n) and switching devices that connect capacitors C11 of the circuits 51 in series.

Each charging circuit 51 has a capacitor C11, a terminal N11 thereof being connected to a high-level side power terminal  $V_{DD}$  via a switching device NMOS transistor QN11 and the other terminal N12 being connected to a low-level side power terminal  $V_{SS}$  via a switching device NMOS transistor QN12. The gates of NMOS transistors QN11 and QN12 are driven by a clock signal  $\phi$ .

PMOS transistors QP11 are switching devices for connecting the capacitors C11 of the charging circuits 51 in series. In detail, each PMOS transistor QP11 is provided to connect a high level-side node N11 of the capacitor C11 of each charging circuit 51 to a low level-side node N12 of the capacitor C11 of the succeeding charging circuit. The gates of the PMOS transistors QP11 are also driven by the clock signal  $\phi$ .

The low level-side node N12 of the capacitor C11 of the first charging circuit 51-1 is connected to the high-level side power terminal  $V_{DD}$  via a PMOS transistor QP12 driven by the clock signal  $\phi$ .

The high level-side node N11 of the capacitor C11 of the last charging circuit 51-n is connected to an output terminal 52 that is connected to the gate of the NMOS transistor QN1 (FIG. 4) via an NMOS transistor QN13 whose gate and source are connected like a diode. Also connected to the output terminal 52 is a resetting NMOS transistor QN14.

An operation of the potential converter 5 shown in FIG. 7 is disclosed.

In each charging circuit 51, the NMOS transistors QN11 and QN12 are turned on at a high-level clock signal  $\phi$  to charge the capacitor C11.

When the clock signal  $\phi$  is turned into LOW, all charging circuits 51 are turned off whereas the PMOS transistors QP11 between adjacent charging circuits and the PMOS transistor QP12 at the first charging circuit are turned on.

These transistor-switching operations serve to connect the capacitors C11 of all charging circuits 51 in series with a reference potential  $V_{DD}$  at the terminal N12 of the capacitor C11 of the first charging circuit 51-1 via the PMOS transistor QP12.

The capacitance-coupling through the series-coupled capacitors C11 of the charging circuits 51 instantaneously produces a high potential at the last charging circuit 51-n. When a charged level for each capacitor C11 is  $V_{DD}$ ,  $2V_{DD}$ ,  $3V_{DD}$ , ..., and  $(n+1)V_{DD}$  appear at the nodes N11 of the capacitors C11 of the first (51-1), the second (51-2), ..., and the last (51-n) charging circuits, respectively, because of successive capacitance-coupling.

At the next high-level clock signal  $\phi$ , the potential converter 5 is reset through the resetting NMOS transistor QN14.

As disclosed, a boosted potential is obtained in synchronism with the low-level clock signal  $\phi$  (the high-level signal clock signal  $\phi$ ). This high potential turns on the NMOS transistor QN11 (FIG. 4), so that the output potential of the high voltage generator 1 is transferred to the capacitor C1 with almost no potential drop.

A charge pump provides potential increase by  $V_{DD}$  only per clock. On the contrary, the potential converter 5 shown in FIG. 7 can produce a boosted potential higher than  $V_{DD}$  per clock.

Moreover, the PMOS transistors QP11 and QP12 do not suffer high voltage application at their source-drain junctions, thus can be integrated in a small area. Each capacitor C11 also does not suffer high voltage application, thus can be formed with a thin dielectric film for large capacitance per unit of area. Therefore, the potential converter 5 in FIG. 7 having those transistors and capacitors can be formed in a small area.

FIG. 8 shows a circuit diagram of a potential converter 5a, a modification to that shown in FIG. 7.

The potential converter 5a has a series of circuit of a capacitor C10 and NMOS transistors QN13 and QN14 at the output stage. The source of the NMOS transistor QN14 is connected to a terminal of the capacitor C10 is connected to the low-level side power terminal  $V_{SS}$ . The drain of the NMOS transistor QN13 connected to the other terminal of the capacitor C10 is also connected to the low-level side power terminal  $V_{SS}$ . The gates of the NMOS transistors QN13 and QN14 are driven by the clock signal  $\phi$ , the same as the charging circuits 51.

At a high-level clock signal  $\phi$ , the capacitors C11 of the charging circuits 51 are charged whereas the capacitor C10 at the output stage is reset by the NMOS transistors QN13 and QN14 and discharged.

The NMOS transistors QN13 and QN14 are turned off when the clock signal  $\phi$  is turned into LOW to output a potential, via the capacitor C10, that has been boosted by series-coupling of the capacitors C11 of the charging circuits 51.

This potential converter 5a also has the same advantages when used for potential detection (FIG. 4) like the potential converter 5 shown in FIG. 7.

The potential converters 5 and 5a shown in FIGS. 7 and 8, respectively, output a high potential by charging a plurality of capacitors and switching of series capacitance-coupling.

FIG. 9 shows a circuit diagram of a potential converter 5b that can be used for potential detection when there is a high voltage generator for generating a boosted potential  $V_{pp}$ .

The gates of differential NMOS transistors 61 and 62 whose sources are grounded together are driven by clock signals  $\phi$  and  $\phi$ , respectively. The drain of these NMOS transistors QN61 and 62 are supplied with a boosted potential  $V_{pp}$  via PMOS transistors QP61 and QP62, respectively. The gates and drains of the PMOS transistors QP61 and QP62 are cross-connected to each other. The potential converter 5b outputs the boosted potential  $V_{pp}$  in synchronism with the clock signal  $\phi$  having a potential the same as a power supply potential.

FIG. 10 shows a circuit diagram of a high voltage generator 1a that is a modification to the charge pump shown in FIG. 4, almost the same structure as those shown in FIGS. 7 and 8.

The high voltage generator 1a has a plurality of charging circuits 71 (71-1 to 71-n) and switching devices for connecting capacitors C71 of the circuits 71 in series.

Each charging circuit 71 has a capacitor C71, a terminal N11 thereof being connected to a high-level side power terminal  $V_{DD}$  via a switching device NMOS transistor QN71 and the other terminal N12 being connected to a low-level side power terminal  $V_{SS}$  via a switching device NMOS transistor QN72. The gates of NMOS transistors QN71 and QN72 are driven by a clock signal  $\phi$ .

PMOS transistors QP71 are switching devices for connecting the capacitors C71 of the charging circuits 71 in series. In detail, the PMOS transistor QP71 connects a high level-side node N11 of the capacitor C71, for example, of the first charging circuit 71-1 to a low level-side node N12 of the capacitor C71 of the second charging circuit 71-2. The gates of PMOS transistors QP71 are also driven by the clock signal  $\phi$ .

The low level-side node N12 of the capacitor C71 of the first charging circuit 71-1 is connected to the high-level side power terminal  $V_{DD}$  via the PMOS transistor QP72 driven by the clock signal  $\phi$ .

The high level-side node N11 of the capacitor C71 of the last charging circuit 71-n is connected to the output terminal 9 (FIG. 4) via an NMOS transistor QN73 whose gate and source are connected like a diode.

The high voltage generator 1a operates the same as the potential converters 5 and 5a shown in FIGS. 7 and 8, respectively, thus generating a boosted high potential per clock cycle, different from a charge pump.

FIG. 11 illustrates a structure of adjacent two high voltage generators 1a shown in FIG. 10. The same structure is applied to the potential converters 5 and 5a shown in FIGS. 7 and 8, respectively.

The capacitors C71 of adjacent two charging circuits 71 are formed on n-type wells 82 isolated from each other in a p-type well of a silicon substrate 80. In detail, each capacitor C71 is a MOS-type capacitor having the n-type well 82 as a terminal and a gate electrode 84 formed on the n-type well 82 via a gate insulating film 83. The PMOS transistor QP71 is also formed in the n-type well 82 for coupling the capacitors C71 of adjacent two charging circuits.

It is apparent from the foregoing disclosure on operation, capacitance-coupling while the PMOS transistors QP71 is on ideally provides potentials on the n-type wells 82 as one of the terminals of the capacitors C71, accumulated by  $V_{DD}$  per well. In reality, however, the junction-capacitance between the n-type well 82 and the p-type well 80 is much larger than the capacitor C71 to restrict a coupling ratio. The number of charging circuits have to be decided in consideration of such restricted coupling ratio for obtaining a required boosted potential.

The PMOS transistors QP71 are switching devices for coupling the capacitors C71 of adjacent charging circuits. The source and drain of each PMOS transistor QP71 do not suffer voltage application higher than  $V_{DD}$ . The PMOS transistors QP71 thus can be arranged on a small area. The capacitors C71 also do not suffer voltage application higher than  $V_{DD}$ . Thus, an NMOS transistor-type capacitor C71 having an insulating film 83 thinner than the gate oxide film of the PMOS transistor QP71 will exhibit large capacitance on a small area. Therefore, the high voltage generator 1a including these transistors and capacitors can be integrated on a small area.

FIG. 12 illustrates a modification to the structure of the high voltage generator 1a shown in FIG. 10 for one charging circuit 71. The same structure can be applied to the potential converters 5 and 5a shown in FIGS. 7 and 8, respectively.

A difference between the structures in FIGS. 11 and 12 is that, in the latter, the PMOS transistor QP71 for coupling the

capacitors C71 of adjacent charging circuits is formed in an n-type well 82b isolated from an n-type well 82a by the p-type well 80 of the silicon substrate. Another difference is that the NMOS transistor QN71 is connected to the gate electrode of the capacitor C71 while the NMOS transistor QN72 is connected to the n-type well 82a, as opposite of FIG. 11.

This structure serves to restrict parasitic capacitance to the high-level side node N11 of the capacitor C71 less than to the low-level side node N12 thereof with respect to the low-level side power terminal  $V_{SS}$ .

Also in the structure shown in FIG. 12, the PMOS transistors QP71 are switching devices for coupling the capacitors C71 of adjacent charging circuits. The source and drain of each PMOS transistor QP71 do not suffer voltage application higher than  $V_{DD}$ . The PMOS transistors QP71 thus can be arranged on a small area. The capacitors C71 also do not suffer voltage application higher than  $V_{DD}$ . Thus, an NMOS transistor-type capacitor C71 having an insulating film 83 thinner than the gate oxide film of the PMOS transistor QP71 will exhibit large capacitance on a small area. Therefore, the high voltage generator 1 in FIG. 12 having these transistor and capacitors can be integrated on a small area.

As illustrated in FIG. 13, each capacitor C71 can be an NMOS FET formed in a p-type semiconductor region or an NMOS transistor having a negative threshold level.

The foregoing disclosure is applied to the potential converters 5 and 5a in FIGS. 7 and 8, respectively. In detail, the structure illustrated in FIG. 11, 12 or 13 is applied to the capacitors C11 and the PMOS transistors QP11 in FIGS. 7 and 8 with a gate insulating film of each capacitor C11 thinner than that of each PMOS transistor QP11 of small area, thus achieving overall integration in a small area.

FIG. 14 shows a modification to the high voltage generator 1 in FIG. 4.

A high voltage generator 1b shown in FIG. 14 has a plurality of capacitors C1 driven by opposite-phase clocks  $\phi$  and  $\phi$  and NMOS transistors QN that function as a diode to transfer charges stored in a capacitor C1 to the next one.

The first capacitor C1 is supplied with  $V_{DD}$  via the MOS transistor QN. Connected to a clock-supplying terminal of each capacitor C1 of the charge pump is the potential converter 5 shown in FIG. 7.

In detail, as shown in FIG. 15A, a potential converter may be formed as one unit of circuit that consists of a capacitor C2, NMOS transistors QN11 and QN12, and PMOS transistors QP11 and QP12, or, as shown in FIG. 15B, it may be formed as series connection of a plurality of (two in FIG. 15B) of unit of circuit.

A dielectric film of the capacitor C2 for the potential converter is preferably thinner than that of the capacitor C1 for the charge pump because the dielectric film of the capacitor C2 will not suffer voltage application higher than a power supply voltage.

The capacitor C2 of the potential converter 5 is charged while the NMOS transistors QN11 and QN12 are on. A drive potential  $V_{DD}$  is supplied to a low-level side terminal of the capacitor C2 whose other terminal is connected to an output terminal OUT when the NMOS transistors QN11 and QN12 are turned off whereas the PMOS transistors QP11 and QP12 are turned on. The output terminal OUT is reset by an NMOS transistor QN14 while the NMOS transistors QN11 and QN12 are on.

In FIG. 15B, the output PMOS transistor QP11 and the driving PMOS transistor QP12 are shared by adjacent two potential converters. In detail, the driving PMOS transistor

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QP12 of the potential converter 51-2 is used as an output transistor of the anterior potential converter 51-1 and the output PMOS transistor QP11 of the potential converter 51-2 is used as a driving transistor of the posterior potential converter 51-3 (not shown). The resetting NMOS transistor QN14 is provided only at the output terminal OUT of the last potential converter for several potential converters connected in series.

In the foregoing structure, the capacitor C2 of an even number stage of the potential converter 5 is coupled in series to the pumping capacitor C1 of the charge pump so that a clock potential boosted by the converter 5 is supplied to the capacitor C1 while the capacitor C1 of an odd number stage of the potential converter 5 is grounded.

On the other hand, the capacitor C2 of an odd number stage of the potential converter 5 is coupled in series to the pumping capacitor C1 of the charge pump so that a clock potential boosted by the converter 5 is supplied to the capacitor C1 while the capacitor C1 of an even number stage of the potential converter 5 is grounded. These two operations are repeated alternately.

According to these modifications, boosted clocks serve to decrease the number of charge pumps for obtaining the output level the same as that in the high voltage generator shown in FIG. 5.

In detail, the potential converter having the capacitance of the capacitor C2 the same as that of the capacitor C1 serves to decrease the number of charge pumps by  $\frac{1}{2}$  and  $\frac{1}{3}$  in FIGS. 15A and 15B, respectively.

The decrease in number of charge pumps allows a small area for the high voltage generator because a thin dielectric film can be used for the capacitor C2 of the potential converter 5 even though the total capacitance of the capacitors used in the high voltage generator is the same between the circuits shown in FIG. 5 and FIGS. 15A and 15B.

In FIGS. 15A and 15B, the NMOS transistors QN11, QN12 and QN14, and the PMOS transistors QP11 and QP12 are turned on in opposite phase. The timing for the NMOS transistors QN11, QN12 and QN14 to be turned off (or on) and that for the PMOS transistors QP11 and QP12 to be turned on (or off) may not meet each other completely. For example, the timing may be delayed a little bit so that the NMOS transistors QN11, QN12 and QN14 and the PMOS transistors QP11 and QP12 are not be turned on simultaneously, for prevention of punch-through current.

The high voltage generator 1 shown in FIG. 14 has charge pumps driven by two-phase clocks. However, it may have charge pumps driven by four-phase clocks shown in FIG. 16.

A high voltage generator 1c shown in FIG. 16 has NMOS transistors M1, the gate thereof being driven by clocks  $\phi 3$  and  $\phi 4$  instead of the transfer devices NMOS transistors QN shown in FIG. 14. The gate of each NMOS transistor M1 is not connected to its drain but to a capacitor C3 via which the clock  $\phi 3$  or  $\phi 4$  is applied. Each capacitor C3 is provided with a charging NMOS transistor M2, the drain thereof being connected to the capacitor C1, the gate thereof being connected to the succeeding capacitor C1.

An operation of the charge pumps shown in FIG. 16 is disclosed with reference to the timing chart illustrated in FIG. 17.

The capacitors C3 are charged via the NMOS transistors M2 during a period from moments t1 to t2 in which both clocks  $\phi 1$  and  $\phi 2$  are HIGH. Each odd number stage of the NMOS transistor M2 is turned off when the clock  $\phi 2$  is turned into LOW at the moment t2. When the clock  $\phi 3$  is turned into HIGH at a moment t3, a high voltage is supplied to the gate of each odd number stage of the NMOS transistor

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M1 via the capacitor C3, so that charges stored in each odd number stage of the capacitor C1 are transferred to the succeeding even number stage of the capacitor C1. When the clock  $\phi 3$  is turned into LOW at a moment t4, each odd number stage of the NMOS transistor M1 is turned off. Likewise, charges stored in each even number stage of the capacitor C1 is transferred to the succeeding odd number stage of the capacitor C1 while the clock  $\phi 4$  is HIGH during next cycle of the clocks  $\phi 4$  and  $\phi 2$ .

The four-phase control provides a voltage applied to the gate of each NMOS transistor M1 higher than that applied to the drain thereof, resulting no effects of substrate bias effect, thus achieving charge transfer efficiency higher than the two-phase control shown in FIG. 14.

The delay for the clock  $\phi 3$  that is turned into HIGH at the moment t3 after the clock  $\phi 2$  has been turned into LOW from the moment t2 is required for protecting the NMOS transistors M2 from a reverse current.

Moreover, the delay for the clock  $\phi 2$  that is turned into HIGH at a moment t5 after the clock  $\phi 3$  has been turned into LOW from the moment t4 is required for protecting the NMOS transistors M1 from a reverse current.

Like the embodiment shown in FIG. 14, the four-phase driven charge pumps are provided with the potential converter 5 shown in FIG. 15A or 15B for supplying a boosted potential to each capacitor C1, thus achieving decrease in the number of charge pumps.

FIG. 18 shows a circuit diagram of another embodiment of the potential detector shown in FIG. 4.

The potential detector in FIG. 4 is provided with one capacitor C2 to which a certain amount of charges stored in the capacitor C1 are supplied.

On the contrary, this embodiment is provided with a plurality of capacitors C2 for varying capacitance, or a ratio of charge distribution to the capacitors C1 and C2, to vary an output boosted potential.

In detail, the embodiment in FIG. 18 is provided with two capacitors C21 and C22 as the capacitors C2. Also provided are an NMOS transistor QN21 connected between the node N1 of the capacitor C1 and the node N2 of the capacitor C21 and an NMOS transistor QN22 connected between the node N2 of the capacitor C21 and the node N3 of the capacitor C22.

A ratio of charge distribution can be varied by driving the gate of the NMOS transistor QN 22 as follows:

When the gate of the NMOS transistor QN 22 is driven by a clock  $\phi$  via a switch 10 connected to this gate, the capacitor C22 is almost always discharged, so that it can be disregarded in operation. The NMOS transistor QN 22 functions as a resetting device for the capacitor C21 together with the NMOS QN3.

The output potential Vout of the high voltage generator 1 in this operation is expressed, like the expression (1), as follows:

$$V_{ref}(C1+C21)/C1 \quad (2)$$

Next, when the NMOS transistor QN 22 is turned on by supplying  $V_{DD}$  to the gate thereof via the switch 10, the two capacitors C21 and C22 are supplied with a certain amount of charges stored in the capacitor C1.

The output potential Vout of the high voltage generator 1 in this operation is expressed as follows:

$$V_{ref}(C1+C21+C22)/C1 \quad (3)$$

As disclosed, the potential detector in this embodiment switches the amount of capacitance to selectively output

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different level of potentials  $V_{out}$  at the output terminal 9 of the high voltage generator 1.

The second capacitor may consist of capacitors of three or more for switching output potential among levels of three or more.

The potential detector according to the present invention generates a potential to be input to a comparator, which is lower than a potential at a terminal to be detected with a potential-charging operation to a capacitor and a charge-distribution operation between the capacitor and another capacitor.

Different from the known potential detector with potential division by resistor, the potential detector according to the present invention generates no D. C. current. Moreover, the capacitor is formed with a large equivalent resistance but a small area, thus occupying a small area on the entire circuit area. The small area for the capacitor allows the potential detector to be almost free from leakage for stable potential detection with no delay in response which will occur when resistors of large resistance are used instead of capacitor.

Different from the known method of dividing an output potential of the high voltage generator by resistors, the high voltage generator according to the present invention requires the drive performance just for driving only the load with no decrease in response of the potential detector even at a large equivalent resistance, thus generating a constant boosted potential.

As disclosed, the present invention offers a potential detector capable of stable potential detection while consuming a low power. Moreover, the present invention offers a semiconductor circuit with the potential detector having an high voltage generator for generating a constant potential output.

What is claimed is:

1. A semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising:

a charge pump having a plurality of first capacitors, adjacent two first capacitors being driven by clocks in opposite timing and a transfer device for transferring

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charges stored in each first capacitor to the succeeding first capacitor; and

a potential converter for supplying a boosted clock to each first capacitor,

wherein the potential converter includes:

a second capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device;

a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the second capacitor;

a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the second capacitor to an output terminal; and

a fifth switching device that is turned on simultaneously with the first switching device to reset a potential at the output terminal,

wherein the second capacitor is charged while the first and the second switching devices are on and the charged second capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

2. The semiconductor integrated circuit according to claim 1, wherein the potential converter includes a plurality of circuits each having the second capacitor and the first, the second, the third, and the fourth switching devices, the circuits being connected in series such that the fourth switching device of each circuit is used as the third switching device of the succeeding circuit, the fifth switching device being provided at an output terminal of the last circuit among the series-connected circuits.

3. The semiconductor integrated circuit according to claim 1, wherein a dielectric film of the second capacitor is thinner than that of the first capacitor.

\* \* \* \* \*



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**Forbes et al.**

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(45) **Date of Patent:** **Aug. 6, 2002**

(54) **EFFICIENT CMOS DC-DC CONVERTERS  
BASED ON SWITCHED CAPACITOR  
POWER SUPPLIES WITH INDUCTIVE  
CURRENT LIMITERS**

(75) **Inventors:** **Leonard Forbes**, Corvallis, OR (US);  
**Kie Y. Ahn**, Chappaqua, NY (US)

(73) **Assignee:** **Micron Technology, Inc.**, Boise, ID  
(US)

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U.S.C. 154(b) by 0 days.

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(52) **U.S. Cl.** ..... **323/282; 363/59**

(58) **Field of Search** ..... **323/282, 272,  
323/222; 363/59, 60, 21**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,636,930 A	*	1/1987	Bingham et al.	363/60
4,999,761 A		3/1991	Bingham et al.	
5,396,527 A	*	3/1995	Schlecht et al.	327/530
5,400,235 A		3/1995	Carroll	
5,485,365 A	*	1/1996	Dan-Harry	363/132
5,680,300 A		10/1997	Szepesi et al.	
5,736,842 A	*	4/1998	Jovanovic	323/222
5,751,561 A	*	5/1998	Ho et al.	363/21.1
5,966,298 A	*	10/1999	Fischer	363/59

**OTHER PUBLICATIONS**

Moore; "Regulator topologies standardize battery powered systems"; *Electronic Design News (European Edition)*; vol. 39, No. 2, pp. 59-64, Jan., 20, 1994.

Sherman; "DC-DC conversion techniques for noise-sensitive applications"; *Electronic Design*, vol. 45, Nov. 17, 1997, 7 total pages.

Mino et al.; "A Compact Buck-Converter Using a ThinFilm Inductor"; *IEEE Power Electronics Conference and Expo.*, vol. 1, Part 1, Mar. 1996, pp. 422-426.

Mino et al.; "Switching Converter Using Thin-Film Microtransformer with Monolithically Integrated Rectifier Diodes"; *IEICE Trans. Electron.*, vol. E80-C, No. 6, Jun. 1997; pp. 821-827.

Matsumoto et al.; "Integration of a Power Supply for System-on-Chip"; *IEICE Trans. Fundamentals*, vol. E80-A, No. 2, Feb. 1997, pp. 276-282.

Moore; "Buck Regulator Answers Portable Challenges"; *Electronic Design*, vol. 46, No. 20, Sep. 1, 1998; pp. 128-134.

(List continued on next page.)

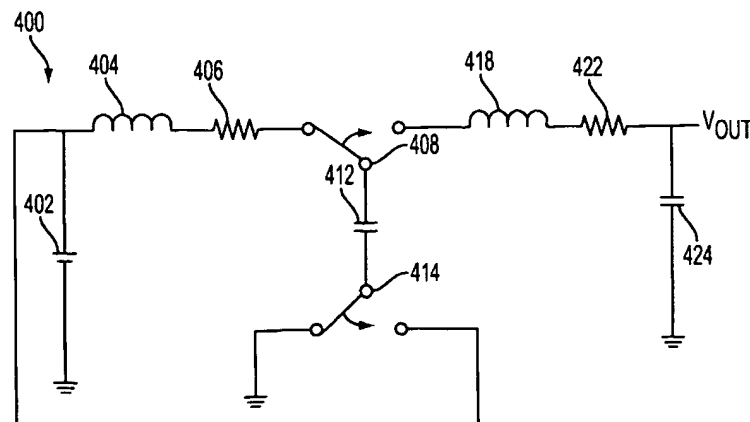
*Primary Examiner*—Rajnikant B. Patel

(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky, LLP

(57) **ABSTRACT**

A novel class of DC to DC power converters and a method of conversion is provided using high-frequency switched capacitors where the switches are implemented by CMOS transistors or diodes on an integrated-circuit chip and using inductors to limit charging current. High efficiency is achieved using inductors to reduce energy losses in circuit capacitors by high frequency switching when inductor current is zero and capacitor voltage is maximized. The high-frequency (100 MHz or greater) operation of the converter circuit permits the use of inductors with a low inductance value on the order of 100 nH ( $100 \times 10^{-9}$  Henrys) capable of fabrication directly on an integrated-circuit (IC) chip. The use of CMOS integrated components allows the entire converter to be formed on a single IC chip, saving significant space within the portable system. Output voltage and current is high enough to permit EEPROM programming. In addition, fluctuations in the output voltage (ripple voltage) are substantially eliminated when several of the converter circuits are used in parallel.

**108 Claims, 12 Drawing Sheets**



## OTHER PUBLICATIONS

Acik et al.; "Active Clamped ZVS Forward Converter with Soft-Switched Synchronous Rectifier for Maximum Efficiency Operation"; Proc. of 29<sup>th</sup> Annual IEEE Power Electronics Specialists Conference, Cat. No. 98CH36196, vol. 2, pp. 1237-1242, 1998, No date.

Dias et al.; "An Improved Self-Resonant PWM Forward Converter"; Proc of 13<sup>th</sup> Annual Power Electronics Conference and Exposition, vol. 2, pp. 620-625, 1998, No Date.

Xi et al.; "A Zero Voltage Switching Forward Converter Topology"; Proc. of 19<sup>th</sup> International Telecommunications Energy Conference, 1997, pp. 116-123, No Date.

Kim et al.; "An Improved Soft Switching Forward DC/DC Converter Using Energy Recovery Snubber"; Proc. of 19<sup>th</sup> International Telecommunications Energy Conference, 1997, pp. 46-49, No date.

Sun et al.; "Forward Converter Regulator Using PWM Controlled Transformer"; Proc. of the IEEE Power Electronics Specialists Conference, 1993, pp. 1116-1122, No Date.

Djekic et al.; "High Frequency Synchronous Buck Converter for Low Voltage Applications", Proc. of 29<sup>th</sup> Annual IEEE Power Electronics Specialists Conference, 1998, pp. 1248-1254, No date.

Tsukamoto et al.; "A Highly Efficient Buck Converter with Double-Anti-Crossover Synchronous Rectification Using a Newly Developed Control IC"; Proc. of 29<sup>th</sup> Annual IEEE Power Electronics Specialists Conference, 1998, pp. 1243-1247, No Date.

Matsuo et al.; "A Novel Soft-Switching Buck-Boost Type AC-DC Converter with High Power Efficiency, High Power Factor and Low Harmonic Distortion"; Proc. of 29<sup>th</sup> Annual IEEE Power Electronics Specialists Conference, vol. 2, 1998, pp. 1030-1035, No Date.

Berkovici et al.; "High Efficient PWM Zero-Voltage-Transition DC-DC Boost Converter"; Proc. of the 1998 IEEE International Symposium on Circuit and Systems, vol. 6, 1998, pp. 442-445, No date.

Shoyama et al.; "Voltage Resonant Buck-Boost Converter Using Multi-Layer-Winding Transformer"; Record of 20<sup>th</sup> Annual IEEE Power Electronics Specialists Conference, vol. 2, 1989, pp. 895-901, No date.

Martino et al.; "An On-Chip Back-Bias Generator for MOS Dynamic Memory"; IEEE Journal of Solid-State Circuits, vol. SC-15, No. 5, Oct. 1980, pp. 820-826.

Gillingham; "High Speed Charge-Pump"; IBM Technical Disclosure Bulletin, vol. 27, No. 29, Feb. 1985, pp. 5407-5409.

Tanzawa et al.; "A Quick Boosting Charge Pump Circuit for High Density and Low Voltage Flash Memories", 1994 Symposium on VLSI Circuits Digest of Technical Papers, pp. 65 and 66, No Date.

Monna, et al, "Charge Pump For Optimal Dynamic Range Filters", Proc. of 1994 IEEE Int. Symposium on Circuits and Systems, vol. 5, pp. 747-750, 1994, No Date.

Wang, et al, "Efficiency Improvement In Charge Pump Circuits", IEEE Journal of Solid-State Circuits, vol. 32, No. 6, pp. 852-860, 1997, No Date.

Favrat, et al, "A New High Efficiency CMOS Voltage Doubler", Proc. Of the IEEE 1997 Custom Integrated Circuits Conference, pp. 259-262, 1997, No Date.

Favrat, et al., "A High-Efficiency CMOS Voltage Doubler", IEEE J. Solid-State Circuits, vol. 33, No. 3, pp. 410-416, Mar. 1998.

Yoon, et al, "Charge pump boosting technique for power noise immune high-speed PLL implementation", Electronics Letters, vol. 34, No. 15, pp. 1445-1446, Jul. 1998.

\* cited by examiner

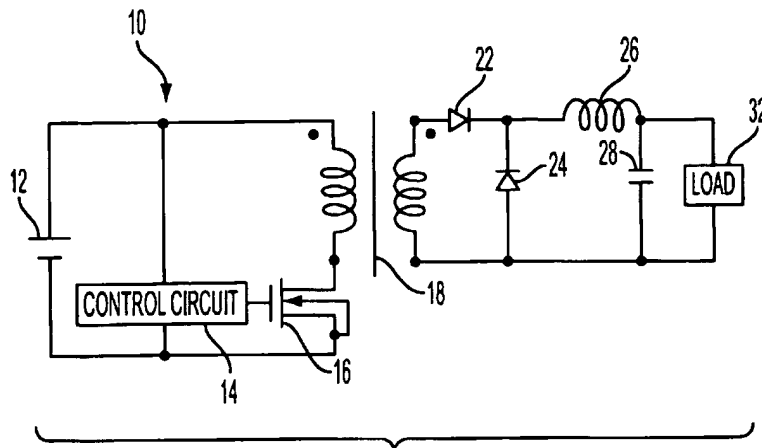


FIG. 1(a)  
(PRIOR ART)

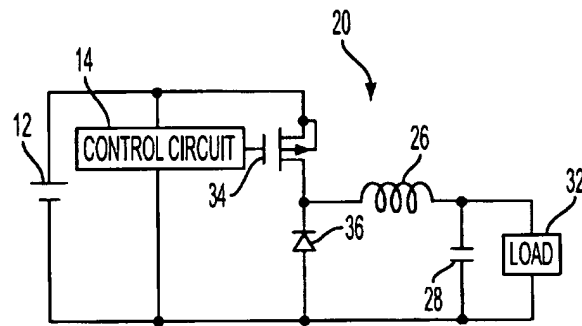


FIG. 1(b)  
(PRIOR ART)

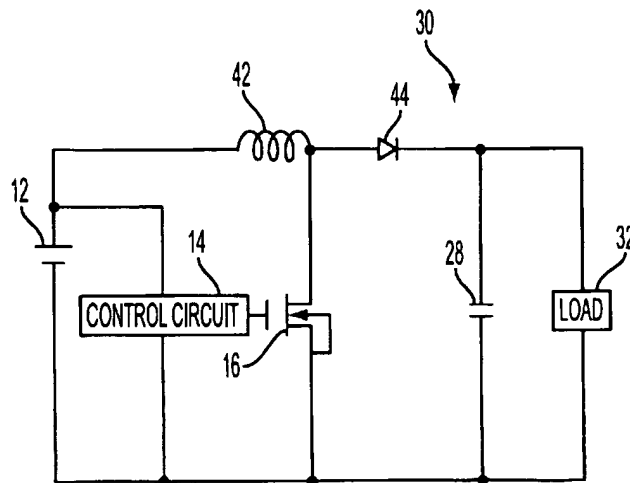
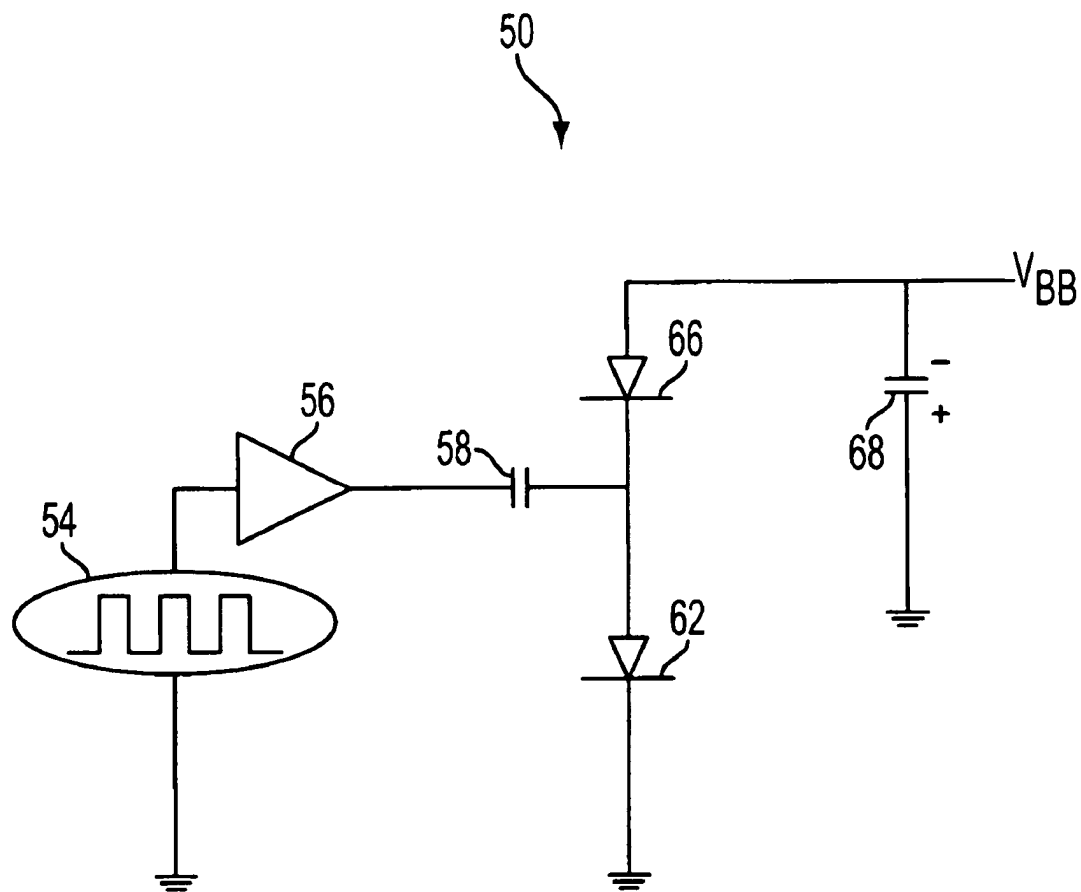


FIG. 1(c)  
(PRIOR ART)





**FIG. 2**  
(PRIOR ART)

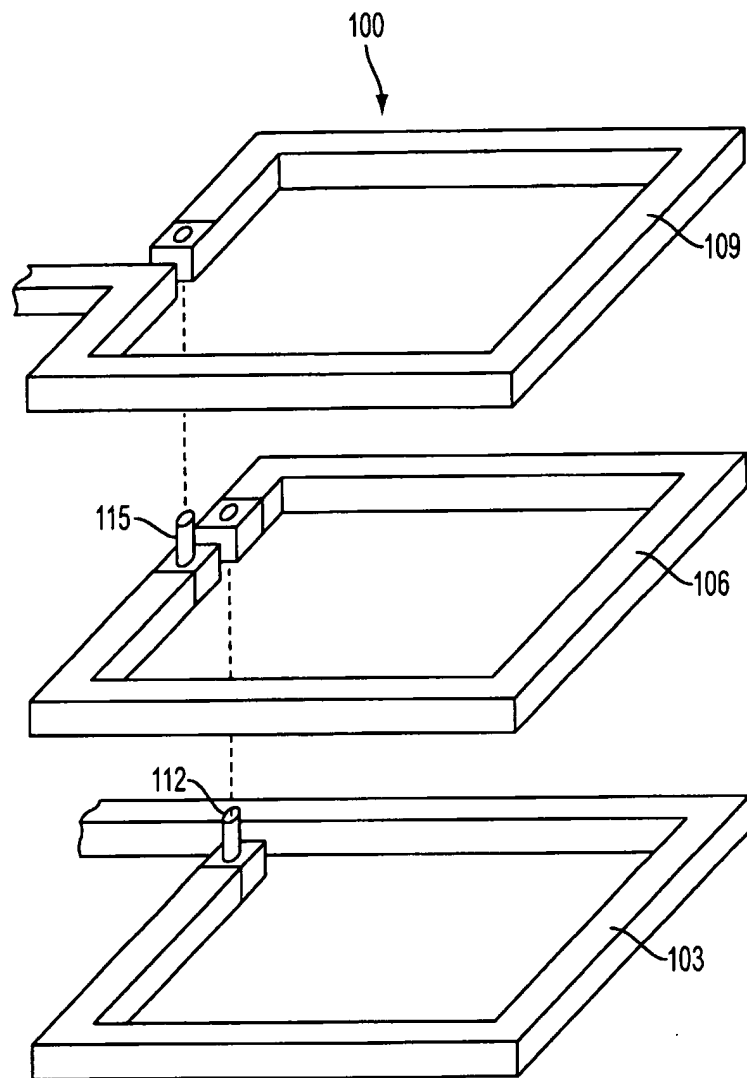


FIG. 3(a)

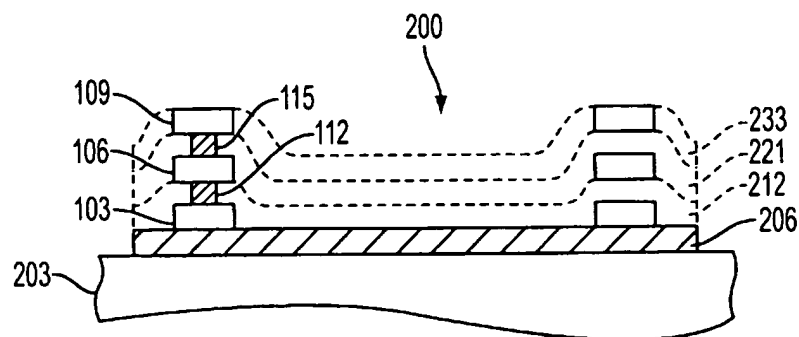


FIG. 3(b)

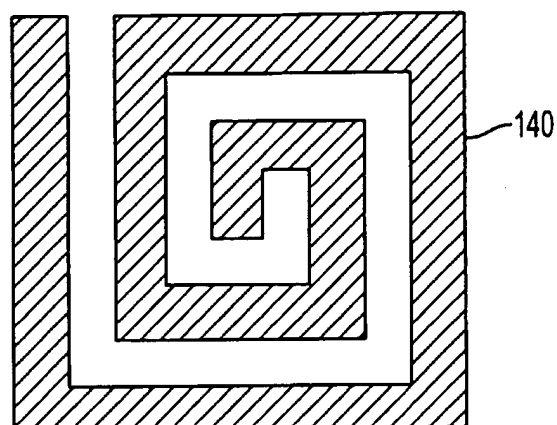


FIG. 3(c)

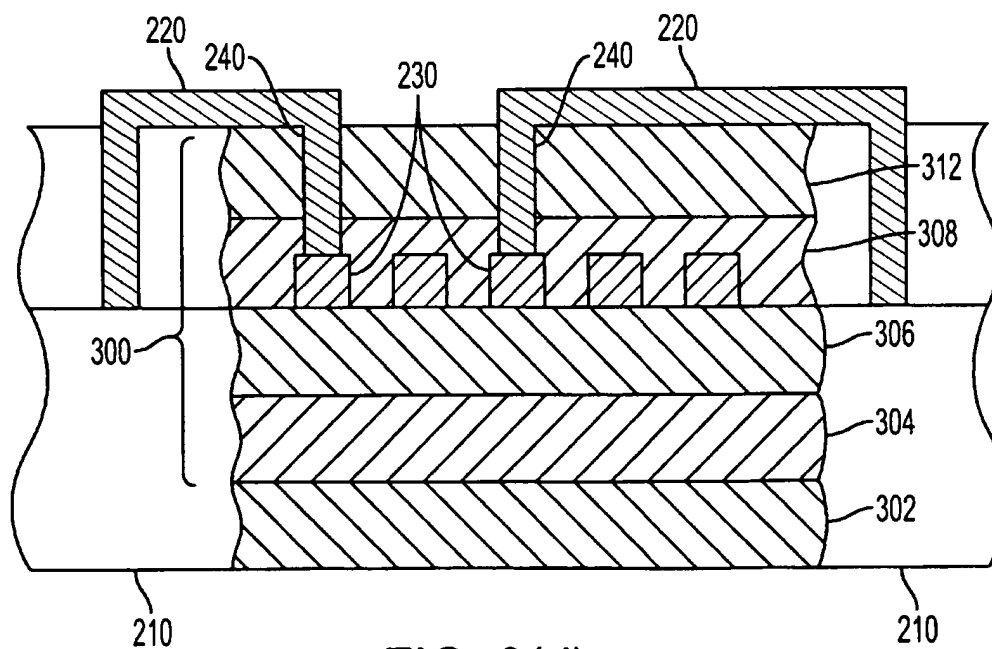


FIG. 3(d)

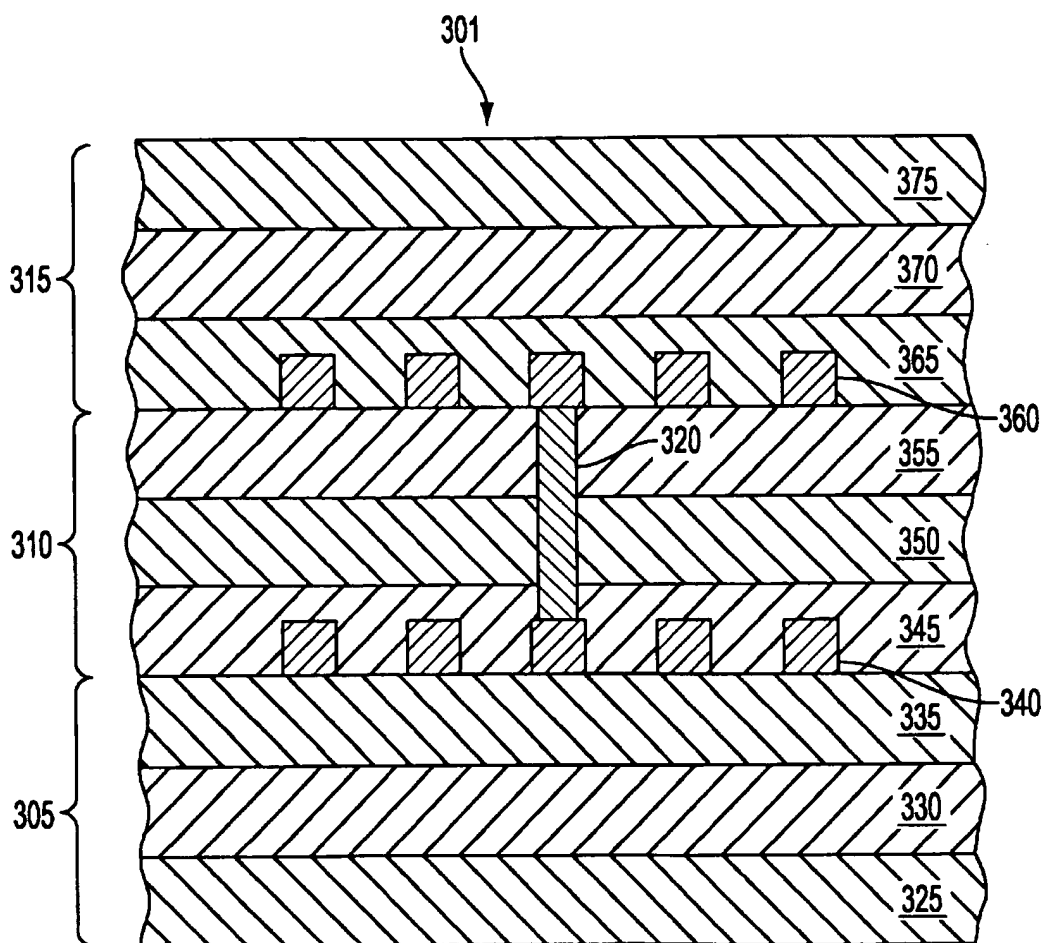


FIG. 3(e)

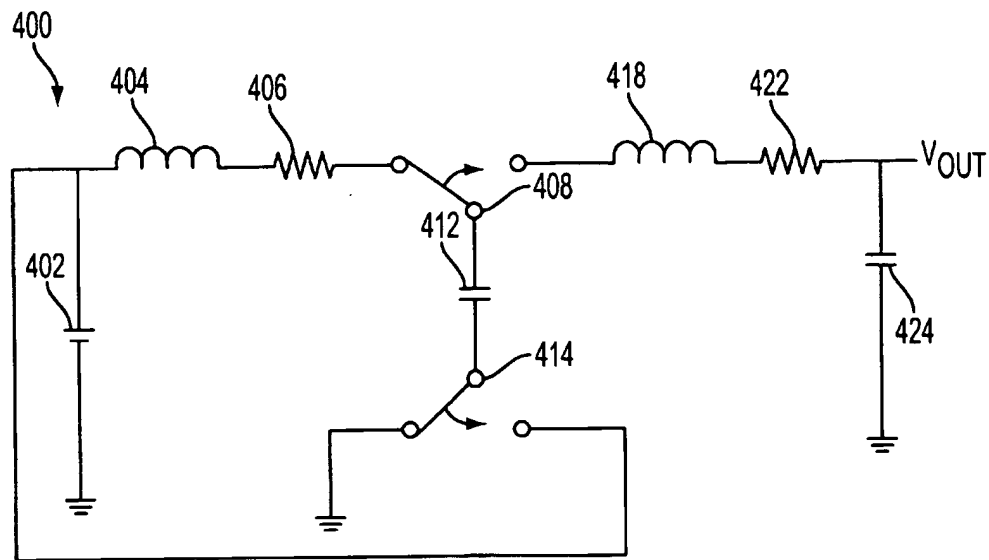


FIG. 4(a)

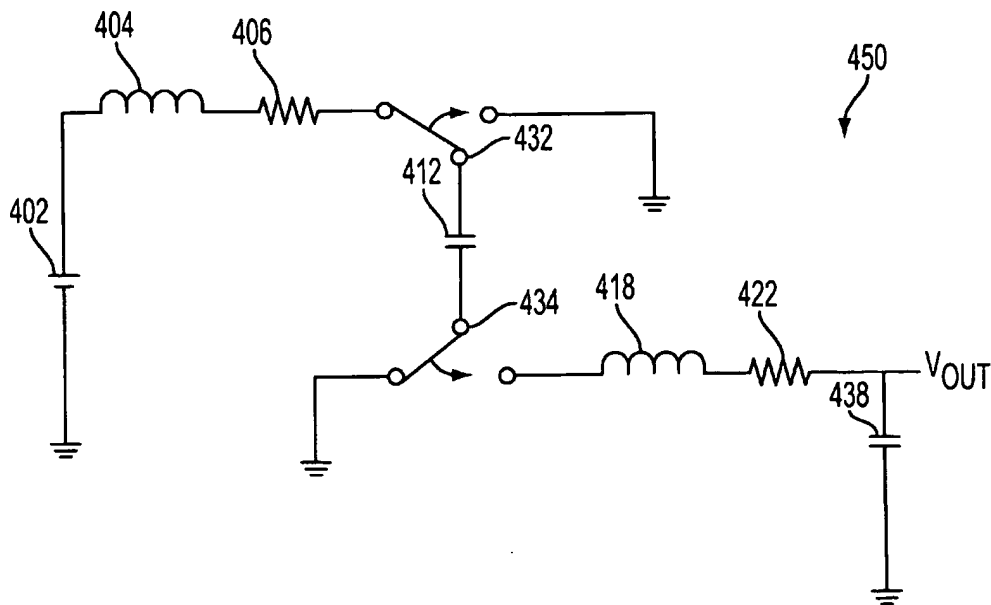


FIG. 4(b)

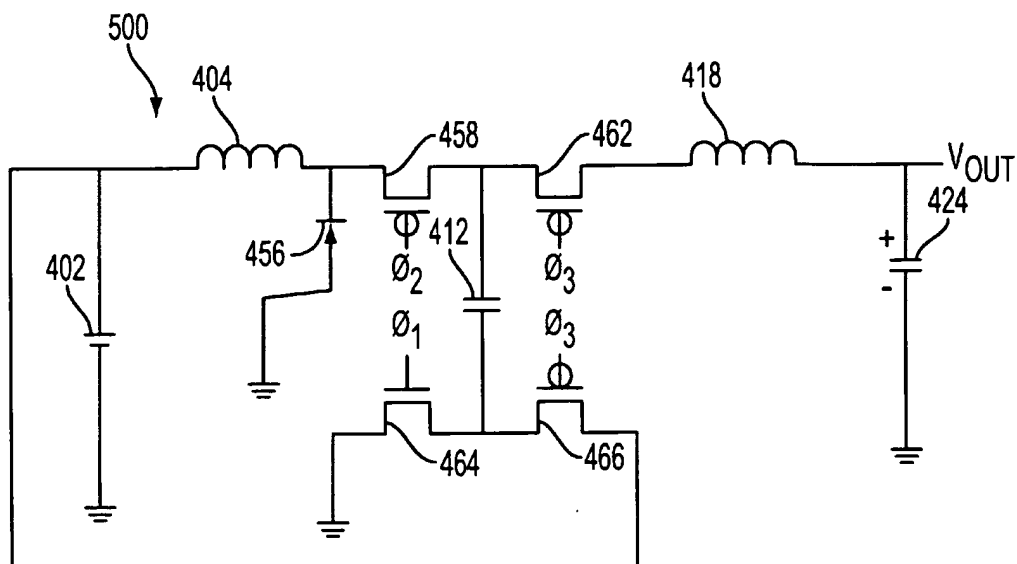


FIG. 5

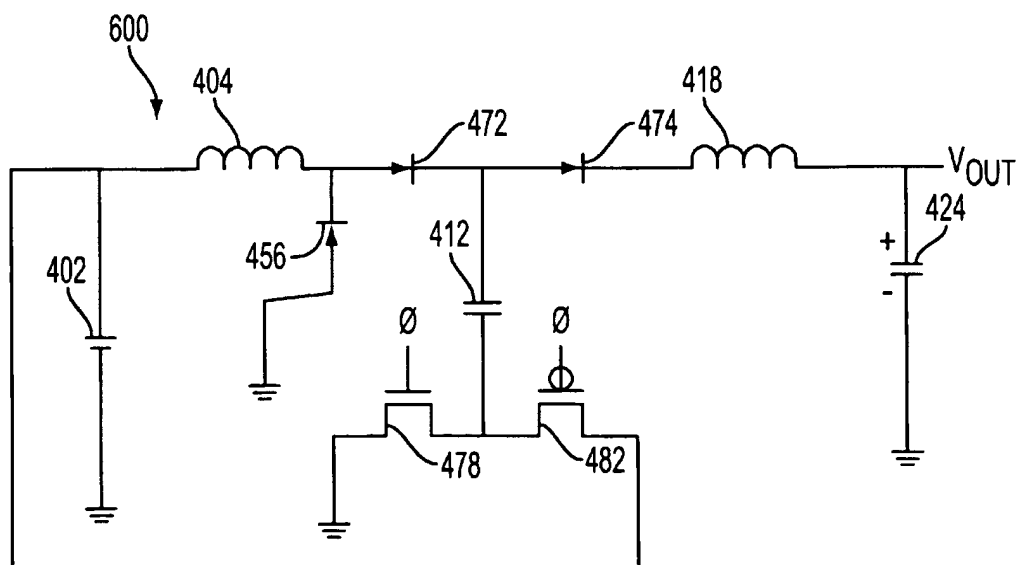


FIG. 6

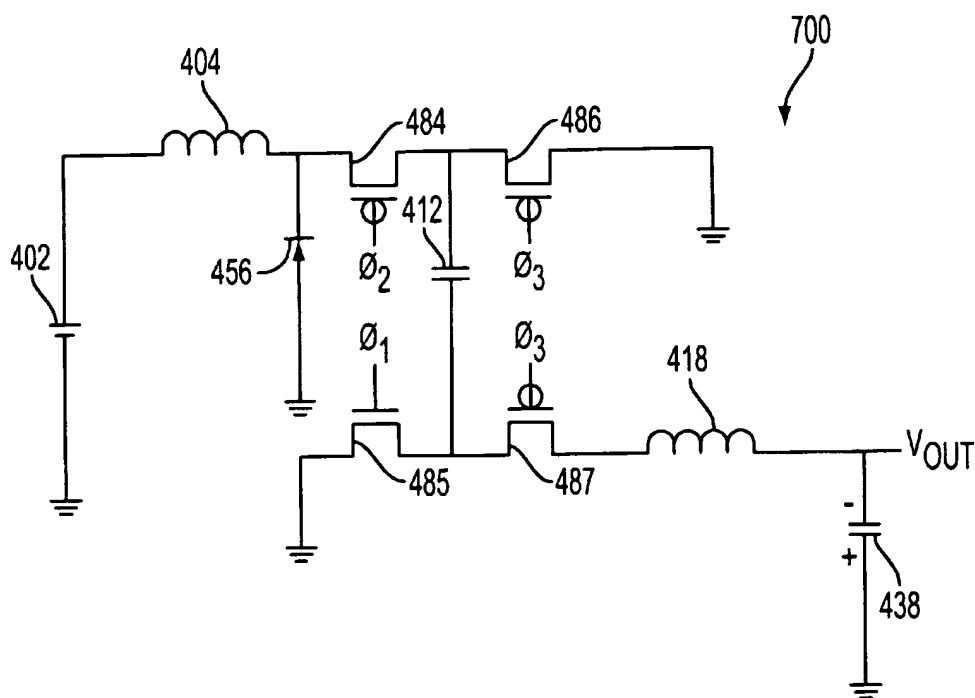


FIG. 7

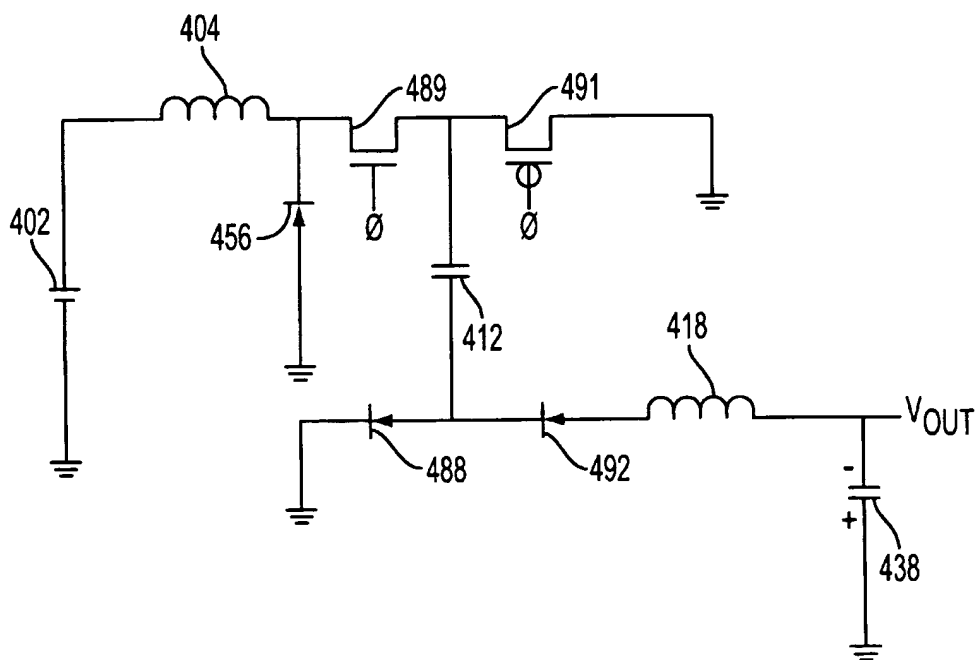


FIG. 8

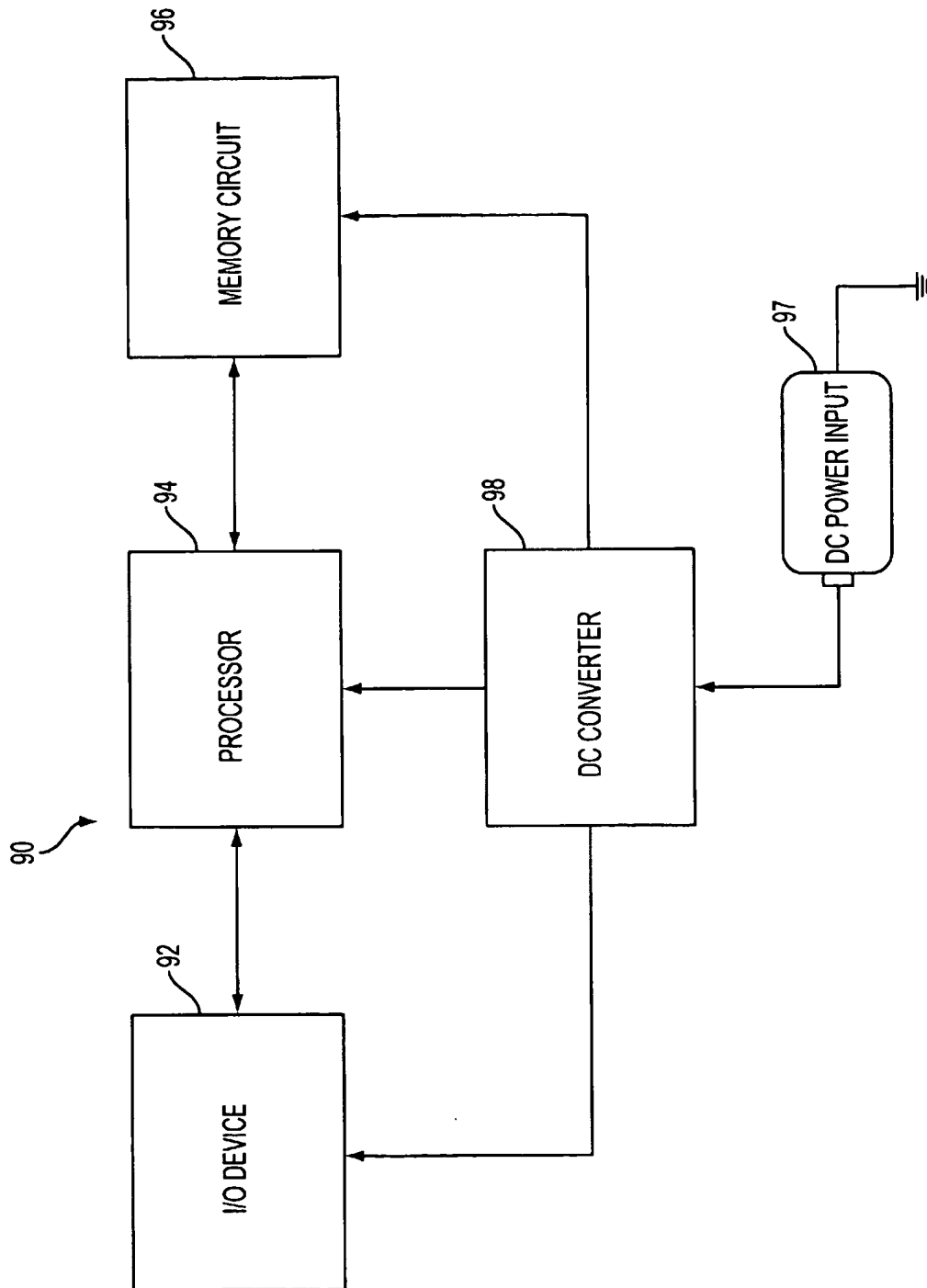


FIG. 9



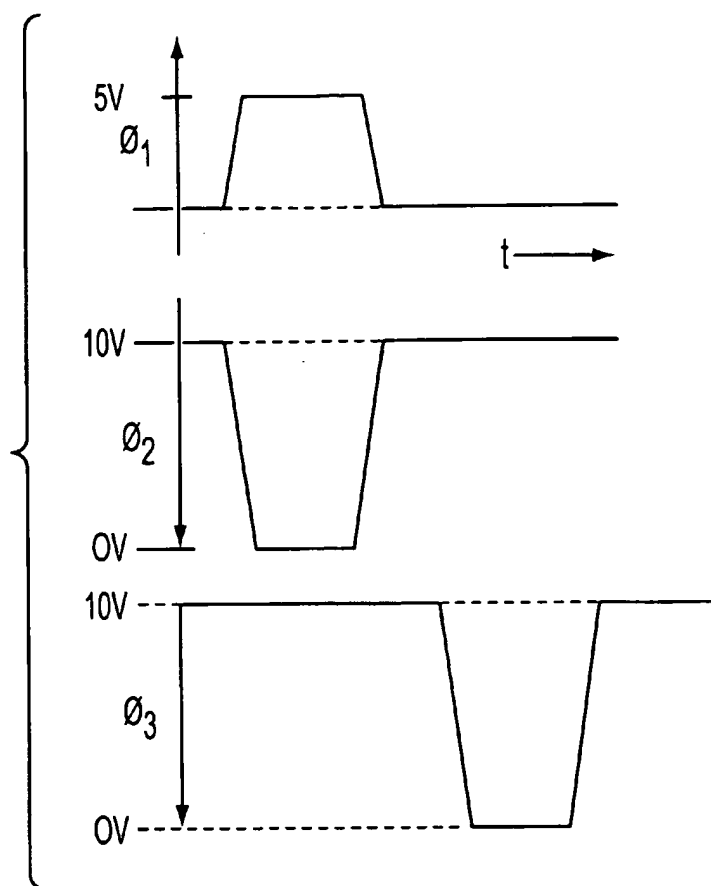


FIG. 10

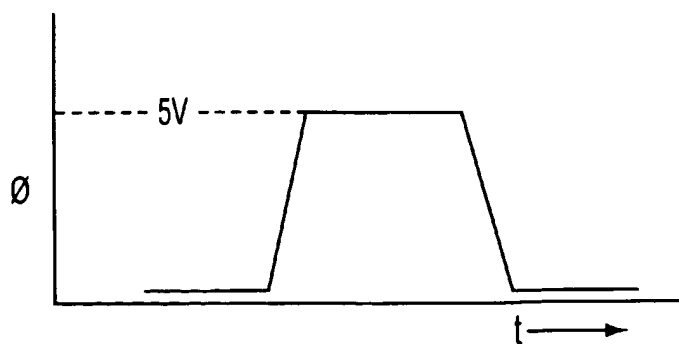


FIG. 11

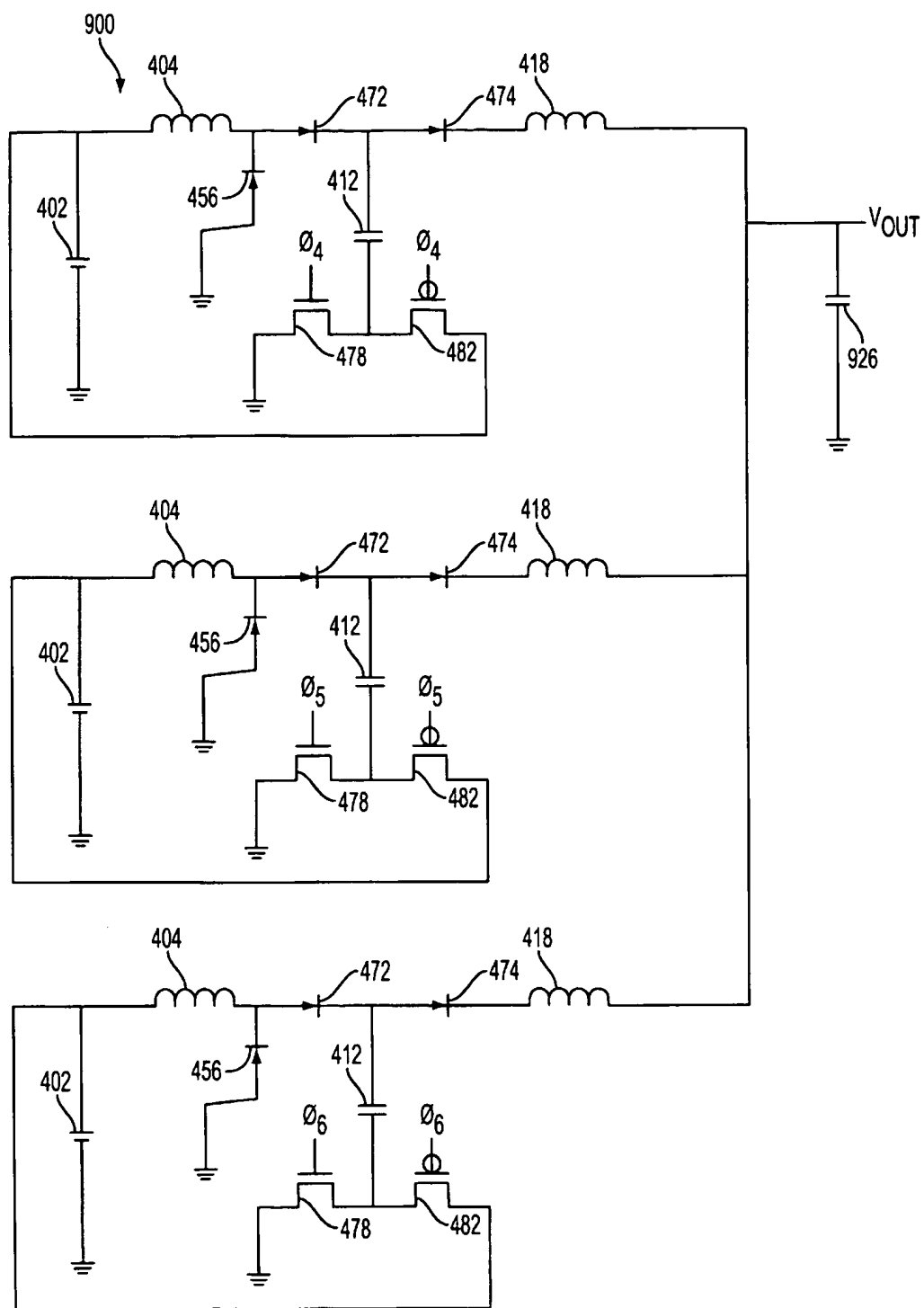


FIG. 12

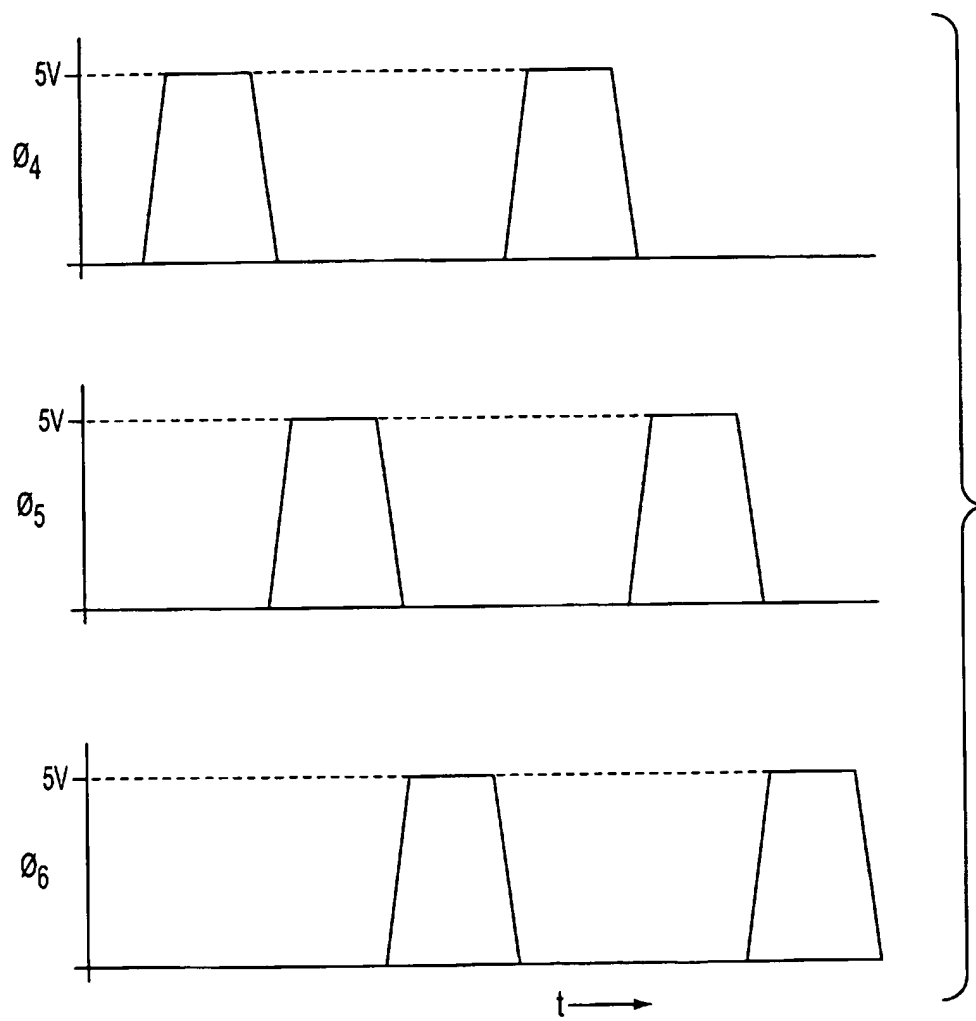


FIG. 13

# EFFICIENT CMOS DC-DC CONVERTERS BASED ON SWITCHED CAPACITOR POWER SUPPLIES WITH INDUCTIVE CURRENT LIMITERS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to the field of electronic systems which require power at more than one voltage, and more particularly, to a DC to DC power converter utilizing switched capacitors and inductive current limiters to achieve high efficiency.

### 2. Description of the Related Art

The evolution of electronic devices from analog to digital circuitry has changed the power supply requirements for circuit components. Yesterday's analog systems typically required a multitude of supply voltages, whereas today's digital systems typically use power at only a few standard voltages such as  $\pm 5V$  or  $3.3V$ . By reducing the number of supply voltages required, system designs benefit through lower cost, lighter weight, reduced volume and higher reliability due to the reduction in the number of power supply components.

In spite of this evolution in electronics, there are still a significant number of systems which require power at voltages in addition to the standard digital  $5V$  or  $3.3V$  levels. For example, systems which include data communication circuits often require negative voltages for compatibility with the Electronic Industries Association (ELA) RS232C interface, a popular interface for data communications, which requires voltage levels ranging from  $-25V$  to  $+25V$ . Furthermore, preamplifiers, required for many interfacing applications, often require a negative supply voltage in addition to a positive supply voltage which is greater than the standard digital voltage of  $5V$ .

In order to satisfy the need for several different supply voltages in digital systems, DC to DC power converters are used to produce output voltages different from the standard input voltage. These converters are available in step-down configurations that reduce the voltage relative to the input, step-up configurations that increase the voltage relative to the input, and inverter configurations that reverse the polarity of the input voltage (e.g.  $+5V$  input results in  $-5V$  output) and may be combined with either step-up or step-down configurations.

For computer system applications, DC to DC converters often operate in a low voltage, high-frequency switched environment. The explosive growth in the field of portable electronic devices, such as portable telephones, radio pagers, and notebook computers, has created a need for DC to DC converters which consume a minimum amount of power and take up as little space in the device as possible. Because batteries are the main power source for these portable devices, low-voltage circuitry is used to reduce power consumption and extend battery life. Battery energy is further saved by using a distributed power supply system with a switched controller which turns the individual converters on and off as they are needed.

Additional advantages with distributed systems can be achieved using controllers and converters which operate at a high frequency. Miniaturized electronics which typically operate at frequencies in the range of  $100\text{ MHz}$  or more, such as semiconductor integrated-circuit devices, save significant amounts of space and weight in portable systems. These devices also can operate at low voltage and power

consumption levels. In addition, improved thermal management and higher power densities as compared to conventional electronics makes integrated-circuit devices a natural choice for portable systems.

One circuit element frequently used in DC to DC converters is the inductor. Inductors are commonly used in the forward, buck (step-down) and boost (step-up) converters shown in FIGS. 1(a), 1(b) and 1(c), respectively (discussed below in more detail). Because conventional converters require inductors with an inductive value on the order of  $1\text{ micro-Henry}$  ( $1 \times 10^{-6}\text{ H}$ ), the inductor used is typically bulky and expensive, and is attached externally to the semiconductor chip which contains the remainder of the converter circuit. Inductors capable of integration on a semiconductor chip are available, but only for lower inductance values. Therefore, there is a need for converter circuits that use low-inductance-value integrated inductors permitting inclusion of all converter components in a single semiconductor chip.

Another common approach for producing additional voltages, that is particularly suited for low-power applications, is the "charge pump" or "flying capacitor" voltage converter. Referring to FIG. 2, an inverting charge pump 50 operates by charging a "pump" capacitor 58 during a clock's first half-cycle, or "pumping phase," to the level of a source voltage 54 via amplifier 56. During the clock's second, non-overlapping half-cycle, or "transfer phase," the pump capacitor 58 is disconnected from the source 54 and connected, with its polarity switched, to a second "reservoir" capacitor 68, thereby "pumping" charge to the reservoir capacitor 68 and providing an output  $V_{BB}$  which is approximately the negative of the input voltage.

With a minor rearrangement of the pump's switching elements, a step-up converter is produced. During the clock's first half-cycle the pump capacitor is charged to the level of the source voltage. During the clock's second half-cycle, the pump capacitor's positive side is disconnected from the source, and its negative side, which had been connected to ground during the first half-cycle, is connected to the source. The positive side, now at twice the source voltage, is connected to the reservoir capacitor, thus charging it to twice the source voltage. This 'doubled' voltage at the reservoir capacitor is then used as a power supply to components requiring the doubled voltage.

Charge pumps are limited in their voltage ranges and ability to supply large currents. Large currents are required to reprogram electrically-erasable programmable read-only memory (EEPROM) arrays, making charge pumps unsuitable for these increasingly popular devices. Conventional forward, buck, and boost converters require large-inductance inductors and/or transformers which are difficult or impossible to fabricate on integrated circuits, increasing the size of the converter.

In addition to size, current and voltage ranges, efficiency is also an important aspect of DC to DC converter performance. All DC to DC converters will dissipate a portion of the input energy in the circuit components, for example some energy is dissipated as heat in each resistor. Greater component losses result in reduced efficiency of the converter. In general, greater current magnitudes over time in the circuit result in greater losses in circuit components and hence lesser efficiency. Also, the use of multiple clocks for switching transistors also dissipates energy and reduces efficiency.

Therefore, there is a desire and need for efficient DC to DC converters suitable for use in small portable electronic

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systems which operate at high frequency and are capable of producing a current output sufficient for EEPROM programming and a range of voltages sufficient to meet various system requirements.

### SUMMARY OF THE INVENTION

The present invention provides a novel class of DC to DC converters based on switched capacitors suitable for use in portable electronic devices that offers improved efficiency, smaller size, and other advantages over conventional converters.

The above and other features and advantages of the invention are achieved by providing a DC to DC power converter circuit using switched capacitors where the switches are implemented by CMOS transistors or diodes on an integrated-circuit chip and using inductors to limit charging currents. The inductors can be fabricated directly on the CMOS integrated circuit or alternatively could be small inductors incorporated in the packaging. The high-frequency operation (100 MHz or greater) of the converter circuit permits the use of inductors with a low inductance value on the order of 100 nH ( $100 \times 10^{-9}$  Henrys) capable of fabrication directly on an integrated-circuit (IC) chip. The use of CMOS integrated components allows the entire converter to be formed on a single IC chip, saving significant space within the portable system.

Although the limit on charging current imposed by the inductor improves the efficiency of the converter by avoiding certain energy losses in the charging capacitor, the output current of the converter is not so limited as in prior designs, allowing the provision of a high output current for EEPROM reprogramming.

The present invention also provides reduced fluctuations in the power supply output voltage (ripple voltage) when several circuits are used in parallel to charge a single capacitor.

Furthermore, an embodiment of the present invention allows some transistor switches to be replaced with diodes to simplify the circuit and improve efficiency by removing the necessity for multiple switching clocks.

### BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will become more apparent from the detailed description of the preferred embodiments of the invention given below with reference to the accompanying drawings in which:

FIG. 1(a) shows a schematic diagram of a prior art single-ended forward converter;

FIG. 1(b) shows a schematic diagram of a prior art buck (step-down) converter circuit;

FIG. 1(c) shows a schematic diagram of a prior art boost (step-up) converter circuit;

FIG. 2 shows a schematic diagram of a prior art charge pump circuit;

FIG. 3(a) illustrates an exploded perspective view of an integrated circuit solenoidal inductor which may be used in the present invention;

FIG. 3(b) illustrates a fragmentary vertical cross-sectional view of the integrated circuit solenoidal inductor of FIG. 3(a);

FIG. 3(c) illustrates a top view of an integrated circuit spiral inductor which may be used in the present invention;

FIG. 3(d) illustrates a fragmentary vertical cross-sectional view of the integrated circuit spiral inductor of FIG. 3(c);

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FIG. 3(e) illustrates a fragmentary vertical cross-sectional view of an alternate arrangement of an integrated circuit spiral inductor which may be used in the present invention;

FIG. 4(a) shows a schematic diagram of a positive output DC to DC converter formed in accordance with a first embodiment of the present invention;

FIG. 4(b) shows a schematic diagram of a negative output DC to DC converter formed in accordance with a second embodiment of the present invention;

FIG. 5 shows a schematic diagram of the positive output DC to DC converter of FIG. 4(a) with transistors used for the switches;

FIG. 6 shows a schematic diagram of the positive output DC to DC converter of FIG. 4(a) with diodes and transistors used for the switches;

FIG. 7 shows a schematic diagram of the negative output DC to DC converter of FIG. 4(b) with transistors used for the switches;

FIG. 8 shows a schematic diagram of the negative output DC to DC converter of FIG. 4(b) with diodes and transistors used for the switches;

FIG. 9 is a block diagram of a processor-based system including a DC to DC converter formed in accordance with the present invention;

FIG. 10 is a phase/clock timing diagram for the DC to DC converters shown in FIGS. 5 and 7;

FIG. 11 is a phase/clock timing diagram for the DC to DC converters shown in FIGS. 6 and 8;

FIG. 12 shows a schematic diagram of a positive output DC to DC converter formed in accordance with a third embodiment of the present invention using several DC to DC converter circuits connected in parallel; and

FIG. 13 is a phase/clock diagram for the DC to DC converter of FIG. 12.

### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The terms "wafer" and "substrate" are used interchangeably and are to be understood as including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. While the embodiments described herein are generally directed toward a +5V or lower input digital system based on one micron ( $1 \times 10^{-6}$  meters) technology, the inventive concepts are equally applicable to integrated circuit technologies with other dimensions and power supply voltages.

FIGS. 1(a)–(c) illustrate three types of typical DC to DC power supply converters used in electronic devices as a source of DC power. FIG. 1(a) shows a single ended forward converter 10 in which the input DC power 12 is chopped by a control circuit 14 at a control transistor 16 to form a series of DC pulses which can be stepped up or down using a transformer 18 and then rectified by first and second rectifiers 22 and 24. An inductor 26 and capacitor 28 are used to smooth out ripples in the output voltage, which is used to power a load 32.

FIG. 1(b) shows a typical buck converter 20. A control transistor 34 is in series with the load 32 and the input

voltage can only be stepped down. The control circuit 14 and the control transistor 34 chop the input DC power 12, and the chopped voltage is filtered by inductor 26, which operates as a choke, and capacitor 28. The diode 36 clamps the chopped voltage to maintain positive polarity.

FIG. 1(c) shows a typical boost converter 30. A control transistor 16 is connected to the input DC power 12 with an inductor 42, and when the input voltage is chopped by the control circuit 14, an alternating flyback voltage is generated. This flyback voltage is higher than the input voltage when rectified by diode 44 and filtered by the capacitor 28. This boost converter 30 can only step up the output voltage to power the load 32.

An alternate means known in the art of providing a limited range of voltages used in electronic equipment is the charge pump circuit 50, illustrated in FIG. 2. An oscillator or ring oscillator circuit 54 drives the charge pump capacitor 58 through an amplifier 56. On the positive-going edge of the oscillator 54 waveform, the capacitor 58 charges through the diode 62 to a ground potential. On the negative-going edge of the oscillator 54 waveform, the capacitor 58 is driven to a negative voltage and the diode 66 conducts, charging the output capacitor 68 to a negative output voltage,  $V_{BB}$ . This output  $V_{BB}$  is used as a back bias power supply or to convert logic pulses to current pulses for phase-locked loop (PLL) circuits.

The present invention combines elements from both conventional DC to DC converter circuits and charge pump circuits to create a new class of DC to DC converters. FIG. 4(a) shows a first embodiment of the invention in which a switched capacitor 412 is arranged in a positive-output boost converter configuration (discussed below in more detail). This configuration is used to step up the voltage level of source 402 while preserving the polarity of the input DC power source (e.g., +5V input is stepped up to +9V output). The present invention is not limited to boost converters or non-inverting converters. FIG. 4(b) shows a second embodiment of the invention in which a switched capacitor is arranged in a negative output (inverting) buck converter configuration in which the output voltage is lesser in magnitude and reversed in polarity (e.g., +5V input is stepped down and inverted to -3.3V output relative to the voltage level of DC source 402). The switched capacitor design common to all embodiments of the present invention can also be used in other configurations allowing any combination of voltage level and polarity output relative to a voltage level and polarity of a DC source.

Referring to the positive output boost converter 400 of FIG. 4(a), DC power source 402 is connected through an inductor 404 having an associated inductive resistance 406 to one pole of switch 408. Switch 408 connects inductor 404 to capacitor 412 or alternately connects capacitor 412 to an output filter including inductor 418 having an associated resistance 422 and, between resistance 422 and ground, capacitor 424. Switch 414 connects the opposite plate of capacitor 412 to ground or alternately to DC power source 402. Switches 408 and 414 alternate between states at a frequency of about 100 MHz or more. The output voltage  $V_{out}$  is the potential difference across the capacitor 424 and is used to power an external electronic component.

During the 'charging phase,' the capacitor 412 is charged through inductor 404 and associated resistance 406 by DC power source 402 when switches 408 and 414 are set to connect these components through to ground potential in the manner illustrated in FIG. 4(a). Thereafter, switches 408 and 414 change to a "transfer" state to connect DC power source

402 directly to the lower plate of capacitor 412 while the upper plate of capacitor 412 is connected to capacitor 424 through inductor 418 and associated resistance 422, thereby charging capacitor 424 to the output voltage  $V_{out}$ . The output voltage  $V_{out}$  is approximately doubled from the input voltage at DC power source 402, as the voltage from source 402 adds to the voltage previously stored on capacitor 412 to charge capacitor 424. The inductor 418, associated resistance 422 and capacitor 424 also act as an output filter smoothing out any ripples in the output voltage  $V_{out}$ .

In addition, if switches 408 and 414 are set to change states when the inductor 404 current reaches zero and the voltage across the capacitor 412 is at a maximum, no stored energy will be lost in the inductor 404. By setting the frequency of all switches according to this scheme, a low-inductance inductor of approximately 100 nH can be used for inductor 404 with high frequency switches 408, 414 operating at 100 MHz or more to minimize energy loss and improve the efficiency of the converter.

FIG. 4(b) shows a schematic diagram of a negative output DC converter 450. DC power source 402 is connected through inductor 404 having associated resistance 406 to one pole of switch 432. An upper plate of capacitor 412 is also connected to switch 432 and the lower plate is connected to switch 434. Switch 432 connects inductor 404 to capacitor 412 or alternately connects capacitor 412 to ground. Switch 434 connects the capacitor 412 to ground or alternately connects capacitor 412 to an output filter including an inductor 418, associated resistance 422 and a capacitor 438. Capacitor 438 is connected between resistance 422 and ground. The output voltage  $V_{out}$  is the potential difference across the capacitor 438 and is used to power an external electronic component.

The negative output DC converter 450 shown in FIG. 4(b) operates to produce an output voltage  $V_{out}$  reversed in polarity relative to the voltage of the input DC source 402. During the 'charging phase,' capacitor 412 is charged through the inductor 404 and associated resistance 406 by DC power source 402 when switches 432 and 434 are set to connect these components through to a ground potential. Thereafter, switches 432 and 434 change to a transfer state to connect the upper plate of capacitor 412 directly to a ground potential and the lower plate of capacitor 412 to the output filter including capacitor 438, inductor 418 and associated resistance 422. This causes capacitor 438 to charge to a voltage which is opposite in polarity to the source voltage 402, i.e. to a negative voltage. The output voltage  $V_{out}$  smoothed by the output filter, is thus reversed in polarity from the input voltage to the converter from source 402. Similar to the positive output converter, the frequency of the switches 432, 434 is set according to the inductance value of the inductor 404 to minimize energy loss and improve efficiency.

The switches 408 and 414 in FIG. 4(a) and switches 432 and 434 in FIG. 4(b) change states in response to external clock signals generated by an external controller which is analogous to the control circuit 14 in the conventional boost converter 30 shown in FIG. 1(c). The clock signals are sent to each switch periodically in accordance with a clock frequency of a constant value.

Because modern integrated circuit switches are designed to operate at frequencies of 100 MHz or more, the inductance value of the inductors 404, 418 required in the present invention is significantly lower than conventional converters which generally operate at a lower frequency. Inductance values on the order of micro Henrys ( $1 \times 10^{-6}$  H) or higher are

required for conventional forward, buck, or boost converters. Such large inductors and/or transformers (for forward converters) are not compatible with CMOS integrated circuit processing. However, due to its high frequency operation, the present invention requires inductance values on the order of 100 nH ( $100 \times 10^{-9}$  H), a difference of a factor often, which may be fabricated directly on a CMOS integrated circuit.

FIGS. 5 and 6 show schematic diagrams of two different specific implementations of the positive output converter depicted in FIG. 4(a). FIG. 5 shows a DC to DC converter 500 which is essentially the same as that depicted in FIG. 4(a), but with transistors 458, 462, 464, 466 used as the switches 408, 414 of FIG. 4(a). Switches 458, 462, 464, and 466 change states according to a three component clocking scheme represented by clock signals  $\phi_1$ ,  $\phi_2$ ,  $\phi_3$ , the timing of which is shown in FIG. 10. The implementation shown in FIG. 5 requires multiple clocks, increasing circuit complexity and consuming circuit power, hence reducing the efficiency of the converter. Diode 456 is a clamping diode which provides a closed path for any residual currents in inductor 404 and prevents large negative voltages at the switch 458 when the switch 458 turns off. Also, if the inductors 404 and 418 are integrated inductors, such as those illustrated in FIGS. 3(a)–(e), the entire converter 500 shown in FIG. 5 may be fabricated on a single integrated circuit chip.

One technique to increase the efficiency of the converter is to replace some of the transistor switches with diodes, which conduct in only one direction and will function as switches for the circuit of the present invention. FIG. 6 shows a modification of the output DC boost converter of FIG. 5, where switches 458 and 462 of FIG. 5 have been replaced with diodes 472 and 474. Diodes are simpler devices than transistors, requiring no clock input, and thus dissipate minimal energy. However, a voltage drop occurs across all diodes, robbing the circuit of some efficiency. For the present invention, a voltage drop of 0.7V is assumed to occur across each integrated circuit diode 472, 474. The resulting converter 600 with diodes shown in FIG. 6, however, is less complex and does not require multiple clocks to generate extra clock signals. Note that only a single clock, with clocking scheme shown in FIG. 11, is required to establish the frequency and phase of the converter, because the input to switch 482 is inverted relative to switch 478. In addition, less power is dissipated through use of a simpler clock scheme. Diode 456 provides a closed path for any residual inductor currents and prevents large negative voltages at switch 472. Also, if the inductors 404 and 418 are integrated inductors, such as those illustrated in FIGS. 3(a)–(e), the entire converter 600 shown in FIG. 6 may be fabricated on a single integrated circuit chip.

FIG. 7 shows a negative output DC converter 700 similar to that depicted in FIG. 4(b), described above, with transistors 484, 485, 486 and 487 used as switches. Switches 484, 485, 486 and 487 change states according to a clocking scheme represented by clock signals  $\phi_1$ ,  $\phi_2$ ,  $\phi_3$ , the timing of which is shown in FIG. 10. DC power source 402 charges capacitor 412 through inductor 404 during the charging phase, and capacitor 438 is charged through inductor 418 to output voltage  $V_{out}$  during the transfer phase. Diode 456 provides a closed path for any residual inductor currents and prevents large negative voltages at switch 484. The implementation shown in FIG. 7 requires multiple clocks with clocking scheme shown in FIG. 10, increasing circuit complexity and consuming circuit power, hence somewhat reducing the efficiency of the converter. If the inductors 404

and 418 are integrated inductors, such as those illustrated in FIGS. 3(a)–(e), the entire converter 700 may be fabricated on a single integrated circuit chip.

FIG. 8 shows a modification of the DC to DC converter of FIG. 7, where switches 485 and 487 of FIG. 7 have been replaced with diodes 488 and 492. Diodes are simpler devices than transistors, requiring no clock input, and thus dissipate minimal energy. However, a voltage drop occurs across all diodes, robbing the circuit of some efficiency. For the present invention, a voltage drop of 0.7V is assumed to occur across each diode 488, 492. Diode 456 provides a closed path for any residual inductor currents and prevents large negative voltages at switch 489. The converter 800 shown in FIG. 8, however, is less complex and does not require multiple clocks to generate extra clock signals. Note that only a single clock, with clocking scheme shown in FIG. 11, is required to establish the frequency and phase of the converter, because the input to switch 491 is inverted relative to switch 489. In addition, less power is dissipated through use of a simpler clock scheme. Also, if the inductors 404 and 418 are integrated inductors, such as those illustrated in FIGS. 3(a)–(e), the entire converter 800 shown in FIG. 8 may be fabricated on a single integrated circuit chip.

Another embodiment of the present invention, illustrated in FIG. 12, provides reduced fluctuations in the power supply output voltage (ripple voltage) when several DC converter circuits (constructed as described above) are used in parallel to charge a single capacitor. For example, a plurality (three shown) of DC converters 600 of FIG. 6 could be connected in parallel, as shown in FIG. 12, each containing all of the components of converter 600 except for the output capacitor 926 and ground. The clocking scheme of the switches must be coordinated as shown in FIG. 13, i.e. the first parallel circuit is clocked by  $\phi_4$ , the second parallel circuit is clocked by  $\phi_5$ , and the third parallel circuit is clocked by  $\phi_6$ , as shown in FIG. 12. While  $\phi_4$ ,  $\phi_5$  and  $\phi_6$  have the same clocking frequency, they are phase offset from one another. Following the FIG. 13 clocking scheme, the parallel circuit is connected as shown in FIG. 12 such that each circuit charges output capacitor 926 at different time periods, thus reducing voltage fluctuations (ripple voltage) at the output  $V_{out}$ .

FIGS. 3(a) and 3(b) show a first integrated circuit inductor which may be used for inductors 404, 418 in the present invention, while FIGS. 3(c) and 3(d) show a second integrated circuit inductor which may be used in the present invention. FIG. 3(e) shows an alternate embodiment of the second integrated circuit inductor of FIGS. 3(c) and 3(d). Although the present invention is not to be limited to the use of such inductors, these IC inductors, which can be directly fabricated in an IC chip, offer additional space and power density advantages over discrete inductors externally mounted to an IC chip.

FIG. 3(a) shows an exploded perspective view of a first integrated inductor formed from a solenoidal inductor pattern 100. Solenoidal pattern 100 is made up of three vertically stacked open conductive patterns 103, 106 and 109 coupled together by conductive segments 112 and 115. In the embodiment shown in FIG. 3(a), each of the three open conductive patterns 103, 106, 109 is an open rectangle. However, the present invention is not limited to a particular open pattern shape. Any shape or shapes that can be combined to form a device in which the voltage across the device is proportional to the derivative of the current passing through the device is suitable for use in connection with the present invention.

Open conductive patterns 103, 106 and 109 are fabricated from a conductive material. In one embodiment, open con-

ductive patterns 103, 106 and 109 are fabricated from copper. In alternate embodiments, they are formed from gold, aluminum, silver, or an alloy of copper, gold, aluminum, or silver, or any combination of metals or alloys capable of conducting electric current.

Also, open conductive patterns 103, 106 and 109 each have a cross-sectional area which varies directly with the current-carrying capacity and varies inversely with the resistance. In other words, as the cross-sectional area decreases, the resistance increases and the current carrying capacity of the open conductive patterns 103, 106, and 109 decreases. The cross sectional area of each pattern 103, 106, 109 is selected to ensure that it is capable of carrying the anticipated operating current.

Referring to FIG. 3(a), open conductive pattern 103 is coupled to open conductive pattern 106 by conductive segment 112, which is perpendicular to both open conductive patterns 103 and 106. Similarly, open conductive patterns 106 and 109 are coupled by conductive segment 115, which is perpendicular to both open conductive patterns 106 and 109.

Each of the open conductive patterns 103, 106, and 109 shown in FIG. 3(a) can be fabricated from a different material. For example, open conductive pattern 103 can be fabricated from aluminum, pattern 106 can be fabricated from copper, and pattern 109 from gold. This provides some flexibility for the inductor designer to control inductor characteristics, such as controlling heat generation by incorporating higher conductivity material into specific sections of the inductor. In addition, the designer is able to control the location of particular materials to limit impurity migration, such as to avoid the incorporation of a barrier layer to protect a substrate from copper migration by instead locating any copper sufficiently far from the substrate.

FIG. 3(b) shows a side view of a cross-sectional slice of solenoid inductor 100 fabricated on a substrate 203. The fabricated structure 200 includes magnetic material layers 206, 212, 221, 233, open inductor patterns 103, 106, 109, and conductive segments 112, 115. Each of the layers, patterns and/or segments may be produced by chemical vapor deposition (CVD) or other processes for metallization, metal layering, and/or etching as is known in the art. Substrate 203 is preferably a semiconductor, such as silicon. Alternatively, substrate 203 is gallium arsenide, germanium, or some other substrate material suitable for use in the manufacturing of integrated circuits.

FIGS. 3(c) and 3(d) depict a second integrated inductor with square spiral inductor pattern 140 which may be used as inductor 404, 418 in the invention. A first integrated inductor with a square spiral pattern 140 is shown in FIG. 3(c). The pattern 140 need not be limited to a square spiral, but may instead be a circular spiral, polygonal spiral, or any contiguous open pattern fabricated from a conductive material. The square spiral inductor pattern 140 is preferred because it is easy to manufacture. Pattern 140 is also preferably fabricated from a high-conductivity material such as copper, but may alternatively be formed from other conducting materials, such as gold, aluminum, silver, or an alloy of copper, gold, aluminum, or silver, or any combination of metals or alloys capable of conducting electric current.

FIG. 3(d) shows a fragmentary vertical cross-sectional view of a second integrated inductor structure 300 using the square spiral inductor pattern 140. The square spiral inductor pattern 140 of FIG. 3(c) is included in the integrated inductor structure 300 as the square cross-sectional areas

230 in FIG. 3(d). Referring to FIG. 3(d), integrated inductor structure 300 is coupled to conducting path 220 through vias 240 to peripheral connection 210. Inductor structure 300 is composed of several layers fabricated on substrate 302 and includes magnetic material layer 304, insulating layer 306, inductor pattern 230, second insulating layer 308, and second magnetic material layer 312. Each layer is formed on the layer below it through deposition or other processes known in the art.

Insulating layers 306 and 308 may be formed from inorganic silicon oxide film, silicon dioxide, or other inorganic insulating materials known in the art. In alternate embodiments designed for a low temperature processing environment, insulating layers 306 and 308 may be organic insulators, such as parylene and polyimide.

Substrate 302 is preferably a semiconductor, such as silicon. Alternatively, substrate 302 is gallium arsenide, germanium, or some other substrate material suitable for use in the manufacturing of integrated circuits. Inductors intended for use in circuits fabricated on a silicon substrate usually operate at a slightly lower frequency, hence requiring slightly larger inductance values, than inductors intended for use in circuits fabricated on a gallium arsenide substrate. A larger inductance value is usually realized in silicon by having the inductor occupy a larger surface area. Rather than increasing the inductance value by occupying a larger surface area, a larger inductance value is here achieved by adding layers of magnetic material 304 and 312 to the inductor. Magnetic material layers 304 and 312 allow the inductor to store a larger amount of energy in a smaller space, increasing the inductance value.

Magnetic material layers 304 and 312 may be formed from a magnetic material selected according to the inductance requirement. In embodiments in which a large inductance value in a small volume is desired, a high permeability ferromagnetic material, such as pure iron or a NiFe alloy is selected. One example of such a high permeability alloy is an alloy of 81% Ni and 19% Fe. Electrically non-conducting films, such as a magnetic oxide film, may also be suitable for use in the present invention.

Locating magnetic material layers 304 and 312 above and below inductor pattern 230, respectively, allows the contribution of the magnetic material to the inductance value of the inductor to be precisely controlled. The thickness of the magnetic material layers 304 and 312 and the magnetic properties of the magnetic material define the inductance value of the inductor structure 300. In addition, magnetic material layers 304 and 312 confine the magnetic flux and noise radiated by current flowing in inductor pattern 230 to the area bounded by the outer surfaces of layers 304 and 312.

By stacking sandwich structures, as well as multiple inductor patterns, a larger inductance can be created without increasing the surface area on the substrate occupied by the inductor, as shown in FIG. 3(e). Referring to FIG. 3(e), one embodiment of a double inductor structure 301 containing two inductors is shown. Double inductor structure 301 includes base structure 305, first sandwich structure 310, second sandwich structure 315, and conducting path 320. Base structure 305 includes substrate 325, magnetic material layer 330, and insulating layer 335. Sandwich structure 310 includes inductor pattern 340, insulating layer 345, magnetic material layer 350, and insulating layer 355. Second sandwich structure 315 includes inductor pattern 360, insulating layer 365, magnetic material layer 370, and insulating layer 375.

Conducting path 320 couples sandwich structure 310 to second sandwich structure 315, and serially connects induc-



tor pattern 340 to inductor pattern 360. A current flowing in the serially connected inductor patterns creates a reinforcing magnetic field in magnetic material layer 350. Magnetic material layers 330 and 370 are located below inductor pattern 340 and above inductor pattern 360, respectively. Magnetic material layers 330 and 370 confine the magnetic flux and noise radiated by a current flowing in inductor patterns 340 and 360 to the area bounded by the outer surfaces of magnetic material layers 330 and 370. By stacking sandwich structures, in one embodiment a large inductance can be created without increasing the surface area occupied by the inductor on the substrate.

FIG. 9 illustrates a processor-based system 90, e.g. a computer system, which utilizes the DC—DC converter of the present invention. The processor-based system 90 comprises a processor 94, a memory circuit 96, and an input/output (I/O) device 92. One or more of the components of the processor-based system 90, for example, one or more of the processor 94 and memory circuit 96, also includes a DC power source 97 connected to a ground potential and to a DC to DC converter 98 constructed in accordance with the present invention (see FIGS. 4–8 and 12). The memory circuit 96 contains one or more of a random access memory (RAM), for example a DRAM, SRAM, SDRAM, or other type of RAM known in the art, or a read only memory (ROM), for example an EPROM, and EEPROM, flash memory, or other type of ROM known in the art. The processor 94 may be an embedded-memory processor in which the memory circuit 96 is included on the same IC chip as the processor 94. The DC to DC converter 98 may also be included on the same IC chip as either or both of the processor 94 and memory circuit 96.

The present invention provides a DC—DC converter with inductive current limiters to improve efficiency as well as conserve valuable space using integrated components, including integrated inductors. These improvements remove the need for bulky conventional inductors and improve power densities and thermal properties of the resulting device while simplifying the circuit and allowing higher output currents, which can be used, for example, for EEPROM reprogramming. Low voltage and low power consumption of the converter permits its implementation in battery-powered portable electronics.

While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. For example, use of the converter is not limited to the computer system implementation described above, but may be incorporated anywhere multiple voltages are needed. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A DC to DC power converter comprising:
  - an input terminal for receiving an input voltage;
  - a charging inductor;
  - an output terminal for outputting an output voltage different from said input voltage;
  - a first capacitor; and
  - a switch circuit operating at a switching frequency of at least about 100 mega Hertz for coupling said input

terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase, said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal.

2. The DC converter of claim 1 wherein said charging inductor has an inductance value less than about 1 micro Henry.

3. The DC converter of claim 1 wherein said switching frequency and an inductance value of said charging inductor are chosen such that there is substantially no current in said charging inductor when said switch circuit transitions from said charging phase to said transfer phase.

4. The DC converter of claim 1 further comprising an output filter connected to said switch circuit and said output terminal whereby said first capacitor transfers charge through said output filter to said output terminal during said transfer phase.

5. The DC converter of claim 4 wherein said output filter includes at least one output capacitor.

6. The DC converter of claim 4 wherein said output filter includes at least one output inductor and at least one output capacitor.

7. The DC converter of claim 1 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and a ground potential, a third switch connected to open or close a third connection between a negative plate of said first capacitor and said ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said output terminal.

8. The DC converter of claim 7 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

9. The DC converter of claim 7 wherein said first switch and said second switch are transistors, and said third switch and said fourth switch are diodes.

10. The DC converter of claim 1 wherein said input voltage is between about -25 to +25 volts.

11. The DC converter of claim 1 wherein said input voltage is less than or equal to about +5 volts.

12. The DC converter of claim 1 wherein said input voltage is greater than or equal to about -5 volts.

13. The DC converter of claim 1 wherein said charging phase and said transfer phase do not overlap.

14. The DC converter of claim 1 wherein said charging inductor is an integrated circuit inductor.

15. The DC converter of claim 14 wherein said integrated circuit inductor is a spiral inductor.

16. The DC converter of claim 14 wherein said integrated circuit inductor is a double-stacked spiral inductor.

17. The DC converter of claim 14 wherein said integrated circuit inductor is a solenoidal inductor.

18. The DC converter of claim 1 wherein the components of said converter are fabricated on at least one integrated circuit chip.

19. The DC converter of claim 1 wherein the converter, including said inductor, is fabricated on a single integrated circuit chip.

20. The DC converter of claim 1 wherein the converter, excluding said inductor, is fabricated on a single integrated circuit chip.

21. The DC converter of claim 8 or 9 wherein said transistors are CMOS transistors.

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22. The DC converter of claim 1 further comprising at least one control terminal for receiving at least one control signal, said switch circuit operating at said switching frequency in response to said at least one received control signal.

23. A DC to DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase, said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal.

24. The DC converter of claim 23 wherein said charging inductor has an inductance value of approximately 100 nH or less.

25. The DC converter of claim 23 wherein said switching frequency is at least about 100 MHz.

26. The DC converter of claim 23 wherein said switching frequency and an inductance value of said charging inductor are chosen such that there is substantially no current in said charging inductor when said switch circuit transitions from said charging phase to said transfer phase.

27. The DC converter of claim 23 further comprising an output filter connected to said switch circuit and said output terminal whereby said first capacitor transfers charge through said output filter to said output terminal during said transfer phase.

28. The DC converter of claim 27 wherein said output filter includes at least one output capacitor.

29. The DC converter of claim 27 wherein said output filter includes at least one output inductor and at least one output capacitor.

30. The DC converter of claim 23 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and a ground potential, a third switch connected to open or close a third connection between a negative plate of said first capacitor and said ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said output terminal.

31. The DC converter of claim 30 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

32. The DC converter of claim 30 wherein said first switch and said second switch are transistors, and said third switch and said fourth switch are diodes.

33. The DC converter of claim 23 wherein said input voltage is between about -25 to +25 volts.

34. The DC converter of claim 23 wherein said input voltage is less than or equal to about +5 volts.

35. The DC converter of claim 23 wherein said input voltage is greater than or equal to about -5 volts.

36. The DC converter of claim 23 wherein said charging inductor is an integrated circuit inductor.

37. The DC converter of claim 36 wherein said integrated circuit inductor is a spiral inductor.

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38. The DC converter of claim 36 wherein said integrated circuit inductor is a double-stacked spiral inductor.

39. The DC converter of claim 36 wherein said integrated circuit inductor is a solenoidal inductor.

40. The DC converter of claim 23 wherein the components of said converter are fabricated on at least one integrated circuit chip.

41. The DC converter of claim 23 wherein the converter, including said inductor, is fabricated on a single integrated circuit chip.

42. The DC converter of claim 23 wherein the converter, excluding said inductor, is fabricated on a single integrated circuit chip.

43. The DC converter of claim 31 or 32 wherein said transistors are CMOS transistors.

44. The DC converter of claim 23 further comprising at least one control terminal for receiving at least one control signal, said switch circuit operating at said switching frequency in response to said at least one received control signal.

45. A DC to DC converter, comprising:

a charge transfer capacitor;

a terminal for receiving a DC source voltage;

a ground connection;

a first inductive circuit coupled to said terminal;

a second inductive circuit;

an output capacitor coupled between said second inductive circuit and said ground connection;

a switch circuit operative in a first mode to couple said terminal through said first inductive circuit to a first plate of said charge transfer capacitor and to couple said ground connection to a second plate of said charge transfer capacitor to enable said charge transfer capacitor to be charged by a DC voltage applied to said terminal, said switch circuit being operative in a second mode to couple said first plate of said charge transfer capacitor to said second inductive circuit and to couple said second plate of said charge transfer capacitor to said terminal to enable said output capacitor to be charged by an additive DC voltage formed by a DC voltage at said terminal and a DC voltage on said charge transfer capacitor.

46. A DC to DC converter, comprising:

a charge transfer capacitor;

a terminal for receiving a DC source voltage;

a ground connection;

a first inductive circuit coupled to said terminal;

a second inductive circuit;

an output capacitor coupled between said second inductive circuit and said ground connection;

a switch circuit operative in a first mode to couple said terminal through said first inductive circuit to a first plate of said charge transfer capacitor and to couple said ground connection to a second plate of said charge transfer capacitor to enable said charge transfer capacitor to be charged by a DC voltage applied to said terminal, said switch circuit being operative in a second mode to couple said first plate of said charge transfer capacitor to said ground connection and to couple said second plate of said charge transfer capacitor to said second inductive circuit to enable said output capacitor to be charged by a DC voltage on said charge transfer capacitor.

47. The DC to DC converter of claim 46 wherein said switch circuit includes a first switch connected to open or

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close a first connection between said first inductive circuit and said first plate of said charge transfer capacitor, a second switch connected to open or close a second connection between said first plate of said charge transfer capacitor and said ground connection, a third switch connected to open or close a third connection between said second plate of said charge transfer capacitor and said ground connection, and a fourth switch connected to open or close a fourth connection between said second plate of said charge transfer capacitor and said second inductive circuit.

48. The DC to DC converter of claim 47 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

49. The DC to DC converter of claim 47 wherein said first switch and said second switch are transistors, and said third switch and said fourth switch are diodes.

50. The DC to DC converter of claim 46 further comprising at least one control terminal for receiving at least one control signal, said switch circuit operating at a switching frequency in response to said at least one received control signal.

51. The DC to DC converter of claim 46 wherein the components of said converter are fabricated on at least one integrated circuit chip.

52. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and said integrated circuit containing a DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency of at least about 100 MHz for coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal.

53. The processor-based system of claim 52 wherein said charging inductor has an inductance value less than about 1 micro Henry.

54. The processor-based system of claim 52 further comprising an output filter connected to said switch circuit and said output terminal whereby said first capacitor transfers charge through said output filter to said output terminal during said transfer phase.

55. The processor-based system of claim 54 wherein said output filter includes at least one output capacitor.

56. The processor-based system of claim 54 wherein said output filter includes at least one output inductor and at least one output capacitor.

57. The processor-based system of claim 52 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and said output terminal, a third switch connected to open or close a third connection between a negative plate of said first capacitor and a ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said input terminal.

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58. The processor-based system of claim 57 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

59. The processor-based system of claim 57 wherein said first switch and said second switch are diodes, and said third switch and said fourth switch are transistors.

60. The processor-based system of claim 52 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and a ground potential, a third switch connected to open or close a third connection between a negative plate of said first capacitor and said ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said output terminal.

61. The processor-based system of claim 60 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

62. The processor-based system of claim 60 wherein said first switch and said second switch are transistors, and said third switch and said fourth switch are diodes.

63. The processor-based system of claim 52 wherein said input voltage is between about -25 to +25 volts.

64. The processor-based system of claim 52 wherein said input voltage is less than or equal to about +5 volts.

65. The processor-based system of claim 52 wherein said input voltage is greater than or equal to about -5 volts.

66. The processor-based system of claim 52 wherein said charging phase and said transfer phase do not overlap.

67. The processor-based system of claim 52 wherein said charging inductor is an integrated circuit inductor.

68. The processor-based system of claim 52 wherein the converter, excluding said inductor, is fabricated on a single integrated circuit chip.

69. The processor-based system of claim 52 further comprising at least one control terminal for receiving at least one control signal, said switch circuit operating at said switching frequency in response to said at least one received control signal.

70. The processor-based system of claim 52 wherein the components of said converter are fabricated on at least one integrated circuit chip.

71. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and said integrated circuit containing a DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal.

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72. A method of voltage conversion, comprising the acts of:

receiving an input voltage from an input terminal;  
outputting an output voltage different from said input voltage to an output terminal;  
charging a first capacitor from said input terminal through a charging inductor during a charging phase;  
transferring charge from said first capacitor to said output terminal during a transfer phase; and  
alternating between said charging phase and said transfer phase at a switching frequency of about at least 100 MHz using a switch circuit, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during said charging phase, and coupling said first capacitor to said output terminal during said transfer phase.

73. The method of claim 72 wherein said charging inductor has an inductance value less than about 1 micro Henry.

74. The method of claim 72 wherein said first capacitor transfers charge during said transfer phase through an output filter connected to said switch circuit and said output terminal.

75. The method of claim 74 wherein said output filter includes at least one output capacitor.

76. The method of claim 74 wherein said output filter includes at least one output inductor and at least one output capacitor.

77. The method of claim 72 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and said output terminal, a third switch connected to open or close a third connection between a negative plate of said first capacitor and a ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said input terminal.

78. The method of claim 77 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

79. The method of claim 77 wherein said first switch and said second switch are diodes, and said third switch and said fourth switch are transistors.

80. The method of claim 72 wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and a ground potential, a third switch connected to open or close a third connection between a negative plate of said first capacitor and said ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said output terminal.

81. The method of claim 80 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

82. The method of claim 80 wherein said first switch and said second switch are transistors, and said third switch and said fourth switch are diodes.

83. The method of claim 72 wherein said input voltage is between about -25 to +25 volts.

84. The method of claim 72 wherein said input voltage is less than or equal to about +5 volts.

85. The method of claim 72 wherein said input voltage is greater than or equal to about -5 volts.

86. The method of claim 72 wherein said charging phase and said transfer phase do not overlap.

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87. The method of claim 72 wherein said charging inductor is an integrated circuit inductor.

88. The method of claim 72 wherein said charging inductor is not an integrated circuit inductor.

89. The method of claim 72 further comprising the acts of receiving at least one control signal and operating said switch circuit at said switching frequency in response to said at least one received control signal.

90. The method of claim 72 wherein conversion is performed by at least one integrated circuit chip.

91. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency of at least about 100 MHz for coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase, said switch circuit coupling said first capacitor to said output terminal and uncoupling said first capacitor from said input terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal;

wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a first plate of said first capacitor, a second switch connected to open or close a second connection between said first plate and said output terminal, a third switch connected to open or close a third connection between a second plate of said first capacitor and a ground potential, and a fourth switch connected to open or close a fourth connection between said second plate and said input terminal.

92. The DC converter of claim 91 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

93. The DC converter of claim 91 wherein said first switch and said second switch are diodes, and said third switch and said fourth switch are transistors.

94. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency of at least about 100 MHz for coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; wherein during said charging phase, said switch circuit connects said input terminal to a positive plate of said first capacitor and a negative plate of said first capacitor to a ground potential, and during said transfer phase, said switch circuit connects said negative plate to said input terminal and said positive plate to said output terminal.

95. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

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an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency of at least about 100 MHz for coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; wherein during said charging phase, said switch circuit connects said input terminal to a positive plate of said first capacitor and a negative plate of said first capacitor to a ground potential, and during said transfer phase, said switch circuit connects said positive plate to said ground potential and said negative plate to said output terminal.

96. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor;

a switch circuit operating at a switching frequency of at least about 100 MHz for coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; and

at least a second charging circuit including at least a second capacitor and a second switch circuit connected in parallel with a first charging circuit including at least said first capacitor and said switch circuit, said switch circuits periodically connecting each of said parallel charging circuits to said output terminal.

97. The DC power converter of claim 96 wherein said output terminal is alternately connected periodically to each of said parallel charging circuits at a frequency of at least about 100 MHz.

98. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal;

wherein said switch circuit includes a first switch connected to open or close a first connection between said input terminal and a positive plate of said first capacitor, a second switch connected to open or close a second connection between said positive plate and

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said output terminal, a third switch connected to open or close a third connection between a negative plate of said first capacitor and a ground potential, and a fourth switch connected to open or close a fourth connection between said negative plate and said input terminal.

99. The DC converter of claim 98 wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

100. The DC converter of claim 98 wherein said first switch and said second switch are diodes, and said third switch and said fourth switch are transistors.

101. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; wherein during said charging phase, said switch circuit connects said input terminal to a positive plate of said first capacitor and a negative plate of said first capacitor to a ground potential, and during said transfer phase, said switch circuit connects said negative plate to said input terminal and said positive plate to said output terminal.

102. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; wherein during said charging phase, said switch circuit connects said input terminal to a positive plate of said first capacitor and a negative plate of said first capacitor to a ground potential, and during said transfer phase, said switch circuit connects said positive plate to said ground potential and said negative plate to said output terminal.

103. A DC power converter comprising:

an input terminal for receiving an input voltage;

a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor; and

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance

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value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; wherein said charging phase and said transfer phase do not overlap.

**104.** A DC power converter comprising:

an input terminal for receiving an input voltage;  
a charging inductor;

an output terminal for outputting an output voltage different from said input voltage;

a first capacitor;

a switch circuit operating at a switching frequency permitting said charging inductor to have an inductance value less than 1 micro Henry, said switch circuit coupling said input terminal to said first capacitor through said charging inductor during a charging phase, said first capacitor being charged during said charging phase,

said switch circuit coupling said first capacitor to said output terminal during a transfer phase whereby said first capacitor transfers charge to said output terminal; and

at least a second charging circuit including at least a second capacitor and a second switch circuit connected in parallel with a first charging circuit including at least said first capacitor and said switch circuit, said switch circuits periodically connecting each of said parallel charging circuits to said output terminal.

**105.** The DC power converter of claim **104** wherein said output terminal is alternately connected periodically to each of said parallel charging circuits at a frequency of at least about 100 MHz.

**106.** A DC to DC converter, comprising:

a charge transfer capacitor;

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a terminal for receiving a DC source voltage;

a ground connection;

a first inductive circuit coupled to said terminal;

a second inductive circuit;

an output capacitor coupled between said second inductive circuit and said ground connection;

a switch circuit operative in a first mode to couple said terminal through said first inductive circuit to a first plate of said charge transfer capacitor and to couple said ground connection to a second plate of said charge transfer capacitor to enable said charge transfer capacitor to be charged by a DC voltage applied to said terminal, said switch circuit being operative in a second mode to couple said first plate of said charge transfer capacitor to said second inductive circuit and to couple said second plate of said charge transfer capacitor to said terminal to enable said output capacitor to be charged by an additive DC voltage formed by a DC voltage at said terminal and a DC voltage on said charge transfer capacitor;

wherein said switch circuit includes a first switch connected to open or close a first connection between said first inductive circuit and said first plate of said charge transfer capacitor, a second switch connected to open or close a second connection between said first plate of said charge transfer capacitor and said second inductive circuit, a third switch connected to open or close a third connection between said second plate of said charge transfer capacitor and said ground connection, and a fourth switch connected to open or close a fourth connection between said second plate of said charge transfer capacitor and said terminal.

**107.** The DC to DC converter of claim **106** wherein said first switch, said second switch, said third switch and said fourth switch are transistors.

**108.** The DC to DC converter of claim **106** wherein said first switch and said second switch are diodes, and said third switch and said fourth switch are transistors.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,429,632 B1  
DATED : August 6, 2002  
INVENTOR(S) : Leonard Forbes et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,


Line 11, " $(1 \times 10^{-6} \text{H})$ " should read --  $(1 \times 10^{-6} \text{H})$  --.

Column 9,

Line 2, "arc" should read -- are --.

Signed and Sealed this

Third Day of December, 2002

A handwritten signature in black ink, appearing to read "James E. Rogan", with a long horizontal flourish extending from the bottom of the signature.

JAMES E. ROGAN  
*Director of the United States Patent and Trademark Office*



US006414863B1

(12) **United States Patent**  
**Bayer et al.**

(10) **Patent No.:** **US 6,414,863 B1**  
(45) **Date of Patent:** **Jul. 2, 2002**

(54) **FREQUENCY CONTROL CIRCUIT FOR  
UNREGULATED INDUCTORLESS DC/DC  
CONVERTERS**

6,049,201 A \* 4/2000 Feldtkeller ..... 323/288  
6,107,862 A \* 8/2000 Mukainakano et al. .... 327/536

\* cited by examiner

(75) Inventors: **Erich-Johann Bayer**, Thonhausen;  
**Hans Schmeller**, Forstern, both of (DE)

*Primary Examiner*—Bao Q. Vu

(74) *Attorney, Agent, or Firm*—J. Dennis Moore; W. James  
Brady, III; Frederick J. Telecky, Jr.

(73) Assignee: **Texas Instruments Incorporated**,  
Dallas, TX (US)

(57) **ABSTRACT**

(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

An unregulated inductorless direct current to direct current  
converter comprising a first voltage-to-current converter  
configured to convert a first voltage to a first current and a  
second voltage-to-current converter configured to convert a  
second voltage to a second current. A regulation circuit is  
coupled to the first and second voltage-to-current converters  
and configured to generate an output current proportional to  
the difference between the first and second currents. Also a  
variable frequency oscillator is coupled to the regulation  
circuit, the oscillator receiving as a control current the output  
current therefrom and outputting a clock signal having a  
frequency proportionate to the control current. The con-  
verter further comprises an output stage coupled to receive  
the clock signal and receiving an input voltage and output-  
ting an output voltage, the output voltage and the input  
voltage having a ratio that is determined by the clock signal.

(21) Appl. No.: **09/943,482**

(22) Filed: **Aug. 30, 2001**

(51) Int. Cl.<sup>7</sup> ..... **H02M 3/18; H02M 7/00**

(52) U.S. Cl. .... **363/60; 307/110; 323/288**

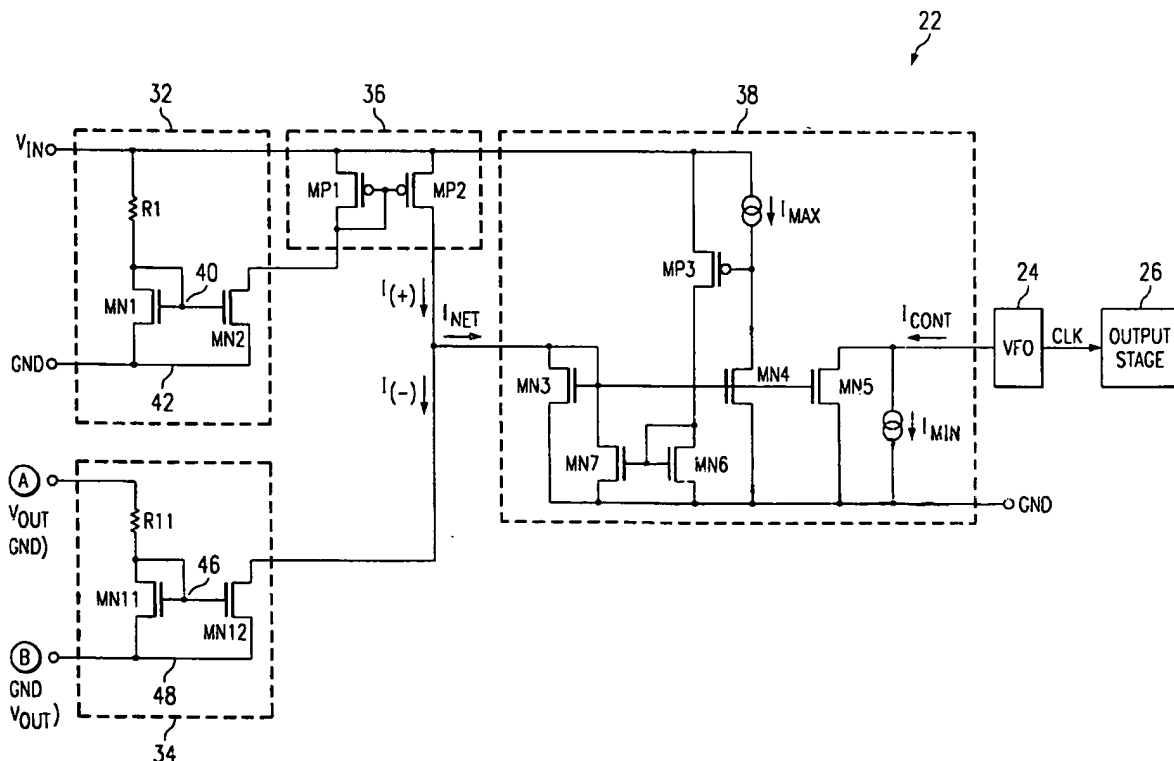
(58) Field of Search ..... **363/59, 60, 61;**  
**307/109, 110; 323/228**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,159,543 A \* 10/1992 Yamawaki ..... 363/60  
5,397,928 A \* 3/1995 Chan et al. .... 307/109  
6,020,781 A \* 2/2000 Fujioka ..... 327/541

**23 Claims, 2 Drawing Sheets**





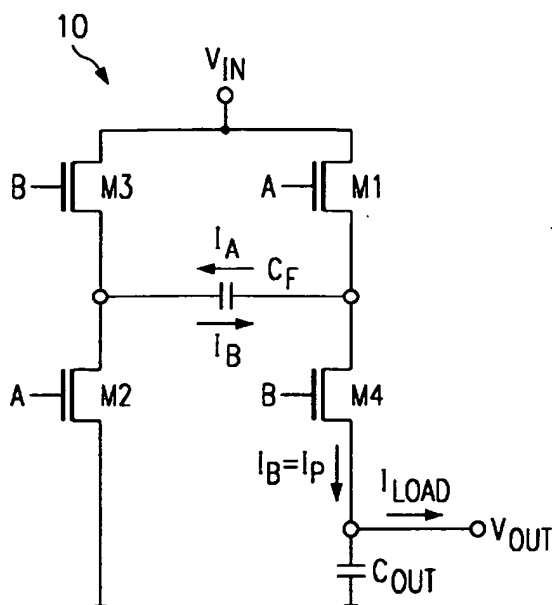


FIG. 1A

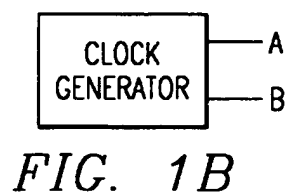


FIG. 1B

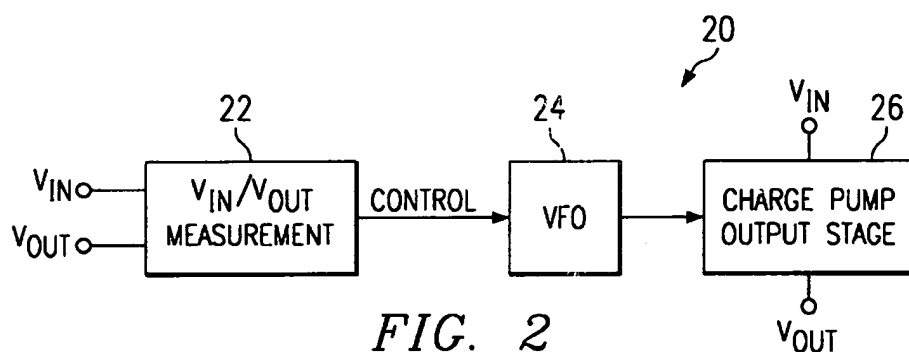


FIG. 2

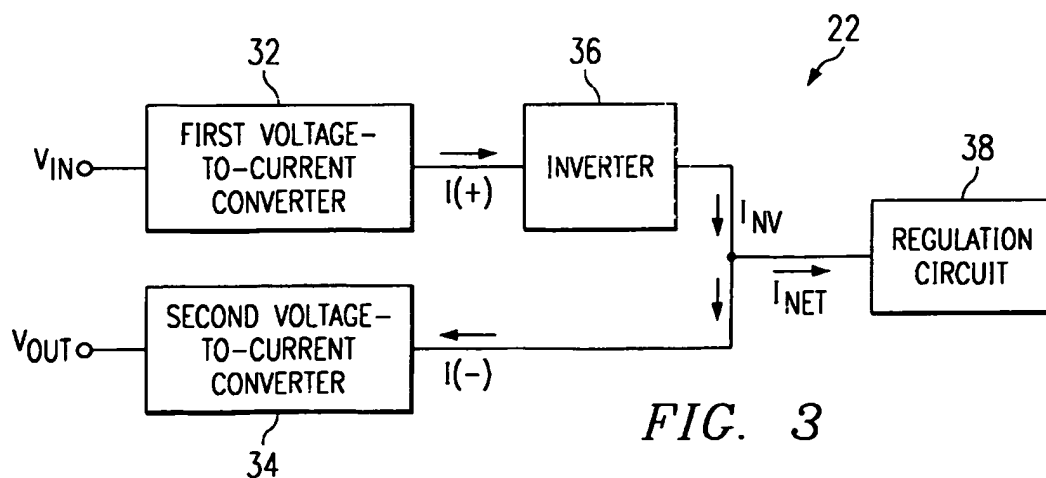


FIG. 3

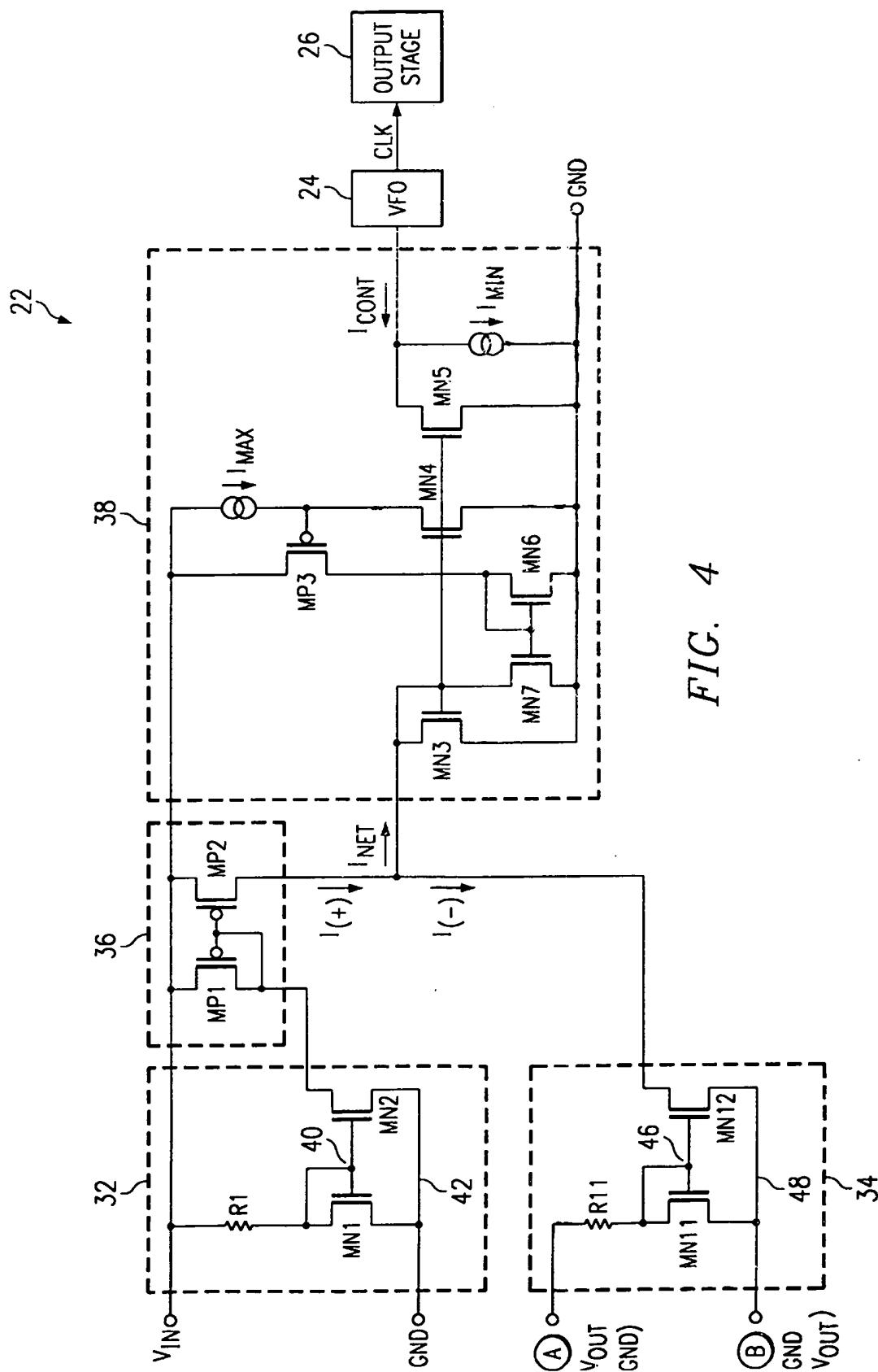


FIG. 4

# FREQUENCY CONTROL CIRCUIT FOR UNREGULATED INDUCTORLESS DC/DC CONVERTERS

## TECHNICAL FIELD OF THE INVENTION

This invention relates to DC/DC converters and more particularly to a frequency control circuit for regulation of an inductorless DC/DC converter.

## BACKGROUND OF THE INVENTION

Unregulated inductorless DC/DC converters (i.e. charge pumps) are used to double, triple, or invert a voltage that is supplied to the converter. These converters, however, do not generate a constant output voltage. An exemplary unregulated converter comprises a clock generator or oscillator and an array of power switches. FIG. 1A, for example, shows a prior art unregulated voltage doubler 10. The voltage doubler 10 is coupled to a clock generator, as shown in FIG. 1B, which generates a signal A and B that serve as inputs into the voltage doubler 10. These signals will turn the multiple transistors M1, M2, M3, and M4 on as needed to double the voltage  $V_{in}$ . When transistors M2 and M1 are turned on (i.e. during phase A when the signal is high), the capacitor  $C_f$  will be charged to the voltage  $V_{in}$ . When transistors M3 and M4 are turned on (i.e. during phase B when the signal is high), the capacitor  $C_p$  which is already charged to the voltage  $V_{in}$ , will be put in series to the input voltage,  $V_{in}$  and the output capacitor,  $C_{out}$  will be charged up to twice the voltage  $V_{in}$ .

In order for the converter to work most efficiently and to be cost effective, there are four independent requirements that must be met. These requirements include 1) a small internal resistance (i.e. a low voltage drop at full load), 2) a low output voltage ripple at full load, 3) a low quiescent current, and 4) small and inexpensive external components (i.e. capacitors). The internal resistance  $R_{i2}$  of an inductorless transistor SC voltage doubler can be calculated as:

$$R_{i2} = \frac{1}{C_f * f_{clk}} + 2 * \sum_{i=1}^4 R_{Mi} \quad (1)$$

were  $C_f$ =pump or "flying" capacitor,  $f_{clk}$ =clock frequency, and  $R_{Mi}$ =ON-resistance of switch  $M_i$ . Thus, to minimize the internal resistance  $R_{i2}$ , a high clock frequency  $f_{clk}$  and/or a large flying capacitor  $C_f$  is needed. The output voltage ripple is represented by:

$$V_{RIPPLE} = \frac{1}{2 * C_{OUT} * f_{clk}} * I_{LOAD} \quad (2)$$

where  $V_{RIPPLE}$ =output voltage ripple,  $C_{OUT}$ =output capacitance, and  $I_{LOAD}$ =load current. To minimize the output voltage ripple, then, a high clock frequency and/or a large output capacitance is needed.

Since the Power MOSFETS in the converter periodically have to change states, their gates periodically need to be charged and discharged. The gates of all power transistors in the converter can be seen as a capacitor which needs to be charged to the input voltage and discharged to ground. When a capacitor is charged from zero to any other voltage, half of the energy gets lost. Compared to an inductive converter, a Charge Pump has higher switching losses from the gate capacitances of the power transistors, since there are more transistors to control. These losses are represented by a quiescent current:

$$I_Q = (V_{IN} * f_{clk}) * \sum_{i=1}^4 C_{Mi} \quad (3)$$

To minimize the quiescent current, a low clock frequency is need. However, the low clock frequency needed to minimize the quiescent current is counter to the high clock frequency which is needed to minimize the internal resistance and the voltage ripple. Thus, it is impossible for the prior art to fulfill all four requirements because prior art devices run at a constant frequency.

In the prior art, designers have generally compromised on the conflicting performance characteristics and offered their devices with different operating frequencies, for example 1, 10, 50, and 100 khz. Thus, consumers must choose to fulfill certain of the requirements while forfeiting others. For example, consumers can typically obtain the first three requirements but at the expense of very costly, large external capacitors which allow a small operating frequency. If the quiescent current  $I_Q$  is not an issue, then high frequency versions with small external capacitors can be utilized. If internal resistance and voltage ripple is not an issue, low frequency versions with small external capacitors can be used, an example of which is the MAX 828 or a like device. Thus, what is needed is a design that will provide efficient and cost effective operation by meeting all four of the requirements.

## SUMMARY OF THE INVENTION

These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by the present invention that is a frequency control circuit for unregulated inductorless DC/DC converters.

In a preferred embodiment method of the present invention, an unregulated inductorless direct current to direct current converter comprises a first voltage-to-current converter configured to convert a first voltage to a first current and a second voltage-to-current converter configured to convert a second voltage to a second current. A regulation circuit is coupled to the first and second voltage-to-current converters and configured to generate an output current proportional to the difference between the first and second currents. The unregulated inductorless direct current to direct current converter further comprises a variable frequency oscillator coupled to the regulation circuit, the oscillator receiving as a control current the output current therefrom and outputting a clock signal having a frequency proportionate to the control current; and an output stage coupled to receive the clock signal and receiving an input voltage and outputting an output voltage, the output voltage and the input voltage having a ratio that is determined by the clock signal.

One advantage of a preferred embodiment of the present invention is that it provides a variable frequency to provide for small internal resistance, low output voltage ripple and quiescent current while allowing for small external capacitors.

Another advantage of a preferred embodiment of the present invention is that it defines a frequency sweep range that increases efficiency and decreases power loss.

Yet another advantage of a preferred embodiment of the present invention is that it provides for a cost effective device by allowing for the use of cheaper external components.

A further advantage of a preferred embodiment of the present invention is that it can flexibly operate with a variety of external components.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter, which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the concepts and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying figures, in which:

FIGS. 1A-1B illustrate a prior art charge pump and its principle of operation;

FIG. 2 is a simple block diagram of the present invention;

FIG. 3 is a block diagram of a preferred embodiment of the present invention; and

FIG. 4 is a schematic of a preferred embodiment of the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The making and using of the presently preferred embodiment is discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the invention.

FIG. 2 is a simple block diagram of an inductorless DC/DC converter 20 implementing a frequency control circuit of the present invention. The converter 20 includes a frequency control circuit 22 coupled to a variable frequency oscillator (VFO) 24 to control the frequency of a charge pump output stage 26. The frequency control circuit 22 measures an input voltage  $V_{in}$  and output voltage  $V_{out}$  from the charge pump output stage 26 and controls the frequency of the oscillator 24 utilizing the ratio of the input voltage  $V_{in}$  to the output voltage  $V_{out}$ .

FIG. 3 is a block diagram of a preferred embodiment frequency control circuit 22 of the present invention. The frequency control circuit 22 comprises a first voltage-to-current converter 32 and a second voltage-to-current converter 34. An input voltage  $V_{in}$  and output voltage  $V_{out}$  of the charge pump output stage 26 are input into the first and second voltage-to-current converters 32 and 34. The voltage-to-current converters 32 and 34 are matched, i.e. they are identical in structure and function in order to provide accurate measurement of the ratio between the input voltage  $V_{in}$  and the output voltage  $V_{out}$ .

The input voltage  $V_{in}$  is input into the first voltage-to-current converter 32 and the output voltage  $V_{out}$  is input into the second voltage-to-current converter 34. The input and output voltages,  $V_{in}$  and  $V_{out}$ , are converted to first and second currents  $I_{(+)}$  and  $I_{(-)}$ , respectively, which are proportional in magnitude to their corresponding voltages. The first voltage-to-current converter 32, however, is connected to an

inverter 36 that converts the first current  $I_{(+)}$  to an inverted current  $I_{INV}$ . The first current  $I_{(+)}$  is inverted because the converters 32 and 34 each produce sink currents that cannot be compared. The inverter 36, then, facilitates the production of the inverted current  $I_{INV}$  (i.e. a source current) that can be compared to the second current  $I_{(-)}$  (i.e. a sink current). The inverter 36 and second voltage-to-current converter 34 are coupled to a regulation circuit 38 that is in turn coupled to the VFO 24 (shown in FIG. 2).

The regulation circuit 38 measures the ratio between the input and output voltages  $V_{in}$  and  $V_{out}$ , respectively, and varies the frequency of the VFO 24 to facilitate a small internal resistance, low output voltage ripple at full load, and low quiescent current while allowing the use of small and inexpensive external capacitors. At light loads, the magnitude of the output voltage is at or close to the magnitude of the input voltage. Since the load current is small there is no problem to run with a low frequency even with small external capacitors. As shown by equation (3), the quiescent current  $I_Q$  would be minimal because of the low frequency. Also the voltage ripple is minimized, in view of equation (2), because the small load current offsets the low clock frequency and small output capacitance (produced by the small external capacitors). The resistance is not an issue because only a small percentage of voltage is lost since the load current is small and the product of load current and internal resistance is small as well.

However, when the load current increases, the output voltage tends to drop; thus the difference between the output voltage and input voltage increases as well. To compensate for this reduction in output voltage, the regulation circuit 38 signals the VFO 24 to run faster and thus run the output stage (i.e. converter) at an efficient level. At full load current the quiescent current is not an issue because it is just a small percentage of the load current and therefore generates only a small degradation of the efficiency. Thus the system runs with maximum frequency to guarantee a small internal resistance and a low output voltage ripple. The VFO 24 is coupled to an output stage that will provide the desired output as dictated by the application in which the device is used.

FIG. 4 is a schematic of a preferred embodiment of the present invention. The first voltage-to-current converter 32 comprises a first transistor MN1 and a second transistor MN2. The first and second transistors MN1, MN2 have gate nodes 40 that are coupled together and source nodes 42 that are tied to a ground node GND. The second transistor MN2 is coupled to the inverter 36, represented in this preferred embodiment as a current mirror comprising two PMOS transistors MP1 and MP2. A first resistor R1 is coupled between the first transistor MN1 and an input node 44 that receives the input voltage  $V_{in}$ .

The matched second voltage-to-current converter 34 comprises a third transistor MN11 and a fourth transistor MN12 having gate nodes 46 that are coupled together and source nodes 48 that are tied to the ground node GND. A second resistor R11 is coupled between the third transistor and the output node 50 that receives the output voltage  $V_{out}$ . The second resistor R11 is preferably matched in value to the first resistor R1. If, for example, first resistor R1 is smaller than second resistor R11, then second resistor R11 will produce an additional offset current which should not be generated when the input voltage is equal to the output voltage (i.e. there is no load current). The additional offset current will operate as a load current and cause the frequency control circuit 22 to operate improperly.

The inverter 36 produces the inverted current  $I_{INV}$ . The inverted current  $I_{INV}$  and second current  $I_{(-)}$  are summed to

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produce a net current  $I_{net}$ . Because the inverted current  $I_{NV}$  and second current  $I_{(-)}$  are of a magnitude that is proportional to their respective voltages, the net current  $I_{net}$  is of a magnitude that represents the difference of the input and output voltages  $V_{in}$  and  $V_{out}$ .

The net current is input into a preferred embodiment regulation circuit 38 that comprises multiple transistors, MN3-MN7 and MP3. The net current  $I_{net}$  is formed on the drain of transistor MN3. The regulation circuit 38 further comprises current sources that represent a maximum current  $I_{max}$  and a minimum current  $I_{min}$  that will be provided to the VFO 24. The minimum and maximum currents  $I_{min}$  and  $I_{max}$  provide the frequency sweep range of the VFO 24 that allows the converter to run efficiently with decreased loss of energy. The frequency of the VFO 24 is limited to a minimum frequency where the input and output voltages  $V_{in}$  and  $V_{out}$  are equal, that is the net current  $I_{net}$  is zero. If there was no designed minimum frequency, the VFO 24 would stop oscillating when the net current  $I_{net}$  was zero. Current source 52 prevents this by supplying the minimum current  $I_{min}$ . The VFO 24 is also limited to a maximum frequency to prevent the VFO 24 from running at frequencies at which no benefits are gained in efficiency and energy is loss.

Transistor MN5 is coupled to transistor MN3 to form a current mirror. Transistor MN5 operates to add the net current  $I_{net}$  to the minimum current  $I_{min}$ . The resulting current is the control current  $I_{cont}$  that is provided to run the VFO 24 at a rate that is proportional in magnitude to the ratio of the input and output voltages  $V_{in}$  and  $V_{out}$ . Transistor MN3 also forms a current mirror with transistor MN4. If transistors MN3 and MN4 are the same size, then the current on the drain of transistor MN4 is the same as that on transistor MN3. Thus, the net current  $I_{net}$  is mirrored onto the drain of transistor MN4. The drain of transistor MN4 is coupled to the gate of transistor MP3 allowing the net current  $I_{net}$  to be compared with the maximum current  $I_{max}$ . If the net current  $I_{net}$  is bigger than the maximum current  $I_{max}$ , then the gate of transistor MP3 becomes negative with respect to its source, MP3 switches on and turns on transistor MN6 (i.e. forces current via transistor MN6). Transistor MN6 turns on transistor MN7 that in turn sinks a portion of the net current  $I_{net}$  from transistor MN3 such that the addition of the net current  $I_{net}$  and the minimum current  $I_{min}$  never exceeds the maximum current  $I_{max}$ . In a preferred embodiment, the VFO 24 minimum frequency is 50 khz and maximum frequency is 500 khz.

Furthermore, the size of transistors MN3 and MN5 can be chosen to provide the necessary control loop sensitivity for the regulation circuit 38. If the VFO 24 sensitivity is not compatible with the sensitivity of the regulation circuit 38 (i.e. the VFO 24 can not detect the changes in control current produced by the regulation circuit 38), the net current can be amplified by a factor necessary to provide correct operation. For example, by choosing the size of transistor MN5 to be 5 times the size of MN3, then the sensitivity of the regulation circuit is increased by a factor of 5. Thus, the bigger the size of MN5, the smaller the output voltage drop you need for the same frequency modulation. However, caution must be taken in matching the voltage-to-current converters 32 and 34 to ensure that the sensitivity of the regulation circuit 38 is not bigger than a matching error, otherwise the frequency control circuit 22 will not operate correctly.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of

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the present application is not intended to be limited to the particular embodiments of the process, manufacture, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. An unregulated inductorless direct current to direct current converter comprising:

a first voltage-to-current converter configured to convert a first voltage to a first current;

a second voltage-to-current converter configured to convert a second voltage to a second current;

a regulation circuit coupled to the first and second voltage-to-current converters and configured to generate an output current proportional to the difference between the first and second currents;

a variable frequency oscillator coupled to the regulation circuit, the oscillator receiving as a control current the output current therefrom and outputting a clock signal having a frequency proportionate to the control current; and

an output stage coupled to receive the clock signal and receiving an input voltage and outputting an output voltage, the output voltage and the input voltage having a ratio that is determined by the clock signal.

2. The converter of claim 1 wherein the first voltage is the input voltage of the output stage and the second voltage is output voltage of the output stage.

3. The converter of claim 1 wherein the first current is inverted before it is input into the regulation circuit.

4. The converter of claim 3 wherein the inverter comprises a current mirror.

5. The converter of claim 1 wherein the first voltage-to-current converter comprises:

a first transistor and a second transistor having gate nodes coupled together and source nodes tied to a ground node; and

a resistor coupled between the first transistor and an input node that receives the input voltage;

whereby the first current is proportional in magnitude to the input voltage.

6. The converter of claim 5 wherein the second voltage-to-current converter comprises:

a third transistor and a fourth transistor having gate nodes coupled together and source nodes tied to a ground node; and

a resistor coupled between the third transistor and an output node that receives the output voltage;

whereby the second current is proportional in magnitude to the output voltage.

7. The converter of claim 1 wherein the first and second voltage-to-current converters are matched converters.

8. The converter of claim 1 further comprising a maximum current source that generates a maximum current.

9. The converter of claim 8 further comprising a minimum current source that generates a minimum current.

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10. The converter of claim 9 wherein the regulation circuit compares the maximum current and the control current which controls the frequency of the variable frequency oscillator to limit the control current to a value that is less than or equal to the maximum current but greater than the minimum current. 5

11. The converter of claim 1 wherein the regulation circuit comprises multiple transistors to control the sensitivity of the variable frequency oscillator.

12. The converter of claim 9 wherein the maximum and minimum currents define the frequency sweep range of the variable frequency oscillator.

13. A control circuit for a variable frequency oscillator comprising:

a first voltage-to-current converter configured to convert a first voltage to a first current; 15

a second voltage-to-current converter configured to convert a second voltage to a second current; and

a regulation circuit coupled to the first and second voltage-to-current converters and configured to generate an output current proportional to the difference between the first and second currents. 20

14. The circuit of claim 13 wherein the first voltage-to-current converter comprises:

a first transistor and a second transistor having gate nodes coupled together and source nodes tied to a ground node; and

a resistor coupled between the first transistor and an input node that receives the input voltage;

whereby the first current is proportional in magnitude of the input voltage. 25

15. The circuit of claim 13 wherein the second voltage-to-current converter comprises:

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a third transistor and a fourth transistor having gate nodes coupled together and source nodes tied to a ground node; and

a resistor coupled between the third transistor and an output node that receives the output voltage;

whereby the second current is proportional in magnitude to the output voltage.

16. The circuit of claim 13 wherein the first and second voltage-to-current converters are matched converters.

17. The circuit of claim 13 wherein the regulation circuit comprises multiple transistors to control the sensitivity of the variable frequency oscillator.

18. The circuit of claim 13 further comprising an inverter that inverts the first current before the first current is input into the regulation circuit.

19. The circuit of claim 18 wherein the inverter comprises a current mirror.

20. The circuit of claim 13 further comprising a maximum current source that generates a maximum current.

21. The circuit of claim 20 further comprising a minimum current source that generates a minimum current.

22. The converter of claim 21 wherein the regulation circuit compares the maximum current and the control current which controls the frequency of the variable frequency oscillator to limit the control current to a value that is less than or equal to the maximum current but greater than the minimum current. 30

23. The circuit of claim 21 wherein the maximum and minimum currents define the frequency sweep range of the variable frequency oscillator.

\* \* \* \* \*



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 (45) **Date of Reissued Patent:** Apr. 3, 2001

(54) **RING OSCILLATOR USING CURRENT MIRROR INVERTER STAGES**

4,210,882 7/1980 Roza et al. .... 333/166  
 4,368,480 1/1983 Senturia .... 357/25  
 4,408,168 10/1983 Higuchi .... 331/57

(75) **Inventors:** Trevor K. Monk, Chepstow; Andrew M. Hall, Edinburgh, both of (GB)

#### FOREIGN PATENT DOCUMENTS

0187572 \* 7/1986 (EP) .  
 0 187 572 A1 7/1986 (EP) .  
 0407082 \* 1/1991 (EP) .  
 0 407 082 A2 1/1991 (EP) .

(73) **Assignee:** STMicroelectronics Limited, Marlow (GB)

#### OTHER PUBLICATIONS

(21) **Appl. No.:** 09/096,693

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(86) **PCT No.:** PCT/GB94/00890

§ 371 Date: May 5, 1995

§ 102(e) Date: May 5, 1995

(87) **PCT Pub. No.:** WO94/26025

PCT Pub. Date: Nov. 10, 1994

#### Related U.S. Patent Documents

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**Issued:** Jun. 11, 1996  
**Appl. No.:** 08/360,699  
**Filed:** May 5, 1995

#### (30) Foreign Application Priority Data

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(51) **Int. Cl.<sup>7</sup>** ..... H03B 5/00

(52) **U.S. Cl.** ..... 331/57; 331/108 R; 331/177 R; 327/278; 327/281; 327/285; 327/288

(58) **Field of Search** ..... 331/57, 108 R, 331/177 R; 327/272, 278, 281, 285, 288

#### (56) References Cited

##### U.S. PATENT DOCUMENTS

3,350,659 10/1967 Henn ..... 331/57

Bennett et al., "Sub-Nanosecond Bipolar LSI" *1<sup>st</sup> I.E.E. European Solid State Circuits Conference*, London, GB, pp. 34-35, 1975.

*IBM Technical Disclosure Bulletin*, 32:(12), pp. 149-151, May 1990.

*IBM Technical Disclosure Bulletin*, 31:(2), pp. 154-156, Jul. 1988.

Kumar, U. and S.P. Suri, "A simple digital 2<sup>n</sup> frequency multiplier," *Int. J. Electronics* 48:(1), pp. 43-45, 1980.

McGahee, T., "Pulse-frequency doubler requires no adjustment," *Electronics* 48:(8), p. 149, Apr. 17, 1975.

Ware, et al., "THPM 14.1: a 200 MHz CMOS Phase-Locked Loop With Dual Phase Detectors," *IEEE International Solid-State Circuits Conference*, New York, USA, pp. 192-193 and 338, 1989.

\* cited by examiner

*Primary Examiner*—Siegfried H. Grimm

(74) *Attorney, Agent, or Firm*—Theodore E. Galanthay; E. Russell Tarleton; Seed IP Law Group PLLC

#### (57) ABSTRACT

A ring oscillator having an odd number of single ended stages, each stage including two transistors connected as a current mirror. The stage provides for low-voltage performance and improved process tolerance characteristics.

25 Claims, 3 Drawing Sheets

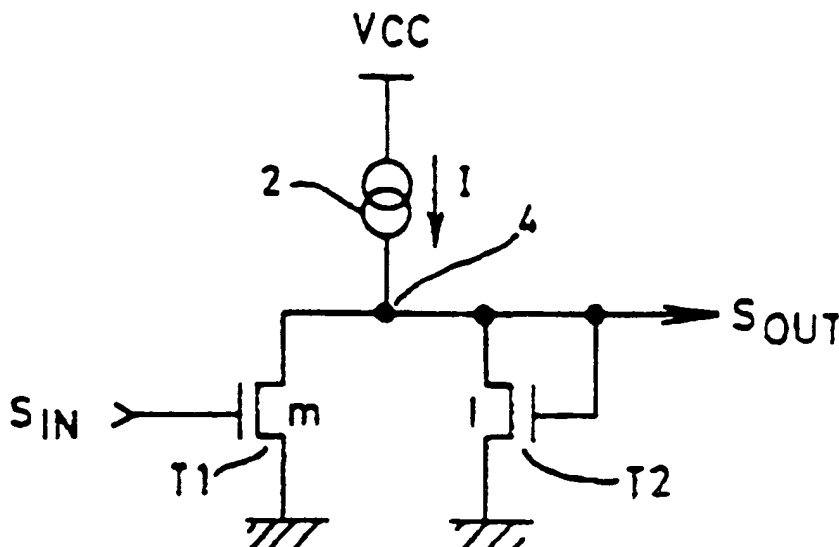


FIG. 1

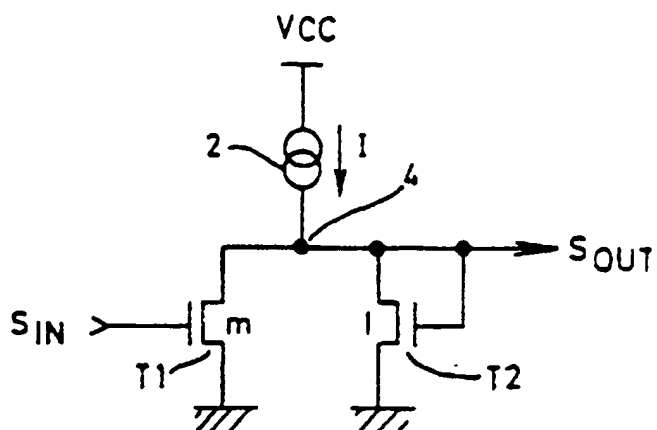


FIG. 1a

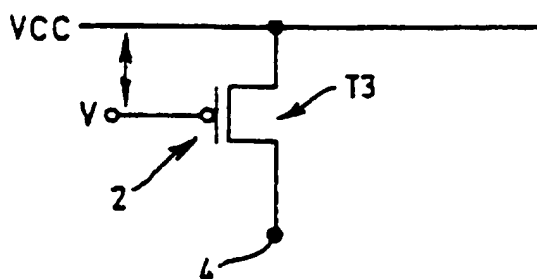


FIG. 2

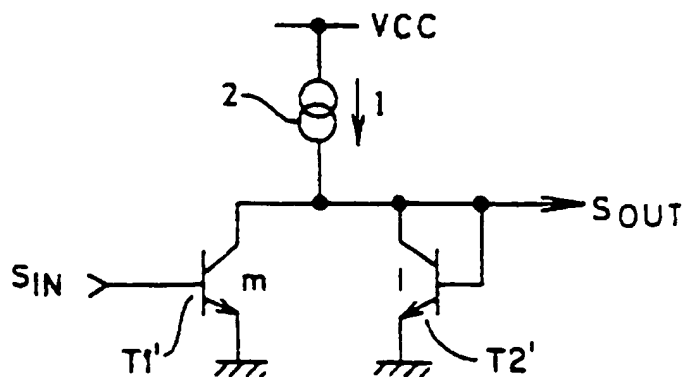




FIG. 3

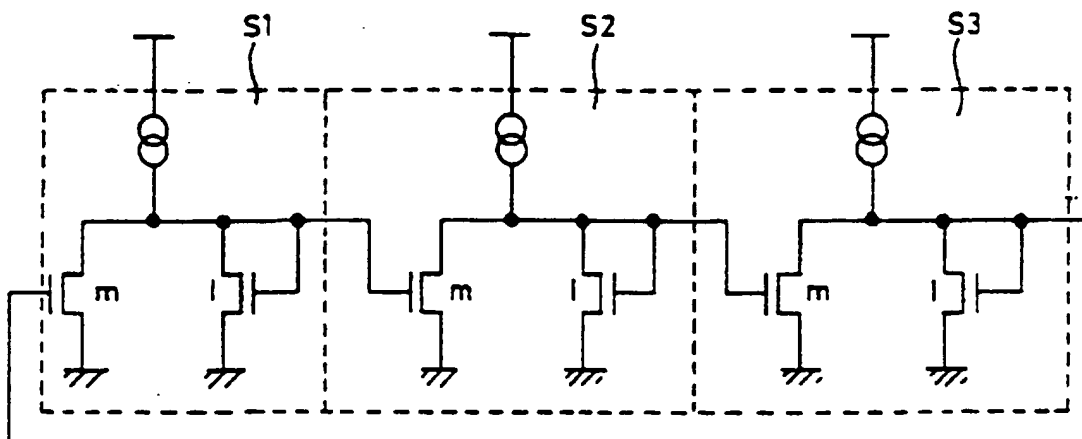
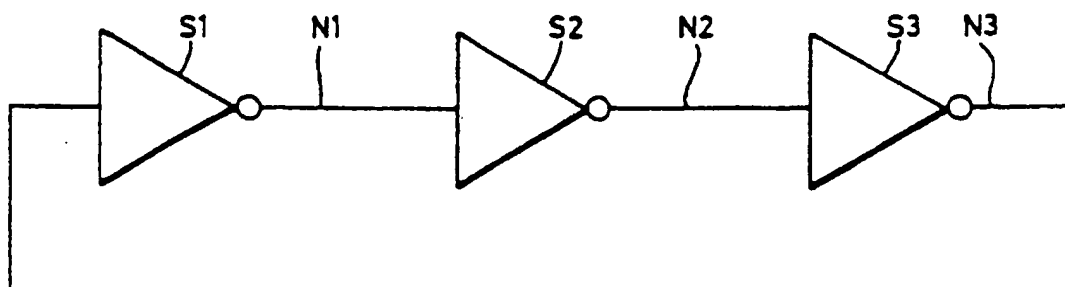
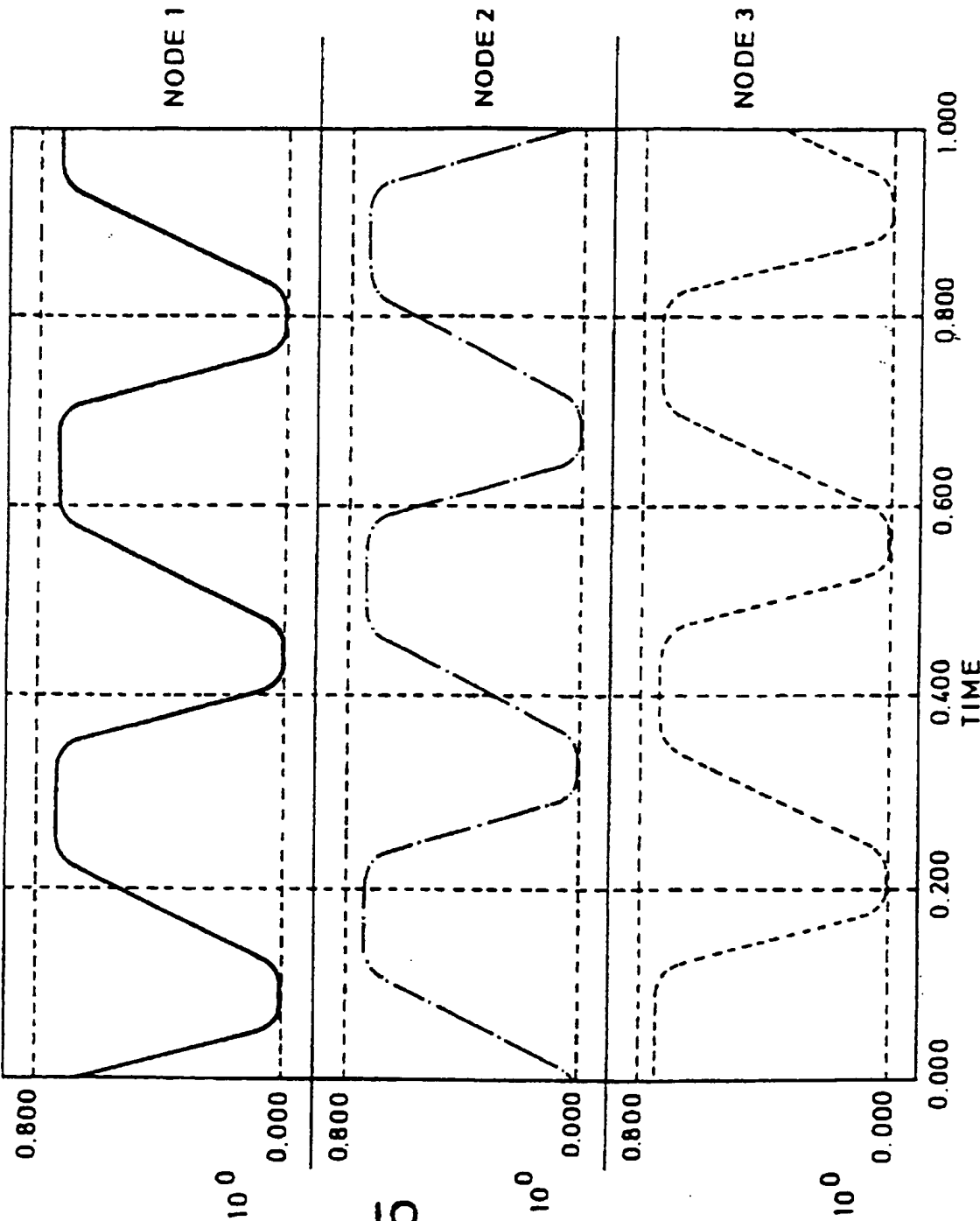


FIG. 4





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## RING OSCILLATOR USING CURRENT MIRROR INVERTER STAGES

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

### FIELD OF THE INVENTION

This invention relates to an oscillator and more particularly to a ring oscillator.

### BACKGROUND OF THE INVENTION

New manufacturing processes and new applications are forcing power supplies to lower voltages (3.3 v now, with 2.4 v and 1.5 v being expected soon). Advanced Phase-Locked Loops require stable oscillators which may be varied in frequency by a control signal.

To help achieve frequency stability, oscillators integrated into a noisy VLSI environment often use a regulator to generate a quiet power supply. This usually has to be at an even lower voltage than the normal power supply.

There is thus a desire to provide oscillators which can work at these very low supply voltages and still produce high quality, high frequency output signals.

Reference is made to IBM Technical Disclosure Bulletin, Vol. 31, No. 2, July 1988, pages 154 to 156 "CMOS Ring Oscillator with controlled frequency" which describes a ring oscillator using CMOS transistors and is designed to give an almost sinusoidal output. This design suffers from stability problems outside a narrow range of frequencies. In particular, as the frequency increases, the amplitude decreases and it becomes difficult to convert the signal to CMOS levels.

### SUMMARY OF THE INVENTION

According to the present invention there is provided a ring oscillator comprising a plurality of oscillator stages, each stage comprising a first and second transistors. The first transistor has a controllable path connected between an output node and a reference voltage and a control node acting as an input node to the stage. The second transistor has a controllable path connected between the output node and the reference voltage and a control node connected to the output node. The gain of each stage is selectively determined by the ratio of the widths of the first and second transistors to produce an output signal having a sawtooth or trapezoidal waveform. Each stage further comprise a respective current source which controls the speed of the stage and which is connected to the output node. The input node of one stage is connected to the output node of a preceding stage to form a ring and the number of stages is selected so that there is a total phase shift of  $360^\circ$  around the ring at the frequency of operation.

For transistors of the same length, the width of the first transistor can be set to  $m$  times the width of the second transistor where  $m > 1$  to determine the d.c. gain of the stage. This ratio  $m$  determines the shape of the waveform output by the oscillator. The higher the value of  $m$ , the more the waveform moves away from a sinusoid. For a three stage oscillator, a ratio of  $m$  close to 2 produces a substantially sinusoidal output. The present invention uses a ratio higher than 2 and preferably with a minimum value of 2.5. In practice the smallest value that can be selected to provide an appropriately shaped waveform will be selected. The maxi-

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imum value of  $m$  is limited by practical considerations and particularly layout considerations. A practical maximum value for  $m$  is likely to be about 10.

The first and second transistors can be n-channel field effect devices having a gate as the control node and the source-drain path as the controllable path. As the transistors are of the same type, process variations affect the transistors in the same manner. The maximum frequency of operation is limited only by the ratio of gain to gate capacitance.

The current source can comprise a p-channel transistor gated by a control voltage.

The first transistor is preferably operated in its saturation region.

The current sources of each stage can either be controlled by a common control signal or by respective different control signals.

The present oscillator can operate at voltages down to a level just above the threshold voltages of the transistors.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made by way of example to the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a low-voltage inverting gain stage in MOS technology;

FIG. 1a is a circuit diagram of an implementation of a current source;

FIG. 2 is a circuit diagram of a low-voltage inverting gain stage in bipolar technology;

FIG. 3 is a diagram showing the transistor structure of a ring oscillator;

FIG. 4 is an equivalent logical schematic for FIG. 3; and

FIG. 5 shows typical waveforms for the 3-stage ring oscillator of FIGS. 3 and 4.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows a low-voltage inverting gain stage in MOS technology. The stage comprises first and second transistors T1, T2 which have their drains connected together and their sources connected to ground. The gate of the first transistor T1 acts as the input  $S_{in}$  for the stage and the gate of the second transistor T2 acts as the output  $S_{out}$ . The gate of the second transistor T2 is connected to its drain. Each stage is controlled by a control current  $I$  which is generated by a current source 2. The current source 2 is connected between a supply voltage  $V_{cc}$  and the drains of the first and second transistors T1, T2. The common node between the current source 2 and the drains of the transistors T1 and T2 is denoted 4. As shown in FIG. 1a, the current source 2 can comprise a p-channel MOS field effect transistor T3 with its source/drain path connected between the supply voltage  $V_{cc}$  and the node 4 and its gate connected to receive a control signal  $V$  which is taken with respect to the supply voltage  $V_{cc}$ . In the following discussion, it will readily be apparent that where reference is made to the control current  $I$ , this can be taken in practice as being derived from the control voltage  $V$ . The stage also has capacitance  $C$ , the largest component of which is the gate capacitance of the transistors connected to the output  $S_{out}$ .

The ratio of gains of the transistors T1, T2 is indicated as " $m$ ". The value of  $m$  controls the relative charge and discharge rates of the output node  $S_{out}$ , and thus determines

the gain of the stage. The speed of the stage (and thus the phaseshift at the frequency of operation) is readily controlled by varying the current  $I$  supplied by the current source 2.

FIG. 2 shows the low-voltage inverting gain stage in bipolar technology. This also has excellent low-voltage operation characteristics and the speed can be controlled using a current source 2 in precisely the same way. Although the rest of this specification refers to MOS circuits, it should be understood that the same idea can easily be applied to bipolar technology.

In FIG. 2, the first and second transistors are denoted  $T_1$  and  $T_2$  and are connected in the same way as for FIG. 1, where gates correspond to bases, drains correspond to collectors and sources correspond to emitters.

FIG. 3 illustrates a 3-stage ring oscillator, the three stages being denoted  $S_1, S_2, S_3$ . Each stage  $S_1, S_2, S_3$  is as illustrated in FIG. 1. Of course, a similar ring oscillator could be produced using the stages of FIG. 2. FIG. 4 shows the ring oscillator in an equivalent logical schematic. Each stage is a so-called single-ended stage, that is with a single input and a single output and is inverting. As is well known in the design of ring oscillators, for oscillation to occur it can be shown that there must be:

- (i) an odd number  $n$  of stages
- (ii) minimum of three stages
- (iii) if all stages are identical and have a gain ratio of " $m$ ", then

$$m > 1/\cos(\pi/n)$$

where

$$\pi = 3.14 \dots$$

$n$  = number of stages

and

$m$  = gain of each stage

For a 3-stage ring, the formula above gives  $m > 2$ .

Where the transistors are of the same length, the gain  $m = W(T_1)/W(T_2)$ , where  $W$  is the width of a transistor.

Thus, by use of an appropriate layout, the parameter  $m$  can be made substantially independent of manufacturing process variables which would tend to affect the width of both transistors by corresponding amounts.

The required value for  $m$ , and hence the transistor sizes, is selected to satisfy small signal and large signal design requirements to provide a sawtooth or trapezoidal waveform. A system designed to produce these waveforms produces a more stable output amplitude from the oscillator across all operating frequencies. A more stable amplitude over a wide range of operating frequencies provides a signal which can be more reliably and easily converted to CMOS levels over a wide range of frequencies.

FIG. 5 shows the waveforms for the 3-stage oscillator of FIG. 4 when  $m=3$ . Node 1, node 2 and node 3 are denoted  $N_1, N_2$  and  $N_3$  in FIG. 4.

The frequency of oscillation of the ring can be controlled by the control current  $I$ . In a symmetrical arrangement, each stage has the same phase shift at the frequency of operation (equal to  $180^\circ/n$  for inverting stages) and receives a common control signal so that the control currents  $I$  are the same. However, the phase shift can differ for each stage provided that the complete phase shift in the loop is  $360^\circ$  at the frequency of oscillation. In this case, the control currents  $I$  for the individual stages can be independently varied.

We claim:

1. A ring oscillator comprising:

a plurality of oscillator stages, each stage comprising first and second transistors, wherein the first transistor has a controllable path connected between an output node and a reference voltage and a control node acting as an input node to the stage and wherein the second transistor has a controllable path connected between the output node and the reference voltage and a control node connected to the output node, the gain of each stage being selectively determined by the ratio of the widths of the first and second transistors to produce an output signal having a sawtooth or trapezoidal waveform and each stage further comprising a respective current source which controls the speed of the stage and which is connected to said output node, wherein the input node of one stage is connected to the output node of a preceding stage to form said ring oscillator and wherein the number of stages is selected so that there is a total phase shift of  $360^\circ$  around the ring at the frequency of operation.

2. A ring oscillator according to claim 1, wherein the first and second transistors are n-channel field effect devices having a gate as the control node and a source/drain path as the controllable path.

3. A ring oscillator according to claim 1, wherein the first and second transistors are bipolar transistors in which the base is the control node and the controllable path extends between a collector and emitter.

4. A ring oscillator according to claim 1, wherein the current source comprises a p-channel MOS field effect transistor gated by a control voltage.

5. A ring oscillator according to claim 2 wherein the current source comprises a p-channel MOS field effect transistor gated by a control voltage.

6. A ring oscillator according to claim 3 wherein the current source comprises a p-channel MOS field effect transistor gated by a control voltage.

7. A ring oscillator having improved process tolerance characteristics, said ring oscillator comprising:

a plurality of oscillator stages, each stage having a gain, a speed, and an operation frequency wherein an input node of one stage is coupled to an output node of a preceding stage to form a ring, and wherein the number of stages is selected so there is a total phase shift of  $360^\circ$  around the ring at the operation frequency, each stage including:

a first transistor having a control node, and a path controlled by the control node, the path coupling a reference voltage to the output node of said stage, wherein the control node is coupled to the input node of said stage;

a second transistor having a control node coupled to the output node of said stage and a controllable path which couples the reference voltage to the output node, wherein the gain of said stage is selectively determined by the ratio of widths of said first transistor and said second transistor, and wherein an output signal of the stage is at least one of a sawtooth waveform and a trapezoidal waveform; and

a current source, which controls the speed of the stage, coupled to the output node.

8. An oscillator for producing a periodic waveform, the oscillator comprising:

a first, a middle, and a last serially coupled stage, each stage having an input terminal and an output terminal and the output terminal of the last stage coupled to the input terminal of the first stage, at least one stage including:

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an input transistor coupled between the output terminal and a reference voltage, and having a control terminal coupled to the input terminal,

a second transistor coupled between the output terminal and the reference voltage, and having a control terminal coupled to the output terminal,

a current source coupled to the output terminal, and wherein a ratio of the gain of the input transistor to the second transistor is greater than 2.

9. The oscillator of claim 8 wherein the input and second transistors comprise respective MOS transistors and wherein a drain of the input transistor is coupled to the output terminal, a gate of the input transistor is coupled to the input terminal, and wherein both a drain and gate of the second transistor are coupled to the output terminal.

10. The oscillator of claim 9 wherein the input and second transistors have respective first and second widths, wherein the ratio of the first width to the second width is greater than 2.

11. The oscillator of claim 8 wherein the input and second transistors comprise respective bipolar transistors and wherein a collector of the input transistor is coupled to the output terminal, a base of the input transistor is coupled to the input terminal, and wherein both a collector and base of the second transistor are coupled to the output terminal.

12. The oscillator of claim 11 wherein the ratio of the gain of the input transistor to the second transistor is a ratio of an area of the input transistor to the area of the second transistor.

13. The oscillator of claim 8 wherein the ratio is at least 2.5.

14. The oscillator of claim 8 wherein the ratio is selected such that at least one of the stages produces a sawtooth waveform at its output terminal.

15. The oscillator of claim 8 wherein the ratio is selected such that at least one of the stages produces a trapezoidal waveform at its output terminal.

16. The oscillator of claim 8 wherein the current source comprises a PMOS transistor having a drain coupled to the output terminal and having a gate coupled to a control voltage.

17. The oscillator of claim 8 wherein the current source comprises a bipolar transistor having a base coupled to a control voltage.

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18. The oscillator of claim 8 wherein the speed of the at least one stage is controlled by the current source.

19. An oscillator for producing a periodic waveform, the oscillator comprising:

at least three stages each having an input terminal and an output terminal, wherein the input terminal of each stage is coupled to the output terminal of another stage so as to constitute a ring, at least one stage including: an input transistor coupled between the output terminal and a supply voltage, and having a control terminal coupled to the input terminal, a second transistor coupled between the output terminal and the supply voltage, and having a control terminal coupled to the output terminal, a current source coupled to the output terminal, and wherein a gain of the at least one stage is approximately 2.

20. The oscillator of claim 19 wherein the input and second transistors comprise respective MOS transistors and wherein a drain of the input transistor is coupled to the output terminal, a gate of the input transistor is coupled to the input terminal, and wherein both a drain and gate of the second transistor are coupled to the output terminal.

21. The oscillator of claim 20 wherein the input and second transistors have respective first and second widths, wherein the ratio of the first width to the second width is greater than 2.

22. The oscillator of claim 19 wherein the input and second transistors comprise respective bipolar transistors and wherein a collector of the input transistor is coupled to the output terminal, a base of the input transistor is coupled to the input terminal, and wherein both a collector and base of the second transistor are coupled to the output terminal.

23. The oscillator of claim 22 wherein the ratio of area of the input transistor to the second transistor is greater than 2.

24. The oscillator of claim 19 wherein the gain is selected such that at least one of the stages produces a sawtooth waveform at its output terminal.

25. The oscillator of claim 19 wherein the gain is selected such that at least one of the stages produces a trapezoidal waveform at its output terminal.

\* \* \* \* \*



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**Umezawa et al.**

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(45) **Date of Patent:** **Feb. 27, 2001**

(54) **BOOSTER CIRCUIT AND SEMICONDUCTOR MEMORY DEVICE HAVING THE SAME**

(75) Inventors: **Akira Umezawa; Shigeru Atsumi,**  
both of Yokohama; **Hironori Banba,**  
Kamakura, all of (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba, Kawasaki**  
(JP)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Feb. 11, 2000**

**Related U.S. Application Data**

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**(30) Foreign Application Priority Data**

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(51) Int. Cl.<sup>7</sup> ..... **G11C 7/00**

(52) U.S. Cl. .... **365/226; 365/189.11; 327/536;**  
327/537

(58) Field of Search ..... **365/226, 189.11;**  
327/536, 537

**(56) References Cited**

**U.S. PATENT DOCUMENTS**

4,837,466 6/1989 Kanauchi ..... 307/605

5,499,209	3/1996	Oowaki et al. ....	365/189.11
5,589,793	12/1996	Kassapian .....	327/536
5,642,072	6/1997	Miyamoto et al. ....	327/535
5,644,534	7/1997	Soejima .....	365/185.23
5,650,741	7/1997	Nakamura et al. ....	327/327
5,812,018	9/1998	Sudo et al. ....	327/537
5,815,446	9/1998	Tobita .....	365/189.09
5,841,703	11/1998	Wojciechowski .....	365/189.09

*Primary Examiner*—Richard Elms

*Assistant Examiner*—Van Thu Nguyen

(74) *Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.

**(57) ABSTRACT**

In a booster circuit, a gate of an input-side transistor whose end is supplied with a power supply voltage is supplied with an inverted signal of a signal supplied to a signal input terminal of a booster unit at a first stage or supplied with an AND signal of the inverted signal and a booster circuit activation signal. Therefore, when the transistor at the first stage operates, the input-side transistor is turned off. Accordingly, a back flow of a current from inside the booster circuit to a power supply is prevented, so that the efficiency of the booster circuit can be improved. Further, fluctuations of the output voltage are not brought about even when the power supply voltage greatly fluctuates, so that the reliability of peripheral elements and memory cells can be improved and the allowable range of an external power supply voltage can be widened.

**17 Claims, 6 Drawing Sheets**

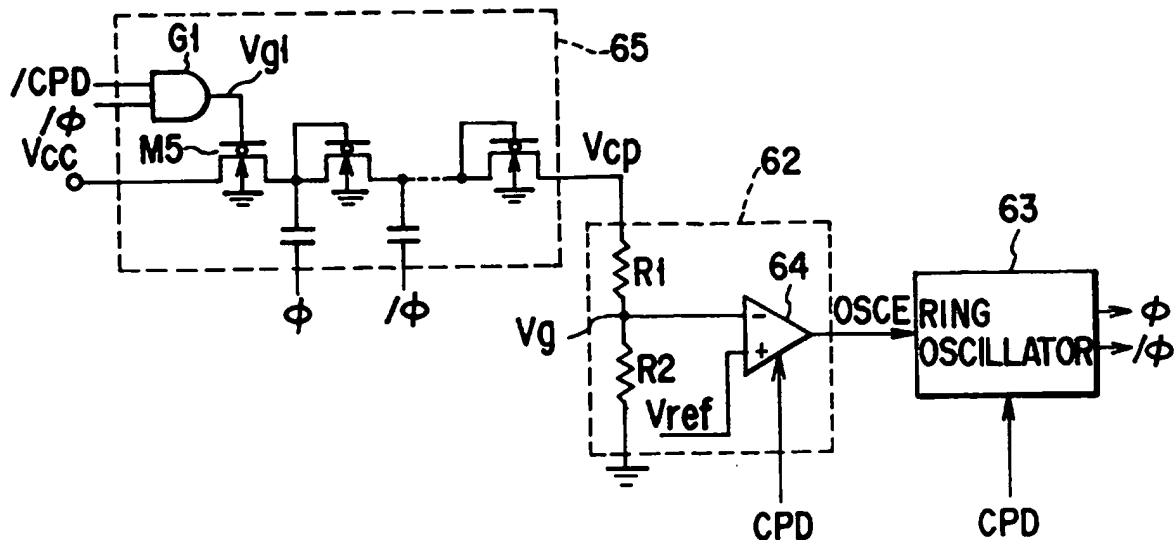


FIG. 1  
(PRIOR ART)

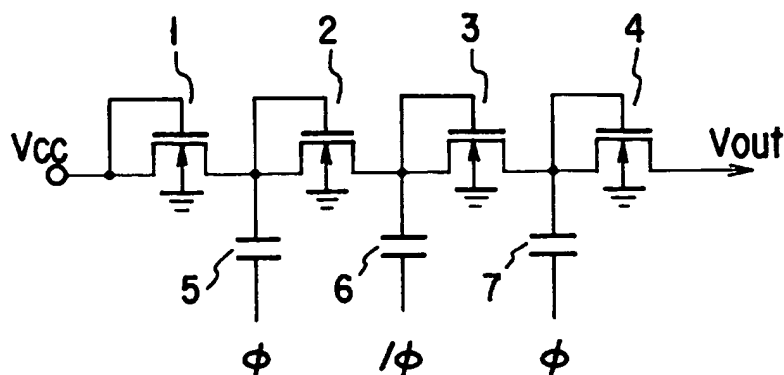


FIG. 2  
(PRIOR ART)

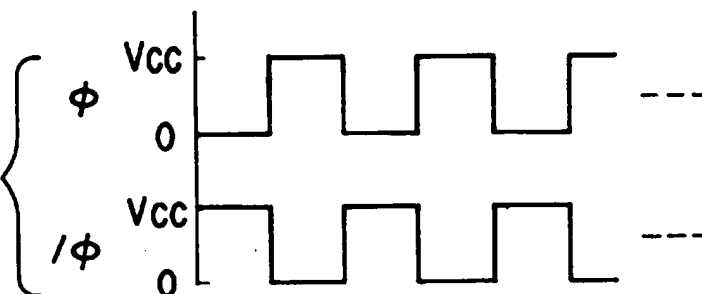


FIG. 3  
(PRIOR ART)

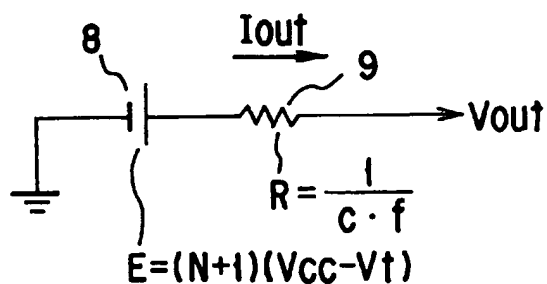
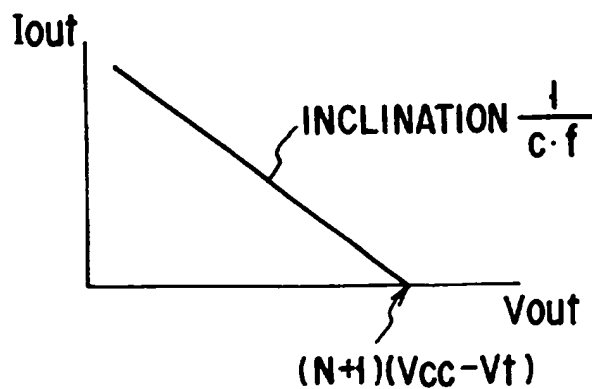
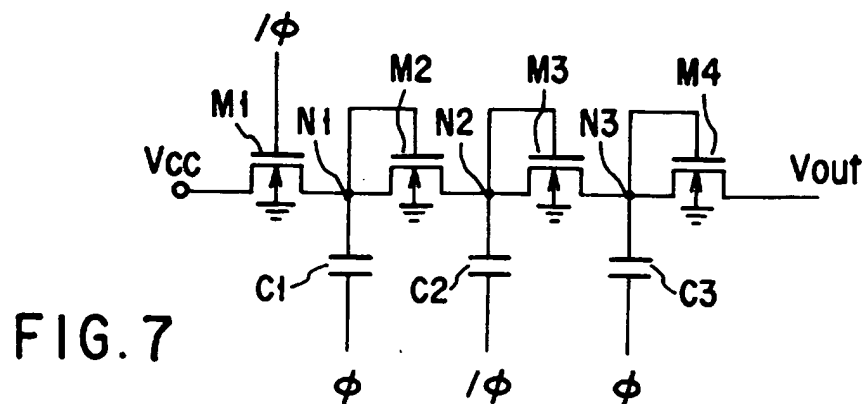
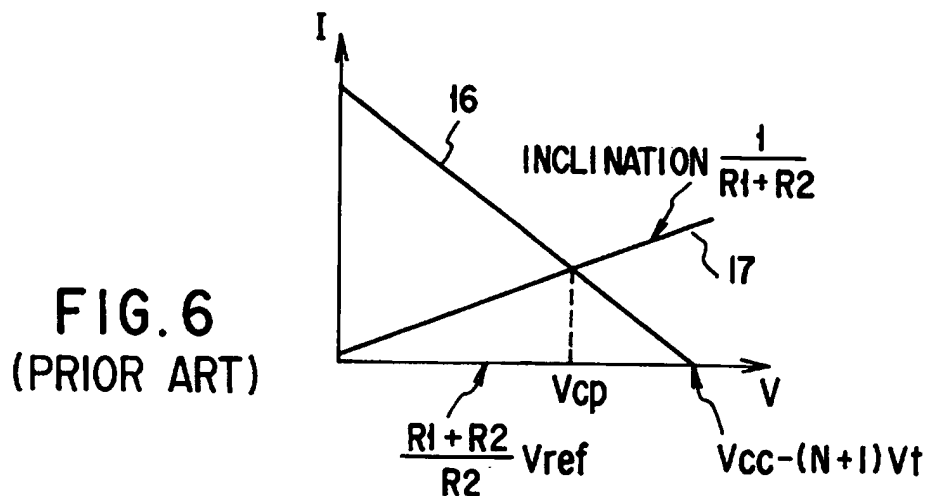
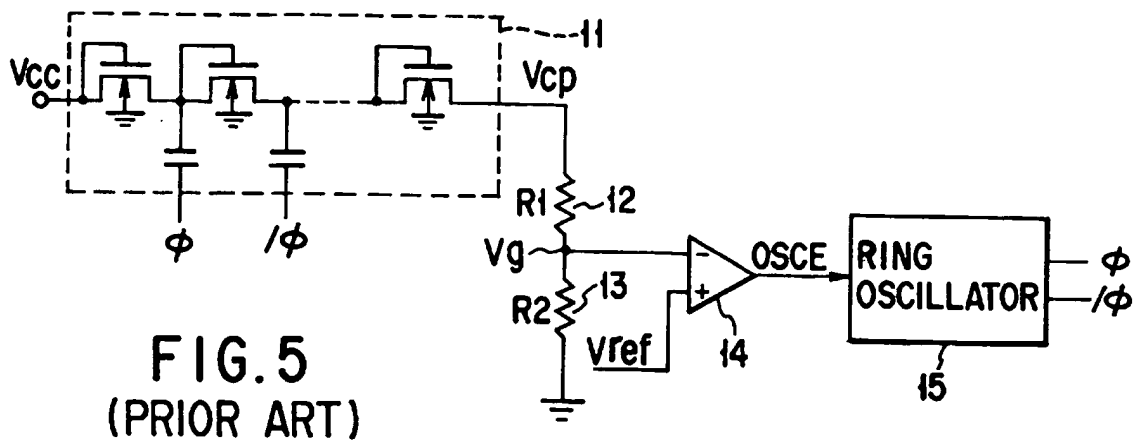
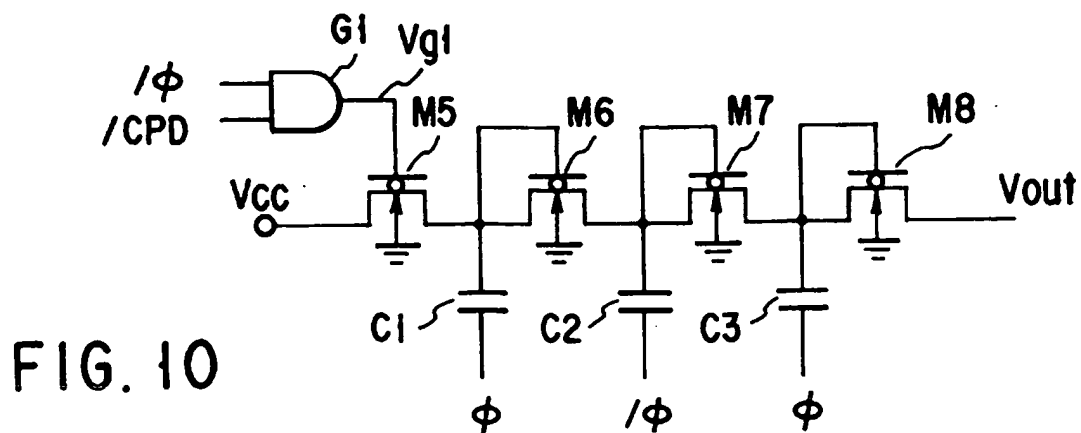
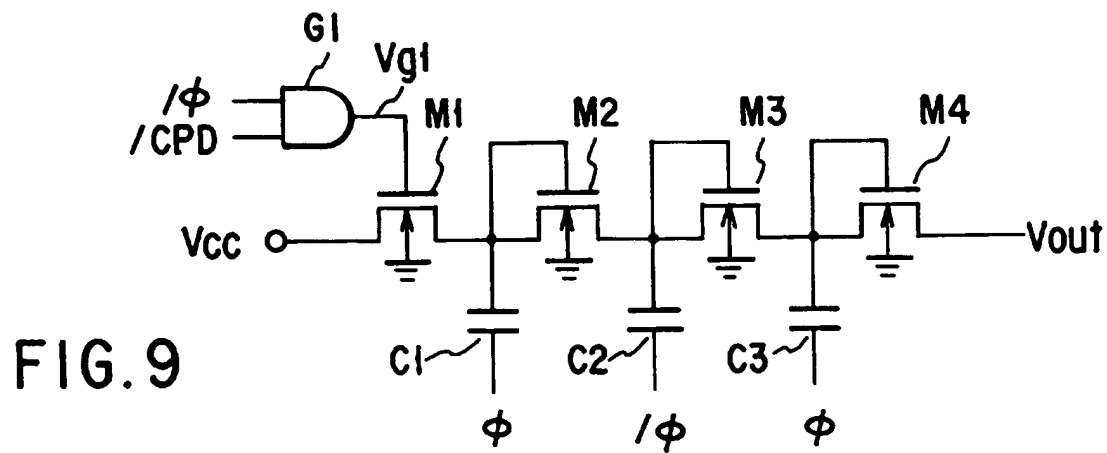
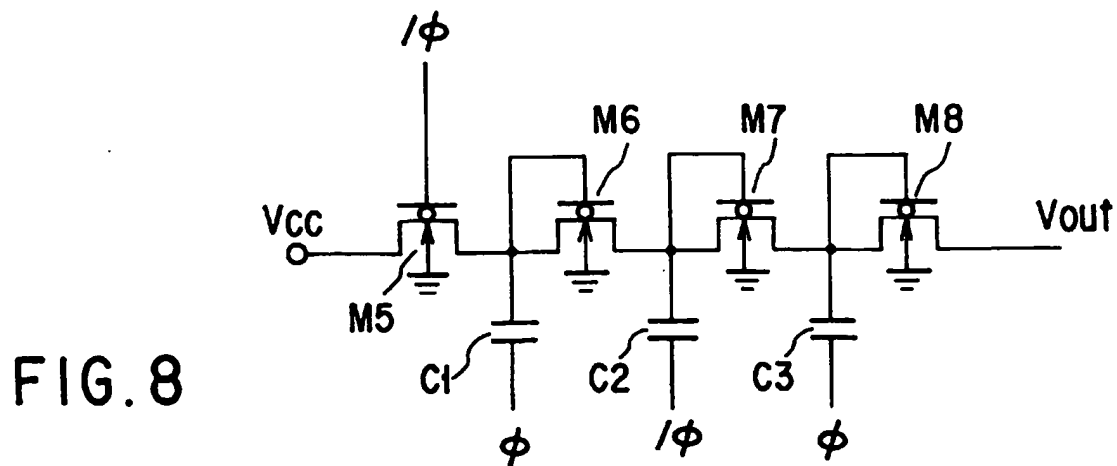


FIG. 4  
(PRIOR ART)









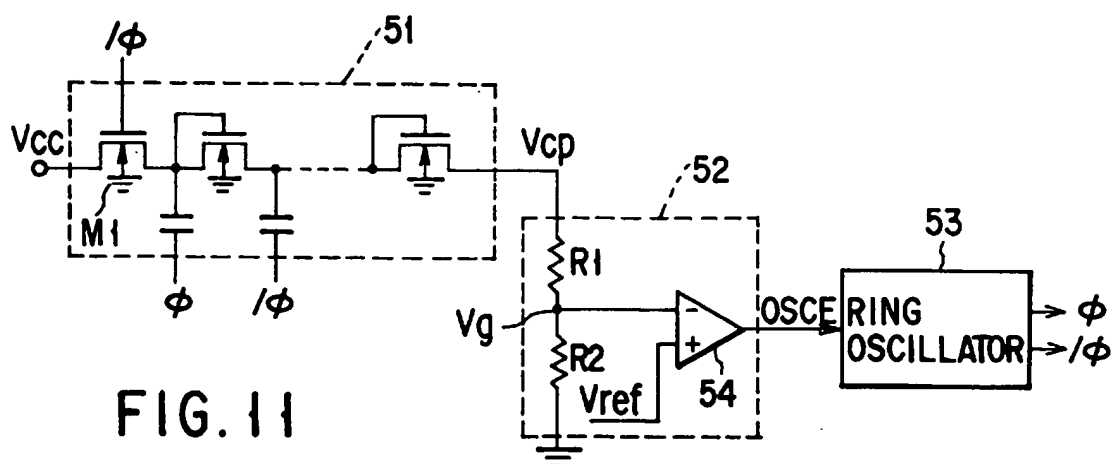


FIG. 11

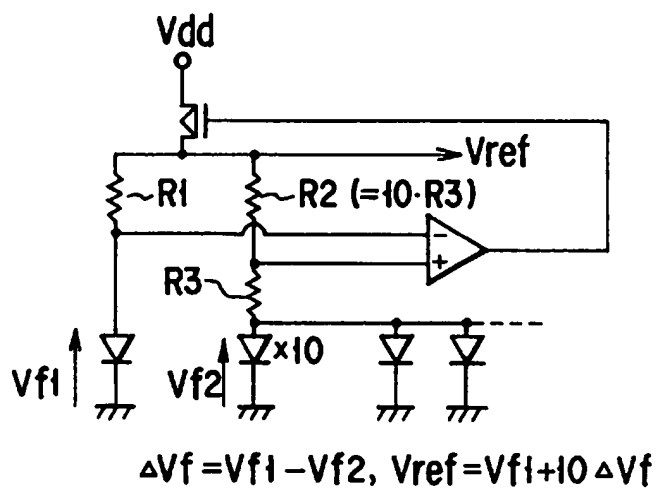


FIG. 12

$$\Delta V_f = V_{f1} - V_{f2}, V_{ref} = V_{f1} + 10 \Delta V_f$$

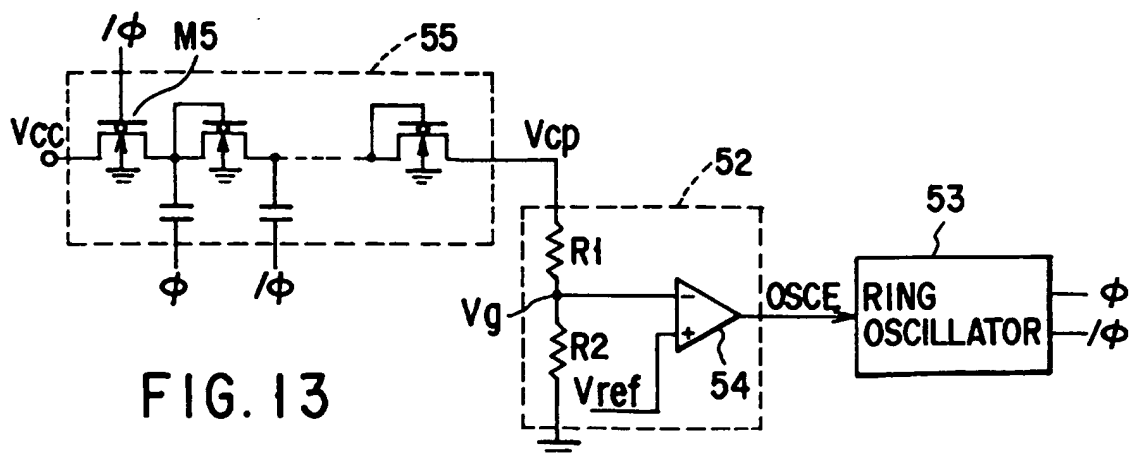


FIG. 13

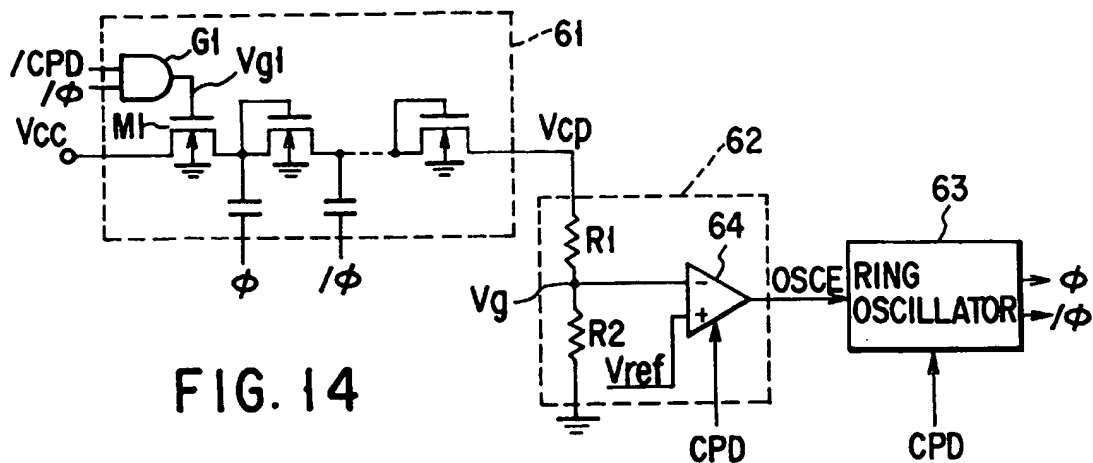


FIG. 14

	$\phi$	$/\phi$	Vgl	OSCE
CPD="H"	UNCHANGED	UNCHANGED	L	L
CPD="L"	CHANGED UNCHANGED	CHANGED UNCHANGED	CHANGED L	H (Vg < Vref) L (Vg > Vref)

FIG. 15

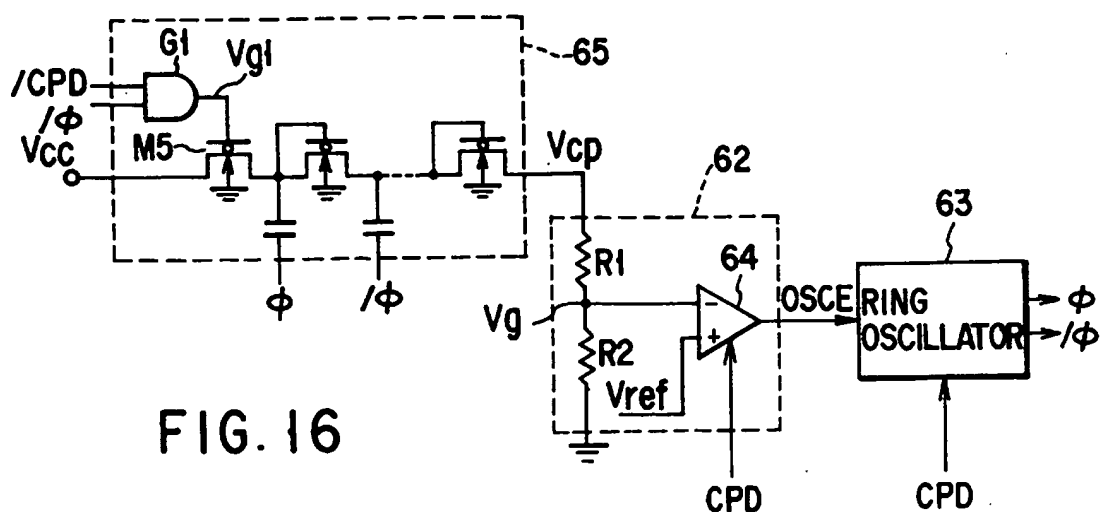


FIG. 16

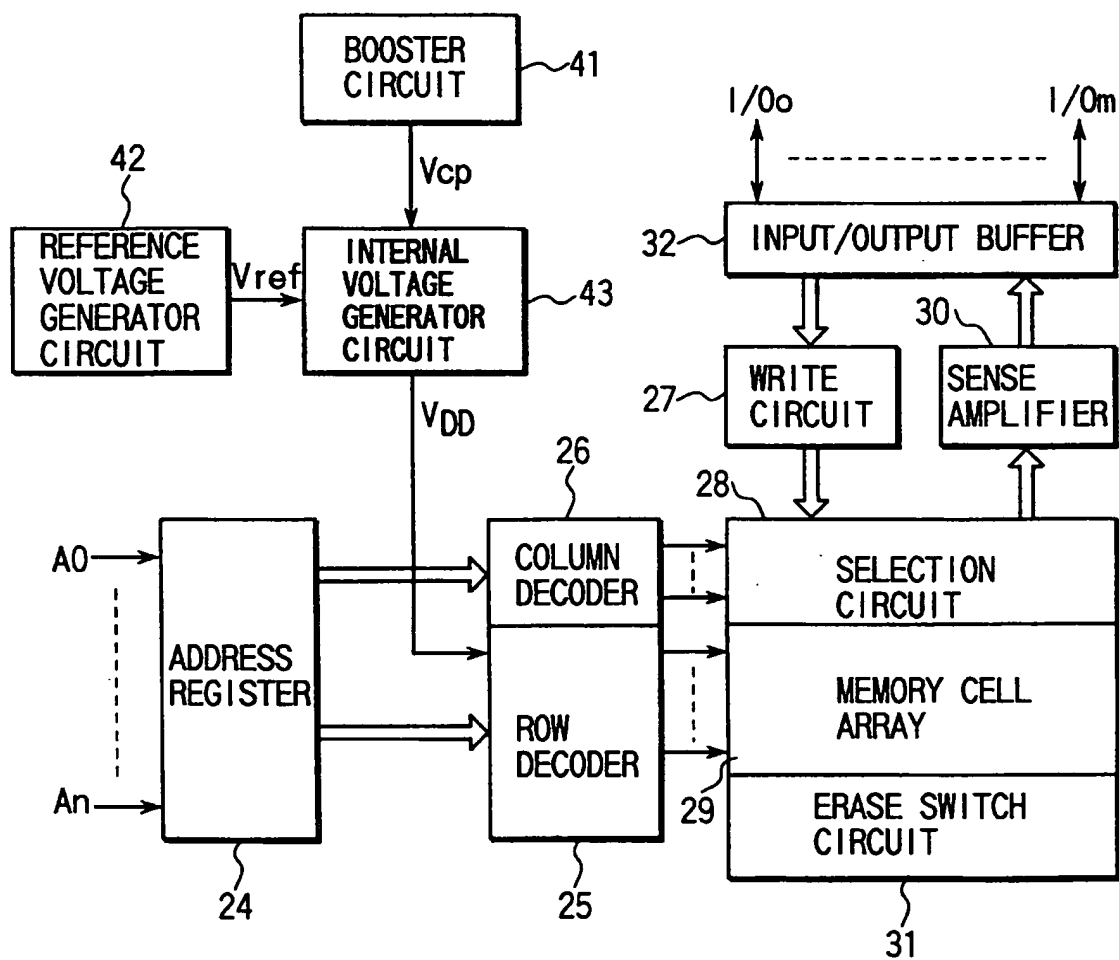


FIG. 17

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# BOOSTER CIRCUIT AND SEMICONDUCTOR MEMORY DEVICE HAVING THE SAME

This application is a Divisional of U.S. application Ser. No. 09/028,221 filed on Feb. 23, 1998 now U.S. Pat. No. 6,041,011.

## BACKGROUND OF THE INVENTION

The present invention relates to a booster circuit and a semiconductor memory device having the same, and more particularly to a booster circuit used in a non-volatile semiconductor memory device such as an EEPROM.

FIG. 1 shows an example of a conventional booster circuit. FIG. 2 shows waveforms of clock pulse signals  $\phi$  and  $\bar{\phi}$  (the mark of "—" means that the signal is inverted).

The booster circuit shown in FIG. 1 includes, for example, four n-channel MOS transistors 1 to 4 and three capacitors 5 to 7. An end of a current path of the transistor 1 and a gate thereof are supplied with a power supply voltage  $V_{cc}$ . The other end of the current path of the transistor 1 is connected to an end of a current path of the transistor 2 and a gate thereof, as well as an end of a capacitor 5. The other end of the capacitor 5 is supplied with a signal  $\phi$ . The other end of the current path of the transistor 2 is connected with an end of a current path of the transistor 3 and a gate thereof, as well as an end of the capacitor 6. The other end of the capacitor 6 is supplied with a signal  $\bar{\phi}$ . The other end of the current path of the transistor 3 is connected with an end of a current path of the transistor 4 and a gate thereof, as well as an end of the capacitor 7. The other end of the capacitor 7 is supplied with a signal  $\phi$ . The other end of the current path of the transistor 4 outputs a boosted voltage  $V_{out}$ .

The clock pulse signal  $\phi$  and the inverted signal  $\bar{\phi}$  thereof oscillate, for example, between the power supply voltage  $V_{cc}$  and 0V as a ground potential as shown in FIG. 2. The clock signals  $\phi$  and  $\bar{\phi}$  have a frequency expressed as  $f$ .

Each of the n-channel MOS transistors 1 to 4 has a threshold value expressed as  $V_t$ . The capacitors 5, 6, and 7 have an equal capacity  $C$ . Further, the number of stages of the booster circuit is expressed as  $N$  and indicates the number of the capacitors of the booster circuit. In the booster circuit shown in FIG. 1,  $N$  is 3.

FIG. 3 shows a circuit equivalent to the booster circuit shown in FIG. 1. The negative electrode of the voltage source 8 is grounded, and the positive electrode of the voltage source 8 is connected to an end of a resistor 9. The other end of the resistor 9 outputs a voltage  $V_{out}$ . The current flowing through the resistor 9 is expressed as  $I_{out}$ . An output voltage  $E$  of the voltage source 8 is obtained by  $(N+1) \times (V_{cc} - V_t)$ . A resistance value  $R$  of the resistor 9 is obtained by  $1/(C \times f)$ .

FIG. 4 shows a relationship between the output voltage  $V_{out}$  and the output current  $I_{out}$ .

In order to increase the output current  $I_{out}$  without changing the frequency  $f$  and the capacity  $C$  of each capacitor, the pentode threshold value  $V_t$  of the MOS transistors 1 to 4 needs to be 0. For example, the threshold value  $V_t$  can be substantially set to 0 by using an intrinsic n-channel MOS transistor, such as an n-channel MOS transistor which is formed on a p-type substrate and has a channel region not implanted with channel ions.

FIG. 5 shows a circuit in which a conventional booster circuit is added with a circuit for detecting an output voltage of the booster circuit to control the booster circuit.

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In FIG. 5, the booster circuit 11 is the same as that shown in FIG. 1, and also, a power supply voltage  $V_{cc}$  and clock pulse signals  $\phi$  and  $\bar{\phi}$  are supplied while a boosted voltage  $V_{cp}$  is outputted. The output voltage  $V_{cp}$  is used, for example, as an internal power supply voltage of a semiconductor integrated circuit.

The boosted voltage  $V_{cp}$  is supplied to an end of a resistor 12, and the other end of the resistor 12 is connected to an end of a resistor 13. The other end of the resistor 13 is grounded. The resistance values of the resistors 12 and 13 are respectively expressed as  $R_1$  and  $R_2$ .

An inverted input terminal of an operational amplifier 14 is connected to a connection point between the resistors 12 and 13. The voltage at the connection point is expressed as  $V_g$ . The inverted input terminal of the operational amplifier 14 is supplied with a reference voltage  $V_{ref}$ . The operational amplifier 14 outputs an oscillator enable signal  $OSCE$ .

A ring oscillator 15 generates and outputs clock pulse signals  $\phi$  and  $\bar{\phi}$  in response to a signal  $OSCE$ .

In the circuit shown in FIG. 1, for example, the gate of the n-channel MOS transistor 1 and a first terminal of the current path is applied with a power supply voltage  $V_{cc}$ . The voltage at a second terminal of the current path of the transistor 1 is boosted to be higher than the power supply voltage  $V_{cc}$ . In this case, since the transistor 1 is turned off, no current must flow back to the first terminal from the second terminal of the current path.

However, if the MOS transistor 1 is of an intrinsic type, the threshold value  $V_t$ , for example, about  $-0.1V$  which is lower than that obtained in case of using an ordinary n-channel MOS transistor. Therefore, while a voltage  $V_{cc}$  is applied to the gate of the transistor 1, a slight current flows through the transistor 1, thus causing a back flow of a current in a direction from a boosted voltage to a power supply voltage. Further, if the back gate voltage of the transistor 1 is small or the power supply voltage  $V_{cc}$  is low, the back flow is more apparent.

Also, if the transistor operates in an environment of a high temperature, the threshold voltage  $V_t$  decreases to satisfy a relation of  $V_t < 0$ . Therefore, a back flow as described above is caused too.

Also, if the transistor is of an enhancement type, the threshold value decreases due to downsizing of the transistor if the transistor, and a back flow is caused too.

Thus, if a transistor having a low threshold value  $V_t$  is used, a leakage current from the output side to the input power voltage  $V_{cc}$  side is always caused due to its back gate effect or a temperature influence, so that the operating current is increased.

Consideration is then taken into a case in which the power supply voltage  $V_{cc}$  is higher than the output voltage  $V_{cp}$  of the booster circuit in the circuit shown in FIG. 5. In FIG. 6, a line 16 represents a load characteristic of the booster circuit in the case, i.e., a relationship between the output voltage and the output current of the booster circuit 11. Another line 17 represents a relationship between a voltage applied between both ends of the resistors 12 and 13 connected in series, and a current flowing through the resistors 12 and 13. The voltage at the cross point of the lines 16 and 17 is the output voltage  $V_{cp}$  of the booster circuit 11. The number of capacitors in the booster circuit 11 is expressed as  $N$ , and the threshold value of the MOS transistors constituting the booster circuit 11 is expressed as  $V_t$ . A desired power supply voltage is  $[(R_1 + R_2)/R_2] \times V_{ref}$ .

Where a relation of  $V_{cc} - (N+1) \times V_t > [(R_1 + R_2)/R_2] \times V_{ref}$  is satisfied, the booster circuit 11 does not perform boosting

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but outputs a voltage obtained by reducing the power supply voltage  $V_{cc}$ , as an internal power supply voltage.

From a relation of  $[R2/(R1+R2)] \times [V_{cc} - (N+1) \times V_1] (= V_g) > V_{ref}$ , the output signal OSCE of the operational amplifier 14 is of a low level. Therefore, the ring oscillator 15 does not operate, and each of the signals  $\phi$  and  $\phi$  is kept at a low or high level.

Consequently, the output voltage  $V_{cp}$  is higher than the desired level  $[(R1+R2)/R2] \times V_{ref}$ . The difference between the output voltage and the desired voltage level increases as an external power supply voltage  $V_{cc}$  increases, as can be seen from FIG. 6.

If the external power supply voltage  $V_{cc}$  is allowed to exceed a standard voltage of 3V and increase to, for example, 5V, the internal power supply voltage increases in accordance with the external power supply voltage  $V_{cc}$ . Then, a problem occurs in the reliability of peripheral elements and memory cells. Like in the booster circuit shown in FIG. 1, a problem occurs in that a current flows back to the power supply voltage in the booster circuit in an operation environment of a high temperature. Further, if the threshold voltage decreases due to the same factors as those in the case of the booster circuit shown in FIG. 1, the internal power supply voltage  $V_{cp}$  increases, thereby affecting the reliability of peripheral elements and memory cells.

#### BRIEF SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a booster circuit in which a current does not flow back to an external power supply voltage and a constant voltage is outputted with a wide margin for an external power supply voltage, and a semiconductor memory device having the booster circuit.

According to an aspect of the present invention, there is provided a booster circuit comprising: a booster unit having a voltage input terminal, a voltage output terminal, and a signal input terminal; and an n-type MOS transistor having a current path having an end supplied with a power supply voltage and another end connected to the voltage input terminal of the booster unit, and having a gate supplied with an inverted signal of a signal supplied to the signal input terminal of the booster unit.

According to another aspect of the present invention, there is provided a booster circuit comprising: a plurality of booster units, each having a voltage input terminal, a voltage output terminal, and a signal input terminal, and connected in series to form a plurality of stages, respectively, such that the voltage input terminal of the booster unit at a present stage is connected to the voltage output terminal of the booster unit at a preceding stage and such that the signal input terminal of the booster unit at the present stage is connected to the signal input terminal of the preceding stage; and an n-type MOS transistor having a current path having an end supplied with a power supply voltage and another end connected to the voltage input terminal of the booster unit at a first stage, and having a gate supplied with an inverted signal of a signal supplied to the signal input terminal of the booster unit at the first stage.

In the booster circuit described above, the n-type MOS transistor is turned off when the booster unit at the first stage operates. Also, the booster circuit may comprise: a detector circuit for comparing a voltage value of the voltage output terminal of the booster unit at a last stage with a preset value, and for outputting an oscillator circuit activation signal in accordance with a comparison result; and an oscillator circuit for generating the signal to be supplied to each of the

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signal input terminals of the plurality of booster units, in accordance with the oscillator circuit activation signal. The n-type MOS transistor may be of an intrinsic type. Each of the booster units may include: an n-type MOS transistor having a current path and a gate, connected such that an end of the current path and the gate are connected to the voltage input terminal and such that another end of the current path is connected to the voltage output terminal; and a capacitor having an end connected to the voltage input terminal and another end connected to the signal input terminal. In this case, the n-type MOS transistors included in the booster units may be of an intrinsic type.

According to further another aspect of the present invention, there is provided booster circuit comprising: a booster unit having a voltage input terminal, a voltage output terminal, and a signal input terminal; and an n-type MOS transistor having a current path having an end supplied with a power supply voltage and another end connected to the voltage input terminal of the booster unit, and having a gate supplied with an AND signal of a booster circuit activation signal and an inverted signal of a signal supplied to the signal input terminal of the booster unit.

According to further another aspect of the present invention, there is provided a booster circuit comprising: a plurality of booster units each having a voltage input terminal, a voltage output terminal, and a signal input terminal, and connected in series to form a plurality of stages, respectively, such that the voltage input terminal of the booster unit at a present stage is connected to the voltage output terminal of the booster unit at a preceding stage and such that the signal input terminal of the booster unit at the present stage is connected to the signal input terminal of the preceding stage; and an n-type MOS transistor having a current path having an end supplied with a power supply voltage and another end connected to the voltage input terminal of the booster unit at a first stage, and having a gate supplied with an AND signal of a booster circuit activation signal and an inverted signal of a signal supplied to the signal input terminal of the booster unit at the first stage.

In the booster circuit described above, the n-type MOS transistor is turned off when the booster unit at the first stage operates. Also, the booster circuit may further comprise: a detector circuit for comparing a voltage value of the voltage output terminal of the booster unit at a last stage with a preset value, and for outputting an oscillator circuit activation signal in accordance with a comparison result and the booster circuit activation signal; and an oscillator circuit for generating the signal to be supplied to each of the signal input terminals of the plurality of booster units, in accordance with the oscillator circuit activation signal and the booster circuit activation signal. The n-type MOS transistor may be of an intrinsic type. Each of the booster units includes: an n-type MOS transistor having a current path and a gate, connected such that an end of the current path and the gate are connected to the voltage input terminal and such that another end of the current path is connected to the voltage output terminal; and a capacitor having an end connected to the voltage input terminal and another end connected to the signal input terminal. In this case, the n-type MOS transistors included in the booster units may be of an intrinsic type.

Further, according to another aspect of the present invention, there is provided a semiconductor memory device comprising: a booster circuit including a plurality of booster units each having a voltage input terminal, a voltage output terminal, and a signal input terminal, and connected in series to form a plurality of stages, respectively, such that the

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voltage input terminal of the booster unit at a present stage is connected to the voltage output terminal of the booster unit at a preceding stage and such that the signal input terminal of the booster unit at the present stage is supplied with an inverted signal of a signal supplied with the signal input terminal of the booster unit at the preceding stage, and an n-type MOS transistor having a current path having an end supplied with a power supply voltage and another end connected to the voltage input terminal of the booster unit at a first stage, and having a gate supplied with an inverted signal of a signal supplied to the signal input terminal of the booster unit at the first stage or supplied with an AND signal of the inverted signal and a booster circuit activation signal; a reference voltage generator circuit for generating a reference voltage; and an internal voltage generator circuit for generating a voltage to be supplied to a memory cell from a boosted voltage obtained through the voltage output terminal of the booster unit at a last stage, with reference to the reference voltage.

In the semiconductor memory device described above, the booster circuit may further comprise: a detector circuit for comparing a voltage value of the voltage output terminal of the booster unit at the last stage with a preset value, and for outputting an oscillator activation signal in accordance with a comparison result; and an oscillator circuit for generating the signal to be supplied to each of the signal input terminals of the plurality of booster units, in accordance with the oscillator circuit activation signal.

In the semiconductor memory device described above, the detector circuit may compare the voltage value of the voltage output terminal of the booster unit at the last stage with the preset value, and may output the oscillator circuit activation signal in accordance with the comparison result and the booster circuit activation signal. Further, the oscillator circuit may generate the signal to be supplied to each of the signal input terminals of the plurality of booster units, in accordance with the oscillator circuit activation signal and the booster circuit activation signal. Also, each of the booster units may include: an n-type MOS transistor having a current path and a gate, connected such that an end of the current path and the gate are connected to the voltage input terminal and such that another end of the current path is connected to the voltage output terminal; and a capacitor having an end connected to the voltage input terminal and another end connected to the signal input terminal. In this case, the n-type MOS transistors included in the booster units may be of an intrinsic type.

Additional objects and advantages of the present invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the present invention. The objects and advantages of the present invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the present invention and, together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the present invention in which:

FIG. 1 is a diagram showing an example of a conventional booster circuit;

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FIG. 2 is a view showing waveforms of clock pulse signals;

FIG. 3 is a diagram showing an equivalent circuit of the circuit shown in FIG. 1;

FIG. 4 is a graph showing a load characteristic of the circuit shown in FIG. 1;

FIG. 5 is a diagram showing an example of a conventional circuit in which a booster circuit is added with a boost level detector circuit;

FIG. 6 is a graph showing load characteristics of the circuit shown in FIG. 5;

FIG. 7 is a diagram showing a structure of a booster circuit according to a first embodiment of the present invention;

FIG. 8 is a diagram showing a structure of a booster circuit according to a second embodiment of the present invention;

FIG. 9 is a diagram showing a structure of a booster circuit according to a third embodiment of the present invention;

FIG. 10 is a diagram showing a structure of a booster circuit according to a fourth embodiment of the present invention;

FIG. 11 is a diagram showing a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a fifth embodiment of the present invention;

FIG. 12 is a diagram showing a general example of a structure of the band gap reference circuit;

FIG. 13 is a diagram showing a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a sixth embodiment of the present invention;

FIG. 14 is a diagram showing a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a seventh embodiment of the present invention;

FIG. 15 is a table showing statuses of signals in the embodiment shown in FIG. 14;

FIG. 16 is a diagram showing a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to an eighth embodiment of the present invention; and

FIG. 17 is a block diagram showing the entire structure of a non-volatile semiconductor memory using a booster circuit according to the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings.

FIG. 7 shows a structure of a booster circuit according to a first embodiment of the present invention. In the following description, same components are referred to by same references, and detailed explanation will be omitted herefrom.

In the circuit shown in FIG. 7, a clock pulse signal  $\phi$  is supplied to an end of a capacitor C1 and an end of a capacitor C3, and an inverted signal  $\phi$  of the clock pulse signal  $\phi$  is supplied to a gate of a n-channel MOS transistor M1 and an end of a capacitor C2. An end of a current path of the n-channel MOS transistor M1 is supplied with a power supply voltage Vcc, and the other end of the current path of the MOS transistor M1 is connected to an end of a

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current path of an n-channel MOS transistor M2 and a gate thereof, as well as an end of the capacitor C1. This connection is obtained at a connection point called a junction point N1. The other end of the current path of the MOS transistor M2 is connected to an end of a current path of an n-channel MOS transistor M3 and a gate thereof, as well as an end of a capacitor C2. This connection is obtained at a connection point called a junction point N2. The other end of the MOS transistor M3 is connected to an end of a current path of an n-channel MOS transistor M4 and a gate thereof, as well as an end of a capacitor C3. This connection is obtained at a connection point called a junction point N3. The other end of the current path of the MOS transistor M4 outputs an output voltage  $V_{out}$ .

The threshold value of each of the n-channel MOS transistors M1 to M4 is expressed as  $V_t$ .

Although the present embodiment adopts MOS transistors M1 to M4 arranged to form a plurality of stages, the structure is not limited hitherto but MOS transistors M3 and M4 may be removed.

In the following, operation of the circuit shown in FIG. 7 will be explained.

In this circuit, the gate of the transistor M1 whose end is supplied with the power supply voltage is supplied with a signal  $\phi$  having a phase opposite to that of the pulse signal  $\phi$  supplied to the signal input terminal of the capacitor C1 for the boosting at the first stage. When the signal  $\phi$  is at a high level, the transistor M1 is conductive. In this state, the signal  $\phi$  is at a low level, so that the transistor M2 is turned off. Therefore, the junction point N1 is charged to a voltage defined by  $V_{cc}-V_t$ .

Next, when the signal  $\phi$  goes to a low level and the signal  $\phi$  goes to a high level, the transistor M1 is turned off and the transistor M2 is turned on. In this state, the voltage at the junction point N1 is  $V_{cc}-V_t+V_{cc}$ . The electric charges charged at the junction point N2 are not discharged since the transistor M1 is turned off and no discharge path to the power supply voltage  $V_{cc}$  exists. As a result, wasteful discharging to the external power supply voltage  $V_{cc}$  can be avoided.

Thus, according to the present embodiment, wasteful discharging from inside of the booster circuit to an external power supply voltage  $V_{cc}$  can be avoided, so that the operation efficiency as a charge pump can be improved.

In addition, in comparison with a conventional apparatus in which a power supply voltage is supplied to the gate of the transistor M1, a ground potential is supplied thereto according to the present embodiment, so that the cut-off current of the transistor M1 is greatly reduced. Therefore, it is not necessary to consider the cut-off characteristic of each transistor, and n-channel MOS transistors each having a short channel length can be used for the booster circuit. As a result of this, it is possible to reduce the parasitic resistance of transfer gates, to decrease the threshold value of each transistor, and to reduce the layout area of the circuit.

FIG. 8 shows a structure of a booster circuit according to a second embodiment of the present invention.

In the circuit shown in FIG. 8, the transistors M1 to M4 in the circuit shown in FIG. 7 are replaced with intrinsic n-channel MOS transistors M5 to M8 each formed on a p-type substrate. The other components are the same as those of the circuit shown in FIG. 7.

Although the present embodiment uses MOS transistors M5 to M8 respectively arranged to form a plurality of stages, the structure is not limited hitherto but may be arranged such that MOS transistors M7 and M8 are removed.

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Operation of the circuit shown in FIG. 8 is the same as that of the circuit shown in FIG. 7.

According to the present embodiment, the same advantages are obtained as those in the first embodiment. Further, an intrinsic n-channel MOS transistor has a threshold value of an enhancement type MOS transistor used in the first embodiment. Therefore, a voltage drop caused at each stage of the transfer gates is reduced, so that a high boosted voltage can be generated with less stages than in the first embodiment, resulting in an improvement of the efficiency of the booster circuit.

FIG. 9 shows a structure of a booster circuit according to a third embodiment of the present invention.

The circuit shown in FIG. 9 is arranged such that the gate of the n-channel MOS transistor M1 shown in FIG. 7 is not supplied with a signal  $\phi$ , but is supplied with a logic product signal which is a logical product of the signal  $\phi$  and an inverted signal  $\phi$  of a charge pump disable signal. Specifically, a first input terminal of an AND gate G1 is supplied with a signal  $\phi$ , and a second input terminal of the AND gate G1 is supplied with an inverted signal  $\phi$  of a charge pump disable signal. The output terminal of the AND gate G1 is connected to the gate of the transistor M1. The other components are the same as those shown in FIG. 7.

In the present embodiment, the signal  $\phi$  is at a low level in a state in which the booster circuit is not operated, for example, in a stand-by state. Therefore, also in this state, the transistor M1 is turned off, so that a back flow to the power supply voltage  $V_{cc}$  can be prevented.

FIG. 10 shows a structure of a booster circuit according to a fourth embodiment.

The circuit shown in FIG. 10 is arranged such that the gate of the n-channel MOS transistor M5 shown in FIG. 8 is not supplied with a signal  $\phi$ , but is supplied with a logic product signal which is a logical product of the signal  $\phi$  and an inverted signal  $\phi$  of a charge pump disable signal. Specifically, a first input terminal of an AND gate G1 is supplied with a signal  $\phi$ , and a second input terminal of the AND gate G1 is supplied with an inverted signal  $\phi$  of a charge pump disable signal. The output voltage of the AND gate G1 is expressed as  $V_{g1}$ . The other components are the same as those shown in FIG. 8.

In the present embodiment, the signal  $\phi$  is at a low level in a state in which the booster circuit is not operated, for example, in a stand-by state. Therefore, also in this state, the transistor M1 is turned off, so that a back flow to the power supply voltage  $V_{cc}$  can be prevented.

FIG. 11 shows a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a fifth embodiment of the present invention.

In the circuit shown in FIG. 11, a booster circuit 51 is the same as the circuit shown in FIG. 7, for example. The output voltage  $V_{cp}$  of the booster circuit 51 is supplied to an input terminal of a boost level detector circuit 52.

In the boost level detector circuit 52, the output voltage  $V_{cp}$  of the booster circuit is supplied to an end of a resistor R1. The other end of the resistor R1 is connected to an end of a resistor R2 and an inverted input terminal of an operational amplifier 54. The voltage at the connection point therebetween is expressed as  $V_g$ . The other end of the resistor R2 is grounded. A non-inverted input terminal of the operational amplifier is supplied with a reference voltage  $V_{ref}$ . The reference voltage  $V_{ref}$  is supplied from a band gap reference circuit, for example. For references, a general example of a structure of the band gap reference circuit is



shown in FIG. 12. The band gap reference circuit is constructed so as to generate a reference voltage  $V_{ref}$  which has a low temperature dependency and a less power supply voltage dependency. The operational amplifier 54 outputs an oscillator enable signal OSCE.

The oscillator enable signal OSCE is supplied to an input terminal of the ring oscillator 53. The ring oscillator 53 generates clock pulse signals  $\phi$  and  $\phi$  to be supplied to the booster circuit 51, in response to the signal OSCE. The clock pulse signals  $\phi$  and  $\phi$  have the same waveforms as shown in FIG. 2.

In the following, operation of the present embodiment will be explained.

A voltage  $v_g$  of the inverted input terminal of the operational amplifier 54 is obtained by  $[R_2/(R_1+R_2)] \cdot V_{cp}$ . The boost level detector circuit 52 monitors the output voltage  $V_{cp}$  of the booster circuit 51. When the output voltage  $V_{cp}$  is lower than a predetermined level, i.e., when  $V_g < V_{ref}$  is satisfied, the output signal OSCE of the boost level detector circuit 52 goes to a high level. The ring oscillator 53 is activated and generates pulse signals  $\phi$  and  $\phi$ . Therefore, the booster circuit 51 performs boosting operation.

When the output voltage  $V_{cp}$  goes to a level higher than a predetermined level, i.e., when  $V_g > V_{ref}$  is satisfied, the output signal OSCE of the boost level detector circuit 52 goes to a low level. Therefore, the ring oscillator 53 is deactivated and does not generate pulse signals  $\phi$  and  $\phi$ . Accordingly, the booster circuit is deactivated and the transistor M1 in the booster circuit 51 is turned off.

Therefore, according to the present embodiment, a back flow of a current to the power supply voltage  $V_{cc}$  can be prevented.

FIG. 13 shows a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a sixth embodiment of the present invention.

The circuit shown in FIG. 13 is arranged such that the booster circuit 51 shown in FIG. 11 is replaced with a booster circuit 55 shown in FIG. 8. The other components are the same as those of the circuit shown in FIG. 11.

Operation of the circuit shown in FIG. 13 is the same as that of the circuit shown in FIG. 11.

The present embodiment achieves the same advantages as those of the second and fifth embodiments. Specifically, a back flow of a current from inside the booster circuit to the power supply voltage  $V_{cc}$  can be prevented. Further, since transistors of the booster circuit 55 are constituted by intrinsic n-channel MOS transistors, it is possible to improve the efficiency of the booster circuit.

FIG. 14 shows a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to a seventh embodiment of the present invention.

In the circuit shown in FIG. 14, a booster circuit 61 is the same as the circuit shown in FIG. 9. The output voltage  $V_{cp}$  of the booster circuit 61 is supplied to an input terminal of a boost level detector circuit 62.

In the boost level detector circuit 62, the output voltage  $V_{cp}$  of the booster circuit is supplied to an end of a resistor R1. The other end of the resistor R1 is connected to an end of a resistor R2 and an inverted input terminal of an operational amplifier 64. The voltage at the connection point therebetween is expressed as  $V_g$ . The other end of the resistor R2 is grounded. A non-inverted input terminal of the operational amplifier 64 is supplied with a reference voltage  $V_{ref}$ . The reference voltage  $V_{ref}$  is supplied from a band gap reference circuit, for example. The operational amplifier 64

is supplied with a charge pump disable signal CPD. The operational amplifier 64 outputs an oscillator enable signal OSCE.

The oscillator enable signal OSCE is supplied to an input terminal of a ring oscillator 63. The ring oscillator 63 is supplied with the charge pump disable signal CPD. The ring oscillator 63 generates clock pulse signals  $\phi$  and  $\phi$ .

FIG. 15 shows statuses of signals CPD,  $\phi$ ,  $\phi$ ,  $V_{g1}$ , and OSCE.

When the signal CPD is at a high level, the operational amplifier 64 stops operating and the signal OSCE goes to a low level. Further, the ring oscillator 62 stops operating since the signal CPD and the signal OSCE are at a low level, so that each of the signals  $\phi$  and  $\phi$  is kept at a low or high level. In addition, since the signal CPD is at a low level, the output signal  $v_{g1}$  of an AND gate G1 goes to a low level. Accordingly, the transistor M1 in the booster circuit 61 is turned off, and therefore, it is possible to prevent a back flow of a current to the power supply voltage  $V_{cc}$ .

When the signal CPD is at a low level, the circuit shown in FIG. 14 operates in the same manner as in the fifth embodiment (in FIG. 11) described above.

The present embodiment achieves the same advantages as those of the third and fifth embodiments described above. Specifically, a back flow of a current from inside the booster circuit to the power supply voltage  $V_{cc}$  can be prevented. Further, in the present embodiment, when the external power supply voltage  $V_{cc}$  goes to a level higher than a boost level, i.e., when  $V_{cc} - (N+1)V_t > [(R_1+R_2)/R_2] \times V_{ref}$  is satisfied,  $V_g > V_{ref}$  is satisfied, so that the signal CPE goes to a high level. In this case, the transistor M1 in the booster circuit is turned off, with the result that the booster circuit is deactivated. Therefore, the output voltage  $V_{cp}$  is not excessively charged to  $V_{cc} - (N+1)V_t$ , unlike in a conventional apparatus. Thus, even when the external power supply voltage  $V_{cc}$  fluctuates, the internal power supply voltage does not fluctuate, so that the booster circuit can be operated stably with respect to an external power supply voltage  $V_{cc}$  which is as high as  $[(R_1+R_2)/R_2] \times V_{ref} + (N+1)V_t$  or more higher.

Thus, according to the present embodiment, even when the power supply voltage  $V_{cc}$  becomes high, the internal elements are supplied with a constant voltage, so that the reliability of the elements is improved.

FIG. 16 shows a structure of a booster circuit added with a boost level detector circuit and an oscillator circuit, according to an eighth embodiment of the present invention.

The circuit shown in FIG. 16 is arranged such that the booster circuit 61 shown in FIG. 14 is replaced with the booster circuit 65 shown in FIG. 10. The other components are the same as those shown in FIG. 14.

Also, the circuit shown in FIG. 16 operates in the same manner as in the seventh embodiment (in FIG. 14) described above.

The present embodiment achieves the same advantages as those of the fourth and fifth embodiments described above. Specifically, in a state in which the booster circuit is not operated, the transistor M1 in the booster circuit is turned off, so that a back flow to the power supply voltage  $V_{cc}$  can be prevented, and fluctuations of the internal power supply voltage can be prevented against fluctuations of the external power supply voltage, with the result that the reliability of the elements can be improved. Further, in a state in which the booster circuit is operated, a back flow of a current from inside the booster circuit to the power supply voltage  $V_{cc}$  can be prevented. In addition, since the transistors in the

booster circuit are of intrinsic n-channel MOS transistors, the boost efficiency can be improved.

FIG. 17 shows the entire structure of a non-volatile semiconductor memory using a booster circuit according to the present invention.

The booster circuit 41 generates a boosted voltage  $V_{cp}$ .

A reference voltage generator circuit 42 generates a reference voltage  $V_{ref}$ . An internal voltage generator circuit 43 generates an internal voltage  $V_{DD}$  so as to correspond to a program mode, a verify mode, or the like, from the boosted voltage  $V_{cp}$ , with reference to the reference voltage  $V_{ref}$ .

Internal address signals (or external address signals)  $A_0$  to  $A_n$  are supplied to a row decoder 25 and a column decoder 26 through an address register 24. In addition, an output voltage  $V_{DD}$  of the internal voltage generator circuit 43 is applied through the row decoder 25 to a specified word line selected by the address signals  $A_0$  to  $A_n$ .

In a program mode, data is supplied to a specified memory cell in the memory cell array 29, through an input/output buffer 32, a write circuit 27, and a selection circuit 28.

In a read mode, data is used for verification, through the selection circuit 28 and a sense amplifier 30, or is outputted to outside the chip, further through the input/output buffer 32.

In an erase mode, the voltage to be applied to a source of a memory cell is switched by an erase switch circuit 31.

In the present embodiment, advantages equivalent to those of the embodiments described above can be obtained by using a booster circuit 41 according to the present invention. Specifically, a current is prevented from flowing back to the power supply voltage  $V_{cc}$ , in the booster circuit 41. Also, fluctuations of the internal power supply voltage are restricted against fluctuations of the external power supply voltage  $V_{cc}$ , so that the reliability of elements can be improved.

The booster circuit is naturally applicable not only to a non-volatile semiconductor memory device but also to other semiconductor memory devices.

As has been described above, according to the present invention, in the booster circuit, the transistor whose end is supplied with a power supply voltage is turned on/off by an inverted signal of a signal for booting a booster unit at a first stage or by an AND signal of the inverted signal and a booster circuit activation signal. Therefore, a back flow of a current from inside the booster circuit to the power supply can be prevented, thereby improving the efficiency of the booster circuit. Further, the fluctuations of the output voltage are not brought about even when the power supply voltage greatly fluctuates, so that the reliability of peripheral elements and memory cells can be improved and the allowable range of an external power supply voltage can be enhanced.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the present invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A semiconductor device comprising:

a booster circuit having an input terminal, an output terminal, an n-number of transistors composed of a first, a second, . . . , an n-th (where n is a positive integer) transistors diode-connected, and an n-number

of capacitors composed of a first, a second, . . . , a n-th capacitors, said n-number of transistors being serially connected between said input terminal and said output terminal, said first transistor being connected to said input terminal and said n-th transistor being connected to said output terminal, each of said n-number of capacitors having a first and a second electrodes, said first electrodes of said n-number of capacitors being respectively connected to gate electrodes of said n-number of transistors, the second electrodes of odd-numbered capacitors among said n-number of capacitors being supplied with a control signal, the second electrodes of even-numbered capacitors among said n-number of capacitors being supplied with a complementary signal of said control signal;

a terminal to which a power supply voltage is supplied;

a charge transfer transistor having a current path and a gate terminal, an end of said current path being connected to said input terminal of said booster circuit, another end of said current path being connected to said terminal, said gate terminal being supplied with said complementary signal of said control signal;

a differential amplifier circuit having a first and a second input terminals and an output terminal, said first input terminal being supplied with a voltage according to a potential of said output terminal of said booster circuit, said second input terminal being supplied with a reference voltage, said output terminal of said differential amplifier circuit outputting an output signal; and

a circuit which is connected to said output terminal of said differential amplifier circuit and produces the control signal and the complimentary signal thereof to be supplied to said booster circuit and said charge transfer transistor.

2. The semiconductor device according to claim 1, wherein said charge transfer transistor is turned off when said first transistor of said first booster circuit operates.

3. The semiconductor device according to claim 1, wherein each of said n-number of transistors is a MOS transistor.

4. The semiconductor device according to claim 1, wherein each of said n-number of transistors is an n-type MOS transistor.

5. The semiconductor device according to claim 1, wherein each of said n-number of transistors is an intrinsic type MOS transistor.

6. The semiconductor device according to claim 1, wherein said charge transfer transistor is a MOS transistor.

7. The semiconductor device according to claim 1, wherein said charge transfer transistor is an n-type MOS transistor.

8. The semiconductor device according to claim 1, wherein said charge transfer transistor is an intrinsic type MOS transistor.

9. A semiconductor device comprising:

a booster circuit having an input terminal, an output terminal, an n-number of transistors composed of a first, a second, . . . , a n-th (where n is a positive integer) transistors diode-connected, and an n-number of capacitors composed of a first, a second, . . . , an n-th capacitors, said n-number of transistors being serially connected between said input terminal and said output terminal, said first transistor being connected to said input terminal and said n-th transistor being connected to said output terminal, each of said n-number of capacitors having a first and a second electrodes, said

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first electrodes of said n-number of capacitors being respectively connected to gate electrodes of said n-number of transistors, the second electrodes of odd-numbered capacitors among said n-number of capacitors being supplied with a control signal, the second 5 electrodes of even-numbered capacitors among said n-number of capacitors being supplied with a complementary signal of said control signal;

- a terminal to which a power supply voltage is supplied;
- a charge transfer transistor having a current path and a gate terminal, an end of said current path being connected to said input terminal of said booster circuit, another end of said current path being connected to said terminal, said gate terminal being supplied with a signal based on said complementary signal of said control signal;
- a differential amplifier circuit having a first and a second input terminals and an output terminal, said first input terminal being supplied with a voltage according to a potential of said output terminal of said booster circuit, said second input terminal being supplied with a reference voltage, said output terminal of said differential amplifier circuit outputting an output signal; and
- a circuit which is connected to said output terminal of said differential amplifier circuit and produces the control signal and the complimentary signal thereof to be supplied to said booster circuit and said charge transfer transistor.

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10. The semiconductor device according to claim 9, wherein said signal based on said complementary signal of said control signal is an AND signal of a booster circuit activation signal and said complementary signal.

11. The semiconductor device according to claim 9, wherein said charge transfer transistor is turned off when said first transistor of said first booster circuit operates.

12. The semiconductor device according to claim 9, wherein each of said n-number of transistors is a MOS transistor.

13. The semiconductor device according to claim 9, wherein each of said n-number of transistors is an n-type MOS transistor.

14. The semiconductor device according to claim 9, wherein each of said n-number of transistors is an intrinsic type MOS transistor.

15. The semiconductor device according to claim 9, wherein said charge transfer transistor is a MOS transistor.

16. The semiconductor device according to claim 9, wherein said charge transfer transistor is an n-type MOS transistor.

17. The semiconductor device according to claim 9, wherein said charge transfer transistor is an intrinsic type MOS transistor.

\* \* \* \* \*



US006020781A

# United States Patent [19]

Fujioka

[11] Patent Number: 6,020,781  
[45] Date of Patent: \*Feb. 1, 2000

- [54] STEP-UP CIRCUIT USING TWO FREQUENCIES
- [75] Inventor: Shinya Fujioka, Kawasaki, Japan
- [73] Assignee: Fujitsu Limited, Kanagawa, Japan
- [\*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

5,159,543	10/1992	Yamawaki	363/60
5,208,557	5/1993	Kersh, III	331/57
5,416,446	5/1995	Holler, Jr. et al.	327/114
5,418,499	5/1995	Nakao	331/57
5,594,391	1/1997	Yoshizawa	327/264
5,633,825	5/1997	Sakuta et al.	365/189.09
5,694,308	12/1997	Cave	363/59
5,801,987	9/1998	Dinh	365/185.18

Primary Examiner—Timothy P. Callahan  
Assistant Examiner—Terry L. Englund  
Attorney, Agent, or Firm—Nikaido Marmelstein Murray & Oram, LLP

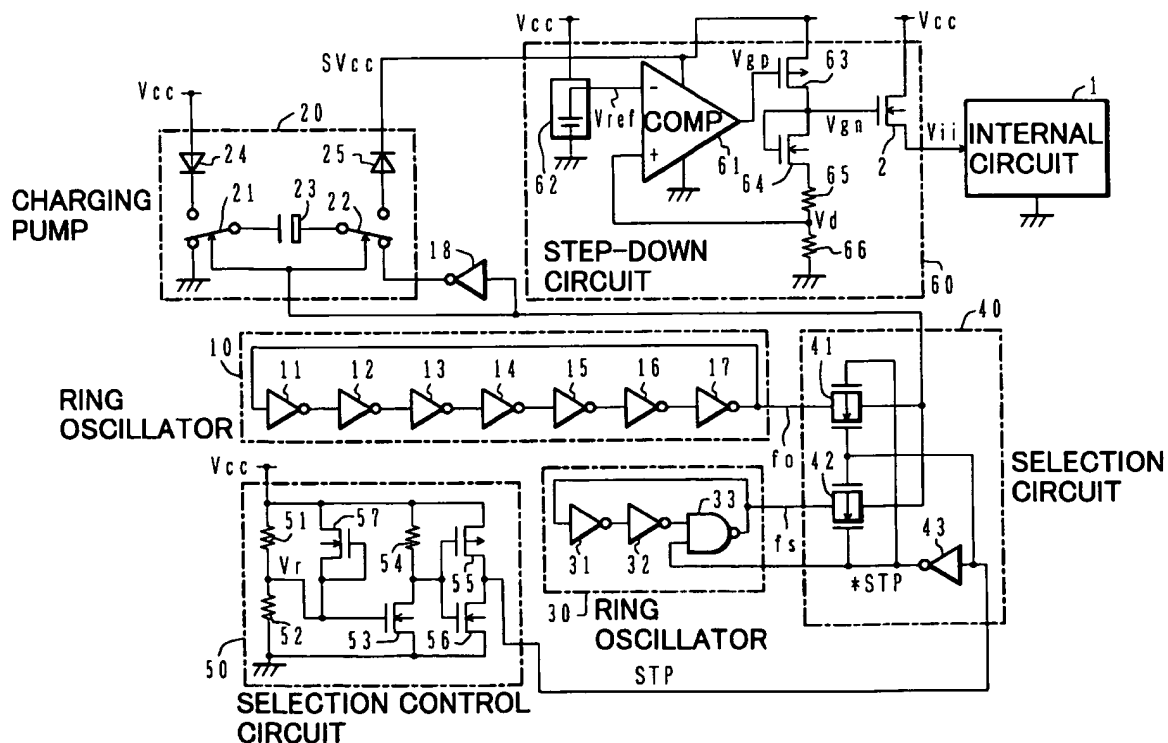
- [21] Appl. No.: 08/932,604
- [22] Filed: Sep. 17, 1997
- [30] Foreign Application Priority Data  
Dec. 27, 1996 [JP] Japan ..... 8-351275
- [51] Int. Cl.<sup>7</sup> ..... G05F 1/10; H03K 3/02
- [52] U.S. Cl. .... 327/541; 327/536; 327/142; 327/198; 365/189.11; 331/46; 331/48; 331/57; 363/60
- [58] Field of Search ..... 327/534, 535, 327/536, 537, 538, 540, 541, 143, 198, 291, 293, 294, 276, 589; 331/46, 48, 49, 50, 57, 177 R; 365/189.09, 189.11, 226; 363/59, 60

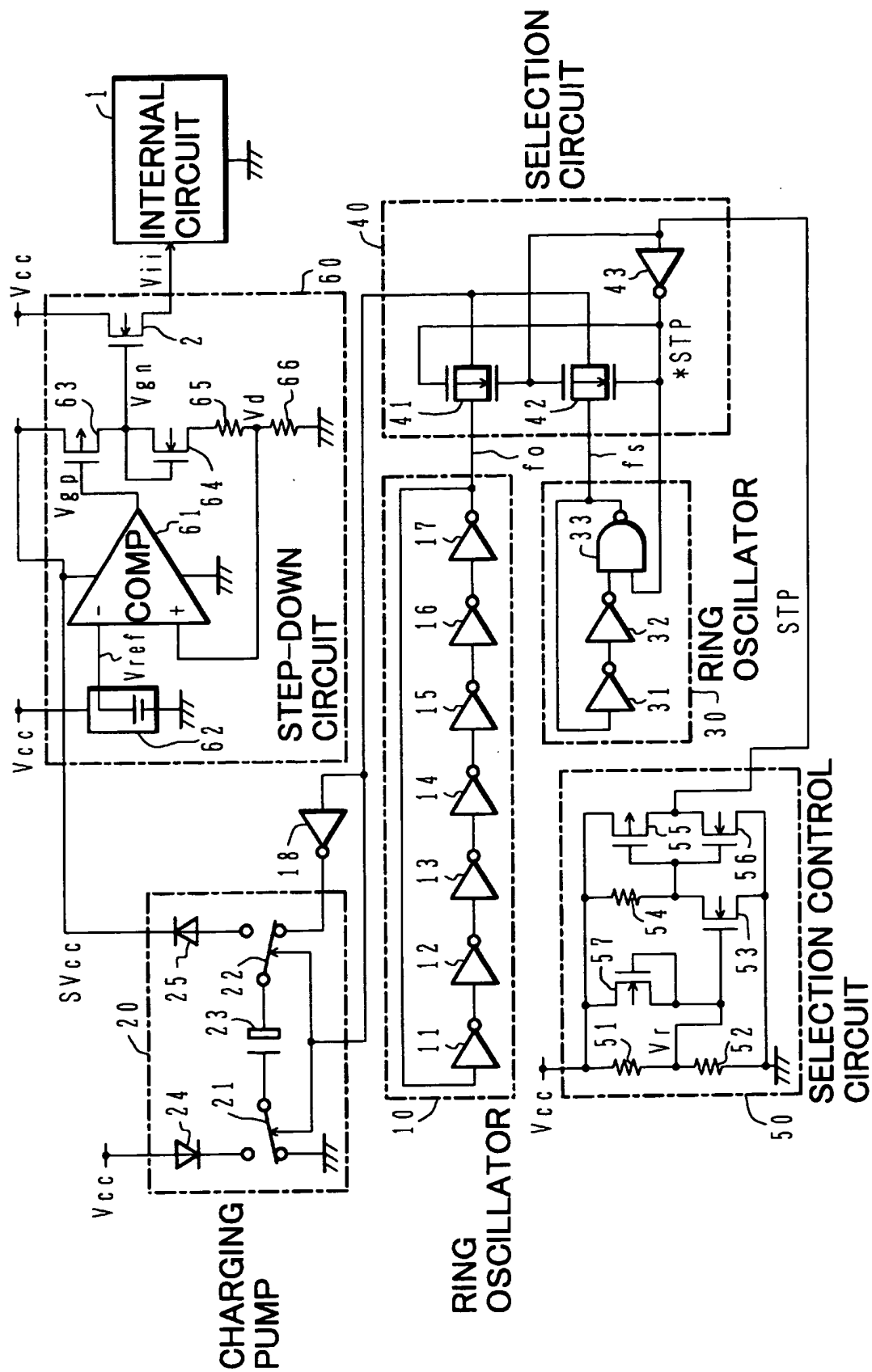
- [56] References Cited
- U.S. PATENT DOCUMENTS
- 5,075,572 12/1991 Poteet et al. .... 327/537

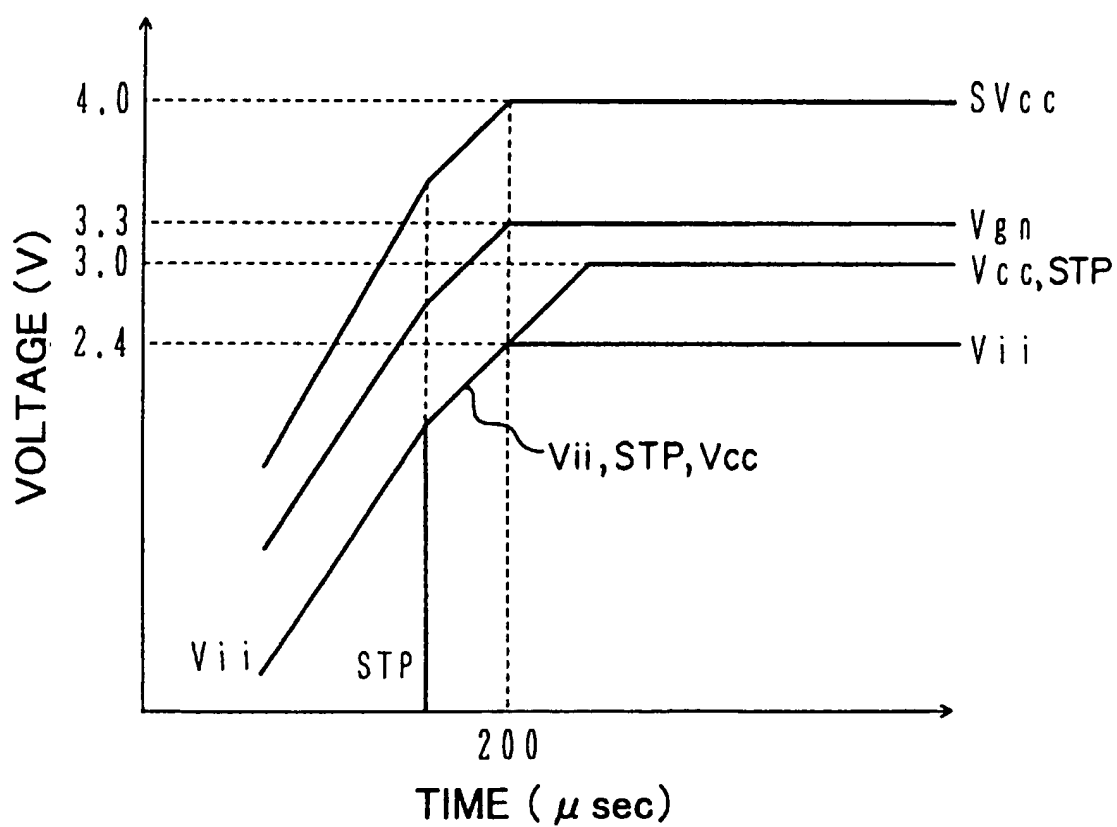
## [57] ABSTRACT

A step-up circuit includes a selection control circuit 50 for activating a start/stop signal STP by detecting an external power-supply voltage  $V_{cc}$ , which is stable at 3.3 V, to reach 2.0 V or more, a ring oscillator circuit 30 for generating and outputting a clock of a high frequency  $f_s$  when the start/stop signal STP is inactive, a ring oscillator circuit 10 for generating a clock of a low frequency  $f_o$ , a selection circuit 40 for selecting the output of the oscillator 30 when the start/stop signal STP is inactive and for selecting the output of the oscillator 10 when the start/stop signal is active, and a charging pump circuit 20 driven by the clocks. High frequency  $f_s$  is initially used to quickly bring an output voltage up to a desired operating level and low frequency  $f_o$  is used, in order to conserve power, to maintain the operating level once a predetermined level of the external power supply voltage  $V_{cc}$  has been reached in order to conserve power.

10 Claims, 7 Drawing Sheets



**FIG. 1**

**FIG. 2**

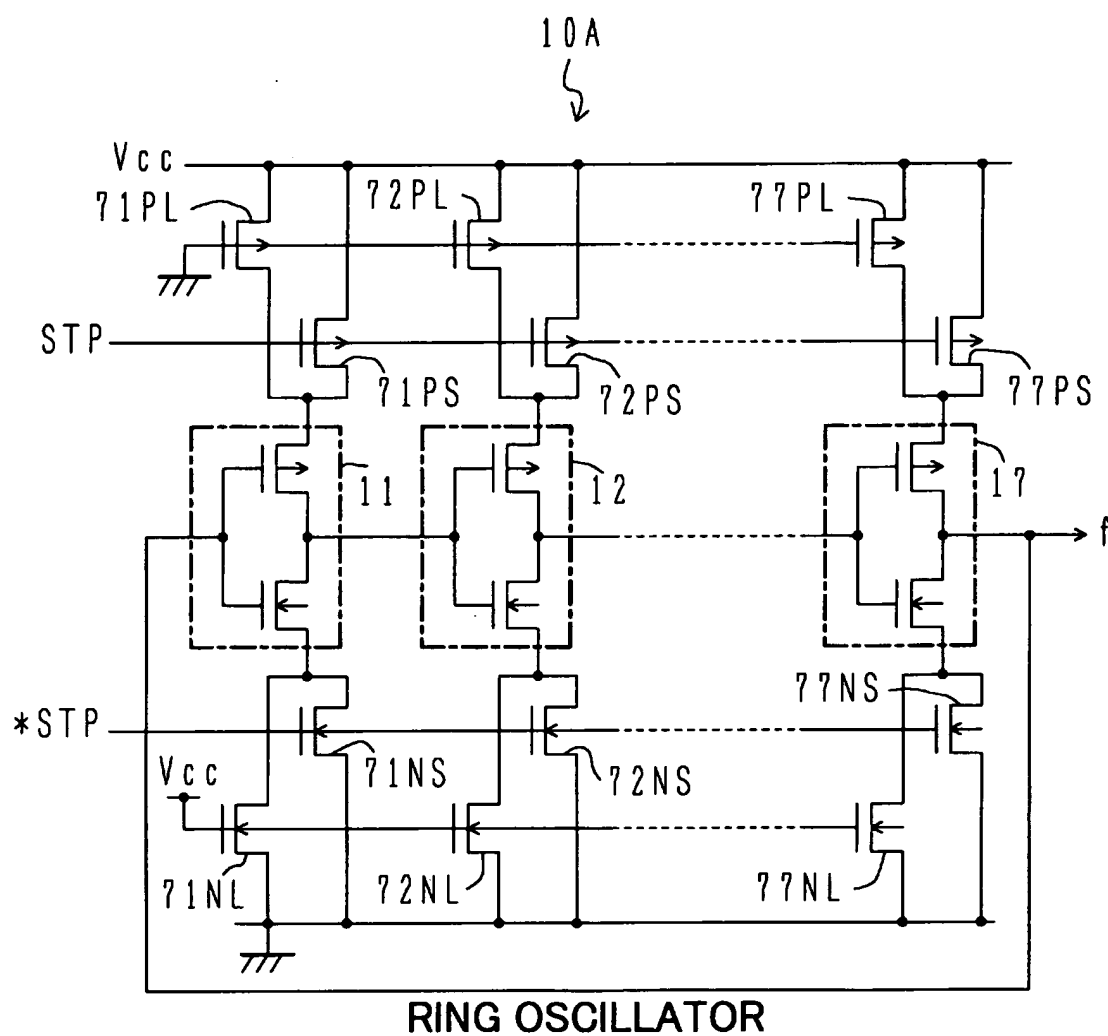
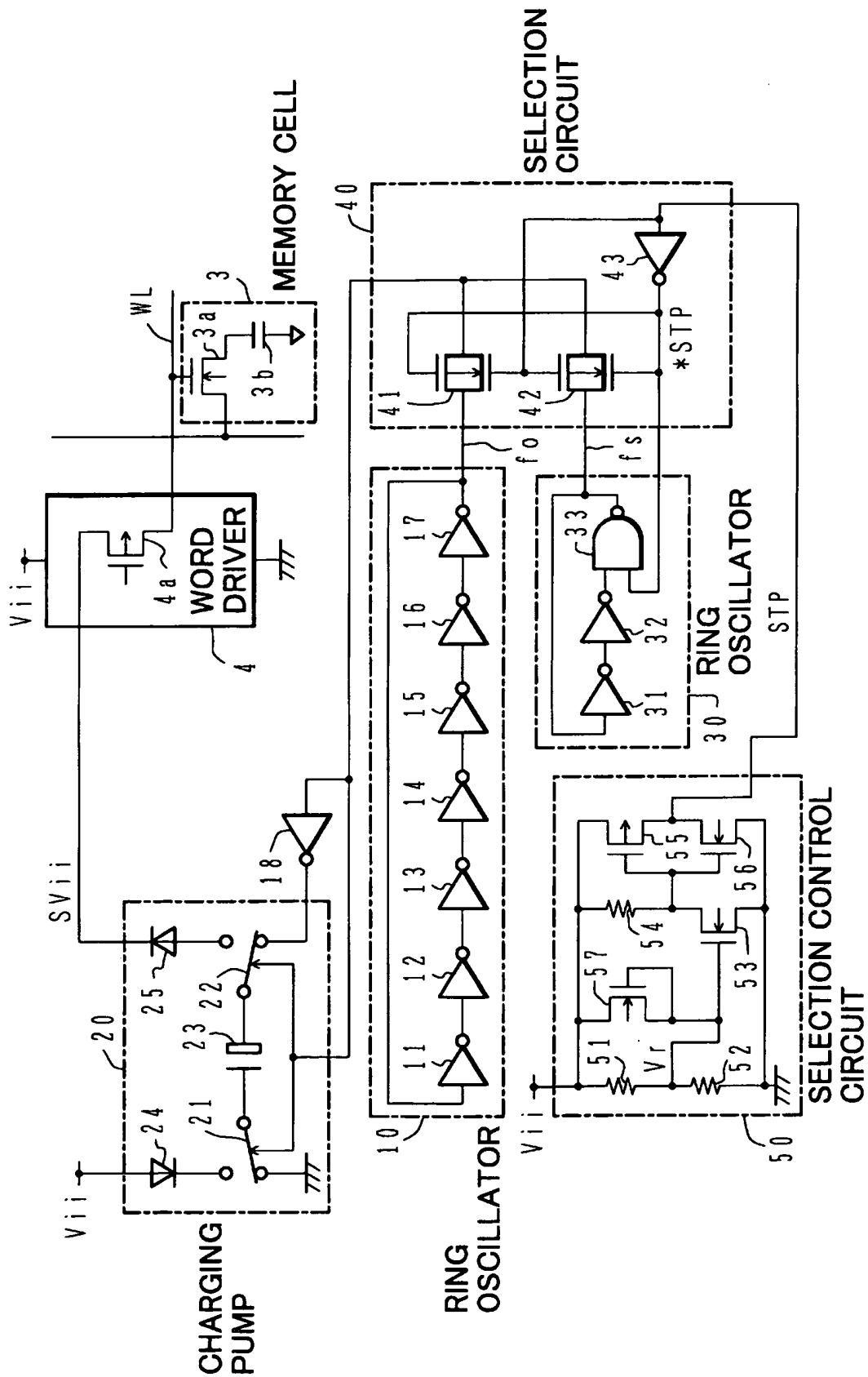
**FIG.3**

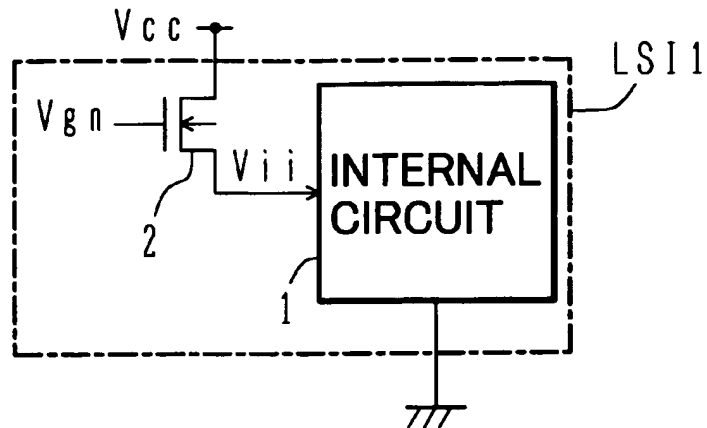




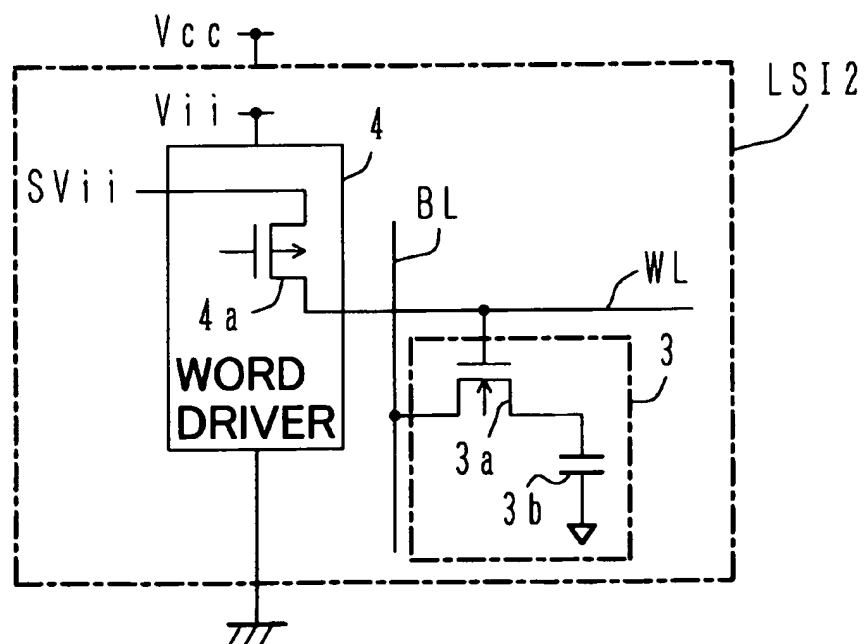
FIG. 5



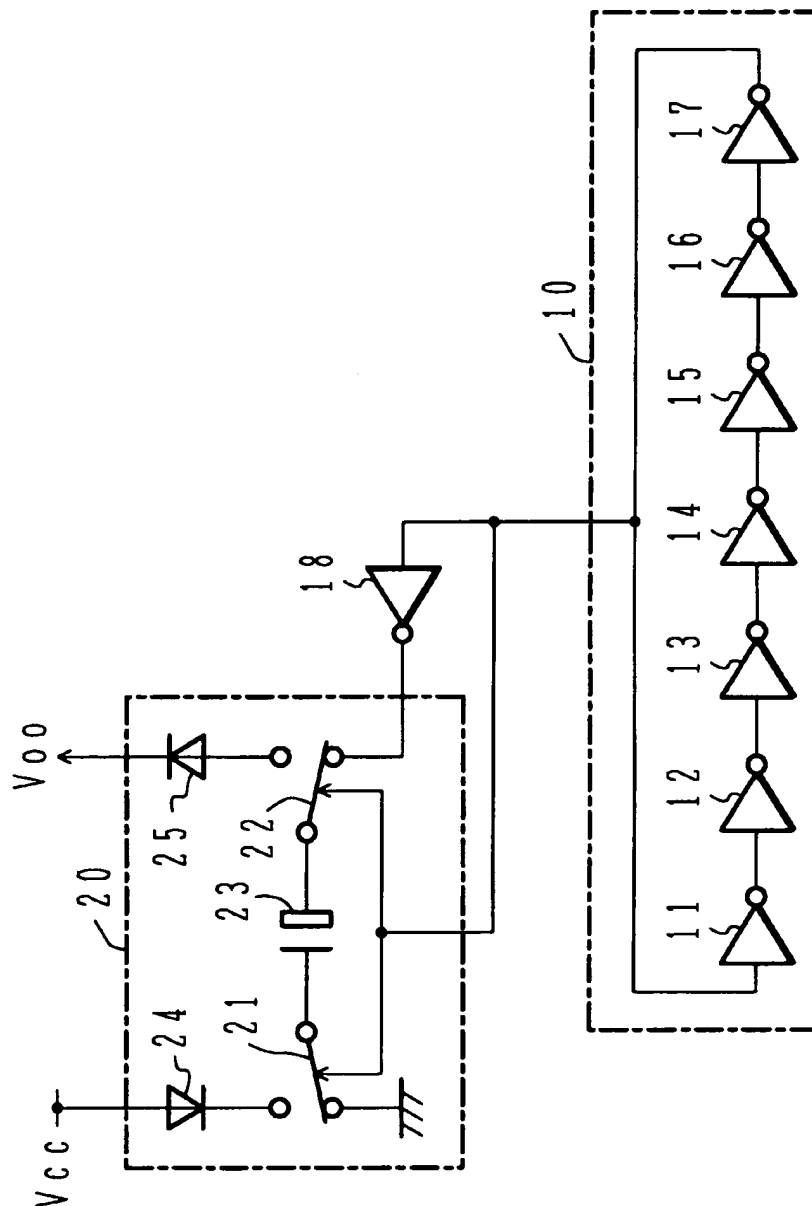
**FIG. 6(A)**  
***prior art***



**FIG. 6(B)**  
**prior art**



**FIG. 7**  
***prior art***



## STEP-UP CIRCUIT USING TWO FREQUENCIES

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a step-up circuit and a semiconductor device employing same.

#### 2. Description of the Related Art

In a semiconductor integrated circuit, along with the minuteness of circuit elements and large-scale circuits, power-supply voltages are being lowered, and different power-supply voltages are being used to power multiple semiconductor devices mounted on printed circuit boards.

In the semiconductor device LSII of FIG. 6(A), for example, an internal circuit 1 as a mainframe circuit operates with a power-supply voltage of  $V_{ii}=2.4$  V. To standardize the power-supply voltage supplied to the various semiconductor devices, an external power-supply voltage of  $V_{cc}=3.0$  V is stepped down to an internal voltage of  $V_{ii}$  by an nMOS transistor 2. Gate potential  $V_{gn}$  is generated at a control circuit (not shown) and provided to the gate electrode of the nMOS transistor 2 to make the internal voltage  $V_{ii}$  constant. By using a pMOS transistor, external power-supply voltage  $V_{cc}$  can be used in the control circuit. However, since gate potential  $V_{gn}$  is about 3.3 V, which is higher than external potential  $V_{cc}$ , an internal step-up circuit is required when using an nMOS transistor.

Here, when using an nMOS as the transistor 2, because it is possible to achieve higher-speed operation than when using a pMOS transistor, the internal power-supply voltage can be better stabilized.

When using a pMOS as the transistor 2, because of the relationship between the inductance component of the external pin connected to the source of the transistor and the feedback control circuit for the pMOS gate potential, overdrive occurs and a back electromotive force which cannot be ignored is generated at the inductance component, causing power supply noise. When using an nMOS transistor, the relationship with the gate potential control circuit is different from the described above, and no such a problem occurs. For these reasons, it is preferred to use an nMOS as the transistor 2.

FIG. 6(B) shows part of semiconductor memory storage LS12 as an example for another occasion requiring an internal step-up circuit. For example, when the charge stored at a capacitor 3b is transferred to a bit line BL by turning on an nMOS transistor 3a, the potential change of the bit line BL is small since the capacity of the bit line BL exceeds that of capacitor 3b. Also, the resistance of Word line WL connected to the gate electrode of the nMOS transistor 3a is considerably high. Therefore, the potential drops that may occur when the electric charge flows through nMOS transistor 3a must be minimized. So, a potential  $SV_{ii}$  provided to the word line WL through a pMOS transistor 4a of a Word driver 4 is set high. For example, the potential  $SV_{ii}$  is 4.5 V when  $V_{ii}=2.4$  V, and an internal step-up circuit is needed.

FIG. 7 shows a prior art step-up circuit. In this circuit, a clock is generated by a ring oscillator 10 comprising inverters 11 to 17 connected in a ring shape. This clock is provided to a charging pump circuit 20 via a buffering inverter 18. The output of ring oscillator circuit 10 is also used for On/Off control of switch elements 21 and 22. If this output is at a low level and switch elements 21 and 22 are in the status shown in the figure, a pumping capacitor 23 is charged by an output potential  $V_{cc}$  of the inverter 18. Next, if the output of

the ring oscillator circuit 10 transits to a low level, switches 21 and 22 are respectively switched to the cathode side of diode 24 and anode side of diode 25, and the voltage of the pumping capacitor 23 is added to the external power-supply voltage  $V_{cc}$ . Thereby, the cathode potential  $V_{00}$  of the diode 25 becomes  $2(V_{cc}-V_{pn})$ , where  $V_{pn}$  is a forward voltage of each diodes 24 and 25. Although the output voltage  $V_{00}$  is lowered according to power consumption, by repeating this step-up operations the voltage  $V_{00}$  can be obtained.

The charging pump circuit 20 in FIG. 7 shows the principle configuration, and actually switch elements are used instead of diodes 24 and 25 in order to reduce the drop in voltage  $V_{pn}$  and the switch elements are turned off during the blocking time for back flow.

When such a step-up circuit is applied to, for example, a circuit generating the gate potential  $V_{gn}$  of the semiconductor device LSII shown in FIG. 6(A) and the power is supplied to the semiconductor device LSII, the problems as described below are encountered. Namely, since the step-up circuit will not operate until the external power supply potential  $V_{cc}$  reaches a specified potential, and since voltages drop due to power consumption, it takes, e.g., 400  $\mu$  second for the power supply voltage  $V_{00}$  to reach the specified value  $\pm 10\%$ , which delays starting operation of the internal circuit 1.

To accelerate the startup time for voltage  $V_{00}$  by increasing the output frequency of the ring oscillator circuit 10 will cause a load driving capacity of the step-up circuit to become unnecessarily large after startup, a power waste arising.

### SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a step-up circuit and a semiconductor device employing same which can reduce the time for a step-up voltage to reach a target value after power-on and save power consumption in normal operation.

According to the 1st aspect of the present invention, there is provided a step-up circuit comprising: a selection control circuit for setting a control signal at one state in response to an external power-supply voltage being above a value which is lower than a normal voltage; a clock generating circuit for providing a first clock with a first frequency when the control signal not being at the one state and for providing a second clock with a second frequency when the control signal being at the one state, the second frequency being lower than the first frequency; and a charging pump circuit driven by the first and second clocks.

With the 1st aspect of the present invention, since the output clock frequency of the clock generation circuit becomes the first frequency higher than the second frequency at the initial stage after a power-on, the charging pump circuit is driven by this clock to step up the power-supply voltage at a high-speed, thus reducing the time needed for the step-up voltage to reach the target value after power-on.

Also, after a mini power failure, the step-up circuit is operated the same way as described above, reducing a failure-recovery time.

Moreover, after the internal power-supply voltage reaches the target value, the output clock frequency of the clock generation circuit is the second frequency lower than the first frequency, and the charging pump circuit is driven by this clock for step-up operation, thus effectively saving power consumption in normal operation.

In the 1st mode of the 1st aspect of the present invention, the clock generating circuit comprises: a first ring oscillator

circuit for generating the first clock when the control signal is not at the one state; a second ring oscillator circuit for generating the second clock; and a selection circuit for selectively providing the first clock to the charging pump when the control signal is not at the one state and for selectively providing the second clock to the charging pump when the control signal is at the one state.

In the 2nd mode of the 1st aspect of the present invention, the clock generating circuit comprises: a ring oscillator including an odd number of CMOS inverters connected in ring shape, each of the CMOS inverters has a pMOS transistor and a nMOS transistor connected in serial to each other, a first pMOS transistor connected between the pMOS transistor of the CMOS inverter and a power-supply potential conductor, its gate electrode receiving a potential to normally turn on the first pMOS transistor; a second pMOS transistor connected between the pMOS transistor of the CMOS inverter and the power-supply potential conductor, its gate electrode receiving a signal associated with the control signal to turn on the second pMOS transistor when the control signal is not at the one state; a first nMOS transistor connected between the nMOS transistor of the CMOS inverter and a reference potential conductor, its gate electrode receiving a potential to normally turn on the first nMOS transistor; and a second nMOS transistor connected between the nMOS transistor of the CMOS inverter and the reference potential conductor, its gate electrode receiving a signal associated with the control signal to turn on the second pMOS transistor when the control signal is not at the one state.

In the 3rd mode of the 1st aspect of the present invention, the second pMOS transistor have a value of (gate width)/(gate length) which is larger than that of the first pMOS transistor, and the second nMOS transistor have a value of (gate width)/(gate length) which is larger than that of the first nMOS transistor.

With the 3rd mode of the 1st aspect of the present invention, since the first frequency at the initial stage after a power-on becomes more higher, it takes less time for a step-up voltage to reach the target value.

In the 4th mode of the 1st aspect of the present invention, the clock generating circuit comprises: a first multi-stage inverter circuit including an odd number, which is 5 or more, of inverters connected in cascade; a second multi-stage inverter circuit including an even number of inverters connected in cascade; a first switch element connected between an output of a last stage inverter of the first multi-stage inverter circuit and an input of a first stage inverter of the second multi-stage inverter circuit; a second switch element connected between an output of a last stage inverter of the second multi-stage inverter circuit and an input of a first stage inverter of the first multi-stage inverter circuit; and a third switch element connected between the output of the last stage inverter of the first multi-stage inverter circuit and the input of the first stage inverter of the first multi-stage inverter circuit; the first, second and third switch elements being turned on, on and off respectively when the control signal is at the one state, and the first, second and third switch elements being turned off, off and on respectively when the control signal is not at the one state.

With the 4th mode of the 1st aspect of the present invention, it is possible to reduce the number of configuration elements of the clock generation circuit more than that of the first mode.

In the 5th mode of the 1st aspect of the present invention, the charging pump circuit comprises a capacitor which

voltage is added to a voltage between the power-supply potential and the reference potential and which capacitance is switched by the control signal in such a way that a value of the capacitance in the case of the control signal not being at the one state is larger than that in the case of the control signal being at the one status.

With the 5th mode of the 1st aspect of the present invention, since the first frequency at the initial stage after a power-on becomes more higher, it takes less time for a step-up voltage to reach the target value.

According to the 2nd aspect of the present invention, there is provided a semiconductor device comprising a step-up circuit formed on a semiconductor chip, wherein the step-up circuit comprises: a selection control circuit for setting a control signal at one state in response to an external power-supply voltage being above a value which is lower than a normal voltage; a clock generating circuit for providing a first clock with a first frequency when the control signal is not at the one state and for providing a second clock with a second frequency when the control signal is at the one state, the second frequency being lower than the first frequency; and a charging pump circuit driven by the first and second clocks.

In the 1st mode of the 2nd aspect of the present invention, the charging pump circuit operates under the external power-supply voltage, wherein the semiconductor device further comprises: a circuit operated under an internal power-supply voltage lower than the external power-supply voltage; a wiring, an nMOS step-down transistor, its drain receiving the external power-supply voltage, its source supplying the internal power-supply voltage; and a control circuit, operated under an output voltage of the charging pump circuit, for providing a constant voltage to a gate electrode of the nMOS step-down transistor.

In the 2nd mode of the 2nd aspect of the present invention, the charging pump circuit operates under an internal power-supply voltage lower than the external power-supply voltage, wherein the semiconductor device further comprises: a memory cell including a nMOS transistor with its gate electrode connected to a word line; and a word driver transistor through which an output voltage of the charging pump is provided to the word line.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing a semiconductor device, to which a step-up circuit of the present invention is applied, of a first embodiment according to the present invention;

FIG. 2 is a diagram showing an operation of the circuit of FIG. 1;

FIG. 3 is a diagram showing a ring oscillator circuit of a second embodiment used for a step-up circuit of the present invention;

FIG. 4 is a circuit diagram showing a semiconductor device, to which a step-up circuit of the present invention is applied, of a third embodiment according to the present invention;

FIG. 5 is a circuit diagram showing a semiconductor device, to which a step-up circuit of the present invention is applied, of a fourth embodiment according to the present invention;

FIGS. 6(A) and 6(B) are diagrams each showing a prior art circuit necessary for a step-up circuit; and

FIG. 7 is a diagram showing a prior art step-up circuit.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference characters designate like or corresponding parts throughout

several views, preferred embodiments of the present invention are described below.

#### First Embodiment

FIG. 1 shows a semiconductor device, to which a step-up circuit of the present invention is applied, of the first embodiment. In FIG. 1, the same configuration elements as in FIGS. 6(A) and FIG. 7 are designated by the same reference characters and these explanation are omitted.

In this step-up circuit, a ring oscillator circuit 30, a selection circuit 40 and a selection control circuit 50 are added to a ring oscillator circuit 10, an inverter 18 and a charging pump circuit 20 of FIG. 7. The charging pump circuit 20 is shown as the principle configuration for simplification as described above.

The ring oscillator circuit 30 consists of an inverter 31, an inverter 32 and a NAND gate 33 which are connected in a ring shape.

If one input, as a control input, of the NAND gate 33 becomes a low, the ring oscillator circuit 30 does not oscillate. If this low level transits to a high, the NAND gate will function as an inverter and the ring oscillator circuit 30 will then oscillate, and a clock of a frequency  $F_s$  is output as pumping pulses. On the other hand, a clock of a frequency which is lower than frequency  $F_s$  is always output as pumping pulses from the ring oscillator circuit 10.

Selection circuit 40 is provided with transfer gates 41 and 42 and inverter 43. Input ends of transfer gates 41 and 42 are connected to the outputs of the ring oscillator circuits 10 and 30, respectively, and output ends thereof are connected to the input of the inverter 18 and to the control inputs of switch elements 21 and 22. Each of the transfer gates 41 and 42 is constructed by connecting a pMOS transistor and an nMOS transistor in parallel. A start/stop signal STP is provided to the gate electrodes of the nMOS transistor of the transfer gate 41 and of the pMOS transistor of the transfer gate 42. A signal \*STP, generated by inverting the binary value of the start/stop signal STP at inverter 43, is provided to the gate electrodes of the pMOS transistor of the transfer gate 41 and of the nMOS transistor of the transfer gate 42. The start/stop signal \*STP is also provided to the input, as the control input, of the NAND gate 33.

When the start/stop signal STP is at a low level, the transfer gates 41 and 42 are off and on respectively and the output clock of the ring oscillator circuit 30 is output from the selection circuit 40. Whereas, when the start/stop signal STP is at a high level, the transfer gates 41 and 42 are on and off respectively and the output clock of the ring oscillator 10 is output from the selection circuit 40.

A power-supply voltage for the ring oscillator circuits 10 and 30 and the selection circuit 40 is an external power-supply voltage  $V_{cc}$ .

In the selection control circuit 50, resistors 51 and 52 are serially connected between a  $V_{cc}$  wiring supplied with an external power-supply potential  $V_{cc}$  and a grounding wiring, and a divided potential  $V_r$  at its connection is provided to the gate electrode of an nMOS transistor 53. The source of the nMOS transistor 53 is connected to the grounding wiring, with its drain connected via a resistor 54 to the  $V_{cc}$  wiring. The drain potential of the nMOS transistor 53 is provided to the gate electrodes of a pMOS transistor 55 and an nMOS transistor 56. The pMOS transistor 55 and the nMOS transistor 56 are serially connected between the  $V_{cc}$  wiring and the grounding wiring, and consists of a CMOS inverter. The start/stop signal STP is output from the output of this inverter.

When the external power-supply potential  $V_{cc}$  has risen to, e.g., 0.4 V from 0 V after power-on, the nMOS transistor

56 turns on, and further when the potential  $V_{cc}$  has risen to 2 V, the divided potential  $V_r$  reaches 0.4 V and the nMOS transistor 53 turns on. Thereby, the pMOS transistor 55 turns on, the nMOS transistor 56 turns off, and the start/stop signals STP and \*STP respectively become high and low.

An nMOS transistor 57 connected between the gate electrode of the nMOS transistor 53 and the  $V_{cc}$  wiring is normally off, but turns on when the external power-supply potential  $V_{cc}$  has dropped near to 0 V by a mini power failure. Thereby the charge at the gate of the nMOS transistor 53 is discharged quickly through the nMOS transistor 57 and when the potential  $V_{cc}$  subsequently rises, the described above operation is ensured.

In a step-down circuit 60, the relationship  $V_{ji} = V_{gn} - V_{th}$  holds, where  $V_{gn}$  and  $V_{th}$  are a gate potential and a threshold voltage of the nMOS transistor 2, respectively. To generate the internal power-supply potential of  $V_{ii} = 2.4$  V even when the external power-supply potential  $V_{cc}$  is such a low as 2.4 or so,  $SV_{cc}$  of, for example, 4.0 V is supplied to a comparator 61.

At the inverting input of the comparator 61, a reference potential  $V_{ref}$  from a reference potential generator circuit 62 is provided, and a gate potential  $V_{gp}$  is output from the comparator 61. Between a wiring of the power-supply potential  $SV_{cc}$  and the grounding wiring, a pMOS transistor 63, an nMOS transistor 64, a resistor 65, and a resistor 66 are serially connected. At the gate electrode of a pMOS transistor 63, the gate potential  $V_{gp}$  is provided. The source potential  $V_{gn}$  of the pMOS transistor 63 is provided to the gate electrode of the nMOS transistor 2. The drain of the nMOS transistor 2 is connected to the  $V_{cc}$  wiring, and the external potential  $V_{cc}$  is lowered, for instance, to 2.4 V for supplying to an internal circuit 1.

The drain and the gate electrodes of the nMOS transistor 64 are short-circuited in order to prevent the internal power-supply potential  $V_{ii}$  from changing according to ambient temperature. A potential  $V_d$  at the connection point of the resistors 65 and 66 is provided to the non-inverting input of the comparator 61.

The comparator 61 outputs the gate potential  $V_{gp}$  so that the potential  $V_d$  becomes equal to the reference potential  $V_{ref}$ . In other words, if  $V_d < V_{ref}$ , then the gate potential  $V_{gp}$  drops and the current flowing through pMOS transistor 63 increases, raising the potential  $V_d$ . Whereas, if  $V_d > V_{ref}$ , then the gate potential  $V_{gp}$  is raised, and the current flowing through pMOS transistor 63 decreases, lowering the potential  $V_d$ .

Referring to FIG. 2, followings are explanations of the operation of the semiconductor device configured as described above.

When the power is turned on,  $V_{cc}$  increases linearly from 0 V to 3.0 V. At a midpoint in this increase, when  $V_{cc}$  reaches about 1.0 V, the step-up circuit starts to operate. At this time, the start/stop signal STP is a low, the transfer gate 41 is off, and the transfer gate 42 is on. The output clock of the ring oscillator circuit 30 is provided via the transfer gate 42 and the inverter 18 to the charging pump circuit 20. In this way, more high-speed step-up operation can be performed than the case of driving the charging pump circuit 20 by using the output clock of the ring oscillator circuit 10.

After that midpoint, when  $V_{cc}$  reaches about 2.0 V,  $V_r$  becomes about 0.4 V, and the nMOS transistor 53 is turned on, the pMOS transistor 55 is turned on and the nMOS transistor 56 is turned off, thereby the start/stop signal STP becomes a high. Then, the transfer gates 41 and 42 turn on and off respectively, and the output clock of ring oscillator

circuit 10 is provided via transfer gate 41 and inverter 18 to the charging pump circuit 20, thereby appropriately lowering the step-up operation speed of the charging pump circuit 20.

After this, when SVcc reaches about 4.0 V, Vgn becomes about 3.3 V and Vii becomes about 2.4 V. Although, Vcc is raised up to 3.0 V after this, SVcc, Vgn and Vii are almost constant.

According to the first embodiment, because the charging pump circuit 20 is driven by the higher frequency output of the ring oscillator circuit 30 at the initial stage after a power-on, the Potential SVcc is stepped up at high-speed, allowing to take 200  $\mu$ second for the internal power-supply potential Vii to reach the target value  $\pm 10\%$ , compared to the conventional 400  $\mu$ second, and reducing the startup time of the internal circuit 1 after a power-on.

After a mini power failure, the step-up circuit is operated the same way as described above, allowing to reduce a failure-recovery time.

After the internal power-supply potential Vii has reached the target value, the ring oscillator circuit 30 stops its operation, and the charging pump circuit 20 is driven by the output of the ring oscillator circuit 10 for step-up operation, allowing to save power consumption in ordinary operation.

#### Second Embodiment

FIG. 3 shows a ring oscillator circuit 10A of the second embodiment that is employed instead of the ring oscillator circuits 10, 30 and the selection circuit 40 in FIG. 1.

This circuit is the same as the ring oscillator circuit 10 in the point where inverters 11 to 17 are connected in ring shape. pMOS transistors 71PL and 71PS are connected in parallel between one end of the inverter 11 and the Vcc wiring. The gate widths of the pMOS transistors 71PL and 71PS are the same but the gate length of the pMOS transistor 71PL is longer than the pMOS transistor 71PS. nMOS transistors 71NL and 71NS are connected in parallel between the other end of the inverter 11 and the grounding wiring. The gate widths of the nMOS transistors 71NL and 71NS are the same, but the gate length of the nMOS transistor 71NL is longer than the nMOS transistor 71NS. The connections for one and the other end of the inverters 12 to 17 are like those of the inverter 11.

The gate electrodes of pMOS transistors 71PL to 77PL are connected to the grounding wiring, and these transistors are normally on. The gate electrodes of nMOS transistors 71NL to 77NL are connected to the Vcc wiring, and these transistors are normally on. The start/stop signal STP is provided to the gate electrodes of the pMOS transistors 71PS to 77PS, and the start/stop signal \*STP is provided to the gate electrodes of the nMOS transistor 71NS to 77NS.

The operation of the ring oscillator circuit 10A configured as described above is as follows.

After power-on, when Vcc reaches about 1.0 V, this circuit starts to operate. At this time, the start/stop signals STP and \*STP are at a low and a high respectively, and the pMOS transistors 71PS to 77PS and nMOS transistors 71NS to 77NS are on. Since a current supply capacity from the Vcc wiring to the inverters 11 to 17, and a current exhausting capacity from the inverters 11 to 17 to the grounding wiring are larger than the case where the pMOS transistors 71PS to 77PS and the nMOS transistors 71NS to 77NS are off, an output frequency f of the ring oscillator circuit 10A becomes higher. Thereby, the charging pump circuit 20 in FIG. 1 driven by the ring oscillator circuit 10A achieves a higher operation speed than normal operation.

After this, when Vcc reaches around 2 V, the start/stop signals STP and \*STP become a high and a low respectively, then the pMOS transistors 71PS to 77PS and the nMOS transistors 71NS to 77NS are turned off, thereby appropriately lowering the output frequency f of the ring oscillator circuit 10A and saving power consumption in normal operation.

#### Third embodiment

FIG. 4 shows a semiconductor device of the third embodiment to which a step-up circuit of the present invention is applied.

In this step-up circuit, a ring oscillator circuit 10B consists of a first part 10a, a second part 10b, a third part 10c and a selection circuit 40A. The first part 10a consists of inverters 11 to 13 connected in cascade. The second part 10b consists of the inverters 14 and 15 connected in cascade and an inverter 19, which is smaller than the inverter 14, connected to the inverter 14 in ring shape. The third part 10c consists of inverters 16 and 17 connected in cascade. The output of the inverter 17 is connected to the input of the inverter 11.

In the selecting circuit 40A, a transfer gate 41 is connected between the output of the inverter 13 and the input of the inverter 14, a transfer gate 42 is connected between the output of the inverter 13 and the input of the inverter 16 and a transfer gate 44 is connected between the output of the inverter 15 and the input of the inverter 16. An on/off control of the transfer gates 41 and 42 is performed by the start/stop signals STP and \*STP in the like manner as the case of FIG. 1. An on/off control of the transfer gate 44 is linked with that of the transfer gate 41.

The inverter 19 prevents a current flow from leaking from the power supply wiring through the inverter 14 to the grounding wiring when the input of the inverter 14 enters in a floating status near a potential Vcc/2.

In a charging pump circuit 20A, a pumping capacitance can be switched according to the start/stop signals. In other words, the positive electrode of the pumping capacitor 23 is connected to the positive electrode of a pumping capacitor 26, and the negative electrode of the pumping capacitor 26 is connected via a transfer gate 27 to the negative electrode of the pumping capacitor 23. The start/stop signals \*STP and STP are respectively provided to the nMOS and pMOS transistors of the transfer gate 27.

Other configurations are the same as those of the first embodiment.

When the start/stop signal STP is at a low, the transfer gates 41 and 44 are off, the transfer gate 42 is on, and a bypass from the output of the inverter 13 via the transfer gate 42 to the input of the inverter 16 is formed, thereby configuring a ring oscillator with 5-stage inverters and allowing to arise a frequency f higher than that of normal operation. Therefore, like effects as in the above first embodiment can be obtained. Also, since the transfer gate 27 is on, the pumping capacitors 23 and 26 are connected in parallel, and the charge amount at the pumping capacitors at every pumping pulse is larger than that of normal operation, thereby increasing a current supply capacity of the charging pump circuit 20A. Thus, the above-described effects improve.

After the above operation, when the start/stop signal STP becomes at a high, the transfer gates 41 and 44 are turned on and the transfer gate 42 is turned off, thereby the 7-stage ring oscillator circuit 10B is configured with the first part 10a, the second part 10b, and the third part 10c, allowing to operate as the same way as the ring oscillator 10 of FIG. 1. Also, the transfer gate 27 is turned off, allowing the charging pump

circuit 20A to operate as the same way as the charging pump circuit 20 of FIG. 1.

#### Fourth Embodiment

FIG. 5 shows a semiconductor device of the fourth embodiment to which a step-up circuit of the present invention is applied.

This device is a semiconductor memory to which the step-up circuit of FIG. 1 is applied, and the power-supply potential SV<sub>ii</sub> output from the charging pump circuit 20 is applied to a word line WL via a pMOS transistor 4a of a word driver 4. For simplification, in FIG. 5, only one memory cell 3 is illustrated.

The charging pump circuit 20 and the selection control circuit 50 are part of the internal circuit 1 of FIG. 1 and the internal power-supply potential V<sub>ii</sub> is applied to the anode of the diode 24 and the power supply wiring in the selection control circuit 50. For example, when V<sub>cc</sub>=3.0 V, V<sub>ii</sub>=2.4 V, the internal power-supply potential SV<sub>ii</sub> is 4.5 V.

According to this semiconductor device, since the time that SV<sub>ii</sub> reaches the target values  $\pm 10\%$  is reduced, the time until a memory access can be started is also reduced compared to prior art.

Although preferred embodiments of the present invention has been described, it is to be understood that the invention is not limited thereto and that various changes and modifications may be made without departing from the spirit and scope of the invention.

For example, although larger (gate width)/(gate length) is preferred for pMOS transistors 71PS to 77PS than pMOS transistors 71PL to 77PL, the present invention may be acceptable without meeting this condition.

The number of the inverters connected in cascade in each ring oscillator of FIGS. 1, 3 and 5 may be any odd number which is 3 or more, and that of ring oscillator 10B in FIG. 4 may be any odd number which is 5 or more.

Charge pump circuit applied to step-up circuit is not limited to the configuration shown in FIG. 1 or 4, and various types of it are applicable.

What is claimed is:

#### 1. A step-up circuit comprising:

- a selection control circuit, receiving an external power supply voltage, for setting a control signal at a first state in response to the external power-supply voltage being lower than a predetermined voltage which is lower than the external power-supply voltage at a stable state;
- a clock generating circuit for providing a first clock with a first frequency when said control signal is at said first state and for providing a second clock with a second frequency when said control signal is at a second state, said second frequency being lower than said first frequency; and
- a charging pump circuit driven by a selected one of said first and second clocks.

#### 2. A step-up circuit according to claim 1 wherein said clock generating circuit comprises:

- a first ring oscillator circuit for generating said first clock when said control signal is at said first state;
- a second ring oscillator circuit for generating said second clock; and
- a selection circuit for selectively providing said first clock to said charging pump circuit when said control signal is at said first state and for selectively providing said second clock to said charging pump circuit when said control signal is at said first state.

3. A step-up circuit according to claim 1 wherein said clock generating circuit comprises a ring oscillator including an odd number of CMOS inverter stages connected in ring shape, each of said CMOS inverter stages includes:

- a CMOS inverter with a pMOS transistor and an nMOS transistor connected in series to each other;
- a first pMOS transistor connected between said pMOS transistor of said CMOS inverter and a power-supply potential conductor, its gate electrode receiving a potential to normally turn on said first pMOS transistor;
- a second pMOS transistor connected between said pMOS transistor of said CMOS inverter and said power-supply potential conductor, its gate electrode receiving said control signal to turn on said second pMOS transistor when said control signal is at said first state;
- a first nMOS transistor connected between said nMOS transistor of said CMOS inverter and a reference potential conductor, its gate electrode receiving a potential to normally turn on said first nMOS transistor; and
- a second nMOS transistor connected between said nMOS transistor of said CMOS inverter and said reference potential conductor, its gate electrode receiving a signal associated with said control signal to turn on said second nMOS transistor when said control signal is at said first state.

#### 4. A step-up circuit according to claim 3,

wherein said second pMOS transistor has a value of (gate width)/(gate length) which is larger than that of said first pMOS transistor; and

wherein said second nMOS transistor has a value of (gate width)/(gate length) which is larger than that of said first nMOS transistor.

#### 5. A step-up circuit according to claim 1 wherein said clock generating circuit comprises:

- a first multi-stage inverter circuit including an odd number, which is 5 or more, of inverters connected in cascade;
  - a second multi-stage inverter circuit including an even number of inverters connected in cascade;
  - a first switch element connected between an output of a last stage inverter of said first multi-stage inverter circuit and an input of a first stage inverter of said second multi-stage inverter circuit;
  - a second switch element connected between an output of a last stage inverter of said second multi-stage inverter circuit and an input of a first stage inverter of said first multi-stage inverter circuit; and
  - a third switch element connected between said output of said last stage inverter of said first multi-stage inverter circuit and said input of said first stage inverter of said first multi-stage inverter circuit;
- said first, second and third switch elements being turned on, on and off respectively when said control signal is at said first state, and said first, second and third switch elements being turned off, off and on respectively when said control signal is at said second state.

6. A step-up circuit according to claim 1 wherein said charging pump circuit comprises a capacitor which voltage is added to said external power-supply voltage and which capacitance is switched by said control signal in such a way that a value of said capacitance when said control signal is at said first state is larger than that when said control signal is at said second state.

7. A semiconductor device comprising a step-up circuit formed on a semiconductor chip, wherein said step-up circuit comprises:



## 11

- a selection control circuit, receiving an external power supply voltage, for setting a control signal at a first state in response to the external power-supply voltage being lower than a predetermined voltage which is lower than the external power-supply voltage at a stable state; 5
  - a clock generating circuit for providing a first clock with a first frequency when said control signal is at said first state and for providing a second clock with a second frequency when said control signal is at a second state, said second frequency being lower than said first frequency; and 10
  - a charging pump circuit driven by a selected one of said first and second clocks.
8. A semiconductor device according to claim 7, wherein said charging pump circuit is connected with a power supply line having said external power-supply voltage, wherein said semiconductor device further comprises: 15
- a circuit connected with a power supply line having an internal power-supply voltage lower than said external power-supply voltage; 20
  - an nMOS step-down transistor, its drain receiving said external power-supply voltage, its source supplying said internal power-supply voltage; and
  - a control circuit, connected with a power supply line 25 having an output voltage of said charging pump circuit, for providing a constant voltage to a gate electrode of said nMOS step-down transistor.
9. A semiconductor device according to claim 7, wherein said charging pump circuit receives an internal power-

## 12

- supply voltage lower than said external power-supply voltage, wherein said semiconductor device further comprises:
- a memory cell including a nMOS transistor with its gate electrode connected to a word line; and
  - a word driver transistor through which an output voltage of said charging pump circuit is provided to said word line.
10. A boost circuit, in a semiconductor integrated circuit receiving a first power supply voltage and a second power supply voltage, which is lower than the first power supply voltage, to operate, comprising:
- a detection circuit connected with a first power supply line having the first power-supply voltage, for detecting when the first power supply voltage is higher than a reference voltage level which is between the first power supply voltage and the second power supply voltage, and for outputting a detection signal;
  - a clock generating circuit for outputting a clock signal with a frequency, the frequency changing to be lower in response to the detection signal indicating that the first power-supply voltage is higher than the reference voltage; and
  - a charge pump circuit connected with the first power supply line for outputting a boost voltage in response to the clock signal.

\* \* \* \* \*



US005892400A

**United States Patent** [19]

van Saders et al.

[11] **Patent Number:** 5,892,400[45] **Date of Patent:** Apr. 6, 1999

[54] **AMPLIFIER USING A SINGLE POLARITY POWER SUPPLY AND INCLUDING DEPLETION MODE FET AND NEGATIVE VOLTAGE GENERATOR**

[75] Inventors: **John van Saders, Asbury; Robert J. Bayruns, Middlesex, both of N.J.**

[73] Assignee: **Anadigics, Inc., Warren, N.J.**

[21] Appl. No.: **764,350**

[22] Filed: **Dec. 12, 1996**

[51] Int. Cl.<sup>6</sup> ..... **H03F 3/16**

[52] U.S. Cl. .... **330/277; 330/296; 327/536**

[58] Field of Search ..... **330/277, 296; 327/535, 536, 537, 538, 539; 323/313, 314**

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,015,609	4/1977	Mensink et al.	128/419
4,175,250	11/1979	Morgan	323/22
4,292,544	9/1981	Ishii et al.	307/52
4,417,202	11/1983	Pascoe	324/51
4,459,538	7/1984	Arai et al.	323/275
4,471,289	9/1984	Duley et al.	323/222
4,527,228	7/1985	Yu	363/98
4,553,047	11/1985	Dillinger et al.	307/297
4,580,065	4/1986	Haque	307/273
4,713,631	12/1987	Enderby et al.	331/36
4,810,905	3/1989	Graham et al.	307/448
4,812,683	3/1989	Fitzpatrick et al.	307/448
4,926,071	5/1990	MacMillan et al.	307/475

4,933,573	6/1990	Takeda et al.	307/296.2
4,994,729	2/1991	Taylor	323/314
5,015,921	5/1991	Carlson et al.	315/208
5,027,266	6/1991	Ishii et al.	363/63
5,050,235	9/1991	Kojima	455/127
5,168,174	12/1992	Naso et al.	307/296.6
5,235,289	8/1993	Kunitomo	330/277
5,247,241	9/1993	Ueda	323/312
5,298,808	3/1994	Terrell et al.	307/475
5,298,869	3/1994	Jinich et al.	330/286
5,300,895	4/1994	Jones	330/251
5,327,583	7/1994	Yamada et al.	455/89
5,374,899	12/1994	Griffiths et al.	330/277
5,408,198	4/1995	Kusunoki	330/277
5,532,640	7/1996	Okunaga	327/536 X

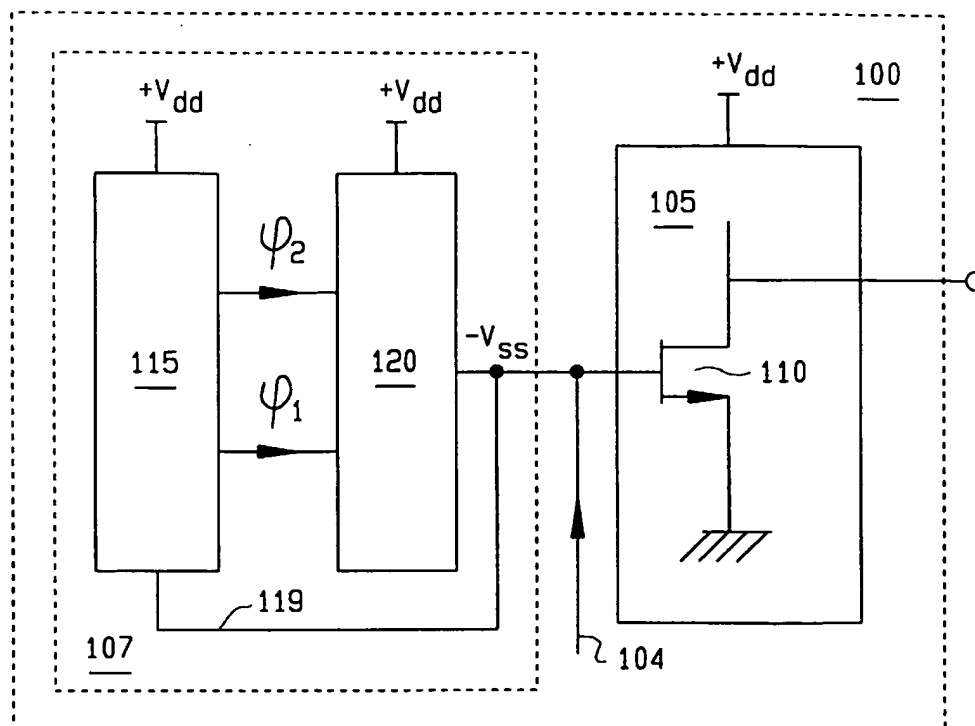
*Primary Examiner*—Steven Mottola

*Attorney, Agent, or Firm*—Pennie & Edmonds LLP

[57] **ABSTRACT**

The present invention provides a power amplifier operating with a single power supply. The amplifier includes at least one depletion-mode FET for amplifying an ac signal and a negative voltage generator for providing a bias to the FET. Preferably the amplifier further includes a negative voltage regulator to provide a regulated bias to bias the FET for a class A, AB or B operation. The negative generator includes a multivibrator for producing two clock signals and a charge pump which receives the clock signals and produces a negative voltage. Advantageously the negative voltage is provided as a low reference potential to the multivibrator so that the clock signals it produced include a negative voltage period, which enables the charge pump to operate in a power efficient manner.

**30 Claims, 18 Drawing Sheets**



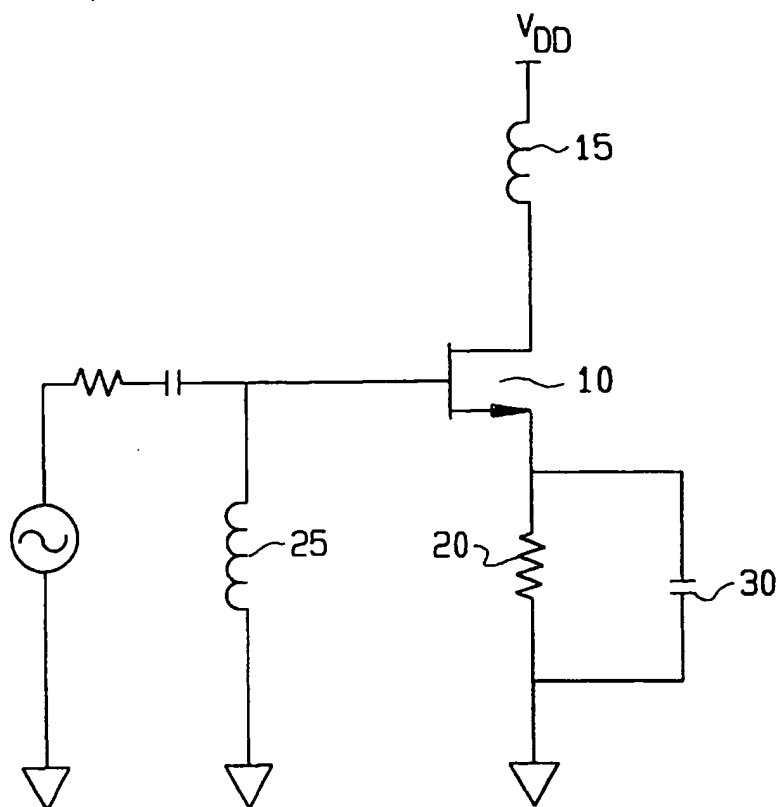


FIG. 1  
Prior Art

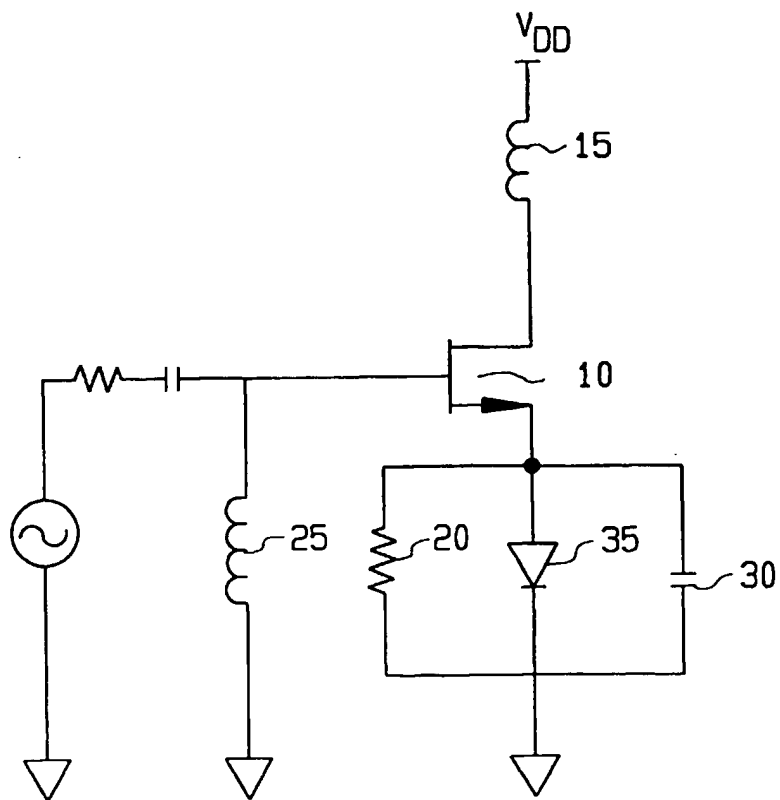
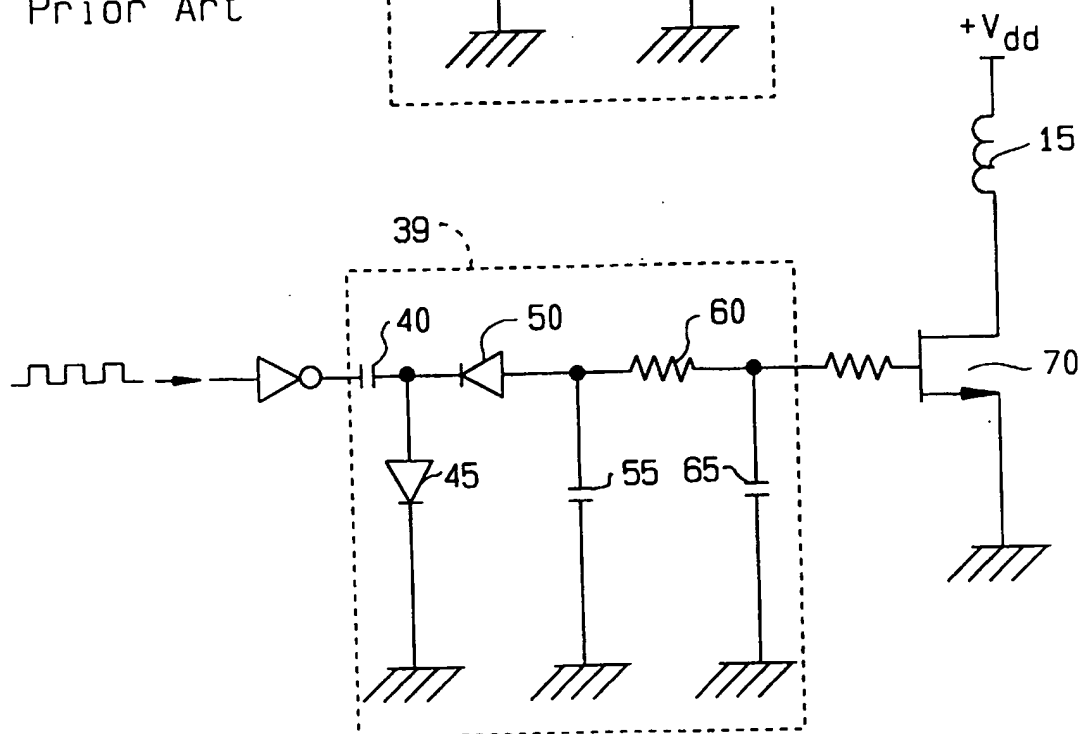
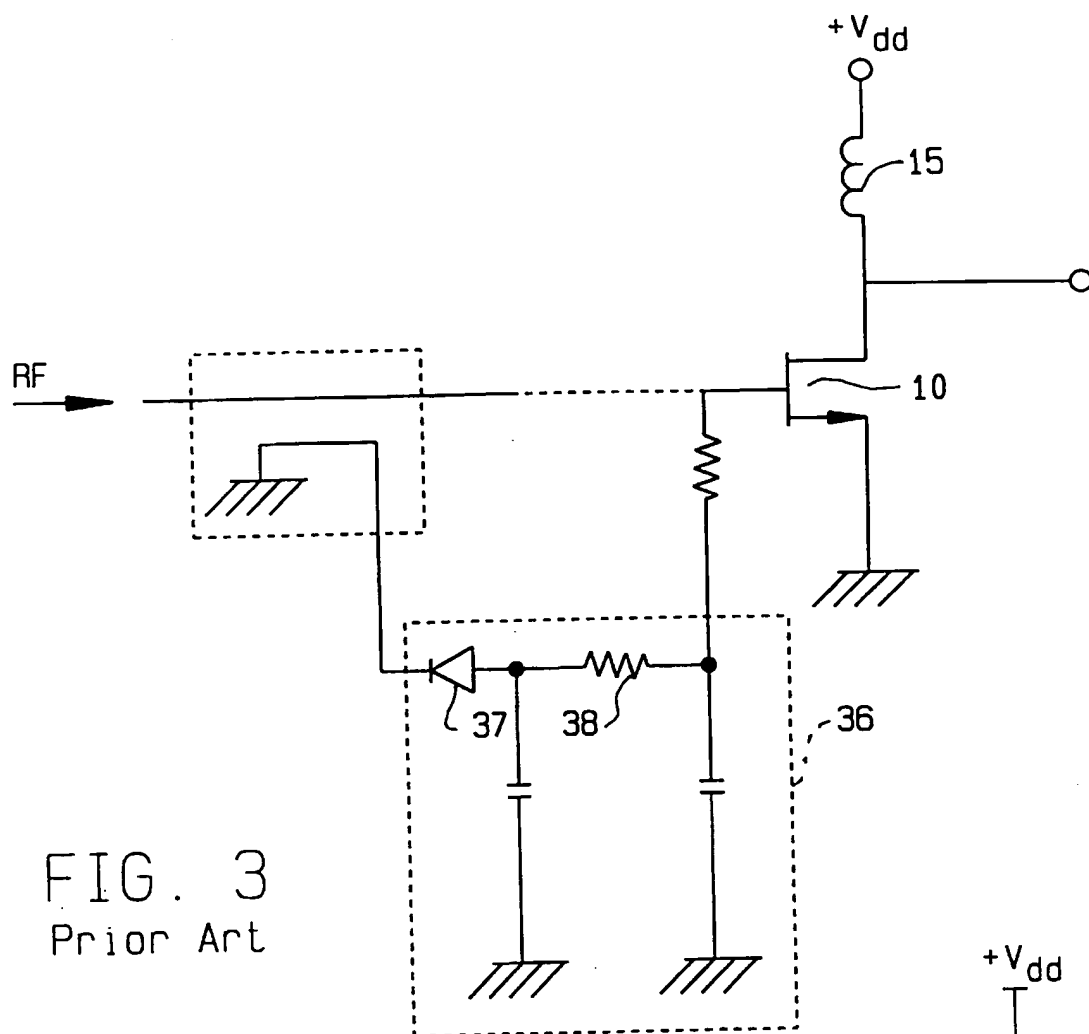


FIG. 2  
Prior Art



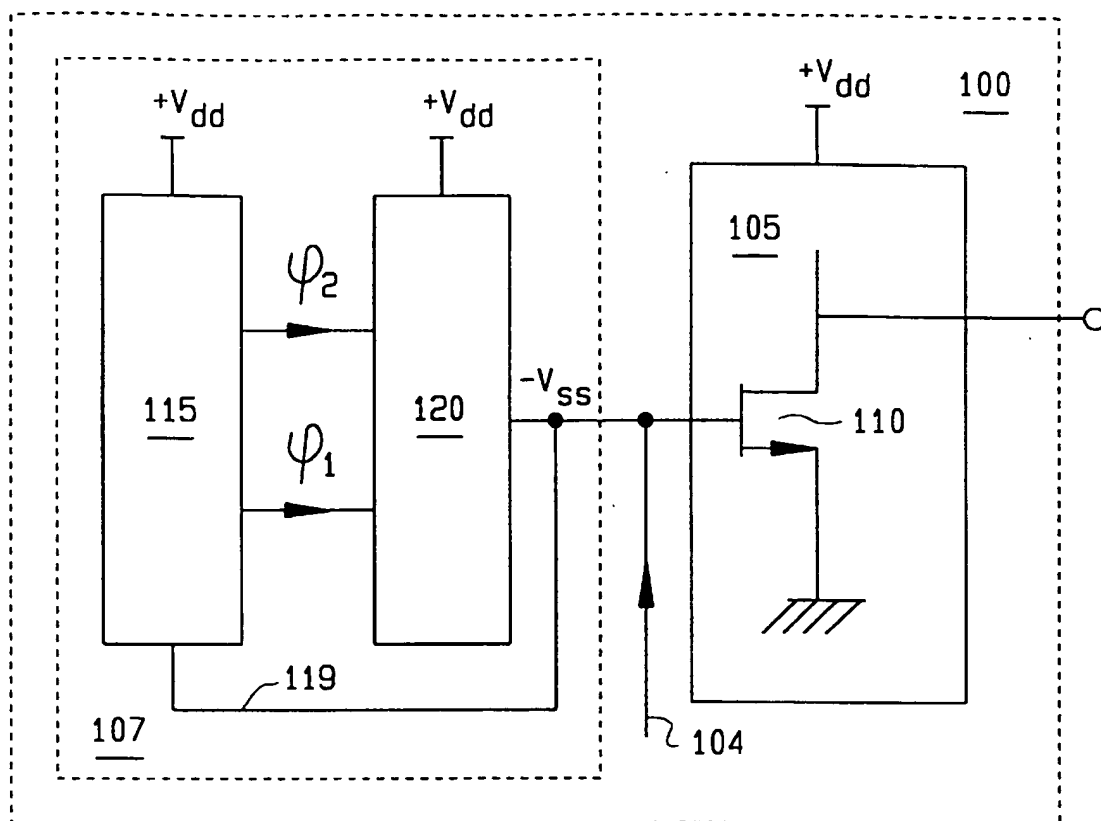


FIG. 5

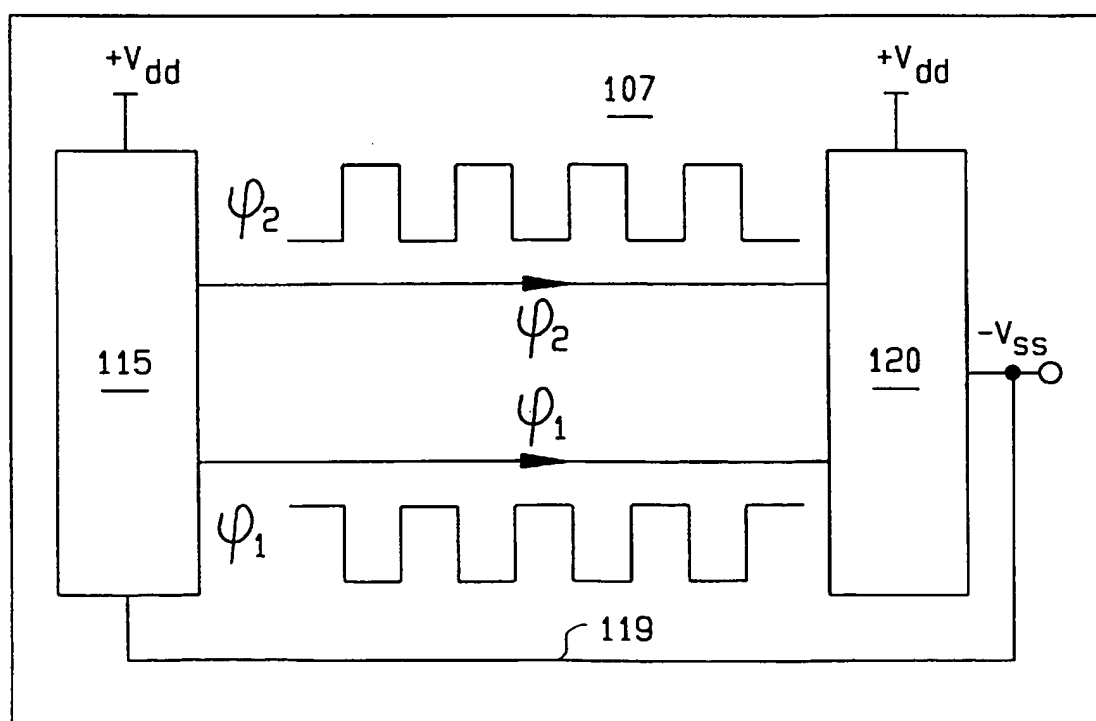


FIG. 6

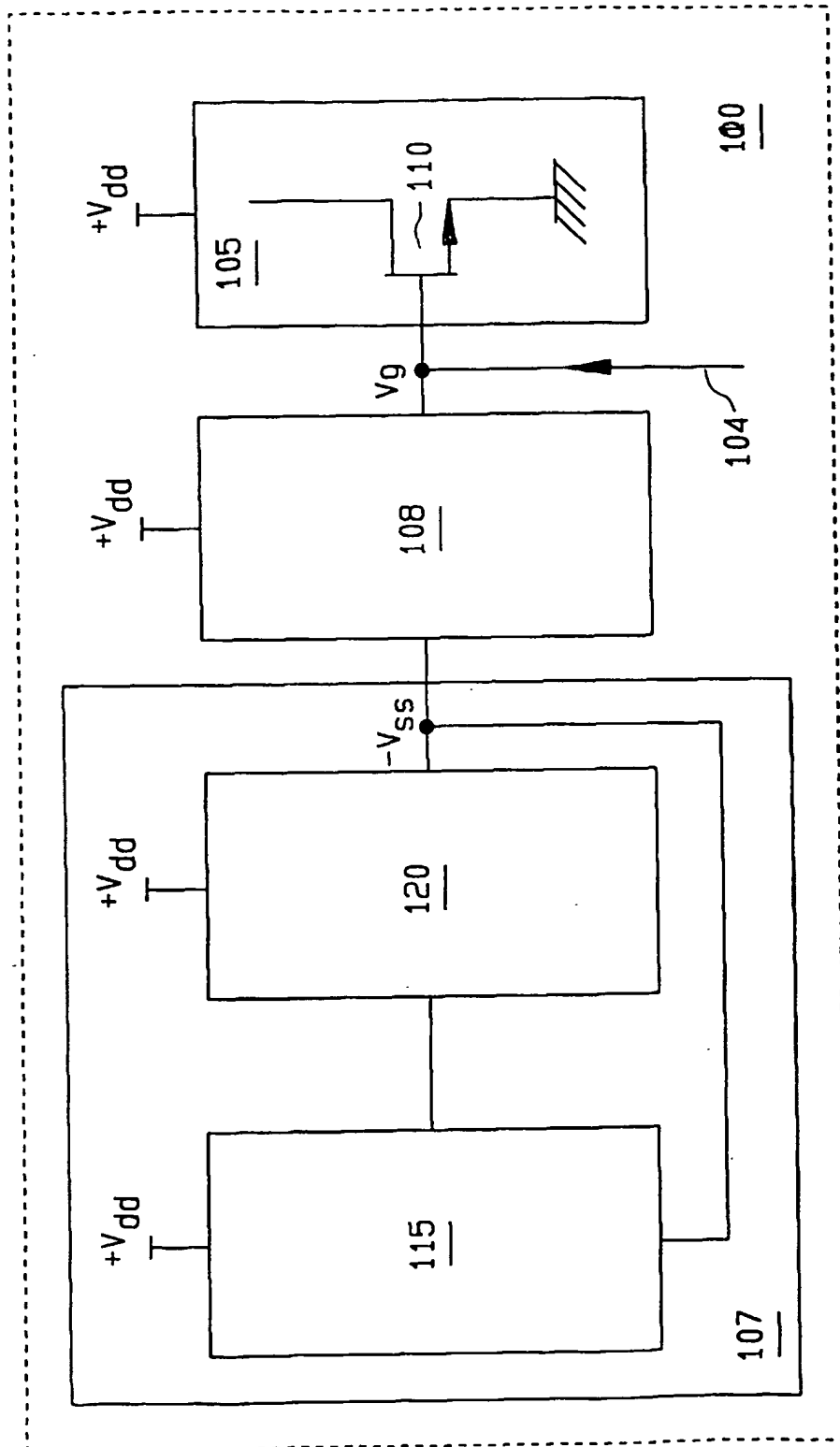


FIG. 7

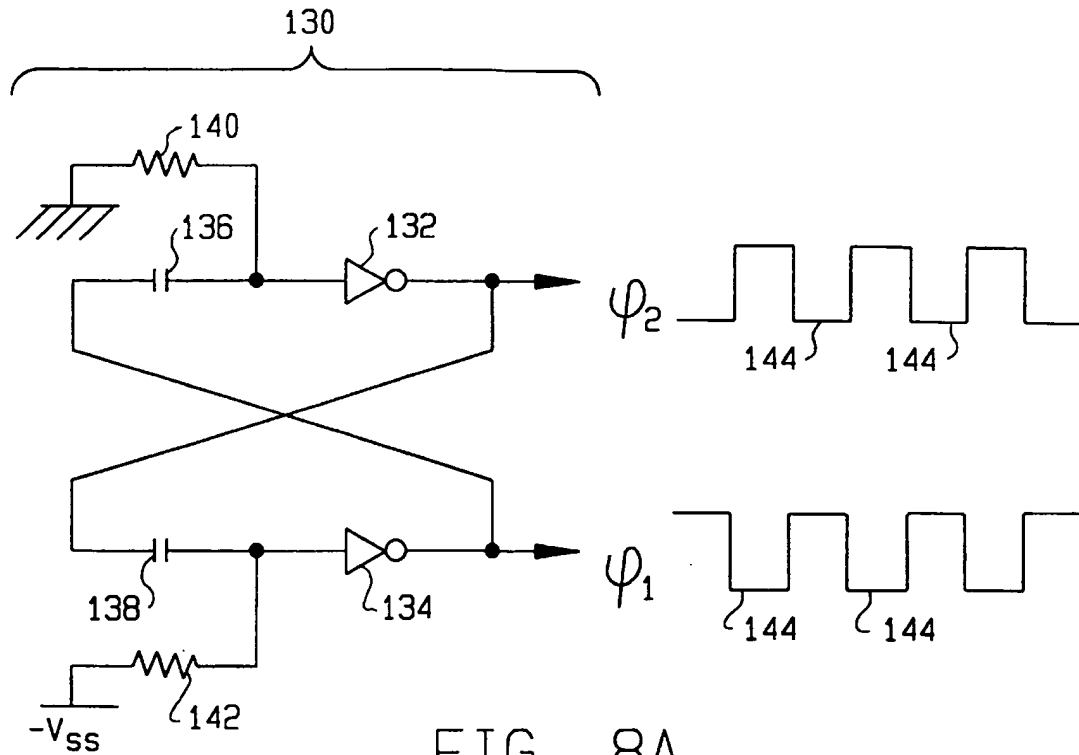


FIG. 8A

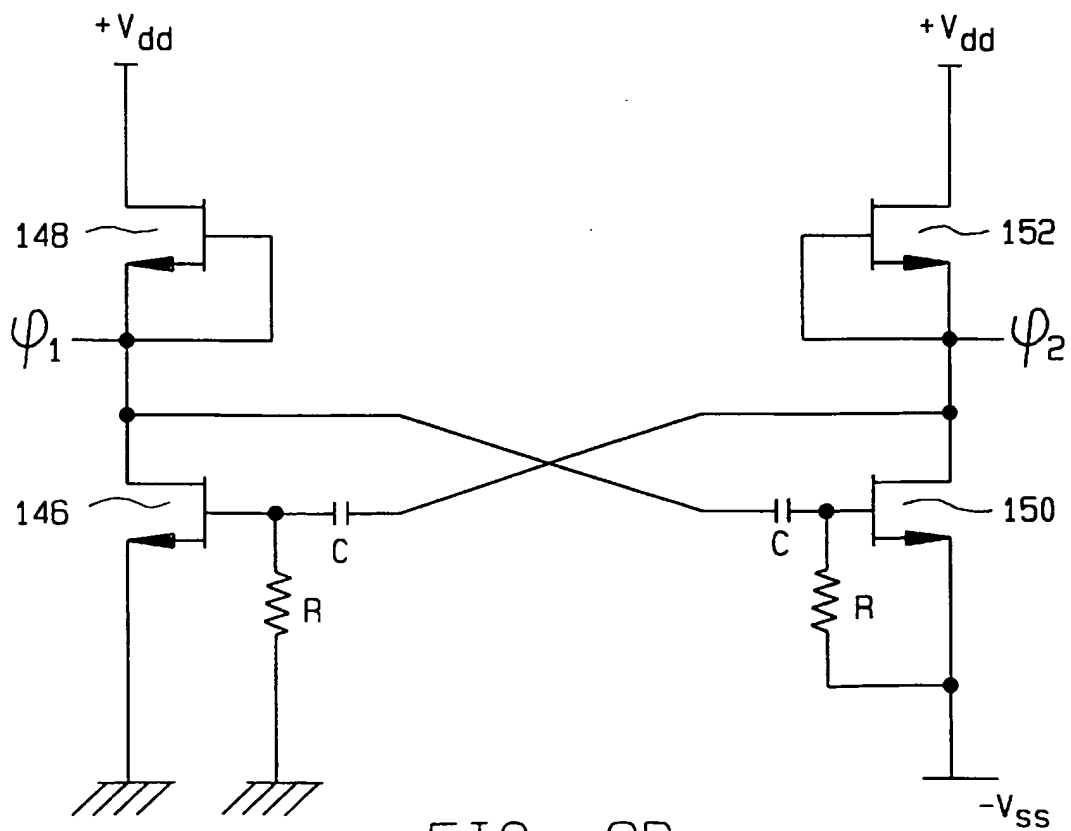


FIG. 8B

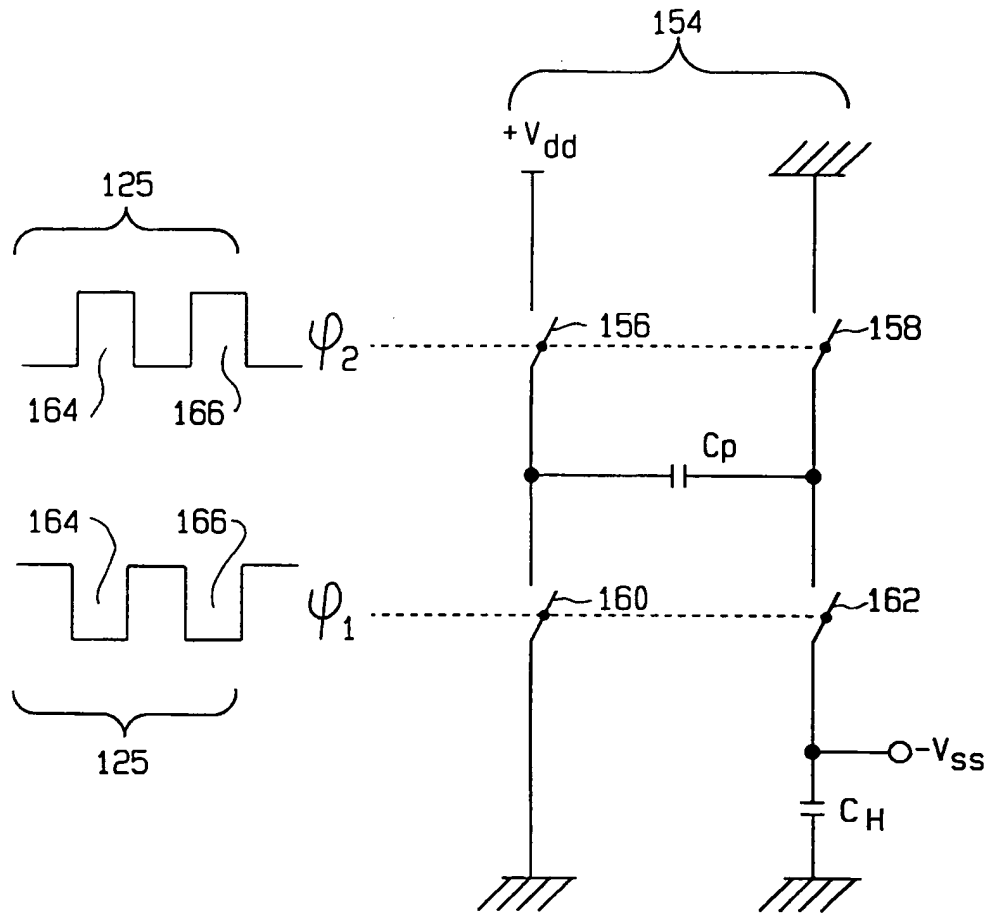


FIG. 9A

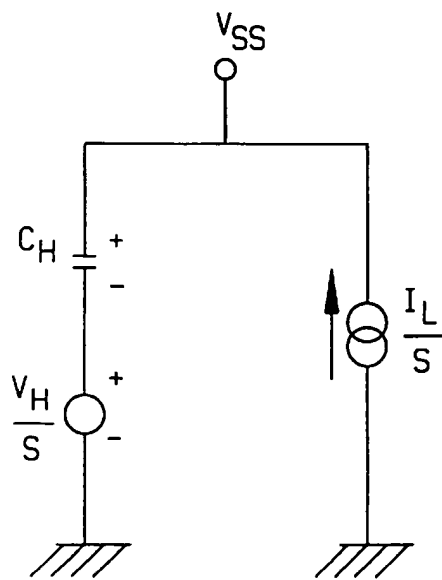


FIG. 9B

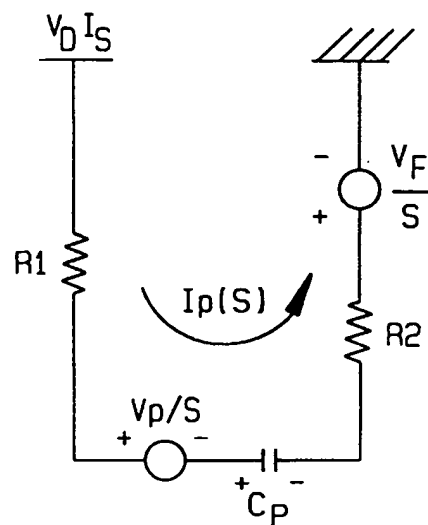


FIG. 9C



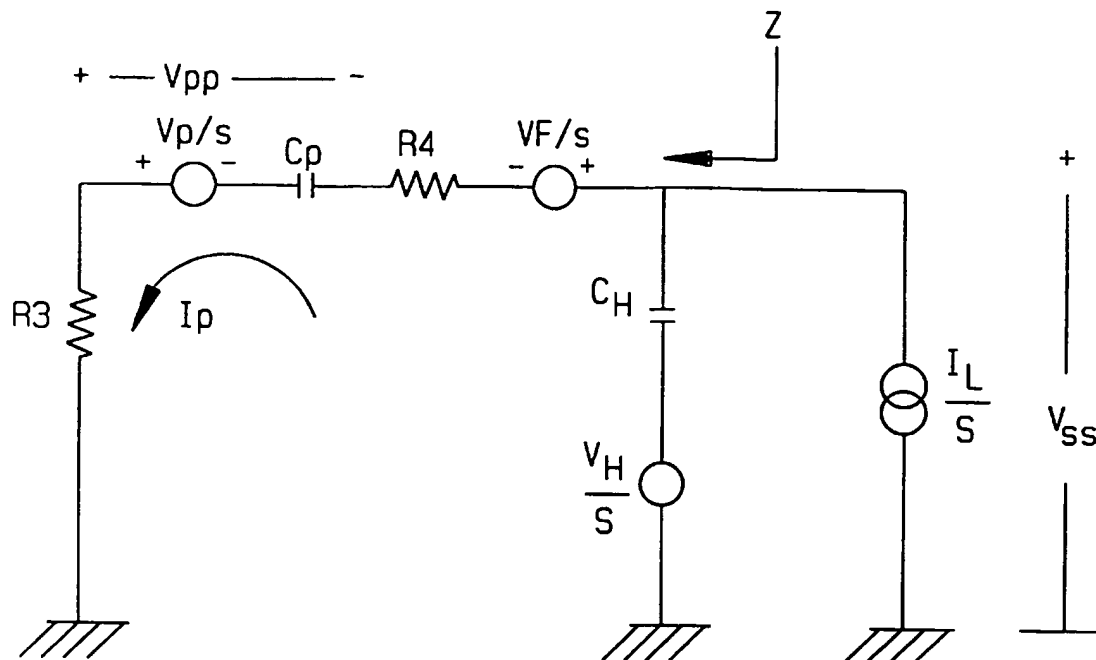


FIG. 9D

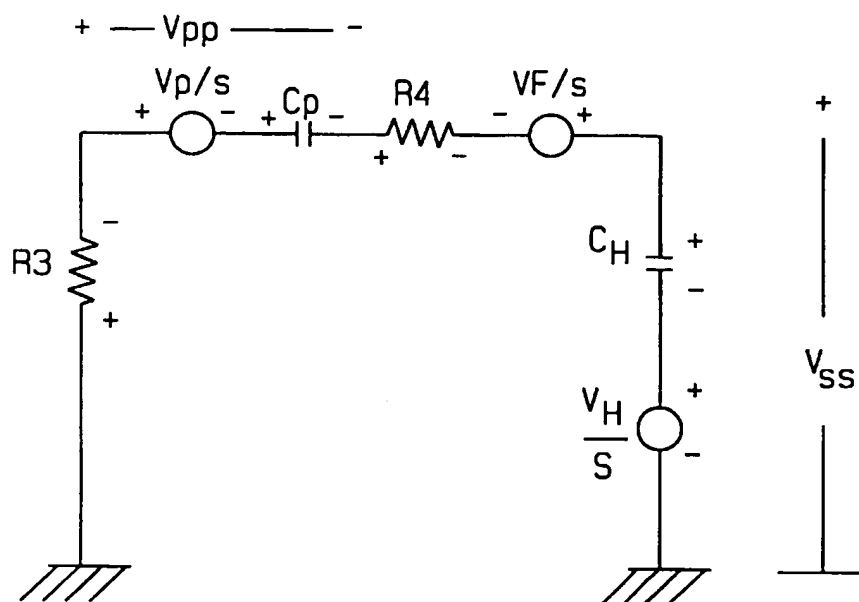


FIG. 9E

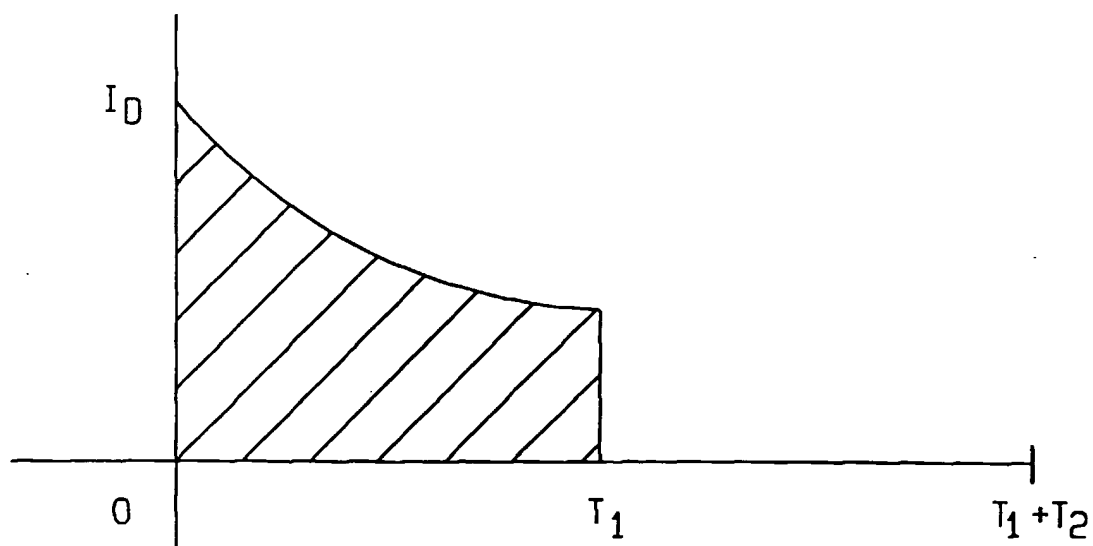


FIG. 9F

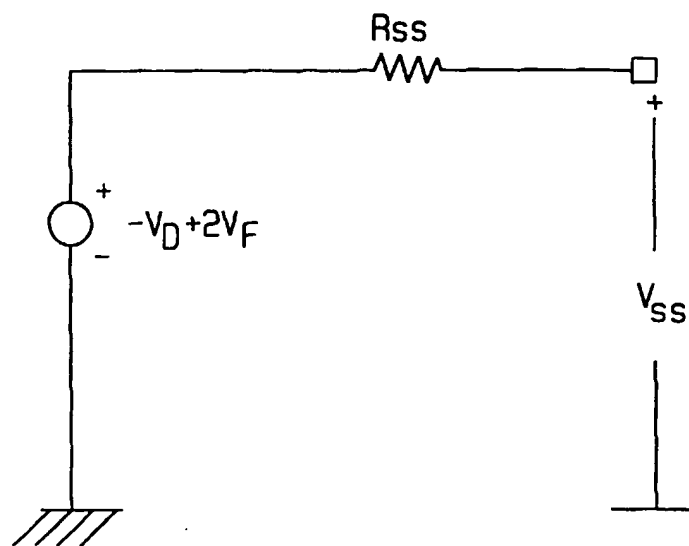


FIG. 9G

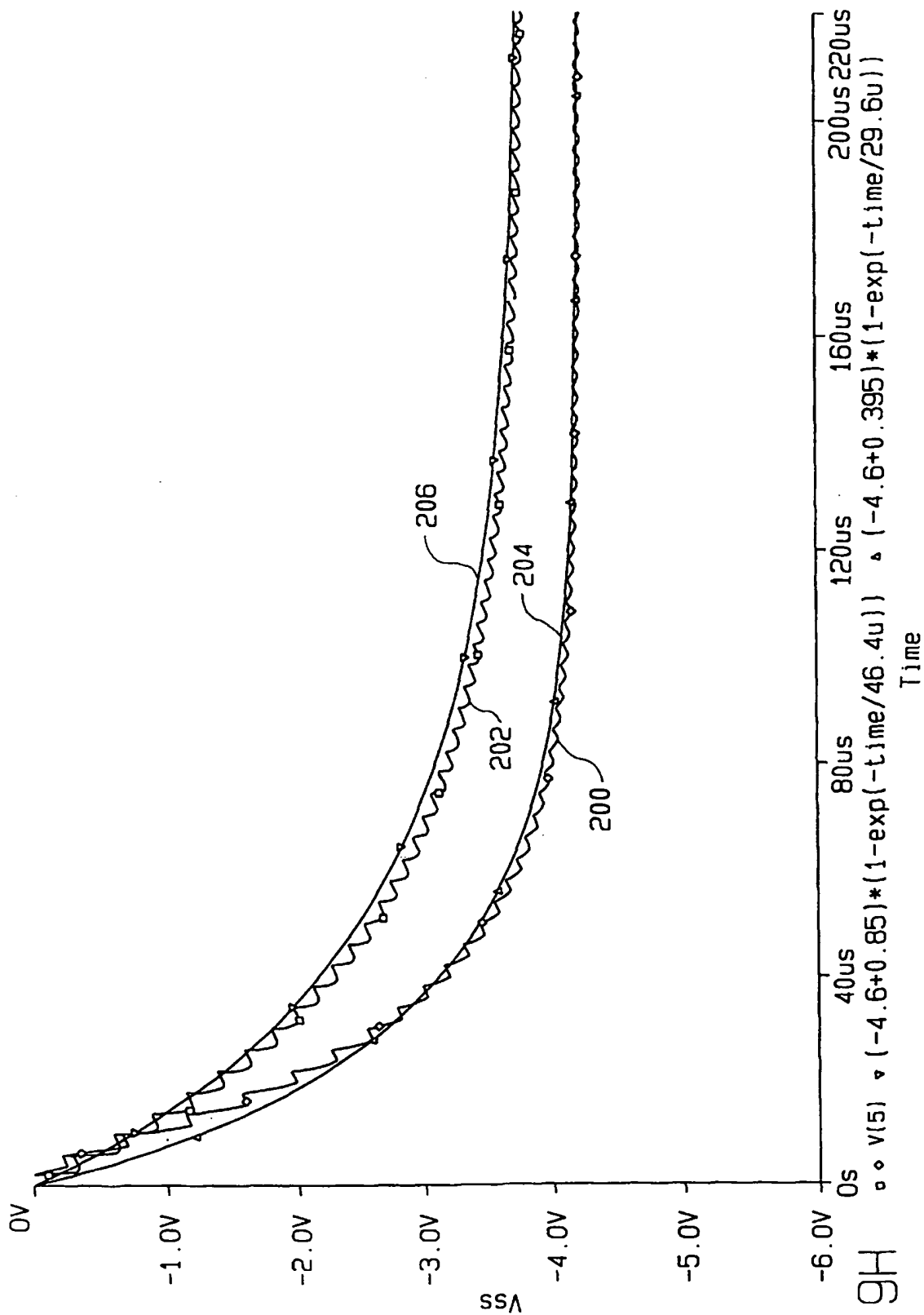


FIG. 9H

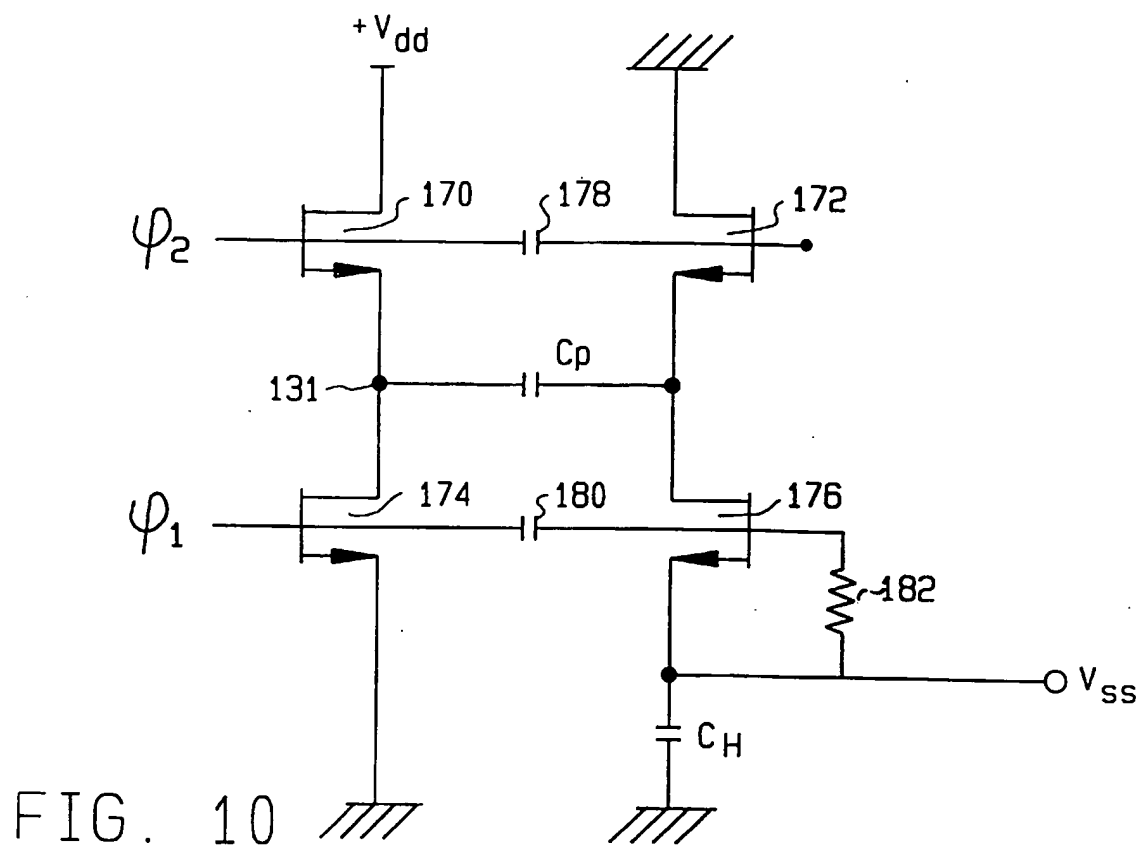


FIG. 10

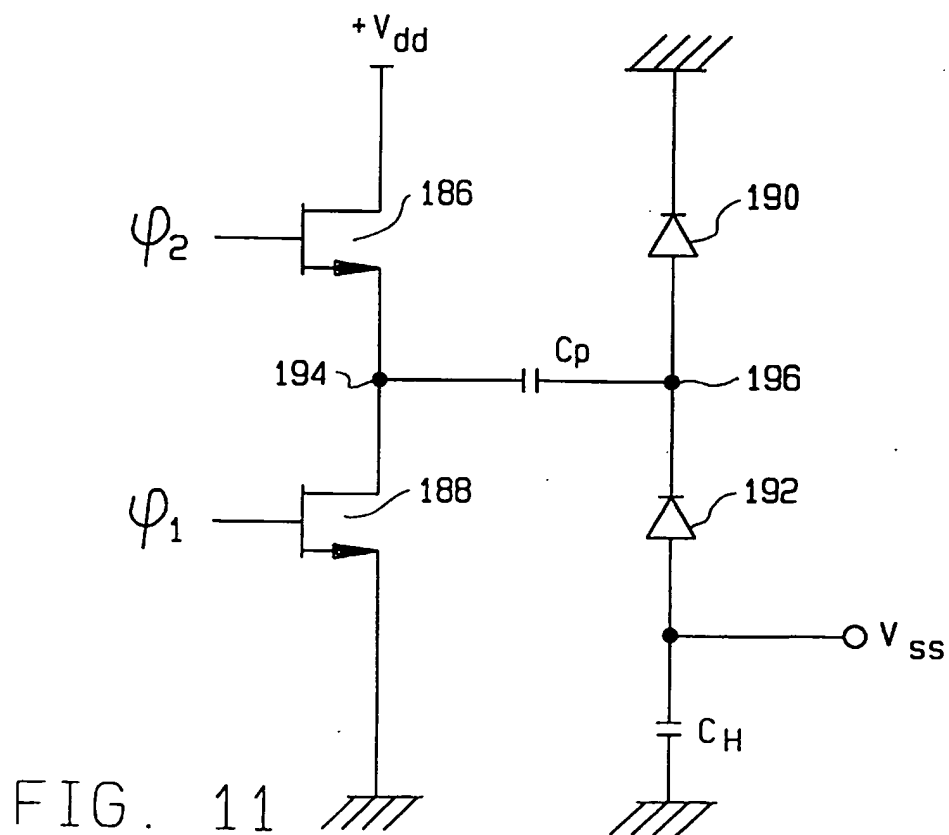


FIG. 11

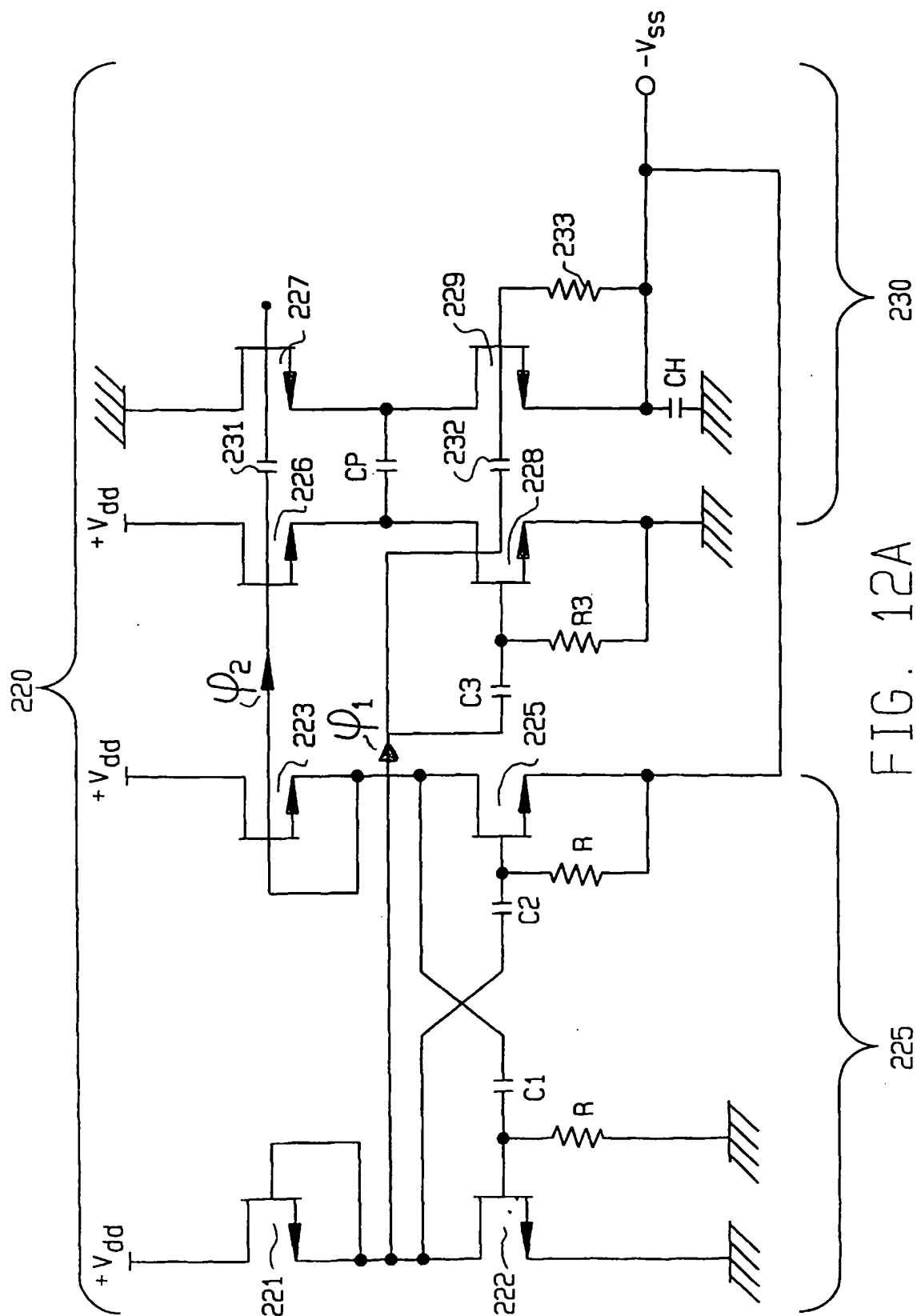


FIG. 12A

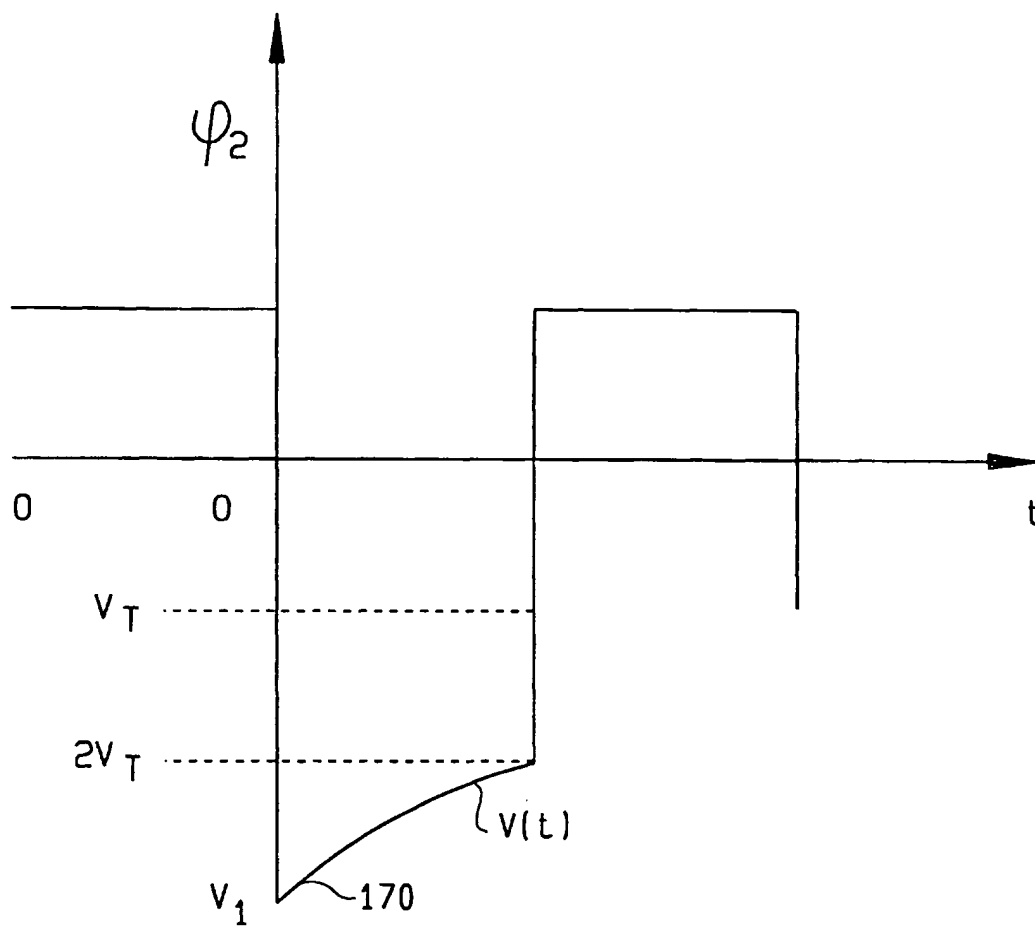


FIG. 12B

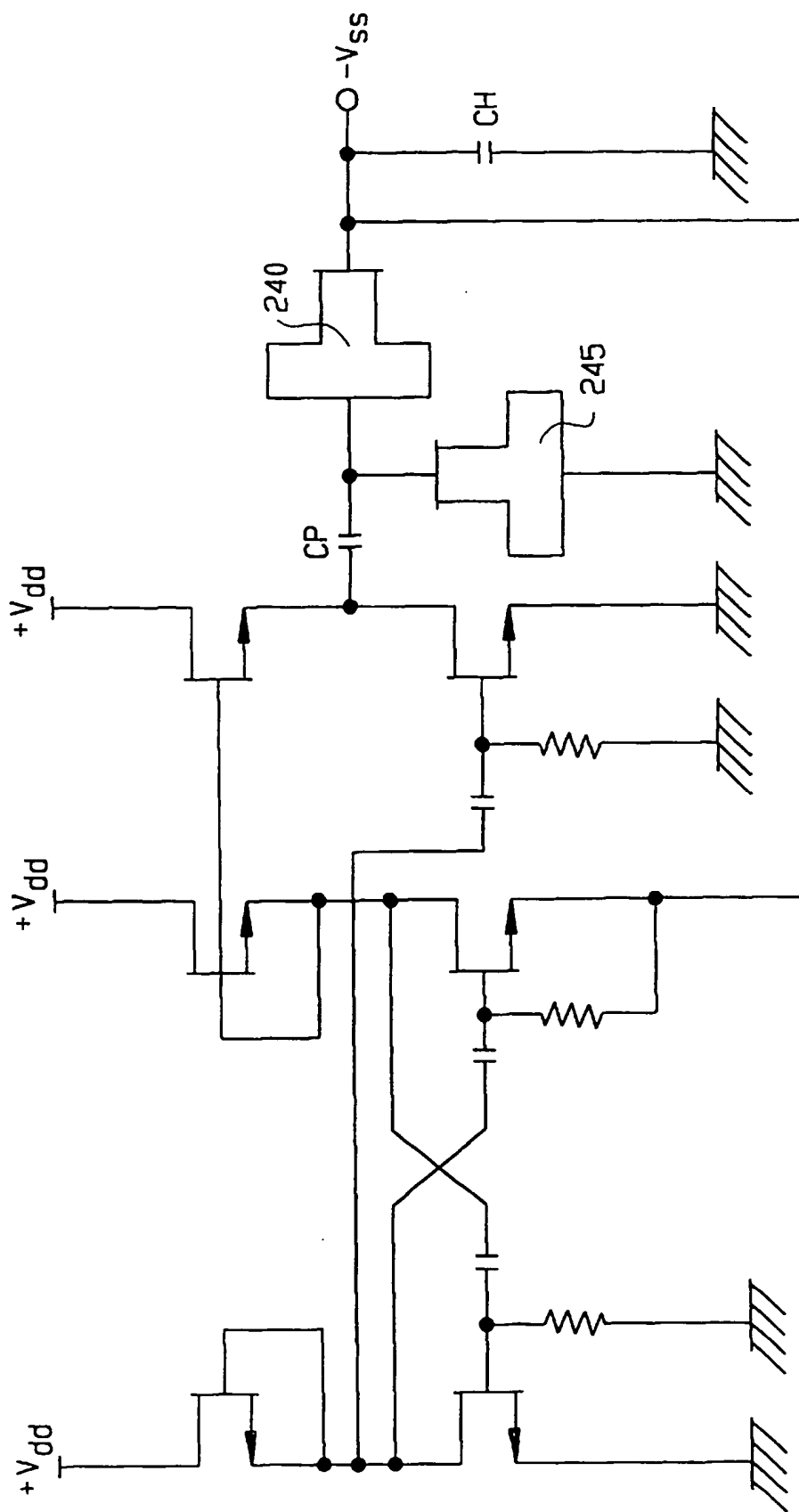


FIG. 13

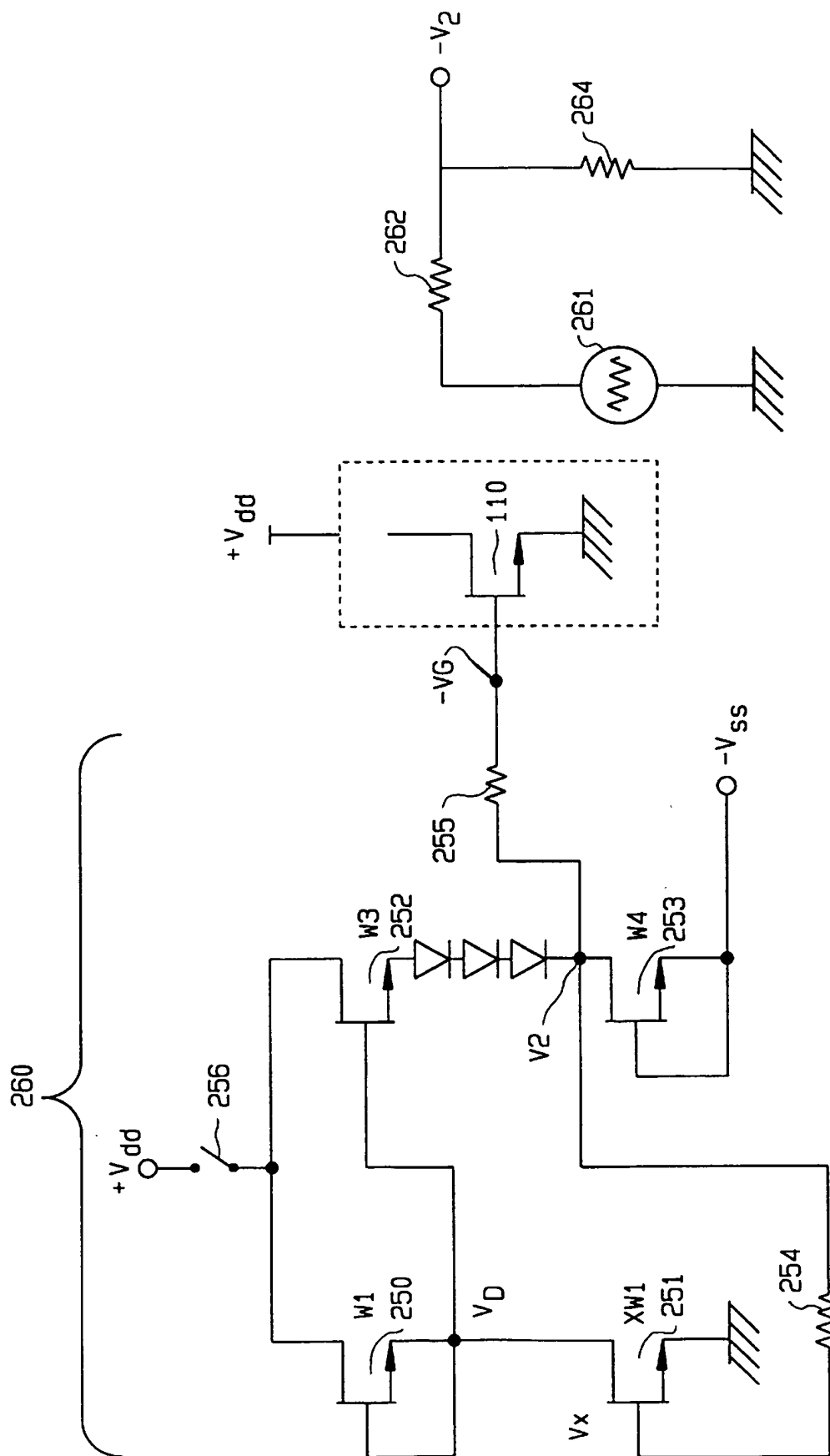


FIG. 15

FIG. 14



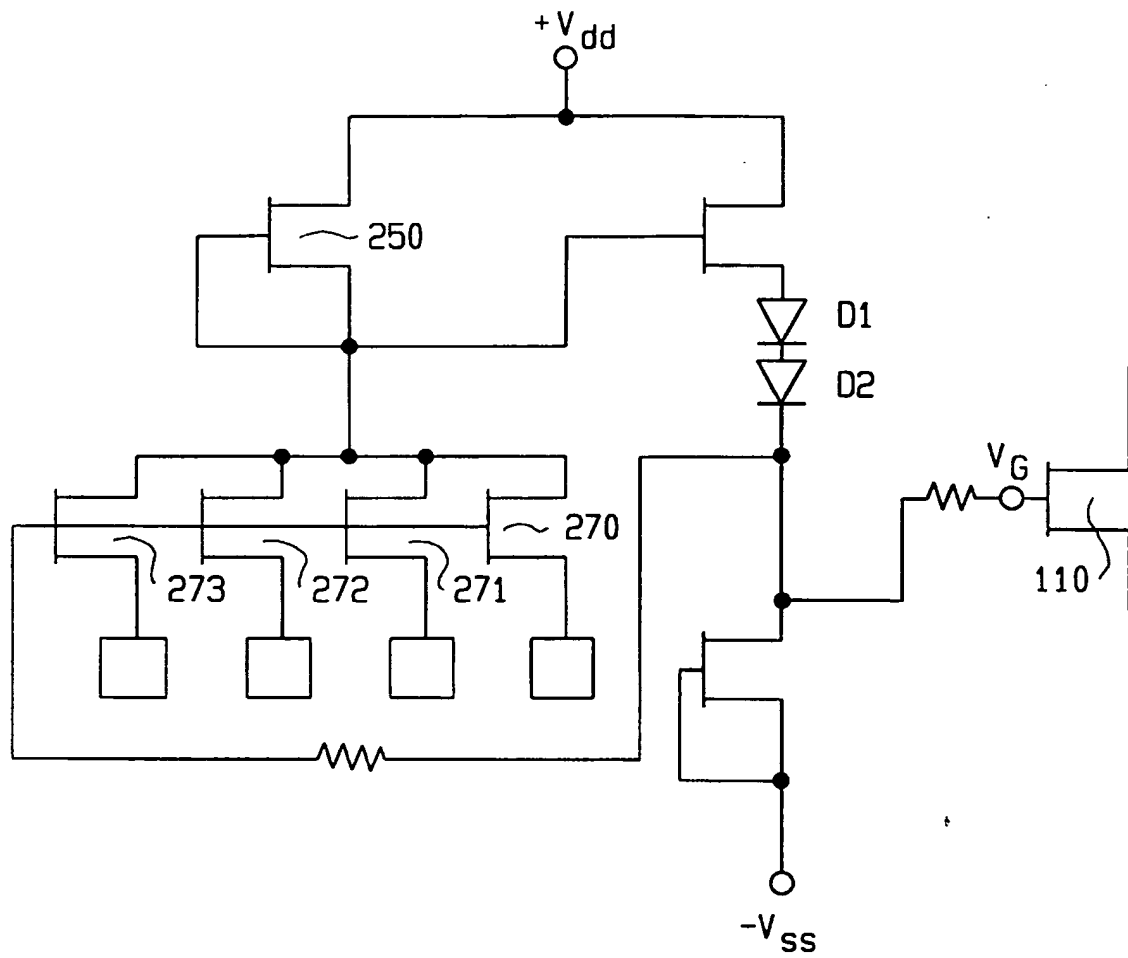


FIG. 16

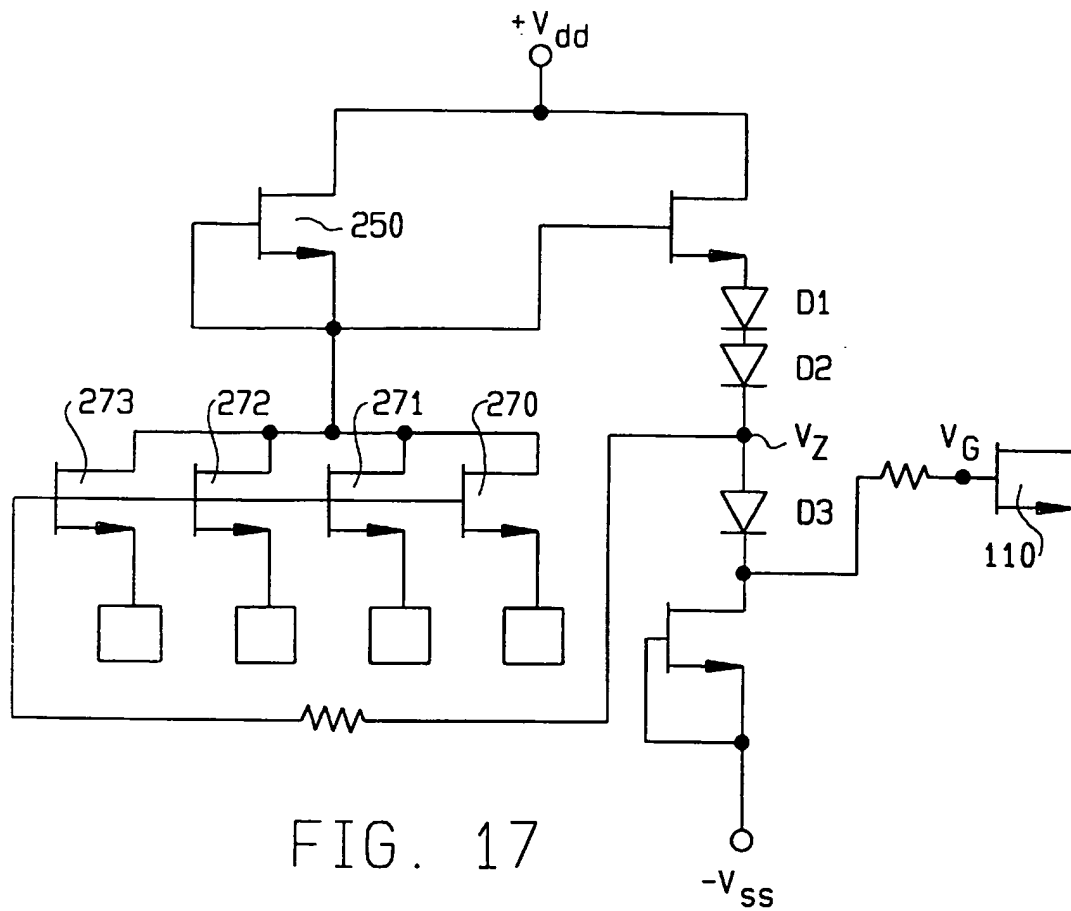


FIG. 17

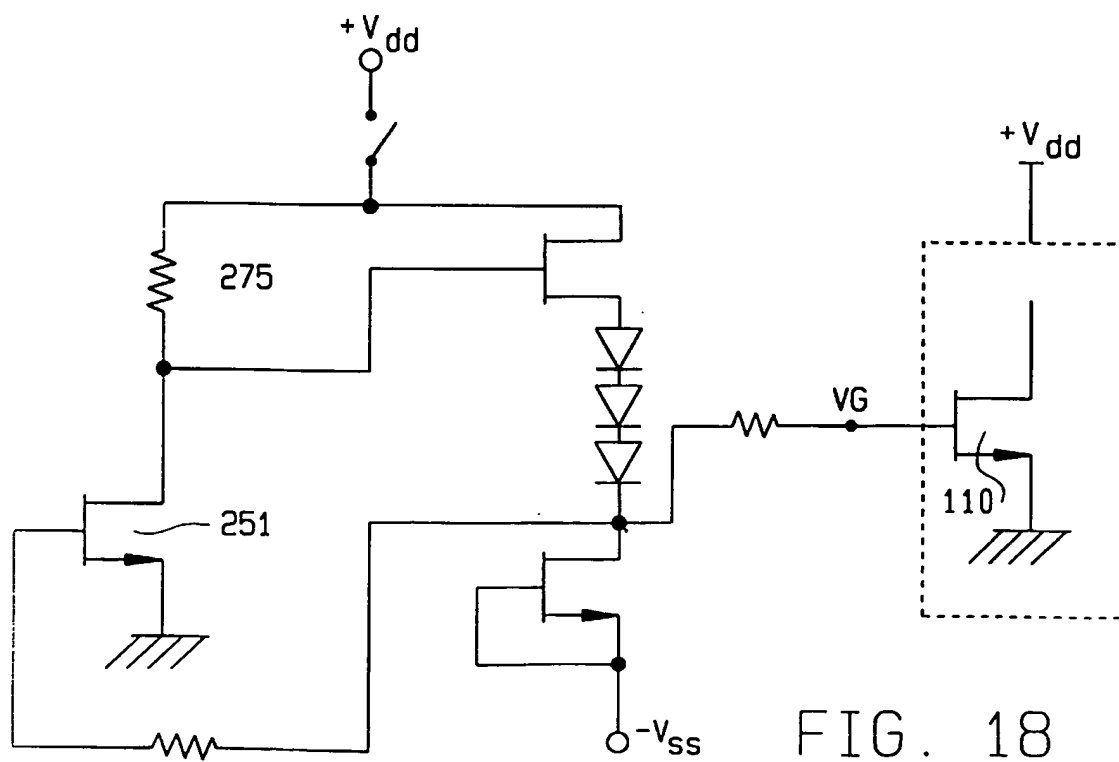


FIG. 18

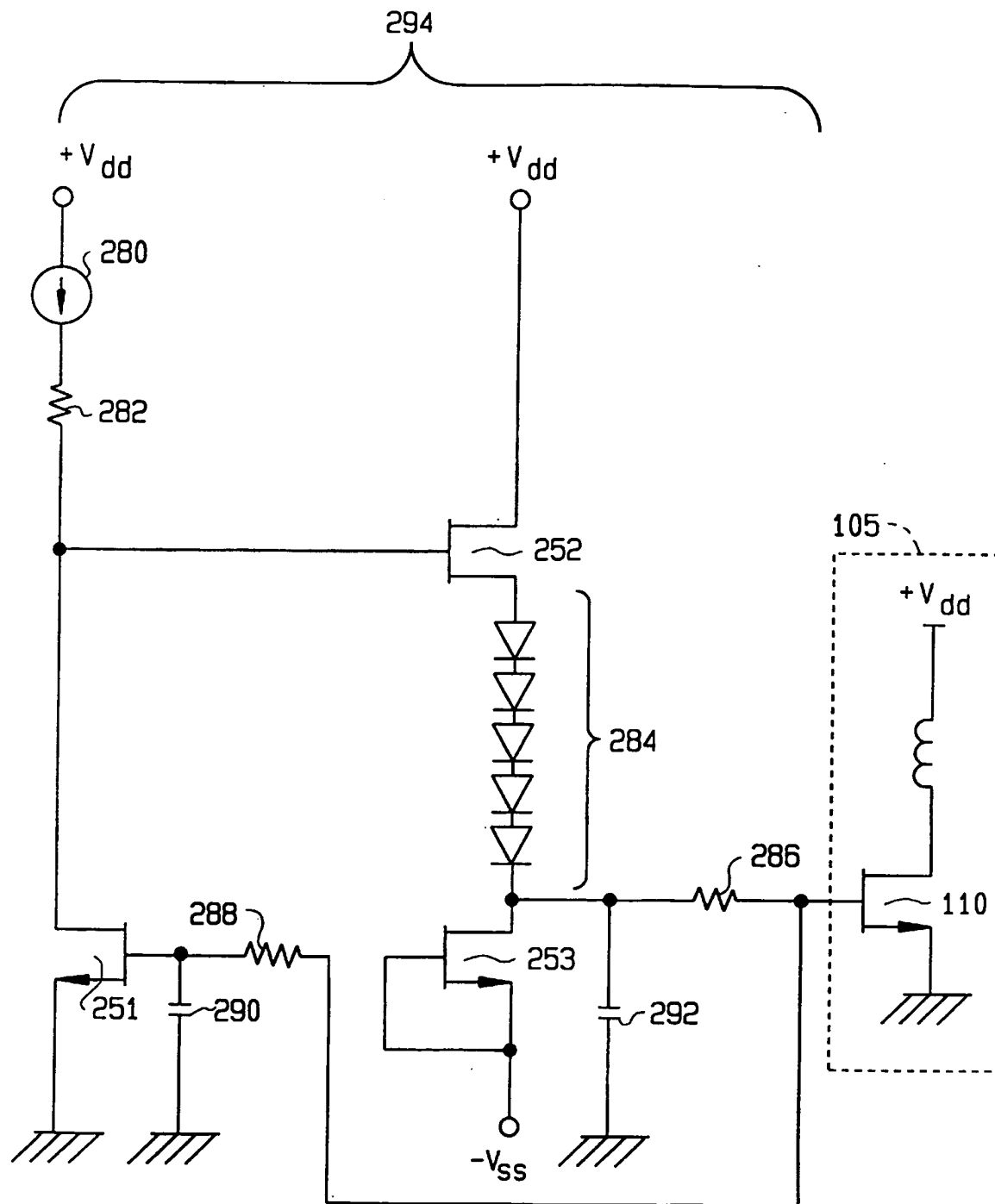


FIG. 19

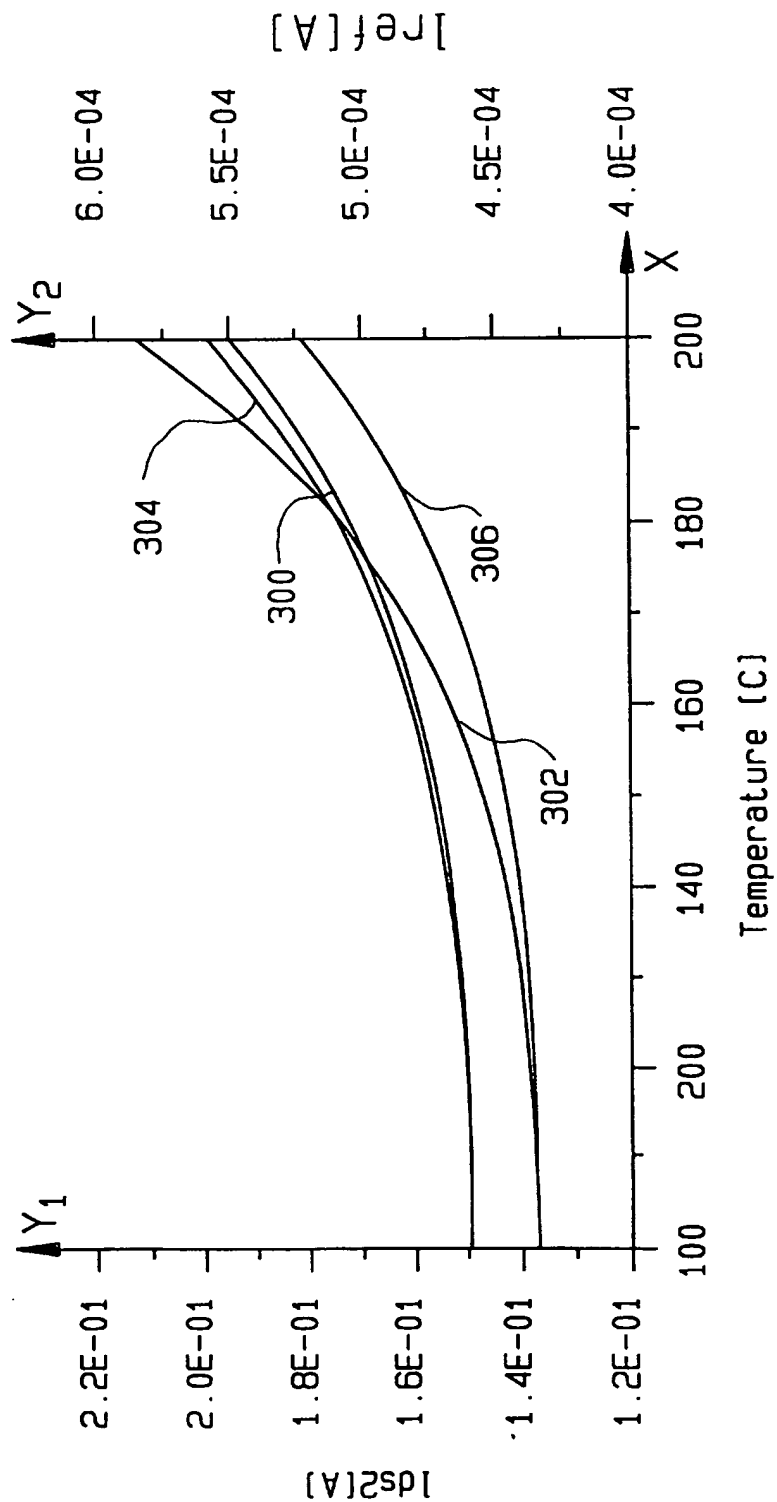


FIG. 20

# AMPLIFIER USING A SINGLE POLARITY POWER SUPPLY AND INCLUDING DEPLETION MODE FET AND NEGATIVE VOLTAGE GENERATOR

## FIELD OF THE INVENTION

The present invention generally relates to the field of amplifiers and more particularly, amplifiers having depletion-mode field effect transistors and operating with a single polarity power supply.

## BACKGROUND OF THE INVENTION

All cellular telephones contain an amplifier for amplifying transmit signal. Because cellular telephones are small in size and preferably contain a single rechargeable battery, the amplifier is preferred to operate with a single polarity power supply. Moreover, it is preferred that the amplifier consumes low power, particularly when the cellular telephones are in a "standby" mode. A cellular telephone is in a "standby mode" when it is able to receive a ring signal indicating an incoming call but cannot send a transmit signal unless it is activated. It is further preferred that the amplifier has high power capability, is durable and can be made at low cost.

Power amplifiers used in cellular phones typically include at least one transistor for signal amplification and a transistor biasing circuit. A known amplifier includes a discrete silicon power transistor such as a silicon bipolar transistor or an enhancement-mode silicon MOSFET, and a transistor biasing circuit which is not monolithically integrated with the power transistor. This amplifier has certain advantages: silicon technology is well understood and well developed; silicon power transistors are readily available; a discrete silicon transistor can be individually optimized for power or efficiency. It however suffers the following drawbacks.

First, as compared with GaAs transistors, silicon transistors are generally slower in speed and have lower power capability. Second, it is difficult to monolithically integrate a silicon power transistor with its biasing circuit, because a silicon integrated circuit ("IC") has large parasitics especially at high frequencies. The large parasitics are caused by the pn junctions used in a silicon ICs for device isolation. In comparison, device isolation in a GaAs IC is typically accomplished by simply forming each device on a mesa on a semi-insulating substrate, which results in lower parasitics.

Further, because of its lower electron mobility and velocity, silicon transistors need to be optimized for power. The optimized transistors generally have structures not compatible for monolithic integration. Consequently, a silicon power transistor used in a power amplifier is normally a discrete device, which results in increased assembly cost and reduced reliability.

GaAs based transistors are more preferable than silicon transistors for use in amplifiers because they provides higher power and are capable of operating at higher frequencies. Moreover, they can be monolithically integrated with a GaAs biasing circuit. Among GaAs field effect transistors ("FETs"), depletion-mode GaAs FETs are most suitable for cellular communications because they provide higher power and operate at higher frequencies than enhancement-mode GaAs FETs.

To bias a depletion-mode GaAs FET at a desired operating point, a negative bias must be applied between the gate and source of the FET. The amplitude of this bias depends on the particular application the amplifier is intended. For a class A amplifier, the FET is biased at one half of its

zero-bias saturation current,  $I_{ds}$ ; the FET conducts current for an entire input cycle and consumes power continuously. For a class AB amplifier, however, the depletion-mode FET is biased at one quarter of  $I_{ds}$  so that the FET is "slightly on" when there is no input signal. For a Class B amplifier, which typically include two depletion-mode FETs arranged in a push-pull fashion such that only one of the FETs is turned on during any half cycle of an input sinusoidal RF signal, the two FETs are biased at pinch-off.

In addition to the negative bias, a depletion FET also requires a positive bias between its drain and source. Thus, a depletion-mode FET requires two biases to operate, a positive bias between the drain and source, and a negative bias between the gate and source. For a typical depletion-mode GaAs MESFET, the positive bias required is about 3 to 12 volts, and the negative bias is about -0.5 to -4 volts. To provide the positive and negative biases, one may use two power supplies, one for the positive bias and the other for the negative bias. It is preferred, however, to use only a single polarity power supply.

There are several known power amplifiers which operate with a single polarity power supply. FIG. 1 depicts a self-biased GaAs amplifier containing a depletion mode GaAs FET 10. The drain of the FET is connected to a positive dc voltage supply,  $+V_{DD}$ , through an inductor 15; the source is connected to ground through a resistor 20; the gate is dc biased to ground through an inductor 25. A capacitor 30 is connected in parallel to resistor 20 for providing an ac path from the source to ground. An input ac signal is provided at the gate of the FET.

In this amplifier, resistor 20 operates to establish a negative bias between the gate and the source. More specifically, because the gate is grounded through inductor 25 and the source is at a positive potential which equals to the voltage on resistor 20, the gate is biased at a potential that is negative with respect to the source. The amplitude of the negative bias approximately equals to the voltage on resistor 20.

This self-biased amplifier is not suitable for cellular communications because, under high power and high frequency conditions, the impedance of inductor 25 and capacitor 30 are no longer negligible. As a result, the amplitude of the negative bias is affected by the input signal. Moreover, the source of the FET is required to directly connect to ground for high frequency operations, a topology not available in this amplifier.

An improved self-biased amplifier is described in U.S. Pat. No. 5,374,899 to Griffiths et al. As depicted in FIG. 2, this amplifier includes, in addition to capacitor 20 and resistor 30, a diode 35 connected in parallel to the resistor. With increased input ac signal, the diode becomes more conductive and consequently, the variation of the source voltage is reduced. Although this circuit appears to have improved power and gain operation over the conventional self-biased amplifier, it remains a disadvantage that the source of the FET is not directly connected to ground.

Referring to FIG. 3, another known amplifier uses a portion of the input ac signal rectified by a rectifier 36 to generate a negative bias. The rectifier consists of a diode 37, a resistor 38 and a pair of capacitors. A major drawback of this amplifier is that in order to generate the negative voltage, it consumes a portion of the input RF signal, thus diminishing the already precious RF source signal. Another problem is that the rectifier generates a relatively stable negative voltage only when the input RF signal is an analog signal. When the input RF signal is digital, the amplitude of the negative voltage varies and it depends on the density of transmit data.

U.S. Pat. No. 5,327,583 to Yamada et al. describes generating a negative bias using a clock signal of a microcomputer. As depicted in FIG. 4, the clock signal is provided from a microprocessor (not shown) to a CMOS inverter and then to a circuit 39 which generates a negative voltage.

We believe this circuit has some significant drawbacks. First, due to process variations in fabricating FETs, the zero-bias saturation current of each FET varies slightly from device to device. As a result, circuit 39 appears to require individually tuning in order to provide a precise negative bias, which requires additional manufacturing steps. Second, this amplifier is not power efficient because one half of the clock signal passes through diode 45 to ground. Further, although circuit 39 includes two capacitors to smooth ripples in the negative bias, we believe that certain amount of ripples still exists which interferes with input ac signal and causes the noise level to increase. It is preferred that the ripples be reduced.

It is therefore an object of the present invention to provide an amplifier having at least one depletion-mode FET and operating with a single polarity power supply;

it is a further object to provide a negative voltage generator within the power amplifier to generate a negative voltage for biasing the FET;

it is still another object to regulate the negative voltage generated by the negative voltage generator to a desired level before providing it to the depletion-mode FET;

it is another object to reduce ripples in the negative voltage generated by the negative voltage generator;

it is still a further object to regulate the negative voltage generated by the negative voltage generator and to make it insensitive to small variation in the negative voltage; and

it is a further object to make the negative voltage regulator power efficient and particularly when the amplifier is in a stand-by mode.

### SUMMARY OF THE INVENTION

Those and other objects are achieved in the present invention which provides a power amplifier operating with a single polarity power supply.

In accordance with the present invention, a amplifier comprises an amplifying stage having at least one depletion-mode FET, and a negative voltage generator providing a negative bias to the FET. The negative voltage generator includes a multivibrator producing two clock signals, and a charge pump which receives the two clock signals and generates a negative voltage. Advantageously, the generated negative voltage is then provided back as a low reference potential to the multivibrator. As a result, the clock signals generated by the multivibrator contain a negative potential period, which enables the charge pump to operate in a power efficient manner.

Preferably, the amplifier further includes a negative voltage regulator which regulates the negative voltage to a value such that it accurately biases the depletion mode FET in the amplifying stage to a desired operating point. No tuning is required to achieve the accurate bias. The negative voltage regulator also operates to smooth the waveform of the negative voltage and to reduce amplitude of ripples present in the negative voltage.

In a preferred embodiment, the multivibrator includes two inverters, each having input and output terminals. A capacitor is coupled between the input terminal of a first inverter to the output terminal of a second inverter. Another capacitor is coupled between the input terminal of the second inverter

and the output terminal of the first inverter. Two resistors, one coupled between the input terminal of the first inverter and ground, and the other between the input terminal of the second inverter and the generated negative voltage, are included. The clock signals generated by the multivibrator are inverting signals.

In a more preferred embodiment, the inverters are realized with FETs. More specifically, the first inverter includes an FET with its source connected to ground, its drain connected to a load and to the output terminal of the first inverter, and its gate connected to the input terminal of the first inverter. The second inverter comprises another FET with its source connected to the negative voltage, its drain connected to another load and to the output terminal of the second inverter, and its gate connected to the input terminal of the second inverter. Preferably, the FETs are all depletion-mode GaAs FETs, and the two loads are also depletion mode FETs.

In accordance with the present invention, the charge pump comprises four electronic switches, a pump capacitor and a hold capacitor. More specifically, first and second electronic switches are connected in series and between the power supply and ground; second, third and the hold capacitor are connected in series and between ground; the hold capacitor is coupled between the intersection of the first and second switches, and intersection of the third and fourth switches.

The clock signals provided to the charge pump includes two phases: a pump phase and a transfer phase. During the pump phase, the first and third electronic switches which are responsive to the second clock signal, are closed, and the second and fourth electronic switches which are responsive to the first clock signal, are open, thereby charging the pump capacitor. During the transfer phase, however, the first and third electronic switches are open and the second and fourth electronic switches are closed, thereby transferring charges from the pump capacitor to the hold capacitor and in the process, producing a negative voltage across the hold capacitor.

To further improve the power efficiency of the charge pump, when coupling the clock signals to the second switch in the charge pump, the first clock signal is slightly delayed with respect to the second clock signal. This slight delay prevents the first and second switches from being simultaneously closed during the initial moment when the clock signals change from the pump phase to transfer phase, thereby preventing a direct current path from the power supply through the first and second switches to ground. As a result, the power efficiency of the charge pump is improved. In a preferred embodiment, the delay is accomplished by an RC network connected between the first output terminal of the multivibrator and the second switch.

In a preferred embodiment of the charge pump, the electronic switches are realized by four FETs: a first FET with its drain coupled to the power supply, its gate connected to receive the second clock signal; a second FET with its drain coupled to the source of the first FET, its gate connected to receive the first clock signal, and its source coupled to ground; a third FET with its drain coupled to ground, a gate coupled to receive the second clock signal; and a fourth FET with its drain connected to a source of the third FET. Coupled between the source of the first and third FETs is a pump capacitor. A hold capacitor is coupled between the source of the fourth FET and ground. Two capacitors, a first coupled between the gates of the first and third FETs and a second coupled between the gates of the second and fourth FETs, couple the clock signals to the third

and fourth FETs. A resistor, coupled between the gate and the source of the fourth FET, bootstraps the FET at the negative voltage which is provided at the source of the fourth FET.

In another preferred embodiment of the charge pump, the switches are realized by two FETs and two diodes: a first FET with its drain coupled to the power supply, its gate connected to receive the second clock signal; a second FET with its drain connected to the source of the first FET, a gate connected to receive the second clock signal, and a source coupled to ground. The cathode of the first diode is coupled to the ground. A second diode has its cathode coupled to the anode of the first diode. The pump capacitor is coupled between the source of the first FET and the anode of the first diode. Coupled between the anode of the second diode and ground is the hold capacitor. The negative voltage is provided across the hold capacitor.

The negative voltage regulator of the present invention utilizes a current mirror. In a preferred embodiment, it comprises a current source and three FETs: a first FET with its drain coupled to the current source and its source connected to ground; a second FET with its drain coupled to the power supply and its gate coupled to the drain of the first FET; a third FET with its drain coupled to the source of the second FET and also to the gate of the first FET. The gate and source of the third FET is connected together and to the negative voltage to be regulated. The regulated negative voltage is provided at the drain of the third FET. The current source can be realized with a resistor or an FET. In a more preferred embodiment, the gate-width of the first FETs is such that the regulator accurately biases the depletion mode FET in the amplifying stage to a desired operating point.

In another preferred embodiment, a negative voltage regulator with improved temperature performance is provided. This regulator is comprised of a current source, and three FETs which are connected as follows: a first FET with its drain coupled to the current source, and its source connected to ground; a second FET with its drain coupled to the power supply, and its gate coupled to the drain of the first FET; a third FET with its drain coupled to the source of the second FET, its gate and source connected together and to the negative voltage to be regulated. The gate of the first FET is resistively coupled to the gate of the depletion mode FET in the amplifying stage. The regulated negative voltage is provided at the drain of the third FET which is resistively coupled to the gate of depletion-mode FET in the amplifying stage.

Advantageously, the coupling between gate of the first FET and the gate of the depletion-mode FET provides a feedback of leakage current at the drain-to-gate junction of the depletion-mode FET. As a result of this feedback, the performance of the regulator under increased temperature is improved.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Those and other objects, features and advantages of the present invention will be more apparent from the following detailed description in conjunction with the appended drawings in which:

FIGS. 1-4 illustrate prior art GaAs amplifiers;

FIG. 5 is a block diagram of an amplifier of the present invention;

FIG. 6 depicts the block diagram of a negative voltage generator of the present invention;

FIG. 7 shows the block diagram of a preferred embodiment of the amplifier;

FIG. 8A is the block diagram of a multivibrator contained in the negative voltage generator;

FIG. 8B is the schematic circuit diagram of the preferred embodiment of the multivibrator;

FIG. 9A depicts a charge pump used in the negative voltage generator;

FIGS. 9B-H illustrates the equivalent circuit and results of simulation of the charge pump during different phase of operation;

FIG. 10 shows the schematic circuit diagram of a preferred charge pump;

FIG. 11 illustrates the schematic circuit diagram of another preferred embodiment of the charge pump;

FIGS. 12A-B show the schematic circuit diagram of a preferred embodiment of the negative voltage generator and a clock signal waveform within the generator, respectively;

FIG. 13 shows the schematic circuit diagram of another preferred embodiment of the negative voltage generator;

FIG. 14 depicts the schematic circuit diagram of a preferred embodiment of the negative voltage regulator of the present invention;

FIG. 15 depicts an output small signal equivalent circuit of the preferred embodiment of the negative voltage regulator;

FIG. 16 is the schematic circuit diagram of another preferred embodiment of the negative voltage regulator;

FIG. 17 is the schematic circuit diagram of an alternative embodiment of the negative voltage regulator shown in FIG. 16;

FIG. 18 is the schematic circuit diagram of an alternative embodiment of the negative voltage regulator shown in FIG. 14;

FIG. 19 is the schematic circuit diagram of yet another preferred embodiment of the negative voltage regulator with a feedback to the circuit mirror; and

FIG. 20 depicts the simulated comparison of temperature effect between the regulators shown in FIG. 14 and FIG. 19.

#### DETAILED DESCRIPTION OF THE INVENTION

The present invention provides an amplifier which includes at least one depletion-mode FET biased by an internally generated negative voltage and which operates with a single polarity power supply.

A "single polarity power supply" is defined herein as a power supply providing only single polarity power. It may include a single power source such as a single battery, and it may include a number of power sources arranged to provide single polarity power. For example, a 12 volt rechargeable battery is a single polarity power supply since it provides a +12 volt power. A power supply including a plurality of batteries arranged to provide +12, +5 and +3 volt power is also a single polarity power supply since it provides only one polarity power. However, a power supply containing two batteries and operating to provide a +5 volt power and a -3 volt power is not a single polarity power supply because the power it provides has two polarities. The amplifier of the present invention requires only a single polarity power supply to operate.

Referring to FIG. 5, an amplifier 100 of the present invention comprises an amplifying stage 105 having a depletion-mode FET 110, and a negative voltage generator 107 providing a negative bias to the FET. FET 110 receives an input ac signal 104 at its gate; the source of the FET is directly connected to ground; the drain is coupled a power supply,  $+V_{dd}$ .

Depicted in more detail in FIG. 6, negative voltage regulator 107 comprises two portions: a multivibrator 115 and a charge pump 120. Multivibrator 115 produces two clock signals,  $\phi 1$  and  $\phi 2$ , preferably one being the inverting signal of the other. Receiving the two clock signals, charge pump 120 generates a negative voltage  $-V_{ss}$  for biasing the FET in the amplifying stage. Advantageously, the negative voltage,  $-V_{ss}$ , generated by the charge pump, is provided back to the multivibrator by means 119 as a low reference potential. Because of this negative low reference potential, the clock signals generated by the charge pump contain a negative voltage period, which allows the charge pump to operate in a power efficient manner.

In a preferred embodiment illustrated in FIG. 7, amplifier 100 further includes a negative voltage regulator 108 which receives the negative voltage  $-V_{ss}$  generated by negative voltage generator 107 and provides a more precise negative voltage for biasing depletion-mode FET 110 to a desired operating point. Such desired operating point includes, for example, for class A operation, one half of  $I_{dss}$  of the depletion mode FET, for class AB operation one quarter of  $I_{dss}$ , or around the pinch-off for class B operation.

In a preferred embodiment, amplifier 100 is a hybrid comprising two monolithic integrated GaAs circuits, one including amplifying stage 105 and negative voltage regulator 108 and the other containing negative voltage generator 115. Forming the amplifier as a hybrid reduces the interference between the input ac signal and the clock signals in the negative voltage generator. If desired, however, the entire amplifier can be made as a monolithic integrated circuit.

It should be noted that, although the amplifying stage as shown includes a single depletion-mode FET, it would be apparent to those of skill in the art that a cascade amplifying stage comprising a plurality of depletion-mode FET can be used in the amplifier, which is within the scope of the present invention.

As it will be detailed later, the amplifier of the present invention operates in a power efficient manner and in particular, consumes little power when in a standby mode. Moreover, the operating point of the FET is accurately set by the negative voltage regulator. Further, the amplifier is small in size and can be made at low cost. Because of those advantages, the amplifier is specially suitable for use in cellular communications.

In this application, unless otherwise specifically provided, a "negative" or "positive" potential or voltage refers to a potential with respect to ground. Thus, a negative voltage or potential is a potential that is more negative than the ground potential, and a positive voltage is a potential more positive than the ground potential. A "positive terminal of a power supply" used hereinafter refers to a terminal of the power supply that provides a positive voltage. A "positive power supply" refers to a power supply so connected that it provides a positive voltage to an amplifier.

A "field effect transistor" ("FET") used herein refers to any transistor that comprises a gate, a source and a drain, and that the current from the drain to source is controlled by the voltage between the gate and the source. It covers, without limitation, FETs based on any material such as silicon, GaAs, InP and it also includes heterojunction FETs based on material such as GaAlAs/GaAs, InGaAs/InP or Si/Ge.

A "GaAs FET" used herein refers to any FET that comprises GaAs material and it includes, without limitation, GaAs MESFETs, GaAs high-electron-mobility-transistors ("HEMTs") or GaAs modulation doped-FET ("MODFETs").

A "depletion-mode FET" used herein refers to any FET, the operating point of which is set by applying a negative voltage between the gate and the source. The term "enhancement-mode FET" used herein refers to any FET, the operating point of which is set by applying a positive voltage between the gate and the source.

The amplifier of the present invention will now be described in detail in terms of the negative voltage generator and the negative voltage regulator.

FIG. 8A is a block diagram of a preferred embodiment of a multivibrator 130. Multivibrator 130 comprises two inverters 132 and 134. The input of inverter 132 is coupled to the output of inverter 134 through a capacitor 136, whereas the input of inverter 134 is coupled to the output of inverter 132 by a capacitor 138. A resistor 140 connects the input of inverter 134 to ground. The input of inverter 134, however, is connected to a negative voltage  $-V_{ss}$  by a resistor 142. This multivibrator provides two inverting clocking signals  $\phi 1$  and  $\phi 2$  at the output terminals of the inverters, the period of which depends on the values of resistors 140 and 142 and capacitors 136 and 138. Advantageously, because of the negative voltage  $-V_{ss}$ , output clock signals  $\phi 1$  and  $\phi 2$  include a negative potential period 144.

FIG. 8B illustrates the schematic circuit diagram of the preferred embodiment of the multivibrator, wherein the two inverters are formed by two pairs of GaAs FETs, 146 and 148, and 150 and 152, respectively. Preferably, all of the GaAs FETs are depletion-mode n-channel GaAs FETs and they have long gate-length to reduce power consumption. For example, the gate-lengths for FETs 146, 148, 150 and 152 are 4 microns, as compared to the gate-length of 0.5 micron for FET 110 in the amplifying stage. Longer gate-length results in lower current and it conserves power. In this multivibrator, FETs 148 and 152 functions as load to FETs 146 and 150 and they may be replaced with resistors.

It is important that the source of FET 150 is connected to the negative potential  $-V_{ss}$ . This negative potential causes the low potential of the clock signals to be negative, which, as detailed below, is critical for turning off depletion mode FETs in the following charge pump to achieve power efficient operation.

The charge pump of the present invention is now described with reference to FIGS. 9A-11.

Referring to FIG. 9A, a charge pump 154 of the present invention includes a first pair of electronic switches 156 and 158 driven by clock signal  $\phi 2$ , and a second pair of electronic switches 160 and 162 driven by clock signal  $\phi 1$ . Coupled between the first pair of switches is a pump capacitor  $C_P$ . A hold capacitor  $C_H$  connects switch 162 to ground.

The charge pump operates as follows: inverting clock signals  $\phi 1$  and  $\phi 2$  contain two phases, a pump phase 164 and a transfer phase 166. During the pump phase, the first pair of switches are closed, connecting the pump capacitor between power supply  $+V_{dd}$  and ground, and the second pair is open. The pump capacitor is thus charged by the power supply.

During the transfer phase, the first pair of switches are open and the second pair are closed. Consequently, a portion of the charge on the pump capacitor  $C_P$  is transferred to the hold capacitor  $C_H$ . Because the voltage across capacitor  $C_P$  cannot be instantly changed, switching from the pump phase to transfer phase produces a negative voltage across the hold capacitor.

The preferred charge pump of the present invention is especially power efficient for two reasons. First, because the



clock signals are inverting, the first and second pairs of switches are not closed at the same time during either the transfer or pump phase and consequently, there is no direct dc current path from the power supply to ground. (As it will be discussed later, at the initial moment of switching from the pump phase to transfer phase, there may be a dc current path from the power supply through switches 156 and 160. This dc path was eliminated by slightly delaying the first clock signal  $\phi_1$  by, for example, an RC network).

Second, when the charge pump is first turned on and begins to operate, during the transfer phase, a portion of the charge on the pump capacitor is transferred to the hold capacitor, and the negative voltage across the hold capacitor will continue to build during the transfer phase until it matches the negative voltage on the pump capacitor. Thereafter no further charge is transferred from the pump capacitor to the hold capacitor. Assuming a subsequent load circuit connected to  $-V_{SS}$  draws little current, after the initial period, no charge is transferred from the pump capacitor to the hold capacitor; the charge pump thus draws little power from the power supply.

The charge pump is analyzed below in terms of its steady state voltage, output impedance, supply current waveforms and settling time, by breaking the operation into a piece-wise linear representation within each of the pump and transfer phase. Within a clock cycle, the duration of the pump phase is  $T_1$  and the transfer phase is  $T_2$ .

#### Pump Phase

FIG. 9B shows an equivalent circuit of the charge pump during the pump phase. The charge stored on the hold capacitor is represented by a step voltage source  $V_H$ . The hold capacitor is continually discharged during the entire pump phase by a dc load  $I_L$ . In the pump phase, the discharge is not replaced so the negative output voltage  $V_{SS}$  is given by:

$$V_{SS}(s) = -\frac{1}{sC_H} \frac{I_L}{s} + \frac{V_H}{s} \quad (1)$$

At the beginning of the pump phase ( $t=0$ ), the negative voltage  $V_{SS}$  is expressed as:

$$V_{SS}(T_1) = -\frac{I_L}{C_H} T_1 + V_{SS}(0) \quad (2)$$

Thus,  $V_{SS}$  displays ripples in its output waveform and the peak-to-peak amplitude of the ripples is  $I_L T_1 / C_H$ . According to equation (2), the amplitude is reduced by increasing the value of hold capacitor  $C_H$  or decreasing the length of the pump phase,  $T_1$ , or combination of both.

While hold capacitor  $C_H$  is discharging, pump capacitor  $C_P$  is charged during this pump phase. Referring to FIG. 9C, the charge stored in pump capacitor  $C_P$  is represented by a voltage source  $V_P$ . Since Switch 158 may be implemented with diodes, a forward voltage drop of  $V_F$  is included as the voltage drop on the diodes. This voltage drop can be set to zero for transistor-based switches (to a first order approximation). A pump current  $I_P(s)$  is given by:

$$I_P(s) = \left( \frac{V_D - V_P - V_F}{R_P} \right) \left( \frac{1}{s + \frac{1}{R_P C_P}} \right) \quad (3)$$

where  $R_P = (R_1 + R_2)$ . In the time domain, the pump current is given by:

$$i_P(t) = \left( \frac{V_D - V_P - V_F}{R_P} \right) e^{-t/R_P C_P} \quad (4)$$

The transient voltage  $V_{CP}$  across the pump capacitor is given by:

$$V_{CP}(s) = (V_D - V_P - V_F) \left[ \frac{1}{s} - \frac{1}{s + \frac{1}{R_P C_P}} \right] \quad (5)$$

Note that  $V_P$  represents the charge stored on the pump capacitor before the pump phase. The resulting voltage across  $C_P$ ,  $V_{PP}$ , at the end of the pump phase ( $t=T_1$  with  $t=0$  at the beginning of the pump phase) is the sum of the initial voltage and the transient voltage:

$$V_{PP}(T_1) = V_{PP}(0) + (V_D - V_{PP}(0) - V_F)(1 - e^{-T_1/R_P C_P}) \quad (6)$$

#### Transfer Phase

FIG. 9D shows an equivalent circuit diagram of the charge pump circuit during the transfer phase, where a forward voltage drop  $V_F$  is included for the case when switch 162 is a diode. This circuit is analyzed below using linear superposition.

First, set all voltages to zero and analyze the effect of the load current. The output voltage  $V_{SS}$  is given by:

$$V_{SS}(s) = Z \frac{I_L}{s} = \frac{I_L}{C_H} \left[ \frac{s + \frac{1}{R_T C_P}}{s + \frac{1}{R_T C_S}} \right] \frac{1}{s^2} \quad (7)$$

where  $R_T = (R_3 + R_4)$  and  $C_S$  is the series combination of the capacitance of  $C_P$  and  $C_H$ . The voltage across the hold capacitor due to the load current alone is then expressed as

$$V_{SS}(t) = \frac{I_L}{C_H} \left[ \frac{C_S}{C_P} + R_T C_S \left( 1 - \frac{C_S}{C_P} \right) \right] (1 - e^{-t/R_T C_S}) \quad (8)$$

where  $t=0$  is the beginning of the transfer phase.

$V_{SS}$  and the impedance of the pump capacitor can be used to calculate a pump current,  $I_P$ , and then find the voltage across the pump capacitor:

$$\text{Voltage Across Pump Capacitor} = \frac{I_L}{R_T C_H C_P} \left[ \frac{1}{s + \frac{1}{R_T C_S}} \right] \frac{1}{s^2} \quad (9)$$

Note that the definition of the pump capacitor voltage leads to a sign change, so in the time domain the voltage due to the load current alone is expressed as

$$V_{PP}(t) = -\frac{I_L}{C_H} \left[ \frac{C_S}{C_P} t - R_T C_S \frac{C_S}{C_P} (1 - e^{-t/R_T C_S}) \right] \quad (10)$$

Next, set the load current to zero and restore all the voltages in the circuit, as shown in FIG. 9E. The voltage across the hold capacitor is given by

$$\text{Voltage Across Hold Capacitor} = \frac{(V_P - V_F + V_H)}{R_T C_H} \left( \frac{1}{s + \frac{1}{R_T C_S}} \right) \frac{1}{s} \quad (11)$$

In steady state, after initial start-up transients have subsided,  $V_{SS}(0) = V_{SS}(T_1 + T_2)$  so that the voltage across the hold capacitor due to the initial voltages alone is expressed as

$$V_{SS}(0) = V_{ss}(T_1) - (V_{PP}(T_1) - V_F + V_{SS}(T_1)) \frac{C_S}{C_H} (1 - e^{-T_2/R_T C_S}) \quad (12)$$

Similarly, for the pump capacitor the voltage due to the initial voltages alone is expressed as

$$V_{PP}(0) = V_{PP}(T_1) - (V_{PP}(T_1) - V_F + V_{SS}(T_1)) \frac{C_S}{C_P} (1 - e^{-T_2/R_T C_S}) \quad (13)$$

Using linear superposition, the total voltage across the hold capacitor at the end of the transfer phase is given by combining equations (8) and (12):

$$V_{SS}(0) = V_{ss}(T_1) - [V_{PP}(T_1) - V_F + V_{SS}(T_1)] \frac{C_S}{C_H} (1 - e^{-T_2/R_T C_S}) + \frac{I_L}{C_H} \left[ \frac{C_S}{C_P} T_2 + R_T C_S \left( 1 - \frac{C_S}{C_P} \right) (1 - e^{-T_2/R_T C_S}) \right] \quad (14)$$

The total voltage across the pump capacitor is obtained by combining Equations (10) and (13):

$$V_{PP}(0) = V_{PP}(T_1) - [V_{PP}(T_1) - V_F + V_{SS}(T_1)] \frac{C_S}{C_P} (1 - e^{-T_2/R_T C_S}) - \frac{I_L}{C_H} \left[ \frac{C_S}{C_P} T_2 - R_T C_S \frac{C_S}{C_P} (1 - e^{-T_2/R_T C_S}) \right] \quad (15)$$

#### Conservation of Charge

In steady state, the total charge supplied during a clock cycle to the load must equal the charge obtained from the power supply during the pump phase:

$$Q_{Pump} = Q_{Load} \quad (16)$$

$$\int_0^{T_1} i_P(t) dt = I_L(T_1 - T_2)$$

Using Equation (4), the steady pump capacitor voltage at the beginning of a clock cycle is then:

$$V_{PP}(0) = V_D - V_F - \frac{I_L(T_1 + T_2)}{C_P(1 - e^{-T_1/R_P C_P})} \quad (17)$$

The supply current is then given by:

$$i_P(t) = \frac{I_L(T_1 + T_2)}{R_P C_P(1 - e^{-T_1/R_P C_P})} e^{-t/R_P C_P} = I_0 e^{-t/R_P C_P} \quad (18)$$

as shown in FIG. 9F.

#### Output Voltage and Impedance

The steady state voltages at the beginning and end of the pump phase are given by Equations (2), (6), (14) and (17). These may be solved for  $V_{SS}(0)$  to obtain the steady state output voltage. Substituting Equations (2), (6) and (17) into Equation (14), the following equation is obtained:

$$V_{SS} = 2V_F - V_D + I_L R_{SS} \quad (19)$$

Where  $R_{SS}$  is the derivative of  $V_{SS}$  with respect to  $I_L$ .

The dc behavior of the charge pump is represented as a voltage source in series with an output resistor  $R_{SS}$  as shown in FIG. 9G. The value of  $R_{SS}$  is given by:

$$R_{SS} = R_T \left( 1 - \frac{C_S}{C_P} \right) + \quad (20)$$

$$\frac{T_1 + T_2}{C_P} \left[ \frac{1}{(e^{T_1/R_P C_P} - 1)} + \frac{1}{(1 - e^{-T_2/R_T C_S})} \right] + \frac{T_1}{C_H} \left[ \frac{1}{(e^{T_2/R_T C_S} - 1)} \right] + \frac{T_1}{2C_H}$$

#### Settling Time

An important consideration is how fast the charge pump reaches a steady state voltage when it is first turned on. The above equations can be written in matrix form to give a transition matrix A that relates the voltages at the start of cycle to the voltages at the beginning of the next cycle. This matrix can be applied m times to give the voltages at  $t=MT$ , where  $T=T_1+T_2$ :

$$x_m = \begin{bmatrix} V_{ss}(mT) \\ V_{PP}(mT) \\ 1 \end{bmatrix} = A^m x_0 \quad (21)$$

The transient behavior of  $V_{SS}$  is almost exponential. While it is difficult to solve for a "best fit", a good estimate of the behavior is given by:

$$V_{SS}(t) = (-V_D + 2V_F + I_L R_{SS})(1 - e^{-t/R_{SS} C_H(1 + \frac{C_S}{C_H})}) \quad (22)$$

The time constant is given by  $T_{ON} = R_{SS} C_H (1 + C_S/C_H)$ . FIG. 9H shows the comparison between the result of a PSICE simulation (curve 200 for charge pump capacitor of 100 nano-farads and curve 202 for charge pump capacitor of 10 nano-farads) and the ones obtained with Equation (22) (curves 204 and 206 for charge pump capacitor of 100 nano-farads and curve 202 for charge pump capacitor of 10 nano-farads, respectively). The y-axis of the plot is the negative voltage  $V_{ss}$  as a function of time t, and the x-axis is the time. FIG. 9H shows that Equation (22) fairly accurately calculates  $V_{ss}$ .

Based on the above analysis, the sensitivity of some important charge pump parameters such as switch resistance and the capacitance of the pump and hold capacitors are summarized below:

Parameter	Decrease Value	Increase Value
switch resistance	*lower output impedance *greater device size *lower $T_{ON}$	*higher output impedance *smaller device size *higher $T_{ON}$
pump capacitor	*higher output impedance *smaller physical size *higher $T_{ON}$	*lower output impedance *larger physical size *lower $T_{ON}$
hold capacitor	*higher output impedance *smaller physical size *higher output ripple *lower $T_{ON}$	*lower output impedance *larger physical size *lower output ripple *higher $T_{ON}$

The above analysis sets forth the basic design principles for charge pump circuit.

In a preferred embodiment, the schematic circuit diagram of which is shown in FIG. 10, the charge pump comprises four depletion-mode GaAs FETs 170, 172, 174 and 176. The gates of FETs 170 and 172 are connected by a capacitor 178. The gates of FETs 174 and 176 are coupled by a capacitor 180. To ensure FET 176 be turned off during the pump phase, its gate is bootstrapped to the negative voltage  $-V_{ss}$  by a resistors 182.

This preferred charge pump operates as follows: at the beginning of the pump phase, the potential at the drain of FET 174, which is connected to the source of FET 130, is

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close to the ground potential. The positive pulse in the clock signal  $\phi_2$  applied to FET 170 and the negative pulse in clock signal  $\phi_1$  applied to FET 174 turn on FET 170 and turn off FET 174. Preferably, the positive and negative pulses are such that FET 170 remains turned on and FET 174 remains turned off during the entire pump phase.

Still at the beginning of the pump phase, the potential at the source of FET 172, which is connected to the drain of FET 176, is close to a steady state negative potential  $-V_{ss}$  generated by the charge pump. The positive pulse of clock signal  $\phi_2$  applied to the gate of FET 172 through capacitor 178 turns on FET 172. Preferably, positive pulse of clock signal  $\phi_2$  keeps FET 172 turned on during the entire pump phase.

Also at the beginning of the pump phase, the negative pulse of  $\phi_1$  applied to FET 176 through capacitor 180 turns off the FET. Preferably, with a properly designed negative pulse, FET 176 remains turned off during the entire pump phase. Thus, during the pump phase, the charge capacitor is charged.

Conversely, during the transfer phase, FETs 170 and 172 are turned off and FETs 174 and 176 are turned on, and a portion of the charge stored on the charge capacitor is transferred to the hold capacitor.

In another preferred embodiment, the schematic of which is illustrated in FIG. 11, a charge pump comprises two depletion mode GaAs FETs 186 and 188 connected in series and between power supply  $+V_{dd}$  and ground, and two diodes 190 and 192. A hold capacitor  $C_H$  is connected between ground and diode 192. A charge capacitor  $C_P$  is connected between the FETs 186 and the diodes.

This charge pump operates as follows: during the pump phase, a positive pulse in clock signal  $\phi_2$  applies to FET 186 and turns it on. Meanwhile, FET 188 is turned off by a negative pulse in clock signal  $\phi_1$ . Consequently, charge capacitor  $C_P$  is charged through the loop including the power supply  $+V_{dd}$ , FET 186, diode 190 and ground. During this time, diode 192 does not conduct current because it is reverse biased.

During the transfer phase, FET 186 is turned off by clock signal  $\phi_2$  and FET 188 is turned on by clock signal  $\phi_1$ , thus connecting one end 194 of the charge capacitor to the ground and forcing the voltage at the other end 196 to become negative. Diode 192 therefor becomes forward biased and conducting. As a result, a negative voltage is provided at the junction between diode 192 and the hold capacitor  $C_H$ . Diode 190 is turned off because it is reverse biased.

It will be apparent to those of skill in the art that, although the described preferred embodiments comprises depletion mode GaAs FETs for they provide higher current than enhancement-mode FETs, other types of FETs including enhancement mode FETs or silicon FETs may also be used in the charge pump, which are all within the scope of the present invention.

FIG. 12A illustrates the schematic circuit diagram of a preferred embodiment of the negative voltage generator of the present invention. In the circuit diagram,  $+V_{dd}$  is a positive terminal of a power supply;  $-V_{ss}$  indicates a circuit terminal where an output negative voltage  $-V_{ss}$  is provided. Preferably, all of the components except pump capacitor  $C_P$  and hold capacitor  $C_H$  are monolithically integrated on a GaAs substrate. Because the pump capacitor  $C_P$  and hold capacitor  $C_H$  are generally large in size, they are off-chip components externally connected to the integrated circuit.

As shown, a negative voltage generator 220 comprises a multivibrator 225 generating inverting clock signals  $\phi_1$  and

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$\phi_2$ , and a charge pump 230 which receives the clock signals and generates a negative voltages,  $-V_{ss}$ . An RC network including a capacitor  $C_3$  and a resistor  $R_3$  couples clock signal  $\phi_1$  to FET 228 of the charge pump.

Multivibrator 225 includes four depletion-mode GaAs MESFETs, two capacitors  $C_1$  and  $C_2$ , and two resistors  $R$ . The period of the clock signals depends on the capacitance of capacitors  $C_1$  and  $C_2$  and the resistance of resistors  $R$ , and it is about  $2Rx(C_1+C_2)$ .

The charge pump has been described in detail previously in this application. Importantly, the negative voltage  $-V_{ss}$  generated at the output of the charge pump is provided back to the multivibrator and more specifically, to the source of FET 225 in the multivibrator to ensure the lower potential of the clock signals is negative. The negative period in the clock signal ensures the FETs in the charge pump are properly turned off when required.

When coupling clock signal  $\phi_1$  to FET 228 of the charge pump, the RC network of  $C_3$  and  $R_3$  introduces a slight delay in the clock signal for turning on FET 228 during the initial moment of the transfer phase such that FETs 228 is turned on only after FETs 226 is turned off. As a result, there is no dc current path from  $+V_{dd}$  to the ground through FETs 226 and 228 when the charge pump switches from the pump phase to the transfer phase. Although in this preferred embodiment the RC network is used to provide such delay, it should be apparent to one of skill in the art that other components may be used to create the delay.

More specifically, for clock signal  $\phi_1$ , because the source of FET 228 is connected to ground, the source-gate junction of FET 228 clamps clock signal  $\phi_1$  so that it swings between approximately 0.7 volt to a negative peak value  $V_1$  approximately equal to  $-(V_{dd}-0.5)$  volts. In a preferred embodiment,  $V_{dd}$  is 6 volts, and the negative peak  $V_1$  is about  $-5.5$  volts.

FIG. 12B illustrates the waveform of clock signal  $\phi_1$ . During the pump phase, the amplitude  $V(t)$  of clock signal  $\phi_1$  is given as

$$V(t) = V_1 \exp(-t/(R_3 C_3)).$$

Based on this,  $t$  is expressed as

$$t = R_3 C_3 \ln(V_1/V(t))$$

In order to keep FET 228 turned completely off during the entire pump phase, the gate-to-source voltage of FET 228 should be at least less than twice of the threshold hold of the FET  $V_T$  at the end of the pump phase. Under this condition, the time at the end of the pump phase,  $t_0$ , is given as

$$t_0 = R_3 C_3 \ln(V_1/2V_T)$$

To keep FET 228 turned off during the pump phase,  $t_0$  must satisfy the condition

$$t_0 > T/2 = R(C_1 + C_2)/2.$$

Consequently, the following condition is derived

$$C_3 > (C_1 + C_2) / (2 \ln(V_1/2V_T)).$$

This is the requirement for capacitor  $C_3$  to keep FET 228 turned off during the entire pump phase.

The threshold voltage,  $V_T$ , for FET 228 is generally the same for all the other FETs in the negative voltage generator. For cable TV applications which generally requires less power than for cellular applications, the threshold voltage of the FETs is lower than that for power amplifiers used in cellular phones. Their comparison as well as their effect on the value of  $2 \ln(V_1/2V_T)$  is listed below

Application	$V_T$ (V)	$2\ln(V_1/2V_T)$
Cable TV Set-top	-0.5	3.41
Power Amplifier	-1.4	1.35

During the pump phase, FET 228 is turned off by a negative pulse of clock signal  $\phi_1$ , which also propagates to the gate of FET 229 through a capacitor 232. Because the gate of FET 229 is bootstrapped to the negative voltage,  $-V_{ss}$ , the gate voltage becomes more negative than  $-V_{ss}$ , and FET 229 is turned off. During this phase, FET 226 is turned on by the positive voltage pulse in clock signal  $\phi_1$ , which also turns on FET 227 through a capacitor 150.

During the transfer phase, FETs 228 and 229 are turned on by the positive pulse of clock signal  $\phi_2$ . FETs 226 and 227, however, are turned off by the negative voltage pulse of clock signal  $\phi_1$ . In this way, the charge pump circuit operates in a power efficient fashion.

FIG. 13 depicts another preferred embodiment of the negative voltage generator wherein two diodes are used in the charge pump. In particular, diodes 240 and 245 are GaAs Schottky diodes formed by connecting the drain and the source of a GaAs FET together as the cathode and by using the gate of the FET as the anode. Preferably, except the pump and hold capacitors, this negative voltage generator is formed as a GaAs MMIC. The multivibrator and the charge pump have been described with reference to FIG. 8B and FIG. 11 and therefore will not be described in detail here.

In a preferred embodiment, the negative voltage generated by the negative voltage generator is not directly used to bias the depletion mode FET in the amplifying stage because (1) the negative voltage contains ripples, and (2) the negative voltage is not precise enough to accurately bias the FET at a desired operation point. It is preferred to reduce the ripple effect of the negative voltage and to accurately regulate the negative voltage to a desired value.

FIG. 14 depicts the schematic circuit diagram of a preferred embodiment of a GaAs negative voltage regulator 260 in accordance with the present invention. The regulator utilizes a current mirror and it operates to reduce the ripples and provides a more accurate bias. More specifically, negative voltage regulator 260 includes an FET 250 as a current source, and FETs 251, 252 and 253. The negative voltage to be regulated,  $-V_{ss}$ , is applied to the source of FET 253, whereas the regulated negative voltage,  $-V_G$ , is provided at the drain of the same FET. Preferably, regulator 260 is monolithically integrated with the amplifying stage. The regulator further includes an on/off switch 250 which is closed when the amplifier is in operation, and opens when the amplifier is in a standby mode.

The dimensions of FETs 250 and 251 are determined as follows: FETs 250 and 251 are made to have the same gate-length and the same pinch-off characteristics that FET 110 has, preferably by making them on the same semiconductor wafer with the same manufacturing steps. The gate-width of FET 251, however, is a predetermined factor X, determined on the basis of the desired operating point, times the gate width of FET 250.

Factor X equals to the zero-bias saturation current of FET 110 divided by the intended operating current of the FET.

For example, to bias FET 110 at one half of its zero-bias current  $I_{dss}$  for class A operation, factor X is 2. For class AB operation where FET 110 is biased at one quarter of the zero-bias current  $I_{dss}$ , the factor X is 4.

The negative voltage regulator operates as follows: because FETs 250 and 251 are connected in series, their currents must be equal. As a result, the gate voltage  $V_X$  of FET 251 must be such that it biases the FET to provide a current equal to that of FET 250. For example, if factor X is 1, which means FET 251 has the same gate-width that FET 250 has, the gate voltage  $V_X$  of FET 251 must be zero, since the gate-to-source voltage of FET 250 is zero. If factor X is 2, in order to maintain the same current in FETs 250 and 251, the voltage at the drain of FET 251,  $V_D$ , will be pulled toward the ground potential, which also causes the voltage at FET 253's drain  $V_Z$  to decrease.  $V_D$  and  $V_Z$  will continue to decrease until the current through FETs 250 and 251 are equal. The voltage  $V_X$  will be the gate voltage needed to bias an FET 110 at one half of its zero-bias saturation current  $I_{dss}$ .

If factor X is 4, FET 110 is biased to provide one quarter of its zero-bias current  $I_{dss}$ . Accordingly, by choosing the appropriate gate-width ratio between FETs 251 and 250, i.e., factor X, FET 110 is biased at desired operating point. For example, by making the gate width of FET 251 ten times as wide as that of FET 250, i.e. factor X be 10, FET 110 will be biased at one-tenth of its  $I_{dss}$ .

In addition to provide a desired gate bias voltage for FET 110, the negative voltage regulator also reduces ripples in the waveform of the negative voltage  $V_{ss}$ . Referring to FIG. 15, which shows a small signal equivalent circuit of an output portion of the regulator, the ripples in negative voltage  $-V_{ss}$  are represented by an ac voltage source 261. Voltage source 261 is applied to a voltage-dividing network consisting of resistors 262 representing the small-signal drain-to-source resistance ( $r_{ds}$ ) of FET 253, and resistor 264 representing an output small signal resistance  $R_{out}$  of the circuit including FETs 250, 251 and 252. Due to this voltage-dividing network, the amplitude of the ripples at the drain of FET 253 is reduced by a factor of

$$R_{out}/(R_{out}+r_{ds})=1/(1+r_{ds}/R_{out})$$

The output resistance  $R_{out}$  is evaluated as follows: referring to FIG. 15, if voltage  $V_Z$  varies, such variation will be amplified by the gain of an inverting gain stage formed by FETs 250 and 251. Consequently,  $R_{out}$  is given as

$$R_{out}=R_{out}(W3)/(1+A)$$

where  $R_{out}(W3)$  is the output resistance of FET 252 and A is the dc gain of the gain stage.  $R_{out}(W3)$  is given as

$$R=1/(g_m W_3)$$

where  $g_m$  is the transconductance and  $W_3$  is the gate-width of FET 252. If the gate width of FET 252 is about 80 microns and the FET is biased at one quarter of its  $I_{dss}$ , its output resistance  $R_{out}(W3)$  is approximately 200 ohms. Considering the dc gain of the gain stage is approximately 60, the output resistance  $R_{out}$  is thus approximately 4 ohms.

Considering the value of  $r_{ds}$  is approximately around 10,000 ohms, the output amplitude of ripples will be reduced by as high as 60 dB. In this way, the negative voltage regulator reduces the ripples presented in the negative voltage generated by the negative voltage generator.

Another advantage of the regulator is that it consumes little power when in the standby mode. Referring to FIG. 14,

when the regulator is in the standby mode, switch 256 opens and as a result, the regulator does not draw any power from the positive power supply  $+V_{dd}$ . In addition, the only conducting FET in the regulator is FET 253 which provides the full and unregulated negative voltage  $-V_{ss}$  to the gate of FET 110 to turn it off. Since the gate leakage current of an FET is quite small, FET 110 thus draws little current from the negative voltage through FET 253. Consequently, the regulator consumes little power when in the standby mode.

In another preferred embodiment illustrated in FIG. 16, a negative voltage regulator can selectively bias FET 110 at, for example, 1,  $\frac{1}{2}$ ,  $\frac{1}{4}$  or  $\frac{1}{8}$  of the zero-bias current  $I_{dss}$ . This is achieved by making FETs 270, 271, 272 and 273 to have gate-widths that are 1, 2, 4 and 8 times, respectively, of the gate-width of FET 250. The source terminals of FETs 270–273 are connected to respective bonding pads, which are selectively connected to ground for activating a particular FET to obtain the desired bias. For example, to bias FET 110 at an half of  $I_{dss}$ , the bonding pad connected to FET 271 is connected to ground. In this way, by connecting appropriate bonding pad to ground, the regulator can provide a bias that is one of a number of designed biasing voltage.

In another preferred embodiment shown in FIG. 17, a diode D3 is used to further lower bias voltage  $V_z$  by a diode voltage drop to set  $V_G$  below the pinchoff voltage of FET 110 for class C operation.

In another preferred embodiment shown in FIG. 18, a resistor 275 is used to replace FET 250 as a current source. The value of the resistor and the gate-width of FET 251 are such that a desired bias is provided to FET 110.

In yet another preferred embodiment illustrated in FIG. 19, a negative voltage regulator 294 comprises a current source 280 and depletion-mode GaAs FETs 251, 252 and 253. The current source is coupled to the drain of FET 251 through a resistor 282. FET 252 has a drain coupled to a positive terminal of a power supply  $+V_{dd}$ , a gate coupled to the drain of FET 251, and a source coupled to the drain of FET 253 through a series of diodes 284. The gate and source of FET 253 is connected together. The drain of FET 253 is connected to the gate of FET 110 through a resistor 286. Advantageously, the gate of FET 251 is connected to the gate of FET 110 through resistor 288. Two by-pass capacitors 290 and 292, one connected between the gate of FET 251 and the ground and the other between the gate of FET 253 and the ground are used to filter the ac signal to be amplified by FET 110.

As compared to the regulator shown in FIG. 15, this negative voltage regulator displays better temperature performance. More specifically, for the regulator shown in FIG. 15, because the current leakage through drain-gate diode of FET 110 increases with temperature, the drain current as well as the gate current of FET 110 increases with temperature. In this regulator, the gate of FET 251 is connected to the gate of FET 110 through a resistor 288 which provides feedback, which results in a reduced drain current for FET 110 and better tracking between the drain currents of FETs 110 and 251 when the temperature increases.

FIG. 20 illustrates the comparison between drain currents of FET 110 and 251 for the regulator shown in FIG. 19, and those for the regulator shown in FIG. 15. The currents are computer-simulated. In this drawing, axis  $Y_1$  and axis  $Y_2$  indicate the drain current in amperes of FET 110 and FET 251, respectively, and the x-axis indicates the temperature in centigrade. The dimensions for the FETs used in the simulation is listed below.

FET	Dimension
FET 251	$W = 150 \mu\text{m}$ , $L = 0.5 \mu\text{m}$
FET 110	$W = 10,000 \mu\text{m}$ , $L = 0.5 \mu\text{m}$
FET 252	$W = 10 \mu\text{m}$ , $L = 0.5 \mu\text{m}$
FET 253	$W = 10 \mu\text{m}$ , $L = 0.5 \mu\text{m}$

In this drawing, plots 300 and 302 shows the drain current of FET 251 and 110, respectively, for the regulator shown in FIG. 15. It shows that, as the temperature increases, the drain current of FET 110 increases significantly due to the gate-drain diode leakage current and it loses track of the drain current of FET 251. For the generator shown in FIG. 19, however, the drain current of FET 110 shown by plot 306 increases less with temperature and it tracks the drain current of FET 251 depicted by plot 304 even at high temperatures. The regulator shown in FIG. 19 therefore offers better temperature performance than the one depicted in FIG. 15.

As will be apparent to those skilled in the art, numerous modifications of the present invention may be made within the scope of the invention, which is not to be limited except in accordance with the following claims.

What is claimed is:

1. An amplifier operating with a single polarity power supply, comprising:

an amplifying stage including at least one depletion-mode FET for amplifying an input ac signal, said FET having a gate coupled to receive said input ac signal, a source connected to ground and a drain coupled to receive a positive voltage; and

a negative voltage generator for providing a negative voltage to bias the gate of said FET,

said negative voltage generator comprising a multivibrator generating first and second clock signals, a charge pump receiving said clock signals and operating to produce said negative voltage, and means for providing said negative voltage as a low potential reference to said multivibrator such that said clock signals include a negative potential period and as a result, said charge pump operating in a power efficient manner.

2. The amplifier of claim 1 further comprising means for providing said clock signals from said multivibrator to said charge pump, and said means including an RC network.

3. The amplifier of claim 1 further comprising a negative voltage regulator for regulating said negative voltage to a desired value and for providing a regulated negative voltage to the gate of said depletion-mode FET.

4. The amplifier of claim 3 wherein said negative voltage generator is a monolithic integrated circuit, and said regulator and said amplifying stage form another monolithic integrated circuit, and said amplifier is a hybrid device including said two monolithic integrated circuits.

5. The amplifier of claim 3 wherein said negative voltage generator, said negative voltage regulator and said amplifying stage form a monolithic GaAs integrated circuit.

6. The amplifier of claim 1 wherein said multivibrator comprises first and second inverters having input and output terminals,

a first capacitive means coupling between the input terminal of said first inverter to the output terminal of said second inverter,

a second capacitive means coupling between the input terminal of said second inverter and the output terminal of said first inverter,

a first resistive means coupled between the input terminal of said first inverter and ground, and

a second resistive means coupled between the input terminal of said second inverter and the negative voltage.

7. The amplifier of claim 6 wherein said first inverter comprises a first FET having a source connected to ground, a drain connected to a first load means and to the output terminal of said first inverter, and gate connected to the input terminal of said first inverter, and

wherein said second inverter comprises a second FET having a source connected to the negative potential, a drain connected to a second load means and to the output terminal of said second inverter, and a gate connected to the input terminal of said second inverter.

8. The amplifier of claim 7 wherein said first load means includes a third FET having gate and source connected together and to the drain of said first FET, and a drain coupled to a positive terminal of said power supply, and wherein said second load means includes a fourth FET having gate and source connected together and to the drain of said second FET, and a drain coupled to the positive terminal of said power supply.

9. The amplifier of claim 1 wherein said charge pump comprises a first electronic switch having a first terminal for connection to a positive terminal of said power supply and a second terminal,

a second electronic switch having a first terminal connected to the second terminal of said first electronic switch and a second terminal for connection to ground,

a third electronic switch having a first terminal for connection to ground and a second terminal,

a fourth electronic switch having a first terminal connected to the second terminal of said third electronic switch and a second terminal,

a pump capacitor coupled between the second terminal of said first electronic switch and the second terminal of said third electronic switch,

a hold capacitor coupled between the second terminal of the fourth electronic switch and ground,

said clock signals having a pump period and a hold period,

said first and third electronic switches being responsive to said second clock signal, and whereas said second and fourth electronic switches being responsive to said first clock signal, such that said first and third electronic switches being closed and said second and fourth electronic switches being open thereby charging said pump capacitor during said pump period, and

said first and third electronic switches being open and said second and fourth electronic switches being closed thereby transferring charge from said pump capacitor to said hold capacitor during said transfer period.

10. The amplifier of claim 9 wherein said charge pump comprises a first FET having a drain coupled to the positive terminal of said power supply, a gate connected to receive said second clock signal, and a source,

a second FET having a drain coupled to the source of said first FET, a gate connected to receive said first clock signal, and a source coupled to ground,

a third FET having a drain coupled to ground, a gate coupled to receive said second clock signal through a first capacitive means, and a source,

a fourth FET having a drain connected to the source of said third FET, a gate coupled to receive said first clock signal through a second capacitive means and a source,

said pump capacitor being coupled between the sources of said first and third FETs, said hold capacitor being coupled between the source of said fourth FET and ground, and

a first resistive means coupled between the gate and the source of said fourth FET, whereby said negative voltage is provided at the source of said fourth FET.

11. The amplifier of claim 9 wherein said charge pump comprises a first FET having a drain for connection to the positive terminal of said power supply, a gate connected to receive said second clock signal, and a source,

a second FET having a drain connected to the source of said first FET, a gate connected to receive said first clock signal, and a source for connection to ground,

a first diode means having a cathode coupled to ground, and an anode,

a second diode means having an anode coupled to the cathode of said first diode means, and an anode,

said pump capacitor being coupled between the source of said first FET and the anode of said first diode means, and

said hold capacitor being coupled between the anode of said second diode means and ground, whereby said negative voltage is provided at the anode of said second diode means.

12. The amplifier of claim 2 wherein said negative voltage regulator comprises a current source,

a first FET having a drain coupled to said current source, a source for connection to ground, and a gate;

a second FET having a drain coupled to said power supply, a gate coupled to the drain of said first FET, and a source;

a third FET having a drain coupled to the source of said second FET and to the gate of said first FET, a gate and a source connected together and to said negative voltage, whereby the regulated negative voltage is provided at the drain of said third FET.

13. The amplifier of claim 12 further comprising diode means connected between the source of said second FET and the drain of said third FET.

14. The amplifier of claim 2 wherein said negative voltage generator comprises a current source,

a first FET having a drain coupled to said current source, a source coupled to ground, and a gate,

a second FET having a drain coupled to said power supply, a gate coupled to the drain of said first FET, and a source,

a third FET having a drain coupled to the source of said second FET, a gate and a source connected together and to said negative voltage, the drain of said third FET being resistively coupled to the gate of said depletion-mode FET in said amplifying stage, and the gate of said first FET being resistively coupled to the gate of said depletion-mode FET in said amplifying stage, whereby the effect of increased temperature on the performance of said regulator is reduced.

15. The amplifier of claim 14 wherein said current source comprises a resistor coupled between said power supply and the drain of said first FET.

16. The amplifier of claim 15 wherein said depletion-mode FET in the amplifying stage and said first FET have substantially the same pinch-off characteristics, and the gate-width of said first FET is such that said negative voltage regulator provides a desired regulated negative voltage to bias said depletion-mode FET.

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17. The amplifier of claim 14 wherein said current source comprises a fourth FET having a drain coupled to said power supply, a gate and a source connected together and to the drain of said first FET.

18. The amplifier of claim 17 wherein said depletion-mode FET in the amplifying stage and said first and fourth FETs have substantially the same pinch-off characteristics, and the gate-width of said first FET is a predetermined factor times the gate-width of said fourth FET, whereby said depletion mode FET is biased at substantially its characteristic zero-bias saturation current divided by said predetermined factor.

19. The amplifier of claim 18 wherein the predetermined factor is 2, whereby said depletion-mode FET in said amplifying stage is biased at substantially one half of said characteristic zero-bias current for class A operation.

20. The amplifier of claim 18 wherein the predetermined factor is 4, whereby said depletion-mode FET in said amplifying stage is biased at substantially one quarter of said characteristic zero-bias current for class AB operation.

21. The amplifier of claim 18 wherein the predetermined factor is such that said depletion-mode FET in said amplify stage is biased around or below pinch-off for class B operation.

22. The amplifier of claim 21 further comprising diode means connected between the source of said second FET and the drain of said third FET.

23. A negative voltage generator operating with a single power supply comprising:

- a multivibrator generating first and second clock signals;
- a charge pump receiving said first and second clock signals and operating to generate a negative voltage; and

means for providing said negative voltage as a low reference potential to said multivibrator such that said clock signals generated by said multivibrator includes a negative potential period and as a result, said charge pump operating in a power efficient manner.

24. The negative voltage generator of claim 23 further comprising means for providing said first and second clock signals from said multivibrator to said charge pump, and said means including an RC network.

25. The negative voltage generator of claim 23 wherein said multivibrator comprises first and second inverters having input and output terminals,

- a first capacitive means coupling between the input terminal of said first inverter to the output terminal of said second inverter,
- a second capacitive means coupling between the input terminal of said second inverter and the output terminal of said first inverter,
- a first resistive means coupled between the input terminal of said first inverter and ground, and
- a second resistive means coupled between the input terminal of said second inverter and the negative voltage.

26. The negative voltage generator of claim 25 wherein said first inverter comprises a first FET having a source connected to ground, a drain connected to a first load means and to the output terminal of said first inverter, and gate connected to the input terminal of said first inverter, and

wherein said second inverter comprises a second FET having a source connected to the negative potential, a

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drain connected to a second load means and to the output terminal of said second inverter, and a gate connected to the input terminal of said second inverter.

27. The negative voltage generator of claim 26 wherein said first load means includes a third FET having gate and source connected together and to the drain of said first FET, and a drain coupled to a positive terminal of said power supply, and wherein said second load means includes a fourth FET having gate and source connected together and to the drain of said second FET, and a drain coupled to the positive terminal of said power supply.

28. The negative voltage generator of claim 23 wherein said charge pump comprises a first electronic switch having a first terminal for connection to a positive terminal of said power supply and a second terminal,

a second electronic switch having a first terminal connected to the second terminal of said first electronic switch and a second terminal for connection to ground,

a third electronic switch having a first terminal for connection to ground and a second terminal,

a fourth electronic switch having a first terminal connected to the second terminal of said third electronic switch and a second terminal,

a pump capacitor coupled between the second terminal of said first electronic switch and the second terminal of said third electronic switch,

a hold capacitor coupled between the second terminal of the fourth electronic switch and ground, said clock signals having a pump period and a hold period,

said first and third electronic switches being responsive to said second clock signal, and whereas said second and fourth electronic switches being responsive to said first clock signal, such that said first and third electronic switches being closed and said second and fourth electronic switches being open thereby charging said pump capacitor during said pump period, and

said first and third electronic switches being open and said second and fourth electronic switches being closed thereby transferring charge from said pump capacitor to said hold capacitor during said transfer period.

29. The negative voltage generator of claim 28 wherein said charge pump comprises a first FET having a drain coupled to the positive terminal of said power supply, a gate connected to receive said second clock signal, and a source,

a second FET having a drain coupled to the source of said first FET, a gate connected to receive said first clock signal, and a source coupled to ground,

a third FET having a drain coupled to ground, a gate coupled to receive said second clock signal through a first capacitive means, and a source,

a fourth FET having a drain connected to the source of said third FET, a gate coupled to receive said first clock signal through a second capacitive means and a source, said pump capacitor being coupled between the sources of said first and third FETs,

said hold capacitor being coupled between the source of said fourth FET and ground, and

a first resistive means coupled between the gate and the source of said fourth FET, whereby said negative voltage is provided at the source of said fourth FET.

30. The negative voltage generator of claim 28 herein said charge pump comprises a first FET having a drain for connection to the positive terminal of said power supply, a gate connected to receive said second clock signal, and a source,

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a second FET having a drain connected to the source of  
said first FET, a gate connected to receive said first  
clock signal, and a source for connection to ground,  
a first diode means having a cathode coupled to ground, 5  
and an anode,  
a second diode means having an anode coupled to the  
cathode of said first diode means, and an anode,

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said pump capacitor being coupled between the source of  
said first FET and the anode of said first diode means,  
and  
said hold capacitor being coupled between the anode of  
said second diode means and ground, whereby said  
negative voltage is provided at the anode of said second  
diode means.

\* \* \* \* \*



UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,892,400  
DATED : April 6, 1999  
INVENTOR(S) : van Saders *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title page, item [60], insert the following:

--[60] Provisional application No. 60/008,678, filed Dec. 15, 1995—

Column 1, line 5, insert the following:

--CROSS REFERENCE TO RELATED APPLICATION

Reference is made to and priority claimed from U.S. provisional application Ser. No. U.S. 60/008,678, filed Dec. 15, 1995, entitled AMPLIFIER USING A SINGLE POLARITY POWER SUPPLY AND INCLUDING DEPLETION MOE FET AND NEGATIVE VOLTAGE GENERATOR--

Signed and Sealed this  
Seventh Day of December, 1999

Attest:



Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,892,400  
DATED : April 6, 1999  
INVENTOR(S) : John van Saders, et. al.

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This certificate supersedes Certificate of Correction issued December 7, 1999.

Signed and Sealed this  
Twenty-fifth Day of January, 2000

Attest:



Attesting Officer

Acting Commissioner of Patents and Trademarks



US005670907A

**United States Patent** [19]

Gorecki et al.

[11] **Patent Number:** **5,670,907**[45] **Date of Patent:** **Sep. 23, 1997**[54] **VBB REFERENCE FOR PUMPED SUBSTRATES**[75] **Inventors:** James Gorecki, Hillsboro; Ravindar Lall; Robert B. Lefferts, both of Portland, all of Oreg.[73] **Assignee:** Lattice Semiconductor Corporation, Hillsboro, Oreg.[21] **Appl. No.:** 403,595[22] **Filed:** Mar. 14, 1995[51] **Int. Cl.** <sup>6</sup> ..... G05F 1/10[52] **U.S. CL.** ..... 327/535; 327/538; 327/539; 323/313[58] **Field of Search** ..... 327/535, 536, 327/537, 538, 539, 77; 323/313, 315[56] **References Cited****U.S. PATENT DOCUMENTS**

4,562,454	12/1985	Schultz et al.	357/51
4,961,007	10/1990	Kumanoya et al.	
4,964,082	10/1990	Sato et al.	365/189.09
5,003,197	3/1991	Nojima et al.	327/536
5,113,088	5/1992	Yamamoto et al.	327/537
5,144,223	9/1992	Gillingham	323/313
5,191,555	3/1993	Tabacco et al.	365/230.08
5,208,776	5/1993	Nasu et al.	365/200
5,220,534	6/1993	Redwine et al.	365/226

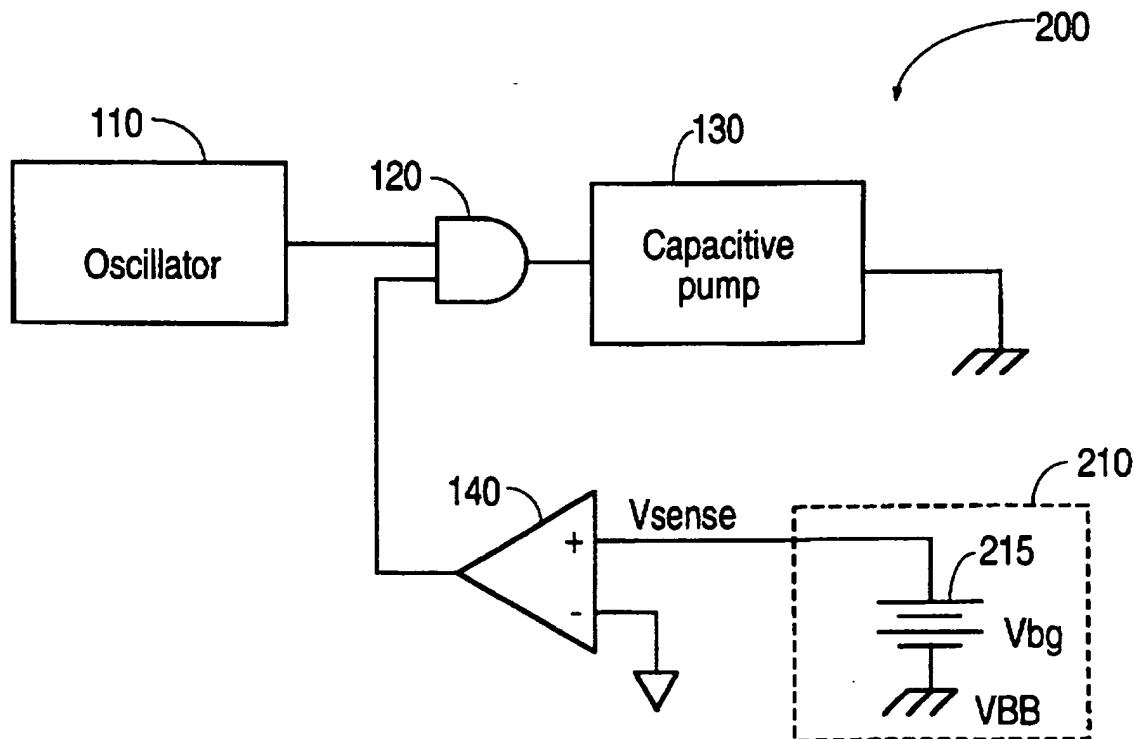
5,227,675	7/1993	Taguchi	327/535
5,309,446	5/1994	Cline et al.	371/21.1
5,345,422	9/1994	Redwine	365/189.09

**FOREIGN PATENT DOCUMENTS**

0015342 9/1980 European Pat. Off. .... 323/313

**OTHER PUBLICATIONS***Analysis and Design of Analog Integrated Circuits, 2d. Ed., Paul R. Gray et al., (1977, 1984), pp. 289-296, 736-737.**Primary Examiner*—Timothy P. Callahan*Assistant Examiner*—Jung Ho Kim*Attorney, Agent, or Firm*—Skjerven, Morrill, MacPherson, Franklin & Friel, L.L.P.; Stephen A. Terrile[57] **ABSTRACT**

An embodiment of a pumped substrate system includes an oscillator, capacitive pump, comparing circuit, and a level shifter. The level shifter is coupled between the substrate and the positive input lead of the comparator and shifts the voltage level present on the substrate by a voltage  $V_{bg}$ . The comparator compares ground potential to the shifted substrate voltage. The oscillator, capacitive pump and comparing circuit form a negative feedback loop which operates to maintain the substrate voltage substantially equal to  $-V_{bg}$ . In one embodiment, the level shifter includes a band gap reference.

**19 Claims, 5 Drawing Sheets**

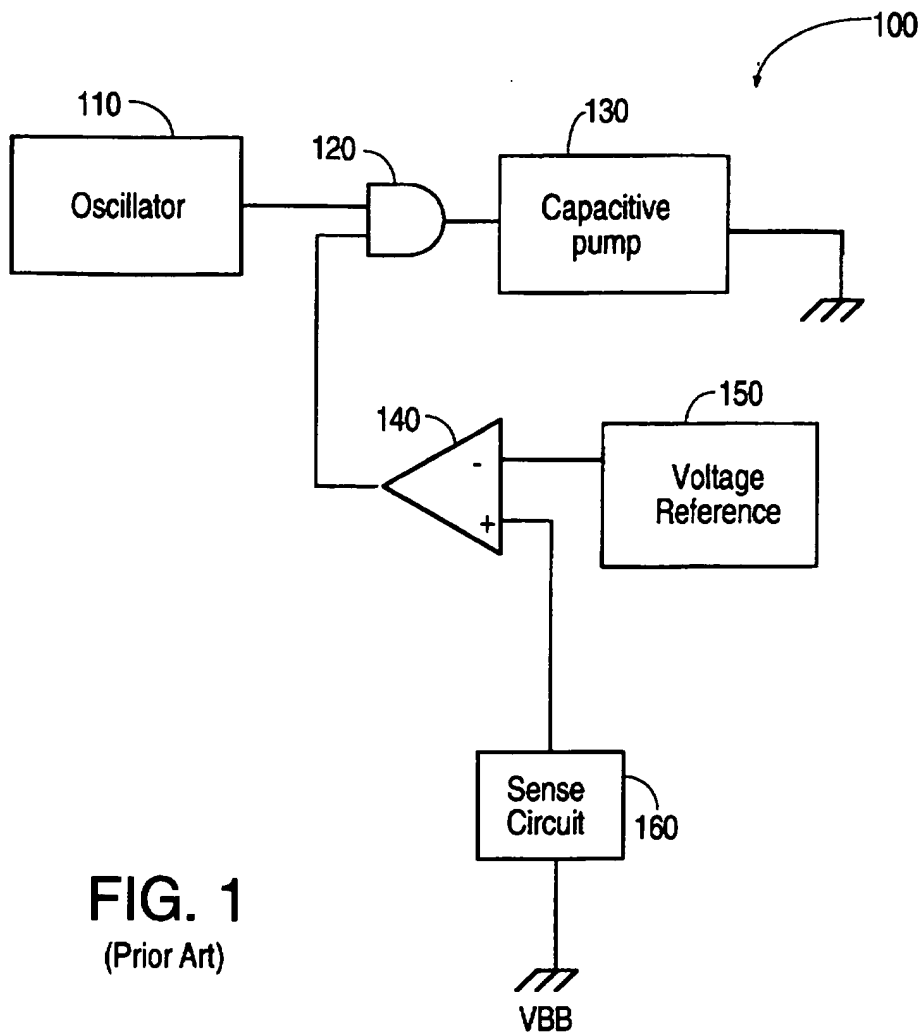


FIG. 1  
(Prior Art)

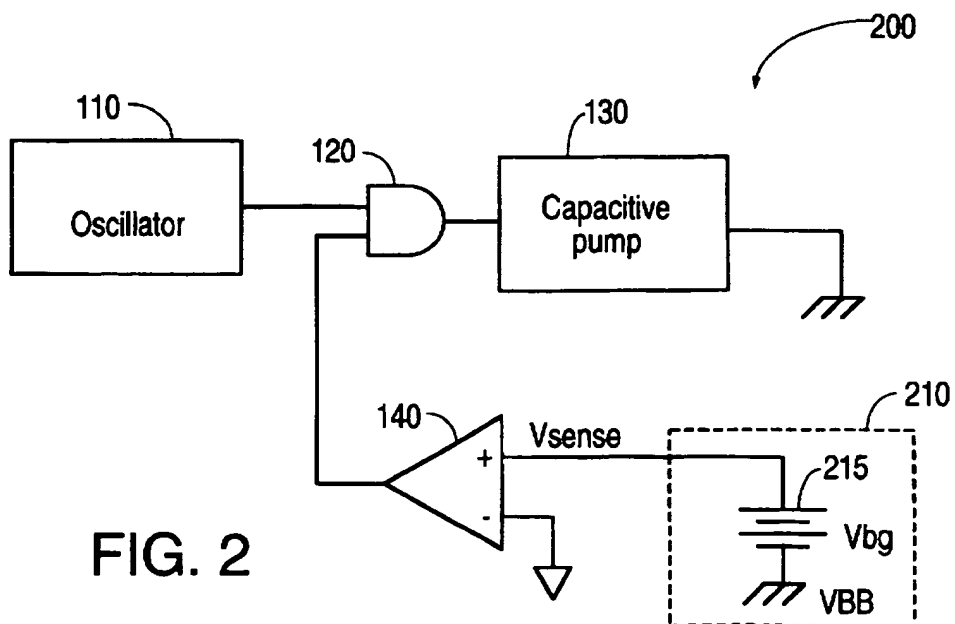


FIG. 2

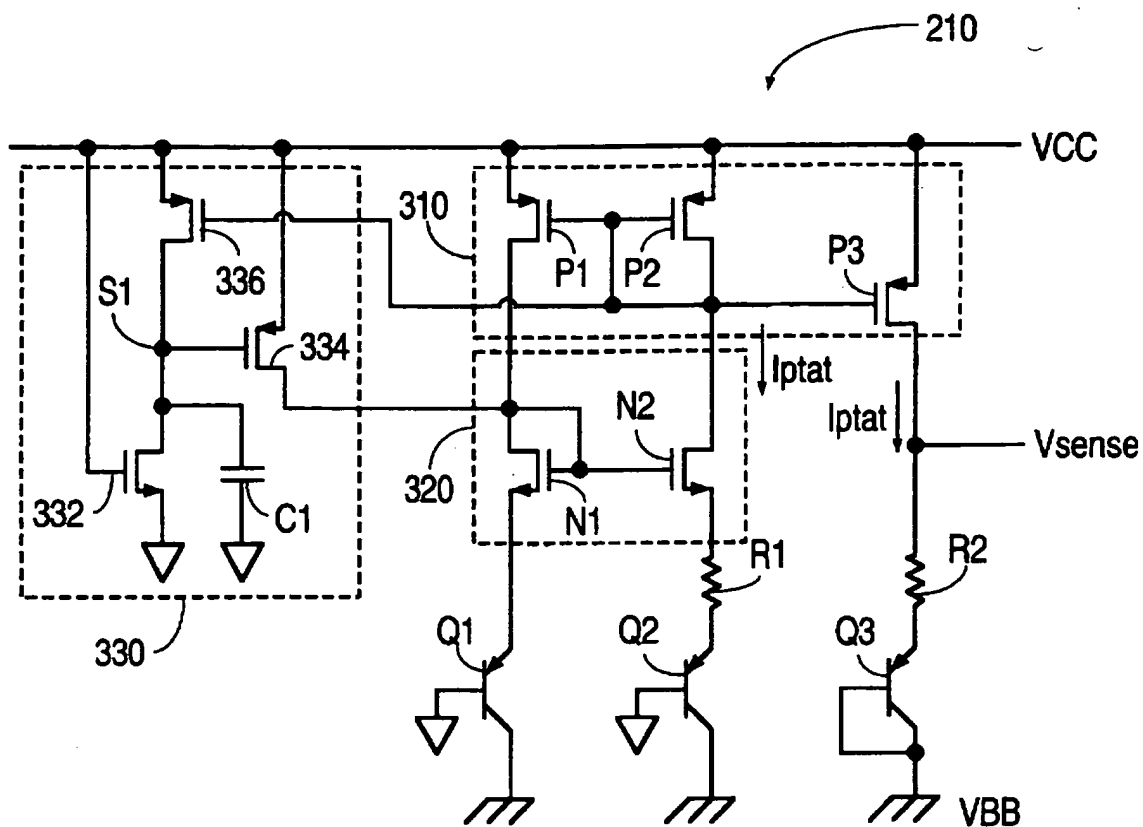


FIG. 3

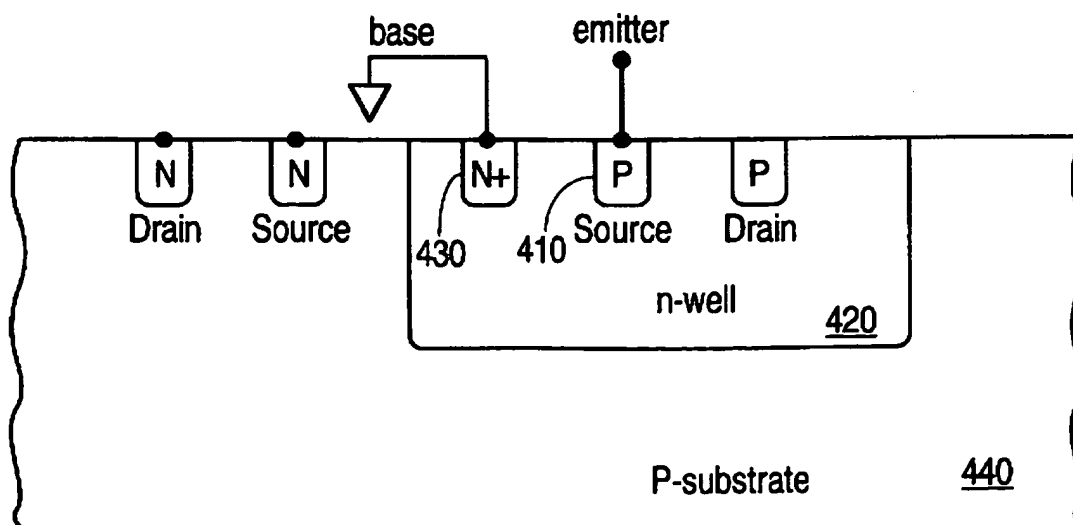


FIG. 4

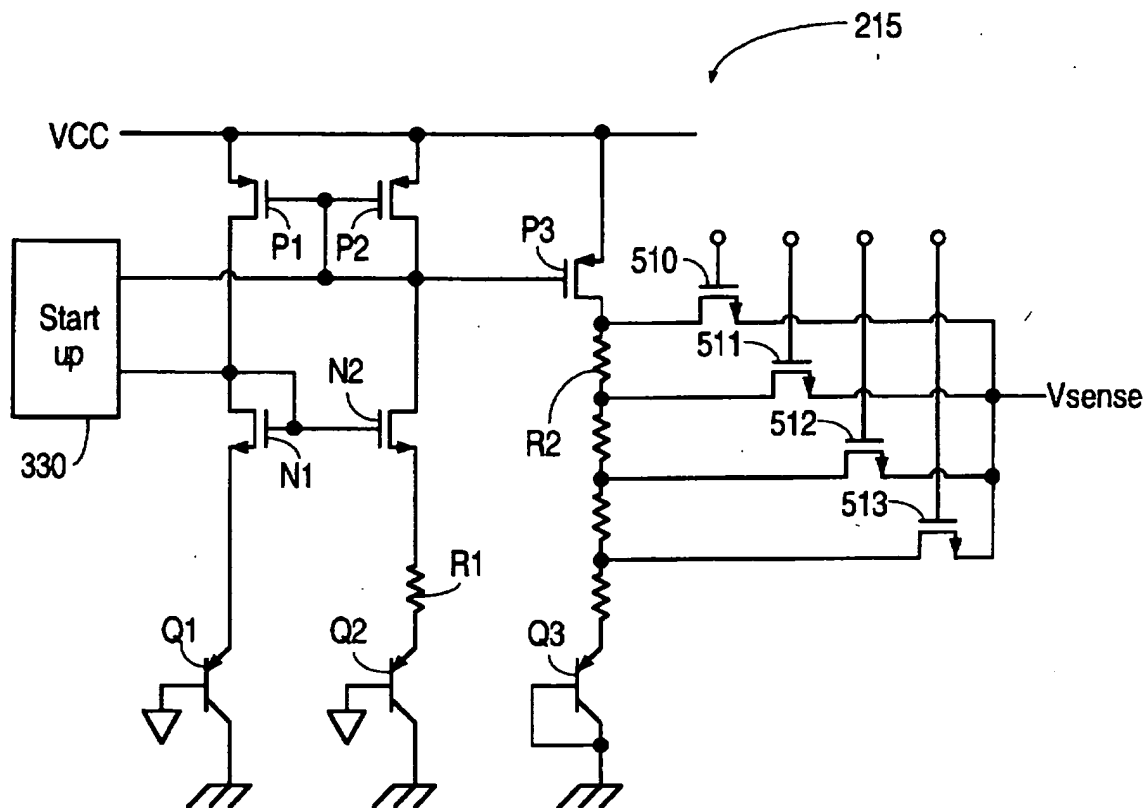


FIG. 5

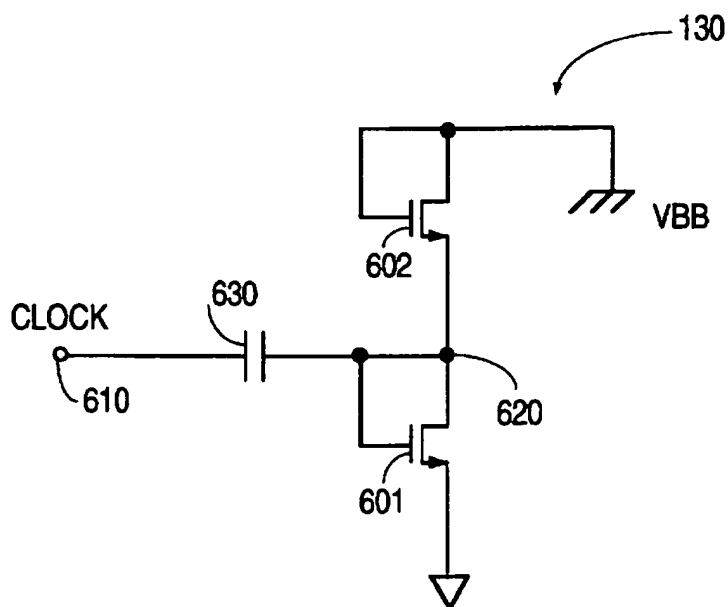


FIG. 6

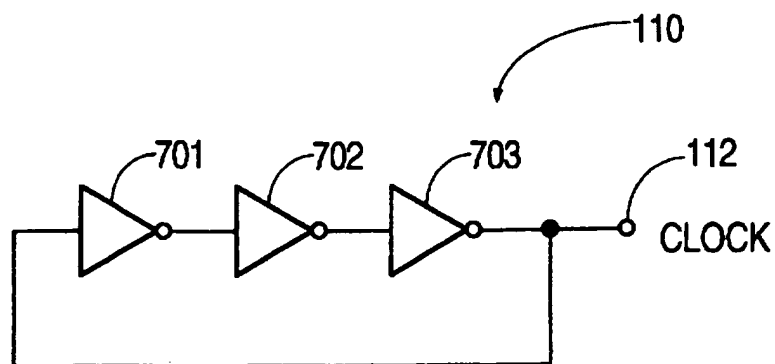


FIG. 7

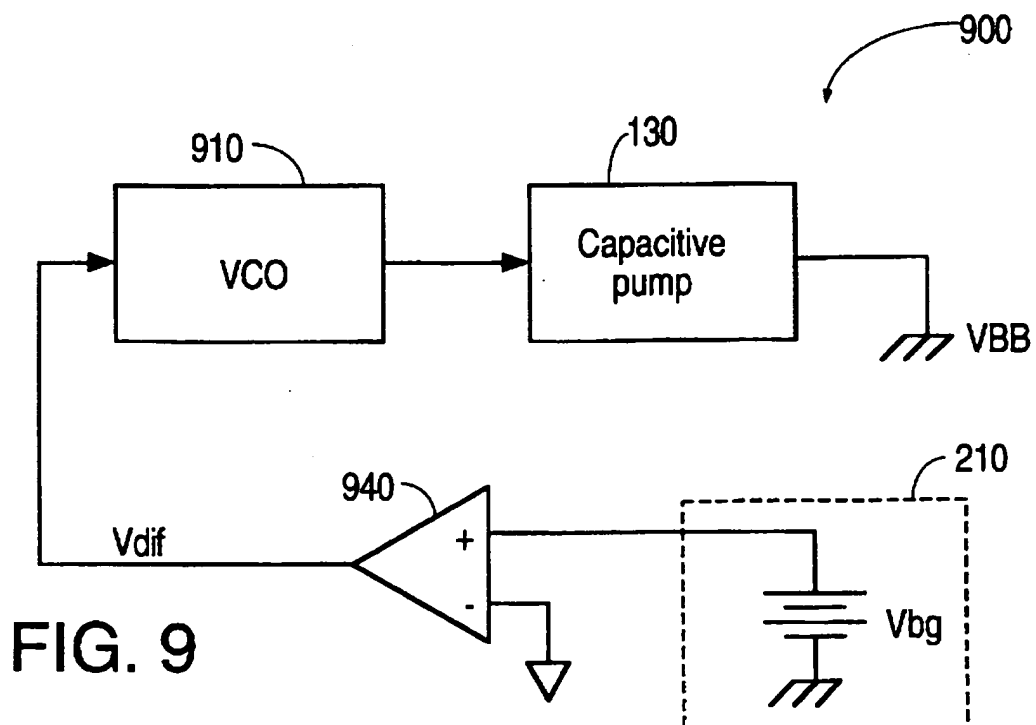


FIG. 9

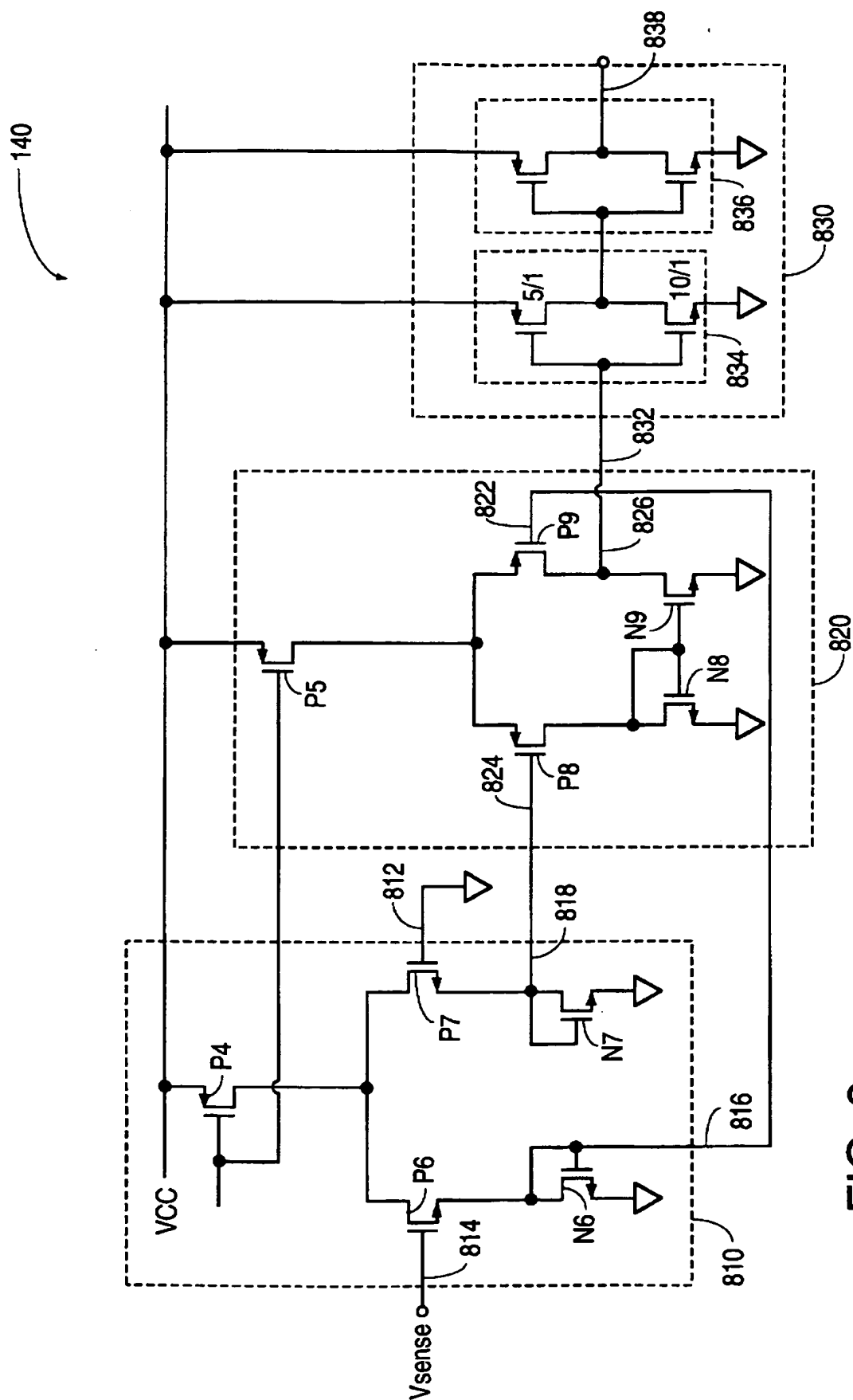


FIG. 8



## VBB REFERENCE FOR PUMPED SUBSTRATES

### 1. Field of the Invention

This invention relates to integrated circuits and, particularly, to integrated circuits having pumped substrates.

### 2. Background

Some MOS and CMOS integrated circuits have a capacitive pump circuit to control the integrated circuit's substrate voltage ("VBB") to improve performance. This scheme is sometimes called a "pumped substrate" technique. The pumped substrate system operates to back-bias the substrate to decrease body effect and reduce parasitic capacitance so that the threshold voltage ( $V_t$ ) of the devices decreases without decreasing the devices' saturation current ( $I_{dsat}$ ).

FIG. 1 shows a pumped substrate system 100 including an oscillator 110, an AND gate 120, a capacitive pump 130, a comparator 140, a voltage reference 150, and a sense circuit 160 forming a conventional pumped substrate system. Voltage reference 150 supplies a voltage  $V_{ref}$  to the negative input terminal of comparator 140. Voltage  $V_{ref}$  is negative so that the substrate is back-biased as described below. Sense circuit 160 senses substrate voltage VBB and provides a voltage intended to be equal to substrate voltage VBB to the positive input terminal of comparator 140. The output lead of comparator 140 is connected to one input lead of AND gate 120. The other input lead of AND gate 120 is coupled to the output lead of oscillator 110.

Thus, when substrate voltage VBB is lower (i.e., more negative) than voltage  $V_{ref}$ , comparator 140 outputs a logic 0 signal to AND gate 120. AND gate 120 receives this logic 0 signal from comparator 140 and, as a result, AND gate 120 outputs a logic 0 signal no matter what the input is to the other input lead of AND gate 120. Thus, the clock signal generated by oscillator 110 is not transmitted to capacitive pump 130. Capacitive pump 130 is a conventional capacitive charge pump that operates to add negative charge to the substrate in response to the clock signal generated by oscillator 110. As a result, capacitive pump 130 does not add negative charge to the substrate when substrate voltage VBB is lower than voltage  $V_{ref}$ .

On the other hand, when substrate voltage VBB is higher (i.e., more positive) than voltage  $V_{ref}$ , comparator 140 outputs a logic 1 signal to AND gate 120. Thus, the clock signal generated by oscillator 110 is gated through AND gate 120 to capacitive pump 130. In response to the clock signal, capacitive pump 130 operates to add negative charge to the substrate, thereby causing substrate voltage VBB to decrease.

However, the negative charge pumped into the substrate will bleed from the substrate, thereby causing voltage VBB to rise. Comparator 140, AND gate 120 and capacitive pump 130 form a negative feedback loop to add negative charge to the substrate to maintain voltage VBB substantially equal to voltage  $V_{ref}$ .

One problem of pumped substrate system 100 is in sensing substrate voltage VBB so that voltage VBB can be compared to voltage  $V_{ref}$ . In this conventional system, sense circuit 160 is a complex circuit that is sensitive to process, temperature and power supply variations. Further, voltage reference 150 is usually implemented using P-channel devices when the substrate is P-type semiconductor material. These P-channel devices are also sensitive to these same variations. As a result, substrate voltage VBB can vary as much as  $-0.5V$  to  $-2.5V$  in pumped substrate system 100, which is unacceptable in many applications.

### SUMMARY

In accordance with the present invention, a method for maintaining the voltage of a substrate at a desired level is

provided, along with a structure for implementing the method. The method employs a level shifter for shifting the voltage at the substrate for comparison with a convenient voltage.

According to one embodiment of the present invention, a pumped substrate system includes an oscillator, capacitive pump, comparing circuit, and a level shifter. The level shifter is coupled between the substrate and the positive input lead of the comparing circuit and shifts the substrate voltage by a voltage  $V_{bg}$ . The negative input lead of the comparator is coupled to a source of ground potential. Thus, there is no need for a complex sense circuit to sense substrate voltage VBB. The comparing circuit compares ground potential to a voltage that is substantially equal to the sum of voltage  $V_{bg}$  and substrate voltage VBB (i.e.,  $V_{sum}$ ). The oscillator, capacitive pump, level shifter, and comparing circuit form a negative feedback loop which operates to maintain voltage  $V_{sum}$  substantially equal to ground potential. As a result, substrate voltage VBB is maintained at a voltage substantially equal to  $-V_{bg}$ .

In this embodiment, the level shifter includes a band gap reference to generate voltage  $V_{bg}$ . Thus, voltage  $V_{bg}$  is relatively insensitive to process, temperature, and power supply variations. As a result, substrate voltage VBB is maintained at a desired voltage, which is also relatively insensitive to process, temperature, and power supply variations.

In this embodiment, the band gap reference implementation includes PNP transistors. As a result, this embodiment is advantageously used in integrated circuits using N-well processes so that the band-gap reference can be implemented using the parasitic vertical PNP transistors available in all N-well processes.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a conventional pumped substrate system.

FIG. 2 shows a block diagram of a pumped substrate system according to one embodiment of the present invention.

FIG. 3 shows a schematic diagram of one embodiment of the level shifter circuit depicted in FIG. 2.

FIG. 4 shows a cross-sectional view of the PNP transistors depicted in FIG. 3.

FIG. 5 shows a schematic diagram of another embodiment of the level shifter circuit depicted in FIG. 2.

FIG. 6 shows a schematic diagram of one embodiment of the capacitive pump depicted in FIG. 2.

FIG. 7 shows a schematic diagram of one embodiment of the oscillator depicted in FIG. 2.

FIG. 8 shows a schematic diagram of one embodiment of the comparator depicted in FIG. 2.

FIG. 9 shows a block diagram of a pumped substrate system according to another embodiment of the present invention.

### DETAILED DESCRIPTION

FIG. 2 shows a pumped substrate system 200 including oscillator 110, AND gate 120, capacitive pump 130, comparator 140 and a level shifter 210. Like reference numerals are used between drawings for like elements.

Level shifter 210 includes a band gap reference 215, which outputs a voltage  $V_{bg}$ . In this embodiment, voltage  $V_{bg}$  is designed to be approximately 1.5V. Although 1.5V is

used in this embodiment, the band gap reference (described further in conjunction with FIG. 3) can be designed to supply an arbitrary voltage between approximately a  $V_{BE_{ON}}$  above ground potential and a threshold voltage  $V_t$  below VCC. Band gap reference 215 is coupled between the output terminal of level shifter 210 and the substrate. As a result, level shifter 210 generates a voltage  $V_{sense}$ , given by the equation

$$V_{sense}=V_{BB}+V_{bg} \text{ or } V_{sense}=V_{BB}+1.5V \quad (1)$$

in this embodiment.

The output lead of level shifter 210 is coupled to the positive input lead of comparator 140. The other input lead of comparator 140 is coupled to a source of ground potential. Thus, when substrate voltage  $V_{BB}$  is less than  $-1.5V$ , voltage  $V_{sense}$  is negative, thereby causing comparator 140 to output a logic 0 signal. The output lead of comparator 140 is coupled to one input lead of AND gate 120 and, thus, AND gate 120 also outputs a logic 0 signal. The other input lead of AND gate 120 is coupled to the output lead of oscillator 110. Consequently, AND gate 120 does not gate the clock signal generated by oscillator 110 to capacitive pump 130, which is coupled to the output lead of AND gate 120. In this embodiment, oscillator 110 outputs a clock signal having a frequency of approximately 40 MHz.

Although an AND gate is used in this embodiment to gate the clock signal to capacitive pump 130, other embodiments may use different gating circuits, such as a NAND gate, a multiplexor, or a switch (provided the switch's output lead, coupled to capacitive pump 130, is not allowed to float).

Capacitive pump 130 is a conventional charge pump having an output lead coupled to the substrate and operates to pump negative charge into the substrate in response to the clock signal received from oscillator 110. Accordingly, when voltage  $V_{sense}$  is lower than ground potential, comparator 140 outputs a logic 0 signal. Consequently, AND gate 120 does not gate the clock signal from oscillator 110, which causes capacitive pump 130 to not operate.

On the other hand, when substrate voltage  $V_{BB}$  is greater than  $-1.5V$ , level shifter 210 outputs a positive voltage  $V_{sense}$ . As a result, comparator 140 outputs a logic 1 signal, thereby causing AND gate 120 to gate the clock signal generated by oscillator 110 to capacitive pump 130. Capacitive pump 130 operates to pump negative charge into the substrate in response to the clock signal received from oscillator 110, thereby causing substrate voltage  $V_{BB}$  to decrease.

Capacitive pump 130 will continue to pump negative charge into the substrate until substrate voltage  $V_{BB}$  decreases below  $-1.5V$ . Then, as described above, comparator 140 will cause AND gate 120 to stop gating the clock signal to capacitive pump 130. However, as negative charge bleeds from the substrate, substrate voltage  $V_{BB}$  will eventually rise above  $-1.5V$ , which will be detected by comparator 140, which will in turn cause AND gate 120 to gate the clock signal from oscillator 110 to operate capacitive pump 130. Thus, the feedback loop formed by level shifter 210, comparator 140, AND gate 120 and capacitive pump 130 operates to maintain substrate voltage  $V_{BB}$  at substantially  $-1.5V$ .

Level shifter 210 and comparator 140, coupled as shown in FIG. 2, provide a less complex circuit for detecting substrate voltage  $V_{BB}$  and comparing it to the desired voltage (in this case,  $-1.5V$ ) than sense circuit 160 coupled and comparator 140, coupled as shown in FIG. 1. Thus, level shifter 210 is easier and less costly to implement than sense circuit 160.

Moreover, because level shifter 210 includes band gap reference 215, level shifter 210 is less sensitive than sense circuit 160 to process, temperature, and power supply variation, thereby enabling pumped substrate system 200 to more accurately maintain substrate voltage  $V_{BB}$  at the desired voltage level.

This embodiment can be used advantageously in CMOS  $E^2$  technology applications such as electrically erasable programmable logic devices (PLD) with cell devices having gate oxides of less than 100Å thickness. The term CMOS is used herein to include silicon gate technologies. The sense current ( $I_{dsat}$ ) and  $V_t$  of the cells are two important parameters that affect the performance of these PLDs. It is desirable to have a large  $I_{dsat}$  and a low  $V_t$  to increase the PLD's speed. By back-biasing the substrate, parasitic capacitance is reduced and mobility is increased. Thus, back-biasing allows the designer to increase channel doping to increase  $I_{dsat}$  while achieving an acceptable  $V_t$ .

Generally,  $V_t$  and  $I_{dsat}$  both improve as substrate voltage  $V_{BB}$  is decreased. However, in these PLD applications, substrate voltage  $V_{BB}$  has a lower limit determined by junction breakdown of the substrate-to-N+ junctions and program retention of the application's electrically erasable cells. Because the cells are programmed with a high positive voltage on some of the cells' N+ diffusions, a large negative substrate voltage increases the risk of junction breakdown. Further, the negative substrate voltage creates an electric field between the substrate and the cells' channel which can remove charge used to program the cells. Thus, the cells can be erased if substrate voltage  $V_{BB}$  is too negative. For these applications, a substrate voltage in the range of  $-1.5V \pm 200$  mV provides relatively good  $V_t$  and  $I_{dsat}$  without a significant risk of junction breakdown and/or cell erasure.

FIG. 3 shows one embodiment of level shifter 210 comprising a P-channel current mirror 310, a N-channel current mirror 320, resistors R1 and R2, and PNP transistors Q1-Q3.

P-channel current mirror 310 comprises substantially identical P-channel transistors P1-P3. Accordingly, the currents conducted by transistors P1-P3 are substantially identical. Transistors P1-P3 of P-channel current mirror 310 each conduct current  $I_{ptat}$ . The channels of transistors P1 and P2 are coupled to the channels of substantially identical N-channel transistors N1 and N2 of N-channel current mirror 320. Thus, N-channel transistors N1 and N2 also conduct current  $I_{ptat}$ .

The source of transistor N1 is connected to the emitter of PNP transistor Q1. The base of transistor Q1 is coupled to a source of ground potential, and the collector of transistor Q1 is coupled to the substrate. Thus, transistor Q1 conducts the current from transistor N1 to the substrate.

The source of transistor N2 is coupled to the emitter of transistor Q2 through resistor R1. The base of transistor Q2 is coupled to a source of ground potential, and the collector of transistor Q2 is coupled to the substrate. Thus, transistor Q2 conducts the current from transistor N2 to the substrate.

The current conducted by the transistors of N-channel current mirror 320 is determined as follows. Because the bases of transistors Q1 and Q2 are coupled to a source of ground potential, the voltage loop equation from the base of transistor Q1 to the base of transistor Q2 is:

$$V_{BE_{Q1}} + (I_{ptat} R1) - V_{BE_{Q2}} = 0, \text{ or } I_{ptat} = (V_{BE_{Q2}} - V_{BE_{Q1}}) / R1 \quad (2)$$

where R1 is the resistance of resistor R1,  $V_{BE_{Q1}}$  is the base-to-emitter voltage of transistor Q1, and  $V_{BE_{Q2}}$  is the base-to-emitter voltage of transistor Q2. The base-to-emitter voltage of a PNP transistor is:

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$$V_{BE} = -V_T (\ln(I_C/I_S)) \quad (3)$$

where  $V_T$  is the thermal voltage,  $I_C$  is the collector current and  $I_S$  is the saturation current of the transistor. Combining equation (3) and equation (2) results in:

$$I_{ptat} = (V_T (\ln(I_{CQ1}/I_{SQ1}) - \ln(I_{CQ2}/I_{SQ2})) / R1 \text{ or } I_{ptat} = (V_T (\ln(I_{SQ2}/I_{SQ1})) / R1 \quad (4)$$

because the collector currents of transistors Q1 and Q2 are substantially equal.

Because  $I_S$  is proportional to cross-sectional area of the transistor's emitter, for a given process, equation (4) reduces to:

$$I_{ptat} = (V_T (\ln(A)) / R1 \quad (5)$$

where A is the ratio of emitter area of transistor Q2 to the emitter area of transistor Q1. Further, thermal voltage  $V_T$  is given by:

$$V_T = kT/q \quad (6)$$

where k is Boltzmann's constant, T is the temperature in °K., and q is the charge of an electron. Thus, equation (5) can be rewritten to:

$$I_{ptat} = (kT/q (\ln(A)) / R1 \quad (7)$$

by combining equations (5) and (6). Equation (7) shows that current  $I_{ptat}$  is proportional to absolute temperature.

Referring back to FIG. 3, the drain of P-channel transistor P3 is coupled through resistor R2 to the emitter of diode-connected PNP transistor Q3. The collector of transistor Q3 is coupled to the substrate. Thus, transistor P3 of P-channel current mirror 310 conducts current  $I_{ptat}$  through resistor R2 and PNP transistor Q3 to the substrate. Therefore, the voltage drop across resistor R2 and transistor Q3 is given by:

$$V_{sense} = V_{BE} = (I_{ptat}(R2) + V_{BE_{Q3}}) \text{ or } V_{sense} = V_{BE} = (kT/q (\ln(A) \times (R2/R1) + V_{BE_{Q3}}) \quad (8)$$

where R2 is the resistance of resistor R2, and voltage  $V_{sense}$  is the voltage supplied to the positive input terminal of comparator 140. Equation (8) defines a voltage in the form of the sum of a base-emitter voltage and the product of the thermal voltage and a constant, which is the standard relation for a band gap reference. Thus, the emitter area ratio of transistors Q2 to Q1, resistance ratio of resistors R2 to R1, and the threshold voltage of transistor Q3 can be determined so that the voltage drop across resistor R2 and transistor Q3 is substantially equal to 1.5V. The positive proportionality of current  $I_{ptat}$  offsets the negative temperature coefficient of the base-to-emitter voltage of PNP transistor Q3 to make a relatively temperature insensitive reference.

In this embodiment of level shifter 210, A is designed to be approximately 10, the ratio of resistor R2 to resistor R1 is approximately 12, and  $V_{BE_{Q3}}$  is approximately 700 mV. Typically,  $V_{BE_{Q3}}$  is set by the process, and A and the resistor ratio are varied to achieve the desired voltage. It is understood that A cannot be equal to 1 for the band gap reference to work as intended.

This embodiment of level shifter 210 results in a fractional temperature coefficient (TC<sub>F</sub>) of  $\pm 300$  ppm/°C. Thus, over a 100° C. temperature range, the voltage change is less than 100 mV, which is well within the voltage limits (i.e., 1.5V $\pm$ 200 mV) of this application.

Although the embodiment of band gap reference 215 of FIG. 3 has the bases of transistors Q1 and Q2 coupled to a

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source of ground potential, these transistors could just as well be diode connected without altering the function of the circuit. Further, current mirrors 310 and 320 can be scaled, which will in turn scale the voltage drop across resistor R2. Still further, current mirrors 310 and 320 can be implemented with Wilson or cascode current sources.

Current mirrors 310 and 320 have two stable states. The desired stable state, described above, is where current mirrors 310 and 320 conduct current  $I_{ptat}$ . The other stable state is where current mirrors 310 and 320 do not conduct any current. Level shifter 210 includes a start-up circuit 330 to ensure that current mirrors 310 and 320 conduct current  $I_{ptat}$  after receiving power.

Start-up circuit 330 includes a N-channel transistor 332 having its gate coupled to the source of voltage VCC and its source coupled to a source of ground potential. Shortly after the VCC voltage source begins supplying power (i.e., when voltage VCC reaches the threshold voltage of transistor 332), transistor 332 turns on and pulls the voltage at a node S1 to approximately ground potential. A capacitor C1 can be optionally coupled between node S1 and a source of ground potential, which serves to add a small delay to help ensure proper start up.

Node S1 is connected to a gate of a P-channel transistor 334. The source of transistor 334 is coupled to a source of voltage VCC. As a result, when transistor 332 pulls down the voltage on node S1 below voltage VCC minus a threshold voltage, transistor 334 turns on. The drain of transistor 334 is connected to the gates of transistors N1 and N2, which causes transistors N1 and N2 to become conductive. The current in the drain of transistor N2 turns on transistors P2 and P1, which then supplies current to transistor N1. The current in transistor N1 then sustains the current in transistor N2, and the circuit now operates normally.

Start-up circuit 330 further comprises a P-channel transistor 336. Transistor 336 also has a gate coupled to the drain of transistor P2 and, consequently, as the current in transistors N1, N2, Q1 and Q2 causes transistors P1 and P2 to conduct current, transistor 336 becomes conductive. Because transistor 336 is much larger than transistor 332, transistor 336 pulls up the voltage at node S1 to be approximately equal to voltage VCC. Thus, transistor 334 is turned off, thereby isolating start-up circuit 330 from current mirrors 310 and 320.

FIG. 4 shows a diagram of the implementation of PNP transistor Q1. PNP transistors Q2 and Q3 are implemented in substantially the same manner. As stated above, pumped substrate system 200 (FIG. 2) is used in a CMOS application. In this CMOS application, the P-channel devices are implemented with a N-well in a P-substrate. The PNP transistors are implemented using the parasitic vertical PNP transistors inherent in the N-well process. The N-channel device, the gates, and the gate oxides of the CMOS device are not used in the PNP transistor implementation and need not be formed. Source diffusion 410 forms the emitter of the PNP transistor. N-well 420 forms the base of the PNP transistor. N+ diffusion 430 couples the base to a source of ground potential. P-substrate 440 forms the collector.

FIG. 5 shows an embodiment of programmable level shifter 215' with FET 510-513 to tap resistor R2. Level shifter 215' is similar to level shifter 215 (FIG. 3) except that resistor R2 of level shifter 215 is replaced with programmable resistor R2'. The resistance of resistor R2' is programmed by providing control signals to the gates of FETs 510-513 to switch FETs 510-513 ON or OFF. Because resistor R2' may be "trimmed", this embodiment is used advantageously in applications where the VBE of transistor

Q3 varies with process so that the voltage drop across resistor R2' can be adjusted to set voltage V<sub>bg</sub> substantially equal to 1.5V. Although in this embodiment resistor R2' is programmable, resistors R1 and/or R2' may be programmable in other embodiments.

FIG. 6 shows one embodiment of the capacitive pump 130 comprising N-channel transistors 601 and 602 having their channels connected in series between a source of ground potential and the substrate. N-channel transistors 601 and 602 are diode-connected, with the source of transistor 601 coupled to a source of ground potential and the drain of transistor 601 coupled to the source of transistor 602. The drain of transistor 602 is coupled to the substrate. Because transistors 601 and 602 form diodes, during normal operation, positive charge can only flow from the substrate to the source of ground potential.

Clock terminal 610 is coupled to node 620 through a capacitor 630. Node 620 is located at the anode of the diode formed by transistor 601 and the cathode of the diode formed by transistor 602. In this embodiment, capacitor 630 has a capacitance of approximately 20 pF. Capacitive pump 130 receives the clock signal generated by oscillator 110 at clock terminal 610. Thus, when the clock signal nears its peak positive voltage, capacitor 630 couples this positive voltage to node 620, causing transistor 601 to become conductive and transistor 602 to become non-conductive. As a result, transistor 601 conducts charge from capacitor 630 to the source of ground potential.

Conversely, in the second half of the clock cycle, capacitor 630 couples node 620 to its most negative value, causing transistor 601 to be non-conductive and transistor 602 to become conductive. Consequently, transistor 602 conducts positive charge from the substrate to capacitor 630. Charge pump 130 can vary substrate voltage V<sub>BB</sub> to approximately  $-V_{CC} + \text{two diode drops}$  (i.e.,  $-V_{CC} + 2V_{TN}$ ). Thus, as the clock signal from oscillator 110 transitions from high-to-low and low-to-high, positive charge is pumped from the substrate to the source of ground potential. This operation is equivalent to pumping negative charge into the substrate.

FIG. 7 shows a schematic diagram of one embodiment of oscillator 110 (FIG. 2). Oscillator 110 is a simple ring oscillator with three inverters 701-703 cascaded, with the output lead of inverter 703 connected to the input lead of inverter 701. The output signal of any of inverters 701-703 approximates a square wave. In this embodiment, the average propagation delay of the inverters is approximately 4.16 ns. As a result, oscillator 110 has a cycle time of approximately 25 ns, thereby providing a clock signal of approximately 40 MHz.

FIG. 8 shows a schematic diagram of one embodiment of comparator 140 (FIG. 2). Comparator 140 includes an input stage 810 having input leads 812 and 814 respectively coupled to a source of ground potential and the output lead of level shifter 210 (FIG. 2). Input stage 810 has output leads 816 and 818 coupled to a second gain stage 820 at input leads 822 and 824, respectively. An output lead 826 of active-load stage 820 is coupled to an output stage 830 at input lead 832.

Input stage 810 includes P-channel transistor P4 having a gate coupled to P-channel current mirror 310 (FIG. 3). Transistor P4 is substantially identical to transistors P1-P3 and serves as a current source for input stage 810, providing a current, mirrored from P-channel current mirror 310, substantially equal to current I<sub>ptat</sub>.

The drain of transistor P4 is coupled to the source-coupled pair formed by P-channel transistors P6 and P7. The gate of transistor P6 serves as the positive input terminal of com-

parator 140 and is coupled to receive voltage V<sub>sense</sub> from level shifter 210 (FIG. 2). The gate of transistor P7 serves as the negative input terminal of comparator 140 and is coupled to a source of ground potential. The drains of transistors P6 and P7 are coupled respectively to negative output lead 816 and positive output lead 818. The drains of transistors P6 and P7 are also coupled respectively to the drains of diode-connected N-channel transistors N6 and N7. As a result, when voltage V<sub>sense</sub> is less than ground potential, transistor P6 becomes more conductive, thereby causing transistor P7 to conduct less current from transistor P4. Thus, the voltage at negative output lead 816 is pulled up, whereas the voltage at positive output lead 818 is pulled down.

Conversely, when voltage V<sub>sense</sub> is greater than ground potential, transistor P6 becomes less conductive, thereby causing transistor P7 to conduct more current from transistor P4. Consequently, the voltage at negative output lead 816 is pulled down, whereas the voltage at positive output lead 818 is pulled up. Accordingly, input stage 810 operates as a differential amplifier, generating a differential output signal at output leads 816 and 818.

Second gain stage 820 is a source-coupled pair with an active load. The current source for the source-coupled pair comprises P-channel transistor P5 having a gate coupled to P-channel current mirror 310 (FIG. 3). Transistor P5 is substantially identical to transistors P1-P3 and provides a current, mirrored from current mirror 310, substantially equal to current I<sub>ptat</sub>. The drain of transistor P5 is coupled to the sources of P-channel transistors P8 and P9, transistors P8 and P9 being substantially identical. The gates of transistors P8 and P9 are respectively coupled to positive input lead 824 and negative input lead 822, thereby receiving the differential output signal generated by input stage 810. The drains of transistors P8 and P9 are coupled respectively to the drains of substantially identical N-channel transistors N8 and N9.

Second gain stage 820 has a structure similar to input stage 810, except that the N-channel transistors (i.e., N8 and N9) that load the source-coupled pair (i.e., P-channel transistors P8 and P9) form a current source instead of the diodes that load the source-coupled pair in input stage 810. Only transistor N8 is diode connected, with the gate of transistor N9 coupled to the gate of transistor N8. The sources of transistors N8 and N9 are both coupled to a source of ground potential, thereby causing transistors N8 and N9 to have the same gate-to-source voltage. An output lead 826 is coupled to the drains of transistors P9 and N9. Negative input lead 822 and positive input lead 824 of second gain stage 820 are coupled respectively to negative output lead 818 and positive output lead 816 of input stage 810.

Consequently, when the voltage on positive input lead 824 rises (the voltage on negative input lead 822 decreases because of the differential output of input stage 810), transistor P8 becomes less conductive while transistor P9 becomes more conductive. Thus, the voltage at the drain of transistor P9 is pulled up, while the voltage at the drain of transistor P8 decreases.

Conversely, when the voltage on positive input lead 824 decreases (the voltage on negative input lead 822 increases because of the differential output of input stage 810), transistor P8 becomes more conductive while transistor P9 becomes less conductive. Accordingly, transistor N9 conducts more current than transistor N8. Because transistors N8 and N9 have the same gate-to-source voltage, transistor N8 enters the ohmic region of operation (i.e., a much smaller V<sub>DS</sub> to conduct the smaller current, which pulls down the voltage at output lead 826. Accordingly, second gain stage

820 operates as a differential amplifier generating an output signal at output lead 826.

Output lead 826 of second gain stage 820 is connected to an input lead 832 of output stage 830 comprising two inverters. An inverter 834 has an input lead coupled to input lead 832. In inverter 834, the W/L ratio of the P-channel transistor is approximately  $\frac{1}{2}$  of the W/L ratio of the N-channel transistor. This ratio of W/L ratios lowers the "trip" voltage of inverter 834 (i.e., the voltage above which the inverter considers the input signal a logic 1 input signal, and below which the inverter considers the input signal a logic 0 input signal) to correspond to the voltage range of the output signal generated by second gain stage 820 at output lead 826. The input lead of inverter 836 is coupled to the output lead of inverter 834, thereby inverting the output signal generated by inverter 834. Thus, comparator 140 has an even number of inversions, resulting in a non-inverted output signal being generated at output lead 838.

FIG. 9 shows pumped substrate system 900 comprising a VCO 910, capacitive pump 130, level shifter 210, and an amplifier 940. Level shifter 210 and capacitive pump 130 operate as described above for pumped substrate system 200 (FIG. 2) and, thus, level shifter 210 outputs a voltage  $V_{sense}$  that is voltage  $V_{bg}$  higher than substrate voltage  $V_{BB}$ .

Amplifier 940 operates in a manner similar to comparator 140 (FIG. 2) except that amplifier 940 outputs a voltage  $V_{dif}$  proportional to the voltage difference between voltage  $V_{bg}$  and substrate voltage  $V_{BB}$  instead of the digital output of comparator 140. As a result, when substrate voltage  $V_{BB}$  is slightly higher than voltage  $V_{bg}$ , amplifier 940 outputs a relatively small positive voltage  $V_{dif}$ , whereas when substrate voltage  $V_{BB}$  is much higher than voltage  $V_{bg}$ , amplifier 940 outputs a relatively large positive voltage  $V_{dif}$ . The output lead of amplifier 940 is coupled to the input lead of VCO 910.

VCO 910 outputs a clock signal having a frequency proportional to the value of  $V_{dif}$ . VCO 910 is a conventional VCO. The output lead of VCO 910 is coupled to the input lead of capacitive pump 130.

Capacitive pump 130 operates to pump negative charge into the substrate. The rate at which capacitive pump 130 pumps negative charge into the substrate is proportional to the frequency of the clock signal received from VCO 910.

Amplifier 940, VCO 910, capacitive pump 130, and level shifter 210 form a feedback loop that operates to maintain substrate voltage  $V_{BB}$  approximately equal to  $-1.5V$ . As described above in conjunction with FIG. 2, the negative charge pumped into the substrate bleeds, thereby causing substrate voltage  $V_{BB}$  to rise. The higher substrate voltage  $V_{BB}$  is than  $-1.5V$ , the larger the value of voltage  $V_{dif}$ . Consequently, VCO 910 generates a higher frequency clock signal, which in turn causes capacitive pump 130 to pump negative charge into the substrate at a greater rate. Thus, substrate voltage  $V_{BB}$  is more quickly driven toward the desired voltage of  $-1.5V$ . As substrate voltage  $V_{BB}$  approaches  $-1.5V$ , voltage  $V_{dif}$  decreases, thereby causing VCO 910 to generate a lower frequency clock signal, which in turn causes capacitive pump 130 to pump negative charge into the substrate at a lower rate. When voltage  $V_{dif}$  is equal to  $0V$ , VCO 910 stops generating a clock signal. However, as negative charge bleeds from the substrate, voltage  $V_{dif}$  will rise above  $0V$ , thus causing VCO 910 to output a clock signal. Thus, the feedback loop operates to continuously maintain substrate voltage  $V_{BB}$  at the desired level of  $-1.5V$ .

The foregoing has described the principles and preferred embodiments of the present invention. However, the inven-

tion should not be construed as being limited to the particular embodiments described. For example, different implementations of the capacitive charge pump and/or amplifiers and/or band gap references may be used. Further, other embodiments may be used in applications different from the CMOS  $E^2$  application described herein. Still further, embodiments may be adapted for N-type substrates. Thus, the above-described embodiments should be regarded as illustrative rather than restrictive. Variations can be made to those embodiments by workers skilled in the art without departing from the scope of the present invention as defined by the following claims.

We claim:

1. A circuit implemented on a substrate having a voltage generated by a charge pump, said circuit comprising:

a current source providing a first current that is proportional to temperature; and

a level shifter coupled to said current source and said substrate, said level shifter providing

a first voltage that is shifted from said voltage of said substrate, wherein said level shifter comprises:

a first P-channel transistor coupled to said current source, said first P-channel transistor conducting a current substantially equal to said first current;

a first resistive device coupled to a drain of said first P-channel transistor; and

a first PNP transistor having a base and collector coupled to said substrate and an emitter coupled to said first resistive device.

2. The circuit of claim 1 wherein a voltage drop across said first resistive device and a base-to-emitter voltage of said first PNP transistor provides a voltage sum.

said first voltage and said voltage of said substrate have a voltage difference, and

the voltage sum is substantially equal to the voltage difference.

3. The circuit of claim 2 wherein said first voltage is substantially equal to ground potential.

4. The circuit of claim 1 wherein said current source comprises:

P-channel current mirror for conducting a second current, the second current being substantially equal to the first current;

a N-channel current mirror for conducting said second current from said P-channel current mirror;

a second PNP transistor having a collector coupled to said substrate and a base coupled to a source of a second voltage;

a second resistive device coupled between said N-channel current mirror and an emitter of said second PNP transistor; and

a third PNP transistor having a collector coupled to said substrate, a base coupled to said source of said second voltage, and an emitter coupled to said N-channel current mirror.

5. The circuit of claim 4 wherein said second voltage is substantially equal to ground potential.

6. The circuit of claim 4 wherein said first, second, and third PNP transistors are vertical parasitic PNP transistors.

7. The circuit of claim 6 wherein said N-channel current mirror comprises:

a first N-channel transistor having a source coupled to said emitter of said third PNP transistor; and

a second N-channel transistor having a source coupled to said second resistive device, said second resistive

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device being coupled in series between said source of said second N-channel transistor and said emitter of said second PNP transistor.

8. The circuit of claim 1 wherein said emitter of said first PNP transistor is formed from a source p+ diffusion, said base of said first PNP transistor is formed from a n-well and said collector of said first PNP transistor is formed from said substrate.

9. A method for maintaining a voltage of a substrate at a predetermined level, said method comprising the steps of: providing a first voltage that is substantially equal to a sum of a base-to-emitter voltage of a transistor and a product of a thermal voltage and a constant, wherein said constant is a product of a ratio of resistances and a natural logarithm of a ratio of emitter areas; applying said first voltage between said substrate and a first node; and varying a charge in said substrate to maintain a voltage of said first node at a second voltage, wherein the voltage of said substrate is maintained at said predetermined level.

10. The method of claim 9 wherein said step of providing comprises the step of varying a resistance ratio, wherein a change in said resistance ratio causes a proportional change in said constant.

11. The method of claim 9 wherein said step of providing comprises the step of varying an emitter area ratio.

12. A structure for maintaining a voltage of a substrate at a predetermined level, said structure comprising:

means for providing and applying a first voltage that is substantially equal to a sum of a base-emitter voltage of a transistor and a product of a thermal voltage and a constant, wherein said constant is a product of a ratio of resistances and a natural logarithm of a ratio of emitter areas;

said first voltage being applied between said substrate and a first node; and

means for varying a charge in said substrate to maintain a voltage of said first node at a second voltage, wherein the voltage of said substrate is maintained at said predetermined level.

13. The structure of claim 12 wherein said means for providing comprises means for varying a resistance ratio, wherein a change in said resistance ratio causes a proportional change in said constant.

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14. The structure of claim 13 wherein said means for providing comprises means for varying an emitter area ratio.

15. The structure of claim 12 wherein said means for varying comprises:

means for comparing said second voltage to said voltage of said first node;

means for generating a first signal when said voltage of said first node is more positive than said second voltage.

16. The structure of claim 15 wherein said means for varying further comprises means for pumping negative charge into said substrate.

17. The structure of claim 16 wherein said means for pumping comprises:

means for providing an oscillating signal; and

means for gating said oscillating signal to a capacitive charge pump.

18. The structure of claim 17 wherein said means for gating comprises:

means for receiving said first signal on a first input lead of an AND gate; and

means for receiving said oscillating signal on a second input lead of said AND gate.

19. A system for maintaining a voltage of a substrate at a predetermined voltage, said system comprising:

an oscillator;

a gating circuit having an input lead coupled to an output lead of said oscillator;

a pump circuit having an input lead coupled to an output lead of said gating circuit and an output lead coupled to said substrate;

a level shifter coupled between said substrate and a node; and

a comparing circuit having a first input lead coupled to said node, a second input lead coupled to a voltage source and an output lead coupled to a control lead of said gating circuit;

wherein said oscillator is a voltage-controlled oscillator and said comparing circuit is an amplifier, said voltage-controlled oscillator having an input lead coupled to an output lead of said amplifier.

\* \* \* \* \*

**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,670,907  
DATED : September 23, 1997  
INVENTOR(S) : Gorecki et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 1, line 16, delete "art" and insert --an--.

Signed and Sealed this  
Ninth Day of June, 1998

*Attest:*



BRUCE LEHMAN

*Attesting Officer*

*Commissioner of Patents and Trademarks*



US005208557A

**United States Patent** [19]**Kersh, III**[11] **Patent Number:** **5,208,557**[45] **Date of Patent:** **May 4, 1993****[54] MULTIPLE FREQUENCY RING OSCILLATOR****[75] Inventor:** David V. Kersh, III, Sugarland, Tex.**[73] Assignee:** Texas Instruments Incorporated, Dallas, Tex.**[21] Appl. No.:** 837,521**[22] Filed:** Feb. 18, 1992**[51] Int. Cl.:** H03B 5/24; H03K 3/354**[52] U.S. Cl.:** 331/57; 307/296.2; 331/74; 331/179**[58] Field of Search:** 331/57, 74, 179; 307/296.2**[56] References Cited****U.S. PATENT DOCUMENTS**

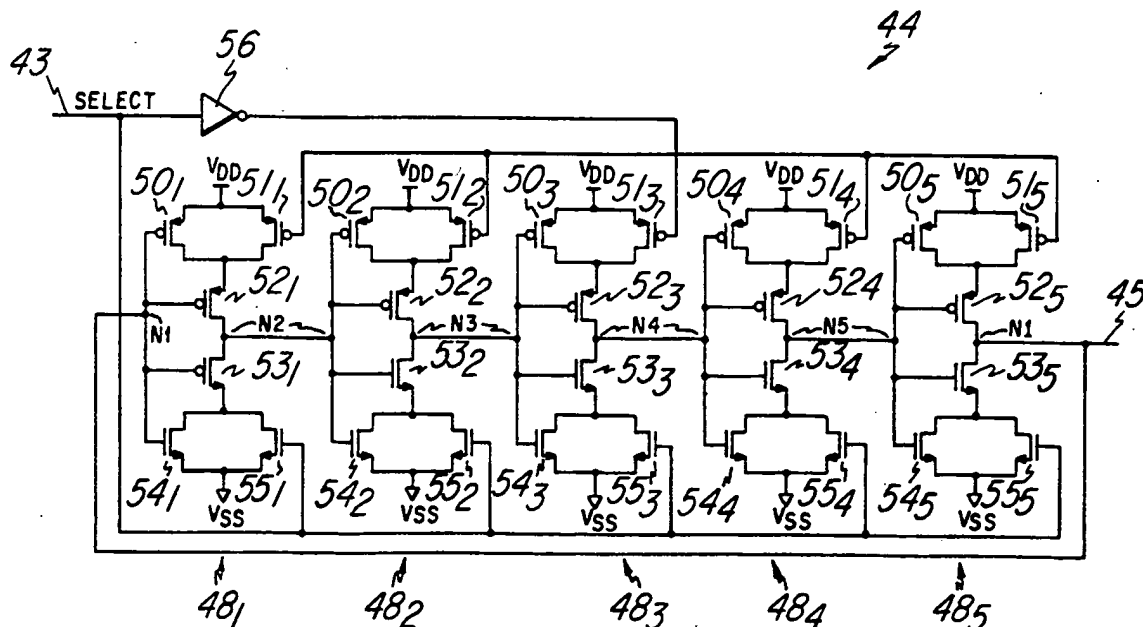
3,931,588 1/1976 Gehweiler ..... 331/57  
4,585,954 4/1986 Hashimoto et al. .... 307/296 R  
4,631,421 12/1986 Inoue et al. .... 307/297  
4,656,369 4/1987 Lou ..... 307/297

**OTHER PUBLICATIONS**

IBM Technical Disclosure Bulletin, vol. 32 No. 4A Sep. 1989, pp. 410-411 "Frequency Modulated Ring Oscillator For A Mode Regulated Substrate Bias Generator".

*Primary Examiner*—Siegfried H. Grimm*Attorney, Agent, or Firm*—W. James Brady, III; B. Peter Barndt; Richard L. Donaldson**[57] ABSTRACT**

A multiple frequency oscillator responds to a control signal to selectively produce an output signal having a first frequency or a second frequency. The oscillator includes a plurality of inverter stages (48<sub>1</sub>–48<sub>5</sub>) with the input of each inverter stage coupled to the output of another inverter stage. At least one of the inverter stages includes first and second transistors (50, 51) having current paths connected in parallel, a third transistor (52) having a current path connected in series with the current paths of the first and second transistors (50, 51) between a first voltage source (V<sub>DD</sub>) and the inverter stage output, and a fourth transistor (53) having a current path connected between the inverter stage output and a second voltage source (V<sub>SS</sub>). The control electrodes of the first, third, and fourth transistors (50, 52, 53) are connected to the input of the inverter stage. A control signal controls the conductivity of the second transistor (51) to select the frequency of output signal of the oscillator (44).

**34 Claims, 5 Drawing Sheets**



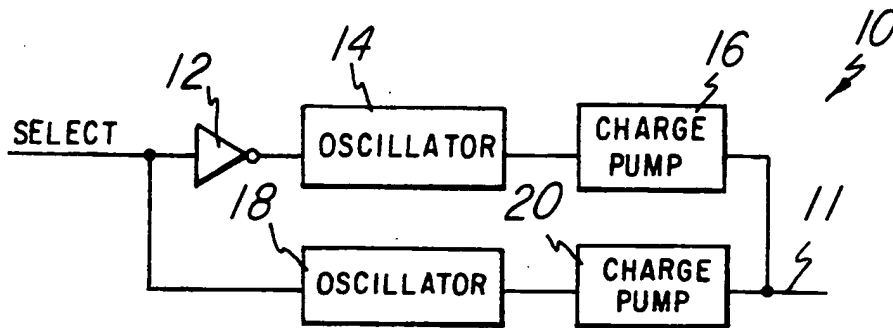


Fig. 1 PRIOR ART

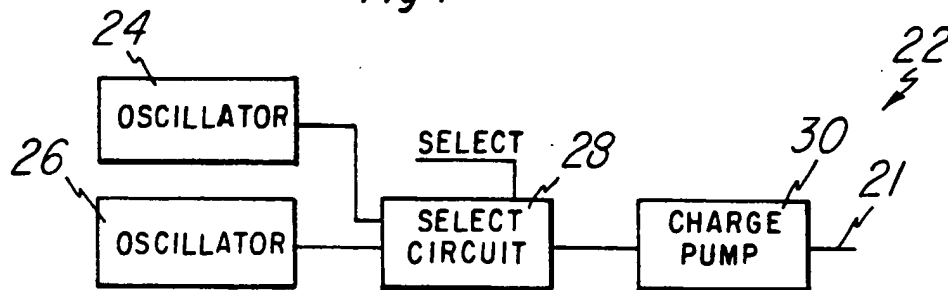


Fig. 2 PRIOR ART

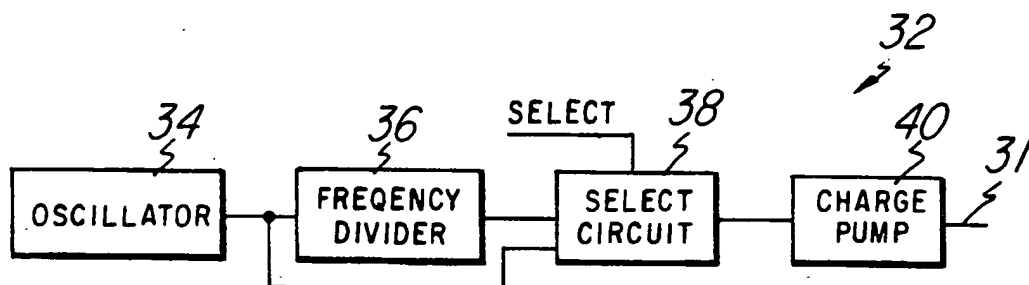


Fig. 3 PRIOR ART

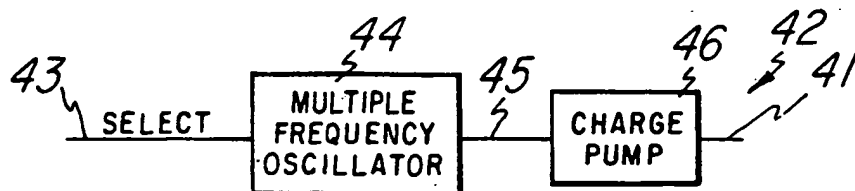


Fig. 4

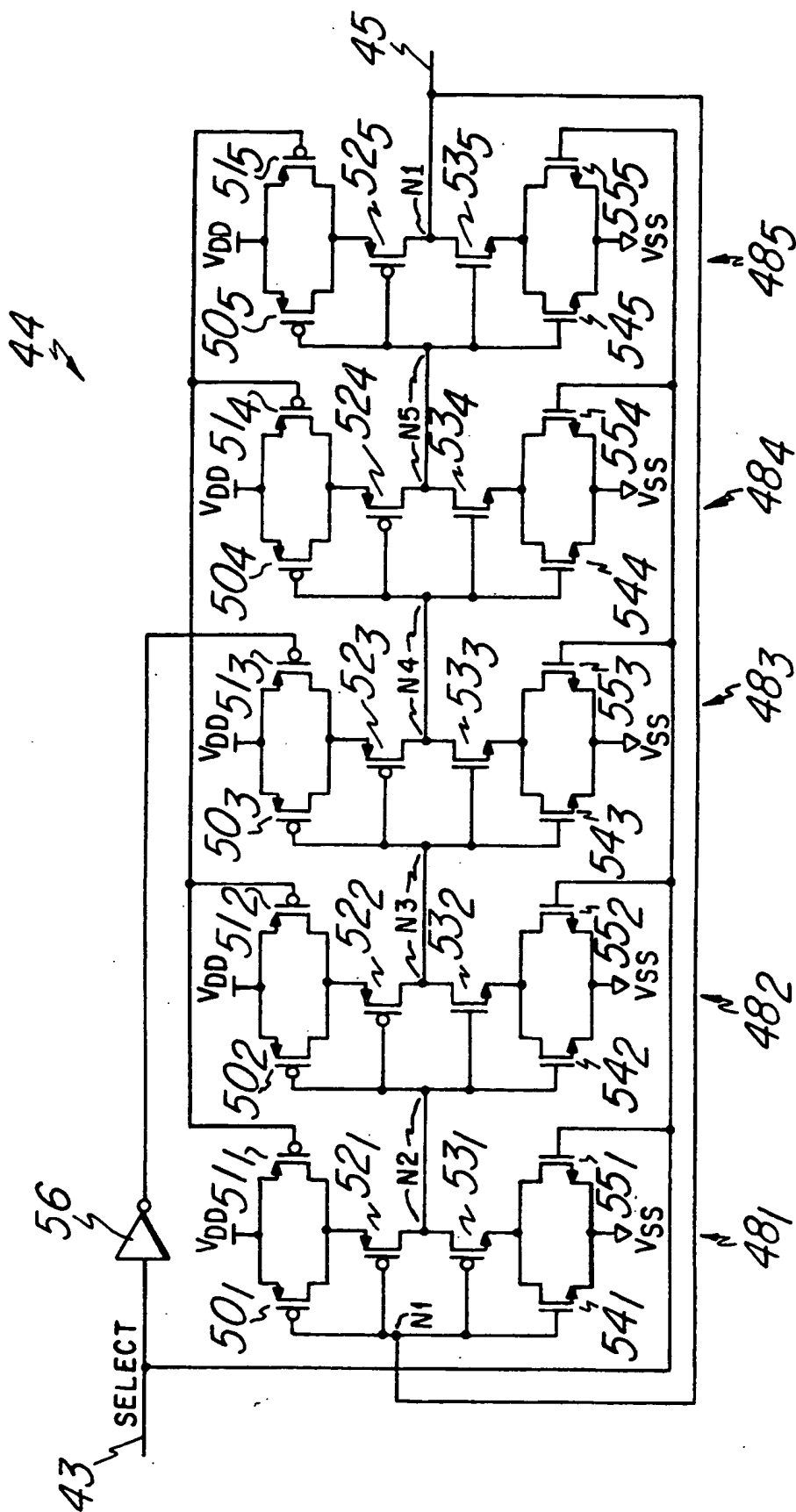


Fig. 5

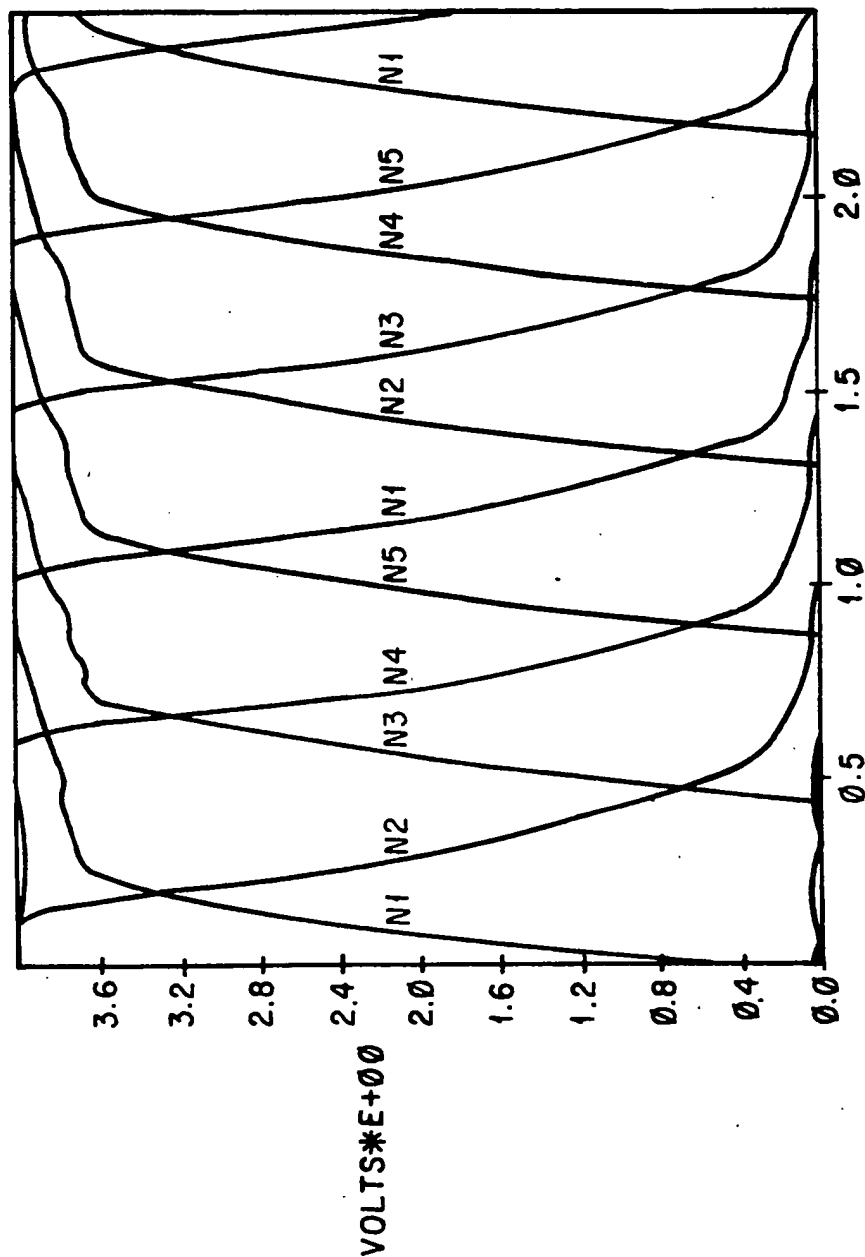


Fig. 6a

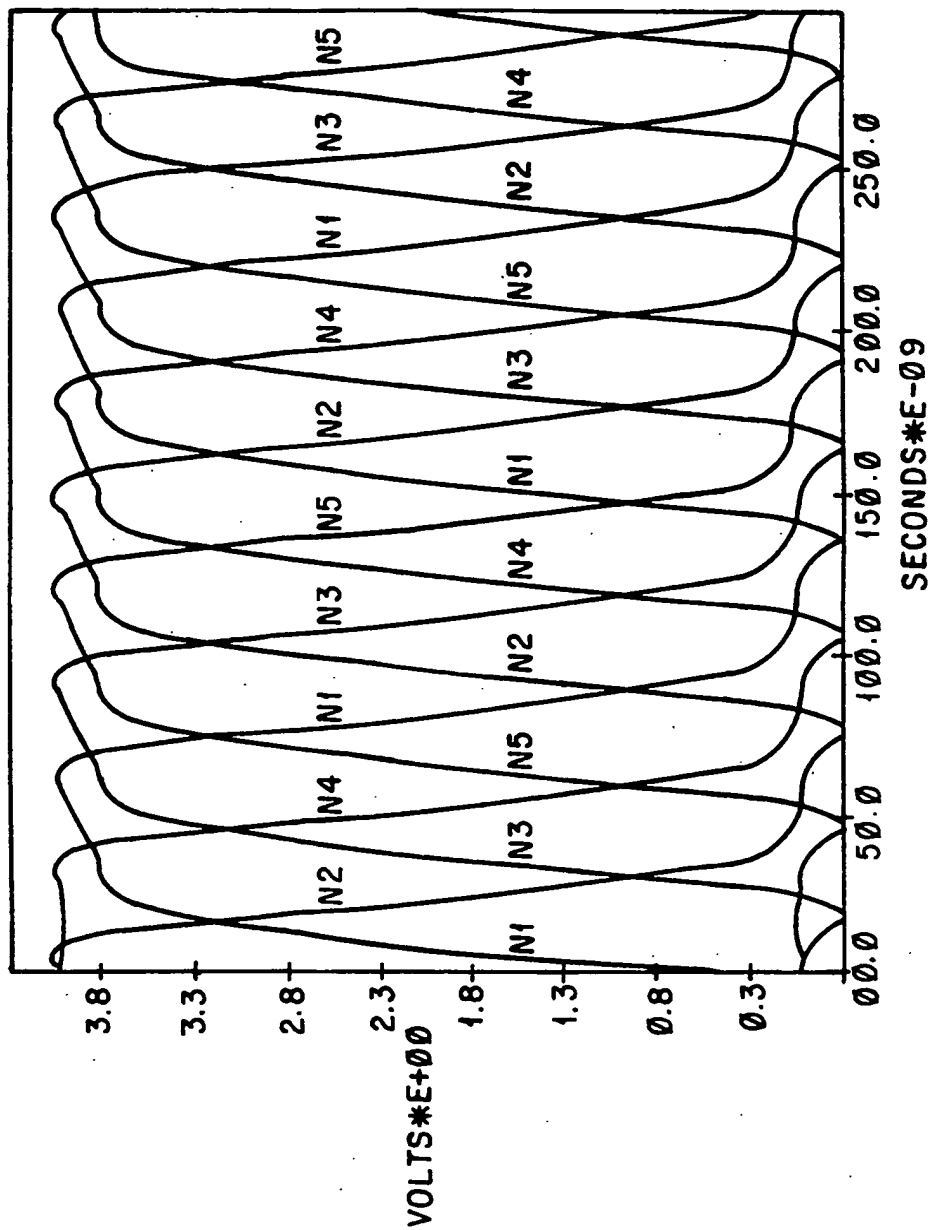


Fig. 6b

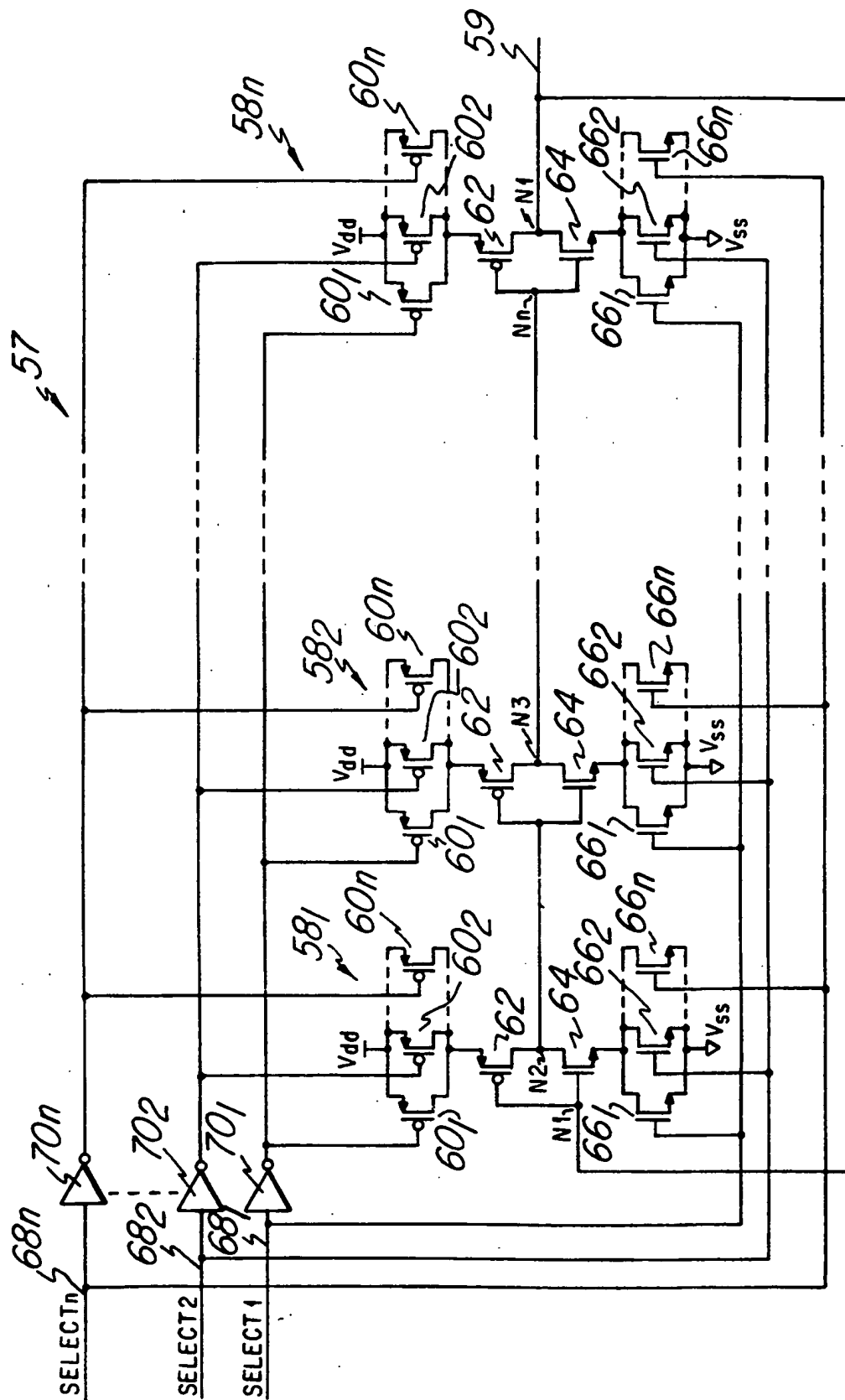


Fig.7

## MULTIPLE FREQUENCY RING OSCILLATOR

### FIELD OF THE INVENTION

This invention generally relates to oscillators and, more particularly, to multiple frequency oscillators.

### BACKGROUND OF THE INVENTION

Without limiting the scope of the invention, its background is described in connection with substrate bias voltage generators for dynamic random access memories (DRAMs) and other semiconductor devices, as an example.

DRAMs, as well as other types of semiconductor devices, are often provided with both an active mode and a standby mode of operation. Power consumption in the standby mode is reduced with respect to that in the active mode to increase efficiency during periods of time in which the device is powered up but idle.

One method to reduce power consumption in the standby mode is to reduce the frequency of operation of various circuits, such as substrate bias voltage generators, that must continually operate while the device is powered up. This method requires dual oscillator frequencies: a higher frequency to drive the circuits at full speed during operation in the active mode, and a lower frequency to drive the circuits at a slower speed, thereby reducing the power consumed by the circuits, during operation in the standby mode.

FIG. 1 shows a substrate bias voltage generator 10 according to the prior art that operates at dual frequencies. As is well known, substrate bias voltage generators are used to bias the substrates of DRAMs and other semiconductor devices to a negative voltage in order to improve performance of the semiconductor device. Substrate bias voltage generator 10 includes a first oscillator 14 and a first charge pump 16 for biasing substrate node 11 when the semiconductor device is operating in the active mode. Substrate bias voltage generator 10 also includes a second oscillator 18 and a second charge pump 20 for biasing substrate node 11 when the semiconductor device is operating in the standby mode.

Oscillator 18 has an input for receiving a SELECT signal while oscillator 14 has an input for receiving an inverted SELECT signal via inverter 12. In the standby mode, the SELECT signal has a high state to activate oscillator 18 and inactivate oscillator 14. Oscillator 18, when activated, supplies an output signal having a first frequency  $f_1$  to charge pump 20. Charge pump 20 biases substrate node 11 in response to the output signal from oscillator 18.

In the active mode, the SELECT signal has a low state to inactivate oscillator 18 and activate oscillator 14. Oscillator 14, when activated, supplies an output signal having a second frequency  $f_2$ , that is greater than  $f_1$ , to charge pump 16. Charge pump 16 biases substrate node 11 in response to the output signal from oscillator 14.

While substrate bias voltage generator 10 is capable of operating at dual frequencies to reduce standby power consumption, the cost is a relatively large amount of silicon area since two separate oscillators and two separate charge pumps are required.

FIG. 2 shows a second substrate bias voltage generator 22 according to the prior art that operates at dual frequencies. Substrate bias voltage generator 22 includes a first oscillator 24 that supplies an output signal having a first frequency  $f_1$  to select circuit 28 and a

second oscillator 26 that supplies an output signal having a second frequency  $f_2$ , that is greater than  $f_1$ , to select circuit 28. Select circuit 28 selectively couples the output signal of oscillator 24 or the output signal of oscillator 26 to charge pump 30 in response to a SELECT signal. Charge pump 30 generate a bias voltage in response to the signal received from select circuit 28.

In the standby mode, the SELECT signal has a first state causing select circuit 28 to couple the output of oscillator 24 to charge pump 30. Charge pump 30 biases substrate node 21 in response to the output signal from oscillator 24.

In the active mode, the SELECT signal has a second state causing select circuit 28 to couple the output of oscillator 26 to charge pump 30. Charge pump 30 biases substrate node 21 in response to the output signal from oscillator 26.

While substrate bias voltage generator 22 is capable of operating at dual frequencies to reduce standby power consumption, the cost is a relatively large amount of silicon area since two separate oscillators and a select circuit are required.

FIG. 3 shows a third substrate bias voltage generator 32 according to the prior art that operates at dual frequencies. Substrate bias voltage generator 32 includes an oscillator 34 that supplies an output signal having a first frequency  $f_2$  to select circuit 38 and to frequency divider 36. Frequency divider 36 supplies an output signal having a second frequency  $f_1$ , that is less than  $f_2$ , to select circuit 38. Select circuit 38 selectively couples the output signal of oscillator 34 or the output signal of frequency divider 36 to charge pump 40 in response to a SELECT signal. Charge pump 40 generate a bias voltage in response to the signal received from select circuit 38.

In the standby mode, the SELECT signal has a first state causing select circuit 38 to couple the output of frequency divider 36 to charge pump 40. Charge pump 40 biases substrate node 31 in response to the output signal from frequency divider 36.

In the active mode, the SELECT signal has a second state causing select circuit 38 to couple the output of oscillator 34 to charge pump 40. Charge pump 40 biases substrate node 31 in response to the output signal from oscillator 34.

While substrate bias voltage generator 32 is capable of operating at dual frequencies to reduce standby power consumption, the cost is a relatively large amount of silicon area since a frequency divider and select circuit are required. In addition, the reduction in power consumption is compromised to some extent by the power required to operate frequency divider 36.

### SUMMARY OF THE INVENTION

Generally, and in one form of the invention, a multiple frequency oscillator, includes: a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of the inverter stage outputs supplying an oscillator output signal; at least one of the inverter stages having an input for receiving a control signal, the control signal selectively having a first state or a second state, the at least one inverter stage responsive to the first state to cause the oscillator output signal to have a first frequency and responsive to the second state to cause the oscillator

output signal to have a second frequency different from the first frequency.

An advantage of the invention is a reduction in the area required by a circuit capable of producing an output signal having a plurality of selectable frequencies.

### BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGS. 1-3 are schematic block diagrams of substrate bias voltage generators according to the prior art;

FIG. 4 is a schematic block diagram of a substrate bias voltage generator according to the invention;

FIG. 5 is a schematic diagram of the dual frequency oscillator of FIG. 4;

FIG. 6a is a diagram showing voltage waveforms at various nodes of the oscillator of FIG. 5 during low frequency operation;

FIG. 6b is a diagram showing voltage waveforms at various nodes of the oscillator of FIG. 5 during high frequency operation; and

FIG. 7 is a schematic diagram of a multiple frequency oscillator.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 4 shows a substrate bias voltage generator 42 according to the invention that operates at multiple frequencies. Substrate bias voltage generator 42 includes a dual frequency oscillator 44 connected to a charge pump 46. Dual frequency oscillator 44 receives a SELECT signal on line 43 and in response supplies an oscillating output signal having a predetermined frequency over line 45 to charge pump 46. The output signal of oscillator 44 has a first frequency f1 when the SELECT signal is low and a second frequency f2, which is greater than f1, when the SELECT signal is high.

Charge pump 46 generates a bias voltage to bias substrate node 41 in response to the signal received from oscillator 44. In the standby mode, the SELECT signal has a first low state to cause oscillator 44 to produce an oscillating output signal having low frequency f1. Charge pump 46 biases substrate node 41 in response to the output signal from oscillator 44 having frequency f1.

In the active mode, the SELECT signal has a second high state to cause oscillator 44 to produce an oscillating output signal having high frequency f2. Charge pump 46 biases substrate node 41 in response to the output signal from oscillator 44 having frequency f2.

Charge pump 46 may be implemented using any of numerous well-known circuits. Suitable charge pump circuits are disclosed in U.S. Pat. Nos. 4,631,421 and 4,628,215, both of which are assigned to Texas Instruments, Incorporated and are incorporated herein by reference.

FIG. 5 shows oscillator 44 in detail. Oscillator 44 is a ring oscillator having an odd number (in this case, five) of cascaded inverter stages 48<sub>1</sub>-48<sub>5</sub>. The outputs of inverter stages 48<sub>1</sub>, 48<sub>2</sub>, 48<sub>3</sub>, 48<sub>4</sub>, and 48<sub>5</sub> are connected to the inputs of stages 48<sub>2</sub>, 48<sub>3</sub>, 48<sub>4</sub>, 48<sub>5</sub>, and 48<sub>1</sub>, respectively.

Each inverter stage 48 includes parallel-coupled p-channel transistors 50 and 51 having drains connected to a source of positive voltage Vdd and sources connected to the drain of p-channel transistor 52. Each

inverter stage 48 also includes parallel coupled n-channel transistors 54 and 55 having sources connected to Vss or ground and drains connected to the source of n-channel transistor 53. The input of each inverter stage 48 is connected to the gates of transistors 50, 52, 53, and 54. The output of each inverter stage 48 is connected between the source of transistor 52 and the drain of transistor 53.

The SELECT signal on line 43 is applied to the gates of n-channel transistors 55<sub>1</sub>-55<sub>5</sub> and to the input of inverter 56. Inverter 56 applies an inverted SELECT signal to the gates of p-channel transistors 51<sub>1</sub>-51<sub>5</sub>.

The frequency of oscillation of the output signal produced by oscillator 44 is determined by the rates at which nodes N1-N5 charge and discharge. The rate at which each of nodes N1-N5 charges is directly proportional to the capacitance at that node and the rate at which current flows to that node. The rate at which each of nodes N1-N5 discharges is directly proportional to the capacitance at that node and the rate at which current flows from that node. The state of the SELECT signal controls whether transistors 51<sub>1</sub>-51<sub>5</sub> and 55<sub>1</sub>-55<sub>5</sub> are conducting or non-conducting to determine the rate at which current flows to or from nodes N1-N5 and thereby the frequency of the output signal produced by oscillator 44 on line 45.

When the SELECT signal is in a low state, oscillator 44 produces an output signal having low frequency f1. This is due to the fact that the low state of the SELECT signal applied to the gates of n-channel transistors 55<sub>1</sub>-55<sub>5</sub> turns transistors 55<sub>1</sub>-55<sub>5</sub> off, while the high state of the inverted SELECT signal applied to the gates of p-channel transistors 51<sub>1</sub>-51<sub>5</sub> also turns transistors 51<sub>1</sub>-51<sub>5</sub> off. The nodes N1-N5 are alternately charged by current flowing through series connected transistor pairs 50<sub>1</sub> and 52<sub>1</sub>; 50<sub>2</sub> and 52<sub>2</sub>; 50<sub>3</sub> and 52<sub>3</sub>; 50<sub>4</sub> and 52<sub>4</sub>; 50<sub>5</sub> and 52<sub>5</sub>, respectively, and discharged by current flowing through series connected transistor pairs 53<sub>1</sub> and 54<sub>1</sub>; 53<sub>2</sub> and 54<sub>2</sub>; 53<sub>3</sub> and 54<sub>3</sub>; 53<sub>4</sub> and 54<sub>4</sub>; 53<sub>5</sub> and 54<sub>5</sub>, respectively.

When the SELECT signal is in a high state, oscillator 44 produces an output signal having high frequency f2. This is due to the fact that the high state of the SELECT signal applied to the gates of n-channel transistors 55<sub>1</sub>-55<sub>5</sub> turns transistors 55<sub>1</sub>-55<sub>5</sub> on, while the low state of the inverted SELECT signal applied to the gates of p-channel transistors 51<sub>1</sub>-51<sub>5</sub> also turns transistors 51<sub>1</sub>-51<sub>5</sub> on. The nodes N1-N5 are alternately charged by current flowing through groups of transistors 50<sub>1</sub>, 51<sub>1</sub> and 52<sub>1</sub>; 50<sub>2</sub>, 51<sub>2</sub> and 52<sub>2</sub>; 50<sub>3</sub>, 51<sub>3</sub> and 52<sub>3</sub>; 50<sub>4</sub>, 51<sub>4</sub> and 52<sub>4</sub>; and 50<sub>5</sub>, 51<sub>5</sub> and 52<sub>5</sub>, respectively, and discharged by current flowing through series connected transistor pairs 53<sub>1</sub>, 54<sub>1</sub> and 55<sub>1</sub>; 53<sub>2</sub>, 54<sub>2</sub> and 55<sub>2</sub>; 53<sub>3</sub>, 54<sub>3</sub> and 55<sub>3</sub>; 53<sub>4</sub>, 54<sub>4</sub> and 55<sub>4</sub>; and 53<sub>5</sub>, 54<sub>5</sub> and 55<sub>5</sub>, respectively. With transistors 51<sub>1</sub>-51<sub>5</sub> and 55<sub>1</sub>-55<sub>5</sub> on, the rate at which current flows to or from nodes N1-N5 is increased to increase the rate at which nodes N1-N5 charge and discharge and therefore the frequency of the output signal produced by oscillator 44.

FIG. 6a shows the voltage waveforms at nodes N1-N5 when the SELECT signal is low. Node N5 is initially low to turn transistors 50<sub>5</sub> and 52<sub>5</sub> on and transistors 53<sub>5</sub> and 54<sub>5</sub> off so that node N1 is charged only by current flowing from Vdd through transistors 50<sub>5</sub> and 52<sub>5</sub>. The rising voltage at node N1 will eventually turn transistors 50<sub>1</sub> and 52<sub>1</sub> off and 53<sub>1</sub> and 54<sub>1</sub> on, permitting current to flow from node N2 to Vss discharging node N2. The falling voltage at node N2 will eventually turn

transistors 50<sub>2</sub> and 52<sub>2</sub> on and 53<sub>2</sub> and 54<sub>2</sub> off, permitting current to flow from V<sub>dd</sub> to node N3 charging node N3. The rising voltage at node N3 will eventually turn transistors 50<sub>3</sub> and 52<sub>3</sub> off and 53<sub>3</sub> and 54<sub>3</sub> on, permitting current to flow from node N4 to V<sub>ss</sub> discharging node N4. The falling voltage at node N4 will eventually turn transistors 50<sub>4</sub> and 52<sub>4</sub> on and 53<sub>4</sub> and 54<sub>4</sub> off, permitting current to flow from V<sub>dd</sub> to node N5 charging node N5. As node N5 charges it will cause node N1 to discharge to complete one-half cycle.

FIG. 6b shows the voltage waveforms at nodes N1-N5 when the SELECT signal is high. Node N5 is initially low to turn transistors 50<sub>5</sub> and 52<sub>5</sub> on and transistors 53<sub>5</sub> and 54<sub>5</sub> off so that node N1 is charged by current flowing from V<sub>dd</sub> through transistors 50<sub>5</sub>, 51<sub>5</sub>, and 52<sub>5</sub>. The rising voltage at node N1 will eventually turn transistors 50<sub>1</sub> and 52<sub>1</sub> off and 53<sub>1</sub> and 54<sub>1</sub> on, permitting current to flow from node N2 to V<sub>ss</sub> via transistors 53<sub>1</sub>, 54<sub>1</sub>, and 55<sub>1</sub> discharging node N2. The falling voltage at node N2 will eventually turn transistors 50<sub>2</sub> and 52<sub>2</sub> on and 53<sub>2</sub> and 54<sub>2</sub> off, permitting current to flow from V<sub>dd</sub> to node N3 via transistors 50<sub>2</sub>, 51<sub>2</sub>, and 52<sub>2</sub> charging node N3. The rising voltage at node N3 will eventually turn transistors 50<sub>3</sub> and 52<sub>3</sub> off and 53<sub>3</sub> and 54<sub>3</sub> on, permitting current to flow from node N4 to V<sub>ss</sub> via transistors 53<sub>3</sub>, 54<sub>3</sub>, and 55<sub>3</sub> discharging node N4. The falling voltage at node N4 will eventually turn transistors 50<sub>4</sub> and 52<sub>4</sub> on and 53<sub>4</sub> and 54<sub>4</sub> off, permitting current to flow from V<sub>dd</sub> to node N5 via transistors 50<sub>4</sub>, 51<sub>4</sub>, and 52<sub>4</sub> charging node N5. As node N5 charges it will cause node N1 to discharge to complete one-half cycle.

The current through each of transistors 50-55 in each of inverter stages 48<sub>1</sub>-48<sub>5</sub> is proportional to the width and length of the transistor. Accordingly, the sizes of transistors 50-55 in inverter stages are chosen to provide the desired low and high frequencies f1 and f2.

Although each of inverter stages 48<sub>1</sub>-48<sub>5</sub> is shown as having both transistors 51 and 55, it is understood that dual frequency operation results when only one of transistors 51 and 55 is used in one or more inverter stages.

FIG. 7 shows a multiple frequency oscillator 57 that provides an output signal having more than two selectable frequencies. Oscillator 57 may be used in substrate bias voltage generator 42 of FIG. 4 in place of dual frequency oscillator 44 whenever it is desired to drive charge pump 46 at more than two frequencies. Oscillator 57 is a ring oscillator having an odd number, n, where n is greater than or equal to 3, of cascaded inverter stages 58<sub>1</sub>-58<sub>n</sub>. The outputs of inverter stages 58<sub>1</sub>, 58<sub>2</sub>-58<sub>n</sub>, are connected to the inputs of stages 58<sub>2</sub>-58<sub>n</sub>, and 58<sub>1</sub>, respectively.

Each inverter stage 58 includes parallel-coupled p-channel transistors 60<sub>1</sub>-60<sub>n</sub> having drains connected to a source of positive voltage V<sub>dd</sub> and sources connected to the drain of p-channel transistor 62. Each inverter stage 58 also includes parallel coupled n-channel transistors 66<sub>1</sub>-66<sub>n</sub> having sources connected to V<sub>ss</sub> or ground and drains connected to the source of n-channel transistor 64. The input of each inverter stage 58 is connected to the gates of transistors 62 and 64. The output of each inverter stage 58 is connected between the source of transistor 62 and the drain of transistor 64.

The SELECT1 signal on line 68<sub>1</sub> is applied to the gates of n-channel transistors 66<sub>1</sub> and to the input of inverter 70<sub>1</sub>. Inverter 70<sub>1</sub> applies an inverted SELECT1 signal to the gates of p-channel transistors 60<sub>1</sub>. When the SELECT1 signal is low, transistors 66<sub>1</sub> and 60<sub>1</sub> are

off. When the SELECT1 signal is high, transistors 66<sub>1</sub> and 60<sub>1</sub> are on.

The SELECT2 signal on line 68<sub>2</sub> is applied to the gates of n-channel transistors 66<sub>2</sub> and to the input of inverter 70<sub>2</sub>. Inverter 70<sub>2</sub> applies an inverted SELECT2 signal to the gates of p-channel transistors 60<sub>2</sub>. When the SELECT2 signal is low, transistors 66<sub>2</sub> and 60<sub>2</sub> are off. When the SELECT2 signal is high, transistors 66<sub>2</sub> and 60<sub>2</sub> are on.

The SELECTn signal on line 68<sub>n</sub> is applied to the gates of n-channel transistors 66<sub>n</sub> and to the input of inverter 70<sub>n</sub>. Inverter 70<sub>n</sub> applies an inverted SELECTn signal to the gates of p-channel transistors 60<sub>n</sub>. When the SELECTn signal is low, transistors 66<sub>n</sub> and 60<sub>n</sub> are off. When the SELECTn signal is high, transistors 66<sub>n</sub> and 60<sub>n</sub> are on.

The frequency of oscillation of the output signal on line 59 produced by oscillator 57 is determined by the rates at which nodes N1-Nn charge and discharge. Nodes N1-Nn charge and discharge in a manner similar to nodes N1-N5 of oscillator 44 of FIG. 4. The rate at which each of nodes N1-Nn charges and discharges is directly proportional to the capacitance at that node and the rate at which current flows to and from that node.

The states of the signals SELECT1-SELECTn control which of transistors 60<sub>1</sub>-60<sub>n</sub> and transistors 66<sub>1</sub>-66<sub>n</sub> are conductive or non-conductive to determine the rate at which current flows to or from nodes N1-Nn and thereby the frequency of the output signal produced by oscillator 57 on line 59. At least one of the signals SELECT1-SELECTn must be high during operation of oscillator 57 to provide at least one current path from V<sub>dd</sub> to V<sub>ss</sub> in each of inverter stages 58<sub>1</sub>-58<sub>n</sub> to permit the charging and discharging of nodes N1-Nn. Increasing the number of SELECT signals that are high increases the rate at which current flows to and from nodes N1-Nn to increase the frequency of the output signal on line 59.

Each inverter stage of oscillator 57 could be provided with first and second additional transistors to eliminate the requirement that one of the SELECT1-SELECTn signals be high in order for oscillator 57 to operate. These first and second additional transistors would correspond to transistors 50 and 54 of FIG. 5. The first additional transistor would have a current path connected in parallel with the current paths of transistors 60<sub>1</sub> and a gate connected to the gates of transistors 63 and 64. The second additional transistor would have a current path connected in parallel with the current paths of transistors 66<sub>1</sub> and a gate connected to the gates of transistors 63 and 64.

A few preferred embodiments have been described in detail hereinabove. It is to be understood that the scope of the invention also comprehends embodiments different from those described, yet within the scope of the claims.

For example, bipolar transistors may be used in place of field effect transistors. In addition, implementation is contemplated in discrete components or fully integrated circuits in silicon, gallium arsenide, or other electronic materials families.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon



reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. A multiple frequency oscillator, comprising:
  - a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of said inverter stage outputs supplying an oscillator output signal;
  - at least one of said inverter stages having an input for receiving a control signal, said control signal selectively having a first state or a second state, said at least one inverter stage responsive to said first state to cause said oscillator output signal to have a first frequency and responsive to said second state to cause said oscillator output signal to have a second frequency different from said first frequency, said at least one inverter stage including a plurality of parallel current paths, at least one of said current paths being non-conductive in response to said first state of said control signal and conductive in response to said second state of said control signal.
2. The multiple frequency oscillator of claim 1, in which said at least one current path includes a transistor, said transistor being non-conductive in response to said first state of said control signal and conductive in response to said second state of said control signal.
3. The multiple frequency oscillator of claim 1, in which said at least one inverter stage includes:
  - first and second transistors having current paths connected in parallel;
  - a third transistor having a current path connected in series with the current paths of said first and second transistors between a first voltage source and the output of said at least one inverter stage;
  - a fourth transistor having a current path connected between said inverter stage output and a second voltage source;
  - the input of said at least one inverter stage coupled to control electrodes of said fourth transistor and at least one of said first and third transistors;
  - said second transistor having a control electrode for receiving said control signal, said second transistor being non-conductive in response to said control signal having said first state and conductive in response to said control signal having said second state.
4. A multiple frequency oscillator for use on an integrated circuit selectively operable in a standby mode or an active mode, comprising:
  - a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of said inverter stage outputs supplying an oscillator output signal;
  - at least one of said inverter stages having an input for receiving a control signal, said control signal having a first state in the standby mode or a second state in the active mode, said at least one inverter stage responsive to said first state to cause said oscillator output signal to have a first frequency and responsive to said second state to cause said oscillator output signal to have a second frequency different from said first frequency, said at least one inverter stage including a plurality of transistors having parallel current paths, at least one of said transistors being non-conductive in response to said

- first state of said control signal and conductive in response to said second state of said control signal.
5. A multiple frequency oscillator, comprising:
  - a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of another inverter stage, one of said inverter stage outputs supplying an oscillator output signal;
  - at least one of said inverter stages including:
    - first and second transistors having current paths connected in parallel;
    - a third transistor having a current path connected in series with the current paths of said first and second transistors between a first voltage source and the output of said at least one inverter stage;
    - a fourth transistor having a current path connected between said inverter stage output and a second voltage source;
    - the input of said at least one inverter stage coupled to control electrodes of said fourth transistor and at least one of said first and third transistors;
    - said second transistor having a control electrode for receiving a first control signal having a first state and a second state, said second transistor being non-conductive in response to said first control signal having said first state and conductive in response to said first control signal having said second state.
6. The multiple frequency oscillator of claim 5, in which said first voltage source is a source of ground.
7. The multiple frequency oscillator of claim 5, in which said second voltage source is a source of positive voltage.
8. The multiple frequency oscillator of claim 5, in which there are  $2n+1$  inverter stages, where  $n$  is an integer greater than or equal to 1.
9. The multiple frequency oscillator of claim 5, in which the input of said at least one inverter stage is coupled to the control electrodes of said first and third transistors.
10. The multiple frequency oscillator of claim 5, in which the input of said at least one inverter stage is coupled to the control electrode of said third transistor, the control electrode of said first transistor receiving a second control signal having a first state and a second state, said first transistor being non-conductive in response to said second control signal having said first state and conductive in response to said second control signal having said second state.
11. The multiple frequency oscillator of claim 5, further including fifth and sixth transistors having current paths connected in parallel, said current path of said fourth transistor connected in series with the current paths of said fifth and sixth transistors between said second voltage source and said inverter stage output, said sixth transistor having a control electrode for receiving the complement of said first control signal, said sixth transistor being non-conductive in response to said first control signal having said first state and conductive in response to said first control signal having said second state.
12. The multiple frequency oscillator of claim 11, in which the input of said at least one inverter stage is coupled to control electrodes of said first, third, and fifth transistors.
13. The multiple frequency oscillator of claim 11, in which the input of said at least one inverter stage is coupled to the control electrode of said third transistor,

the control electrode of said first transistor receiving a second control signal having a first state and a second state and a control electrode of said fifth transistor receiving the complement of said second control signal, said first and fifth transistors being non-conductive in response to said second control signal having said first state and conductive in response to said second control signal having said second state.

14. The multiple frequency oscillator of claim 13, further including:

a seventh transistor having a current path coupled in parallel with the current paths of said first and second transistors and a control electrode for receiving a third control signal having a first state and a second state;

an eighth transistor having a current path coupled in parallel with the current paths of said fifth and sixth transistors and a control electrode for receiving the complement of said third control signal, said seventh and eighth transistors being non-conductive in response to said third control signal having said first state and conductive in response to said third control signal having said second state.

15. The multiple frequency oscillator of claim 5, in which said first, second, third, and fourth transistors are field effect transistors.

16. The multiple frequency oscillator of claim 5, in which said first, second, and third transistors are of a first conductivity type and said fourth transistor is of a second conductivity type opposite said first conductivity type.

17. The multiple frequency oscillator of claim 16, in which said first, second, and third transistors are n-channel transistors and said fourth transistors is a p-channel transistor.

18. The multiple frequency oscillator of claim 5, in which said oscillator output signal has a first frequency when said first control signal has said first state and a second frequency when said first control signal has said second state, said first frequency being less than said second frequency.

19. A voltage generator for supplying a bias voltage to a node in an integrated circuit, comprising:

a multiple frequency oscillator for producing an output signal having a frequency selected in response to at least one control signal; and

a charge pump responsive to said output signal for supplying said bias voltage to said node;

said multiple frequency oscillator including:

a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of said inverter stage outputs supplying said output signal;

at least one of said inverter stages having an input for receiving said control signal, said control signal selectively having a first state or a second state, said at least one inverter stage responsive to said first state to cause said output signal to have a first frequency and responsive to said second state to cause said output signal to have a second frequency different from said first frequency, said at least one inverter stage including a plurality of parallel current paths, at least one of said current paths being non-conductive in response to said first state of said control signal and conductive in response to said second state of said control signal.

20. The voltage generator of claim 19, in which said control signal has said first state when said integrated circuit operates in a standby mode and said second state when said integrated circuit operates in a standby mode and said second state when said integrated circuit operates in an active mode.

21. The voltage generator of claim 19, in which said at least one current path includes a transistor, said transistor being non-conductive in response to said first state of said control signal and conductive in response to said second state of said control signal.

22. The voltage generator of claim 19, in which said at least one inverter stage includes:

first and second transistors having current paths connected in parallel;

a third transistor having a current path connected in series with the current paths of said first and second transistors between a first voltage source and the output of said at least one inverter stage;

a fourth transistor having a current path connected between said inverter stage output and a second voltage source;

the input of said at least one inverter stage coupled to control electrodes of said fourth transistor and at least one of said first and third transistors;

said second transistor having a control electrode for receiving said control signal, said second transistor being non-conductive in response to said control signal having said first state and conductive in response to said control signal having said second state.

23. A multiple frequency oscillator, comprising:

a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of said inverter stage outputs supplying an oscillator output signal;

at least one of said inverter stages having a frequency control circuit connected between a first voltage source and the output of said at least one inverter stage, said frequency control circuit receiving a first control signal selectively having a first state or a second state, said frequency control circuit having a first resistance in response to said first state to cause said oscillator output signal to have a first frequency and having a second resistance less than said first resistance in response to said second state to cause said oscillator output signal to have a second frequency greater than said first frequency;

said at least one inverter stage including:

a first transistor having a current path connected in parallel with said frequency control circuit;

a second transistor having a current path connected in series with the current path of said first transistor between said first voltage source and the output of said at least one inverter stage;

a third transistor having a current path connected between the output of said at least one inverter stage and a second voltage source;

the input of said at least one inverter stage coupled to control electrodes of said third transistor and at least one of said first and second transistors.

24. The multiple frequency oscillator of claim 23, in which said frequency control circuit includes a fourth transistor having a current path connected in parallel with the current path of said first transistor and a control electrode for receiving said first control signal, said fourth transistor being non-conductive in response to

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said first control signal having said first state and conductive in response to said first control signal having said second state.

25. The multiple frequency oscillator of claim 23, in which the input of said at least one inverter stage is coupled to the control electrodes of said first and second transistors.

26. The multiple frequency oscillator of claim 23, in which the control electrode of said first transistor receives a second control signal selectively having a first state or a second state, said first transistor being non-conductive in response to said second control signal having said first state and conductive in response to said second control signal having said second state.

27. The multiple frequency oscillator of claim 23, in which said first voltage source is a source of ground.

28. The multiple frequency oscillator of claim 23, in which said first voltage source is a source of positive voltage.

29. A multiple frequency oscillator, comprising:  
a plurality of inverter stages, each inverter stage including an input and an output, the input of each inverter stage coupled to the output of at least one other inverter stage, one of said inverter stage outputs supplying an oscillator output signal;

at least one of said inverter stages receiving a first control signal, said first control signal selectively having a first state or a second state, said at least one inverter stage responsive to said first state to cause said oscillator output signal to have a first frequency and responsive to said second state to cause said oscillator output signal to have a second frequency different from said first frequency, the input of said at least one inverter stage remaining at a substantially constant capacitance irrespective of the state of said first control signal, said at least one inverter stage including a frequency control circuit connected between a first voltage source and the output of said at least one inverter stage, said frequency control circuit receiving said first control signal, said frequency control circuit having a first resistance in response to said first state to cause said oscillator output signal to have a first frequency

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and having a second resistance less than said first resistance in response to said second state to cause said oscillator output signal to have a second frequency greater than said first frequency;

said at least one inverter stage including:

a first transistor having a current path connected in parallel with said frequency control circuit;

a second transistor having a current path connected in series with the current path of said first transistor between said first voltage source and the output of said at least one inverter stage;

a third transistor having a current path connected between the output of said at least one inverter stage and a second voltage source;

the input of said at least one inverter stage coupled to control electrodes of said third transistor and at least one of said first and second transistors.

30. The multiple frequency oscillator of claim 29, in which said frequency control circuit includes a fourth transistor having a current path connected in parallel with the current path of said first transistor and a control electrode for receiving said first control signal, said fourth transistor being non-conductive in response to said first control signal having said first state and conductive in response to said first control signal having said second state.

31. The multiple frequency oscillator of claim 29, in which the input of said at least one inverter stage is coupled to the control electrodes of said first and second transistors.

32. The multiple frequency oscillator of claim 29, in which the control electrode of said first transistor receives a second control signal selectively having a first state or a second state, said first transistor being non-conductive in response to said second control signal having said first state and conductive in response to said second control signal having said second state.

33. The multiple frequency oscillator of claim 29, in which said first voltage source is a source of ground.

34. The multiple frequency oscillator of claim 29, in which said first voltage source is a source of positive voltage.

\* \* \* \* \*

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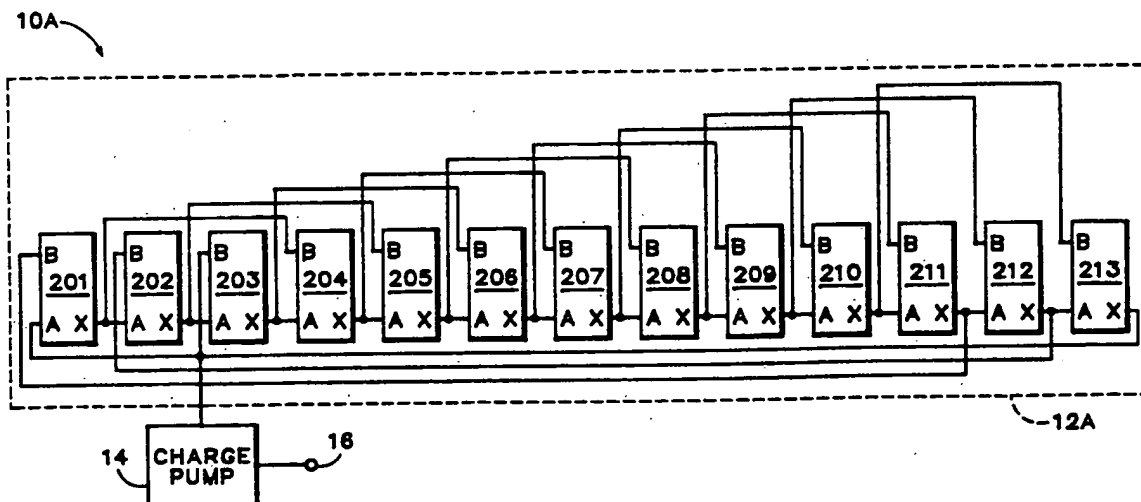
**United States Patent** [19][11] **Patent Number:** **5,182,529****Chern**[45] **Date of Patent:** **Jan. 26, 1993****[54] ZERO CROSSING-CURRENT RING OSCILLATOR FOR SUBSTRATE CHARGE PUMP****[75] Inventor:** Wen-Foo Chern, Colorado Springs, Colo.**[73] Assignee:** Micron Technology, Inc., Boise, Id.**[21] Appl. No.:** 847,331**[22] Filed:** Mar. 6, 1992**[51] Int. Cl.<sup>5</sup> .....** H03P 5/02; H03K 3/354**[52] U.S. Cl. ....** 331/57; 307/296.2**[58] Field of Search ....** 331/57, DIG. 3; 307/296.2**[56] References Cited****U.S. PATENT DOCUMENTS**

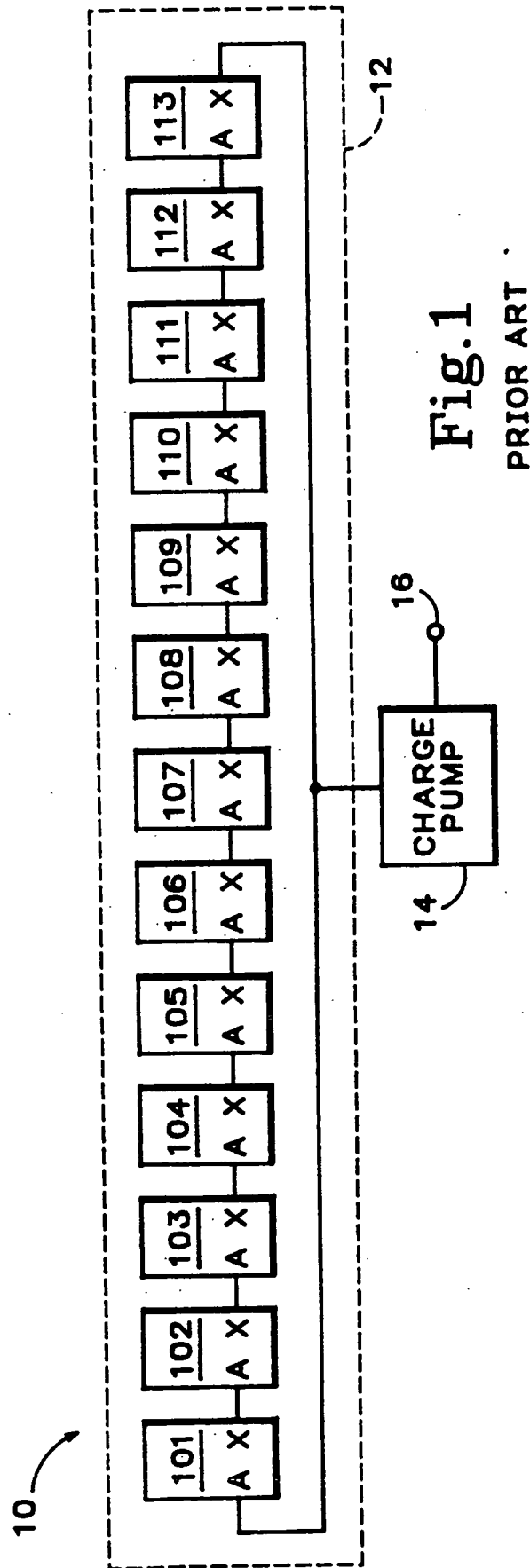
3,350,659 10/1967 Henn ..... 331/57

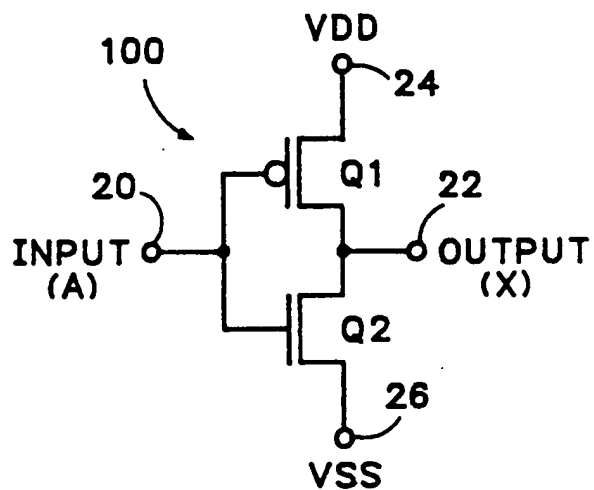
4,705,966 11/1987 Van Zanten ..... 307/296.2

*Primary Examiner*—Siegfried H. Grimm*Attorney, Agent, or Firm*—Marger, Johnson, McCollom & Stolowitz**[57] ABSTRACT**

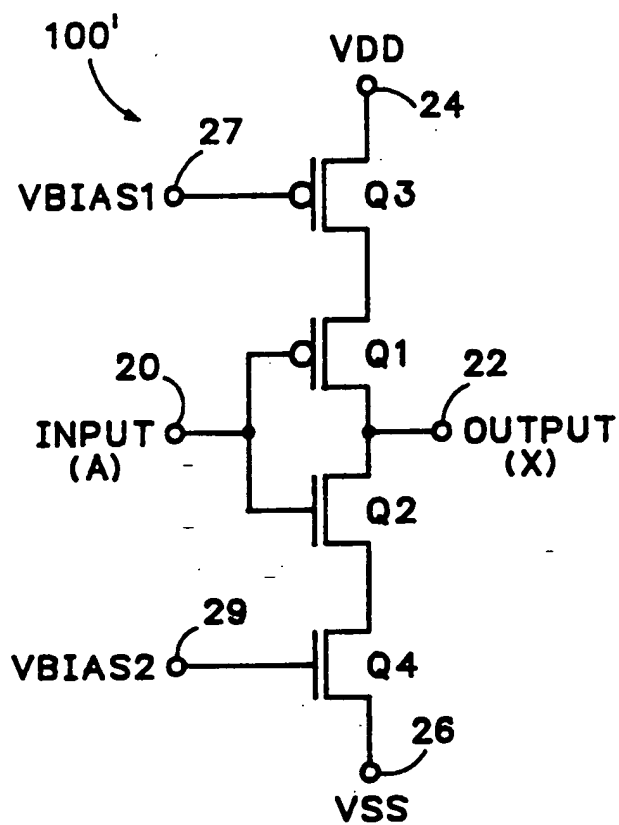
A ring oscillator for use with a charge pump includes an odd number of inverter stages each having a primary input, a secondary input, and an output. Both inputs are switched to the same logic state to invert the logic signal at the output of the inverter stage. No crossing-current flows within the inverter stage if the inputs have different logic states. The output of each inverter stage is coupled to the primary input of a following inverter stage in a serially-connected ring fashion. The output of a last inverter stage is coupled to the primary input of a first inverter stage and forms an oscillating signal output, which is coupled to the charge pump. The secondary input of each stage is coupled to the output of a preceding inverter stage. The preceding inverter precedes the current inverter by an odd integer greater or equal to three. The ring oscillator includes a transistor coupled to the output of each inverter stage for impressing a initial pattern of alternating logic levels to begin the oscillation.

**20 Claims, 7 Drawing Sheets**



**Fig. 2**

PRIOR ART

**Fig. 3**

PRIOR ART

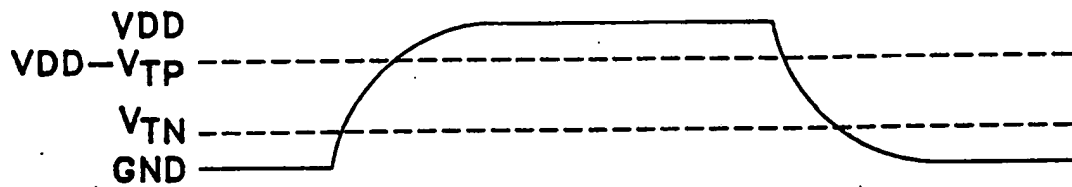


Fig. 4  
PRIOR ART

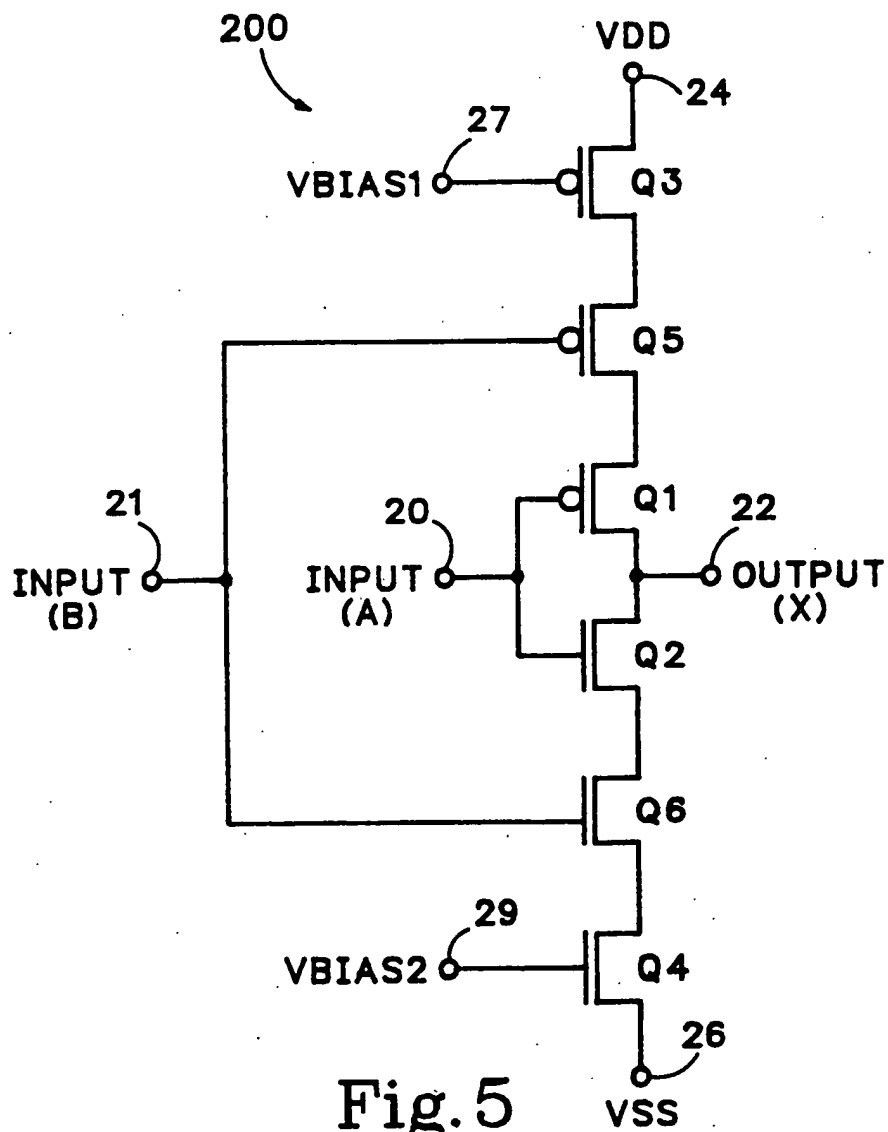


Fig. 5

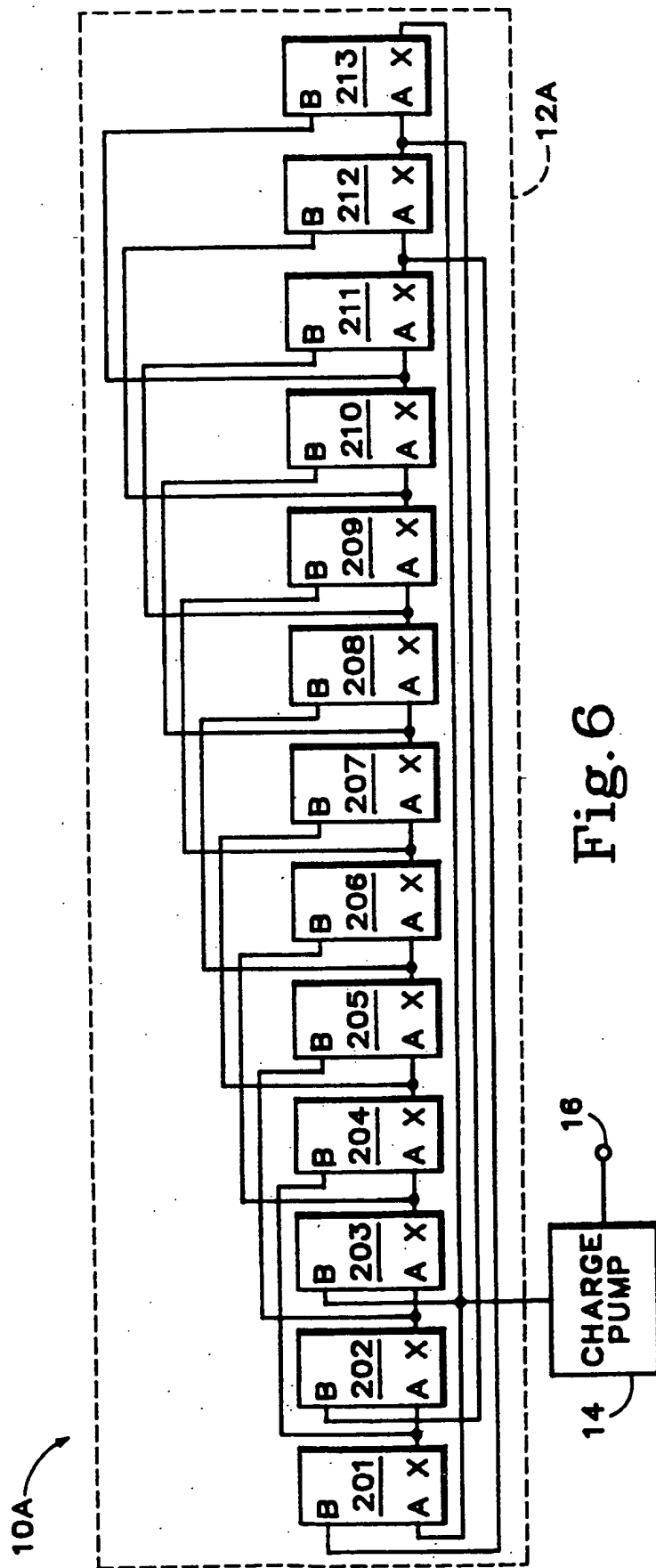
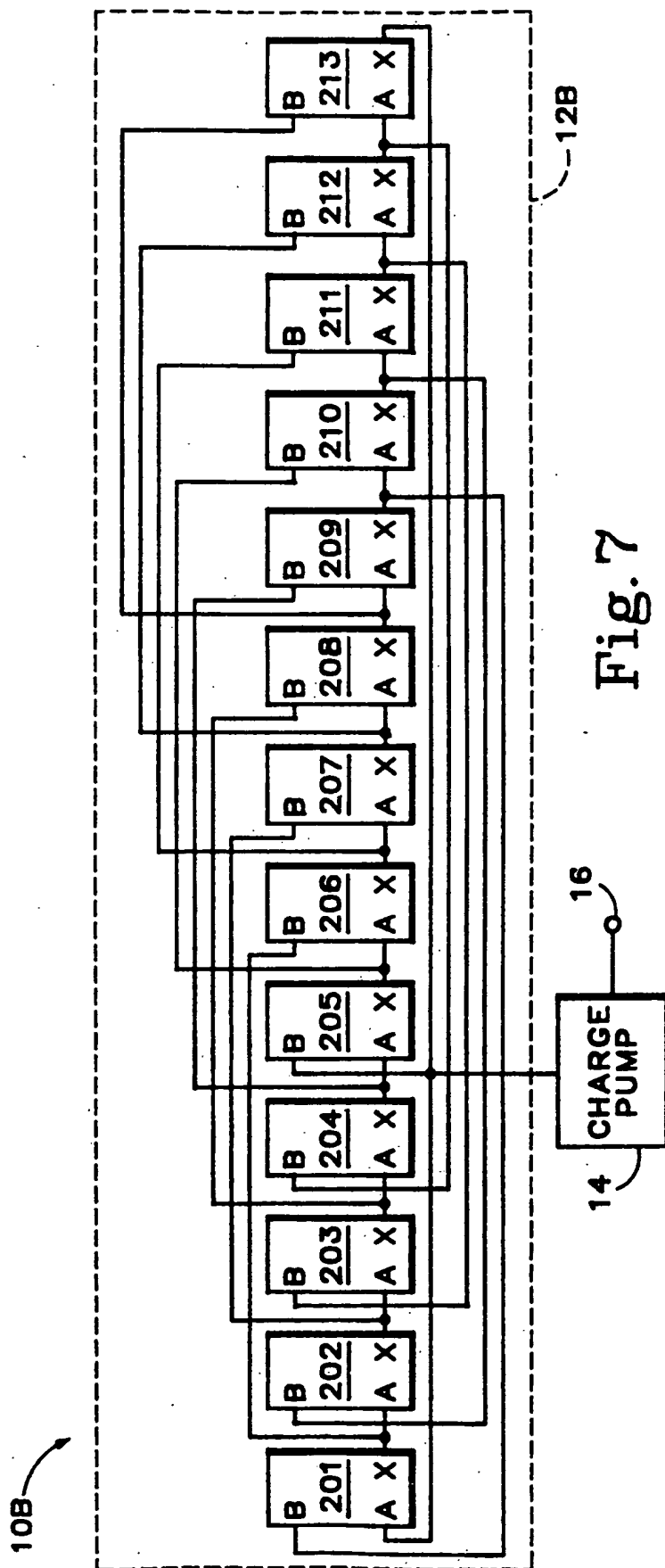
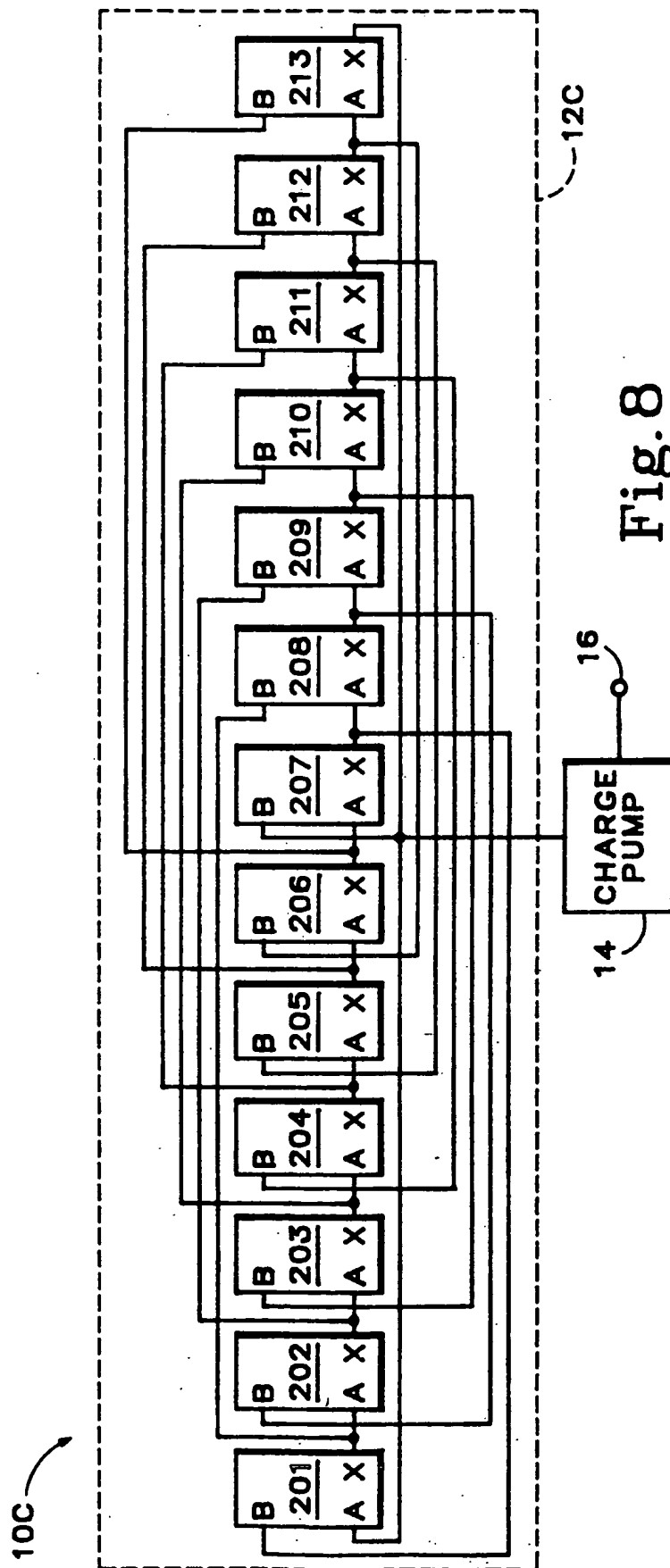


Fig. 6







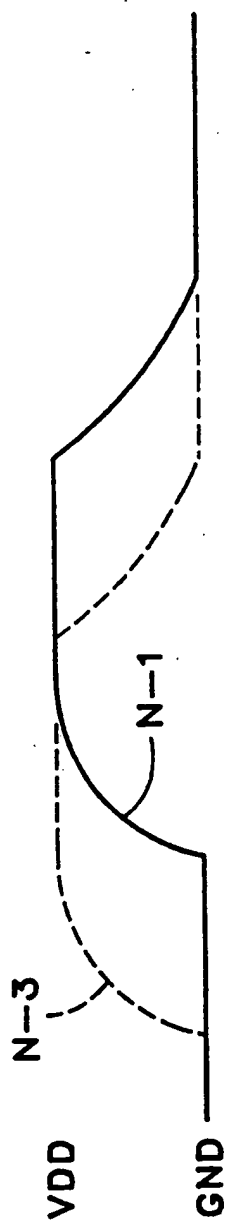


Fig. 9

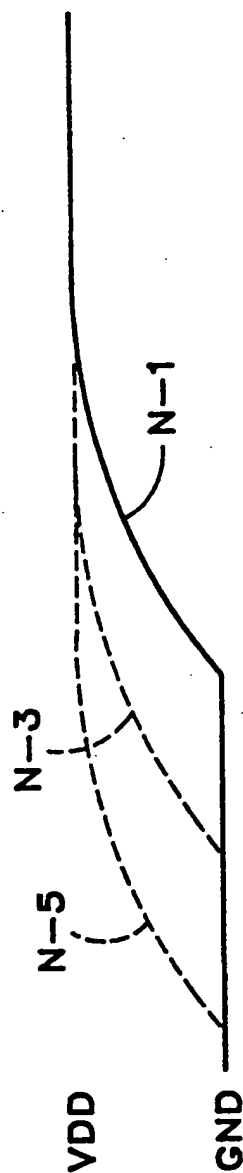


Fig. 10

## ZERO CROSSING-CURRENT RING OSCILLATOR FOR SUBSTRATE CHARGE PUMP

### BACKGROUND OF THE INVENTION

This invention relates generally to charge pumps for maintaining a constant voltage bias on the substrate of an integrated circuit, and, more particularly, to a substrate pump having reduced power requirements by eliminating the crossing-current in the gates of the ring oscillator used in conjunction with the charge pump.

A typical charge pump system 10 is shown in FIG. 1, including a ring oscillator 12 for providing a square-wave oscillating signal to a charge pump 14. The charge pump 14, which is coupled between a positive supply voltage and ground, usually includes two diodes and a capacitor for converting the square-wave oscillating signal into a negative voltage, although other more sophisticated circuits exist. The negative voltage is provided at output 16 for driving the substrate of an integrated circuit in the absence of an external source of negative supply voltage. In the alternative, substrate pump 14 is sometimes configured to provide a voltage higher than the most positive supply voltage for driving isolated wells on the integrated circuit. The ring oscillator 12 includes an odd number of inverter stages 101-113 arranged in a serially-connected ring fashion. Thirteen inverter stages are shown in FIG. 1, but the exact number can be any odd number depending upon the delay through each stage and the desired oscillating frequency. The "X" output of each inverter is coupled to the "A" input of a succeeding inverter in the ring. The output of the last inverter 113 is coupled to the input of the first inverter 101 to form the oscillating output, which is in turn coupled to the input of the charge pump 14.

A typical prior art inverter stage 100 is shown in the schematic diagram of FIG. 2. Inverter stage 100 includes a P-channel transistor Q1 and an N-channel transistor Q2. The gates of transistors Q1 and Q2 are coupled together to form the A input at node 20 and the drain of transistors Q1 and Q2 are coupled together to form the inverted X output at node 22. Power for the inverter is supplied by a source of positive voltage VDD, usually five volts, at node 24. Node 24 is also the source of transistor Q1. The source of transistor Q2 is coupled to ground or a second voltage source VSS at node 26. The exact values of the power supplies VDD and VSS are determined by the level of logic swings required and the physical dimensions of the transistors, among other factors.

Another prior art inverter stage 100' is shown in the schematic diagram of FIG. 3. Inverter stage 100' again includes P-channel transistor Q1 and an N-channel transistor Q2, and in the same configuration, except for the source connections. The source of transistor Q1 is coupled through an additional P-channel load transistor Q3 to VDD, while the source of transistor Q2 is coupled through an additional N-channel load transistor to VSS. The extra transistors of inverter stage 100' enable the designer to adjust channel dimensions for minimum parasitic output capacitance at node 22. For example, the channel length of transistors Q3 and Q4 can be made quite large, minimizing power requirements and decreasing inverter gain. The channel width and length of transistors Q1 and Q2 can be made quite small to minimize parasitic drain capacitance. Transistor Q3 is biased on with bias voltage VBIAS1 at node 27, while transi-

tor Q4 is biased on with bias voltage VBIAS2 at node 29.

Inverters 100 and 100' both exhibit undesirable "crossing-current". This term refers to the characteristic of the inverter whereby current flows directly from VDD to VSS through the transistors Q1-Q2 or Q1-Q4 during an edge transition of the input signal. Referring now to FIG. 4, a portion of the square-wave oscillating signal is shown having GND and VDD logic levels. The oscillating signal and operation of the inverters are divided into three zones. If the input signal is less than the threshold voltage  $V_{TN}$  of transistor Q2, current is directed from VDD through output node 22 into the load and transistor Q1 is off. If the input signal is greater than VDD minus the threshold voltage  $V_{TP}$  of transistor Q1, current is directed from the load through output node 22 to VSS and transistor Q2 is off. If the input signal is between  $V_{TN}$  and  $VDD - V_{TP}$ , transistors Q1 and Q2 are both on, and an undesirable crossing-current component flows from VDD to VSS. The current, which can be made small in a single inverter, is nonetheless significant if multiplied by the number of inverters required in the ring oscillator 12. The total current, multiplied by the difference in voltage between the VDD and VSS power supplies, represents a significant amount of wasted power consumption in the charge pump system 10.

Accordingly, a need remains for a charge pump system in which the power consumption due to crossing-current in the inverter stages of the ring oscillator is minimized or even eliminated.

### SUMMARY OF THE INVENTION

It is, therefore, a principal object of the invention to conserve power consumption in charge pump systems.

It is a further object of the invention to provide a novel low-power ring oscillator configuration.

According to the present invention, a ring oscillator for use with a charge pump includes an odd number of inverter stages each having a primary input, a secondary input, and an output. Both inputs are switched to the same logic state to invert the logic signal at the output of the inverter stage. No crossing-current flows within the inverter stage if the inputs have different logic states. The output of each inverter stage is coupled to the primary input of a following inverter stage in a serially-connected ring fashion. The output of a last inverter stage is coupled to the primary input of a first inverter stage and forms an oscillating signal output, which is coupled to the charge pump. The secondary input of each stage is coupled to the output of a preceding inverter stage. The preceding inverter precedes the current inverter by an odd integer greater or equal to three. The ring oscillator includes a transistor coupled to the output of each inverter stage for impressing an initial pattern of alternating logic levels to begin the oscillation.

In the preferred embodiment, each inverter stage includes first and second P-channel transistors and first and second N-channel transistors coupled in series between first and second sources of supply voltage. The gates of the first P-channel and N-channel transistors are coupled together to form the primary input, and the drains of the first P-channel and N-channel transistors being coupled together to form the output. The gates of the second P-channel and N-channel transistors are coupled together to form the secondary input. If de-

sired, the inverter further can include high channel resistance first and second transistor loads. The resistance of each transistor load is determined through the use of appropriate gate bias voltages.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified block diagram of a prior art charge pump system including a ring oscillator and a charge pump.

FIGS. 2-3 are schematic diagrams of prior art inverters used in the ring oscillator of FIG. 1.

FIG. 4 illustrates the oscillating waveform provided by the ring oscillator of FIG. 1.

FIG. 5 is a schematic diagram of an inverter for use in a ring oscillator according to the present invention.

FIGS. 6-8 are block diagrams of three embodiments of charge pump systems according to the present invention.

FIG. 9 illustrates the oscillating waveforms provided by the charge pump system shown in FIG. 6.

FIG. 10 illustrates the oscillating waveforms provided by the charge pump system shown in FIG. 7.

#### DETAILED DESCRIPTION

Referring now to FIG. 5, an inverter stage 200 used in the ring oscillator of the present invention inverts the logic signal at the output node 22 if both the primary and secondary inputs 20 and 21 are switched from a first logic state to a second logic state. The inverter stage 200 inhibits crossing-current (current flow between VDD and VSS) if the primary and secondary inputs 20 and 21 are at different logic states. In operation, if inverter 200 is switched from a condition wherein the primary and secondary inputs are at different logic states to a condition wherein the primary and secondary inputs are at the same logic state, current can only flow into or out of the load, and no zero crossing current flows within the inverter.

Inverter stage 200 includes a first P-channel transistor Q1 and a first N-channel transistor Q2. The gates of the first P-channel and N-channel transistors Q1 and Q2 are coupled together to form the primary "A" input at node 20. The drains of the first P-channel and N-channel transistors Q1 and Q2 are coupled together to form the "X" output at node 22. A second P-channel transistor Q5 has a drain coupled to the source of the first P-channel transistor Q1, and a source coupled (through P-channel load transistor Q3) to the supply voltage VDD. A second N-channel transistor Q6 has a drain coupled to the source of the first N-channel transistor Q2, and a source coupled (through N-channel load transistor Q4) to the supply voltage VSS. The gates of the second P-channel and N-channel transistors Q5 and Q6 are coupled together to form the secondary "B" input at node 21.

The P-channel load transistor Q3 is optional, but is desirable for decreasing the gain of inverter stage 200. Decreasing the gain of the inverter stage 200 allows the oscillating frequency of the ring oscillator 12 to slow down without an excessive capacitive load, which would increase operating current. Load transistor Q3 has a source coupled to VDD, a drain coupled to the source of the second P-channel transistor Q5, and a gate

coupled to a first source of bias voltage VBIAS1. The value of the first bias voltage is set to  $VDD - V_{TP} + \Delta$ , wherein  $V_{TP}$  is the threshold voltage of the load P-channel transistor Q3, and  $\Delta$  is a predetermined incremental voltage. The incremental voltage is set to slightly bias load transistor Q3 to a high-resistance (low current) operating point. Similarly, the N-channel load transistor Q4 is optional but desirable for decreasing inverter gain. Load transistor Q4 has a source coupled to VSS, a drain coupled to the source of the second N-channel transistor Q6, and a gate coupled to a second source of bias voltage VBIAS2. The value of the second bias voltage is set to  $VSS + V_{TN} + \Delta$ , wherein  $V_{TN}$  is the threshold voltage of the load N-channel transistor Q4, and  $\Delta$  is a predetermined incremental voltage. The incremental voltage is set to bias load transistor Q4 at the high-resistance operating point, which need not necessarily be the same as for load transistor Q3.

For normal CMOS logic levels, the value of the first source of supply voltage, VDD, is about five volts and the value of the second source of supply voltage, VSS, is about zero volts. These values can change, especially if high-density, sub-micron transistor geometries are used. For example, if submicron geometries are used, VDD is typically set to 3.3 volts to reduce electric field. Other values of VDD and VSS can be used to accommodate non-standard CMOS logic levels. Depending upon the application, VDD can have a range of voltage between two and six volts.

A first embodiment of a ring oscillator 12A for use in a charge pump system 10A is shown in FIG. 6. Ring oscillator 12A includes an odd number of inverter stages 201-213 each having a primary A input, a secondary B input, and an X output. Thirteen inverter stages are shown in FIG. 6, but any odd number can be used. The X output of each inverter stage 201-213 is coupled to the primary A input of a following inverter stage in a serially-connected ring fashion. The X output of the last inverter stage 213 is coupled to the primary A input of the first inverter stage 201, which forms an oscillating signal output coupled to charge pump 14. The output 16 of charge pump 14 provides the negative bias voltage for biasing the substrate of an integrated circuit containing the charge pump system 10A. The secondary B input of each inverter stage 201-213 is coupled to the X output of an Mth preceding inverter stage, wherein M is an odd integer greater or equal to three. In the ring oscillator 12A of FIG. 6, M is equal to three. Thus, the secondary B input of inverter stage 208 is coupled to the X output of inverter stage 205. Similarly, the secondary B input of inverter stage 207 is coupled to the X output of inverter stage 204. Since the inverter stages 201-213 are coupled in a ring fashion, all inverter stages are similarly coupled. For example the secondary B input of inverter stage 201 is coupled to the X output of inverter stage 211.

The operation of ring oscillator 12A is best seen in FIG. 9. The solid waveform is the square wave formed by the ring oscillator. The N-1 waveform represents the wavefront at an (N-1)th inverter stage output (primary A input to an Nth inverter stage) and the N-3 waveform represent the wavefront at an (N-3)th inverter stage output (secondary B input to the Nth inverter stage). Recalling the operation of an inverter stage 200 described previously and shown in FIG. 5, when the N-3 waveform (B input) is at a logic high level and the N-1 waveform (A input) is at a logic low level, there is no current flow within the inverter stage.

When the N-3 and N-1 waveforms have both reached the logic high level, current flows from the output into N-channel transistors Q2 and Q6 from the load (the input of the succeeding inverter stage), and the output of the inverter changes logic state. However, P-channel transistors Q1 and Q5 are both off and therefore no undesirable crossing-current can flow from VDD to VSS.

An alternative embodiment, ring oscillator 12B is shown in FIG. 7 in which M is equal to five. The secondary B input of inverter stage 208 is coupled to the X output of inverter stage 203. Similarly, the secondary B input of inverter stage 207 is coupled to the X output of inverter stage 202. As in the previous embodiment, inverter stages 201-213 are coupled in a ring fashion, and therefore all inverter stages are similarly coupled. Thus, the secondary B input of inverter stage 201 is coupled to the X output of inverter stage 209.

The operation of ring oscillator 12B is best seen in FIG. 10. The N-1 waveform represents the wavefront at an (N-1)th inverter stage output (primary A input to an Nth inverter stage) and the N-5 waveform represents the wavefront at an (N-5)th inverter stage output (secondary B input to the Nth inverter stage). The N-3 waveform represents the wavefront at an (N-3)th inverter stage output that is not coupled in any way to the current or Nth inverter stage. When the N-5 waveform (B input) is at a logic high level and the N-1 waveform (A input) is at a logic low level, there is no current flow within the inverter stage. When the N-5 and N-1 waveforms have both reached the logic high level, current flows from the output into N-channel transistors Q2 and Q6 from the load, and the output of the inverter changes logic state. As in the previous embodiment, P-channel transistors Q1 and Q5 are both off and no undesirable crossing-current can flow from VDD to VSS.

The embodiment of FIG. 7 is desirable for ring oscillators having long rise and fall times on the leading and trailing edges of the oscillating output waveform. Referring again to FIG. 10, it can be seen that the N-3 waveform is not appropriate for switching the Nth inverter stage. If the N-3 waveform is used, a period of time will exist wherein all transistors in the inverter stage are biased on, leading to undesirable crossing-current similar to that described in conjunction with the prior art inverter stages 100 and 100' shown in FIGS. 2 and 3. Note that the N-5 waveform is at a logic high level prior to the point at which the N-1 waveform begins to switch. No period of time exists in which all inverter stage transistors are biased on and therefore no crossing-current can flow.

The above operation can be further extended depending upon the rise and fall time of the ring oscillator. For example, a ring oscillator 10C in which M is equal to seven is shown in FIG. 8. The secondary B input of inverter stage 209 is coupled to the X output of inverter stage 202. Similarly, the secondary B input of inverter stage 208 is coupled to the X output of inverter stage 201. As in the previous embodiment, inverter stages 201-213 are coupled in a ring fashion, and therefore all inverter stages are similarly coupled. The secondary B input of inverter stage 201 is coupled to the X output of inverter stage 207. The operation of ring oscillator 10C is very similar to that of ring oscillators 10A and 10B described above, and whose output waveforms are shown in FIGS. 9 and 10. The only difference is that it may be desirable to use ring oscillator 10C in those cases

where the oscillating waveform has extremely long rise and fall times due to the nature of the devices used, parasitic capacitance, and other factors. In the final analysis, the exact configuration of the ring oscillator should be tailored to the characteristics of the oscillating output waveform. The rise and fall time can be measured and a corresponding odd M number selected for proper A and B input timing such that no crossing-current can flow.

The operation of ring oscillators 10A-10C has proceeded with an analysis of the rise time. It is apparent to those skilled in the art that the analysis of the fall time portion of the waveform is very similar and need not be explicitly conducted. The same elimination of zero crossing current occurs during the fall time of the oscillating output waveform.

It is desirable to include in ring oscillators 10A-10C means for providing initial voltage conditions at the output of each of the inverter stages 201-213. A single P-channel or N-channel transistor can be coupled between each output and ground or VDD. An initial pattern of alternating logic levels is then loaded at the gates of each transistor, and therefore correspondingly at the outputs of the inverter stages. Once the pattern is established, the transistors are turned off and the ring oscillator can be activated. Other initial condition patterns can be used, and other means for establishing those patterns can also be used.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it is apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles.

I therefore claim all modifications and variation coming within the spirit and scope of the following claims:

1. A ring oscillator for use in a charge pump comprising N inverter stages each having a primary input, a secondary input, and an output, wherein N is an odd integer,

the output of each inverter stage is coupled to the primary input of a following inverter stage in a serially-connected ring fashion such that the output of a last inverter stage is coupled to the primary input of a first inverter stage and forms an oscillating signal output, and

the secondary input of each stage is coupled to the output of an Mth preceding inverter stage, wherein M is an odd integer greater or equal to three.

2. A ring oscillator as in claim 1 in which M is equal to three.

3. A ring oscillator as in claim 1 in which M is equal to five.

4. A ring oscillator as in claim 1 in which M is equal to seven.

5. A ring oscillator as in claim 1 further comprising means for providing initial voltage conditions at the output of each of the inverter stages.

6. A ring oscillator as in claim 1 further comprising means for impressing an initial pattern of alternating logic levels at the outputs of the inverter stages.

7. A ring oscillator as in claim 1 in which each inverter stage comprises:

means for inverting the logic signal at the output if both the primary and secondary inputs are switched from a first logic state to a second logic state; and

means for inhibiting zero crossing current if the primary and secondary inputs are at different logic states.

8. A ring oscillator as in claim 1 in which each inverter stage comprises:

a first P-channel transistor having a gate, a drain, and a source;

a first N-channel transistor having a gate, a drain, and a source, the gates of the first P-channel and N-channel transistors being coupled together to form the primary input, and the drains of the first P-channel and N-channel transistors being coupled together to form the output;

a second P-channel transistor having a gate, a drain coupled to, the source of the first P-channel transistor, and a source coupled to a first source of supply voltage;

a second N-channel transistor having a gate, a drain coupled to the source of the first N-channel transistor; and a source coupled to a second source of supply voltage, the gates of the second P-channel and N-channel transistors being coupled together to form the secondary input.

9. A ring oscillator as in claim 8 in which the inverter further comprises:

a first load interposed between the source of the second P-channel transistor and the first source of supply voltage; and

a second load interposed between the source of the second N-channel transistor and the second source of supply voltage.

10. A ring oscillator as in claim 9 in which the first load comprises a third P-channel transistor having a source coupled to the first source of supply voltage, a drain coupled to the source of the second P-channel transistor, and a gate coupled to a first source of bias voltage.

11. A ring oscillator as in claim 10 in which the value of the first bias voltage is set to  $V_{DD} - V_{TP} + \Delta$ , wherein  $V_{DD}$  is the value of the first source of supply voltage,  $V_{TP}$  is the threshold voltage of the third P-channel transistor, and  $\Delta$  is a predetermined incremental voltage.

12. A ring oscillator as in claim 9 in which the second load comprises a third N-channel transistor having a source coupled to the second source of supply voltage, a drain coupled to the source of the second N-channel transistor, and a gate coupled to a second source of bias voltage.

13. A ring oscillator as in claim 12 in which the value of the second bias voltage is set to  $V_{SS} + V_{TN} + \Delta$ , wherein  $V_{SS}$  is the value of the second source of supply voltage,  $V_{TN}$  is the threshold voltage of the third N-channel transistor, and  $\Delta$  is a predetermined incremental voltage.

14. A ring oscillator as in claim 8 in which the value of the first source of supply voltage ranges from about two volts to six volts and the value of the second source of supply voltage is about zero volts.

15. A method of generating an oscillating signal that minimizes power consumption due to zero-crossing current, the method comprising the steps of:

providing a ring oscillator for use in a charge pump including N inverter stages each having a primary input, a secondary input, and an output, wherein N is an odd integer;

coupling the output of each inverter stage to the primary input of a following inverter stage in a serially-connected ring fashion;

coupling the output of a last inverter stage to the primary input of a first inverter stage to form an output for generating the oscillating signal; and

coupling the secondary input of each stage to the output of an Mth preceding inverter stage, wherein M is an odd integer greater or equal to three.

16. The method of claim 15 further comprising the step of setting M equal to three.

17. The method of claim 15 further comprising the step of setting M equal to five.

18. The method of claim 15 further comprising the step of setting M equal to seven.

19. The method of claim 15 further comprising the step of providing initial voltage conditions at the output of each of the inverter stages.

20. The method of claim 15 further comprising the step of impressing an initial pattern of alternating logic levels at the outputs of the inverter stages.

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**Adverse Decisions In Interference**

Patent No. 5,182,529, Wen-Foo Chern, ZERO CROSSING-CURRENT RING OSCILLATOR FOR SUBSTRATE CHARGE PUMP, Interference No. 104,624, final judgment adverse to the patentee rendered January 7, 2002, as to claims 1-20.

*(Official Gazette February 12, 2002)*



### [54] HIGH FREQUENCY CMOS VCO WITH GAIN CONSTANT AND DUTY CYCLE COMPENSATION

[75] Inventor: Richard R. Rasmussen, Fremont, Calif.

[73] Assignee: National Semiconductor Corporation, Santa Clara, Calif.

[21] Appl. No.: 642,677

[22] Filed: Jan. 17, 1991

[51] Int. Cl.<sup>3</sup> ..... H03B 1/00

[52] U.S. Cl. .... 331/57; 331/108 B

[58] Field of Search ..... 331/57, 108 A, 108 B, 331/177 R; 307/448

### [56] References Cited

#### U.S. PATENT DOCUMENTS

4,876,519 10/1989 Davis et al. .... 331/57

#### OTHER PUBLICATIONS

Ware et al., "A 200 MHz CMOS Phase-Locked Loop with Dual Phase Detectors", IEEE Transactions on Solid State Circuits, May 10, 1989.

Yousefi, "14 MHz-100 MHz CMOS L Based Frequency Synthesizer IC".

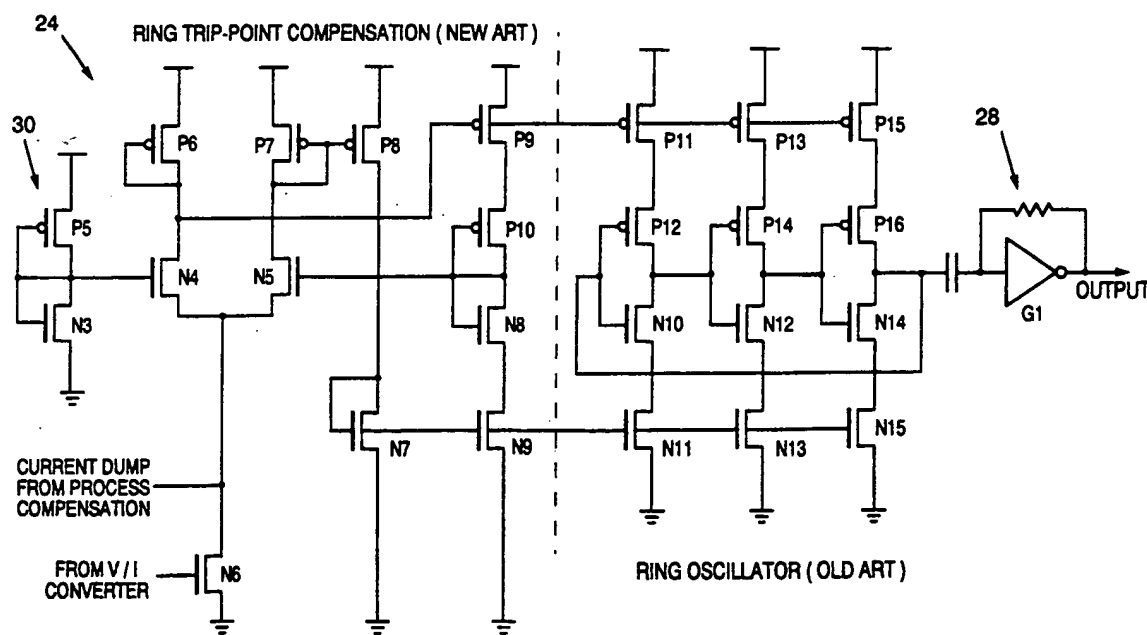
Primary Examiner—Robert J. Pascal

Attorney, Agent, or Firm—Limbach, Limbach & Sutton

### [57] ABSTRACT

The present invention provides a high frequency CMOS voltage controlled oscillator circuit with gain constant and duty cycle compensation. The voltage controlled oscillator circuit includes a multi-stage ring oscillator that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors. The ring oscillator responds to a control current signal for controlling the frequency of oscillation of the ring oscillator. A voltage-to-current converter converts a tuning voltage input signal to a corresponding output current signal that is independent of the channel strength of the N-channel and P-channel transistors. Process compensation circuitry responds to the tuning voltage input signal to provide a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors. Trip-point compensation circuit provides a net ring current signal as the current control signal to the ring oscillator. The net ring current signal represents the difference between the output current signal and the current dump output signal and responds to the balance between the output buffer trip point and a ring oscillator dummy stage.

4 Claims, 8 Drawing Sheets



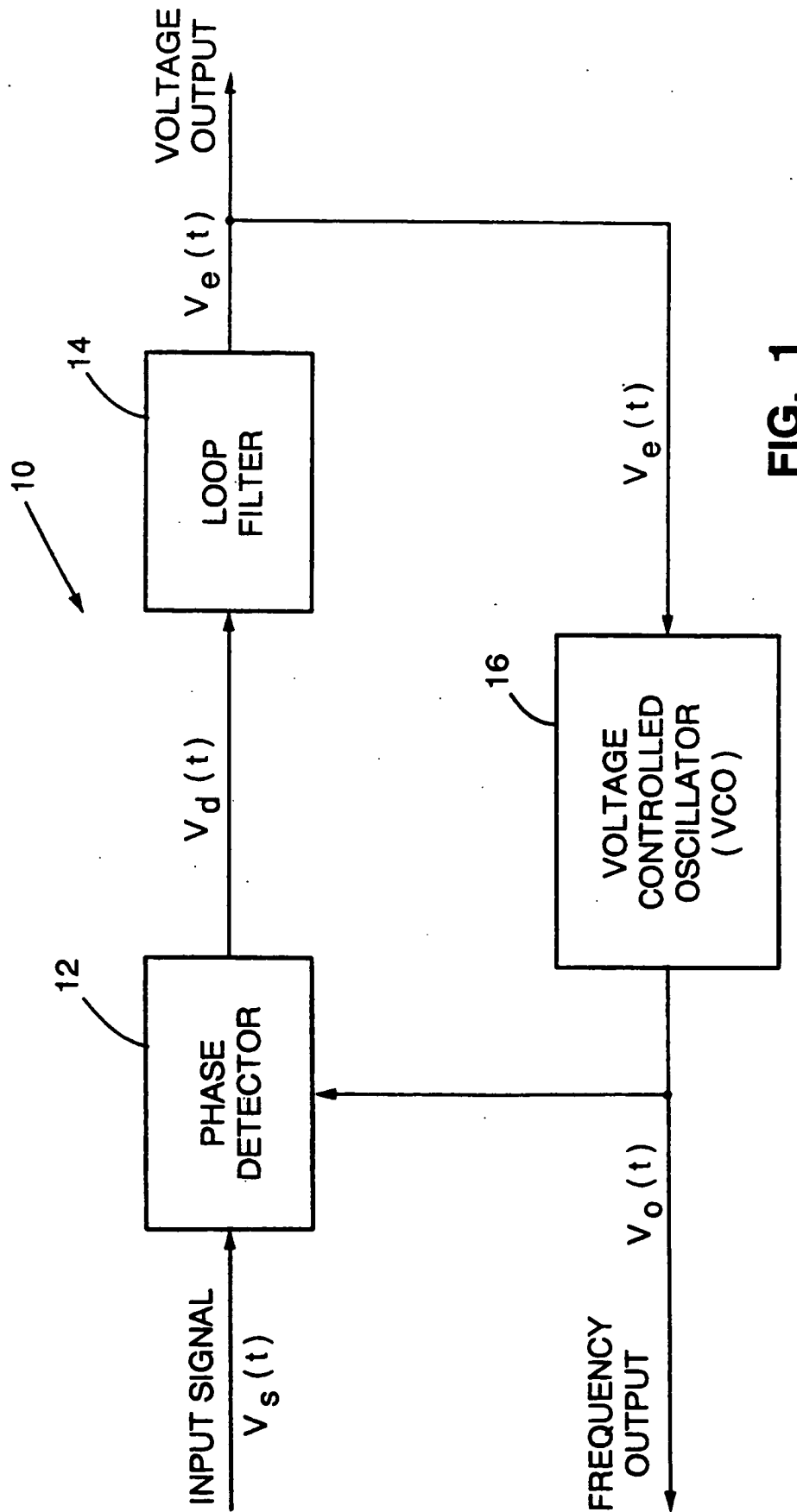


FIG. 1

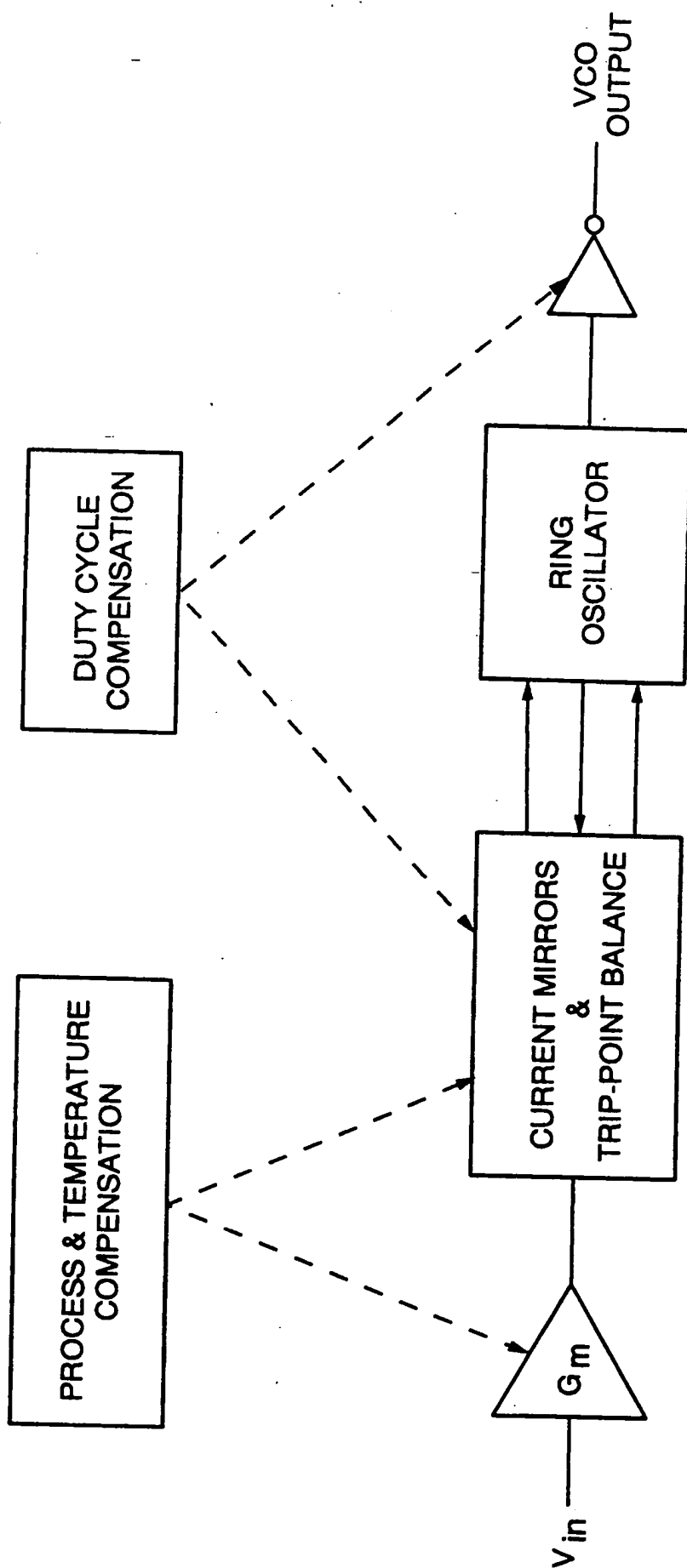


FIG. 2

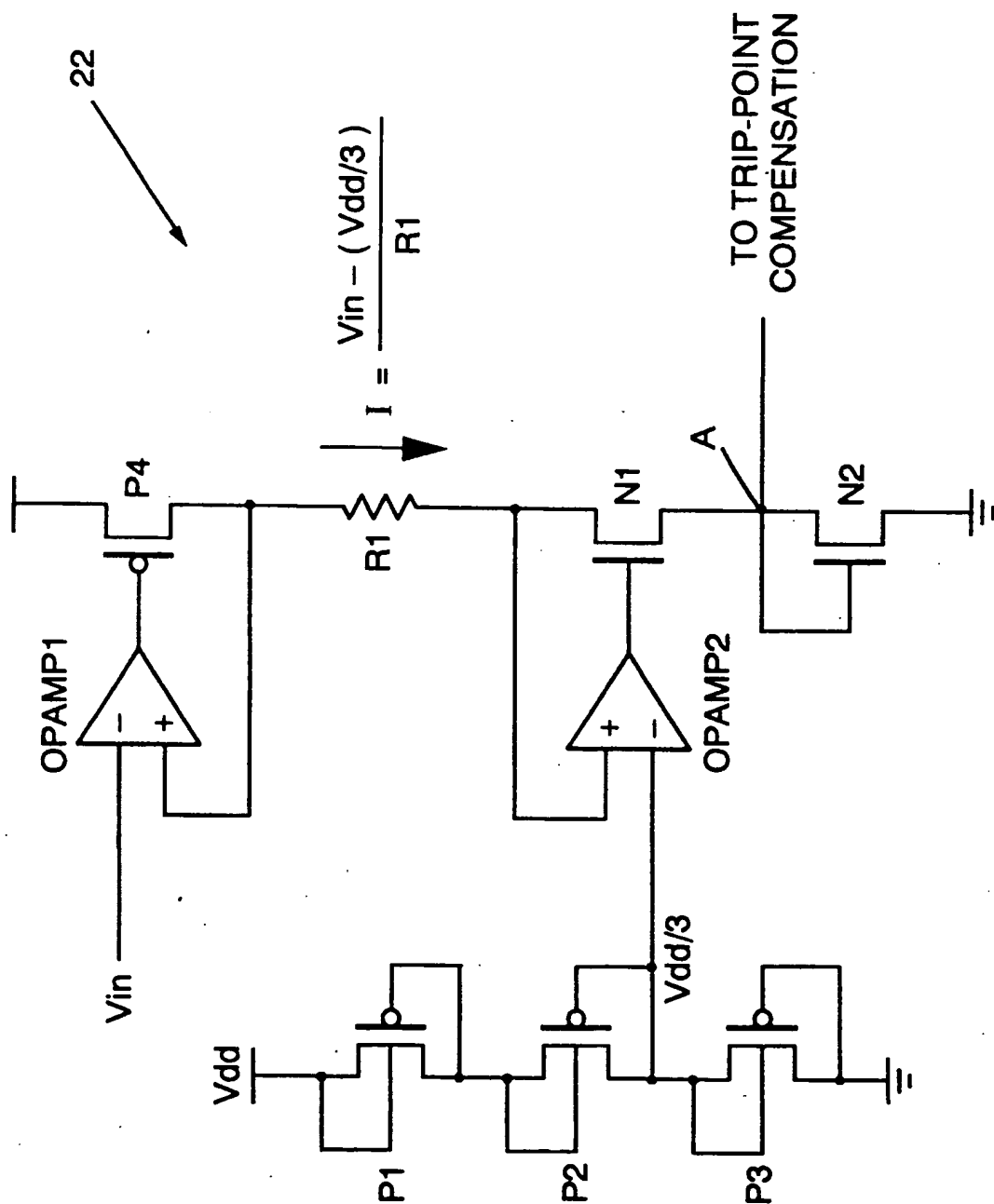
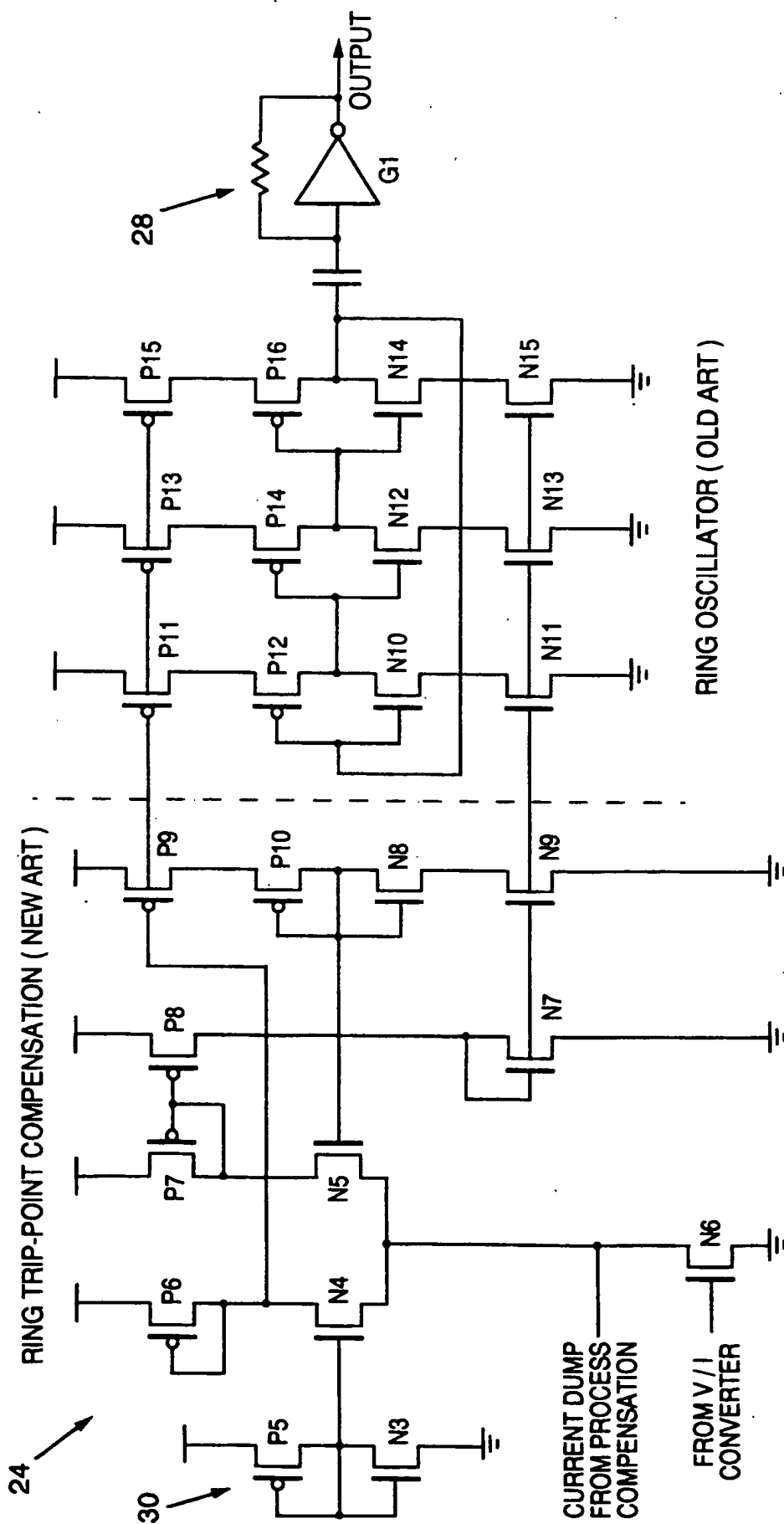
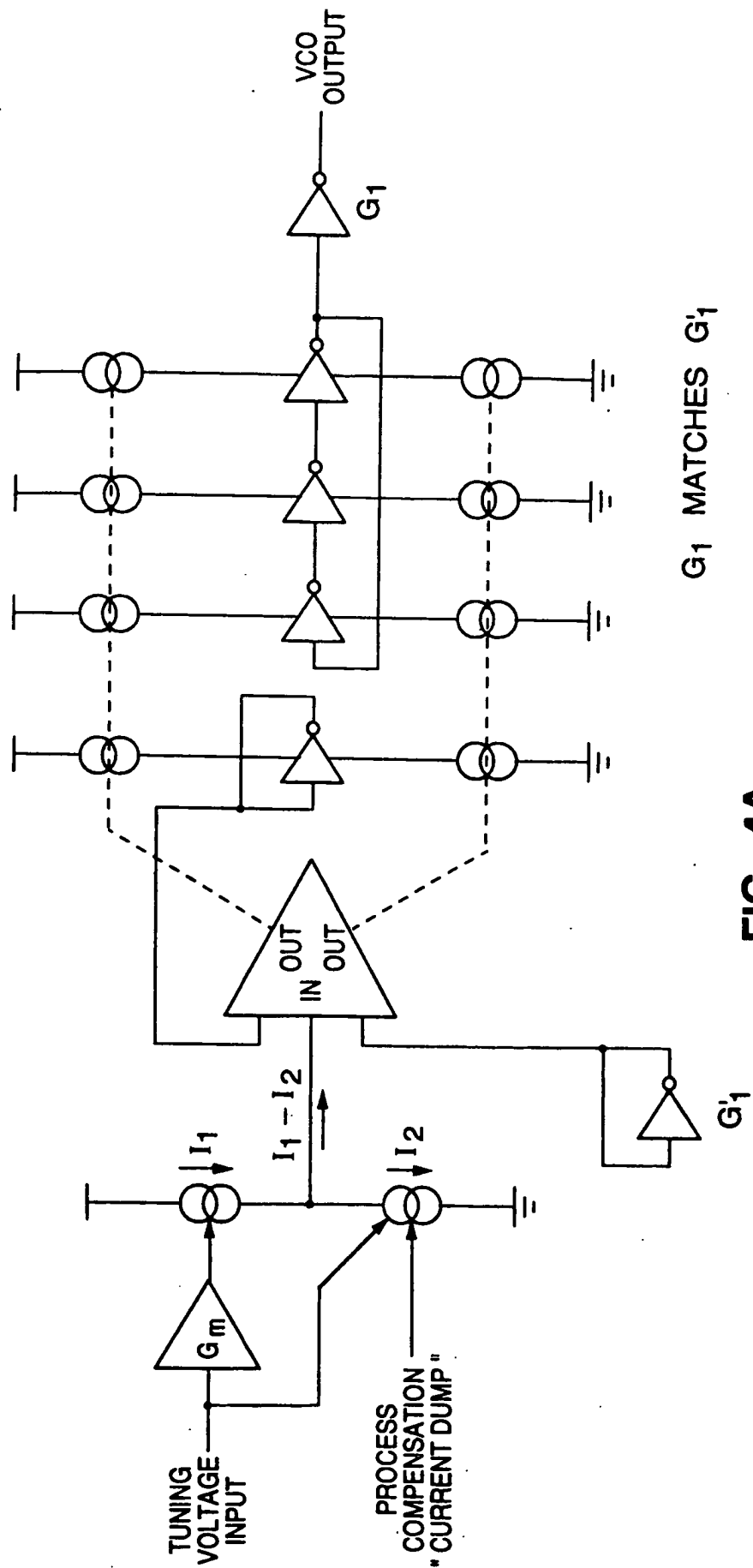


FIG. 3





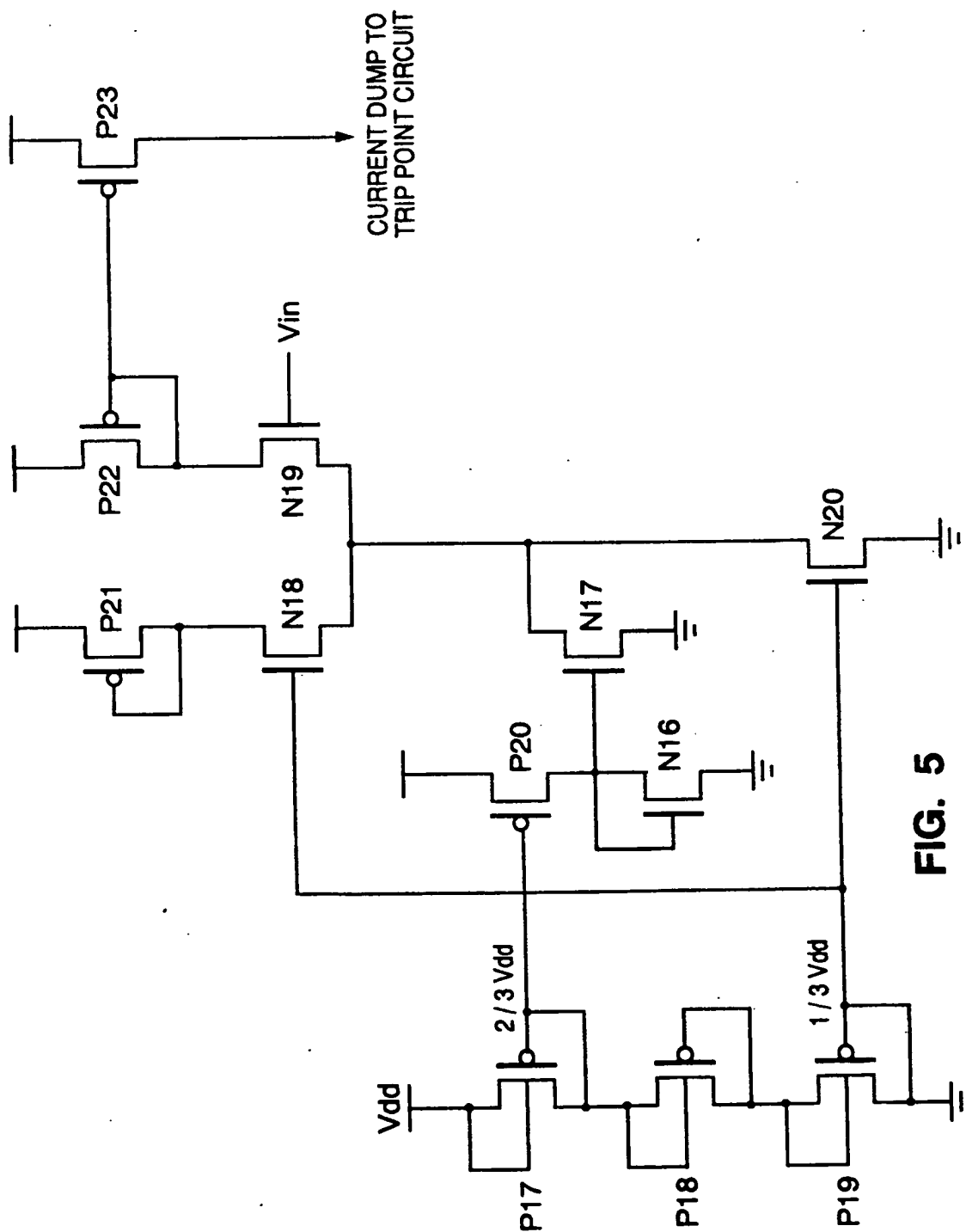


FIG. 5

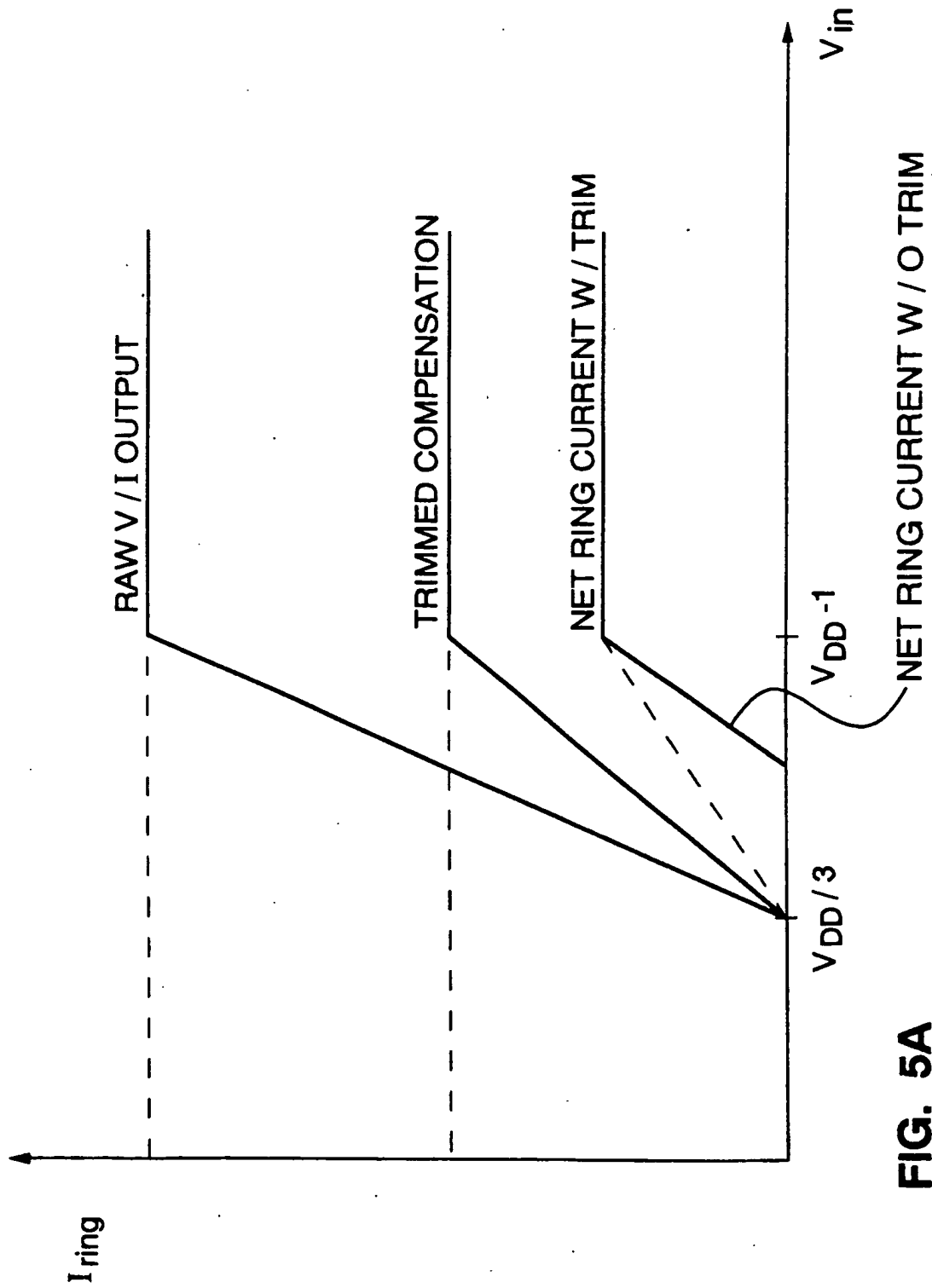
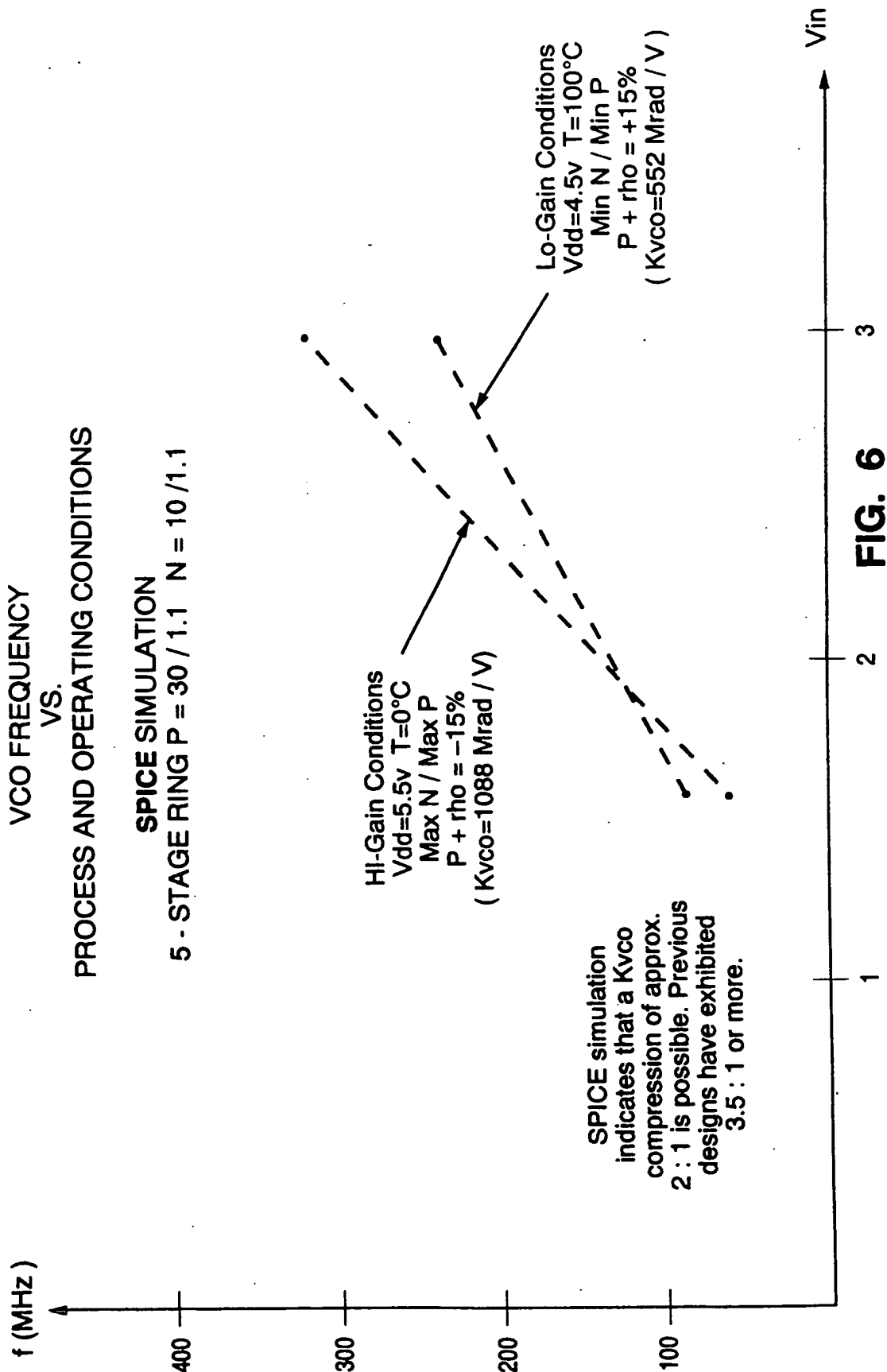


FIG. 5A





# HIGH FREQUENCY CMOS VCO WITH GAIN CONSTANT AND DUTY CYCLE COMPENSATION

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to voltage-controlled oscillators and, in particular, to methods and apparatus for obtaining a variable clock frequency having a well-controlled output range and duty cycle over varying temperature, process and supply voltage.

### 2. Discussion of the Prior Art

As shown in FIG. 1, a basic phase-locked loop (PLL) system 10 includes three essential elements—a phase detector 12, a loop filter 14 and a voltage-controlled oscillator (VCO) 16—interconnected to form a feedback system. The phase detector 12 compares the phase of the input signal  $V_d(t)$  with the output frequency  $V_o(t)$  of the VCO 16 and generates an error voltage  $V_e(t)$  corresponding to the difference. The error voltage signal  $V_e(t)$  is then filtered by the loop filter 14 and applied to the control terminal of the VCO 16 in the form of an error voltage  $V_c(t)$  to control its frequency of oscillation.

The VCO 16 is the most critical element of the PLL system 10. The tuning slope, that is, the output frequency  $V_o(t)$  dependence on control voltage  $V_c(t)$ , is determined by the conversion gain constant  $K_{VCO}$  of the VCO 16. Similarly, the linearity of the voltage-to-frequency conversion characteristics of the PLL system 10 is determined solely by the limitations of the control characteristics of the VCO 16. Thus, the stability and control characteristics of the VCO 16 are key design parameters in monolithic PLL circuits.

The VCO 16, which is basically an analog circuit, must be immune to on-chip and off-chip noise sources. If it is not, then its output  $V_o(t)$  will exhibit short-term frequency instability, or jitter. Maintaining a low VCO gain constant  $K_{VCO}$  is one method of reducing noise sensitivity. The required operating frequency for conventional VCOs ranges from a few MHz to beyond 200 MHz. Tuning ranges up to 2 to 1 are also required. To be easily compatible with 5 V power supply constraints and minimum phase detector/charge pump solutions, the tuning voltage should be approximately 1.5 V to ( $V_{cc} - 1.5$  V).

As stated above, the VCO gain constant  $K_{VCO}$  must be well controlled so that loop filtering schemes are predictable and stable. This is especially important in data acquisition and mass storage applications such as disk controllers and constant density recording. At higher output frequencies, the duty cycle is also critical.

In many applications, the process of choice for VCO design has been complementary-metal-oxide-semiconductor (CMOS) technology. However, previous CMOS VCO designs have been greatly affected by process variations, which can cause large changes in the VCO gain constant  $K_{VCO}$ , and/or have required external trimming components. External trimming adds pins and cost to the PLL chip and provides an antenna through which noise can be coupled into the sensitive analog sections of the chip.

One example of a high frequency CMOS phase-locked loop is described by Ware et al, "a 200 MHz CMOS Phase-Lock-Loop with Dual Phase Detectors", IEEE Transactions on Solid State Circuits, May 10, 1989. The Ware et al PLL features a VCO that requires the use of a bandgap regulator that relies on parasitic

NPN transistors. It achieves frequency control by varying the applied voltage across the ring oscillator stages. The VCO utilized by Ware is based on a ring of three inverting amplifiers.

Yousefi, "14 MHz-100 MHz CMOS PLL Based Frequency Synthesizer IC", describes a PLL design where the VCO gain constant compensation depends upon the use of an external resistor.

U.S. Pat. No. 4,876,519, issued on Oct. 24, 1989 to Craig M. Davis and Richard R. Rasmussen, and commonly assigned herewith, discloses a PLL implementation in emitter-coupled-logic (ECL) technology. Although the Davis/Rasmussen design provides significant advantages, its Bipolar/CMOS process requirement prohibits its use in some applications.

It would, therefore, be desirable to have available a CMOS-based PLL that features good VCO frequency control, gain control and duty-cycle characteristics without using external components.

## SUMMARY OF THE INVENTION

The present invention provides a high frequency CMOS voltage controlled oscillator circuit with gain constant and duty cycle compensation. The voltage controlled oscillator circuit includes a multi-stage ring oscillator that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors. The ring oscillator responds to a control current signal for controlling the frequency of oscillation of the ring oscillator. A voltage-to-current converter converts a tuning voltage input signal to a corresponding output current signal that is independent of the channel strength of the N-channel and P-channel transistors. Process compensation circuitry responds to the tuning voltage input signal to provide a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors. Trip-point compensation circuit provides a net ring current signal as the current control signal to the ring oscillator. The net ring current signal represents the difference between the output current signal and the current dump output signal.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings which set forth an illustrative embodiment in which the foregoing features of the invention are utilized.

## DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the basic elements of a conventional phase-locked loop (PLL).

FIG. 2 is a block diagram illustrating an embodiment of voltage-controlled oscillator (VCO) in accordance with the present invention.

FIG. 3 is a schematic diagram illustrating an embodiment of a V/I converter utilizable in the VCO shown in FIG. 2.

FIG. 4 is a schematic diagram illustrating an embodiment of ring trip-point compensation circuitry together with a conventional ring oscillator utilizable in the VCO shown in FIG. 2.

FIG. 4A is a schematic diagram illustrating a generalized representation of the FIG. 4 circuit.

FIG. 5 is a schematic diagram illustrating an embodiment of process compensation circuitry utilizable in the VCO shown in FIG. 2.

FIG. 5A is a plot of control current to the ring oscillator versus tuning voltage.

FIG. 6 is a graph illustrating VCO frequency versus process and operating conditions for a VCO in accordance with the present invention.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a block diagram of a CMOS voltage-controlled oscillator (VCO) 20 with gain constant and duty cycle compensation in accordance with the present invention.

VCO 20 includes a voltage-to-current V/I converter 22 with gain  $G_m$  that amplifies input signal  $V_{in}$  to current mirror and trip-point compensation circuitry 24. The outputs of the trip-point compensation circuitry 24 are provided to a CMOS ring oscillator 26. The selected phase signal of the ring oscillator 26 is provided as the VCO output via an output buffer 28.

In accordance with the present invention, the VCO 20 includes process and temperature compensation for the V/I converter 22 and process compensation for the trip-point circuitry 24. Duty cycle compensation for both the trip-point balance circuitry 24 and the output buffer 28 is derived from matching devices within these two circuit elements.

An embodiment of a V/I converter 22 utilizable in the VCO 20 is shown in greater detail in FIG. 3.

In the FIG. 3 V/I converter circuit 22, tuning voltage input signal  $V_{in}$  is provided to the inverting input of operational amplifier OPAMP1. The non-inverting input of op amp OPAMP1 is connected to the drain of P-channel transistor P4 which is driven by the output of op amp OPAMP1. A second operational amplifier OPAMP2 drives N-channel sense transistor N1, which has its source connected to an output node A. The non-inverting input of op amp OPAMP2 is connected to the drain of P-channel sense transistor P4 via internal current control resistor R1. The inverting input of op amp OPAMP2 is connected to receive a  $V_{DD}$  driver stage output, the driver stage comprising three series-connected, P-channel transistors P1, P2 and P3 which are connected between a supply voltage  $V_{DD}$  and ground. An N-channel output mirror transistor N2 is connected between the output node A and ground.

Thus, the output current at node A of the V/I converter 22 is controlled by forcing the bottom side of resistor R1 to  $V_{DD}/3$  and the top side of resistor R1 to  $V_{in}$ . The output current is, therefore,

$$I = \frac{V_{in} - (V_{DD}/3)}{R1}$$

and is relatively independent of supply  $V_{DD}$  and its only process sensitivity is the tolerance of the internal resistor R1. The transconductance slope is totally independent of supply  $V_{DD}$ .

Resistor R1 can also be an external component for even greater accuracy. In this case, both external connections are floating above ground and external noise can be made common-mode.

The current at node A is then mirrored into the ring oscillator 26, as described below.

An embodiment of current mirror and ring trip-point compensation circuitry 24 is shown in greater detail in FIG. 4.

Trip-point compensation is desirable in order to maintain symmetric VCO output waveforms as the process

varies. For example, when the process tends toward weak N-channel and strong P-channel transistors, the resultant VCO output waveform will have a higher duty cycle than when the N-channel and P-channel transistor strengths are well matched.

The FIG. 4 circuit includes a differential stage, comprising N-channel transistors N4 and N5, that allows the total ring oscillator current from the V/I converter 22 to be shared as process shift demands. That is, as the P-channel transistors of the VCO get weaker because of process variation, the self-biased inverter (transistors P10 and N8) voltage in the FIG. 4 circuit will tend to drop, forcing more current to be steered through input transistor N4 and then mirrored from P-channel transistor P6 to P-channel current sensing transistors P9, P11, P13 and P15. Similarly, when the N-channel transistors get weaker, more current is steered through P-channel input transistor P7 and mirrored into transistors P8 and N7 and current sensing transistors N9, N11, N13 and N15.

As further shown in FIG. 4, the ring trip-point compensation circuitry includes a dummy inverter stage (transistors P10 and N8) that is identical in form to the three inverter stages (P12/N10, P14/N12 and P16/N14) of the ring oscillator.

The ring oscillator is a standard design having an output frequency equal to  $1/6T$ , where T is the propagation delay of an inverter (P12/N10, P14/N12, P16/N14).

From the above description, those skilled in the art will recognize that the FIG. 4 circuitry can be more generally illustrated as shown in FIG. 4A. That is, as shown in FIG. 4A, the amplified V/I converter control input received from buffer  $G_m$  drives a first current I1. The current dump from the process compensation circuitry drives a second current source I2. The net ring oscillator current equals the V/I current I1 minus the process compensation current I2.

As shown in FIG. 4, the compensation circuit 24 uses a self-biased inverter 30 comprising P-channel transistor P5 and N-channel transistor N3 to drive the ring oscillator bias such that the resultant oscillation is also matched with the output buffer G1. Output buffer G1 amplifies and squares the ring oscillator signal.

An embodiment of process compensation circuitry is shown in detail in FIG. 5.

The process compensation circuit maintains a constant frequency tuning range over process variations such as transistor threshold voltage, transconductance and source/drain capacitance. It also compensates for externally induced variations, such as temperature and supply voltage  $V_{DD}$ .

As shown in FIG. 5, a  $V_{DD}$  voltage splitter stage consisting of P-channel transistors P17, P18 and P19 sets up a  $V_{DD}$ -dependent gate bias on P-channel transistor P20 and N-channel transistor N20. As P-channel strength increases, the currents in N-channel sensing transistors N16 and N17 increase proportionally. Likewise, as N-channel strength increases, the current in N-channel sensing transistor N20 increases. The P-channel and N-channel strength-dependent currents sum to become the tail current in the differential stage comprising N-channel transistors N18 and N19, which is part of a  $K_{VCO}$  compression network. Thus, as the tuning voltage  $V_{in}$  applied to input transistor N19 increases, so does the current in P-channel transistor P22 and P-channel mirror transistor P23. This current

dumps into the trip-point compensation circuit 24 and effectively "steals" current away from the ring oscillator, thereby maintaining a constant output frequency. Since the "stolen" current is proportional to the tuning voltage  $V_{in}$ , the VCO gain constant  $K_{VCO}$  is further compressed.

This concept is further illustrated in the FIG. 5A plot of control current  $I_{ring}$  to the ring oscillator versus tuning voltage  $V_{in}$ . As shown in FIG. 5A, the current  $I_{ring}$  supplied by the V/I converter circuit (FIG. 3) rises from zero When  $V_{in}$  equals  $V_{DD}/3$ , the slope of the curve being dependent on the value of resistor  $R_I$ . As stated above, as process strength varies, the slope of the V/I converter output remains constant. Thus, without current trimming, the net ring current will not be process dependent. With current trimming provided in accordance with the present invention, ring current  $I_{ring}$  is controlled over a widened range of tuning voltages  $V_{IN}$ .

FIG. 6 provides a plot of VCO frequency versus process and operating conditions based on a SPICE simulation of the concepts of the invention described above for a 5 V integrated circuit under worst case operating conditions. The simulation indicates that VCO gain constant ( $K_{VCO}$ ) compression of approximately 2:1 is possible. Conventional VCO designs exhibit gain constant compression of 3.5:1 or more.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that methods and apparatus within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. A voltage controlled oscillator circuit comprising:
  - (a) multi-stage ring oscillator means that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors, the ring oscillator means responsive to a control current signal for controlling the frequency of oscillation of the ring oscillator means; and
  - (b) voltage-to-current converter means for converting a tuning voltage input signal to a corresponding output signal that is independent of the channel strength of the N-channel and P-channel transistors;
  - (c) process compensation means responsive to the tuning voltage input signal for providing a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors; and
  - (d) trip-point compensation means responsive to the output signal and the current dump output signal to provide a net ring current signal as the control current signal to the ring oscillator means, the net ring current signal representing the difference be-

tween the output signal and the current dump output signal and responding to the balance between the output buffer's input threshold and a ring inverter dummy stage.

2. A voltage controlled oscillator circuit as in claim 1 wherein the voltage-to-current converter means comprises:

- (a) supply voltage divider means connected between a supply voltage and ground for providing a voltage driver output signal;
- (b) a first operational amplifier that receives the tuning voltage input signal at its inverting input;
- (c) a second operational amplifier that receives the voltage driver output signal at its inverting input;
- (d) a P-channel sense transistor having its gate connected to receive the output signal of the first operational amplifier, its source connected to the supply voltage and its drain connected both to the non-inverting input of the first operational amplifier and to the first side of a current control resistor;
- (e) a N-channel sense transistor having its gate connected to receive the output signal of the second operational amplifier, its drain connected both to the non-inverting input of the second operational amplifier and to the second side of the current control resistor, and its source connected to an output node that provides the output current signal; and
- (f) a N-channel output mirror transistor having its drain and gate commonly connected to the output node and its source connected to ground.

3. A voltage controlled oscillator circuit as in claim 1 wherein the process compensation means comprises:

- (a) supply voltage splitter means connected between the supply voltage and ground for generating first and second bias voltage output signals;
- (b) channel strength sensing means responsive to the first and second bias voltage output signals for providing a tail current signal; and
- (c) gain constant compression means responsive to the tail current and to the tuning voltage input signal for providing current dump output signal corresponding to the tuning voltage input signal.

4. A voltage controlled oscillator circuit as in claim 1 wherein the trip-point compensation means comprises:

- (a) current steering means for steering the control current signal to the ring oscillator means depending upon the channel strength of the N-channel and P-channel transistors;
- (b) an input node for providing the current dump output signal as tail current to the current steering means; and
- (c) a N-channel transistor connected between the input node and ground for providing the current input to the ring oscillator.

\* \* \* \* \*

[54] DEPLETION-MODE FET FOR THE REGULATION OF THE ON-CHIP GENERATED SUBSTRATE BIAS VOLTAGE

[75] Inventor: Deepraj S. Puar, Sunnyvale, Calif.

[73] Assignee: Signetics Corporation, Sunnyvale, Calif.

[21] Appl. No.: 258,156

[22] Filed: Apr. 27, 1981

[51] Int. Cl.<sup>4</sup> ..... H03L 5/00

[52] U.S. Cl. .... 307/297; 307/296 R; 307/200 B

[58] Field of Search ..... 307/297, 296 A, 296 R, 307/304, 200 B; 323/313

## [56] References Cited

### U.S. PATENT DOCUMENTS

4,004,164	1/1977	Cranford, Jr. et al.	307/297
4,115,710	9/1978	Lou	307/297 X
4,142,114	2/1979	Green	307/297 X
4,296,340	10/1981	Horan	307/238.3 X
4,322,675	3/1982	Lee et al.	307/297 X

### FOREIGN PATENT DOCUMENTS

2001494	1/1979	United Kingdom	307/297
2028553	3/1980	United Kingdom	307/297

### OTHER PUBLICATIONS

Harroun, "Substrate Bias Voltage Control", *IBM Tech. Disc. Bull.*, vol. 22, No. 7, Dec. 1979, pp. 2691-2692.  
Hummel, "Sentry Circuit for Substrate Voltage Con-

trol", *IBM Tech. Disc. Bull.*, vol. 15, No. 2, 6-1972, pp. 478-479.

Jacobson, "Threshold Detector", *IBM Tech. Disc. Bull.*, vol. 22, No. 7, 12-1979, pp. 2765-2767.

U.S. Defensive Publication T 954,006-Filed: 4/2/76-1/4/77, Inventor: James M. Lee (International Business Machines).

Primary Examiner—Stanley D. Miller

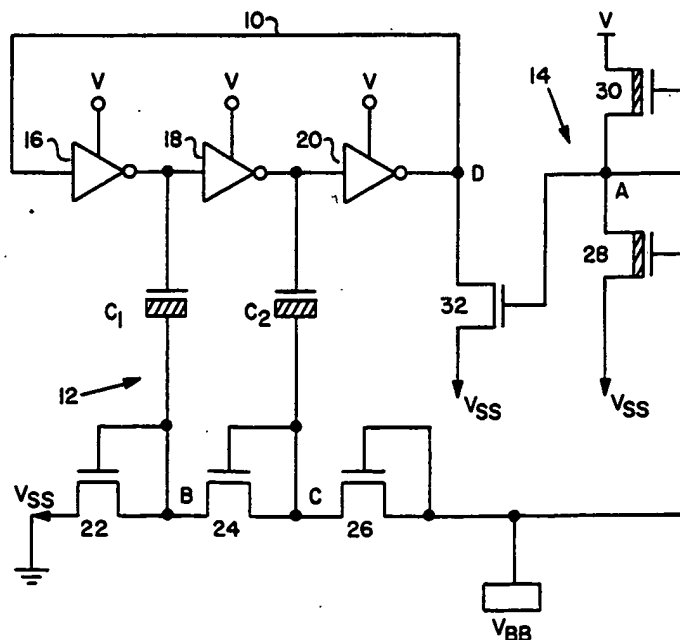
Assistant Examiner—D. R. Hudspeth

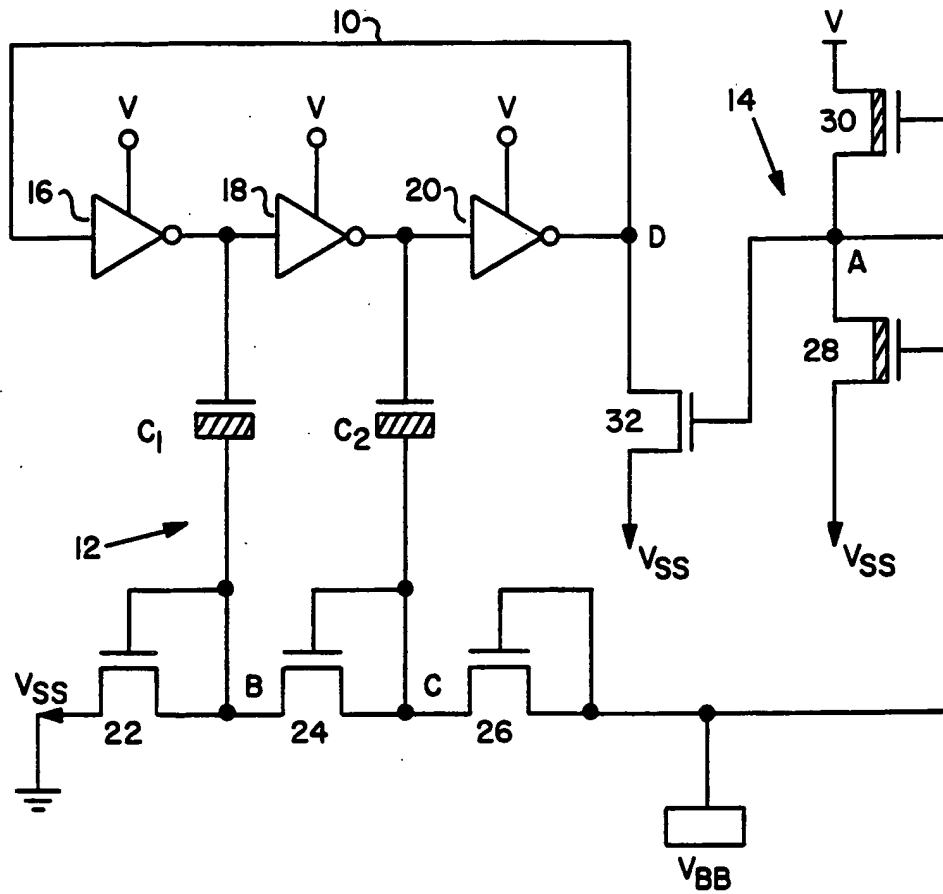
Attorney, Agent, or Firm—R. J. Meetin; J. Oisher; T. Briody

## [57] ABSTRACT

An on-chip regulated substrate bias voltage generator for an MOS integrated circuit includes a ring oscillator (10) for developing a true signal and its complement. The signals are applied to a charge pump (12) that includes two capacitors (C1 and C2) and a plurality of rectifiers (22, 24, and 26). The charge pump produces a substrate bias voltage ( $V_{BB}$ ) which is supplied to the gate of a depletion-mode field-effect transistor (28) whose source receives a reference voltage ( $V_{SS}$ ). The transistor forms part of a control circuit (14) coupled to the ring oscillator. In the N-channel case, the charge pumping action on the substrate drives the substrate bias negative until it reaches the sum of the reference voltage and threshold voltage of the depletion-mode transistor. This enables the control circuit to control the operation of the ring oscillator so as to regulate the substrate bias voltage.

10 Claims, 1 Drawing Sheet





# DEPLETION-MODE FET FOR THE REGULATION OF THE ON-CHIP GENERATED SUBSTRATE BIAS VOLTAGE

## BACKGROUND OF THE INVENTION

This invention relates to on-chip generation of substrate bias voltage for semiconductor integrated circuit devices, and particularly by means for regulating the substrate bias voltage.

Some integrated circuits utilizing MOS (Metal Oxide Semiconductor) field effect transistors require a substrate bias to avoid unwanted conduction of parasitic junction diodes or parasitic MOS transistors. Substrate bias generators in common use generate the required bias from a charge pumping circuit that operates from the dc supply. Examples of some substrate bias generators and charge pumps are disclosed in the following:

U.S. Pat. No. 4,115,710

U.K. patent application No. GB 2,028,553A

U.K. patent application No. GB 2,001,494A

U.S. defensive publication No. T 954,006

Typically in the prior art circuits, the intent is to pump sufficient charge into the substrate until the threshold voltage of a MOS transistor, either depletion or enhancement type, equals a predetermined value and thereafter to maintain the threshold voltage at that value by controlling the charge pumping. Thus, while the threshold voltage may remain substantially fixed at the predetermined value, the substrate bias voltage is allowed to vary over a wide range to compensate for other variable factors which may affect the threshold voltage, such as operating temperature or process parameters.

## SUMMARY OF THE INVENTION

According to the invention, there is provided a regulated substrate bias voltage generator for an integrated circuit that includes a depletion type field effect transistor.

A reference voltage is supplied to the source of the transistor. Consider the case in which the reference voltage is ground potential and the transistor is an N-channel device. Means are provided for developing a substrate bias voltage that can be altered between a value above and below the threshold voltage of the depletion type field effect transistor. Means are also provided for applying the substrate bias to the gate of the depletion type transistor to render it non-conducting when the gate voltage falls below the threshold voltage and to render it conducting when the gate voltage equals or exceeds the threshold voltage. Further, means are provided for coupling the transistor to the substrate bias generating means to increase the substrate bias when it falls below the threshold voltage of transistor and to decrease the substrate bias when it equals or exceeds the threshold voltage of the transistor.

In a specific embodiment of the invention a ring oscillator is used to generate a true signal and its complement which are applied to a charge pumping means. The charge pumping means pumps charge from the substrate until the substrate bias equals or exceeds the threshold voltage. The substrate bias is applied to the gate of the depletion type field effect transistor which forms part of a control circuit coupled to the ring oscillator. The control circuit regulates the substrate bias by stopping the ring oscillator when the bias has reached the threshold voltage and by turning on the ring oscilla-

tor when the substrate bias tends to rise above the threshold voltage. The components of the invention operate in the same way when the depletion type transistor is a P-channel device except that the voltage polarities are reversed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The single FIGURE is a schematic diagram of a substrate bias voltage generator and regulating means according to the invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

In the drawing there is shown a substrate bias voltage generator and regulating means for NMOS which comprises a ring oscillator 10, a charge pump 12, and a control circuit 14. The ring oscillator 10 includes an odd number of inverter stages, such as three stages of inverters 16, 18, 20, for example, for generating a true signal  $\phi$  and its complement  $\bar{\phi}$ . The signals  $\phi$  and  $\bar{\phi}$  are rectangular in form and opposite in phase. The inverters 16, 18, 20 may each comprise a MOS pull-down transistor of the enhancement type coupled in series with a MOS pull-up load transistor of the depletion type connected as a resistor by having its gate coupled in common to its source. Other means for generating the signals  $\phi$  and  $\bar{\phi}$  besides the ring oscillator 10 may be used, the only requirement being that the signals be recurring, rectangular, equal in amplitude, and opposite in phase.

The signals  $\phi$  and  $\bar{\phi}$  are coupled through capacitors C1 and C2 to nodes B and C respectively of the charge pump 12. Other elements of the charge pump 12 include three enhancement mode transistors 22, 24, and 26 connected as diodes by having their respective gates coupled in common to their drains. The transistors 22, 24, 26 function as voltage level shifters, as will be explained. The transistors 22, 24, 26 are connected in series between a reference source supply  $V_{SS}$ , such as ground, and the node  $V_{BB}$  at which the substrate bias voltage is generated.

The substrate bias control circuit 14 comprises three transistors 28, 30 and 32. The transistors 28 and 30 are depletion type and the transistor 32 is enhancement type. The depletion type transistors 28 and 30 are connected in series between reference source supply  $V_{SS}$  and positive dc supply V, such as +5 volts dc. The gate of pull-down transistor 28 is connected directly to the substrate bias potential node  $V_{BB}$ , the source is connected to reference source supply  $V_{SS}$ , and the drain is connected to node A which is common to the source of pull-up transistor 30 and the gate of enhancement transistor 32.

The pull-up transistor 30 is connected as a resistor by having its gate connected to its source. Since the pull-up transistor 30 functions as load device, it may be replaced by an enhancement type transistor or simply a resistor. The source of enhancement transistor 32 is connected to reference source supply  $V_{SS}$  and the drain is coupled to node D which is a common node in the feedback path between the input of the first inverter 16 and the output of the final inverter 20.

The operation of the substrate bias voltage generator and regulating means will now be described. When the supply voltage V is applied to the circuit, the substrate bias potential at node  $V_{BB}$  is initially close to ground potential. As a result, the pull-down depletion transistor 28 is in its low impedance or conducting state. By

choosing the impedance of pull-up depletion transistor 30 to be much larger than that of pull-down depletion transistor 28, common node A is kept near ground potential.

As a result of node A being low or at ground potential, the enhancement transistor 32 is in its high impedance or non-conducting state and the ring oscillator 10 comprised of inverters 16, 18, 20 will be allowed to oscillate. Thus at the plates of the capacitors C1 and C2, the signal pulses  $\phi$  and  $\bar{\phi}$  will appear as voltage swings of 0 to +5 volts and +5 volts to 0 respectively.

The 5 volt voltage swings on one side of each capacitor will appear on the opposite side thereof as 4 volt swings, reduced by one volt because of parasitic capacitances at nodes B and C respectively. Due to the presence of the transistors 22, 24, 26, a level shifting occurs at nodes B, C, and  $V_{BB}$ . Thus when node B goes positive, it will cause transistor 22 to conduct when the gate reaches its threshold potential, which is about 1 volt positive relative to its source which is at ground potential. The potential at node B thus can go no further positive than one threshold voltage drop above  $V_{SS}$ .

At the end of the first half cycle of the signal pulse  $\phi$ , when it goes negative, node B will change in the negative direction by 4 volts, thus dropping from +1 volt to -3 volts.

In similar fashion a 5 volt swing imposed on capacitor C2 by the complementary signal pulse  $\bar{\phi}$  will be translated to a 4 volt swing at node C which is equal and opposite in phase to the 4 volt swing on node B. Since node C can go no further positive than one threshold voltage drop relative to node B, by virtue of conduction of transistor 24, node C on its positive swing is limited to -2 volts. On its negative swing, therefore it will change by 4 volts to a maximum of -6 volts.

The 4 volt swing on node C is translated to a corresponding 4 volt swing at the drain of transistor 26, which is connected to the substrate bias node  $V_{BB}$ . Thus, a voltage swing between -2 and -6 volts on node C would tend to be translated to a voltage swing, unregulated between -1 and -5 volts at  $V_{BB}$  because  $V_{BB}$  is one threshold voltage drop above node C. However, as the voltage at  $V_{BB}$  approaches -3 volts, which is the threshold voltage for the depletion transistor 28, whose gate is tied to  $V_{BB}$ , the depletion transistor 28 starts to go into its high impedance or cut-off state, and node A starts to charge towards the supply voltage V through transistor 30.

When the potential on node A is high enough to switch transistor 32 into its low impedance or ON state, then the potential on node A is held close to ground potential, thereby causing the ring oscillator 10 to stop oscillating. The charge pumping action then stops and the potential on node  $V_{BB}$  does not go further negative than -3 volts.

Since all the reverse biased junction leakages on the chip are from various positively charged circuit nodes to  $V_{BB}$ , the potential on node  $V_{BB}$  will then start moving positive until it causes transistor 28 to go into its low impedance state once again. This in turn causes the potential on node A to drop, thus putting transistor 32 into its high impedance state. The ring oscillator starts to oscillate again until the potential on  $V_{BB}$  is sufficiently negative to cause transistor 28 to go into its high impedance state once more. The voltage regulation cycle repeats itself and results in a substrate bias voltage that is close to the depletion threshold voltage of transistor 28, which is very close to -3 volts.

The circuit of the invention may also be used for PMOS by inverting the polarity of the supply voltages  $V_{SS}$  and V.

Although the best mode contemplated for carrying out the present invention has been shown and described, it will be apparent that modification and variation may be made without departing from what is regarded to be the subject matter of the invention.

What is claimed is:

1. In an integrated circuit having a semiconductor substrate, a voltage generator for providing a substrate bias voltage for the substrate, the voltage generator comprising:

a depletion-mode field-effect transistor having a source for receiving a reference voltage, a gate for receiving the bias voltage, and a drain;

a ring oscillator comprising an odd number of at least three inverters serially arranged in a ring, the inverters providing a pair of complementary signals that repetitively vary when the transistor is conductive;

a charge pump responsive to the complementary signals as they repetitively vary for pumping the bias voltage to a value (1) less than the sum of the reference voltage and the threshold voltage of the transistor where it is N-channel type or (2) greater than the sum of the reference voltage and the threshold voltage of the transistor where it is P-channel type; and

means for stopping the oscillator from oscillating when the transistor is non-conductive so that the bias voltage (1) increases where the transistor is N-channel type or (2) decreases where the transistor is P-channel type.

2. A voltage generator as in claim 1 wherein the means for stopping disables the oscillator in response to the voltage at the drain of the transistor when it is non-conductive.

3. A voltage generator as in claim 2 wherein the means for stopping comprises a like-polarity enhancement-mode field-effect transistor having a source for receiving the reference voltage, a gate coupled to the drain of the depletion-mode transistor, and a drain coupled to the oscillator.

4. A voltage generator as in claim 3 further including a load device coupled to the drain of the depletion-mode transistor.

5. A voltage generator as in claim 4 wherein the load device comprises a like-polarity resistively-connected depletion-mode field-effect transistor.

6. A voltage generator as in claim 4 wherein the load device comprises a resistor.

7. A voltage generator as in claim 4 wherein one of the complementary signals is provided from a node between one pair of the inverters, the other of the complementary signals is provided from a node between another pair of the inverters, and the drain of the enhancement-mode transistor is coupled to a node between a pair of the inverters.

8. A voltage generator as in claim 2 wherein the charge pump comprises:

a first rectifier having one end coupled to a voltage supply;

a second rectifier having one end coupled to the other end of the first rectifier so as to be forwardly in series therewith, the other end of the second rectifier being coupled to a substrate node at which the bias voltage is provided to the substrate;



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a first capacitor having a pair of plates of which one is coupled to one end of the second rectifier and the other receives one of the complementary signals; and

a second capacitor having a pair of plates of which one is coupled to the other end of the second rectifier and the other receives the other of the complementary signals.

9. A voltage generator as in claim 8 wherein the

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charge pump further includes a third rectifier forwardly coupled between the second rectifier and the substrate node.

10. A voltage generator as in claim 9 wherein each rectifier is a like-polarity diode-connected field-effect transistor.

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[54] **HIGH FREQUENCY CMOS VCO WITH GAIN CONSTANT AND DUTY CYCLE COMPENSATION**

[75] Inventor: **Richard R. Rasmussen**, Fremont, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **642,677**

[22] Filed: **Jan. 17, 1991**

[51] Int. Cl.<sup>5</sup> ..... **H03B 1/00**

[52] U.S. Cl. .... **331/57; 331/108 B**

[58] Field of Search ..... **331/57, 108 A, 108 B, 331/177 R; 307/448**

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,876,519 10/1989 Davis et al. .... 331/57

**OTHER PUBLICATIONS**

Ware et al., "A 200 MHz CMOS Phase-Locked Loop with Dual Phase Detectors", IEEE Transactions on Solid State Circuits, May 10, 1989.

Yousefi, "14 MHz-100 MHz CMOS L Based Frequency Synthesizer IC".

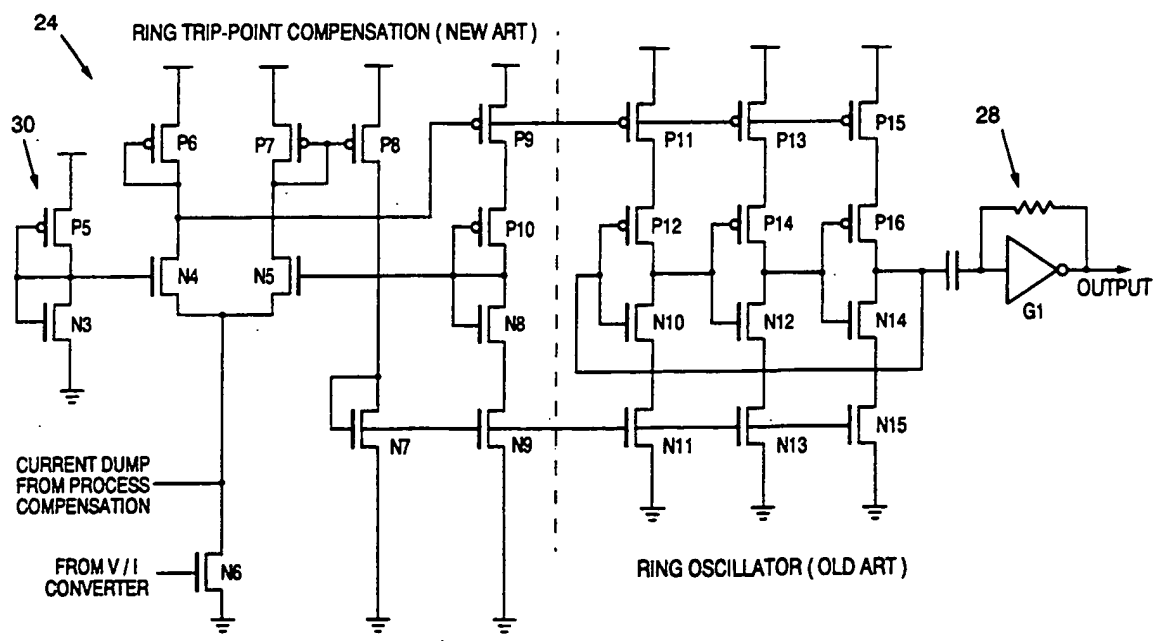
Primary Examiner—Robert J. Pascal

Attorney, Agent, or Firm—Limbach, Limbach & Sutton

[57] **ABSTRACT**

The present invention provides a high frequency CMOS voltage controlled oscillator circuit with gain constant and duty cycle compensation. The voltage controlled oscillator circuit includes a multi-stage ring oscillator that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors. The ring oscillator responds to a control current signal for controlling the frequency of oscillation of the ring oscillator. A voltage-to-current converter converts a tuning voltage input signal to a corresponding output current signal that is independent of the channel strength of the N-channel and P-channel transistors. Process compensation circuitry responds to the tuning voltage input signal to provide a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors. Trip-point compensation circuit provides a net ring current signal as the current control signal to the ring oscillator. The net ring current signal represents the difference between the output current signal and the current dump output signal and responds to the balance between the output buffer trip point and a ring oscillator dummy stage.

**4 Claims, 8 Drawing Sheets**



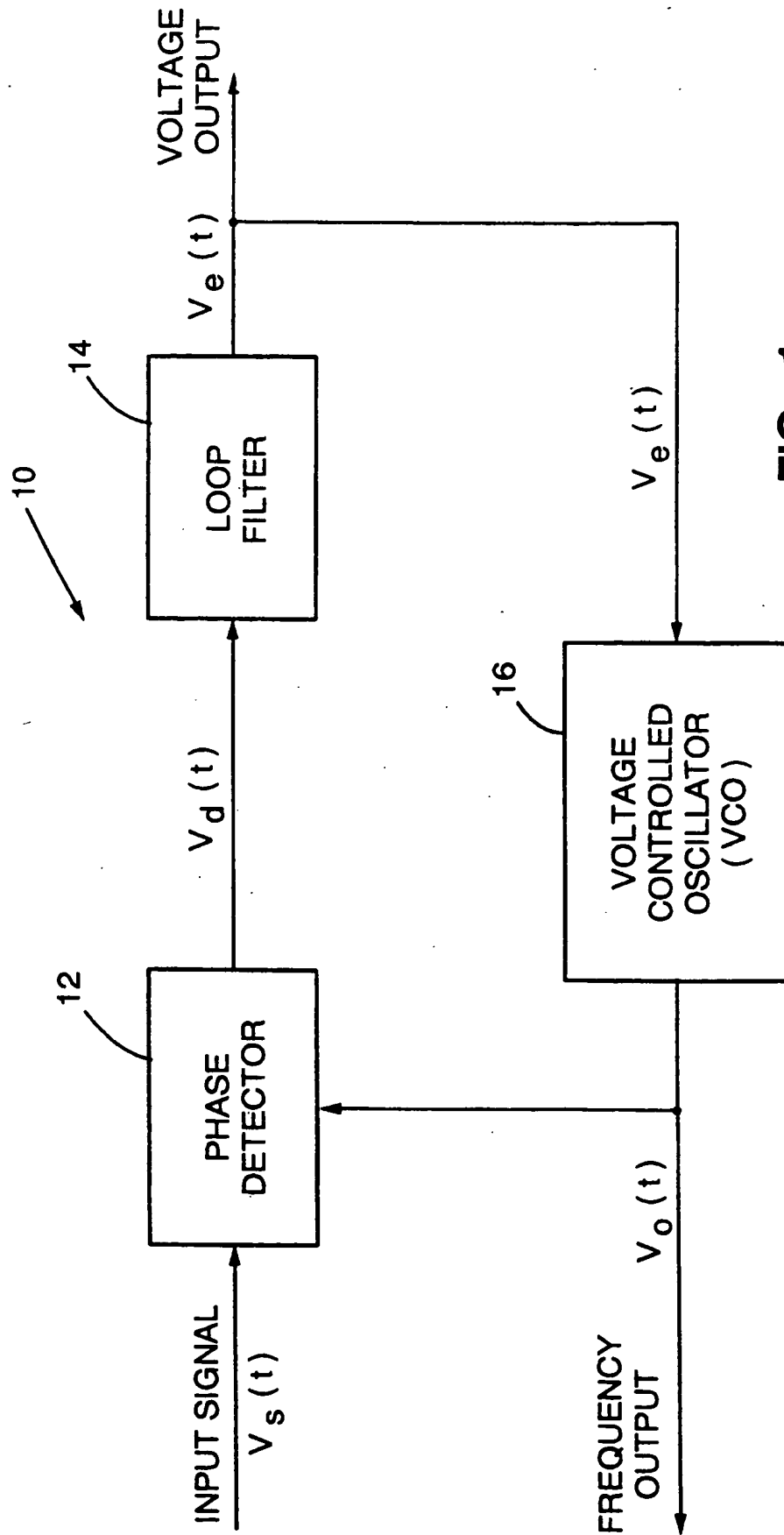


FIG. 1

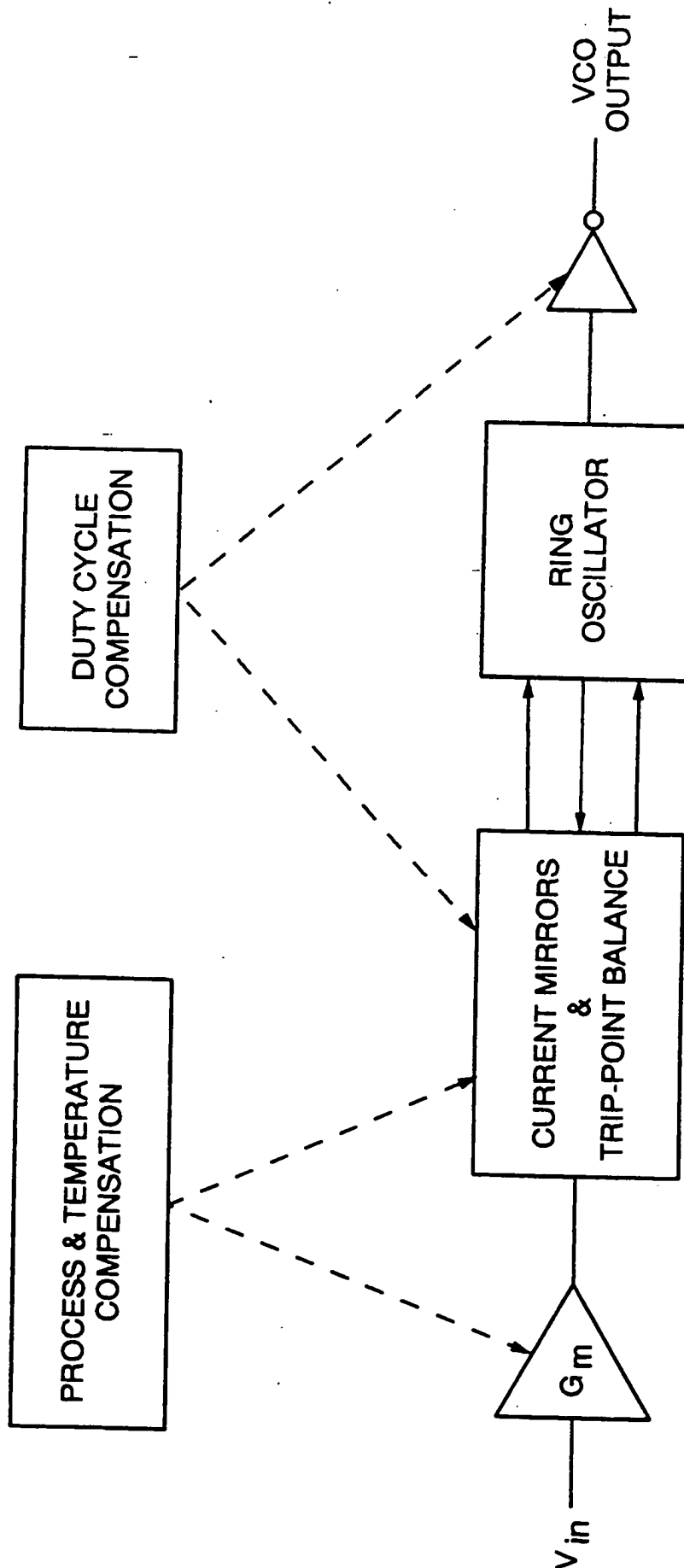
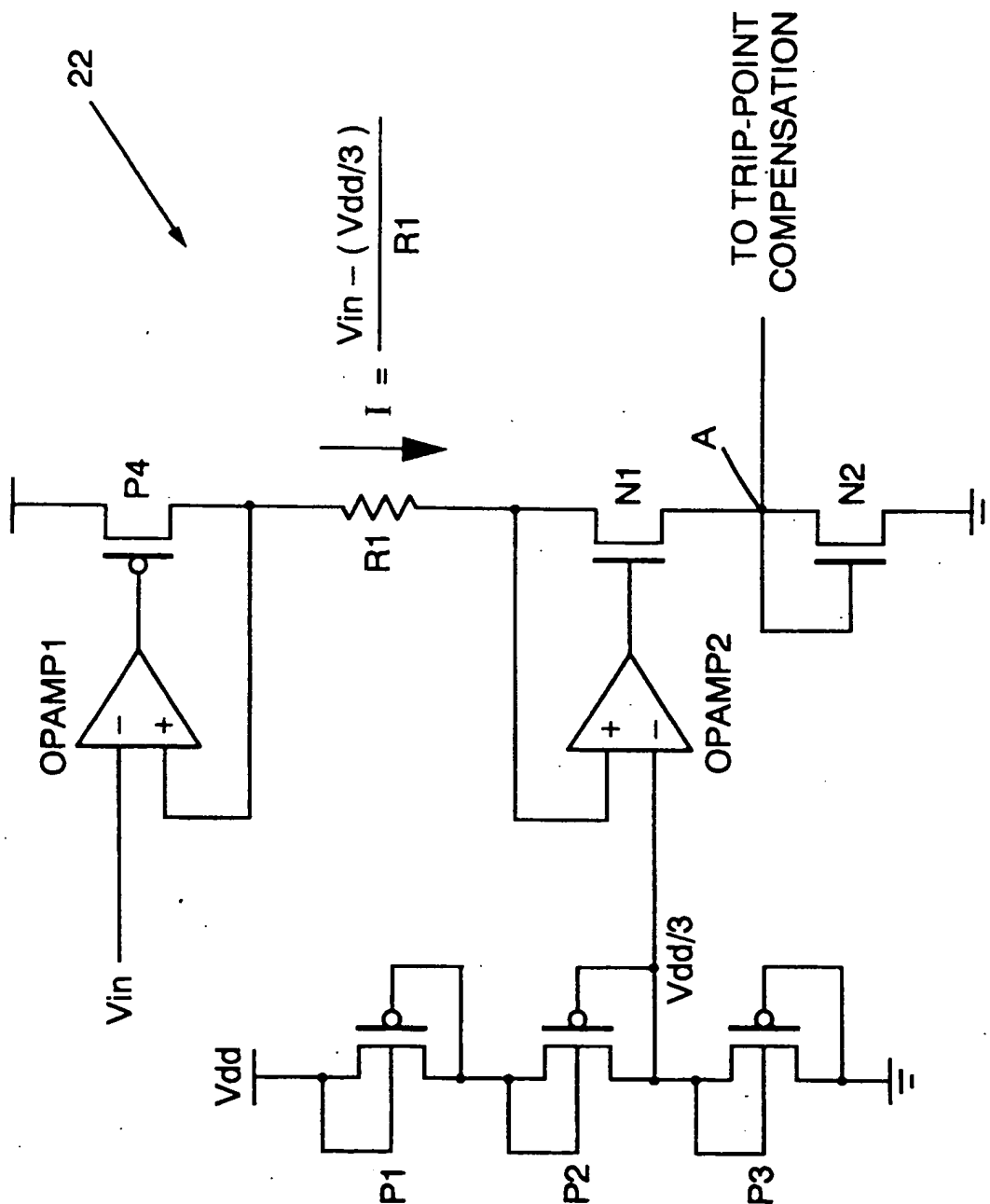
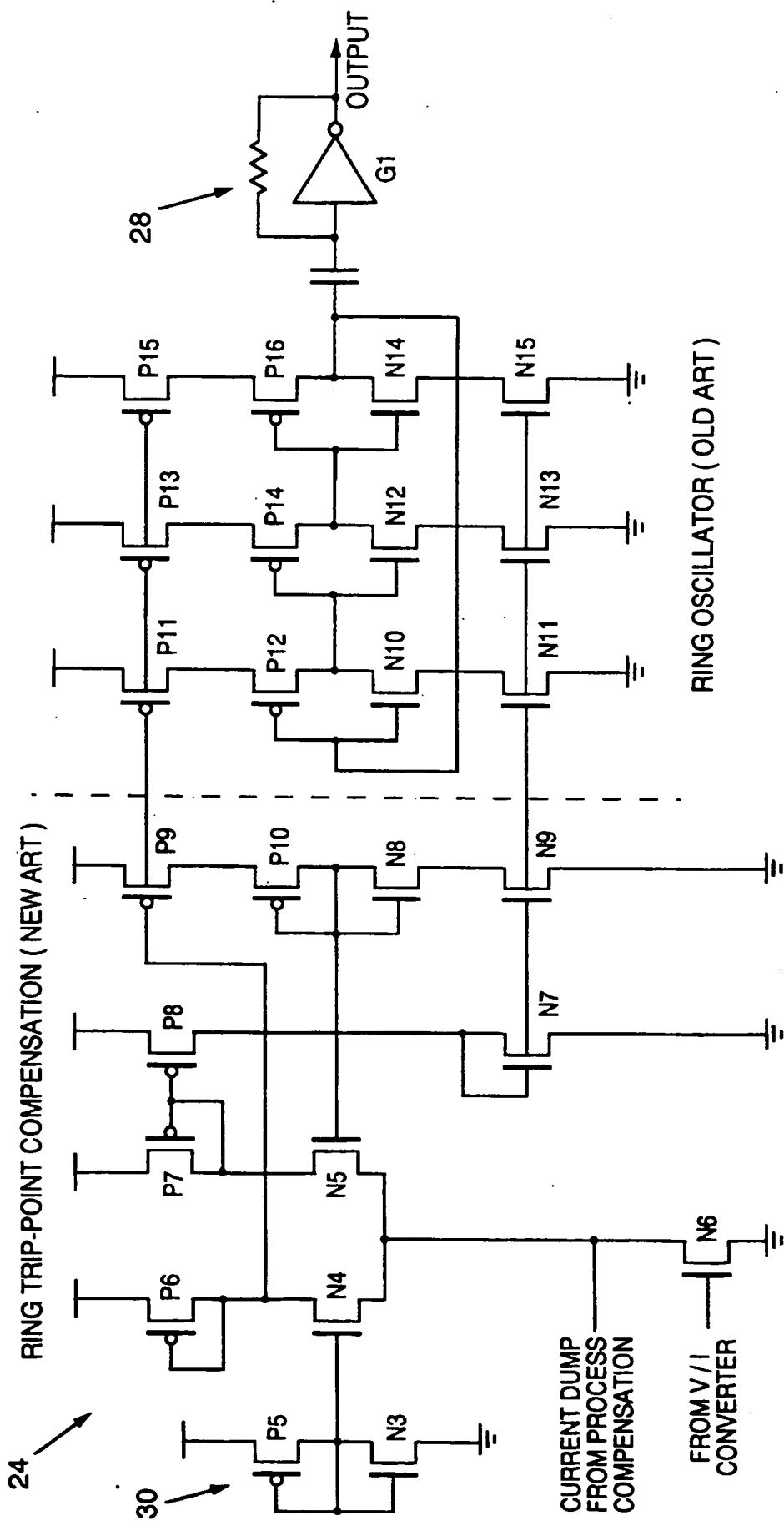


FIG. 2



**FIG. 3**



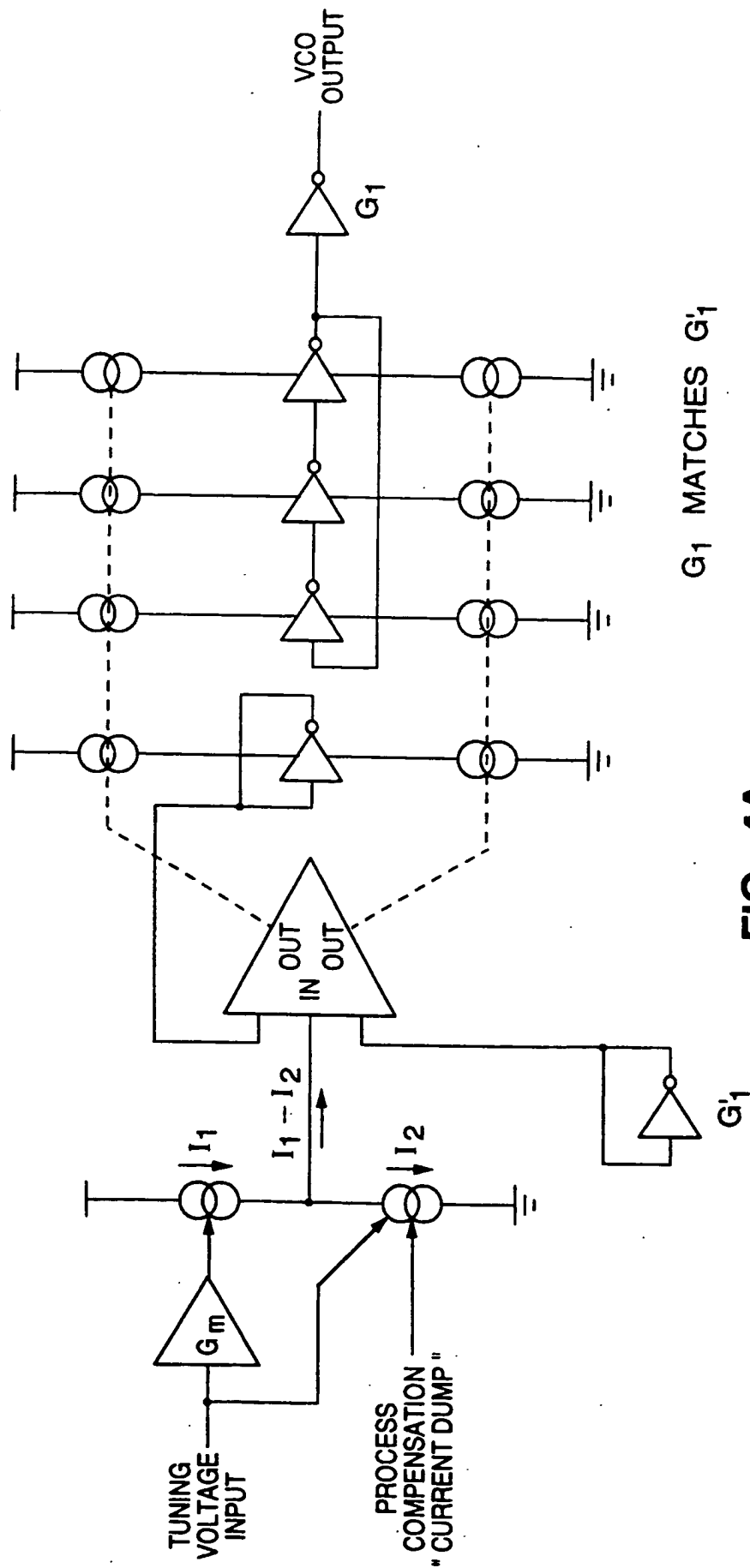
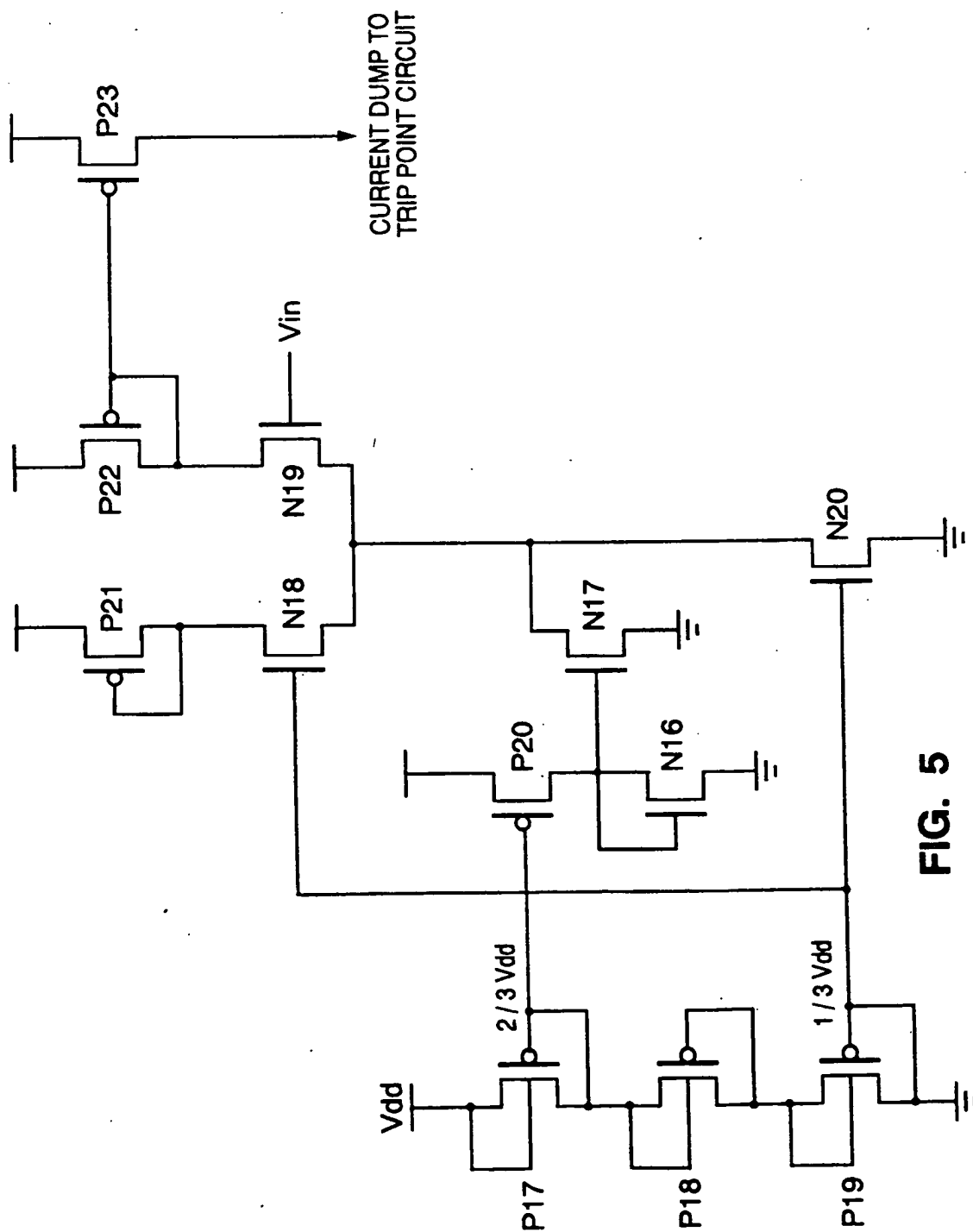


FIG. 4A





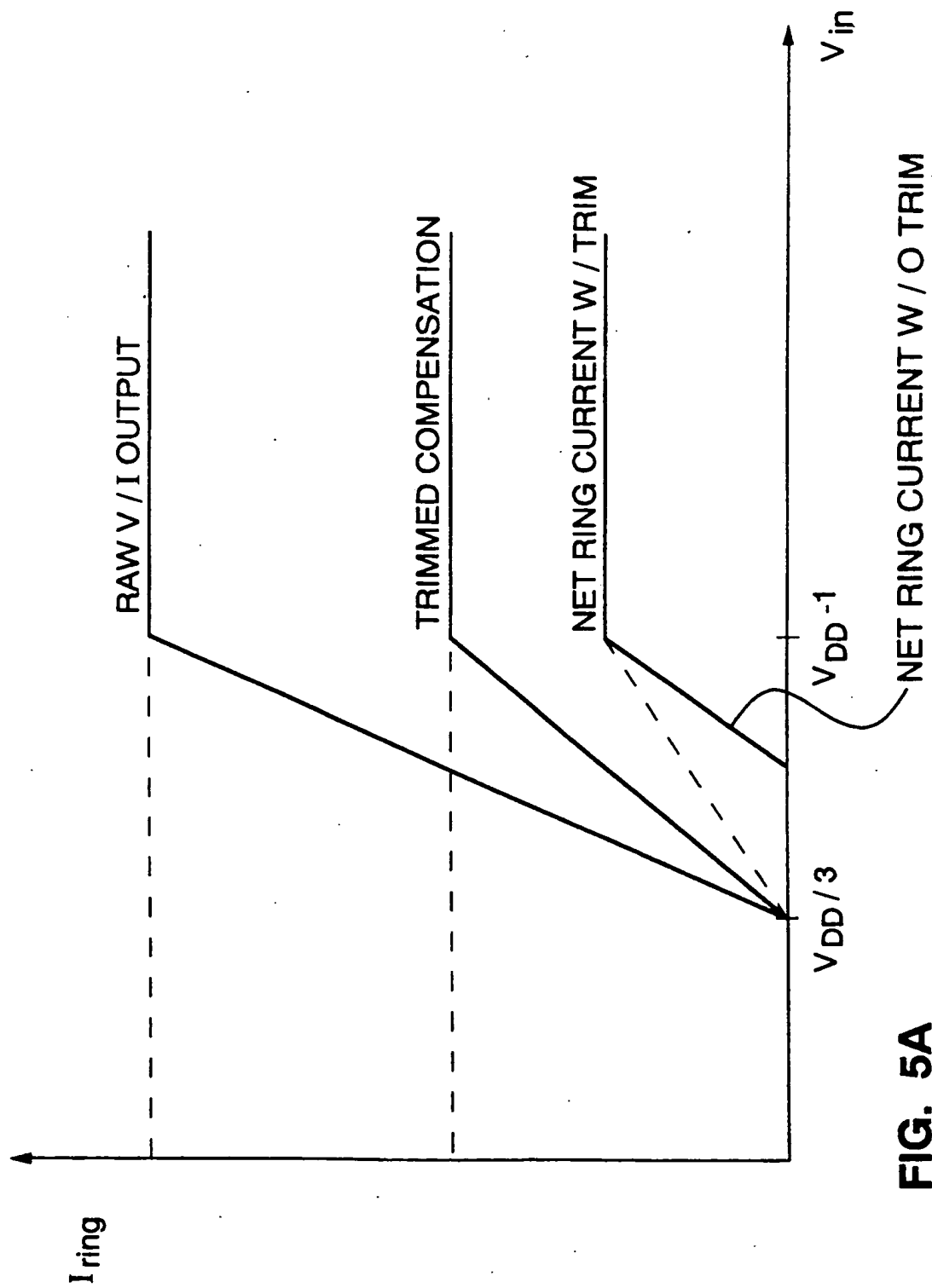
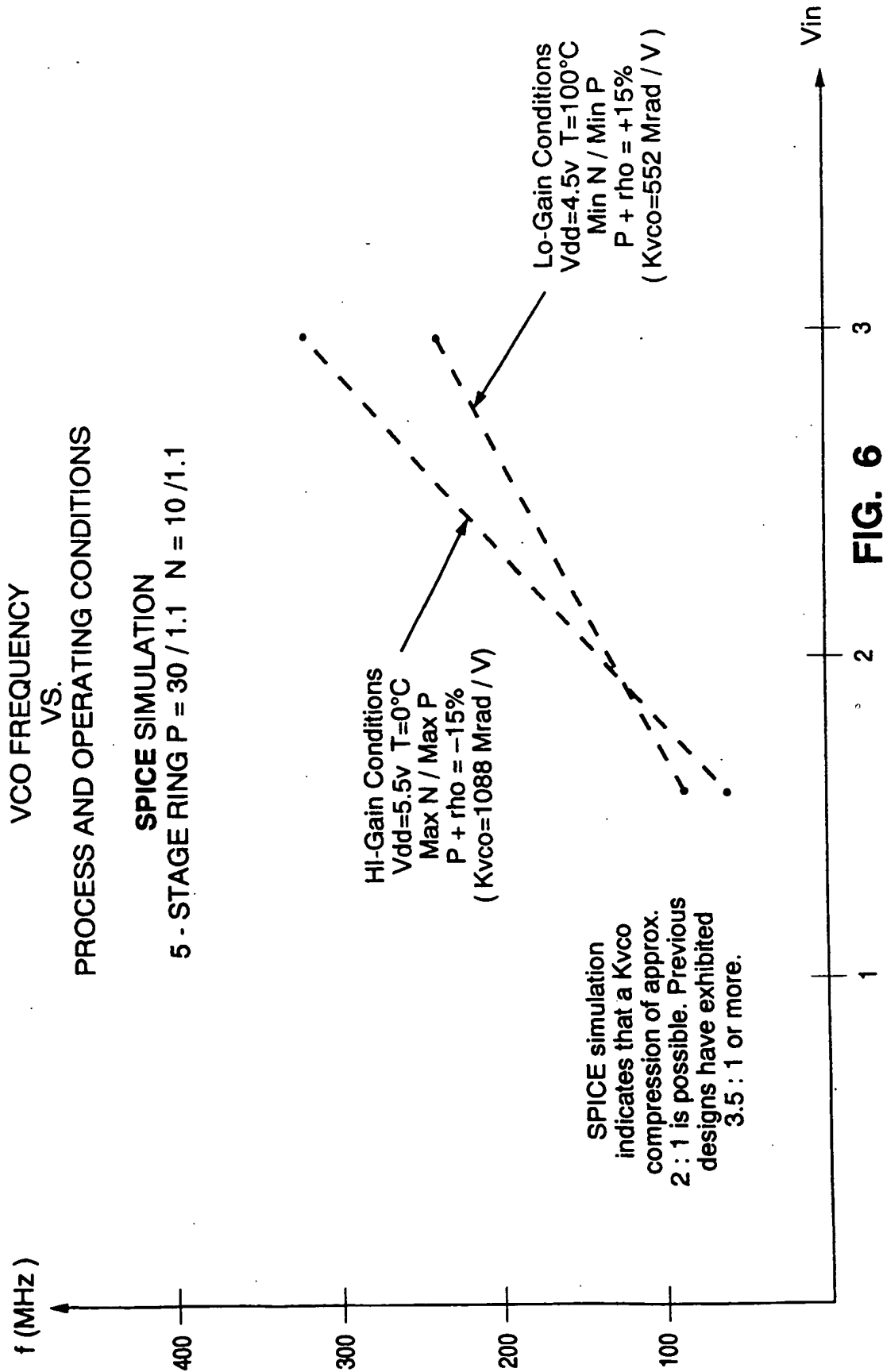


FIG. 5A



## HIGH FREQUENCY CMOS VCO WITH GAIN CONSTANT AND DUTY CYCLE COMPENSATION

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to voltage-controlled oscillators and, in particular, to methods and apparatus for obtaining a variable clock frequency having a well-controlled output range and duty cycle over varying temperature, process and supply voltage.

#### 2. Discussion of the Prior Art

As shown in FIG. 1, a basic phase-locked loop (PLL) system 10 includes three essential elements—a phase detector 12, a loop filter 14 and a voltage-controlled oscillator (VCO) 16—interconnected to form a feedback system. The phase detector 12 compares the phase of the input signal  $V_i(t)$  with the output frequency  $V_o(t)$  of the VCO 16 and generates an error voltage  $V_d(t)$  corresponding to the difference. The error voltage signal  $V_d(t)$  is then filtered by the loop filter 14 and applied to the control terminal of the VCO 16 in the form of an error voltage  $V_d(t)$  to control its frequency of oscillation.

The VCO 16 is the most critical element of the PLL system 10. The tuning slope, that is, the output frequency  $V_o(t)$  dependence on control voltage  $V_d(t)$ , is determined by the conversion gain constant  $K_{VCO}$  of the VCO 16. Similarly, the linearity of the voltage-to-frequency conversion characteristics of the PLL system 10 is determined solely by the limitations of the control characteristics of the VCO 16. Thus, the stability and control characteristics of the VCO 16 are key design parameters in monolithic PLL circuits.

The VCO 16, which is basically an analog circuit, must be immune to on-chip and off-chip noise sources. If it is not, then its output  $V_o(t)$  will exhibit short-term frequency instability, or jitter. Maintaining a low VCO gain constant  $K_{VCO}$  is one method of reducing noise sensitivity. The required operating frequency for conventional VCOs ranges from a few MHz to beyond 200 MHz. Tuning ranges up to 2 to 1 are also required. To be easily compatible with 5 V power supply constraints and minimum phase detector/charge pump solutions, the tuning voltage should be approximately 1.5 V to ( $V_{cc} - 1.5$  V).

As stated above, the VCO gain constant  $K_{VCO}$  must be well controlled so that loop filtering schemes are predictable and stable. This is especially important in data acquisition and mass storage applications such as disk controllers and constant density recording. At higher output frequencies, the duty cycle is also critical.

In many applications, the process of choice for VCO design has been complementary-metal-oxide-semiconductor (CMOS) technology. However, previous CMOS VCO designs have been greatly affected by process variations, which can cause large changes in the VCO gain constant  $K_{VCO}$  and/or have required external trimming components. External trimming adds pins and cost to the PLL chip and provides an antenna through which noise can be coupled into the sensitive analog sections of the chip.

One example of a high frequency CMOS phase-locked loop is described by Ware et al, "a 200 MHz CMOS Phase-Lock-Loop with Dual Phase Detectors", IEEE Transactions on Solid State Circuits, May 10, 1989. The Ware et al PLL features a VCO that requires the use of a bandgap regulator that relies on parasitic

NPN transistors. It achieves frequency control by varying the applied voltage across the ring oscillator stages. The VCO utilized by Ware is based on a ring of three inverting amplifiers.

Yousefi, "14 MHz-100 MHz CMOS PLL Based Frequency Synthesizer IC", describes a PLL design where the VCO gain constant compensation depends upon the use of an external resistor.

U.S. Pat. No. 4,876,519, issued on Oct. 24, 1989 to Craig M. Davis and Richard R. Rasmussen, and commonly assigned herewith, discloses a PLL implementation in emitter-coupled-logic (ECL) technology. Although the Davis/Rasmussen design provides significant advantages, its Bipolar/CMOS process requirement prohibits its use in some applications.

It would, therefore, be desirable to have available a CMOS-based PLL that features good VCO frequency control, gain control and duty-cycle characteristics without using external components.

### SUMMARY OF THE INVENTION

The present invention provides a high frequency CMOS voltage controlled oscillator circuit with gain constant and duty cycle compensation. The voltage controlled oscillator circuit includes a multi-stage ring oscillator that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors. The ring oscillator responds to a control current signal for controlling the frequency of oscillation of the ring oscillator. A voltage-to-current converter converts a tuning voltage input signal to a corresponding output current signal that is independent of the channel strength of the N-channel and P-channel transistors. Process compensation circuitry responds to the tuning voltage input signal to provide a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors. Trip-point compensation circuit provides a net ring current signal as the current control signal to the ring oscillator. The net ring current signal represents the difference between the output current signal and the current dump output signal.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings which set forth an illustrative embodiment in which the foregoing features of the invention are utilized.

### DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the basic elements of a conventional phase-locked loop (PLL).

FIG. 2 is a block diagram illustrating an embodiment of voltage-controlled oscillator (VCO) in accordance with the present invention.

FIG. 3 is a schematic diagram illustrating an embodiment of a V/I converter utilizable in the VCO shown in FIG. 2.

FIG. 4 is a schematic diagram illustrating an embodiment of ring trip-point compensation circuitry together with a conventional ring oscillator utilizable in the VCO shown in FIG. 2.

FIG. 4A is a schematic diagram illustrating a generalized representation of the FIG. 4 circuit.

FIG. 5 is a schematic diagram illustrating an embodiment of process compensation circuitry utilizable in the VCO shown in FIG. 2.

FIG. 5A is a plot of control current to the ring oscillator versus tuning voltage.

FIG. 6 is a graph illustrating VCO frequency versus process and operating conditions for a VCO in accordance with the present invention.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a block diagram of a CMOS voltage-controlled oscillator (VCO) 20 with gain constant and duty cycle compensation in accordance with the present invention.

VCO 20 includes a voltage-to-current V/I converter 22 with gain  $G_m$  that amplifies input signal  $V_{in}$  to current mirror and trip-point compensation circuitry 24. The outputs of the trip-point compensation circuitry 24 are provided to a CMOS ring oscillator 26. The selected phase signal of the ring oscillator 26 is provided as the VCO output via an output buffer 28.

In accordance with the present invention, the VCO 20 includes process and temperature compensation for the V/I converter 22 and process compensation for the trip-point circuitry 24. Duty cycle compensation for both the trip-point balance circuitry 24 and the output buffer 28 is derived from matching devices within these two circuit elements.

An embodiment of a V/I converter 22 utilizable in the VCO 20 is shown in greater detail in FIG. 3.

In the FIG. 3 V/I converter circuit 22, tuning voltage input signal  $V_{in}$  is provided to the inverting input of operational amplifier OPAMP1. The non-inverting input of op amp OPAMP1 is connected to the drain of P-channel transistor P4 which is driven by the output of op amp OPAMP1. A second operational amplifier OPAMP2 drives N-channel sense transistor N1, which has its source connected to an output node A. The non-inverting input of op amp OPAMP2 is connected to the drain of P-channel sense transistor P4 via internal current control resistor R1. The inverting input of op amp OPAMP2 is connected to receive a  $V_{DD}$  driver stage output, the driver stage comprising three series-connected, P-channel transistors P1, P2 and P3 which are connected between a supply voltage  $V_{DD}$  and ground. An N-channel output mirror transistor N2 is connected between the output node A and ground.

Thus, the output current at node A of the V/I converter 22 is controlled by forcing the bottom side of resistor R1 to  $V_{DD}/3$  and the top side of resistor R1 to  $V_{in}$ . The output current is, therefore,

$$I = \frac{V_{in} - (V_{DD}/3)}{R1}$$

and is relatively independent of supply  $V_{DD}$  and its only process sensitivity is the tolerance of the internal resistor R1. The transconductance slope is totally independent of supply  $V_{DD}$ .

Resistor R1 can also be an external component for even greater accuracy. In this case, both external connections are floating above ground and external noise can be made common-mode.

The current at node A is then mirrored into the ring oscillator 26, as described below.

An embodiment of current mirror and ring trip-point compensation circuitry 24 is shown in greater detail in FIG. 4.

Trip-point compensation is desirable in order to maintain symmetric VCO output waveforms as the process

varies. For example, when the process tends toward weak N-channel and strong P-channel transistors, the resultant VCO output waveform will have a higher duty cycle than when the N-channel and P-channel transistor strengths are well matched.

The FIG. 4 circuit includes a differential stage, comprising N-channel transistors N4 and N5, that allows the total ring oscillator current from the V/I converter 22 to be shared as process shift demands. That is, as the P-channel transistors of the VCO get weaker because of process variation, the self-biased inverter (transistors P10 and N8) voltage in the FIG. 4 circuit will tend to drop, forcing more current to be steered through input transistor N4 and then mirrored from P-channel transistor P6 to P-channel current sensing transistors P9, P11, P13 and P15. Similarly, when the N-channel transistors get weaker, more current is steered through P-channel input transistor P7 and mirrored into transistors P8 and N7 and current sensing transistors N9, N11, N13 and N15.

As further shown in FIG. 4, the ring trip-point compensation circuitry includes a dummy inverter stage (transistors P10 and N8) that is identical in form to the three inverter stages (P12/N10, P14/N12 and P16/N14) of the ring oscillator.

The ring oscillator is a standard design having an output frequency equal to  $1/6T$ , where T is the propagation delay of an inverter (P12/N10, P14/N12, P16/N14).

From the above description, those skilled in the art will recognize that the FIG. 4 circuitry can be more generally illustrated as shown in FIG. 4A. That is, as shown in FIG. 4A, the amplified V/I converter control input received from buffer  $G_m$  drives a first current I1. The current dump from the process compensation circuitry drives a second current source I2. The net ring oscillator current equals the V/I current I1 minus the process compensation current I2.

As shown in FIG. 4, the compensation circuit 24 uses a self-biased inverter 30 comprising P-channel transistor P5 and N-channel transistor N3 to drive the ring oscillator bias such that the resultant oscillation is also matched with the output buffer G1. Output buffer G1 amplifies and squares the ring oscillator signal.

An embodiment of process compensation circuitry is shown in detail in FIG. 5.

The process compensation circuit maintains a constant frequency tuning range over process variations such as transistor threshold voltage, transconductance and source/drain capacitance. It also compensates for externally induced variations, such as temperature and supply voltage  $V_{DD}$ .

As shown in FIG. 5, a  $V_{DD}$  voltage splitter stage consisting of P-channel transistors P17, P18 and P19 sets up a  $V_{DD}$ -dependent gate bias on P-channel transistor P20 and N-channel transistor N20. As P-channel strength increases, the currents in N-channel sensing transistors N16 and N17 increase proportionally. Likewise, as N-channel strength increases, the current in N-channel sensing transistor N20 increases. The P-channel and N-channel strength-dependent currents sum to become the tail current in the differential stage comprising N-channel transistors N18 and N19, which is part of a  $K_{VCO}$  compression network. Thus, as the tuning voltage  $V_{in}$  applied to input transistor N19 increases, so does the current in P-channel transistor P22 and P-channel mirror transistor P23. This current

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dumps into the trip-point compensation circuit 24 and effectively "steals" current away from the ring oscillator, thereby maintaining a constant output frequency. Since the "stolen" current is proportional to the tuning voltage  $V_{in}$ , the VCO gain constant  $K_{VCO}$  is further compressed.

This concept is further illustrated in the FIG. 5A plot of control current  $I_{ring}$  to the ring oscillator versus tuning voltage  $V_{in}$ . As shown in FIG. 5A, the current  $I_{ring}$  supplied by the V/I converter circuit (FIG. 3) rises from zero when  $V_{in}$  equals  $V_{DD}/3$ , the slope of the curve being dependent on the value of resistor  $R_I$ . As stated above, as process strength varies, the slope of the V/I converter output remains constant. Thus, without current trimming, the net ring current will not be process dependent. With current trimming provided in accordance with the present invention, ring current  $I_{ring}$  is controlled over a widened range of tuning voltages  $V_{IN}$ .

FIG. 6 provides a plot of VCO frequency versus process and operating conditions based on a SPICE simulation of the concepts of the invention described above for a 5 V integrated circuit under worst case operating conditions. The simulation indicates that VCO gain constant ( $K_{VCO}$ ) compression of approximately 2:1 is possible. Conventional VCO designs exhibit gain constant compression of 3.5:1 or more.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that methods and apparatus within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. A voltage controlled oscillator circuit comprising:
  - (a) multi-stage ring oscillator means that includes a plurality of series-connected inverter stages comprising N-channel and P-channel transistors, the ring oscillator means responsive to a control current signal for controlling the frequency of oscillation of the ring oscillator means; and
  - (b) voltage-to-current converter means for converting a tuning voltage input signal to a corresponding output signal that is independent of the channel strength of the N-channel and P-channel transistors;
  - (c) process compensation means responsive to the tuning voltage input signal for providing a current dump output signal corresponding to the channel strength of the P-channel and N-channel transistors; and
  - (d) trip-point compensation means responsive to the output signal and the current dump output signal to provide a net ring current signal as the control current signal to the ring oscillator means, the net ring current signal representing the difference be-

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tween the output signal and the current dump output signal and responding to the balance between the output buffer's input threshold and a ring inverter dummy stage.

2. A voltage controlled oscillator circuit as in claim 1 wherein the voltage-to-current converter means comprises:

- (a) supply voltage divider means connected between a supply voltage and ground for providing a voltage driver output signal;
- (b) a first operational amplifier that receives the tuning voltage input signal at its inverting input;
- (c) a second operational amplifier that receives the voltage driver output signal at its inverting input;
- (d) a P-channel sense transistor having its gate connected to receive the output signal of the first operational amplifier, its source connected to the supply voltage and its drain connected both to the non-inverting input of the first operational amplifier and to the first side of a current control resistor;
- (e) a N-channel sense transistor having its gate connected to receive the output signal of the second operational amplifier, its drain connected both to the non-inverting input of the second operational amplifier and to the second side of the current control resistor, and its source connected to an output node that provides the output current signal; and
- (f) a N-channel output mirror transistor having its drain and gate commonly connected to the output node and its source connected to ground.

3. A voltage controlled oscillator circuit as in claim 1 wherein the process compensation means comprises:

- (a) supply voltage splitter means connected between the supply voltage and ground for generating first and second bias voltage output signals;
- (b) channel strength sensing means responsive to the first and second bias voltage output signals for providing a tail current signal; and
- (c) gain constant compression means responsive to the tail current and to the tuning voltage input signal for providing current dump output signal corresponding to the tuning voltage input signal.

4. A voltage controlled oscillator circuit as in claim 1 wherein the trip-point compensation means comprises:

- (a) current steering means for steering the control current signal to the ring oscillator means depending upon the channel strength of the N-channel and P-channel transistors;
- (b) an input node for providing the current dump output signal as tail current to the current steering means; and
- (c) a N-channel transistor connected between the input node and ground for providing the current input to the ring oscillator.

\* \* \* \* \*

# United States Patent [19]

Weaver et al.

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[45] Date of Patent: Apr. 5, 1988

## [54] VOLTAGE CONTROLLED OSCILLATOR WITH FREQUENCY SENSITIVITY CONTROL

[75] Inventors: Gary R. Weaver, Manhattan Beach;  
Dana H. Theis, Long Beach; Bernard  
L. Walsh, Jr., Northridge; Bryce M.  
Smith, Los Angeles, all of Calif.

[73] Assignee: Hughes Aircraft Company, Los  
Angeles, Calif.

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[52] U.S. Cl. .... 331/117 R; 331/117 D;  
331/117 V; 332/30 V

[58] Field of Search ..... 331/36 C, 117 R, 117 FE,  
331/177 V, 117 D; 332/30 V, 18

### [56] References Cited

#### U.S. PATENT DOCUMENTS

4,009,448	2/1977	Hopwood et al.	331/4
4,288,875	9/1981	Carter	455/197
4,310,809	1/1982	Buck et al.	331/177 V X
4,392,113	7/1983	Jackson	331/14
4,462,110	7/1984	Baldwin et al.	377/43

#### OTHER PUBLICATIONS

Niehenke et al, "A Microstrip Low-Noise X-Band  
Voltage-Controlled Oscillator", IEEE Trans. Micro-

wave Theory and Techniques, vol. MTT-27, No. 12,  
Dec. 1979.

Ku-Band Digitally Tuned Oscillator will soon be avail-  
able for Systems Designers, C. Pham, J. Lee, D. Kuma-  
moto, Defence Electronics, Feb. 1982, pp. 46-53.

Primary Examiner—Siegfried H. Grimm

Attorney, Agent, or Firm—S. M. Mitchell; M. J. Meltzer;  
A. W. Karambelas

### [57] ABSTRACT

A voltage controlled oscillator is tuned with a network comprising two varactor diodes and two transmission lines. By selecting appropriate values of varactor capacitance and transmission line length and width the overall reactance of the network is such that, when a varactor tuning voltage is varied, the output frequency of the voltage controlled oscillator will vary in an fashion with respect to the tuning voltage. Such a voltage controlled oscillator is gain compensated and exhibits a controlled modulation sensitivity over a range of frequencies. If the required frequency range of the oscillator is known beforehand, an alternate embodiment of the invention may be employed in which one of the varactor diodes is replaced with a fixed capacitor having a suitable value for the desired frequency range.

6 Claims, 2 Drawing Sheets

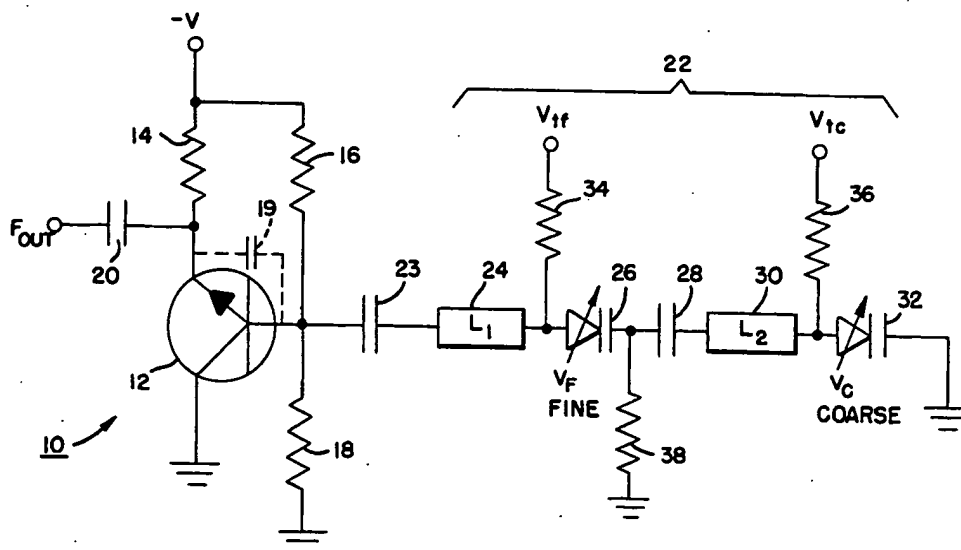
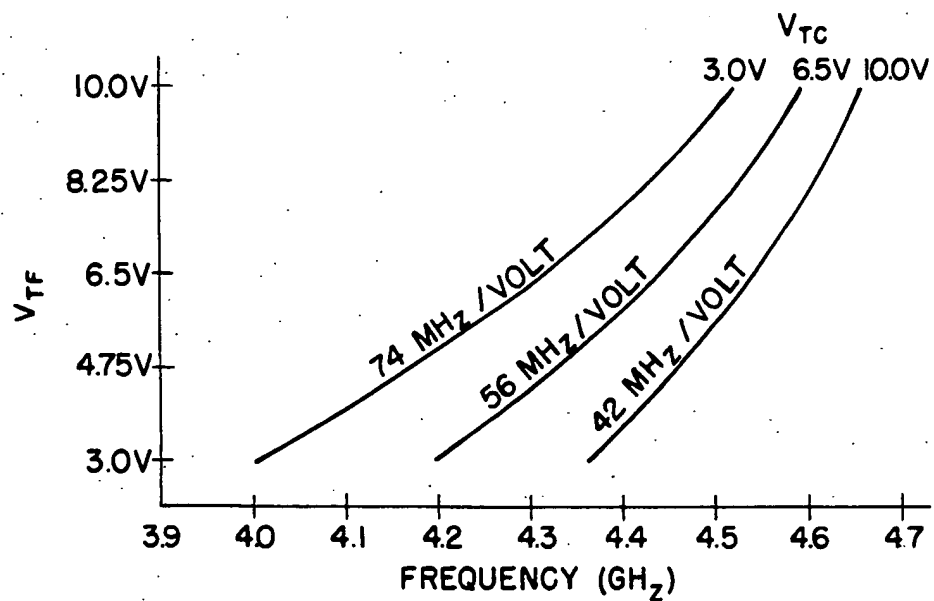
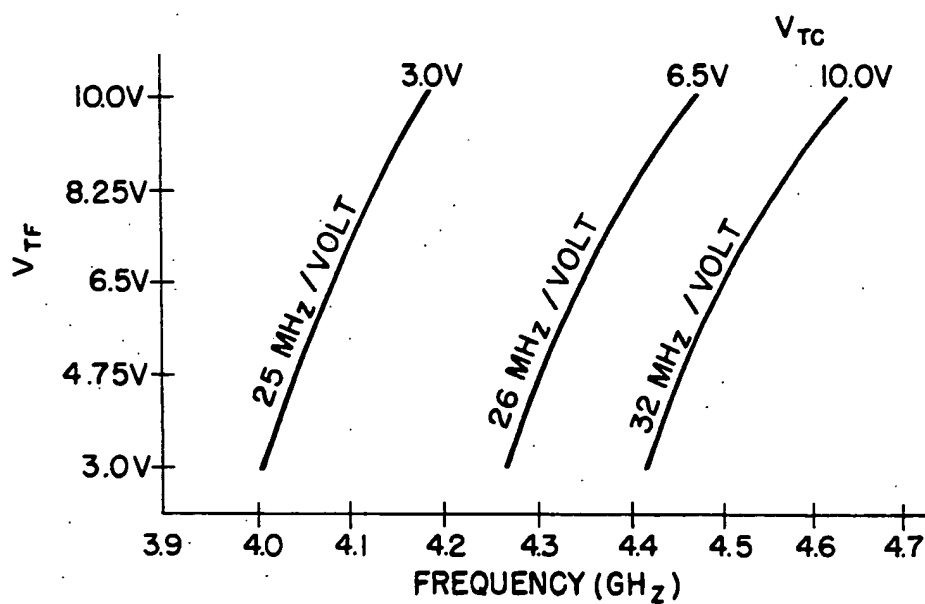




FIG. 2.FIG. 3.



## VOLTAGE CONTROLLED OSCILLATOR WITH FREQUENCY SENSITIVITY CONTROL

### BACKGROUND

This invention relates to voltage controlled oscillators and, more particularly, to a gain compensated varactor tuning network for a voltage controlled oscillator.

Voltage controlled oscillators (VCO's) are oscillators which have a frequency output which may be varied in response to an applied voltage signal. VCO's are typically employed as a component within a phase-locked loop (PLL) circuit. A PLL is typically utilized when it is desired to synchronize two signals in both phase and frequency. As an example, one signal may be a local oscillator within a communications device, while the second signal may be a received frequency.

A phase-locked loop may be characterized as a closed-loop electronic servomechanism the output of which locks onto and tracks a reference signal. Phase lock is achieved by comparing the phase of the PLL output signal to the phase of the reference signal. Any phase difference between the two signals is converted to a correction voltage, typically by a phase detector circuit. This correction voltage is applied to the VCO circuit, thereby adjusting its output frequency such that it tracks the reference frequency.

As may be appreciated, the response time of the VCO circuit to a change in the applied correction voltage is an important parameter of such a circuit, especially if the reference frequency is varying rapidly. As may be further appreciated, the control of the VCO's tuning characteristic, that is the ability of the VCO output frequency to vary in a controlled and predictable fashion with respect to a change in the correction voltage, is also an important consideration.

Achieving a specific VCO voltage-to-frequency relationship is especially difficult when the VCO uses one or more varactor diode components as frequency tuning elements. Varactor diodes are essentially two terminal semiconductor diodes wherein the inherent p-n junction capacitance is emphasized. By varying a reverse bias applied to such a varactor diode, the junction capacitance may be varied, thus making the device equivalent to a voltage controlled capacitor. By their inherent nature however, varactor diodes have an undesirable nonlinear voltage-to-capacitance relationship, that is, the capacitance varies in a nonlinear fashion with respect to the applied reverse bias voltage. Furthermore, the particular nonlinear characteristic of a varactor diode is dependent, typically, on certain specific physical characteristics of the diode. When such a varactor diode is utilized as a tuning component in a VCO, the resulting output frequency of the VCO likewise exhibits an undesirable voltage-to-frequency relationship, the frequency being dependent on the capacitance of the varactor diode. In response to the problem created by this inherent voltage-to-capacitance relationship of a varactor diode, it has been known in the prior art to utilize various linearization techniques to compensate for the undesirable nonlinearity characteristics of the varactor diode.

One such technique employs a high speed linearizing driver circuit to provide a linearized correction voltage to the VCO. Such a driver circuit is typically comprised of a high slew-rate operational amplifier combined with a breakpoint generator, the generator acting to change

the gain of the amplifier at preset "breakpoints" as the input correction voltage varies. The resulting output signal is thereby composed of a number of linear segments, the number of such segments increasing with an increasing number of breakpoints of the generator. The output linearized correction voltage is thus made to vary in a nonlinear fashion with respect to the applied correction voltage. The response time of the circuit with respect to a change in the applied correction voltage is typically in the range of 50 to 500 nanoseconds. The effect of the linearized correction voltage is to compensate for the nonlinear voltage-to-capacitance characteristic of the varactor tuning components, thereby providing a VCO having an output frequency which varies in a more linear fashion with respect to the correction voltage.

A disadvantage of such a linearizing circuit is that, in order to achieve a minimum response time to a change in the correction signal, a high-slew rate and, hence, expensive operational amplifier is required. Another disadvantage of such a circuit is that the power consumed by components of the breakpoint generator, such components typically being transistors and resistors, varies with respect to the operating frequency. Hence, the thermal time constants and thermal stability of these components are critical factors which affect the short term frequency stability of the VCO.

While the linearizing circuit as described above is adapted for use with an input analog correction voltage, it may also be utilized in a PLL which employs digital components within the feedback loop between the VCO output and the phase detector. Typically, a digital counter is utilized to divide the output frequency of the VCO. The outputs of the digital counter are applied as inputs to a digital to analog converter (DAC), whereby an analog correction voltage is produced for application to the breakpoint amplifier of the linearizing circuit. As may be appreciated, the signal delay incurred by the operation of the DAC is additive to that of the linearizer, with the resulting overall response time of the DAC linearizer combination being in the range of approximately 500 to 2000 nanoseconds.

Because of the aforementioned problems of high cost and sensitivity to thermal effects associated with the breakpoint type of linearizer, it has been known in the art to replace the breakpoint linearizer with a digital look-up table, the look-up table being disposed between the output of the counter and the input to the DAC. The look-up table is contained typically within a high speed programmable read only memory (PROM). The PROM is configured such that its address inputs are connected to the outputs of the counter. The data outputs of the PROM are connected correspondingly to the digital inputs of the DAC. In operation, the outputs of the counter address a word of data within the PROM, the PROM thereafter outputting on its data lines the data so addressed. The value of each word of data contained within the PROM is determined by a calibration procedure performed when the PLL is first constructed. During the calibration procedure, the counter is driven such that it will output all possible combinations of PROM addresses. For each such address a corresponding PROM output is determined which, when applied to the DAC, produces an analog correction voltage which provides a linear VCO voltage-to-frequency transfer function. The digital value so determined is stored in the PROM at the addressed

word. Thus, it can be seen that the aforementioned analog breakpoint linearizer is replaced with a digital look-up table contained within the PROM, the PROM providing a number of equivalent breakpoints that correspond to the number of words within the PROM. For example, if the PROM has 12 address inputs, the VCO will be linearized at the equivalent of 2,048 breakpoints.

While the aforementioned prior art table look-up scheme is suitable for modifying the voltage-to-frequency characteristics of a VCO utilizing varactor diode tuning elements, it is also disadvantageous for several reasons.

One problem created by the table look-up approach is that an additional response delay is introduced by the data access time of the PROM. This delay is additive to the delay of the DAC and results in a minimum response time delay of approximately 1000 nanoseconds.

Another problem created by this approach is that in each PLL system incorporating such a table look-up PROM, the system must be individually calibrated and the PROM custom programmed in order to compensate for the intrinsic characteristics of the VCO components, especially the nonlinearity characteristics of the varactor devices incorporated therein. This requirement for individualized system calibration is time consuming and costly, especially in relatively high production environments. An additional problem created by this approach is that if a system component is required to be changed at a later time, such as during field use, it may be necessary to recalibrate the system and program a new PROM in order to compensate for the different characteristics of the new component introduced into the system.

### SUMMARY OF THE INVENTION

The foregoing problems are overcome and other advantages are realized by a voltage controlled oscillator circuit and a method for adjusting parameters thereof to achieve a controllable modulation sensitivity by the use of both coarse and fine tuning means, at least one of which is electronically variable. In one embodiment of the invention the coarse and the fine tuning means are serially coupled together, the fine tuning means being further coupled to an active oscillatory element. The fine tuning means is comprised of a length of transmission line and a varactor, the varactor being coupled to a source of fine tuning voltage which is adjusted to select the varactor capacitance. The coarse tuning means is similarly comprised of a second length of transmission line and a second varactor, the second varactor being coupled to a source of coarse tuning voltage which is adjusted to select the varactor capacitance. The length of each transmission line is preset to a length such that each transmission line exhibits an impedance which, in combination with the controlled capacitance of the corresponding varactor, yields a VCO which has an output frequency which varies in a desired and controlled nonlinear or linear fashion with respect to the applied tuning voltage. In an alternative embodiment of the invention the fine tuning voltage is fixed, thereby fixing the capacitance of the fine tuning varactor. The resultant VCO circuit is tuned by varying the coarse tuning voltage. In a further embodiment of the invention the fine tuning varactor is replaced with a fixed capacitor, the resultant VCO circuit being similarly tuned by varying the coarse tuning voltage.

When utilized as a component within a phase locked loop circuit, such a voltage controlled oscillator pro-

vides for a fast response, minimum complexity, linear output phase locked loop without the disadvantages of the prior art linearization methods employing expensive components or individualized calibration procedures.

### BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features and other aspects of the invention are explained in the following description taken in connection with the accompanying drawings wherein:

FIG. 1 is a schematic diagram showing a voltage controlled oscillator (VCO) having a tuning network constructed in accordance with one embodiment of the invention;

FIG. 2 is a graph showing the modulation sensitivity exhibited by the VCO of FIG. 1 wherein the tuning network is constructed with components each having a given value; and

FIG. 3 is a graph showing the modulation sensitivity exhibited by the VCO of FIG. 1 wherein the tuning network is constructed with components each having another given value.

### DETAILED DESCRIPTION

With reference to FIG. 1 there is shown an exemplary voltage controlled oscillator 10 constructed in accordance with an embodiment of the invention. Oscillator 10 comprises transistor 12 and bias setting resistors 14, 16 and 18. Transistor 12 is shown as an NPN type having a collector connected to circuit ground and an emitter connected to a source of negative voltage  $-V$  through emitter resistor 14. The base of transistor 12 is biased through the voltage divider comprising resistors 16 and 18 such that transistor 12 may function as an oscillator. Regenerative feedback to sustain the oscillation of transistor 12 is provided by the intrinsic parasitic capacitance 19 present within transistor 12. The regenerative feedback provided in this manner results in a frequency of oscillation in the range of one to ten gigahertz if a bipolar device is utilized for transistor 12. If a field effect transistor (FET) device is utilized, the frequency of oscillation will be consequently higher. The frequency output of transistor 12 is coupled from the emitter through a capacitor 20 to a load (not shown).

In order to control the self-oscillatory mode of transistor 12 so that the device may be utilized as a voltage controlled oscillator (VCO), a frequency determining impedance network 22 is coupled to the base of transistor 12 through a DC blocking capacitor 23. The capacitance of capacitor 23 is chosen to be of a sufficient magnitude such that the reactance of capacitor 23 is negligible at the frequency of operation, resulting in capacitor 23 appearing essentially as a short circuit at the frequency of operation.

The frequency determining impedance network 22 comprises a fine-tuning diode device in the form of a varactor 26, a coarse-tuning diode device in the form of a varactor 32, a fine tuning high impedance transmission line 24 and a coarse-tuning high impedance transmission line 30. A fine-tuning voltage  $V_{if}$  and a coarse-tuning voltage  $V_{ic}$  are applied to varactors 26 and 32 through resistors 34 and 36, respectively, by conventional means (not shown). Resistors 34 and 36 preferably employ metal film type resistive elements, the reason being that metal film elements typically exhibit a small associated parasitic capacitance component. As shown in FIG. 1, varactors 26 and 32 are connected so that their respective anodes are coupled to the tuning voltages  $V_{if}$  and

$V_{tc}$ . The normal mode of operation for such a varactor diode device is that the device is operated in a reverse biased state, therefore the polarities of both  $V_{tf}$  and  $V_{tc}$  must be negative in the circuit as shown in FIG. 1. However, in an alternative embodiment of the invention (not shown) the varactor diodes may be connected with their cathodes coupled to the tuning voltage. If the varactors are so connected the polarity of the tuning voltage must be positive in order to properly reverse bias the varactors. Resistor 38, preferably a metal film type, provides a ground reference for varactor 26.

A second DC blocking capacitor 28 is connected between fine tuning varactor 26 and transmission line 30 to prevent the interference of coarse tuning voltage  $V_{tc}$  with varactor 26. As was described above with reference to blocking capacitor 23, the capacitance of capacitor 28 is chosen such that it presents a negligible impedance at the desired frequency or range of frequencies of operation of VCO 10.

Transmission lines 24 and 30, when terminated as described herein, may be considered to introduce a phase shift or impedance shift, thereby transforming the reactances of their corresponding varactors 26 and 32. At microwave frequencies, the transmission lines 24 and 30 are constructed of well known wave-guide microstrip, stripline or coaxial components while, at lower frequencies, a well known ladder network of discreet inductors and capacitors may be employed. The amount of phase shift introduced by transmission lines 24 and 30 at microwave frequencies is a function of their lengths and widths. By adjusting the length of such a transmission line, the reflected impedance may also be adjusted. In operation, the capacitive reactance of the coarse tuning varactor 32 is transformed by line 30, thereby providing a new reactance. This new reactance is combined with the reactance of line 24 and varactor 26, thus providing an overall reactance. This overall reactance will approach zero ohms at the resonant frequency of the oscillator. The frequency of oscillation of transistor 12 can therefore be seen to be a function of the inherent parasitic capacitance 19 of transistor 12 and the overall reactance of the impedance network comprised of transmission lines 24 and 26 and varactors 26 and 32. As may be appreciated, if the capacitances of varactors 26 and 32 are electronically varied, as will occur if the tuning voltages  $V_{tf}$  and  $V_{tc}$  are varied, the overall reactance of the aforementioned impedance network will vary. Thus it may be seen that the frequency of oscillation of transistor 12 will also vary, resulting in transistor 12 acting as a voltage controlled oscillator.

In order to better appreciate the beneficial effects conferred by the invention upon the operation of a voltage controlled oscillator, it is advantageous to construct a graph which shows a series of modulation sensitivity, or tuning, curves. Referring to FIG. 2, one such graph is illustrated. The graph of FIG. 2 is constructed by setting the coarse tuning voltage  $V_{tc}$  to a fixed value, thereby essentially setting the capacitance of varactor 32 to a fixed capacitance. The fine tuning voltage  $V_{tf}$  is then varied and the resulting output frequency of the VCO 10 is measured for several different values of  $V_{tf}$ . As may be seen by an inspection of the graph of FIG. 2, as the coarse tuning voltage  $V_{tc}$  is set at successively higher magnitudes, the rate of frequency change of the VCO 10 for a given range of  $V_{tf}$  values is correspondingly less. This tuning characteristic is known as negative gain compensation, and is dependent upon the component values selected to construct the impedance net-

work 22. As an example, the component values selected to yield the negatively compensated tuning curves of FIG. 2 are shown in TABLE 1 as follows:

TABLE 1

#	DESCRIPTION	VALUE
24	Fine Tuning Line	$Z = 120 \text{ ohms } l = 211 \text{ degrees}$
26	Fine Tuning Varactor	$C = 0.56\text{--}0.18 \text{ picofarads}$
30	Coarse Tuning Line	$Z = 80 \text{ ohms } l = 16 \text{ degrees}$
32	Coarse Tuning Varactor	$C = 1.59\text{--}0.24 \text{ picofarads}$

Referring now to FIG. 3, another graph of tuning curves is shown. The graph of FIG. 3 is constructed in a similar fashion to the graph of FIG. 2, that is, the magnitude of  $V_{tc}$  is fixed while the magnitude of  $V_{tf}$  is varied over a range of values. However, an inspection of FIG. 3 reveals that as the magnitude of  $V_{tc}$  is set at successively higher magnitudes, the rate of frequency change of the VCO 10 for a given range of  $V_{tf}$  values is correspondingly greater. This tuning characteristic is termed positive gain compensation, and is likewise dependent upon the particular values of the impedance network 22. In this example, the component values selected to yield the positively compensated tuning curves of FIG. 3 are shown in TABLE 2 as follows:

TABLE 2

#	DESCRIPTION	VALUE
24	Fine Tuning Line	$Z = 20 \text{ ohms } l = 117 \text{ degrees}$
26	Fine Tuning Varactor	$C = 15.9\text{--}2.15 \text{ picofarads}$
30	Coarse Tuning Line	$Z = 80 \text{ ohms } l = 79 \text{ degrees}$
32	Coarse Tuning Varactor	$C = 0.38\text{--}0.17 \text{ picofarads}$

An examination of the tuning curves of FIGS. 2 and 3 shows that the curves are of a varying slope exhibiting a lesser or a greater rate of change at a lower frequency. This nonlinearity results in what is known as frequency variable modulation sensitivity. This variable modulation sensitivity may have a detrimental effect on both the capture range and the noise features of a PLL circuit incorporating such a VCO if the amount of variable modulation sensitivity is unknown or uncontrolled. The aforementioned prior art tuning curve control techniques attempt to compensate for this variable modulation sensitivity by driving a tuning varactor with a nonlinear tuning voltage, creating, however, problems which have an adverse effect on either cost, complexity, or response time.

A varactor tuning network constructed in accordance with the invention does successively compensate for this nonlinearity by apportioning the components values of the transmission lines 24 and 30 and the varactors 26 and 32 such that the amount of modulation sensitivity may be accurately controlled. In other words, the lengths of transmission lines 24 and 30 and the capacitance values of varactors 26 and 32 are selected such that the resulting network 22 exhibits a controlled gain compensation curve that may fall between the curves shown in FIGS. 2 and 3. For example, the lengths of lines 24 and 30 may be adjusted such that the curves obtained are made essentially into straight line elements. The resulting network 22 exhibits therefore a constant value of modulation sensitivity over a desired range of frequencies. The specific component values utilized are of course dependent upon a variety of factors such as the range of frequencies over which the VCO will operate, the inherent circuit parasitic capacitances, and other application dependent factors. Referring once

again to FIGS. 2 and 3 and TABLES 1 and 2 above, it can be seen that a specific combination of transmission line lengths and widths and varactor values may be chosen such that a variation in tuning voltage results in corresponding linear variation in VCO output frequency. Thus, the modulation sensitivity of the VCO 10 will remain constant over a desired range of frequencies, resulting in a VCO 10 which may be said to be gain compensated or gain linear.

In similar fashion, other component values may be chosen to provide a VCO having a controlled amount of positive or negative modulation sensitivity over a range of frequencies. Thus, the overall PLL response may be made linear, which is a desired result. The VCO may be required to be linear or nonlinear in order to compensate for other PLL characteristics.

Although the tuning network of the invention has been described as having two variable tuning voltages  $V_{tc}$  and  $V_{tf}$ , it may be appreciated that if the desired range of frequencies over which operation is required is predetermined, the fine tuning voltage  $V_{tf}$  may be fixed. The magnitude of  $V_{tf}$ , if fixed, is determined such that when  $V_{tc}$  is varied, the output frequency of VCO 10 will correspondingly vary within the desired range of frequencies. As an example, and referring once again to FIG. 2, if it is desired to operate VCO 10 over a range of frequencies of 4.0 to 4.35 GHz,  $V_{tf}$  could be fixed at a magnitude of 3.0 volts. If  $V_{tc}$  is subsequently varied between 3.0 to 10.0 volts, the output of VCO 10 will vary within the desired range of frequencies.

Likewise, it may be appreciated that if the desired range of frequencies is predetermined as in the foregoing example, that  $V_{tf}$  may be eliminated altogether and the varactor 26 replaced with a suitable fixed value of capacitance, one such value being 0.56 picofarads. Of course, if varactor 26 is replaced with a fixed capacitor the blocking capacitor 28 could be eliminated from the circuit of FIG. 1.

Thus it can be seen that both a novel tuning circuit for a VCO, and a method for tuning a VCO, has been described. The characteristics of the tuning circuit are well suited for use with a VCO that is a component of a PLL, although the tuning circuit of the invention is not limited to that application. Therefore it is to be understood that the above described embodiments of the invention are illustrative only and that modifications thereof may occur to those skilled in the art. Accordingly, this invention is not to be regarded as limited to the embodiments disclosed herein, but as to be limited only as defined by the appended claims.

What is claimed is:

1. A method of tuning a voltage controlled oscillator to provide a selectable modulation sensitivity, said oscillator comprising an active element with feedback and a tuning circuit connected to said active element for inducing oscillation, said method comprising the steps of:

selecting a first and a second transmission line and a first and a second voltage variable capacitor for said tuning circuit;

connecting one end of said first transmission line to said active element;

terminating a second end of said first transmission line, said step of terminating including a connecting of said first capacitor serially between the second end of said first transmission line and a first end of said second transmission line;

terminating said second transmission line by connecting said second capacitor to a second terminal of said second transmission line;

adjusting the length of said second transmission line to provide a reactance for interaction with a capacitive reactance of said second capacitor;

adjusting the length of said first transmission line to provide a reactance for interaction with a capacitive reactance of said first and said second capacitors; and

electronically varying the capacity of one of said capacitors to select a frequency of said oscillation.

2. A tuning method according to claim 1 further comprising a step of electronically varying the capacity of the other of said capacitors to select a range of frequencies of said oscillation.

3. A tuning method according to claim 2 wherein each of said capacitors is a varactor, and each of said steps of electronically varying capacity is accomplished by applying a voltage to a varactor.

4. A tuning method according to claim 2 further wherein said step of electronically varying capacity to select a frequency is accomplished by varying the capacity of said second capacitor.

5. A tuning method according to claim 2 further wherein said step of electronically varying capacity to select a range of frequencies is accomplished by varying the capacity of said first capacitor.

6. A voltage controlled oscillator providing an output frequency having a controllable modulation sensitivity curve, said oscillator comprising;

an active element with feedback for inducing an oscillatory signal having said output frequency and a tuning circuit coupled to said active element for varying said output frequency, said tuning circuit including fine tuning means and coarse tuning means;

said fine tuning means being series connected between said coarse tuning means and said active element and comprising a first means, connected to said active element, for transforming a reactance, and a first capacitive means serially connected thereto, said first capacitive means being variable by an applied voltage; and

said coarse tuning means being serially coupled to said fine tuning means and comprising a second means for transforming a reactance, and a second capacitive means, said second capacitive means being variable by an applied voltage.

\* \* \* \* \*

[54] CMOS BIAS VOLTAGE GENERATING  
CIRCUIT

[75] Inventor: Kikuo Kimura, Tokyo, Japan

[73] Assignee: Oki Electric Industry Co., Ltd.,  
Tokyo, Japan

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[52] U.S. Cl. .... 307/297; 307/296 R;  
323/286; 323/311

[58] Field of Search ..... 323/282, 286, 311;  
363/19-21; 307/265, 296 R, 297

[56] References Cited

U.S. PATENT DOCUMENTS

4,233,672 11/1980 Suzuki et al. .... 307/296 R X  
4,300,061 11/1981 Mihalich et al. .... 307/297  
4,344,121 8/1982 Weber ..... 363/21 X  
4,355,277 10/1982 Davis et al. .... 363/21 X  
4,420,700 12/1983 Fay et al. .... 323/282 X  
4,430,582 2/1984 Bose et al. .... 307/297

Primary Examiner—Stanley D. Miller

Assistant Examiner—D. R. Hudspeth

Attorney, Agent, or Firm—Frishauf, Holtz, Goodman &  
Woodward

[57] ABSTRACT

A bias generating circuit for reducing an external DC power supply voltage to a predetermined, lower, stable DC voltage used as a power source for internal logic circuits in a semiconductor IC chip includes an oscillator for converting the external DC voltage into a pulse signal, a smoothing circuit for converting a pulse signal into the lower DC voltage, and a control circuit interposed between the oscillator and the smoothing circuit for varying the pulse duration of the pulse signal from the oscillator to a changed pulse signal, and for regulating the lower DC voltage to a predetermined amplitude in response to the voltage variation in the lower DC voltage. The control circuit comprises a CMOS inverter, a CMOS buffer circuit for varying the pulse duration of the output signal of the CMOS inverter, and a voltage compensating circuit for controlling the transconductance of the CMOS inverter in response to the variation of the lower DC voltage.

6 Claims, 4 Drawing Figures

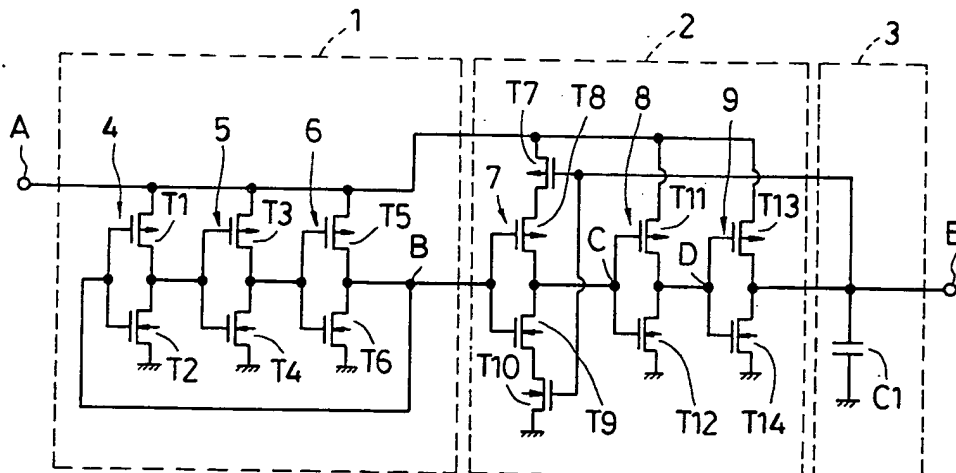


FIG. 1

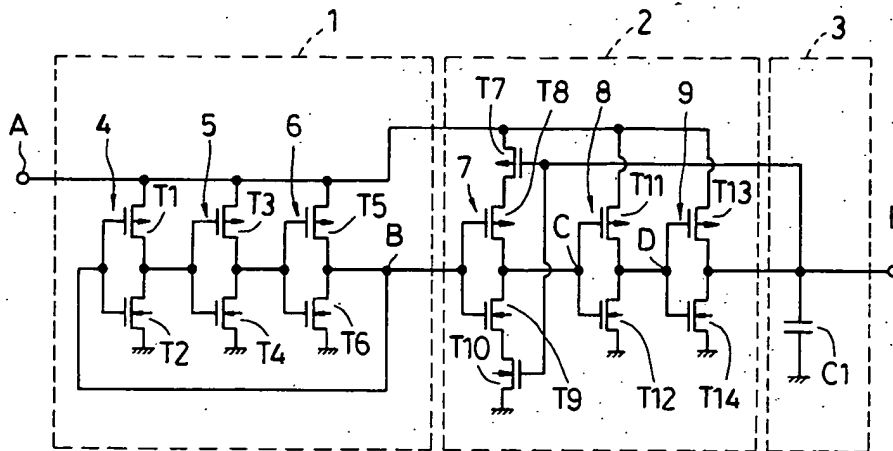


FIG. 3

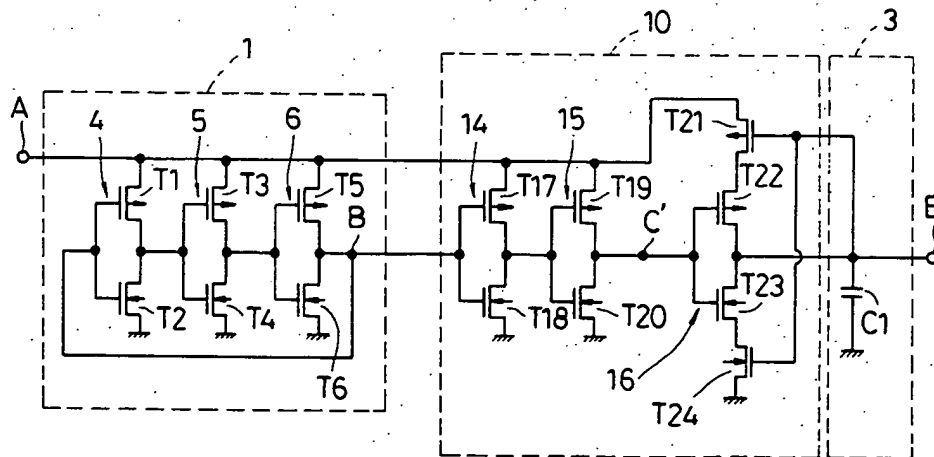


FIG. 2

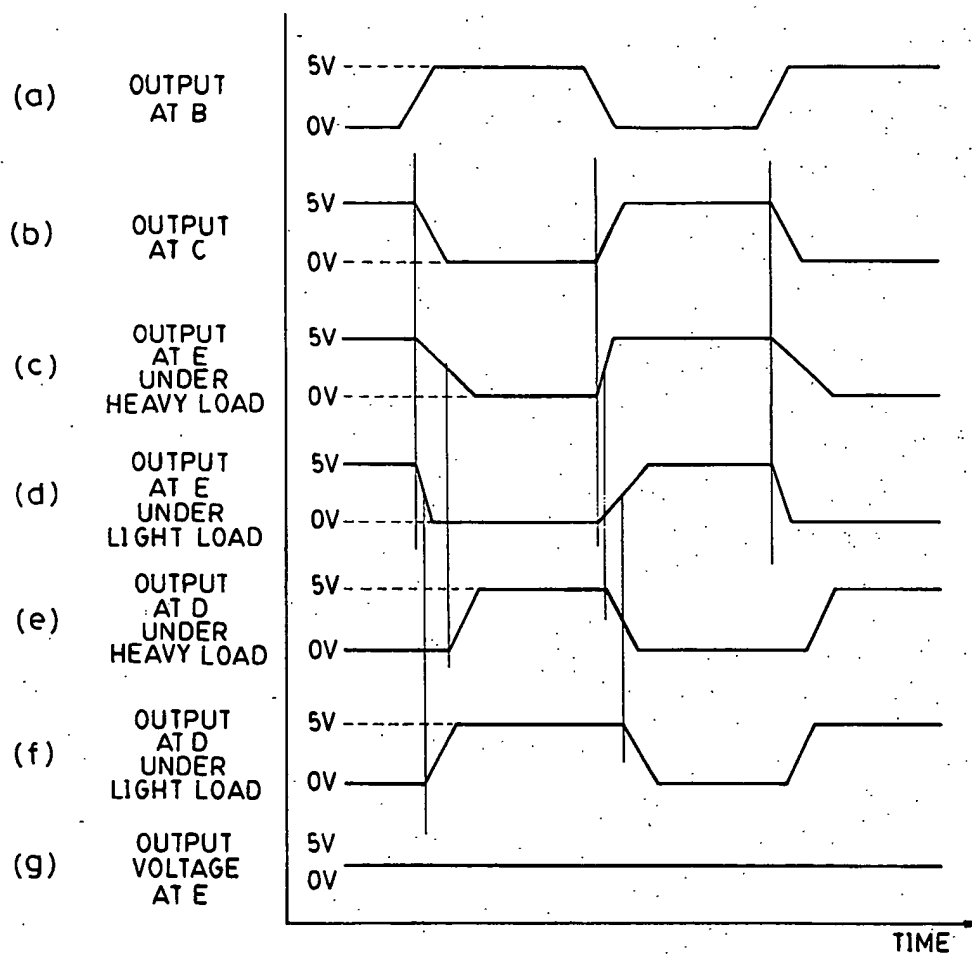
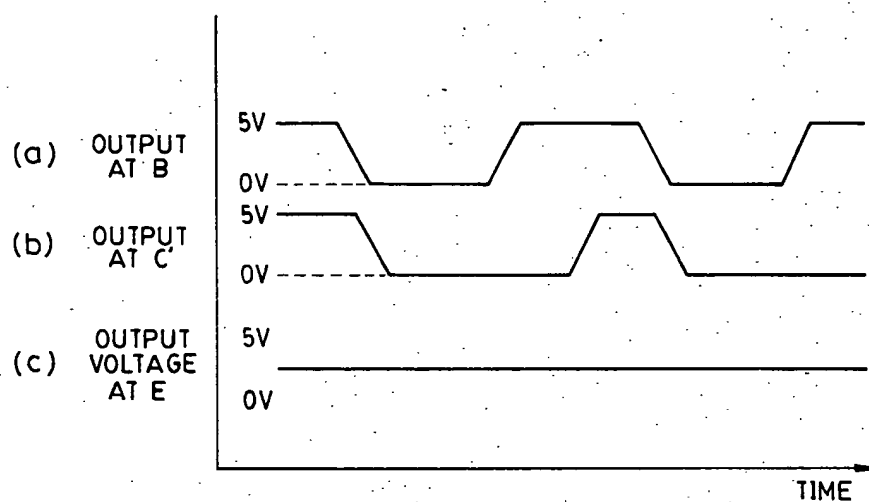


FIG. 4





## CMOS BIAS VOLTAGE GENERATING CIRCUIT

## BACKGROUND OF THE INVENTION

This invention relates to a bias generating circuit, or a DC voltage reducing circuit, suitable for an internal low voltage power source in a large-scale integrated circuit (IC) device.

In general, since digital electronic apparatuses composed of many MOS IC devices operate with TTL logic signals, the MOS IC devices are powered by using 5-volt power supply. On the other hand, MOS transistors in the MOS IC devices are remarkably being miniaturized with years. However, in the case such miniaturized MOS transistors are operated with the 5-volt power supply, they seriously suffer from hot electron and impact ionization phenomena, and the short-channel effect.

An advantageous method of precluding these adverse effects is to lower the power supply voltage. However, because system designers do not want any complexity in system design considerations and an increased number of power supplies, the 5-volt power supply has been used as a standard power source without change.

Therefore, in MOS IC devices, it is desired that the input and output circuits therein are powered on 5 volts to interface external logic circuits, while internal logic circuits are powered on a lower DC voltage (for example, 2.5 to 3 volts) of a magnitude that will not bring about the aforementioned physical phenomena.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a bias generating circuit capable of generating as an internal power source a lower, stable DC voltage for internal logic circuits in an IC chip by reducing an external DC power voltage.

Another object of the present invention is to provide a bias generating circuit which comprises a plurality of CMOS inverters.

According to the present invention, the foregoing objects are attained by providing a bias generating circuit capable of reducing an external DC power supply voltage to a lower DC bias voltage, comprising oscillating means for converting the external voltage into a first pulse signal, smoothing means for converting a second pulse signal into the lower DC bias voltage, and control means for varying a pulse duration of the first pulse signal from the oscillating means to generate the second pulse signal, and for regulating the lower DC bias voltage to a predetermined amplitude in response to a voltage variation in the lower DC bias voltage.

In one aspect of the invention, the control means includes a CMOS inverter for inverting the first pulse signal from the oscillating means, a CMOS buffer means for varying the pulse duration of the output signal of the CMOS inverter to output the second pulse signal to the smoothing means, and a voltage compensating means for controlling the transconductance of the CMOS inverter in response to the variation of the lower DC voltage.

In another aspect of the invention, the bias generating circuit includes a CMOS buffer means for varying the first pulse duration of the pulse signal from the oscillating means to output the second pulse signal, a CMOS inverter for inverting the second pulse signal from the CMOS buffer means, and a voltage compensating means for controlling the transconductance of the

CMOS inverter in response to the variation of the lower DC voltage.

Thus, according to the invention, an external DC power supply voltage can be reduced to a predetermined and highly stable DC bias voltage used for powering internal logic circuits in a semiconductor chip. The invention is applicable to all forms of semiconductor IC devices such as large-scale memory ICs and microprocessor ICs.

The above and other objects, features and advantages of the invention will be more apparent from the following detailed description taken in connection with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating a first embodiment of a bias generating circuit according to the present invention;

FIG. 2 is a waveform diagram of signals associated with the circuit of FIG. 1 and is useful in describing the operation thereof;

FIG. 3 is a circuit diagram illustrating a second embodiment of a bias generating circuit according to the present invention; and

FIG. 4 is a waveform diagram of signals associated with the circuit of FIG. 3 and is useful in describing the operation thereof.

## DETAILED DESCRIPTION

The present invention will now be described in detail with reference to the drawings.

In the description to follow, the transistors employed in the illustrated embodiments of the invention are enhancement-type MOS FETs.

Referring first to FIG. 1 illustrating a first embodiment of the invention, the bias generating circuit is shown to comprise a ring oscillator 1 for converting an external voltage (for example, 5 volts) into a pulse signal, a control circuit 2 for varying the pulse width or duration of the output signal from the ring oscillator 1 and for regulating a lower DC output voltage to a predetermined amplitude in response to the DC output voltage, and a smoothing circuit 3 for converting the pulse signal from the control circuit 2 into the lower DC output voltage.

The ring oscillator 1 comprises three CMOS inverters serially connected which include P-type MOS transistors T1, T3, T5, and N-type MOS transistors T2, T4, T6. The input of the CMOS inverter 4 and the output of the CMOS inverter 6 are connected to a point B.

The control circuit 2 comprises a CMOS inverter 7, 8, 9, a P-type MOS transistor T7 and an N-type MOS transistor T10. The CMOS inverters include P-type MOS transistors T8, T11, T13, and N-type MOS transistors T9, T12, T14. The CMOS inverters 8 and 9 are serially connected to vary the pulse duration of the output signal from the CMOS inverter 7. The CMOS inverters 8 and 9 also act as a buffer for shaping the output signal of the CMOS inverter 7.

The P-type MOS transistor T7 has its source electrode connected to the external power voltage input terminal A and its drain electrode connected to the source electrode of the P-type MOS transistor T8, and the N-type MOS transistor T10 has its source electrode connected to the ground and its drain electrode connected to the source electrode of the N-type MOS transistors T9. The gates of the MOS transistors T7 and T10

are commonly connected to an output terminal E. The P-type MOS transistors T7 varies its conductive condition by an output voltage of the terminal E to control the transconductance (gm) of the P-type MOS transistor T8, while the N-type MOS transistor T10 varies its conductive condition by an output voltage of the terminal E to control the transconductance of the N-type MOS transistor T9.

In other words, the MOS transistors T7 and T10 act as a voltage compensating means for controlling the transconductance of the CMOS inverter 7 in response to the load variation of the output terminal E.

The smoothing circuit 3 comprises a capacitor C1 connected between ground and the output terminal E. The output terminal E is connected to internal logic circuits in an MOS IC device to supply a lower DC power voltage.

According to the invention, the amplitude of the lower DC output voltage is determined by the pulse duration of the pulse signal from the control circuit 2.

The operation of the bias generating circuit having the foregoing construction in accordance with the first embodiment of the invention will now be described with reference to the waveforms shown in FIG. 2.

With the application of an external DC voltage (for example, 5 volts) to the input terminal A, the CMOS ring oscillator 1 produces a pulse signal having the waveform of (a) of FIG. 2 to the output terminal B. The pulse signal is inverted by the CMOS inverter 7 as shown in (b) of FIG. 2. The pulse signal at the point C is sent by way of the CMOS inverters 8 and 9 and is converted into a lowered DC voltage as shown in (d) of FIG. 2 by the capacitor C1.

If the output voltage across the capacitor C1 drops due to a heavy load to the output terminal E, the internal resistance of the P-type MOS transistor T7 decreases while the internal resistance of the N-type MOS transistor T10 increases. As a result, the switching of the CMOS inverter 7 becomes fast in rise time and slow in fall time, as shown in (c) of FIG. 2. The CMOS inverter 8 outputs the pulse signal as shown in (e) of FIG. 2. This results in an increase in the conductive time of the P-type MOS transistor T13, so that the voltage drop at the output terminal E is compensated for so as to increase a voltage at the output terminal E.

In the similar manner, when the voltage at the output terminal E suddenly boosts, the switching of the CMOS inverter 7 becomes slow in rise time and fast in fall time, as shown in (d) of FIG. 2. The CMOS inverter 8 outputs the pulse signal as shown in (f) of FIG. 2. This results in an increase in the conductive time of the N-type MOS transistor T14, so that the voltage boosts at the output terminal E is compensated for so as to regulate the voltage of the output terminal E.

A second embodiment of the present invention will now be described with reference to FIG. 3. The control circuit 2 in FIG. 1 is modified in FIG. 3.

A control circuit 10 comprises CMOS inverters 14, 15, 16, a P-type MOS transistor T21, and an N-type MOS transistor T24. Each CMOS inverter includes a P-type MOS transistor and an N-type MOS transistor. The CMOS inverters 14 and 15 are serially connected to vary the pulse duration of the output signal from the ring oscillator 1. The CMOS inverters 14 and 15 also act as a buffer for shaping the output signal of the CMOS ring oscillator 1.

The CMOS inverter 16 is placed between the output of the CMOS buffer 15 and the output terminal E to invert an output signal of the CMOS inverter 15. The MOS transistors T21 and T24 are controlled by a voltage at the output terminal E to adjust the transconductance (gm) of the CMOS inverter 16.

The operation of the bias generating circuit according to the second embodiment of the invention will now be described with reference to FIG. 4.

With the application of an external DC voltage (for example, 5 volts) to the input terminal A, the CMOS ring oscillator 1 produces a pulse signal as shown in (a) of FIG. 4. The pulse signal has its pulse duration varied in the CMOS inverters 14 and 15 as shown in (b) of FIG. 4. The pulse signal at the point C' is inverted by the CMOS inverter 16 and is smoothed by the capacitor C1 to convert into a lower DC voltage in response to a change in the voltage at the output terminal E, as shown in (c) of FIG. 4. The voltage variation due to a load at the terminal E is regulated by controlling the transconductance of the MOS transistors T21 and T24.

In the bias generating circuit according to the invention, the output DC voltage can be widely changed by making greater the transconductance (gm) ratio between P-type and N-type MOS transistors forming the CMOS inverter. The difference transconductance can be easily obtained by changing MOS transistors in size.

The bias generating circuit according to the invention is particularly applicable to the internal power source for semiconductor memory IC devices.

As many apparently widely different embodiments of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.

What is claimed is:

1. A CMOS bias voltage generating circuit for use in a semiconductor integrated circuit device and for reducing an external DC power supply voltage to a lower DC bias voltage, comprising:

oscillating means coupled to said external DC power supply for converting said external voltage into a first clock pulse signal;

smoothing circuit means for converting a second clock pulse signal into said lower DC bias voltage;

CMOS inverter means for inverting said first clock pulse signal from said oscillating means;

CMOS buffer means for varying the pulse duration of the output signal from said CMOS inverter means to output said second clock pulse signal to said smoothing circuit means; and

voltage compensating means for varying the transconductance of said CMOS inverter means in response to a variation of said lower DC bias voltage to regulate the pulse duration of said first clock pulse signal to thereby regulate said lower DC bias voltage to a predetermined amplitude.

2. The circuit of claim 1, wherein said voltage compensating means comprises P and N-type MOS transistors connected to said CMOS inverter means, respectively.

3. The circuit of claim 2, wherein said CMOS buffer means comprises a plurality of CMOS inverters serially connected to one another, said oscillating means comprises a CMOS ring oscillator, and said smoothing circuit means comprises a capacitor.

4. A CMOS bias voltage generating circuit for use in a semiconductor integrated circuit device and for re-

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ducing an external DC power supply voltage to a lower DC bias voltage, comprising:

oscillating means coupled to said external DC power supply for converting said external voltage into a first clock pulse signal;

smoothing circuit means for converting a second clock pulse signal into said lower DC bias voltage;

CMOS buffer means for varying the pulse duration of said first clock pulse signal from said oscillating means to output said second clock pulse signal;

CMOS inverter means for inverting said second clock pulse signal from said CMOS buffer means; and

voltage compensating means for varying the transconductance of said CMOS inverter means in re-

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sponse to a variation of said lower DC bias voltage to regulate the pulse duration of said second clock pulse signal to thereby regulate said lower DC bias voltage to a predetermined amplitude.

5 5. The circuit of claim 4, wherein said voltage compensating means comprises P and N-type MOS transistors connected to said CMOS inverter means, respectively.

10 6. A circuit as claimed in claim 5, wherein said CMOS buffer means comprises a plurality of CMOS inverters serially connected to one another, said oscillating means comprises a CMOS ring oscillator, and said smoothing circuit means comprises a capacitor.

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# United States Patent

Pfiffner

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[45] Feb. 29, 1972

## [54] HIGH-SPEED SAMPLE AND HOLD SIGNAL LEVEL COMPARATOR

[72] Inventor: Harold J. Pfiffner, Los Angeles, Calif.

[73] Assignee: Hughes Aircraft Company, Culver City, Calif.

[22] Filed: Oct. 16, 1970

[21] Appl. No.: 81,235

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[51] Int. Cl. .... H03k 5/00

[58] Field of Search .... 307/235, 289, 290; 328/150, 328/151

### [56] References Cited

#### UNITED STATES PATENTS

3,375,501	3/1968	McCutcheon et al.	328/151 X
3,469,112	9/1969	Hands et al.	328/151 X
3,548,221	12/1970	Hintz	307/289 X
3,551,697	12/1970	Candy	307/289 X

Primary Examiner—John Zazworsky

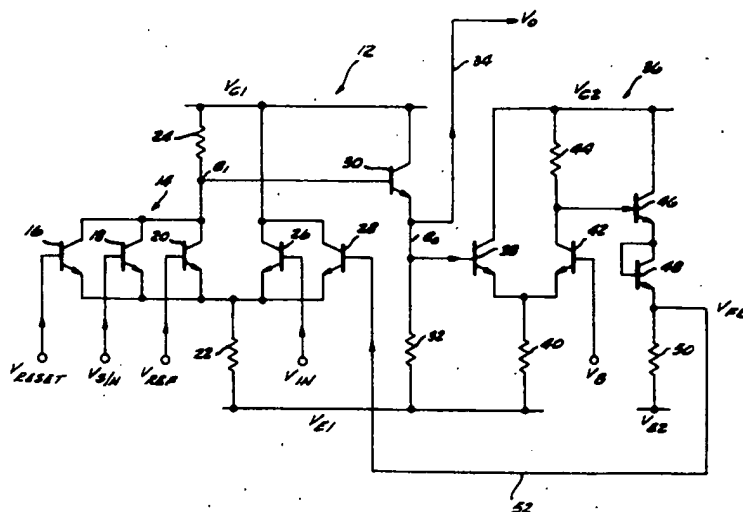
Attorney—James K. Haskell and Robert Thompson

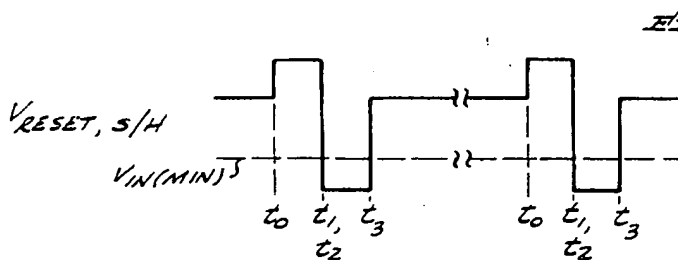
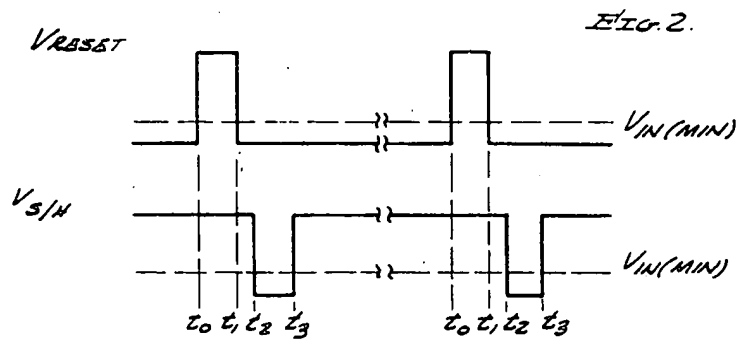
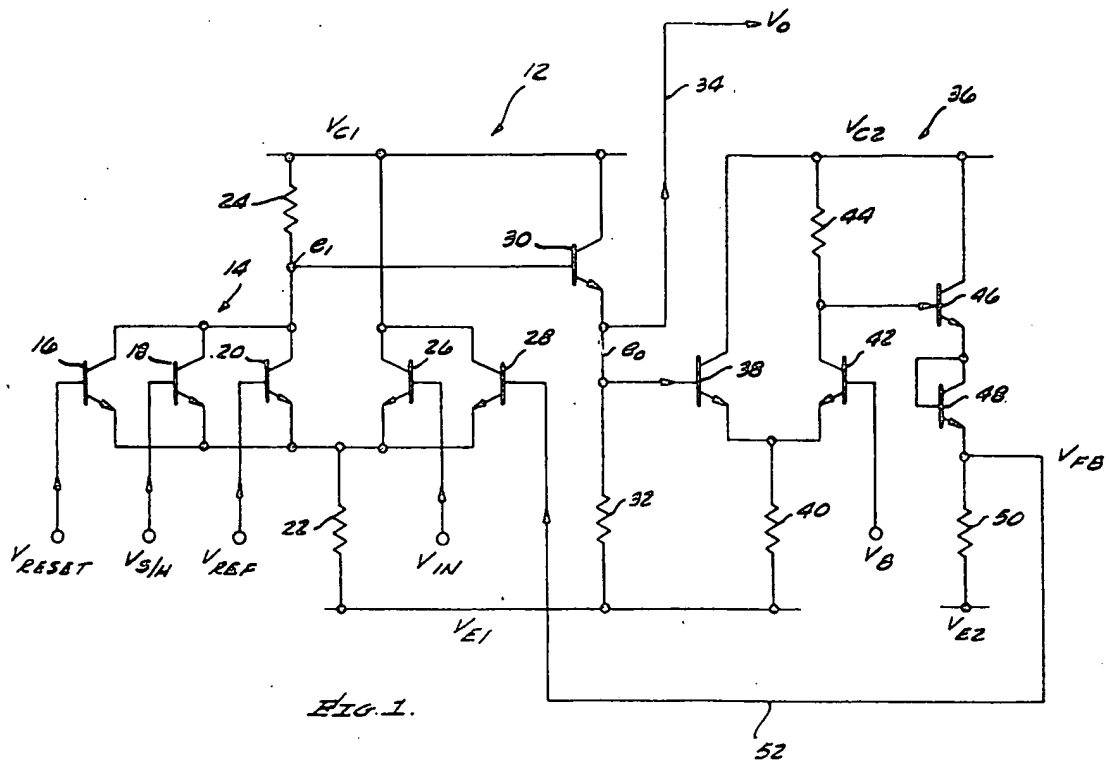
[57]

### ABSTRACT

A sample and hold comparator fabricated with emitter coupled logic using only one transistor-type, resistors, and interconnects and including a differential comparator and logic circuit for comparing an input signal  $V_{IN}$  with a reference signal  $V_{RRV}$  in response to a short duration sample and hold pulse  $V_{SH}$  to produce a digital ONE or ZERO output signal depending upon whether the compared input signal is above or below the reference signal. The differential comparator and logic circuit being further responsive to a regenerative feedback signal produced by a differential amplifier in response to the output signal for latching or holding the state of the sample and hold comparator at the comparison state so that it is not further responsive to variations in the input signal  $V_{IN}$  until after a reset pulse  $V_{RESET}$  is received by it for clearing the sample and hold comparator circuitry.

18 Claims, 3 Drawing Figures





INVENTOR.  
 HAROLD J. PFIFFNER.  
 BY  
 Robert Thompson  
 ATTORNEY

PATENTED FEB 29 1972

3,646,361

## HIGH-SPEED SAMPLE AND HOLD SIGNAL LEVEL COMPARATOR

### BACKGROUND OF THE INVENTION

This invention relates generally to logic circuitry and relates more particularly to a sample and hold signal level comparator of a type which can, for example, be utilized in analog-to-digital converters and other circuits.

There is a need for sample and hold comparator circuits having small sampling aperture times so that high speed operation can be attained. Heretofore, sample, hold, and reset operations have been accomplished with combinations of a plurality of circuit components. For example, a separate sample and hold circuit has been utilized for sampling the instantaneous magnitude of an input signal voltage and temporarily holding this sampled value. A standard comparator amplifier sensed the relative magnitude of the temporarily held sampled signal with respect to a reference voltage level and subsequently generated a logical ONE or ZERO output depending upon whether the sampled value of the input signal was greater than or less than the compared reference signal. Thereafter, an output memory flip-flop stored and detected ONE or ZERO signal until required for subsequent use.

The objectives of a sample and hold comparator having small sampling apertures and high operating speed can be attained with the provision of a comparator and switching logic which compares the voltage of an input signal with a reference signal and which has high speed switching capabilities in response to input signals such as reset pulses, sample and hold pulses, and latching capabilities in response to a regenerative feedback signal. A preferred embodiment is featured by emitter coupled logic gates preferably fabricated from NPN-transistors, resistors, and interconnect lines and which transistors are operable in their active regions below saturation. Advantages of the regenerative feedback is that it enhances switching speed and signal sensitivity as a result of a short signal propagation path within the sample and hold comparator between the input  $V_{IN}$  and the output of a feedback amplifier. In addition, the embodiment has the advantage of being capable of fabrication on a single wafer by integrated circuit techniques since all of the transistors are of the same type and the only passive elements are resistors and interconnect lines. Furthermore, the circuit has the advantage of temperature compensation since the transistors have emitter-base voltage matches having low temperature coefficients whereupon changes in temperature affect all transistors the same since the transistors temperature track equally, especially when the circuit is fabricated on a single wafer. Consequently, there is a reduced need for precision in the voltage levels of the sample and hold pulses and reset pulses. Furthermore, the circuit is capable of improving the speed of operation in analog-to-digital converters and eliminates the need for separate sample and hold circuits, comparator circuits, and output memory circuits.

### BRIEF DESCRIPTION OF THE DRAWINGS

Other objectives, features, and advantages of this invention will become apparent upon reading the following detailed description and referring to the accompanying drawings wherein:

FIG. 1 is a schematic circuit diagram of the sample and hold comparator including: a comparator and switching logic that receives an input signal  $V_{IN}$ , a reference signal  $V_{REF}$ , a sample and hold pulse  $V_{SIH}$ , a reset pulse  $V_{RESET}$ , and a feedback signal  $V_{FB}$ ; a buffer amplifier for producing a digital output signal  $V_O$ ; and a feedback amplifier responsive to the output signal for producing a regenerative feedback signal  $V_{FB}$  which latches the circuit in its compared condition;

FIG. 2 is a timing chart graphically illustrating the waveforms of the reset pulse  $V_{RESET}$  and the sample and hold pulse  $V_{SIH}$  relative to each other and the minimum level of input signal  $V_{IN}$  that the circuit of FIG. 1 will operate on; and

FIG. 3 is another embodiment of input signal waveform illustrated as a three level combined reset, sample, and hold pulse.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

The sample and hold comparator 12 illustrated in FIG. 1 compares the voltage magnitude of an input signal  $V_{IN}$  with the voltage magnitude of a reference voltage  $V_{REF}$  during the duration of a sample and hold pulse  $V_{SIH}$  (FIG. 2) to produce a positive voltage level output signal  $V_O$  which has been arbitrarily designated as a digital ONE when the magnitude of input voltage  $V_{IN}$  exceeds the reference voltage  $V_{REF}$  magnitude and to provide a relatively negative voltage output signal  $V_O$  which is arbitrarily designated as a digital ZERO when the input voltage  $V_{IN}$  is less than the reference voltage  $V_{REF}$ .

Hereinafter when a pulse voltage signal or a voltage level is referred to as being high, or going high, this should be understood as being high relative to the signal's more negative voltage state. Conversely, when the pulse signal or signal level is referred to as being low or going low, this is now relative to its more positive voltage level. Furthermore, when signal levels are referred to this is intended to, refer to voltage levels unless otherwise stated.

As will be explained in more detail, the state of the output signal  $V_O$  is used by the sample and hold comparator 12 to produce a regenerative feedback signal  $V_{FB}$  that latches the output signal state  $V_O$  so that the sample and hold comparator 12 is not further responsive to variations in the input signal  $V_{IN}$  until a high reset pulse  $V_{RESET}$  is subsequently received. The reset pulse  $V_{RESET}$  resets the sample and hold comparator's circuitry to an initial condition before any new voltage level magnitude comparisons can be made between the input signal  $V_{IN}$  and the reference voltage  $V_{REF}$ .

More specifically, the sample and hold comparator 12 is cleared and reset between the times  $t_0$  and  $t_1$  in response to a reset pulse  $V_{RESET}$  graphically illustrated in FIG. 2. For example, at time  $t_0$  the leading edge of the high reset pulse  $V_{RESET}$  which can, for example, be 1 to 2 nanoseconds in duration is received at one input terminal of a comparator and switching logic circuit 14 which produces an output signal  $e_1$  related to the relative voltage magnitudes between the input signal  $V_{IN}$  and the reference signal  $V_{REF}$ . The level of this output signal  $e_1$  controls the state of the output signal  $V_O$  in response to a sample and hold pulse  $V_{SIH}$ , holds the state of the output signal  $V_O$  in response to the feedback signal  $V_{FB}$ , and clears the sample and hold comparators circuitry to produce the low output  $V_O$  in response to the reset signal  $V_{RESET}$ . It should be pointed out that the most positive voltage level of these four input signals' waveforms applied to the comparator and switching logic 14 are related to each other in the following manner:  $V_{RESET} > V_{FB} > V_{SIH} > V_{IN}$ ;  $V_{RESET} > V_{FB} > V_{SIH} > V_{REF}$ , and  $V_{REF}$  is within full range of  $V_{IN}$ . As will be explained, the signal having the most positive voltage level at any instant of time dominates the comparator and switching logic circuit 14 by overriding all other input signals.

Assuming that the input signal  $V_{IN}$  has a voltage magnitude less than the reference voltage  $V_{REF}$ , the sample and hold comparator 12 is reset between the times  $t_0$  and  $t_1$  by a reset pulse  $V_{RESET}$  applied to the base terminal of an emitter coupled logic transistor 16 to turn NPN transistor 16 on. Coupled in parallel circuit relationship with the emitter coupled logic transistor 16 are emitter coupled logic NPN-transistors 18 and 20 in a first circuit branch. The emitter terminals of these three NPN-transistors are coupled to one end of a common emitter resistor 22 which operates as a current source and which has the other end coupled to a DC emitter voltage  $V_{E1}$ . The collector terminals of these transistors are coupled to one end of a common collector resistor 24 which has its other end connected to a DC collector voltage  $V_{C1}$ . The emitter voltage  $V_{E1}$  and the collector voltage  $V_{C1}$  are selected to operate the transistors in their active regions below saturation in response

to the base terminal input signals received by the comparator and switching logic 14. The base terminal of transistor 18 is coupled to receive the sample and hold pulse  $V_{SIH}$ , and the base terminal of transistor 20 is coupled to receive the reference voltage  $V_{REF}$ .

In addition, the base terminal of an emitter coupled logic NPN transistor 26 is coupled to receive the input voltage signal  $V_{IN}$  which transistor is in turn coupled in parallel circuit relationship with an emitter coupled logic NPN-transistor 28 in a second circuit branch. The base terminal of emitter coupled logic transistor 28 is coupled to receive a feedback voltage  $V_{FB}$ . The emitter terminal of transistor 28 is coupled in common with the emitter terminal of transistor 26 to one end of the emitter resistor 22, and their collector terminals are coupled in common to the collector voltage  $V_{C1}$ . As a result, the emitter coupled logic transistor operates as a logical differential comparator amplifier.

Operationally, since the high level of the reset pulse  $V_{RESET}$  is more positive than the most positive levels of the sample and hold signal  $V_{SIH}$  and the most positive level of the input signal  $V_{IN}$  during the time  $t_0-t_1$ , the emitter coupled logic transistor 16 is turned on and all of the other emitter coupled logic transistors 18, 20, 26 and 28 are turned off. The resultant collector current flow through the transistor 16 increases the voltage drop across resistor 24 and results in a drop in the voltage level of the output signal  $e_1$  at the junction between one end of the collector resistor 24 and the common collector terminals to its low level. This voltage signal  $e_1$  is fed to an emitter follower buffer transistor 30.

The emitter follower buffer transistor 30 is responsive to the output signal  $e_1$  from the comparator and switching logic 14 to produce the two state output signal  $V_O$  and to drive a feedback amplifier 36. Specifically, the voltage signal  $e_1$  is applied to the base terminal of emitter follower buffer transistor 30 which has its collector terminal connected to the collector voltage  $V_{C1}$  and its emitter terminal coupled to one end of an emitter follower resistor 32. The other end of resistor 32 is coupled to the emitter voltage  $V_{E1}$ . Operationally, a decrease in the voltage  $e_1$  applied to the base terminal of transistor 30 causes a corresponding decrease in the collector-emitter current conducted therethrough. This decrease in the emitter current causes a corresponding decrease in the voltage drop across emitter resistor 32 whereupon the voltage level  $e_o$  at the emitter terminal decreases. The voltage signal  $e_o$  at the emitter terminal of transistor 30 is tapped by an output line 34 to provide a low state output signal  $V_O$  which is indicative of a digital zero reset condition. In addition, the emitter voltage  $e_o$  of transistor 30 is fed to the feedback amplifier 36.

The feedback amplifier 36 is responsive to the emitter voltage  $e_o$  from the emitter follower buffer transistor 30 to produce a regenerative feedback signal  $V_{FB}$  that is fed to the comparator and switching logic 14. Specifically, the emitter signal is applied to the base terminal of an NPN-transistor 38 that forms one branch of a differential amplifier. The collector terminal of transistor 38 is coupled to a collector voltage  $V_{C2}$  and the emitter terminal is coupled to one end of an emitter resistor 40. The other end of emitter resistor 40 is coupled to the emitter voltage  $V_{E1}$ . Coupled in parallel with the transistor 38 is an NPN-transistor 42 in a second branch which has its emitter terminal coupled to the one end of emitter resistor 40 and its collector terminal coupled to one end of a collector resistor 44 which, in turn, has its other end coupled to the collector voltage  $V_{C2}$ . The base terminal of voltage amplifying transistor 42 is coupled to receive a DC base bias voltage  $V_B$  which is selected to have a voltage level between the most negative voltage of output signal  $e_o$  applied to the base terminal of transistor 38 and the most positive voltage of signal  $e_o$ . Thus, since the voltage of the low signal  $e_o$  applied to the base of transistor 38 is more negative than the base bias voltage  $V_B$  applied to transistor 42, transistor 38 is turned off and transistor 42 is turned on. The resultant collector current through collector resistor 44 causes an increase in the voltage drop thereacross and a corresponding decrease in the collector voltage.

For amplification, the base terminal of an emitter follower NPN-transistor 46, which operates as a current amplifier, receives the collector voltage signal from the differential amplifier to also decrease current flow from its collector terminal, which is coupled to the collector voltage  $V_{C2}$ , to the emitter terminal. The emitter terminal of transistor 46 is coupled to a diode connected transistor 48.

To reset the voltage level of the feedback signal  $V_{FB}$ , diode connected transistor 48 is responsive to the emitter output from transistor 46 to rereference by DC shifting the voltage level of the feedback signal  $V_{FB}$  produced at its emitter terminal to a voltage range where the low voltage level of the feedback signal  $V_{FB}$  is lower than the lowest voltage of any acceptable input signal  $V_{IN}$  and the high voltage level of the feedback  $V_{FB}$  is higher than the most positive voltage level of any acceptable input signal  $V_{IN}$ . Structurally, the diode connected resistor 48 has its base terminal connected directly to the collector terminal whereupon both will receive the emitter signal from transistor 46. The emitter terminal of NPN-transistor 48 is connected to one end of an emitter resistor 50 which has its other end coupled to an emitter voltage  $V_{E2}$ . The emitter voltage  $V_{E2}$  is a pulldown voltage which establishes current flow through the emitter resistor 50 for all signal conditions. The feedback signal  $V_{FB}$  produced at the junction between the emitter of transistor 48 and one end of emitter resistor 50 tapped by a feedback line 52 is applied to the comparator and switching logic 14. Operationally, a decrease in the emitter current of transistor 46 causes a corresponding decrease in the emitter current of diode connected transistor 48 whereupon the voltage drop across emitter resistor 50 decreases causing a corresponding drop in the feedback voltage  $V_{FB}$  to its low level. It should be noted that several diode connected transistors 48 could be used or that a Zener diode could be used for DC level shifting in other embodiments.

Since the feedback voltage  $V_{FB}$  applied to the base terminal of transistor 28 in the comparator and switching logic 14 is at a lower level than the input signal  $V_{IN}$  applied to the base terminal of transistor 26, these two transistors remain off, at least for the duration of the reset pulse  $V_{RESET}$  received by transistor 16.

Between the times  $t_1$  and  $t_2$ , where time  $t_2$  can even occur partially coincident with the reset pulse depending upon the duration of time  $t_0-t_1$  and time  $t_2-t_3$ , the reset pulse  $V_{RESET}$  goes low to a voltage level more negative than the lowest acceptable input signal  $V_{IN}$  voltage to turn off transistor 16 and the sample and hold pulse  $V_{SIH}$  remains at its high level to turn on transistor 18 because the sample and hold signal  $V_{SIH}$  now has a voltage level higher than the reset signal  $V_{RESET}$ , the reference signal  $V_{REF}$ , the input voltage  $V_{IN}$ , and the feedback signal  $V_{FB}$ . As a result, the level of the output signal  $e_1$  from the comparator and switching logic 14 remains low whereupon the conducting states and signal levels of the remainder of the circuit, and the associated output signal  $V_O$  and feedback signal  $V_{FB}$  remain substantially the same, except for substantially insignificant transient variations.

If the combined three level reset, sample and hold signal  $V_{RESET}$ ,  $V_{SIH}$  is used and applied to the base terminal of transistor 16, for example, the transistor 18 could be removed from the comparator and switching logic 14 since one transistor 16 would control the operations of reset, sample and hold.

For the assumed signal condition of input voltage  $V_{IN}$  greater than the reference voltage  $V_{REF}$ , at time  $t_2$  the sample and hold pulse  $V_{SIH}$  goes low to a voltage level more negative than the minimum input voltage  $V_{IN}$ . Thus, since the voltage of input signal  $V_{IN}$  is greater than the voltages of any of the other input signals including the reset signal  $V_{RESET}$ , the sample and hold signal  $V_{SIH}$ , the reference voltage  $V_{REF}$ , and the reset feedback voltage  $V_{FB}$ , transistor 26 is turned on while transistors 16, 18, 20, and 28 are turned off. The resulting decrease in current flow through collector resistor 24 causes a decrease in the voltage drop thereacross and a corresponding increase in the output voltage level  $e_1$  from the comparator and switching logic 14 during the time period during the times  $t_2$  and  $t_3$ .



The voltage level of the output signal  $V_O$  produced by the emitter follower buffer transistor 30 goes high in response to the high output level  $e_1$  received at its base terminal from the comparator and switching logic 14. Operationally, as the voltage  $e_1$  goes high, emitter follower buffer transistor 30 conducts more current causing an increase in the emitter current through the emitter follower resistor 32 thereby increasing the voltage drop thereacross. This increase in the voltage drop results in an increase in the voltage  $e_o$  at the emitter terminal which is tapped by output line 34 to produce the output signal  $V_O$  and which is applied to the feedback amplifier 36. This high output signal  $V_O$  is indicative of a digital ONE corresponding to the condition of the input voltage  $V_{IN}$  exceeding the reference voltage  $V_{REF}$ .

The feedback amplifier 36 is responsive to the level of output signal  $e_o$  to produce a regenerative feedback signal  $V_{FB}$  which has a high voltage level more positive than the maximum voltage level of any operationally acceptable input signal  $V_{IN}$ . Specifically, since the base bias voltage  $V_B$  applied to the base terminal of transistor 42 has been selected to be at a voltage level more negative than the maximum voltage level of the emitter follower buffer output signal  $e_o$  applied to the base terminal of transistor 38, transistor 42 is turned off and transistor 38 is turned on. As transistor 42 is turned off the collector current flow through collector resistor 44 decreases causing a decrease in the voltage drop thereacross and a corresponding increase in the collector terminal voltage.

This increased collector terminal voltage applied to the base terminal of emitter follower transistor 46 causes an increase in the emitter current that is fed to the diode connected transistor 48. This, in turn causes an increase in the emitter current of diode connected transistor 48 through the emitter resistor 50. This increase current flow through emitter resistor 50 causes an increase in the voltage drop thereacross and a corresponding increase in the voltage developed at its junction with emitter terminal of transistor 48. As previously stated, since the emitter voltage  $V_{e1}$  and the DC rereferencing level produced by the diode connected transistor 48 have been selected to place the maximum voltage of feedback signal  $V_{FB}$  to a level greater than the maximum voltage of input signal  $V_{IN}$ , the feedback voltage  $V_{FB}$  selectively turns on emitter coupled logic transistor 28 whereupon transistor 26 is turned off.

At the comparator and switching logic transistor 28 then becomes the dominant transistor since it has the most positive voltage signal applied to its base terminal thereby latching the sample and hold comparator 12 in its digital ONE state by the time  $t_3$ . The time duration for this latching operation between times  $t_2$  and  $t_3$  has been determined to be 1 to 2 nanoseconds for selected circuits. Of course, it should be understood that for lower signal levels the response speeds of the transistors would increase whereupon the time duration for the latching operation would decrease; and for higher signal levels less than the saturable levels of the transistors their operating speeds would be decreased to decrease the speed of operation of this circuit. Once the circuit is latched and held into its sampled state, variations in the input signal  $V_{IN}$  will not thereafter affect the level of output signal  $V_O$  since the feedback signal  $V_{FB}$  is the most positive signal received by the comparator and switching logic 14 until the next subsequent reset pulse is received.

At time  $t_0$  the next subsequent reset pulse  $V_{RESET}$  is received by the sample and hold comparator 12 whereupon the output signal  $V_O$  goes low to digital ZERO as the circuit is cleared for the next sampling operation. Specifically, since the high level of the reset pulse  $V_{RESET}$  is more positive than any other input signal, including the high feedback signal  $V_{FB}$ , transistor 16 is turned on and dominates the circuit current flow while transistors 18, 20, 26, and 28 are turned off. Thereafter, the sample and hold comparator 12 returns to the circuit condition described previously for the time period between times  $t_0$  and  $t_1$ . For example, the output signal  $e_1$  from the comparator and switching logic goes low base biasing emitter follower buffer transistor 30 so that the emitter current decreases causing a decrease in the emitter voltage  $e_o$  and the output voltage

$V_O$ . In addition, this emitter voltage  $e_o$  applied to feedback amplifier 36 turns off transistor 38 while transistor 42 is turned on by the base bias voltage  $V_B$  causing a decrease in the collector voltage. This decreased collector voltage applied to the base terminal of transistor 46 decreases its emitter current which is fed to the diode connected transistor 48 which in turn decrease its emitter current. This results in a decrease in the voltage level of the feedback signal  $V_{FB}$  to a level more negative than the lowest acceptable input signal  $V_{IN}$ .

It should be noted that although a substantial hold period can occur between time  $t_3$  and the next  $t_0$ , the sample and hold comparator 12 is capable of high sample rates.

Assuming a second input condition of the magnitude of the input voltage  $V_{IN}$  being less than the magnitude of the reference voltage  $V_{REF}$ , the sample and hold comparator 12 is in the same reset operating condition between times  $t_1$  and  $t_2$  as previously described.

At time  $t_2$  the sample and hold pulse goes from its dominant most positive voltage level to a low level more negative than the minimum input voltage  $V_{IN}$ . Consequently, the reference voltage  $V_{REF}$  applied to the base terminal of transistor 20 becomes the most positive voltage signal received by the comparator and switching logic 14, whereupon transistor 20 conducts and transistors 16, 18, 26, and 28 are turned off. This causes the output signal  $e_1$  from the comparator and switching logic to remain low.

The emitter follower buffer transistor 30 receives the low output  $e_1$  from the comparator and switching logic 14 to maintain its low emitter current conduction level. Consequently, the output signal  $V_O$  on output line 34 from the emitter terminal signal  $e_o$  is low for a digital ZERO condition. In addition, the signal  $e_o$  at the emitter terminal is applied to the feedback amplifier 36.

The feedback amplifier 36 is responsive to the output signal  $e_o$  from the emitter follower buffer transistor 30 to maintain the low feedback signal  $V_{FB}$ . Specifically, since the signal applied to the base terminal of transistor 38 is lower than the base bias voltage  $V_B$  applied to the base terminal of transistor 42, transistor 38 is turned off and transistor 42 is turned on thereby increasing current flow through the collector resistor 44. The resultant voltage drop across resistor 44 causes a decrease in the collector terminal voltage which is applied to the base terminal of an emitter follower transistor 46. This base bias causes a decrease in the emitter current in transistor 46 resulting in a corresponding decrease in the collector emitter current in diode connected transistor 48. The decrease current flow through emitter follower resistor 50 results in a decrease in the voltage level of the feedback signal  $V_{FB}$  to a low voltage level less than the minimum voltage level of the input signal  $V_{IN}$ .

The comparator and switching logic 14 is responsive to the low feedback signal  $V_{FB}$  and the remaining input signals so that the reference signal  $V_{REF}$ , between times  $t_2$  and  $t_3$ , remains the most positive voltage signal received. Consequently, emitter coupled logic transistor 20 remains on while transistors 16, 18, 26, and 28 remain off. Thus, the circuit operating conditions remain the same and the output signal  $V_O$  is low for a digital ZERO for the condition when the input signal  $V_{IN}$  has a lower voltage level than the reference signal  $V_{REF}$ .

At time  $t_3$  the sample and hold pulse  $V_{SIH}$  goes more positive than the maximum input signal  $V_{IN}$ . As a result, the sample and hold pulse  $V_{SIH}$  applied to the base terminal of emitter coupled logic transistor 18 turns it on whereas the lower level voltages applied to the base terminals of transistors 16, 20, 26, and 28 turn them off. Consequently, the output signal  $e_1$  from the comparator switching logic 14 remains low.

The base of emitter follower buffer transistor 30 receives the signal  $e_1$  and remains at its low conducting state. This low level of emitter current results in the lower voltage drop across emitter follower resistor 32 resulting in the low level emitter voltage  $e_o$ . This emitter voltage is fed on output line 34 as the low output signal  $V_O$  representative of a ZERO.

Similarly, the operation of the feedback amplifier 36 remains the same with transistor 38 off and transistor 42 on. The low level collector voltage for transistor 42 base biases emitter follower transistor 46 so that it continues to conduct at its low level. Similarly, diode connected transistor 48 conducts at its low level so that the emitter current produces a low voltage drop across emitter follower resistor 50. Consequently, the feedback voltage  $V_{FB}$  remains at its low level which is less than the minimum voltage level for any expected input signal  $V_{IN}$ .

The comparator and switching logic 14 receives the input signals such that the sample and hold pulse  $V_{SH}$  applied to the base terminal of emitter coupled logic transistor 18 which is now the most positive voltage signal input. Consequently, transistor 18 is turned on and transistor 20 is turned off. Transistors 16, 26, and 28 remain off. The operating condition of remainder of the sample and hold comparator 12 remains substantially the same and the level of output signal  $e_1$  from the comparator and switching logic 14 remains the same. Thus, the level of the output signal  $V_O$  from buffer transistor 30 remains at its low level digital ZERO. Thus, the sample and hold comparator circuit 12 is effectively latched in its hold state and will not be affected by voltage variation in the input signal  $V_{IN}$  until the next high reset pulse  $V_{RESET}$  is received.

Although the embodiment has been disclosed utilizing only one transistor type, it is feasible to construct other embodiments using a combination of active circuit types and that it is feasible to construct embodiment using PNP-transistors. Thus, while salient features have been illustrated and described with respect to a particular embodiment, it should be readily apparent that modifications can be made within the spirit and the scope of the invention.

What I claim is:

1. A sample and hold comparator comprising:  
comparator logic means including a plurality of emitter coupled logic transistors, having a common output circuit, said transistors being selectively coupled to receive at their respective base terminals individual ones of a plurality of input voltages including an input voltage, a reference voltage, a reset voltage, a sample and hold voltage and a feedback voltage, amplifier means coupled to said common output circuit and operable when said sample and hold voltage is applied for producing an output voltage of a first level if said input voltage is less than said reference voltage, and an output voltage of a second level if said input voltage is greater than said reference voltage; and  
feedback amplifier means responsive to the level of said output voltage for regeneratively producing said feedback voltage which is operable to maintain said output voltage of said comparator logic means.
2. The sample and hold comparator of claim 1 in which said transistors are only operable in their active regions below saturation.
3. The sample and hold comparator of claim 2 in which all of said transistors are of the same transistor type.
4. The sample and hold comparator of claim 1 in which all of said transistors are NPN transistors.
5. The sample and hold comparator of claim 1 which all of said transistors are of the same transistor type.
6. The sample and hold comparator of claim 1 wherein said comparator logic means further includes an emitter coupled logic transistor coupled to receive at a base terminal a reset voltage which overrides the other applied voltages when the reset voltage is at a level that relatively exceeds the level of the other applied voltages to switch the output voltage of said comparator logic means to the first level during the time of the reset voltage, and a second emitter coupled logic transistor coupled to receive at a base terminal a sample and hold voltage which overrides the other applied voltages to switch the output voltage of said comparator logic means to the first level when the sample and hold voltage is at a level that relatively exceeds the level of the other applied voltages.

7. The sample and hold comparator of claim 6 in which two of said plurality of emitter coupled logic transistors of said comparator logic means are operably responsive to the sample and hold voltage so that the greatest relative magnitudes of the input voltage and the reference voltage to selectively turn on one of said emitter coupled logic transistors to produce an output voltage of the first level of the second level respectively.

8. The sample and hold comparator of claim 7 wherein one of said plurality of emitter coupled logic transistors of said comparator logic means is responsive to the feedback voltage such that the reference voltage and the sample and hold voltage are operable to produce the second level output voltage of said comparator logic means when the reference voltage is relatively greater than the input voltage and the input voltage and the feedback voltage are operable to produce the first level output voltage if the input voltage is relatively greater than the reference voltage.

9. The sample and hold comparator of claim 8 in which said comparator logic means includes a plurality of emitter coupled logic transistors coupled as a logical differential amplifier having a first circuit branch with a first, a second, and a third transistor each with their collector terminals and their emitter terminals respectively coupled in common, the base terminals of individual ones of said three transistors being coupled to receive the reset voltage, the sample and hold voltage, and the reference voltage, respectively, and a second circuit branch including a fourth and a fifth emitter coupled logic transistor having their emitter terminals and their collector terminals respectively coupled in common circuit relationship and their base terminals respectively coupled to receive the input voltage and the feedback voltage.

10. The sample and hold comparator of claim 9 in which said feedback amplifier includes a differential amplifier having a first transistor coupled to receive a voltage corresponding to the output voltage at a base terminal and a second transistor coupled to receive a base bias voltage at a base terminal such that said first transistor is turned on and said second transistor is tuned off when the received output voltage is at one of the first and second levels and said second transistor is turned on and said first transistor is turned off when the received output voltage is at the other of the said first level and second level, impedance means coupled to the collector terminal of one of said transistors in said differential amplifier to produce a voltage corresponding to the level of the received input signal, and transistor means coupled to receive the last said voltage to produce a regenerative feedback voltage of a first level having a minimum voltage level relatively greater than the maximum expected input voltage and of a second level having a voltage level relatively less than the maximum expected input voltage level, the first and the second levels of the feedback voltage corresponding to the levels of the output voltages.

11. The sample and hold comparator of claim 10 in which said transistor means coupled to receive the output signal of said feedback amplifier includes means for rereferencing the voltage level of the feedback voltage signal relative to the input voltage range.

12. The sample and hold comparator of claim 10 in which said transistor means coupled to receive the output voltage of said feedback amplifier to produce a feedback voltage includes diode connected transistor means for rereferencing the voltage level of the feedback voltage relative to the input voltage range.

13. The sample and hold comparator of claim 12 further including buffer means including an emitter follower transistor having a base terminal coupled to receive the output voltage of said comparator logic means and an emitter terminal coupled to an emitter follower resistor, and the output voltage being produced by the voltage drop across said emitter follower resistor.

14. The sample and hold comparator of claim 1 wherein two of said plurality of emitter coupled logic transistors of said comparator logic means are operably responsive to the sample

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and hold voltage so that the greatest relative magnitudes of the input voltage and the reference voltage to selectively turn on one of said emitter coupled logic transistors to produce an output voltage of the first level or the second level respectively.

15. The sample and hold comparator of claim 14 wherein one of said plurality of emitter coupled logic transistors of said comparator logic means is responsive to the feedback voltage such that the reference voltage and the sample and hold voltage is operable to produce the second level output voltage of said comparator logic means when the reference voltage is relatively greater than the input voltage and the input voltage and the feedback voltage are operable to produce the first level output voltage if the input voltage is relatively greater than the reference voltage.

16. The sample and hold comparator of claim 15 in which said feedback amplifier includes a differential amplifier having a first transistor coupled to receive a signal corresponding to the output voltage at a base terminal and a second transistor coupled to receive a base bias voltage at a base terminal such that said first transistor is turned on and said second transistor is turned off when the received output voltage is at one of the first and second levels and said second transistor is turned on and said first transistor is turned off when the received output

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voltage is at the other of the said first level and second level, impedance means coupled to the collector terminal of one of said transistors in said differential amplifier to produce a voltage corresponding to the level of the received input voltage, and transistor means coupled to receive the last said voltage to produce a regenerative feedback voltage of a first level having a minimum voltage level relatively greater than the maximum expected input voltage and of a second level having a voltage level relatively less than the minimum expected input voltage level, the first and the second levels of the feedback voltages corresponding to the levels of the output voltages.

17. The sample and hold comparator of claim 16 in which said transistor means coupled to receive the output voltage of said feedback amplifier includes means for rereferencing the voltage level of the feedback voltage relative to the input voltage range.

18. The sample and hold comparator of claim 16 in which said transistor means coupled to receive the output voltage of said feedback amplifier to produce a feedback voltage includes diode connected transistor means for rereferencing the voltage level of the feedback voltage relative to the input voltage range.

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**United States Patent** [19]  
**Yamashiro**

[11] E

**Patent Number: Re. 31,749**

**[45] Reissued Date of Patent: Nov. 27, 1984**

**[54] CLASS B FET AMPLIFIER CIRCUIT**

[75] Inventor: **Osamu Yamashiro, Ohmiya, Japan**  
[73] Assignee: **Hitachi, Ltd., Tokyo, Japan**  
[21] Appl. No.: **168,777**  
[22] Filed: **Jul. 11, 1980**

**Related U.S. Patent Documents**

Reissue of:

[64] Patent No.: **4,100,502**  
Issued: **Jul. 11, 1978**  
Appl. No.: **719,238**  
Filed: **Aug. 31, 1976**

**[30] Foreign Application Priority Data**

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[51] Int. Cl.<sup>3</sup> ..... **H03F 3/16; H03F 3/26**

[52] U.S. Cl. .... **330/264; 307/270;**  
**330/267; 331/116 FE**

[58] Field of Search ..... **307/451, 270, 260-261;**  
**330/263, 264, 265, 267, 268, 277; 331/116 R,**  
**116 FE**

**[56] References Cited**

**U.S. PATENT DOCUMENTS**

2,791,644	5/1957	Sziklai	330/263
3,067,337	12/1962	Bowman	307/496
3,443,237	5/1969	Prozeller	330/301
3,566,145	2/1971	Goodale	330/264
3,676,801	7/1972	Musa	331/116 R
3,760,584	9/1973	Dargent	331/116 R
3,855,549	12/1974	Heuner et al.	331/116 R X
3,855,552	12/1974	Thanhaeuser	331/116 R
3,906,255	9/1975	Mensch, Jr.	357/51 X
3,953,875	4/1976	Cave et al.	330/307
4,015,214	3/1977	Yokoyama	330/264

**FOREIGN PATENT DOCUMENTS**

1293230	4/1969	Fed. Rep. of Germany .
1916736	10/1970	Fed. Rep. of Germany .
2502697	8/1975	Fed. Rep. of Germany ..... 330/264
52846	5/1975	Japan .
55658	5/1976	Japan .
1395337	5/1975	United Kingdom .

**OTHER PUBLICATIONS**

Kalin, "Proceedings of the National Electronic Conference"; vol. 28, Oct. 8-10, 1973, Oakbrook (U.S.) pp. 368-372.

Electronics & Nucleonics Dictionary-Markus, 1966, pp. 106-107, 3rd Ed., Group A.U. 252.

Primary Examiner—Larry N. Anagnos

Attorney, Agent, or Firm—Antonelli, Terry & Wands

**[57] ABSTRACT**

A complementary inverter amplifier circuit comprising a complementary inverter including a p-channel MIS FET connected to a first source potential, an n-channel MIS FET connected to a second source potential, the gate of the two FETs being applied with a common linear input, respective load resistors connected to the drains of the complementary FETs, an output being derived from the interconnection point of the load resistors or from the drains of the FETs, and a bias resistor connected between the gate and the drain of each of the complementary FETs, the input being supplied to the gates of the FETs through respective capacitors. The p-channel FET and n-channel FET are individually biased so that the circuit may serve as a class B push pull amplifier of low power consumption.

**16 Claims, 8 Drawing Figures**

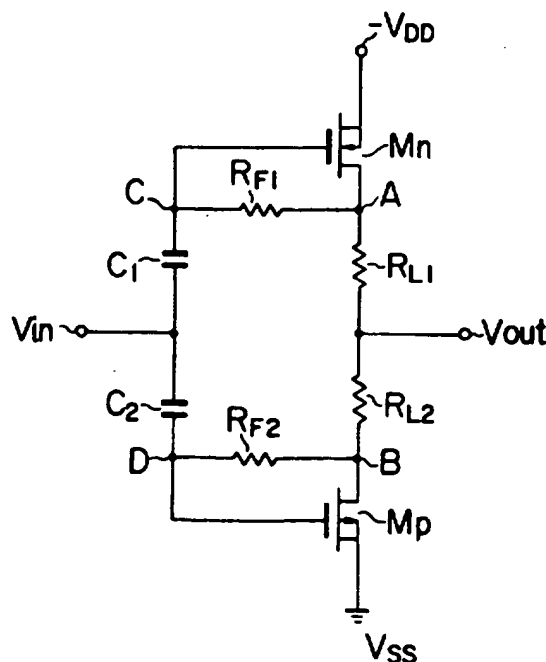


FIG. 1

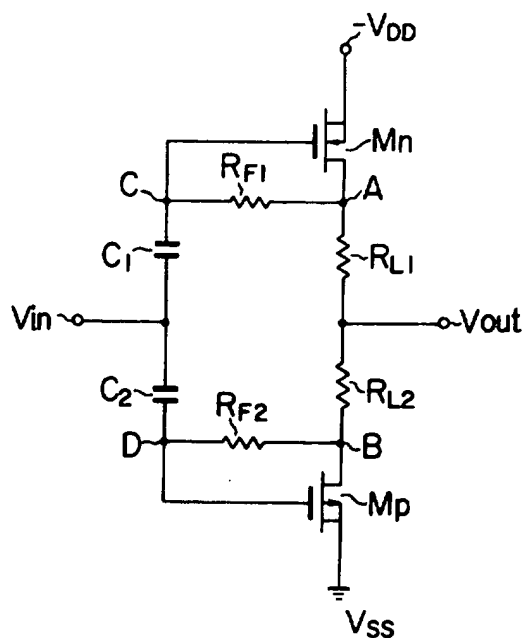


FIG. 2

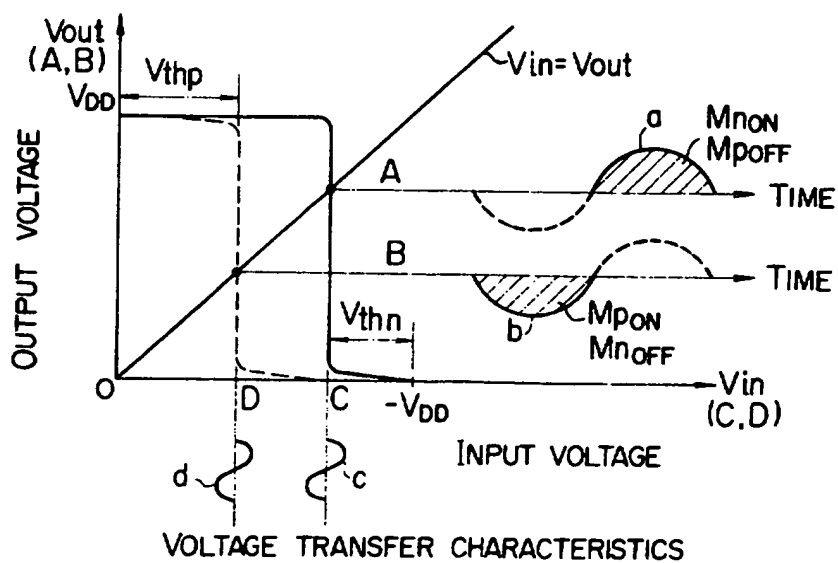


FIG. 3

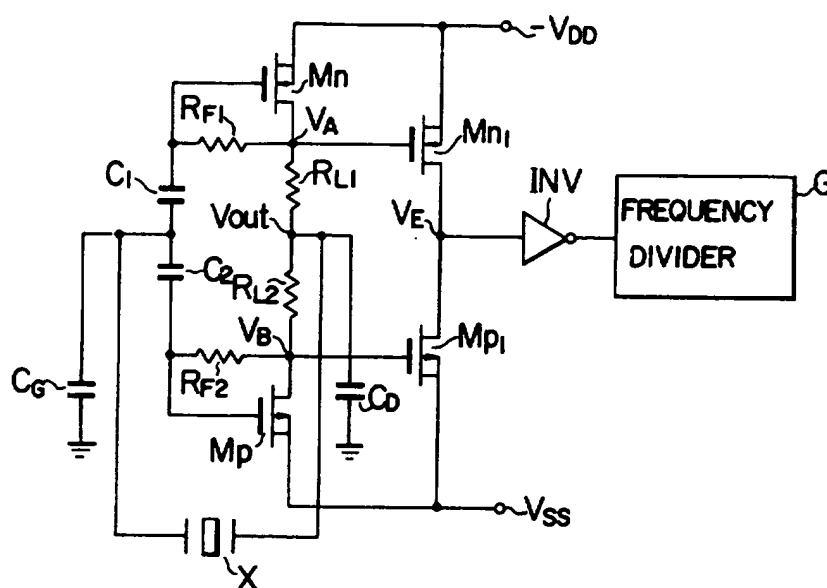


FIG. 4  
PRIOR ART

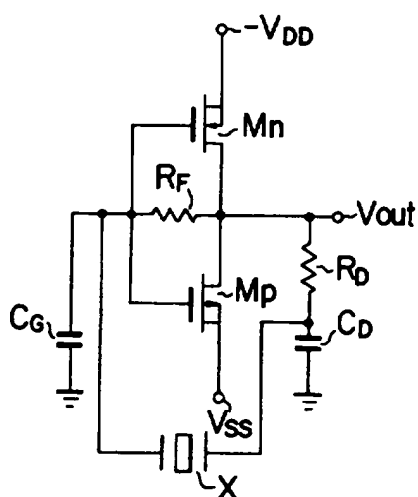


FIG. 5  
PRIOR ART

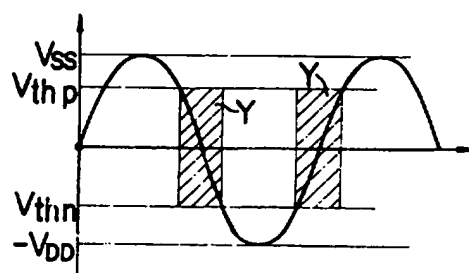


FIG. 6

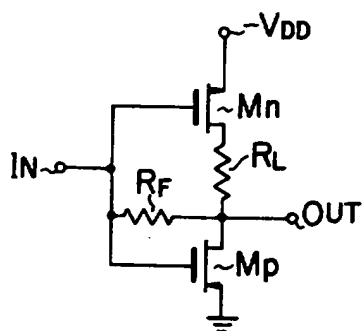


FIG. 7

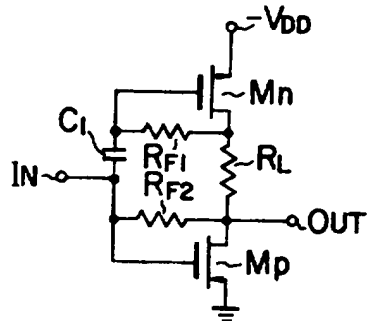
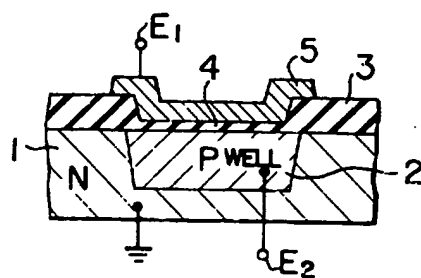


FIG. 8



## CLASS B FET AMPLIFIER CIRCUIT

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

### BACKGROUND OF THE INVENTION

#### 1. FIELD OF THE INVENTION

This invention relates to an amplifier circuit and more particularly to a complementary metal-insulator-semiconductor (C-MIS) amplifier circuit comprising a p-channel metal-insulator-semiconductor field effect transistor (referred to as MIS FET or simply as FET, hereinafter) and an n-channel MIS FET.

#### 2. DESCRIPTION OF THE PRIOR ART

Conventionally, such a circuit as shown in FIG. 4 has been known as a crystal oscillator circuit used in an electronic wristwatch from U.S. Pat. No. 3,676,801 issued to F. H. Musa, an American publication, "RCA COS/MOS Integrated Circuits Manual" by RCA Corporation, pages 192 to 205, 1972, etc. The circuit of FIG. 4 basically comprises a C-MIS inverter circuit including an n-channel FET  $M_n$  and a p-channel FET  $M_p$ , and a positive feedback circuit or a regenerative feedback loop connected between the input and output terminals of the inverter circuit and including a crystal oscillator X and capacitors  $C_D$  and  $C_G$ . A resistor  $R_D$  provided at the output of the amplifier circuit serves to stabilize the oscillation frequency.

Such a circuit as described above, however, has a problem in that the power consumption becomes large. This can be described as follows.

When the complementary inverter amplifier circuit constituting the main part of the oscillator circuit is driven with a complementary digital input signal without other components, the period during which both complementary FETs are turned on is very short and the power consumption due to the dc current passing through the two FETs caused little problem since the complementary FETs operate in a push-pull manner. When a linear (e.g., a sinusoidal) signal as shown in FIG. 5 is applied to the input terminal, however, the period during which the two FETs operate in the transfer region or in the neighborhood of the switching point (the region between the threshold voltages  $V_{thn}$  and  $V_{thp}$  of the FETs  $M_n$  and  $M_p$ , i.e., the hatched region Y in FIG. 5) becomes long and the power dissipation increases.

### SUMMARY OF THE INVENTION

An object of this invention is, therefore, to provide a complementary inverter amplifier circuit of low power consumption.

Another object of this invention is to provide a complementary inverter amplifier circuit accompanied with no loss current through MIS FETs which occurs due to the threshold voltage of the MIS devices in the case of amplifying a linear input.

A further object of this invention is to provide a complementary MIS inverter amplifier circuit serving as a linear amplifier means in an oscillator circuit and having an arrangement of preventing a loss or invalid current through the inverter in supplying an oscillation output to a waveform shaping MIS inverter of the following stage.

Another object of this invention is to provide a complementary MIS inverter amplifier circuit capable of monolithic integration and adapted for use in the circuit requiring low power consumption such as a micro-power crystal-controlled oscillator in an electronic timepiece such as an electronic wristwatch.

Another object of this invention is to provide a complementary MIS inverter amplifier circuit having a complementary MIS inverter biased to serve as a class B push-pull amplifier.

According to one aspect of this invention, there is provided a complementary inverter amplifier comprising a complementary inverter including a first FET of a first conductivity type connected to a first source potential and a second FET of a second conductivity type connected to a second source potential, an input being applied commonly to the gates of the first and the second FETs, the amplifier comprising a first and a second load resistors connected in series between the first and the second FETs, bias resistors connected between the gate and the drain of the first and the second FETs, an input being supplied to the gates of the FETs through respective capacitive elements and an output being derived from the interconnection point of the first and the second load resistors or from the drains of the first and the second FETs thereby providing a class B push-pull amplifier function.

These and other objects, features and advantages of the present invention will become more apparent from the following detailed description of the invention when taken in conjunction with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a complementary inverter amplifier according to an embodiment of this invention.

FIG. 2 shows voltage transfer characteristic curves for illustrating the operation of the circuit of FIG. 1.

FIG. 3 is a circuit diagram of an oscillator circuit including an embodiment of the amplifier circuit according to this invention.

FIG. 4 is a circuit diagram of a conventional oscillator circuit.

FIG. 5 is a graph for illustrating the reason for allowing a loss through-current in the conventional circuit of FIG. 4.

FIG. 6 is a circuit diagram of a complementary MIS FET amplifier according to another embodiment of this invention.

FIG. 7 is a circuit diagram illustrating a modification of FIG. 1.

FIG. 8 is a sectional view of an MIS capacitor illustrating an ac coupling capacitor used in the present amplifier.

Throughout the drawings, the same reference letters or characters indicate the same parts.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a complementary inverter amplifier according to an embodiment of this invention, in which the circuit is arranged to operate as a class B push-pull amplifier by appropriately selecting the operational bias point of each of FETs  $M_n$  and  $M_p$  and to achieve reduction of the power consumption.

An n-channel enhancement mode FET  $M_n$  (grounded source) connected to a potential source  $-V_{DD}$  and a



p-channel enhancement mode FET  $M_p$  (grounded source) connected to a different potential source  $V_{SS}$ , ground in this example are connected in a series fashion to form a complementary inverter. Here, between the complementary FETs  $M_n$  and  $M_p$ , two load resistors  $R_{L1}$  and  $R_{L2}$  of equivalent resistance are connected in series. Further, biasing resistors  $R_{F1}$  and  $R_{F2}$  are connected for the FETs  $M_n$  and  $M_p$  between the gate and the drain thereof, respectively. The gate of the FETs  $M_n$  and  $M_p$  are supplied with a common input signal  $V_{in}$  through respective capacitors  $C_1$  and  $C_2$  for ac coupling. An output  $V_{out}$  of the circuit is derived from the interconnection point of the load resistors  $R_{L1}$  and  $R_{L2}$ . Letters C, D, A and B denote various points shown in the figure, i.e., the gates and drains of the FETs. The purposes of this invention can be achieved by the above structure as will be apparent from the following description of the operation of the circuit.

In FIG. 2, the ordinate represents the output voltage of the FET and the abscissa the input voltage. The solid curve represents the relation between the voltages c and a at the gate C and the drain A of the FET  $M_n$ , i.e., the voltage transfer characteristic curve of the FET  $M_n$ , while the broken curve represents the relation between the voltages d and b at the gate D and the drain B of the FET  $M_p$ , i.e., the voltage transfer characteristic curve of the FET  $M_p$ . The biasing resistors  $R_{F1}$  and  $R_{F2}$  serve to equalize the dc levels of the gate and the drain voltages of the FETs  $M_n$  and  $M_p$ , respectively. The lower the biasing resistance, the better stabilized is the biasing voltage, while the higher the biasing resistance, the higher held is the amplification factor. Considering these properties, the resistances of the biasing resistors  $R_{F1}$  and  $R_{F2}$  may be selected as approximately 10 megohms and may be formed of diffused resistors, polycrystalline Si resistors or on-resistances between the source and the drain of FETs. In detail, the biasing resistors  $R_{F1}$  and  $R_{F2}$  may be formed of on-resistances of a transmission gate of high resistance in the range of several to several tens megohms, which is formed of complementary MIS FETs to enable a monolithic integrated circuit form. The MIS FETs of the transmission gate are connected in parallel between the input and output terminals of the amplifier circuit. Here, the gate of the p-channel MIS FET is connected to the power supply voltage  $-V_{DD}$  and the gate of the n-channel MIS FET to ground. Further, the higher is selected the resistance of the load resistors  $R_{L1}$  and  $R_{L2}$  compared to the on-resistance of the respective FETs, the steeper slope shows the voltage transfer characteristic curve and the closer the potential differential between the drain and the source (or gate-to-source) of each of the FETs  $M_n$  and  $M_p$  approaches the respective threshold voltage, the closer the biasing voltage approaches the threshold voltage, reducing the power consumption. Since the dc component in the input voltage  $V_{in}$  is blocked by the ac coupling or dc blocking capacitors  $C_1$  and  $C_2$ , the biasing points of the FETs  $M_n$  and  $M_p$  are determined separately and independently of the input signal level.

When an input signal  $V_{in}$ , e.g., a linear signal such as a sinusoidal wave by the oscillating operation, is applied, the voltages at the gate points as shown by C and D in FIG. 1, of the FETs  $M_n$  and  $M_p$  receiving the input signal through the respective capacitors  $C_1$  and  $C_2$  are represented by the curves c and d in FIG. 2 respectively. Then, the FETs  $M_n$  and  $M_p$  having operational points as described above provide amplified outputs a and b at the respective drain points as shown by A and

B in FIG. 1. A total output may take the combination of these signals a and b.

Therefore, in the former half of the cycle the FET  $M_p$  is turned on to generate a signal at the point B and in the latter half the FET  $M_n$  is turned on to generate a signal at the point A. Namely, the output signal in the whole cycle has a waveform as shown by the hatched areas in FIG. 2. In this way, the two FETs of the complementary type take charge of the amplification in respective half cycles to totally perform the operation of a class B push-pull amplifier.

According to the above structure, the present circuit performs the class B push-pull operation and hence the period during which the two FETs are both turned on becomes short. Thus, the period of allowing a through-current to pass becomes short and the power consumption is greatly reduced.

The above analysis holds perfectly when the circuit operates ideally. In practical use, however, there remains a small possibility of momentarily allowing the turning-on of both FETs, i.e., the flow of a through-current, from the relation to the operational speed of the FETs even in the above circuit. In such a case, however, the through-current is limited in magnitude by the load resistors  $R_{L1}$  and  $R_{L2}$  and is almost negligible. Therefore, a complementary inverter amplifier of low power consumption is provided.

The present invention is not limited to the above embodiment and various alternations and modifications would be possible.

For example, the output of the above complementary amplifier is derived from the interconnection of the load resistors  $R_{L1}$  and  $R_{L2}$  connected in series between the conduction paths of the two FETs  $M_n$  and  $M_p$  in the above embodiment, but it may be replaced by those derived from the respective drains of the two FETs according to the use or purposes. An example of such a case is shown in FIG. 3 in which the inverter amplifier is used in an oscillator circuit.

FIG. 3 shows a crystal-controlled oscillator circuit for use in an electronic wristwatch. The complementary inverter circuit according to an embodiment of this invention is used as the amplifier means and a positive feed-back circuit including a crystal oscillator X and capacitors  $C_D$  and  $C_G$  is connected between the input and output terminals of the amplifier. Generally, an output signal  $V_{out}$  of this oscillator circuit is applied to a frequency divider circuit through a waveform shaping inverter which is also called a logic circuit. Here, the following problem arises.

Since the load resistors  $R_{L1}$  and  $R_{L2}$  are provided in the complementary inverter of the oscillator circuit, the output  $V_{out}$  of the oscillator resembles a sinusoidal wave. Therefore, if such a sinusoidal wave is directly applied to an inverter of the next circuit stage, a through-current is allowed to pass through the inverter for a long period to increase the power consumption.

Therefore, in the circuit of FIG. 3, the voltages  $V_A$  and  $V_B$  at the respective drains of the FETs  $M_n$  and  $M_p$  are derived as the outputs of the complementary amplifier and are applied to the gates of an n-channel FET  $M_{n1}$  and a p-channel FET  $M_{p1}$  of a complementary inverter, respectively, whose drain electrodes are connected in common to constitute an output terminal  $V_E$ . The source electrodes of the FETs  $M_{n1}$  and  $M_{p1}$  are connected to the operating potential sources  $-V_{DD}$  and  $V_{SS}$  respectively. The output of the complementary inverter is then supplied to a frequency divider G

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through a waveform shaping inverter INV. In this arrangement, two amplified output signals  $V_A$  and  $V_B$  are supplied to the gates of the corresponding FETs  $M_N$  and  $M_P$  of the complementary inverter in the next circuit stage. Then, since no load resistor is used in this complementary inverter, a square wave is provided at an output terminal  $V_E$ . Hence, the through-current in the waveform shaping inverter INV is minimized and an oscillator circuit of low power operation is provided.

FIG. 6 shows a complementary MIS amplifier circuit according to another embodiment of this invention, in which an n-channel MIS FET  $M_N$  and a p-channel MIS FET  $M_P$  are connected in series between two operating voltage terminals, one at  $-V_{DD}$  and the other at a reference level, e.g., ground. A resistor  $R_L$  is connected between the drains of the MIS FETs  $M_N$  and  $M_P$  to suitably limit a current passing through the conduction paths of these FETs. A biasing resistor  $R_F$  is coupled between an input terminal IN and an output terminal OUT of the amplifier. The bias point for the MIS FET  $M_P$  which is set at a potential in the neighborhood of the threshold voltage  $V_{th}$  of the MIS FET  $M_P$  is shown by way of example. The gates of the complementary MIS FETs  $M_N$  and  $M_P$  are commonly in ac sense connected to the input terminal IN. Output deriving points and linear biasing of the circuit may be selected in various manners according to the need of the designer, for example, as shown in FIG. 1 or FIG. 3.

In this circuit, since the conduction current limiting resistor  $R_L$  is provided in the drain side of the amplifier FET but not in the source side, a feed-back loop as in the latter case is not formed, so that the amplifier circuit can achieve low power consumption without substantially lowering its amplification, and also, the dispersion or variation in the amplification of the amplifier due to the manufacturing dispersion of the resistance of the resistor  $R_L$  becomes small. Further, since the MIS FET  $M_P$  is biased to operate as class B amplifier, low power dissipation is successfully achieved.

FIG. 7 illustrates a modified circuit of FIG. 6 but similar to FIG. 1, in which no ac coupling capacitor is provided between the input terminal IN and the MIS FET  $M_P$  and instead, this transistor is biased directly by the biasing resistor  $R_F$ . Consequently, no attenuation of an ac input signal due to the ac coupling capacitor, which will be applied to the MIS FET  $M_P$  will occur. Also, since the number of circuit components is reduced compared with the circuit of FIG. 1, it is advantageous to produce the circuit in an IC chip. The output terminal OUT may be provided at the drain of the MIS FET  $M_N$ .

Capacitors for ac coupling capacitors  $C_1$  and  $C_2$  may be integrated in an MIS integrated circuit. Namely, an MIS capacitor for the capacitor  $C_1$  or  $C_2$  may be formed as shown in FIG. 8 using a so-called silicon-gate MOS process by which other transistors are fabricated in the same chip. In the MIS capacitive structure, a p-type semiconductor well region 2 is formed in an n-type semiconductor substrate 1 grounded to constitute one electrode of the capacitor. A silicon dioxide layer 3 is formed over the surface of the semiconductor substrate. On the surface of the well region 2 a thin silicon dioxide film 4 is formed, on which a polycrystalline silicon layer 5 is provided to constitute the other electrode of the capacitor. The electrode layer 5 is led to a terminal  $E_1$ . A p<sup>+</sup>-type diffused region (not shown) is formed in the p-type well region 2 from which another terminal  $E_2$  is formed through the silicon dioxide layer 3. Thus, the

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capacitor is formed of an MOS capacitance established between the p-type well region and the polycrystalline silicon layer 5, and is isolated from ground. The leadout p<sup>+</sup>-type region is diffused in the well region 2 simultaneously with the step of diffusing source and drain regions for other MIS elements.

It will be apparent that in the amplifier circuits described above, the polarities of the FETs may be reversed with the inversion of the polarity of the power source potentials.

Further, any circuits and/or circuit elements may be added to the basic circuit structures of the above embodiments for operating the circuit more effectively.

This invention can be widely utilized as an amplifier circuit of low power consumption adapted for monolithic integration.

What we claim is:

1. An FET circuit comprising an amplifier stage and a waveform shaping stage; said amplifier stage including a first p-channel FET and a first n-channel FET, means for biasing the gate of each of said FETs at a dc level nearly equal to its drain potential [;()], means for setting the potential differential between the source and the drain of each of said [FETs] FETs at a voltage nearly equal to its threshold voltage [;()], said potential differential setting means being coupled between the drains of said FETs, and means for supplying a linear input signal to said gates through respective capacitors; and said waveform shaping stage comprising means for converting a linear signal into a digital signal including a second p-channel FET having a gate coupled to the drain of said first p-channel FET, and a second n-channel FET having a gate coupled to the drain of said first n-channel FET and a drain coupled to the drain of said second p-channel FET, and output means coupled to the drains of the second p-channel and n-channel FETs for deriving the digital signal.

2. An amplifier circuit comprising a complementary inverter including a first FET of a first conductivity type connected to a first source potential, a second FET of a second conductivity type connected to a second source potential, and an input terminal connected to the gates of said first and second FETs, the circuit comprising:

a series connection of first and second load resistors connected between said first and second FETs; a respective bias resistor connected between the gate and the drain of each of said first and second FETs; a respective capacitor connected between the input terminal and the gate of each of said FETs; and output means connected to the drains of said FETs.

3. The amplifier circuit according to claim 2, in which said output means comprises a terminal connected to the interconnection point of said load resistors.

4. The amplifier circuit according to claim 2, in which said output means comprises a pair of terminals connected to the drains of said first and second FETs, respectively.

5. An amplifier circuit comprising, in combination, first and second operating voltage terminals of different potential level;

first and second field effect transistors (FET) of complementary conductivity type, each having a source, a gate and a drain, the sources of said complementary FETs being connected to said first and second operating voltage terminals respectively,

the gates of said complementary FETs being ac-coupled to an input terminal; and

a resistor connected between the drains of said complementary FETs, the connection between said resistor and said complementary FETs serving as an output terminal.]

[6. The amplifier circuit according to claim 5, further comprising a biasing resistor connected between the gate and the drain of at least one of said first and second FETs, the bias potential between the gate and the source of said FETs being determined at a potential nearly equal to its threshold voltage.]

7. [The] An amplifier circuit [according to claim 5, further comprising] comprising, in combination, first and second operating voltage terminals of different potential level;

first and second FETs of complementary conductivity type, each having a source, a gate and a drain, the sources of said complementary FETs being connected to said first and second operating voltage terminal respectively, the gates of said complementary FETs being ac-coupled to an input terminal;

a resistor connected between the drains of said complementary FETs, the connection between said resistor and at least one of said complementary FETs serving as an output terminal; and

bias means for applying the gates of said complementary FETs with bias voltages which have different potentials, wherein said bias means includes a first and a second biasing [resistors] resistor connected between the gates and the drains of said first and second FETs respectively, and an ac coupling capacitor connected between the gate of said first FET and said input terminal, the input terminal being connected directly to the gate of said second FET.

[8. A complementary push-pull amplifier comprising:

a p-channel FET having a source coupled to a positive power source terminal, a gate and a drain; an n-channel FET having a source coupled to a negative power source terminal, a gate and a drain; resistive means coupled between said drains of said FETs and;

means for applying an a.c. input signal to said gates of said FETs to operate said FETs in a push-pull mode.]

[9. The amplifier as defined in claim 8 further including means for applying to the gate of one of said FETs a bias voltage substantially equal to its drain d.c. potential.]

10. [The] A complementary push-pull amplifier [as defined claim 9 further including] comprising:

a p-channel FET having a source coupled to a positive power source terminal, a gate and a drain; an n-channel FET having a source coupled to a negative power source terminal, a gate and a drain; resistive means coupled between said drains of said FETs;

means for applying an a.c. input signal to said gates of said FETs to operate said FETs in a push-pull mode; bias means for applying the gate of said FETs with bias voltages which have different potentials, said bias means including means for applying to the gate of one of said FETs a bias voltage substantially equal to its drain d.c. potential; and means for applying to the gate of the other FET a bias voltage substantially

equal to its drain d.c. potential, and a d.c. blocking capacitor coupled between said gates of said FETs.

11. A complementary push-pull amplifier comprising a p-channel FET, an n-channel FET, resistive load means connected [to at least one of] between the drains of said FETs, a resistive bias means coupled between the gate and drain of [said] one [FET] of said FETs for applying a bias voltage substantially equal to the drain d.c. potential of said FET to said gate thereof, another bias means for applying the gate of the other FET with a bias voltage which has a potential different from the potential at the gate of said one FET, means for connecting said FETs and said resistive load means so that said resistive load means and the conduction paths between the sources and the drains of the respective FETs are connected in series and, means for applying an a.c. input signal to the gates of said FETs, the resistance of said load means being higher than the on-resistance of said one FET and the potential differential between the source and gate of said one FET approaching its threshold voltage and, output means coupled to the drain of at least one of said FETs for deriving at least one output signal.

[12. The amplifier as defined in claim 11 comprising a d.c. blocking capacitor coupled between the gates of said FETs, resistive bias means coupled between the gate and drain of the other FET of applying a bias voltage substantially equal to the drain d.c. potential of the other FET to the gate thereof and, output deriving means wherein said load means is coupled between the drains of both FETs so as to act as a common load for said FETs, the resistance of said load means being higher than the on-resistance of the other FET and the potential differential between the source and gate of the other FET approaching its threshold voltage, said output deriving means deriving at least one output from the node between the drains of both FETs.]

13. The amplifier as defined in claim [12] 22 in which a single capacitor is connected between the gates of said both FETs, said a.c. input signal being directly applied to the gate of one of said FETs and being applied to the gate of the other by way of said single capacitor.

[14. A complementary FET circuit comprising an amplifier stage and a succeeding state, each being comprised of complementary FETs, said amplifier stage including means for producing two output signals having d.c. potentials different from each other in response to an input signal, said succeeding stage having two input terminals for receiving said two output signals.]

[15. The FET circuit as defined in claim 14, in which each of said stages comprises a p-channel FET and an n-channel FET, the respective potential differential between the source and the drain of each FET in said amplifier stage is supplied between the source and the gate of the corresponding FET in said succeeding stage, respectively, and said respective potential differential is substantially equal to the threshold voltage of that FET.]

16. A complementary push-pull amplifier comprising: a first p-channel and a first n-channel FET; a pair of bias resistive means each connected between the gate and the drain of said each FET; another resistive means connected between the drains of said first p-channel and n-channel FETs; capacitive means connected between the gates of said first p-channel and n-channel FETs;

input means coupled to the gates of said first p-channel and n-channel FETs for applying an input signal to said gates; and

output means coupled to said drains of said first p-channel and n-channel FETs for deriving at least one output signal.

17. The amplifier as defined in claim 16 further comprising a succeeding amplifier including a second p-channel and a second n-channel FET, the drains of which are connected to each other, the gates of the second p-channel and n-channel FETs being connected to said drains of said first p-channel and n-channel FETs, respectively, the drains of the second p-channel and n-channel FETs serving as said output means.

18. The amplifier as defined in claim 17, in which said another resistive means comprises two resistive means connected in series, the node between the two resistive means serving as another output means.

19. An amplifier comprising

a first series circuit of first p-channel and n-channel FETs connected between a pair of power source terminals, and

a second series circuit of second p-channel and n-channel FETs connected between said power source terminals,

said first series circuit including resistive connection means for connecting the drain of said first p-channel FET to the drain of said first n-channel FET and bias means for applying to the gate of each of said first p-channel and n-channel FETs from the drain thereof a bias voltage substantially equal to the drain d.c. potential, and input means coupled to the gates of said first p-channel and n-channel FETs for applying an input signal to said gates, and

said second series circuit including first connecting means for connecting the drains of said second p-channel and n-channel FETs in common, and second connecting means for connecting the gates of said second p-channel and n-channel FETs to the drains of said first p-channel and n-channel FETs respectively, thereby causing respective bias points of said second p-channel and n-channel FETs to be substantially equal to those of said first p-channel and n-channel FETs, respectively, the drains of the second p-channel and n-channel FETs serving as an output means.

20. An amplifier circuit comprising:

a p-channel FET;

an n-channel FET, the conduction path between the source and the drain thereof being connected in series with the conduction path between the source and the drain of said p-channel FET between a pair of power source terminals;

means coupled between said drains of said both FETs for producing two output signals at said drains, the two output signals having different d.c. potentials, the difference between the d.c. potentials being determined by a voltage drop across said means;

first bias means coupled between said drain and said gate of said p-channel FET for causing the gate potential to respond to the drain d.c. potential thereof;

second bias means coupled between said drain and said gate of said n-channel FET for causing the gate potential to respond to the drain d.c. potential thereof; and means for applying an input signal to both gates of said FETs.

21. A complementary inverter amplifier circuit comprising, in combination,

a first and a second inverting amplifier device of complementary types each having a common electrode, an input electrode and an output electrode and operating in push-pull mode;

a power source, the both ends of which are coupled between said common electrodes for applying an operating energy to said first and second inverting amplifier devices;

an input terminal for applying an input signal to said input electrodes of said first and second inverting amplifier devices in common-mode;

bias means for applying said input electrodes of said first and second inverting amplifier devices with bias voltages which have different potentials;

an a.c. coupling capacitor coupled between said input electrodes of said first and second inverting amplifier devices;

a circuit device coupled between said output electrode of said first and second inverting amplifier devices for producing two output signals which have a phase being opposite to the phase of the common-mode signals at said input electrodes of said first and second inverting amplifier devices, and which have different d.c. potentials; and

a succeeding complementary inverter amplifier stage having two input terminals for receiving said two output signals and having an output terminal for deriving an output signal which has the same phase as said common-mode signals at said input electrodes of said first and second inverting amplifier devices.

22. A complementary push-pull amplifier comprising a p-channel FET, an n-channel FET, resistive load means connected between the drains of said FETs, a resistive bias means coupled between the gate and drain of one of said FETs for applying a bias voltage substantially equal to the drain d.c. potential of said FET to said gate thereof, another resistive bias means coupled between the gate and the drain of the other FET for applying a bias voltage substantially equal to the drain d.c. potential of the other FET to the gate thereof, a d.c. blocking capacitor coupled between the gate of said FETs, means for connecting said FETs and said resistive load means so that said resistive load means and the conduction paths between the sources and the drains of the respective FETs are connected in series and, means for applying an a.c. input signal to the gates of said FETs, the resistance of said load means being higher than the on-resistance of said one FET and the potential differential between the source and gate of said one FET approaching its threshold voltage, and output deriving means wherein said load means is coupled between the drains of both FETs so as to act as a common load for said both FETs, said output deriving means deriving at least one output from the drains of both FETs.

\* \* \* \* \*

[54] BIAS-VOLTAGE GENERATOR

[75] Inventor: Setsuo Kurafuji, Yokohama, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

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[52] U.S. Cl. .... 307/296 R; 307/297;  
307/304; 307/471; 331/108 C

[58] Field of Search ..... 307/296, 297, 304, 200 B;  
331/108 C

[56] References Cited

U.S. PATENT DOCUMENTS

3,806,741 4/1974 Smith ..... 307/304  
4,115,710 9/1978 Lou ..... 307/200 B  
4,142,114 2/1979 Green ..... 307/297

4,266,151 5/1981 Hoffman et al. .... 307/297

Primary Examiner—Larry N. Anagnos

Assistant Examiner—B. P. Davies

Attorney, Agent, or Firm—Staas & Halsey

[57] ABSTRACT

A substrate bias-voltage generator is comprised of an oscillator, and a charge pumping circuit, driven by the oscillator via a coupling capacitor, which transfers accumulated electric charges, out of the semiconductor substrate. The oscillator frequency is varied in accordance with the variation of the voltage level of the semiconductor substrate, preferably by means of an RC circuit, fabricated by a MOSFET variable resistance (R) and a capacitor (C), within a ring oscillator or a multi-vibrator. The gate electrode of the MOSFET variable resistance is directly connected to the semiconductor substrate.

5 Claims, 10 Drawing Figures

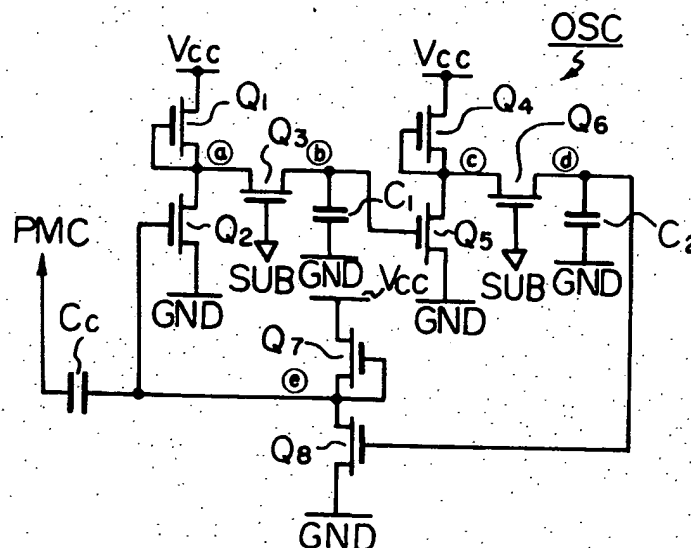


Fig. 1

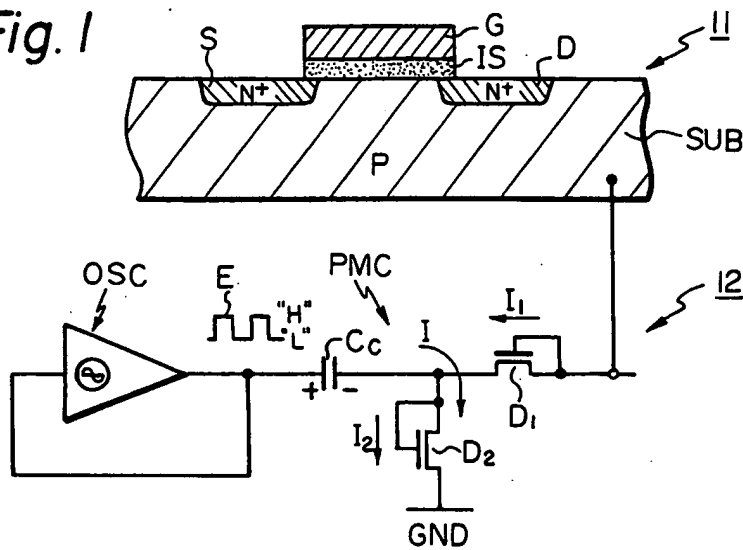


Fig. 2

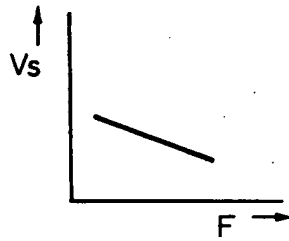
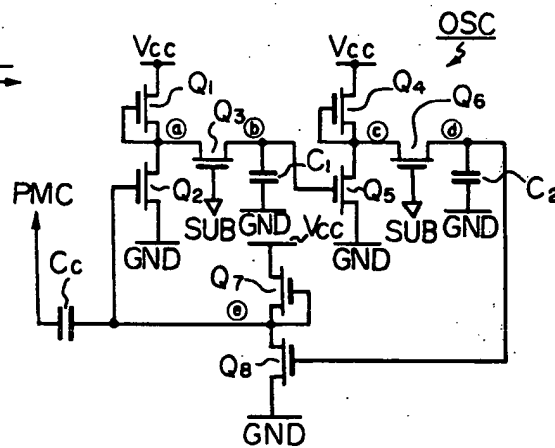
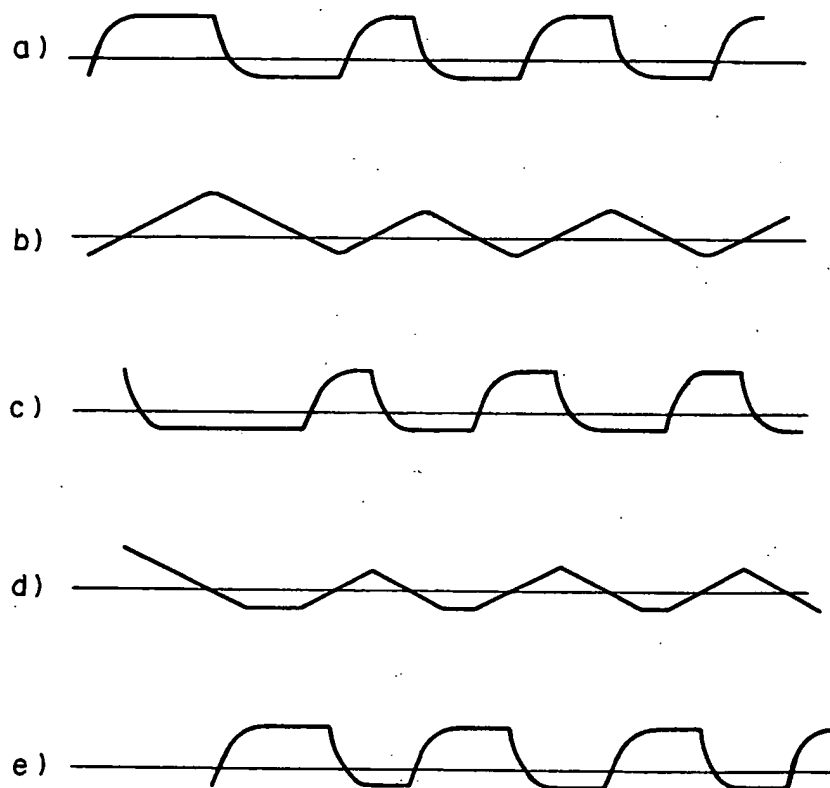


Fig. 3



*Fig. 4*



*Fig. 5*

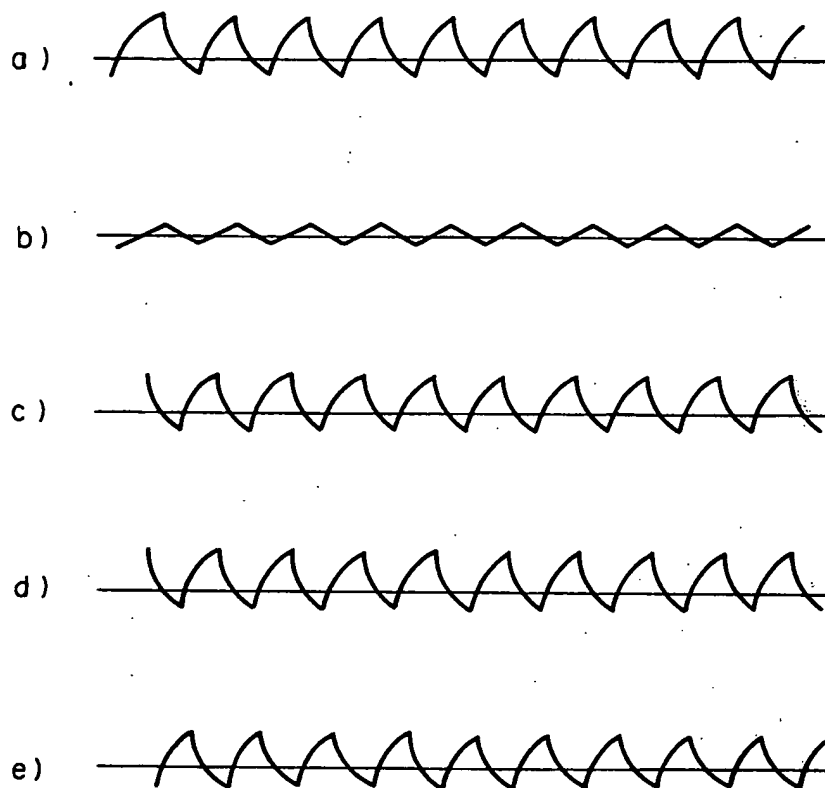
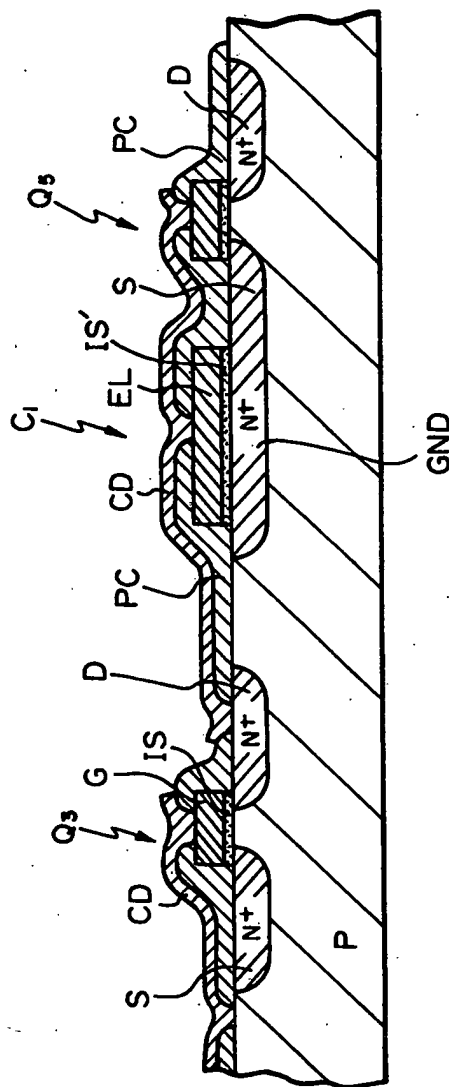








Fig. 10



## BIAS-VOLTAGE GENERATOR

### BACKGROUND OF THE INVENTION

The present invention relates to a bias-voltage generator, and more particularly to a bias-voltage generator producing a bias voltage to be applied to a semiconductor substrate on which a MOS (Metal Oxide Semiconductor) integrated circuit is mounted.

Generally, the MOS integrated circuit is provided with the bias-voltage generator so as to establish and maintain the desired optimum circuit operation of each of the semiconductor devices, such as FETs (Field Effect Transistors), which constitute the MOS integrated circuit. For instance, if the threshold voltage is below a specified or nominal level, the semiconductor device is unstable in operation, as it may be improperly rendered conductive by a noise signal, and is thus particularly unsuitable for use in logic circuits. However, if the threshold voltage is greater than the desired level, the speed of the operation of the semiconductor device is reduced, and the semiconductor device may fail to be turned on when an input signal is applied to the control electrode. Thus, the level of the threshold voltage must be maintained at a desired optimum level. The maintenance of the level of the threshold voltage at a desired optimum level is achieved by the bias-voltage generator, whose function is to absorb the so-called substrate current which flows through the substrate.

In the prior art, such a bias-voltage generator has been proposed in, for example U.S. Pat. No. 3,806,741, entitled SELF-BIASING TECHNIQUE FOR MOS SUBSTRATE VOLTAGE, by Frederick J. Smith. In this technique the bias-voltage generator can absorb the substrate current in such a manner that the amplitude of the current varies in accordance with the variation of the operating frequency of a dynamic-type circuit, for example a dynamic-type storage device in which there is a lower limit which respect to the operating frequency. This is because such a dynamic-type storage device is operated by using electric charges stored in the stray capacitances.

Briefly speaking, in the above mentioned prior art bias-voltage generator, the output signal to be produced from the bias-voltage generator and supplied to the substrate, varies in magnitude of the voltage thereof in accordance with the variation of the operating frequency of the dynamic-type circuit.

Contrary to the above, in the present invention, as will be explained hereinafter, the output signal to be produced from the bias-voltage generator and supplied to the substrate, varies in frequency in accordance with the variation of the voltage level of the semiconductor substrate.

In recent years, a great number of MOS devices, for fabricating a desired MOS integrated circuit, have been mounted on a single semiconductor chip with a very high degree of integration. Accordingly, in each MOS device, the channel between the drain and the source thereof should considerably be shortened in length. Thus, a very short channel must be formed therein. However, as the length of the channel becomes shorter, the intensity of the electric field created adjacent to the drain becomes stronger. As a result, an impact ionization current is induced across the electric field. At this time, separated holes and electrons move in respective directions. That is, the electrons move toward the drain, while the holes move toward the substrate. These sepa-

rated holes and electrons create a bad effect on the normal operation of a MOS integrated circuit. In particular, the holes absorbed into the substrate create a serious problem. This is because the voltage level of the substrate, with respect to a ground of a MOS integrated circuit, is unnecessarily increased by the holes themselves, from the optimum voltage level.

### SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a bias-voltage generator which can also suppress the undesired increase of the voltage level of the semiconductor substrate.

### BRIEF DESCRIPTION OF THE DRAWING

The present invention will be more apparent from the ensuing descriptions with reference to the accompanying drawings wherein:

FIG. 1 illustrates both a typical conventional MOSFET, as a sectional view thereof, and a conventional bias-voltage generator, as an equivalent circuit diagram thereof;

FIG. 2 is a graph used for explaining a relationship between the oscillating frequency  $F$  of an oscillating AC signal  $E$  shown in FIG. 1 and the voltage level  $V_s$  of a substrate  $SUB$  shown in FIG. 1;

FIG. 3 illustrates an equivalent circuit diagram of a first embodiment for constructing an oscillator including RC circuits according to the present invention;

FIG. 4 depicts waveforms of signals appearing in the circuit shown in FIG. 3;

FIG. 5 depicts waveforms of signals appearing in the circuit shown in FIG. 3, provided that one of the RC circuits is removed therefrom;

FIG. 6 illustrates an equivalent circuit diagram of a second embodiment for constructing an oscillator, including the RC circuits according to the present invention;

FIG. 7 depicts waveforms of signals appearing in the circuit shown in FIG. 6;

FIG. 8 illustrates an equivalent circuit diagram of a third embodiment for constructing an oscillator, including the CR circuit according to the present invention;

FIG. 9 depicts waveforms of signals appearing in the circuit shown in FIG. 8; and

FIG. 10 is a cross sectional view of, for example MOSFET  $Q_3$ , capacitor  $C_1$  and MOSFET  $Q_5$  shown in FIG. 3.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, which illustrates both a typical conventional MOSFET, as a sectional view thereof, and a conventional bias-voltage generator, as an equivalent circuit diagram, the reference numeral 11 represents the typical conventional MOSFET, as a sectional view thereof, and the reference numeral 12 represents the conventional bias-voltage generator. The MOSFET 11 is comprised of a semiconductor substrate  $SUB$ , for example a P-type substrate, a source  $S$ , which is an  $N^+$ -type region formed in the substrate  $SUB$ , a drain  $D$ , which also is an  $N^+$ -type region formed therein, and a gate electrode  $G$ , which is a conductive layer of e.g., aluminum or poly-silicon. The conductive layer ( $G$ ) is formed on a thin insulation layer  $IS$ , made of silicon dioxide ( $SiO_2$ ). The insulation layer  $IS$  is located above

the channel created between the source S and the drain D.

As previously mentioned, the length of the channel is very short, so as to realize a MOS integrated circuit with a high degree of integration. Therefore, holes are absorbed into the substrate SUB due to the presence of the impact ionization current. Thus the voltage level of the substrate SUB varies in accordance with the variation of the amplitude of the impact ionization current.

However, the conventional bias-voltage generator 12 cannot respond to such variation of the voltage level of the substrate SUB, but merely functions to absorb the constant substrate current. The operation of the conventional bias-voltage generator 12 is as follows. The generator 12 is comprised of an oscillator OSC producing an oscillating AC signal E therefrom, a coupling capacitor Cc connected, at one end, to the oscillator OSC, a charge pumping circuit PMC connected, firstly to the other end of the coupling capacitor Cc, secondly to a ground GND of the MOS integrated circuit, and lastly to the substrate SUB on which the MOS integrated circuit is mounted. The charge pumping circuit PMC is comprised of a first diode D<sub>1</sub> and a second diode D<sub>2</sub>. To be more specific, the diode D<sub>1</sub> is made up of a MOSFET in which the drain and the gate electrode thereof are shorted. Therefore, a current I<sub>1</sub> flows in the direction of the arrow shown in FIG. 1. The diode D<sub>2</sub> is made of a MOSFET in which the drain and the gate electrode thereof are shorted. Therefore, a current I<sub>2</sub> flows in the direction of the arrow indicated in FIG. 1. The bias-voltage generator 12, including a charge pumping circuit PMC therein, has merit in that the generator 12 does not require a two-level voltage source, but only a single voltage source.

When the MOS integrated circuit, mounted on the substrate SUB is activated, and accordingly the bias-voltage generator 12 is also activated, the generator 12 produces the oscillating AC signal E. The signal E is a pulse train, the voltage level of which changes between "H" (high) level and "L" (low) level, alternately. When the voltage level is "H", the current I<sub>2</sub> flows through the coupling capacitor Cc and the diode D<sub>2</sub>, to the ground GND. The ground GND is a ground of the MOS integrated circuit and is not electrically connected to the substrate SUB. When the current I<sub>2</sub> flows through the capacitor Cc (at this time, the current I<sub>1</sub> does not flow), the capacitor Cc is charged with polarities (+, -) indicated in FIG. 1. Next, when the signal E having the level "L" is produced, the current I<sub>1</sub> flows through the diode D<sub>1</sub> and the capacitor Cc, into the oscillator OSC (at this time, the current I<sub>2</sub> does not flow). Since the current I<sub>1</sub> is created by electric charges (holes), accumulated in the substrate SUB, the voltage level of the substrate SUB can be reduced as the current I<sub>1</sub> is absorbed from the substrate SUB. Thus, the voltage level of the substrate SUB is maintained at a negative level, such as -3V, with respect to the level of the ground GND. It should be noted that the conventional charge pumping circuit PMC absorbs a constant amount of electric charges (holes) per unit of time from the substrate SUB. Consequently, the circuit PMC cannot proportionally follow the variation of the voltage level of the substrate SUB, induced by the variation of the amplitude of the impact ionization current.

Although the bias-voltage generator, which is disclosed in the aforesaid U.S. Pat. No. 3,806,741, can proportionally follow the variation of the operating frequency of the dynamic-type device, it cannot follow

the variation of the voltage level of the substrate SUB, so that the voltage level cannot be maintained at a predetermined optimum level. In addition, the bias-voltage generator of the U.S. Pat. No. 3,806,741 follows said variation of the operating frequency by controlling the level of the magnitude of the voltage level of the output signal to be produced therefrom.

In the present invention, the bias-voltage generator can follow the variation of the voltage level of the substrate SUB. Further, the bias-voltage generator of the present invention does not require a special means for monitoring the variation of the voltage level of the substrate SUB. Furthermore, the bias-voltage generator of the present invention does not operate to vary the level of the magnitude of the voltage level of the oscillating AC signal, as does the generator of the aforesaid U.S. patent, but instead varies the oscillating frequency of the oscillating AC signal E. If the oscillating frequency of the signal E is relatively high, the voltage level of the substrate SUB decreases toward a negative level sharply, while, if the oscillating frequency of the signal E is relatively low, the voltage level of the substrate SUB increases toward a positive level. The relationship between the frequency F of the signal E and the voltage level V<sub>s</sub> of the substrate will be clarified with reference to a graph depicted in FIG. 2. As seen from the graph of FIG. 2, the voltage level V<sub>s</sub> has a linear relationship with respect to the oscillating frequency F. As will be apparent from descriptions mentioned hereinafter, the voltage level V<sub>s</sub> can easily and simply be controlled by varying the oscillating frequency F, when compared with the prior art control by varying the level of the magnitude of the oscillating AC signal. Thus, an oscillator (OSC), contained in the bias-voltage generator according to the present invention, produces the oscillating AC signal having variable frequency. The frequency thereof varies in proportion to the variation of the voltage level of the substrate SUB. To be more specific, the oscillator contains therein a means for varying the frequency of the AC signal, based on the voltage level of the substrate SUB. The means for varying the frequency, according to the present invention, is constructed as an RC circuit, comprised of a capacitor (C) and a variable resistance (R). The resistance value of the variable resistance (R) varies in reverse proportion to the voltage level of the substrate SUB. To achieve this, the resistance value of the variable resistance (R) might be controlled by a means for monitoring the variation of the voltage level of the substrate SUB. However, according to the present invention, such a means for monitoring is not required, but instead a MOSFET is employed, the gate of which is directly connected to the substrate SUB. Further it should be noted that the MOSFET also functions as the variable resistance itself of the RC circuit, simultaneously. The capacitor (C) of the RC circuit can be fabricated, as is usually done, by an insulation layer, such as silicon dioxide (SiO<sub>2</sub>), formed on the surface of the substrate SUB.

As previously mentioned, the oscillator contains therein the RC circuit and cooperates therewith. FIG. 3 illustrates an equivalent circuit diagram of a first embodiment for constructing the oscillator (OSC) including the RC circuit therein, according to the present invention. The oscillator OSC of the present invention is comprised of an odd number of inverters and at least one RC circuit, connected in series so as to form a ring oscillator, as shown in FIG. 3. To be specific, three

inverters and two CR circuits are used. The first inverter is comprised of MOSFETs  $Q_1$  and  $Q_2$ , the second inverter is comprised of MOSFETs  $Q_4$  and  $Q_5$ , and the third inverter is comprised of MOSFETs  $Q_7$  and  $Q_8$ . In each of the MOSFETs  $Q_1$ ,  $Q_4$  and  $Q_7$ , the MOSFET is a depletion-type MOSFET, and the gate electrode and the source thereof are shorted. The MOSFETs  $Q_1$ ,  $Q_4$  and  $Q_7$  respectively function as load transistors with respect to the MOSFETs  $Q_2$ ,  $Q_5$  and  $Q_8$ . In order to prevent the MOSFETs  $Q_1$ ,  $Q_4$  and  $Q_7$  from being fully cut off, these MOSFETs are preferably depletion-type MOSFETs. If at least one of these MOSFETs is cut off, the oscillator OSC will stop oscillating. Each of the MOSFETs  $Q_2$ ,  $Q_5$  and  $Q_8$  is an enhancement-type MOSFET. If there were no RC circuits, the oscillator would produce an AC signal having a constant oscillating frequency which is defined by a delay time obtained when the AC signal passes through each inverter. However, the oscillator OSC of FIG. 3 produces an AC signal E having variable oscillating frequency, because at least one RC circuit is inserted between two adjacent inverters. Since the resistance value of the resistance (R) in the RC circuit is variable, the oscillator OSC acts as a variable oscillator. A first RC circuit is comprised of both a MOSFET  $Q_3$  and a capacitor  $C_1$ , and a second RC circuit is comprised of both a MOSFET  $Q_6$  and a capacitor  $C_2$ . These MOSFETs  $Q_3$  and  $Q_6$  are preferably depletion-type MOSFETs. It should be noted that, although one end of each inverter and also one end of each capacitor are connected to the ground GND of the MOS integrated circuit, mounted on the substrate, the gate electrodes of the MOSFETs ( $Q_3$ ,  $Q_6$ ), for forming the CR circuits, are connected directly to the substrate. Thus, the MOSFETs  $Q_3$  and  $Q_6$  can respond to the voltage level of the substrate. Since the MOSFETs  $Q_3$  and  $Q_6$  of FIG. 3 are made of N-channel MOSFETs, the MOSFETs  $Q_3$  and  $Q_6$  gain a high degree of conductivity, that is respective mutual conductances ( $g_m$ ) increase, when the voltage level of the substrate goes toward "H" level. At this time, the equivalent resistance values of these MOSFETs  $Q_3$  and  $Q_6$  reduce, and accordingly respective time constants  $\tau_1$ , defined by the resistor ( $Q_3$ ) and the capacitor ( $C_1$ ), and  $\tau_2$ , defined by the resistor ( $Q_6$ ) and the capacitor ( $C_2$ ), are made small, respectively. Then the oscillating frequency of the oscillator OSC is made high. Thus, the AC signal E having a high frequency is supplied, via the coupling capacitor  $C_c$ , to the charge pumping circuit PMC. As a result, the electric charges (holes), accumulated in the substrate, are quickly absorbed by the circuit PMC, and thereby the voltage level of the substrate goes toward "L" level.

Contrary to the above, when the voltage level of the substrate goes toward "L" level, the equivalent resistance values of these MOSFETs  $Q_3$  and  $Q_6$  increase and accordingly the respective time constants  $\tau_1$ , defined by the resistor ( $Q_3$ ) and the capacitor ( $C_1$ ), and  $\tau_2$ , defined by the resistor ( $Q_6$ ) and the capacitor ( $C_2$ ), are made large. Then the oscillating frequency of the oscillator OSC is made low. Thus, the AC signal E having a low frequency is supplied, via the coupling capacitor  $C_c$ , to the charge pumping circuit PMC. As a result, the electric charges (holes), accumulated in the substrate, are less rapidly absorbed by the circuit PMC, and thereby the voltage level of the substrate goes toward "H" level.

FIG. 4 depicts waveforms of signals appearing in the circuit shown in FIG. 3. The waveforms of rows (a),

(b), (c), (d) and (e) correspond respectively to waveforms of signals appearing at portions (a), (b), (c), (d) and (e) indicated in FIG. 3.

As previously mentioned, at least one RC circuit is incorporated into the oscillator OSC in FIG. 3. Accordingly, either the first RC circuit or the second RC circuit may be removed from the oscillator OSC. FIG. 5 depicts waveform of signals appearing in the circuit shown in FIG. 3, provided that the second RC circuit ( $Q_6$ ,  $C_2$ ) is not incorporated in the oscillator OSC. In FIG. 5, rows (a), (b), (c), (d) and (e) respectively depict the waveforms of signals appearing at the portions (a), (b), (c), (d) and (e) shown in FIG. 3.

Comparing the waveforms of FIG. 4 with the waveforms of FIG. 5, it may be concluded that the oscillator OSC, including two RC circuits therein, has a capability for more quickly following the variation of the voltage level of the substrate, than that of the oscillator which includes only one RC circuit therein. This is because, the integration of the signals depicted in row (e) of FIG. 4, is larger than that of the signals depicted in row (e) of FIG. 5, which integration is proportional to the electric charges (holes) to be absorbed from the substrate.

FIG. 6 illustrates an equivalent circuit diagram of a second embodiment for constructing the oscillator OSC, including the RC circuits therein, according to the present invention. The oscillator OSC, shown in FIG. 6, of the present invention is constructed as a multivibrator, comprised of MOSFETs  $Q_{11}$ ,  $Q_{12}$ ,  $Q_{13}$ ,  $Q_{14}$ ,  $Q_{15}$  and  $Q_{16}$ . RC circuits, identical to the aforesaid RC circuits, are formed respectively by the MOSFET  $Q_{13}$  and a capacitor  $C_{12}$ , and the MOSFET  $Q_{16}$  and a capacitor  $C_{11}$ . The drain of the MOSFET  $Q_{12}$  and the gate electrode of the MOSFET  $Q_{15}$  are interconnected with each other, via the capacitor  $C_{11}$ . Similarly, the drain of the MOSFET  $Q_{15}$  and the gate electrode of the MOSFET  $Q_{12}$  are interconnected with each other, via the capacitor  $C_{12}$ . The MOSFETs  $Q_{11}$  and  $Q_{12}$  form an inverter. The MOSFETs  $Q_{14}$  and  $Q_{15}$  form an inverter. The gate electrodes of the MOSFETs  $Q_{13}$  and  $Q_{16}$  are directly connected to the substrate (SUB), as the MOSFETs  $Q_3$  and  $Q_6$  of FIG. 3 are. The oscillating AC signal E is supplied to the charge pumping circuit PMC (see FIG. 1), via the coupling capacitor  $C_c$ . The oscillating frequency of the oscillator OSC varies under control of the MOSFETs  $Q_{13}$  and  $Q_{16}$ , in proportion to the voltage level of the substrate. FIG. 7 depicts waveforms of signals appearing in the circuit shown in FIG. 6. In FIG. 7, rows (a), (b), (c) and (d) depict waveforms of signals appearing at portions (a), (b), (c) and (d) shown in FIG. 6, respectively.

FIG. 8 illustrates an equivalent circuit diagram of a third embodiment for constructing the oscillator OSC, including the RC circuit therein, according to the present invention. The oscillator, shown in FIG. 8, of the present invention includes the RC circuit, comprised of a MOSFET  $Q_{26}$  and a capacitor  $C_{21}$ . The operation of the oscillator will be apparent from waveforms of signals depicted in FIG. 9. The waveforms depicted in rows (a), (b) and (c), respectively represent the waveforms of signals appearing at portions (a), (b) and (c), indicated in FIG. 8.

FIG. 10 is a cross sectional view of, for example, the MOSFET  $Q_3$ , the capacitor  $C_1$  and the MOSFET  $Q_5$  shown in FIG. 3. It should be understood that identical members, such as the MOSFET  $Q_6$ , the capacitor  $C_2$  and the MOSFET  $Q_8$  in FIG. 3, the MOSFET  $Q_{13}$

(Q<sub>16</sub>), the capacitor C<sub>12</sub> (C<sub>11</sub>) and the MOSFET Q<sub>15</sub> (Q<sub>12</sub>) in FIG. 6, will also provide the same sectional views as shown in FIG. 10. In this figure, the members represented by the same reference symbols as those of FIG. 1 are identical with each other. The capacitor C<sub>1</sub> is fabricated by an N<sup>+</sup>-type region, acting as the ground (GND) and also the source of the MOSFET Q<sub>5</sub>, an insulation layer IS' and an electrode EL, made of aluminum or polysilicon. The reference symbols CD represent conductive layers, acting as lead conductors, made of, for example aluminum. It should be recognized that the gate electrode G of the MOSFET Q<sub>3</sub>, acting as a part of the aforesaid CR circuit, is directly connected to the substrate SUB, via the conductor CD. Although, in FIG. 1, the oscillator OSC is separately located with respect to the substrate SUB, it is preferable, in the present invention, to mount the oscillator OSC directly on the substrate SUB, so that the gate electrodes of the MOSFETs, acting as the resistors (R) of the CR circuits, may easily be connected to the substrate SUB. The reference symbols PC represent protective covers, formed by insulation layers.

As explained in detail, the bias-voltage generator of the present invention can maintain the voltage level of the substrate at a predetermined optimum level, without introducing any special and complicated devices therein. Further, the bias-voltage generator of the present invention can automatically compensate for a deviation of the threshold voltage V<sub>th</sub>, which the deviation is necessarily produced during a manufacturing process. That is, if the threshold voltage V<sub>th</sub> of the produced MOSFET, such as the MOSFET Q<sub>3</sub>, Q<sub>6</sub> and so on, is lower than the predetermined threshold voltage V<sub>th</sub>, the oscillating frequency of the oscillator OSC becomes high. Then the voltage level of the substrate goes toward "L" level. As a result, the threshold voltage V<sub>th</sub> of the produced MOSFET, shifts toward high threshold voltage level. Contrary to this, if the threshold voltage V<sub>th</sub> of the produced MOSFET, is higher than the predetermined threshold voltage V<sub>th</sub>, the oscillating frequency of the oscillator OSC becomes low. Then the voltage level of the substrate goes toward "H" level. As a result, the threshold voltage V<sub>th</sub> of the produced MOSFET shifts toward low threshold voltage level.

What is claimed is:

1. A bias-voltage generator for applying a bias voltage to a semiconductor substrate having an integrated circuit thereon, said generator comprising:

an oscillator producing an oscillating AC signal, said oscillator comprising an RC circuit for varying the frequency of said oscillating AC signal in response to variations of the voltage level of said semiconductor substrate, said RC circuit including a capacitor (C) and a variable resistance (R) comprising a MOSFET having a gate electrode directly connected to the semiconductor substrate such that said variable resistance varies in accordance with the variations of the voltage level of the semiconductor substrate;

a coupling capacitor connected, at one end thereof, to the output of said oscillator; and

a charge pumping circuit for absorbing electric charges accumulated in said semiconductor substrate, connected firstly to the other end of said coupling capacitor, secondly to a ground of said integrated circuit, and thirdly to said semiconductor substrate,

wherein the oscillating frequency of said oscillating AC signal produced by said oscillator varies in proportion to the variation of the voltage level of said semiconductor substrate.

2. A generator as set forth in claim 1, wherein said RC circuit is mounted on the semiconductor substrate together with a desired MOS integrated circuit.

3. A generator as set forth in claim 1, wherein said oscillator comprises an odd number of inverters,

wherein at least one RC circuit is inserted between at least one pair of said inverters, and wherein said inverters and at least one said RC circuit are connected in series so as to form a ring oscillator.

4. A generator as set forth in claim 1, wherein said oscillator is formed as a multivibrator, comprised of:

a cross-connected pair of MOSFETs, a pair of load transistors, each load transistor being operatively connected to a corresponding one of said pair of MOSFETs, and

two of said RC circuits, wherein said cross-connected pair of MOSFETs are interconnected with each other, at respective drains and gate electrodes thereof, via said RC circuits.

5. A generator as set forth in claim 3, wherein each of said inverters comprises both a depletion-type load MOSFET and an enhancement-type MOSFET, and wherein said MOSFET variable resistance of at least one said RC circuit is a depletion-type MOSFET.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 4,390,798  
DATED : JUNE 28, 1983  
INVENTOR(S) : SETSUO KURAFUJI

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 1, line 39, "which" should be --with--.

Col. 3, line 31, after "including" insert --such--.

Col. 5, line 55, after "increase" insert --,--.

Col. 6, line 8, "waveform" should be --waveforms--.

**Signed and Sealed this**

*Eighth* **Day of** *November 1983*

**[SEAL]**

*Attest:*

**GERALD J. MOSSINGHOFF**

*Attesting Officer*

*Commissioner of Patents and Trademarks*





US005808505A

**United States Patent** [19]**Tsukada**[11] **Patent Number:** **5,808,505**[45] **Date of Patent:** **Sep. 15, 1998**[54] **SUBSTRATE BIASING CIRCUIT HAVING CONTROLLABLE RING OSCILLATOR**[75] **Inventor:** Shyuichi Tsukada, Tokyo, Japan[73] **Assignee:** NEC Corporation, Tokyo, Japan[21] **Appl. No.:** 924,735[22] **Filed:** Sep. 5, 1997**Related U.S. Application Data**

[63] Continuation of Ser. No. 605,588, Feb. 22, 1996, abandoned, which is a continuation of Ser. No. 508,972, Jul. 28, 1995, abandoned, which is a continuation of Ser. No. 248,674, May 25, 1994, abandoned.

[30] **Foreign Application Priority Data**

May 25, 1993 [JP] Japan ..... 122226/1993

[51] **Int. Cl.<sup>6</sup>** ..... G05F 1/10[52] **U.S. Cl.** ..... 327/536; 327/535; 327/537[58] **Field of Search** ..... 257/299; 307/109, 307/110; 327/156, 157, 535, 536, 537; 331/57[56] **References Cited****U.S. PATENT DOCUMENTS**

4,455,493	6/1984	Morton et al.	327/537
4,692,689	9/1987	Takemae	327/537
4,695,745	9/1987	Mimoto et al.	327/536
4,853,654	8/1989	Sakurai	331/57

5,041,739	8/1991	Goto	327/536
5,043,597	8/1991	Furuyama et al.	257/299
5,066,870	11/1991	Kobatake	327/536
5,180,995	1/1993	Hayashi et al.	331/57
5,302,919	4/1994	Abe	331/57
5,347,171	9/1994	Cordoba et al.	327/537

**FOREIGN PATENT DOCUMENTS**

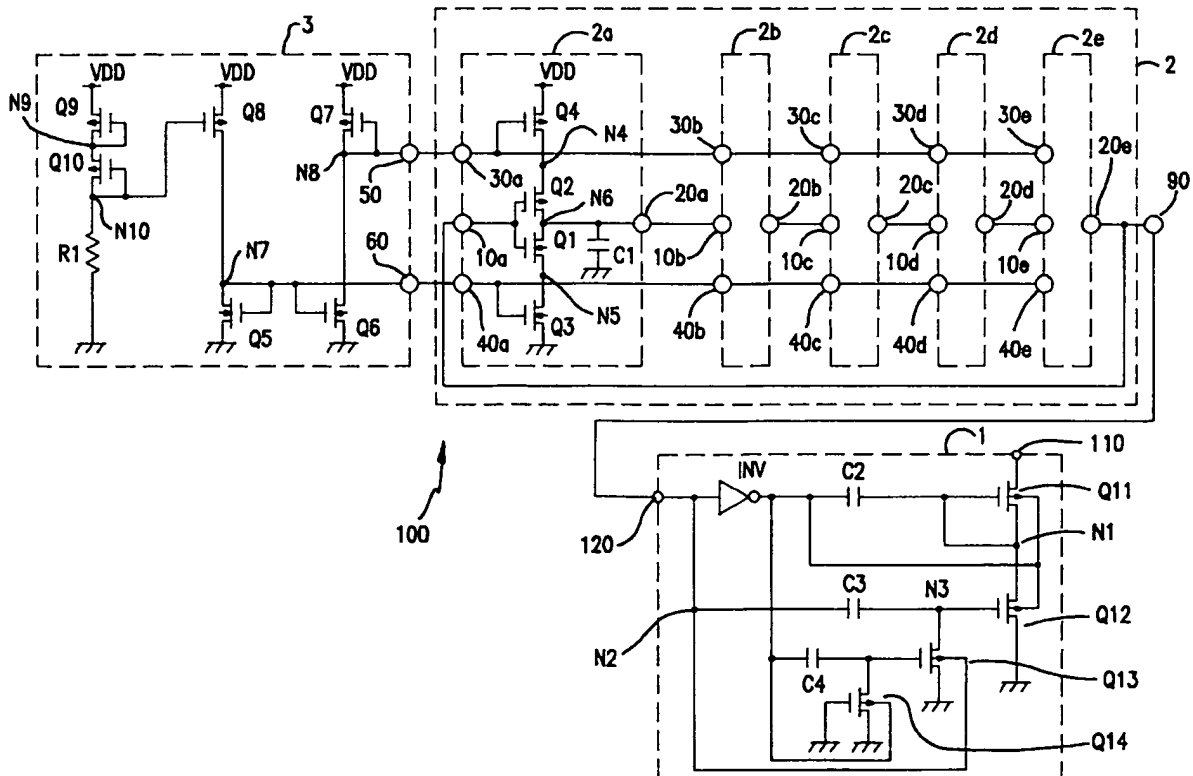
62-222713 9/1987 Japan .

**OTHER PUBLICATIONS**

"Design of CMOS Ultra LSI", issued on Apr. 25, 1989, pp. 193-195.

*Primary Examiner*—Toan Tran*Assistant Examiner*—Jeffrey Zweizig*Attorney, Agent, or Firm*—Young & Thompson[57] **ABSTRACT**

A substrate biasing circuit is disclosed which includes a ring oscillator oscillating to a drive pulse signal, a charge pump circuit connected to the ring oscillator to receive the drive pulse signal and generating a substrate-bias voltage in response thereto, and a current control circuit connected to the ring oscillator. The ring oscillator includes a plurality of delay circuits and the current control circuit controls each of the delay circuits such that a current flowing there through is stabilized against the variation in power voltage and relative to a threshold voltage of a transistor for the charge pump circuit.

**9 Claims, 4 Drawing Sheets**

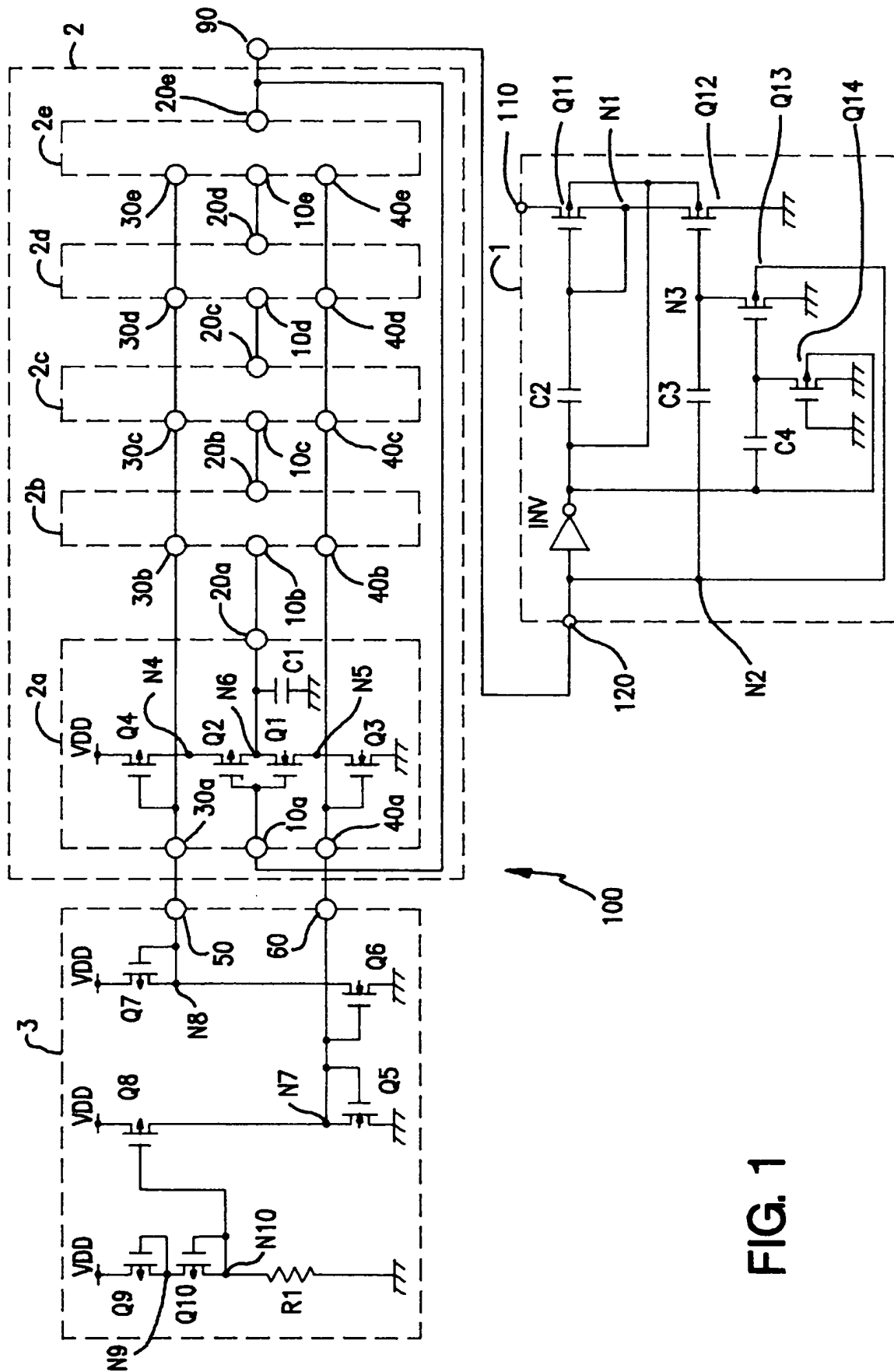


FIG. 1

FIG. 2A

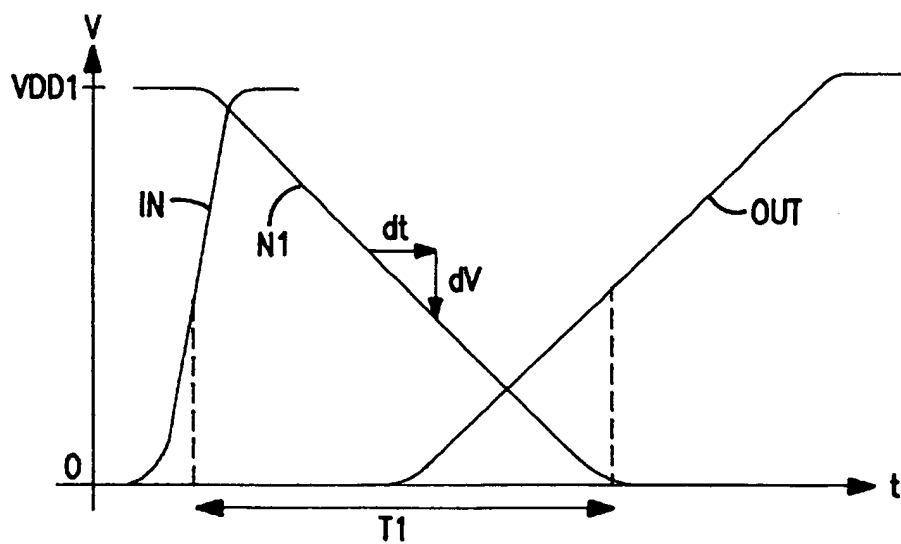


FIG. 2B

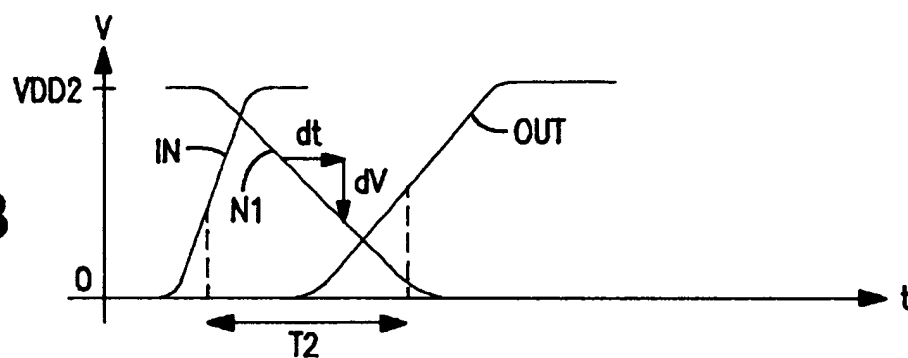
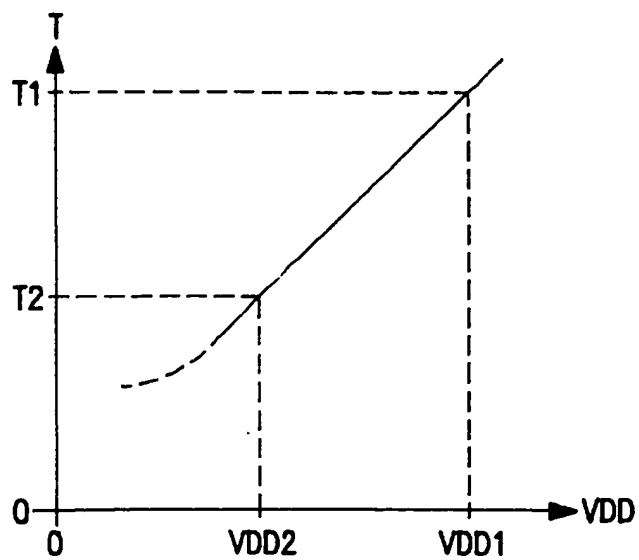


FIG. 2C



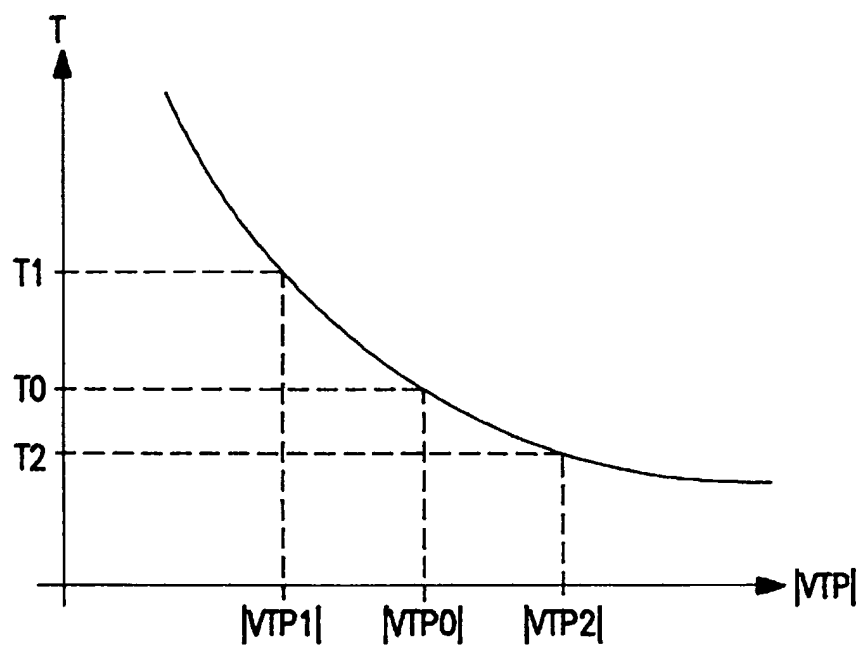


FIG. 3

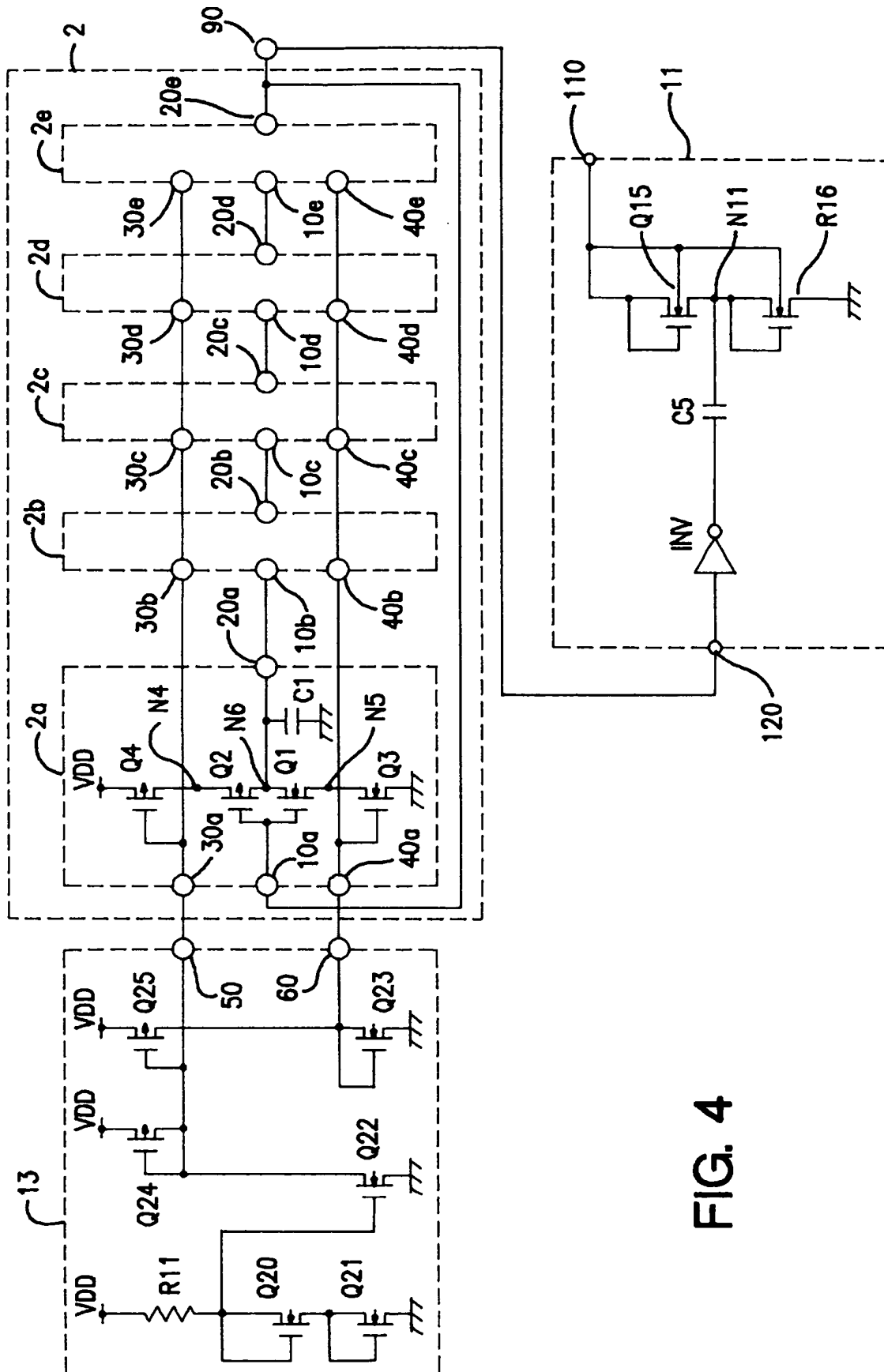


FIG. 4

## SUBSTRATE BIASING CIRCUIT HAVING CONTROLLABLE RING OSCILLATOR

This application is a continuation of application Ser. No. 08/605,588, filed Feb. 22, 1996, which is a continuation of Ser. No. 08/508,972, filed Jul. 28, 1995, which is a continuation of Ser. No. 08/248,674, filed May 25, 1994, all of which are now abandoned.

### BACKGROUND OF THE INVENTION

This invention relates to a substrate biasing circuit and, more particularly, to such a circuit that supplies a constant bias to a semiconductor substrate on which a semiconductor memory circuit is fabricated.

In a semiconductor memory device, a semiconductor substrate is generally supplied with a bias voltage in order to improve access speed and/or data hold characteristics. For example, in a semiconductor memory device having a p-type semiconductor substrate and operating on a positive power supply voltage, a negative bias voltage is applied to the substrate. A substrate biasing circuit is used to generate and supply the substrate-bias voltage and is composed of an oscillator circuit for generating an oscillation signal of a certain frequency and a charge-pump circuit generating the substrate-bias in response to the oscillation signal.

Because of no externally provided components being required, a ring oscillator is widely employed as the oscillator circuit. The ring oscillator includes an odd number of delayed-inverter circuits connected in the form of a ring. The oscillation frequency of the ring oscillator depends on the delay time of each delayed-inverter circuit. This delay time is shortened by an increase in power supply voltage or by the threshold voltage of transistors for the delayed-inverter circuits being lower than a design value. This is because the increased power supply voltage becomes or the lowered threshold voltage of the transistor causes the gate source bias voltage of the transistor becomes to be deepened and the current ability thereof to be made large. As a result, the oscillation frequency of the ring oscillator becomes high. Conversely, when the power supply voltage is reduced or the threshold voltage of the transistor becomes larger than the design value, the oscillation frequency becomes low.

On the other hand, the substrate-bias voltage generated by the charge-pump circuit depends on the frequency of the oscillation signal from the ring oscillator and is hence changed by the variation in the power supply voltage and/or the deviation in threshold voltage of the transistor from design value. The change in substrate-bias voltage brings about a change in effective threshold voltage in operation of each of the transistors constituting the memory circuit to make the data access operation unstable. At the worst, error in access or destruction of stored data, takes place.

Since the change in oscillation frequency of the delayed-inverter circuit contributes to change in delay time, it may be difficult to stabilize the delay time irrespective of variation in the power supply voltage. For this purpose, it is proposed in Japanese Patent Laid-Open Application No. Sho. 62-222713 to insert a constant current source in series with one of transistors constituting the delayed-inverter circuit. The current source thus inserted is used to make the current flowing through the circuit constant irrespective of the variation in power supply voltage. The delay time is thus made constant. It is further disclosed in a text book titled "Design of CMOS Ultra LSI" issued on Apr. 25 (1989), Baihoukan, that it is possible to control the oscillation frequency by attaching current sources to respective tran-

sistors of a CMOS inverter, the current of the current sources being provided with a desired characteristic.

It should be noted, however, that the substrate-bias voltage depends not only on the oscillation frequency of the ring oscillator but also on the current ability of transistors constituting the charge pump circuit. For example, even if the oscillation frequency of the ring oscillator is made constant by the means disclosed in the above-mentioned references against the increase in the power supply voltage, the current ability of the transistors for the charge pump circuit increases due to increase in power supply voltage, resulting in changing the substrate-bias. It is therefore needed, when power supply voltage rises, to lower the oscillation frequency of the ring oscillator to maintain the substrate-bias voltage constant. When the threshold value of the transistors in the charge pump circuit is made larger than the design value due to variation in the fabrication process thereof, the current ability of the transistors decreases correspondingly. Hence in this case, it is necessary to increase the oscillation frequency of the ring oscillator to compensate for the decrease in current ability.

As stated above, in order to keep the substrate-bias constant, the oscillation frequency of the ring oscillator must be controlled in response to circuit constructions and operations of both the ring oscillator and the charge pump circuit. A control circuit for that purpose is not taught, by the prior art mentioned above.

### SUMMARY OF THE INVENTION

It is therefore a principal object of the present invention to provide a substrate biasing circuit capable of generating and outputting a constant substrate-bias voltage against variations in power supply voltage and deviations of the threshold voltage of transistors from design value.

A substrate biasing circuit according to the present invention comprises a charge pump circuit receiving a drive pulse signal and generating a substrate-bias voltage in response thereto, a ring oscillator including a plurality of delayed-inverter circuits connected in a ring form to produce and supply the drive pulse signal to the charge pump circuit, and a current control circuit for controlling each of the delayed-inverter circuits such that a current flowing therethrough is stabilized against variation in a power supply voltage and is relative to a threshold voltage of a transistor contained in the charge pump circuit.

### BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a circuit diagram illustrative of a substrate biasing circuit according to a first embodiment of the present invention;

FIG. 2(a) is a graph for illustrating a delay time of a delayed-inverter circuit shown in FIG. 1 when the power supply voltage is high;

FIG. 2(b) is a graph for illustrating the delay time of the delayed-inverter circuit when the power supply voltage is low;

FIG. 2(c) is a graph indicating the relationship between the power supply voltage and the delay time of the delayed-inverter circuit;

FIG. 3 is a graph indicating the relationship between the threshold voltage of a transistor and the delay time of the delayed-inverter circuit; and

FIG. 4 is a circuit diagram illustrative of a substrate biasing circuit according to a second embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a substrate biasing circuit 100 according to the first embodiment of the present invention includes a charge pump circuit 1 having an output terminal 110 connected to a semiconductor substrate (not shown) on which this circuit is fabricated together with a memory circuit (not shown). The circuit 100 further includes a ring oscillator 2 supplying a drive pulse signal to the charge pump circuit 1. The ring oscillator 2 consists of delayed-inverter circuits 2a, 2b, 2c, 2d and 2e cascaded at an odd number of stages (five stages in this embodiment) in the ring form as shown. The current flowing in each of these circuits 2a-2e 2 is controlled by a current control circuit 3 which will be described in detail later.

The charge pump circuit 1 has an input terminal 120 receiving an oscillation signal from the ring oscillator 2 as the drive pulse, signal. The terminal 120 is connected to the input terminal of an inverter INV and one terminal of a capacitor C3. The output of the inverter INV is connected to the respective terminals of capacitors C2 and C4. The other terminal of a capacitor C2 is connected to the gate of a p-channel MOS transistor Q11 and to a node N1. The source-drain path of Q11 is connected between the voltage output terminal 110 and the node N1. The back gate of transistor Q11 is connected to the output of the inverter INV. The other terminal of the capacitor C3 is connected to the gate of a p-channel MOS transistor Q12 of which the drain-source path is connected between the node N1 and a ground and the back gate of which is connected to the output of the inverter INV. The other terminal of the capacitor C4 is connected to the gate of a p-channel MOS transistor Q13 of which the drain-source path is connected between node N3, which is the other terminal of the capacitor C3, and ground. The back gate of the transistor Q13 is connected to the drive pulse input terminal 120. There is further provided a p-channel MOS transistor Q14 with a gate grounded and a drain-source path connected between the other terminal of the capacitor C4 and the ground. The back gate of the p-channel transistor Q14 is connected to the output of the inverter INV.

The drive pulse signal supplied to the terminal 120 have an amplitude corresponding to the potential between a power supply voltage (VDD) line and a ground (GND) line. When the drive pulse at the drive-pulse input terminal 120 changes from VDD to GND, the level of the node N3 drops by VDD because of the coupling through the capacitor C3. When the node N2 accordingly drive pulse input terminal 120) is at VDD, the level of the node N3 is forced to be at GND level by the p-channel transistor Q13 and the capacitor C4. Owing to this, when the node N2 becomes GND, the level of the node N3 goes to -VDD level, and in turn the voltage applied to the gate of the p-channel transistor Q12 becomes -VDD. Thus the p-channel transistor Q12 is turned on, then the node N1 being dropped to GND.

When the level at drive pulse input terminal 120 changes from GND to VDD, and correspondingly the output of the inverter INV goes from VDD to GND then the node N1 drops by VDD to -VDD through the coupling of the capacitor C2. In turn, the p-channel transistor Q11 is turned on, and thereby the potential of the substrate-bias output terminal 110 falls until the potential between the substrate-

bias output terminal 110 and the node N1 reaches below the threshold voltage of the p-channel transistor Q11.

Subsequently the node N2 goes from VDD to GND, which causes the node N1 to go to GND, and consequently the p-channel transistor Q11 is turned off.

As described above, every time the incoming drive pulse of a specified frequency changes from VDD to GND and from GND to VDD, the voltage at the substrate-bias output terminal 110 is affected by the negative level until a certain voltage at which it becomes stabilized.

The ring oscillator 2 consists of the delay circuits 2a, 2b, 2c, 2d, and 2e connected in a ring form. Herein all the delay circuits have the same configuration, and hence the delay circuit 2a only will be set forth.

The delay circuit 2a consists of a p-channel transistor Q2 and a n-channel transistor Q1 connected in series between nodes N4 and N5 and via a node N6, their gates being connected to a common input terminal 10a; a capacitor C1 connected between the node N6 and GND, the output terminal 20a of which being connected to the node N6; a p-channel transistor Q4 connected between VDD and the node N4, the gate of which being connected to a control terminal 30a; and an n-channel transistor Q3 connected between GND and the node N5, the gate of which being connected to a control terminal 40a. In the ring oscillator 2, the output terminal 20a of the preceding-stage delay circuit is connected to the input terminal 10a of each delay circuit, and the output terminal 20a of the last-stage delay circuit 2e is connected to drive pulse input terminal 120 of the charge pump circuit 1 through output terminal 90 of the ring oscillator 2 and also to the input terminal of the first stage delay circuit.

The delay time of the delay circuit 2a depends on magnitude of charge for the charging capacitor C1, i.e. the amount of the electric current flowing. The current flowing through the inverter constructed of p-channel and n-channel transistors Q2, Q1 is determined by the control voltage applied to the gates of p-channel and n-channel transistors Q4, Q3. Therefore, the current flowing through the inverter can be controlled constantly, and thereby constant current can be fed without being affected by variation of power supply voltage, which enables the control of delay time. Refer to FIG. 2(a) which plots an input signal IN supplied to the input terminal 10, an output signal OUT from the output terminal 20, and delay time of the delay circuit when operating at power supply voltage VDD1. When the input signal IN supplied to the input terminal 10 changes from GND to VDD, the p-channel transistor Q2 goes from off-state to on-state, and the n-channel transistor Q1 goes from on-state to off-state. Thereby the potential of the node N6 changes gradually from VDD to GND. Now letting I be the current constant of n-channel and p-channel transistors Q3, Q4, and C be the total capacitance of the node N6 which is the sum of capacitor C1 and parasitic capacitance, the potential change rate is represented by

$$dV/dt = I \cdot (1/C) \quad (1)$$

Since current constant I and the total capacity C are independent of variation of power supply voltage VDD1, the rate of change of the potential of the node N6 is unvaried. It follows that the time taking for the potential of the node N6 to become VDD1 to GND is proportional directly to power supply voltage VDD1 or its amplitude. Hence the delay time T1 between the input signal IN and the output signal OUT are proportional directly to power supply volt-

age VDD1. Likewise when the input signal IN becomes GND to VDD1, the absolute value of  $dV/dt$  is definite and hence the delay time is proportional directly to power supply voltage VDD1.

Referring to FIG. 2(b) showing graph by the operation at an alternative power supply voltage VDD2 lower than VDD1, as understood from which, the rate of change of the potential  $dV/dt$  is equal to FIG. 2(a), and the delay time in FIG. 2(b) where the voltage amplitude of the note N6 is small is shorter than FIG. 2(a).

As shown in FIG. 2(c), therefore it is understood that the delay circuit 2a is proportional directly to power supply voltage VDD, and its delay time is increased.

The current source circuit 3 consists of a p-channel transistor Q8 connected between VDD and a node N7; an n-channel transistor Q5 connected between the node N7 and GND, and the gate of which being connected to the node N7; a n-channel transistor Q6 connected between a node N8 and GND, and the gate of which being connected to the node N7 and output terminal 60; and a p-channel transistor Q7 connected between the node N8 and VDD and the gate of which is connected to output terminal 50. The output terminal 50 is connected to the respective input terminals 30a-30c of the delay circuits 2a, 2b, 2c, 2d and 2e, and output terminal 60 is similarly connected to input terminals 40a-40e of the delay circuits.

Now n-channel transistors Q5 and Q6 constitutes a current Miller circuit, and hence the current flowing through the n-channel transistor Q6 is determined by the n-channel transistor Q5, and the current flowing through the n-channel transistor Q5 is determined by the current flowing through the p-channel transistor Q8. The current flowing through the p-channel transistor Q8 is determined by the voltage between the gate and source thereof. The p-channel transistor Q4 in the delay circuit 2a and the p-channel transistor Q7 constitutes another current miller circuit. The n-channel transistor Q3 in the delay circuit 2a and the n-channel transistor Q6 constitutes another current miller circuit. The current flowing through all the delay circuits 2a, 2b, 2c, 2d, and 2e is determined by the current through the p-channel transistor Q8. In this embodiment, the ratio of an output current to an input current of each of the current miller circuits is designed to be 1. Therefore, respective currents flowing through all the delay inverter 2a through 2e are the same.

The current source circuit 3 further comprises a p-channel transistor Q9 connected between VDD and a node N9, the gate of which being connected to the node N9; a p-channel transistor Q10 connected between nodes N9 and N10, the gate of which being connected to the node N10, and a resistor R1 connected between the node N10 and GND. The node N10 is connected to the gate of the transistor Q8.

Letting  $V_{tp}$  be the threshold value of each p-channel transistor, then the voltage of node N10 is  $VDD - 2|V_{tp}|$  [Wherein  $|V_{tp}|$  represents the absolute value of  $V_{tp}$ ] which is supplied to the gate of the p-channel transistor Q8. It follows that the voltage between the gate and source of the p-channel transistor Q8 is  $2 V_{tp}$ . By the way the current flowing the p-channel transistor Q8 is determined by the voltage between the gate and source, and it is only the voltage depending on the threshold voltage  $V_{tp}$  that is applied between the gate and source. The current flowing through the p-channel transistor Q8 depends only on  $V_{tp}$  and not on VDD.

Thus letting  $\beta$  and  $I_{Q8}$  be the conductance constant and current constant of the p-channel transistor Q8, then

$$\begin{aligned} I_{Q8} &= (1/2) \cdot \beta \cdot (2|V_{tp}| - |V_{tp}|^2) \\ &= (1/2) \cdot \beta \cdot (|V_{tp}|^2) \end{aligned} \quad (2)$$

Furthermore since the delay time of the delay circuit is inversely proportional to the current, the delay time T is expressed in relation to the threshold voltage  $V_{tp}$  by

$$T = 1/|V_{tp}|^2 \quad (3)$$

Therefore the relationship between the absolute value of the threshold voltage  $V_{tp}$  and the delay time based on the above equation (3) is indicated in FIG. 3. As is apparent from FIG. 3, the smaller the threshold value of the transistor, the longer the delay time is, as the relation of T1 to  $|V_{tp}|$  and the larger the threshold value of the transistor, the shorter the delay time is, as the relation of T2 to  $|V_{tp}|^2$ . Hence when p-channel transistors Q11 and Q12 degrades, i.e. when the p-channel transistors have a greater threshold due to variation in the device fabrication process, then the voltage on the node N10 is increased, which increases the currents flowing the p-channel transistors Q4 and the n-channel transistor Q3 of the delay circuit 2a, which in turn reduces the delay time, resulting in increasing the output frequency of the ring oscillator 2. Conversely when the p-channel transistors have a smaller threshold, then the currents flowing the p-channel transistors Q4 and the n-channel transistor Q3 of the delay circuit 2a is decreased, which reduces the delay time, resulting in decreasing the output frequency of the ring oscillator 2. The ability of charge pump circuit 1 depends on the frequency of the drive pulse the higher the frequency is, the higher the ability is, and the lower the frequency is, the lower ability is. In this way, even if the threshold value of the transistor changes, the frequency can be altered according to the change, and thereby the ability of the charge pump circuit 1 can follow the change to enable to output an unvaried bias.

Turning to FIG. 4, a substrate biasing circuit according to the second embodiment of the present invention includes a charge pump circuit 11, a ring oscillator 2 feeding drive pulses to the charge pump circuit 11, and a current control circuit 13. Ring oscillator 2 is the same as that of FIG. 1, and its explanation will be therefore omitted.

The charge pump circuit 11 comprises an n-channel transistor Q15 with a gate connected to the substrate-bias output terminal 110, and source/drain connected between the substrate-bias output terminal 110 and a node N11, and an n-channel transistor Q16 with a gate connected to the node N11 and source-drain path connected between the node N11 and GND, an inverter INV with the input connected to the drive-pulse input terminal and a capacitor C5 connected between the output of the inverter INV and the node N11.

This charge pump circuit 11, when the drive-pulse input terminal 120 is at GND, drives the node N11 N-1 from VDD which is raised in virtue of the coupling with capacitor C5 down to GND by the n-channel transistor Q16 of diode construction, and when drive pulse input the terminal 120 becomes raised from GND to VDD, drives the node N11 from GND down by VDD in virtue of the coupling with the capacitor C5, thereby the voltage of the substrate-bias output terminal 110 being lowered down to a negative level.

This charge pump circuit 11 employs n-channel transistors as Q15 and Q16 which is variable in ability due to deviation from the design values based on variation in fabrication process, etc. For suppressing this variation in ability of the charge pump circuit 11, it is needed to control the frequency of the drive pulse outputted from the ring



oscillator 2 by the use of threshold value  $V_{tn}$  in the same way as FIG. 1.

For this purpose, a current control circuit 13 of the present invention rises a resistor R11, four n-channel transistors Q20 through Q23, and two p-channel transistors Q24, Q25, and interconnected as shown. Especially the current flowing through transistor Q22 is correspondent to only the threshold voltage of the n-channel transistor. This current flows to each delay inverter through the current miller circuits each consisting of transistors Q24 and Q25; Q25 and Q24; and Q23 and Q23; respectively, and the values of these currents are all the same. Thus also in the present embodiment a constant substrate bias is obtained.

Similar effect is obtained also in the case of modification in FIG. 1 of replacing by transistors of the other conductivity type, using inversely VDD and GND, and connecting the charge pump circuit 11 instead of the charge pump circuit 1 to output terminal 90. Furthermore the number of transistor pairs such as Q9, Q10 or Q20 or Q21 of diode-connection may be increased.

As described above, a current source is placed between the terminals of each inverter-structure transistors constituting a delay circuit, and the current of the current source is controlled by the threshold value so that when the absolute value of the threshold voltage is lower, the current is correspondingly decreased to increase the delay time. In addition, since the charge and discharge at the output terminals of the inverter-structure transistors are carried out by the current of the current source. By these, the rate of change of the potential at the output terminal is constant independent of variation of power supply. Since the amplitude of the output voltage increases with increasing power supply voltage, the frequency of the drive pulse outputted from the ring oscillator can be decreased. Conversely when the absolute value of the threshold voltage is higher, the current is increased and thereby the delay time is decreased. Thus since the lower the power supply voltage is, the larger the amplitude of the output voltage becomes, it is possible to increase the frequency of the drive pulse outputted from the ring oscillator. Therefore when the ability of the charge pump circuit is increased, i.e. when the power supply voltage becomes higher, or when the absolute value of the threshold value is decreased, then the frequency of the drive pulse is decreased to suppress the ability of the charge pump circuit. When the ability of the charge pump circuit decreases, i.e. when power supply voltage is lower, or the absolute value of the threshold value increases, the frequency of the drive pulse is increased so that the ability of the charge pump circuit is improved by increasing the frequency of the drive pulse. In this way the substrate-bias outputted from the substrate-bias generator can be maintained constant.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is thereof contemplated that the appended claims will cover any modifications or embodiment as fall within the true scope of the invention.

What is claimed is:

1. A substrate biasing circuit comprising a charge pump circuit receiving a drive pulse signal and generating a substrate-bias voltage at an output terminal in response thereto, said charge pump circuit including an output transistor coupled to said output terminal to output said

substrate-bias voltage, a ring oscillator including a plurality of delayed-inverter circuits connected in a ring form to produce said drive pulse signal, said drive pulse signal having a frequency, and a current control circuit controlling each of said delayed-inverter circuits such that the frequency of said drive pulse signal is increased when a threshold voltage of said output transistor is larger than a predetermined value and is decreased when said threshold voltage of said output transistor is smaller than said predetermined value.

2. The circuit as claimed in claim 1, wherein each of said delayed-inverter circuits includes a first transistor of a first channel type connected between a first power supply line and a first node and having a gate connected to a first control terminal, a second transistor of said first channel type connected between said first node and a second node and having a gate connected to an input terminal, a third transistor of a second channel type connected between said second node and a third node and having a gate connected to said input terminal, and a fourth transistor of said second channel type connected between said third node and a second power supply line and having a gate connected to a second control terminal.

3. The circuit as claimed in claim 2, wherein said current control circuit includes a fifth transistor of said first channel type connected between said first power supply line and said first control terminal and having a gate connected to said first control terminal, a sixth transistor of said second channel type connected between said first control terminal and said second power supply line and having a gate connected to said second control terminal, a seventh transistor of said second channel type connected between said second control terminal and said second power supply line and having a gate connected to said second control terminal, an eighth transistor of said first channel type connected between said second control terminal and said first power supply line and having a gate connected to a third control terminal, and a bias circuit supplying a bias voltage to said third control terminal.

4. The circuit as claimed in claim 3, wherein said output transistor is of said first channel type and is connected between a fourth node and said output terminal, said output transistor operating, when said drive pulse signal is at a first level, to output said substrate-bias voltage at said output terminal, said charge pump circuit further including a restore transistor of said first channel type connected between said fourth node and said second power supply line and operating, when said drive pulse is at a second level, to connected said fourth node to said second power supply line.

5. The circuit as claimed in claim 4, wherein said bias circuit includes a ninth transistor of said first channel type connected between said first power supply line and a fifth node and having a gate to said fifth node, a tenth transistor of said first channel type connected between said fifth node and said third control terminal and having a gate connected to said third control terminal, and a resistive element connected between said third control terminal and said second power supply line.

6. A substrate biasing circuit according to claim 1, wherein:

said current control circuit includes a current controlling transistor, said current controlling transistor also having said threshold voltage, and said current controlling transistor controlling each of said delayed-inverter circuits such that the frequency of said drive pulse signal is increased when said threshold voltage is larger than a predetermined value and is decreased when said threshold voltage is smaller than said predetermined value.

## 7. A circuit comprising:

- a first transistor of a first channel type having a source connected to a first voltage supply line, a drain connected to a first node and a gate connected to said first node;
  - a second transistor of said first channel type having a source connected to said first node, a drain connected to a second node and a gate connected to said second node;
  - a resistive element connected between said second node and a second power supply line; and
  - a third transistor of said first channel type having a source connected to said first power supply line, a drain connected to an output node and a gate connected to said second node, such that a current at said output node is determined by a threshold voltage of at least one of said first, second and third transistors.
8. A circuit comprising:
- a delayed-inverter including,
    - a first transistor of a first channel type connected between a first power supply line and a first node and having a gate connected to a first control terminal;
    - a second transistor of said first channel type connected between said first node and an output node and having a gate connected to an input node;
    - a third transistor of a second channel type connected between said output node and a second node and having a gate connected to said input node, said first channel type being opposite to said second channel type, and
    - a fourth transistor of said second channel type connected between said second node and a second power supply line and having a gate connected to a second control terminal; and
  - a current control circuit including,
    - a fifth transistor of said first channel type connected between said first power supply line and a third node and having a gate connected to said third node;
    - a sixth transistor of said first channel type connected between said third node and a fourth node and having a gate connected to said fourth node;
    - a resistive element connected between said fourth node and said second power supply line;
    - a seventh transistor of said first channel type connected between said first power supply line and said second control terminal and having a gate connected to said fourth node;

- an eighth transistor of said second channel type connected between said second control terminal and said second power supply line and having a gate connected to said second control terminal;
  - a ninth transistor of said first channel type connected between said first power supply line and said first control terminal and having a gate connected to said first control terminal; and
  - a tenth transistor of said second channel type connected between said first control terminal and said second power supply line and a gate connected to said second control terminal.
9. A substrate biasing circuit comprising:
- a charge pump circuit receiving a drive pulse signal at an input terminal and generating a substrate bias voltage at an output terminal, said charge pump circuit comprising,
    - an inverter with an inverter input connected to said input terminal and to an input to a first capacitor, and with an inverter output connected to inputs to second and third capacitors,
    - a first transistor with one terminal connected to said output terminal, a second terminal and a gate connected to an output from said second capacitor, and a back gate connected to said inverter output,
    - a second transistor with one terminal connected to said second capacitor output, a second terminal connected to ground, a gate connected to an output from said first capacitor, and a back gate connected to said inverter output,
    - a third transistor with one terminal connected to said first capacitor output, a second terminal connected to ground, a gate connected to an output from said third capacitor, and a back gate connected to said inverter input, and
    - a fourth transistor with one terminal connected to said third capacitor output, a second terminal and a gate connected to ground, and a back gate connected to said inverter input;
  - a ring oscillator including a plurality of ring-connected delayed-inverter circuits providing said drive pulse signal with a frequency to said input terminal; and
  - a current control circuit controlling said delayed-inverter circuits so that the frequency of the drive pulse signal increases when a threshold voltage of said first transistor is larger than a predetermined value and decreases when the threshold voltage of said first transistor is smaller than the predetermined value.

\* \* \* \* \*



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**United States Patent** [19]

Utsunomiya et al.

[11] **Patent Number:** 6,122,185[45] **Date of Patent:** Sep. 19, 2000[54] **ELECTRONIC APPARATUS**

WO 89/07836 8/1989 WIPO .

[75] **Inventors:** Fumiyasu Utsunomiya; Yoshifumi Yoshida; Miwa Moriuchi, all of Chiba, Japan[73] **Assignee:** Seiko Instruments R&D Center Inc., Japan[21] **Appl. No.:** 09/121,061[22] **Filed:** Jul. 21, 1998[30] **Foreign Application Priority Data**

Jul. 22, 1997	[JP]	Japan	9-196109
Oct. 14, 1997	[JP]	Japan	9-280925

[51] **Int. Cl.<sup>7</sup>** ..... H02M 3/18[52] **U.S. Cl.** ..... 363/60[58] **Field of Search** ..... 363/59, 60; 327/530, 327/534, 536; 307/110[56] **References Cited****U.S. PATENT DOCUMENTS**

4,127,782	11/1978	Omura et al.	307/10.1
4,163,278	7/1979	Onoue et al.	363/101
4,634,953	1/1987	Shoji et al.	320/1
4,831,322	5/1989	Mashino et al.	322/28
4,971,451	11/1990	Suomalainen	323/222
5,179,508	1/1993	Lange et al.	363/16

**FOREIGN PATENT DOCUMENTS**

241219 10/1987 European Pat. Off. .

**OTHER PUBLICATIONS**

PATENT ABSTRACTS OF JAPAN, vol. 97, no. 10, Oct. 31, 1997.

PATENT ABSTRACTS OF JAPAN, vol. 96, no. 6, Jun. 28, 1996.

*Primary Examiner*—Adolf Deneke Berhane  
*Attorney, Agent, or Firm*—Adams & Wilks

[57] **ABSTRACT**

An electronic apparatus is comprised of a generator 11 in which a voltage is changed as time elapses, a booster circuit 12 for boosting an output voltage of the generator 11, and an oscillator circuit 13 that drives the booster circuit 12. When the voltage of the generator 11 changes as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, the oscillator circuit 13 obtains power for starting oscillation from the generator 11. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator 11. Since the oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12, even if the voltage of the generator 11 changes as time elapses so that the voltage becomes lower than the minimum driving voltage of the oscillator circuit 13, the voltage can be boosted to the minimum driving voltage of the oscillator circuit 13 or higher.

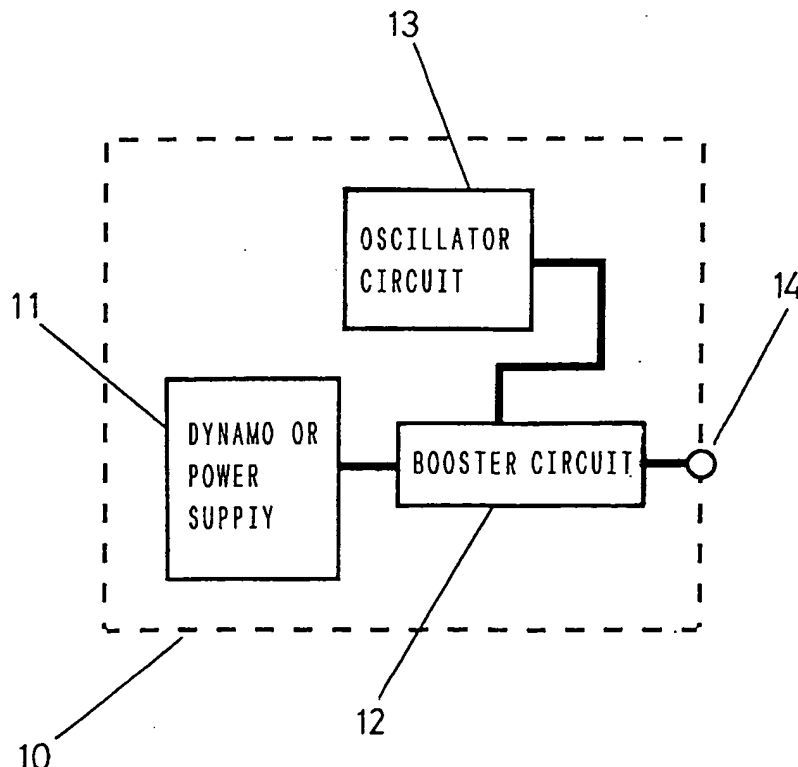
**28 Claims, 27 Drawing Sheets**

FIG. 1

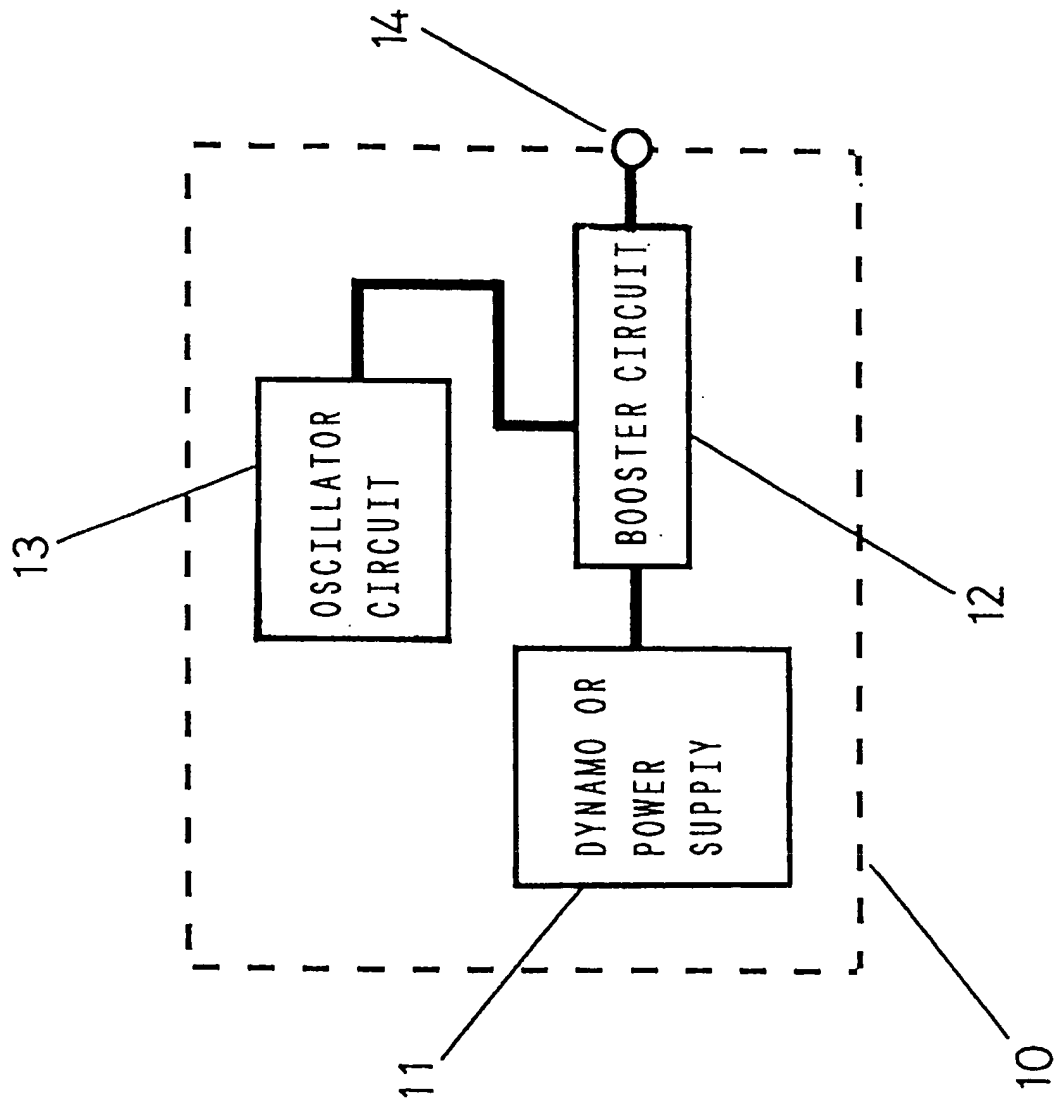
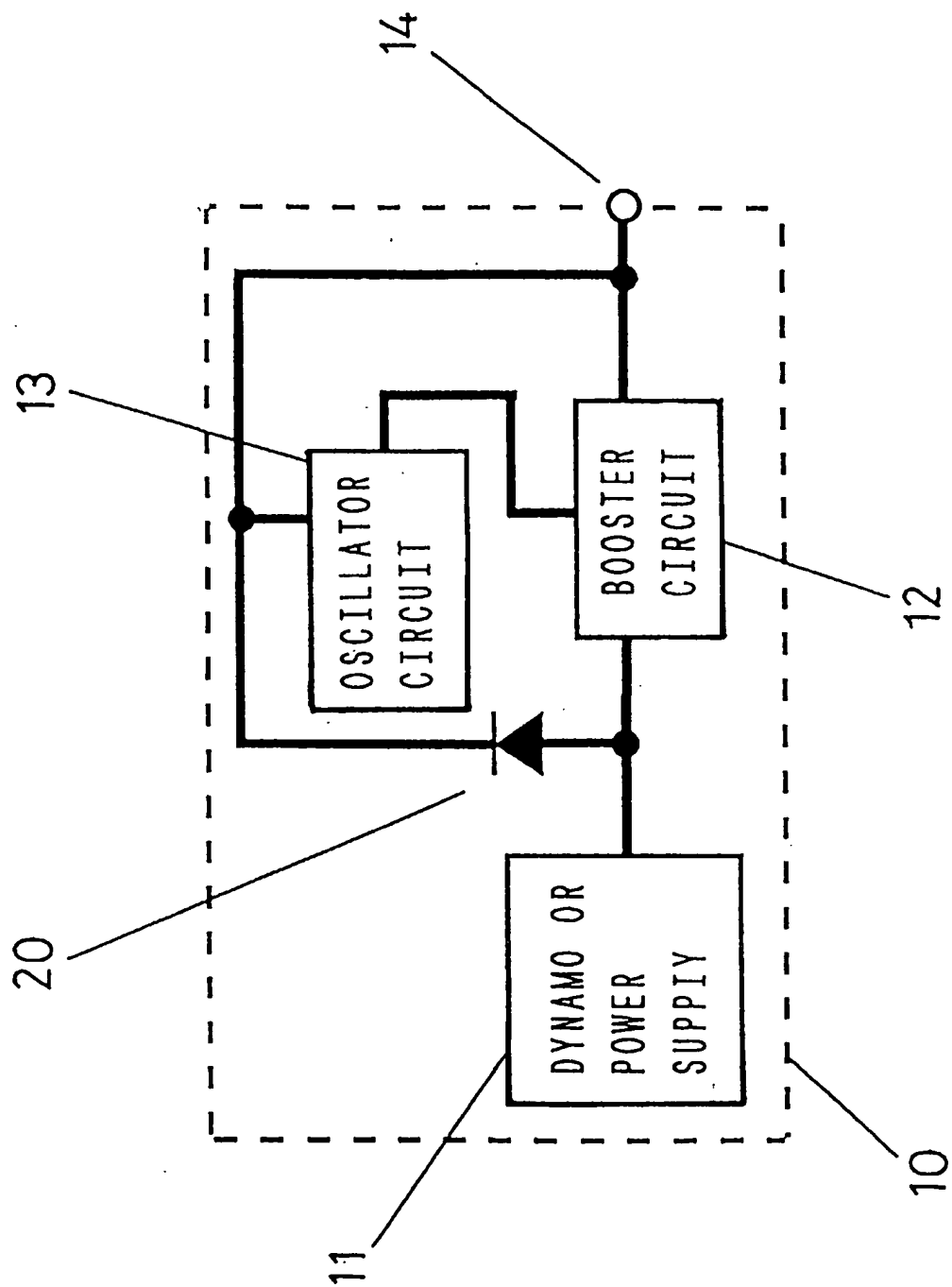
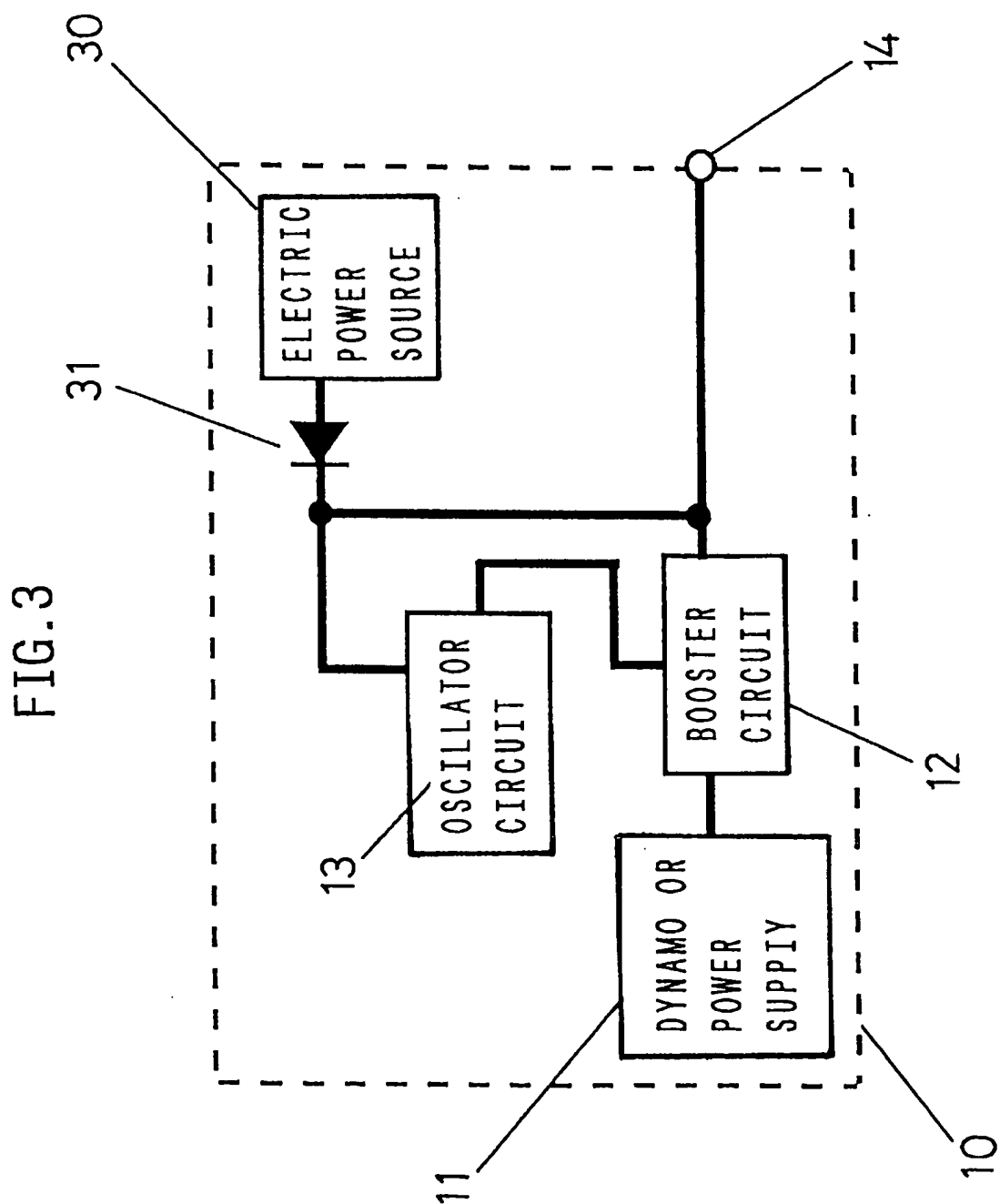


FIG. 2





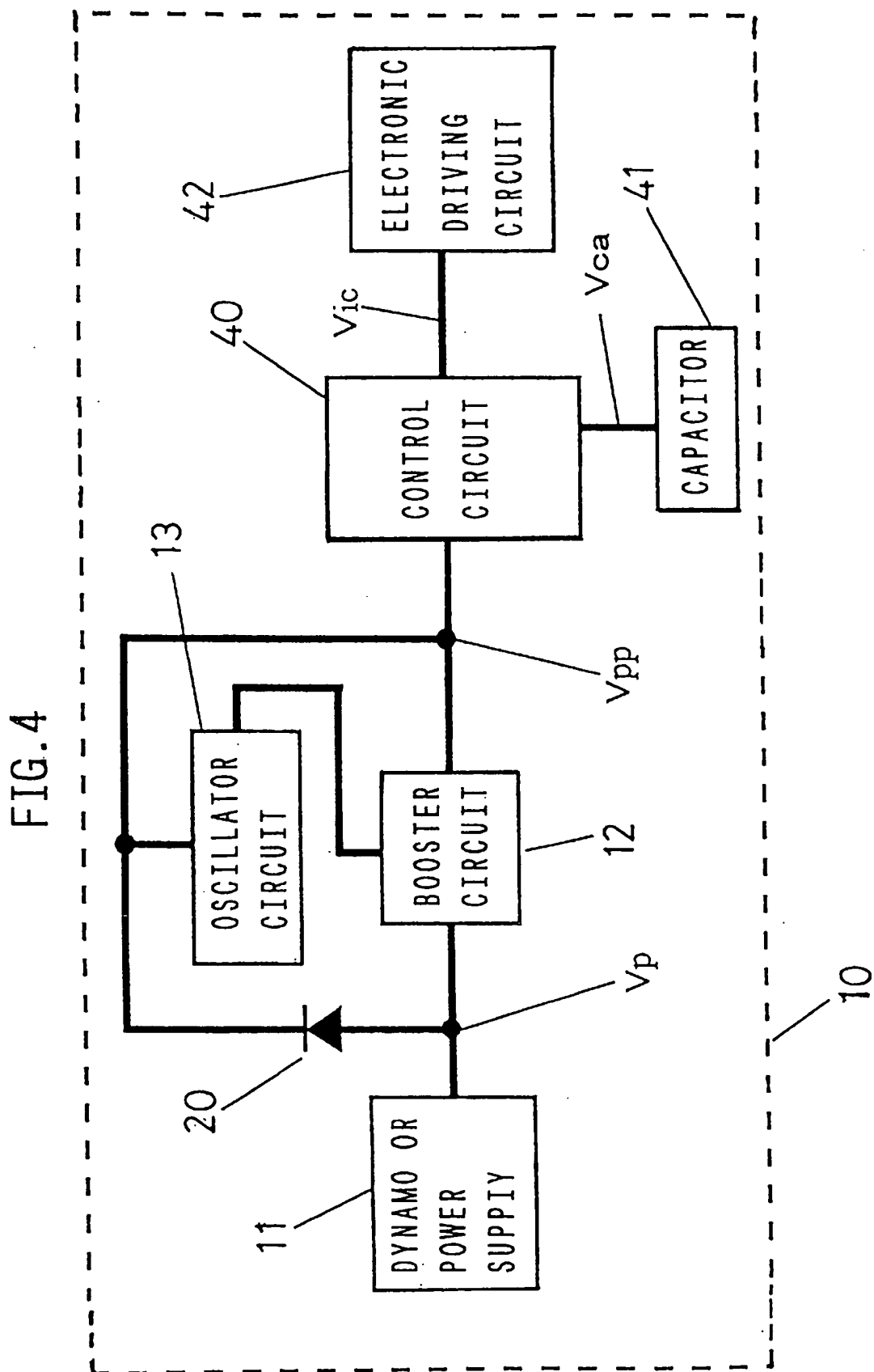


FIG. 5 A

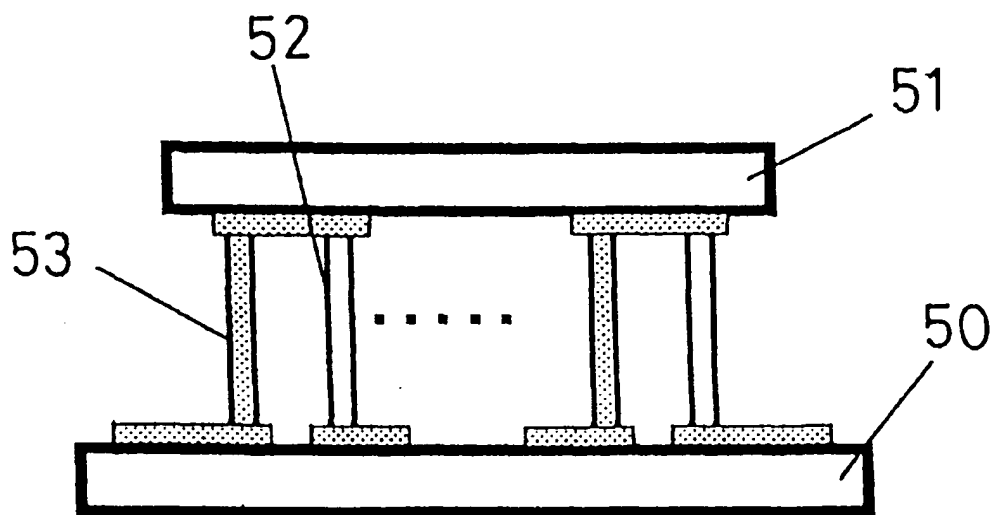
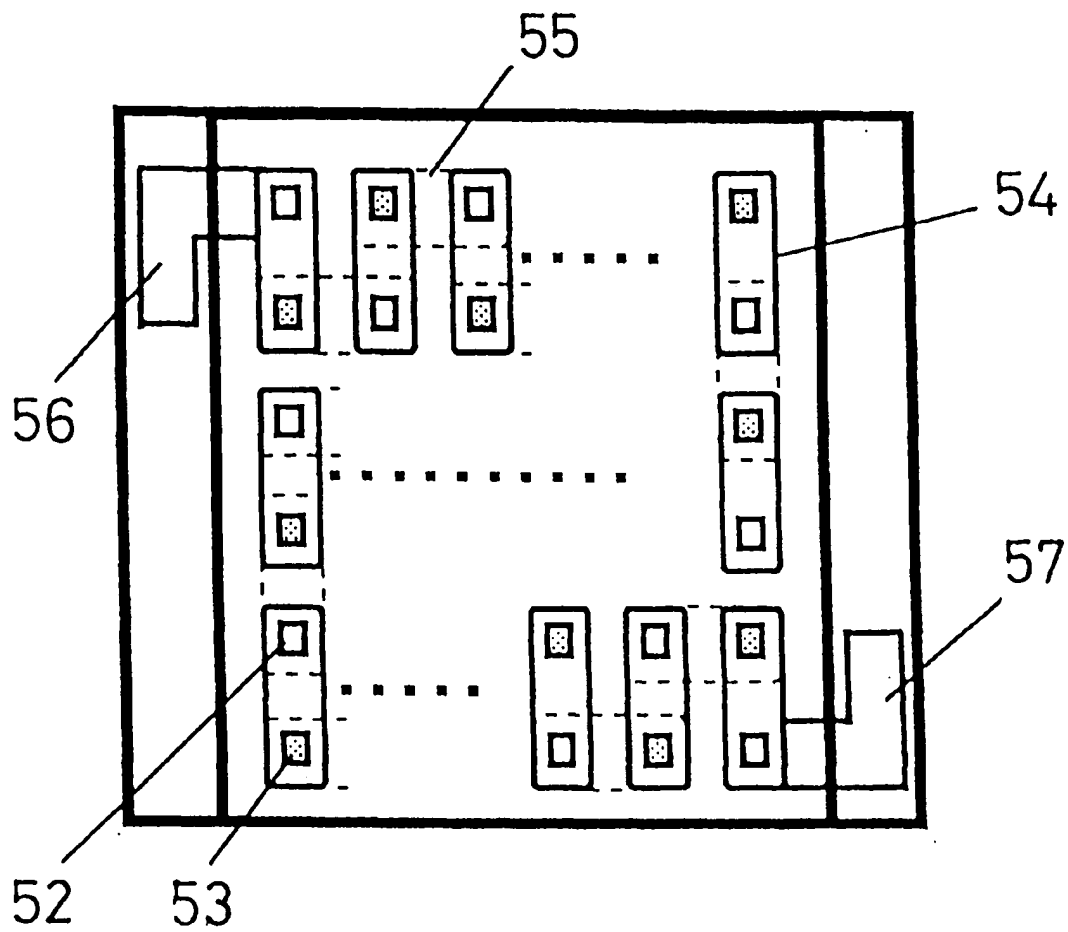


FIG. 5 B



FIG. 6

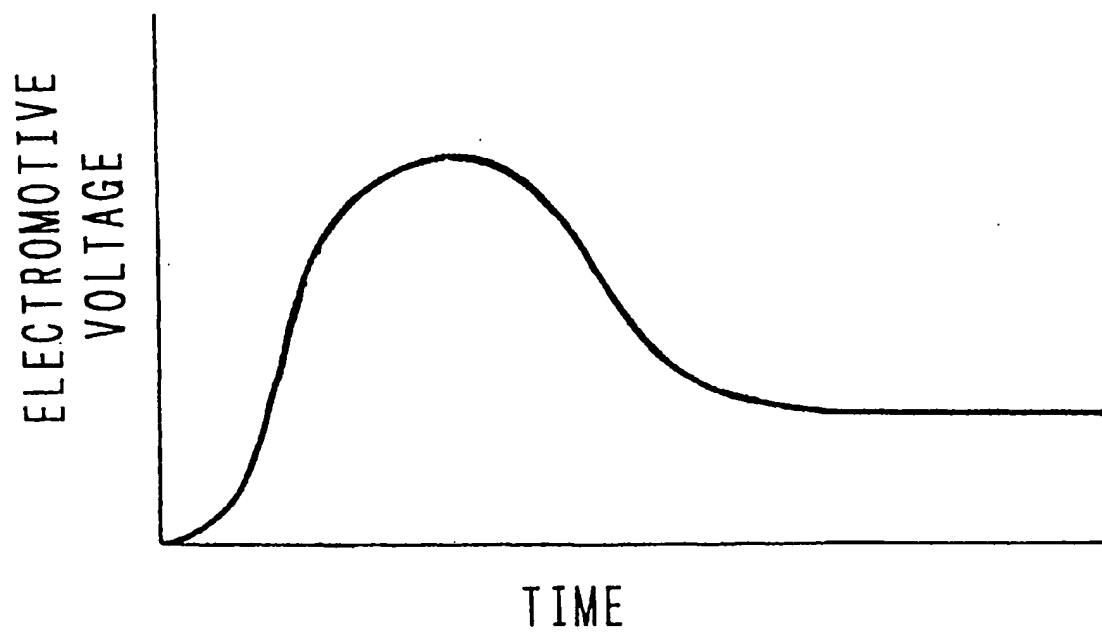


FIG. 7

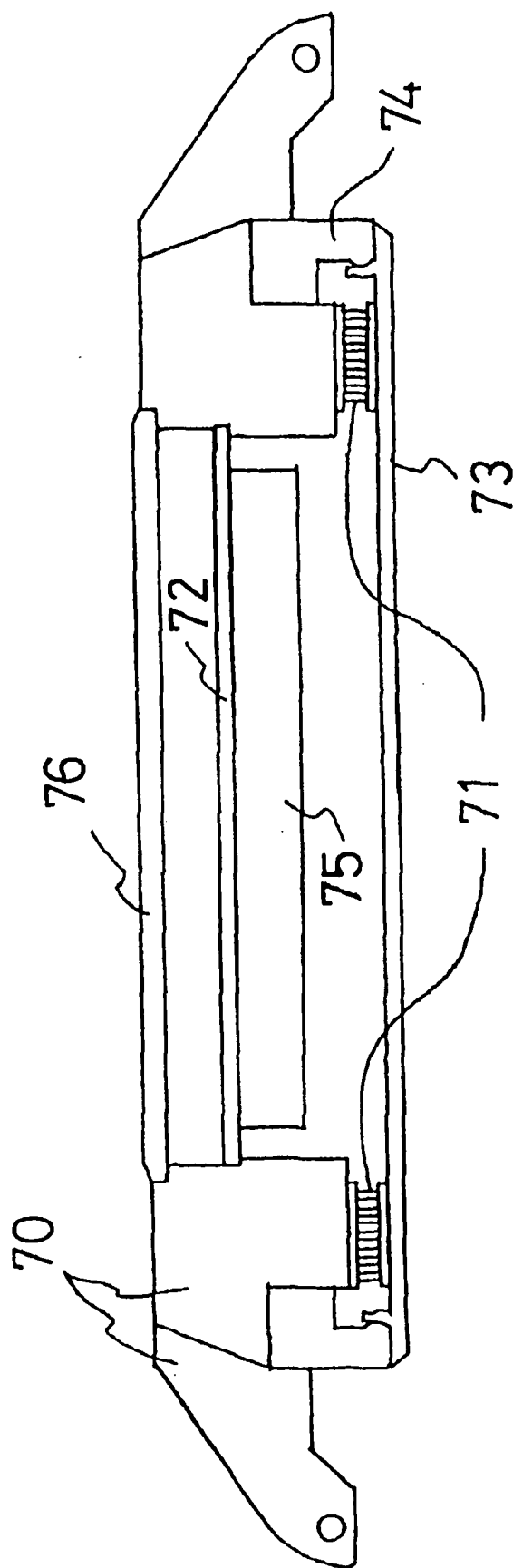


FIG. 8

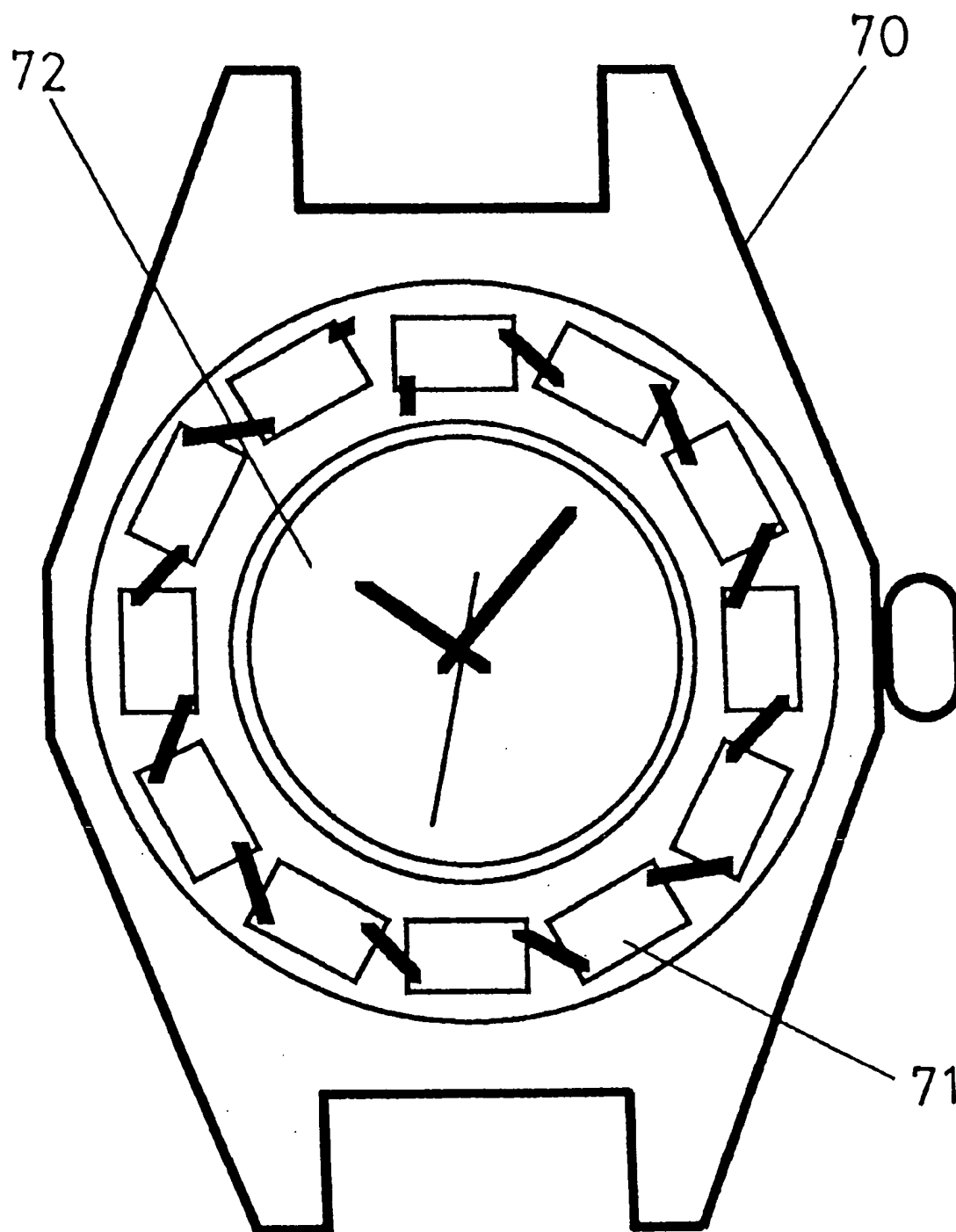


FIG. 9  
PRIOR ART

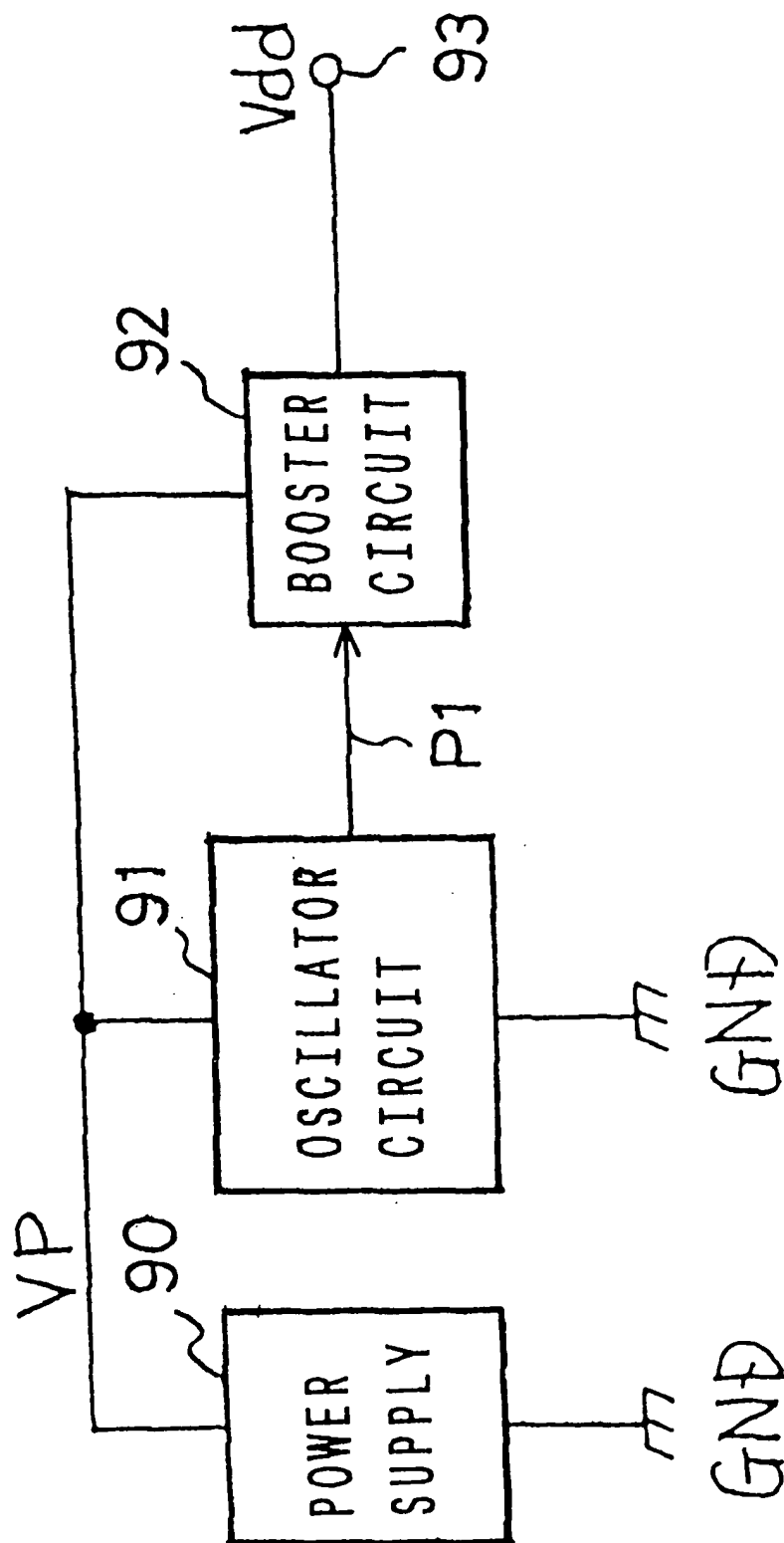


FIG. 10

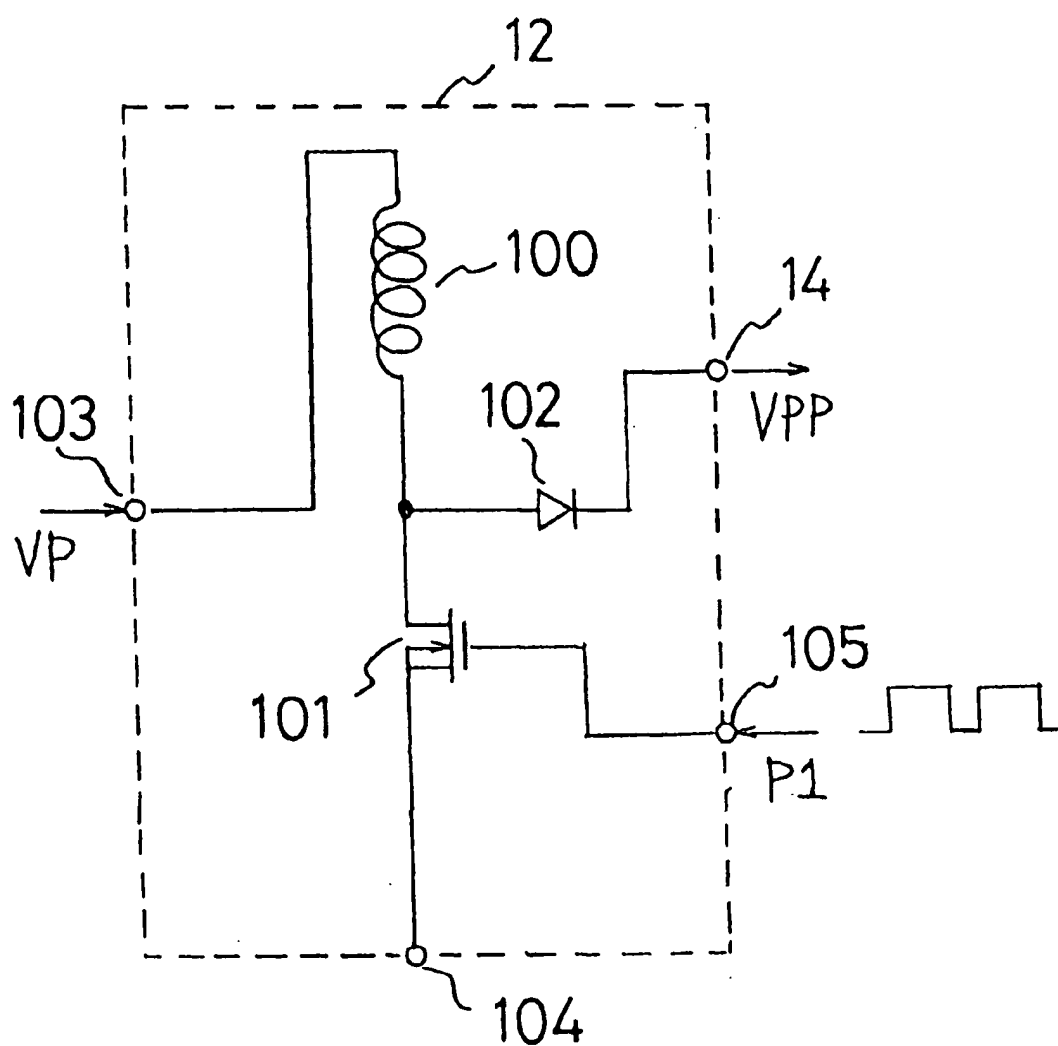


FIG. 11

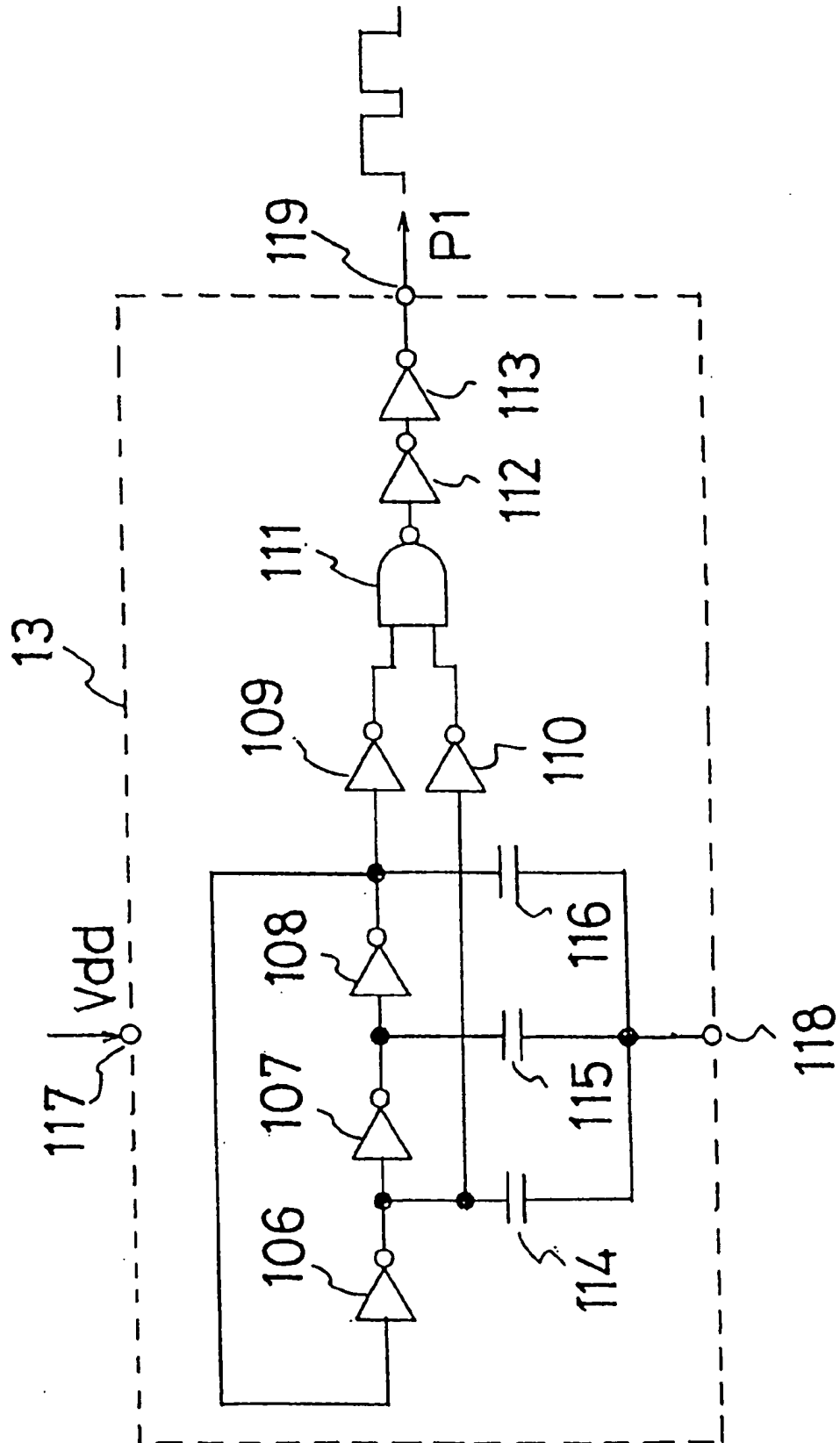


FIG. 12

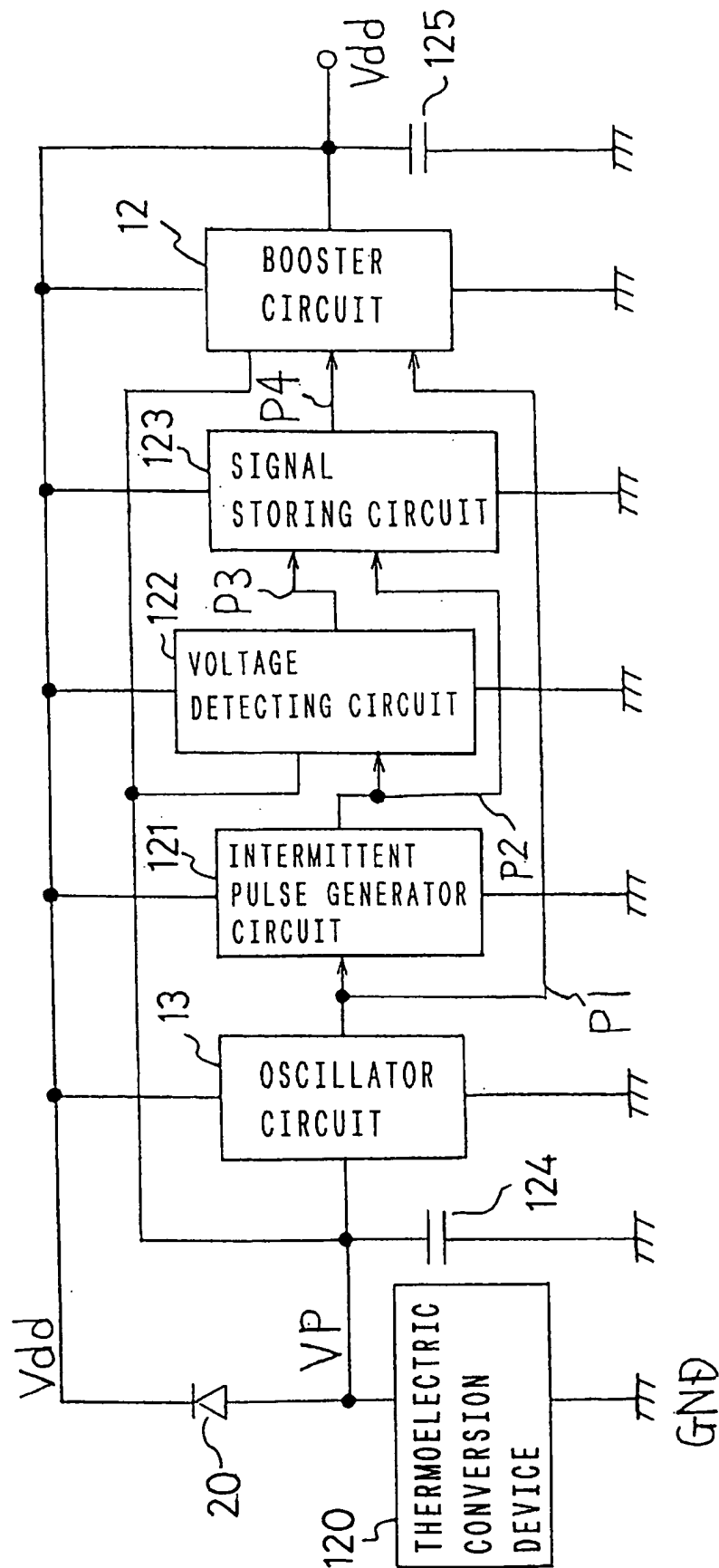


FIG. 13

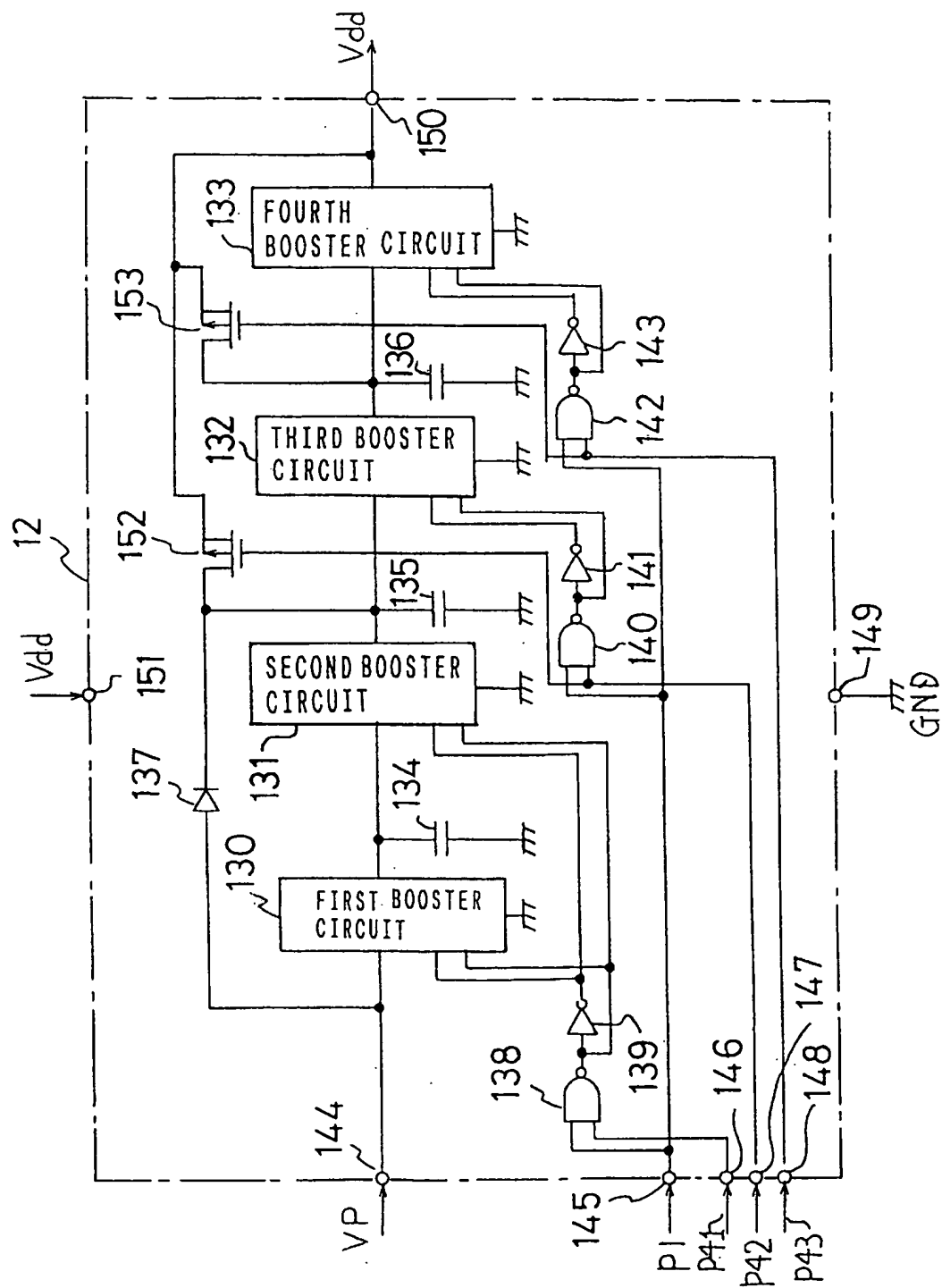




FIG. 14

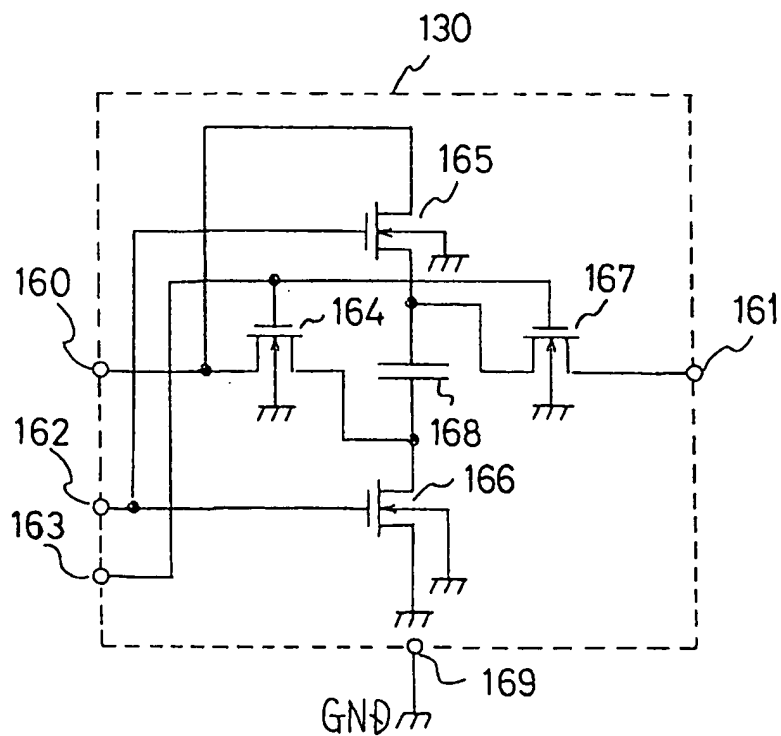


FIG. 15

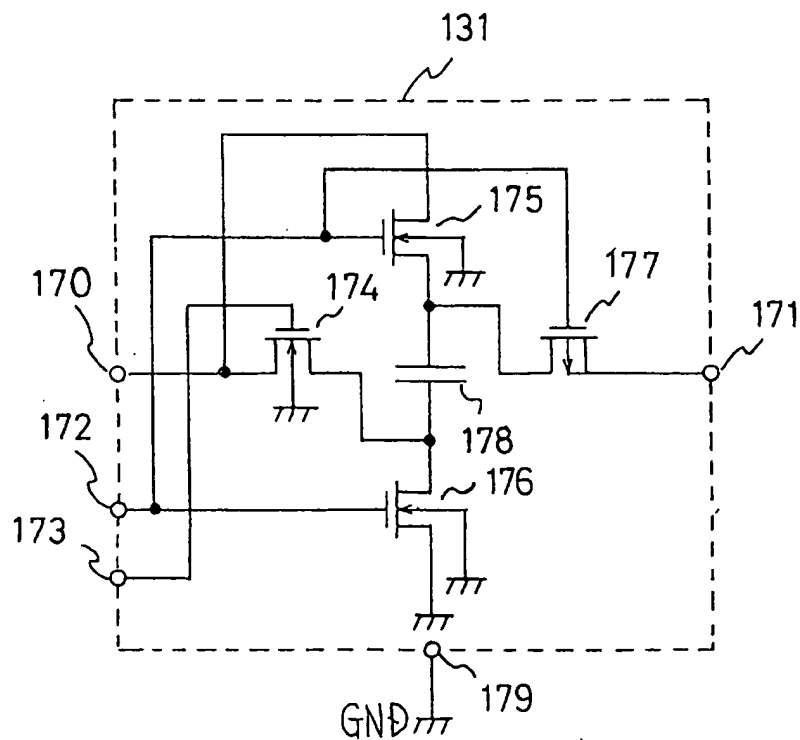


FIG. 16

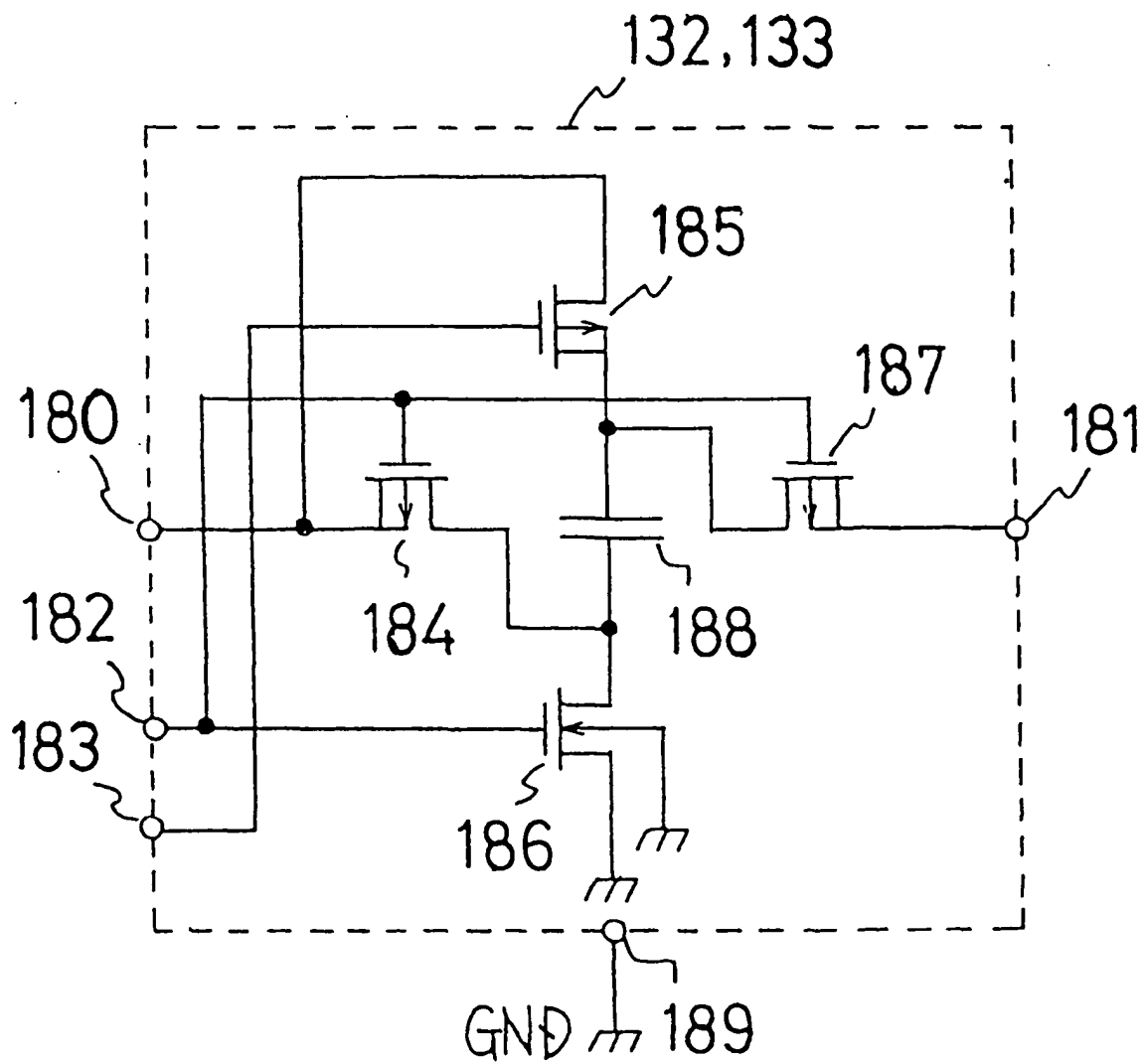


FIG. 17

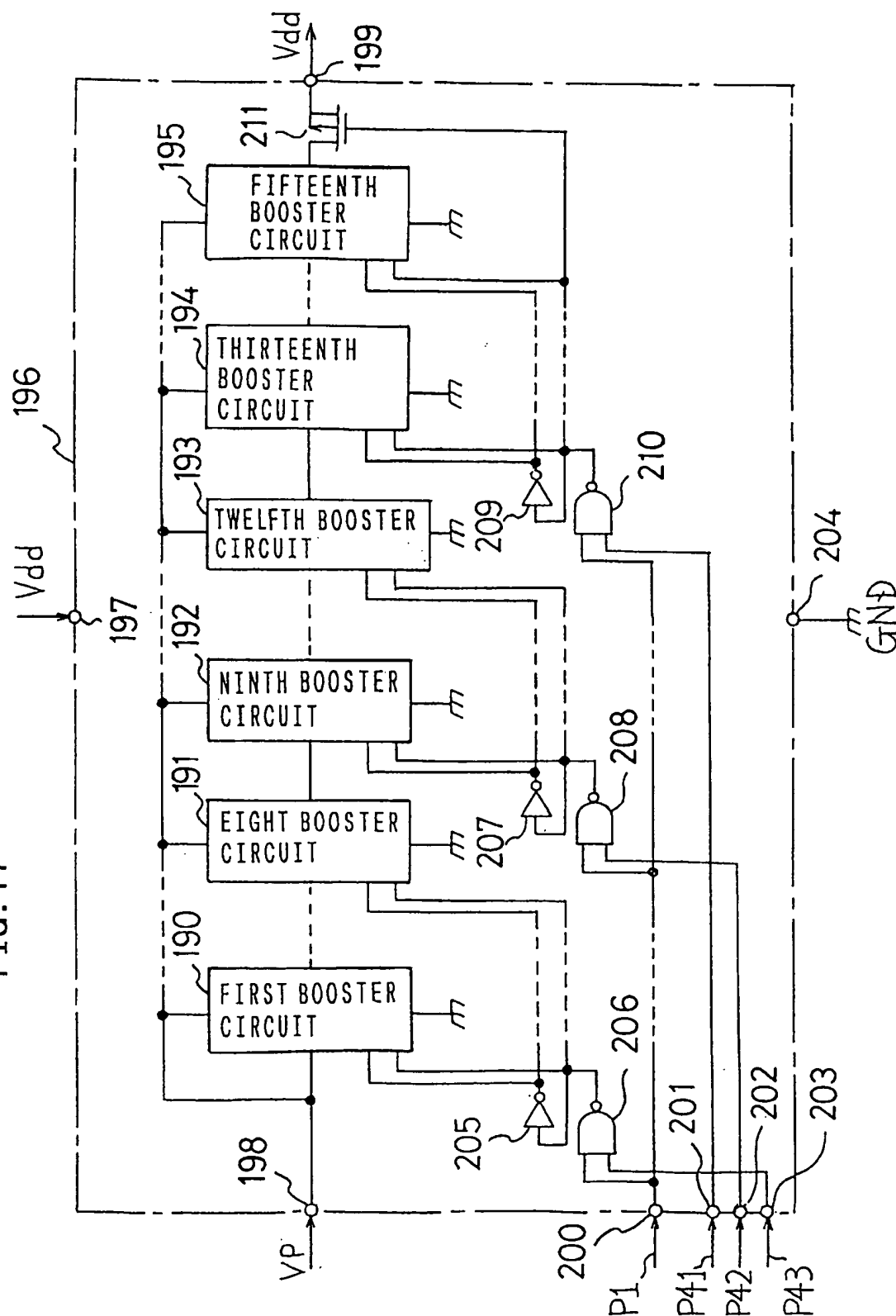


FIG. 18

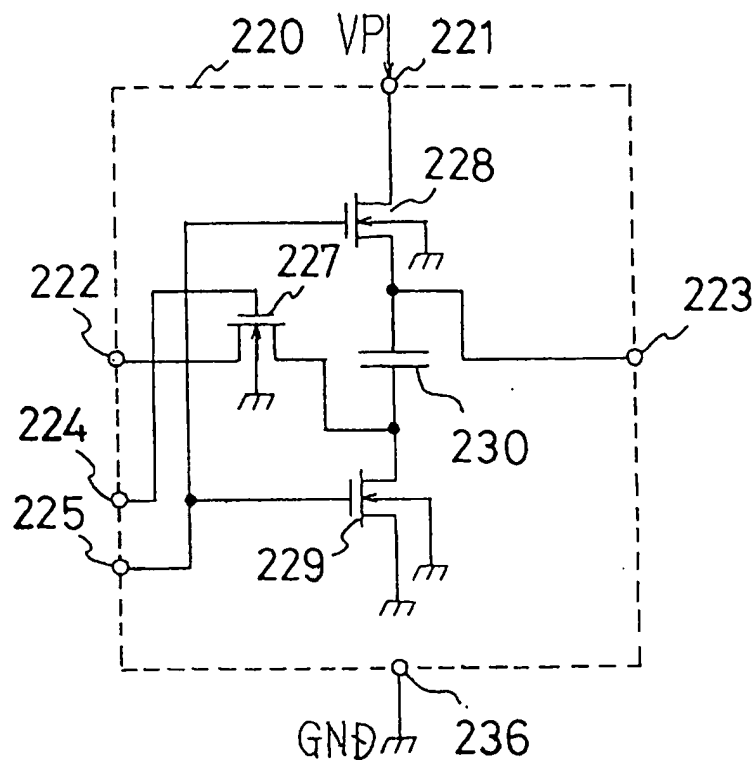


FIG. 19

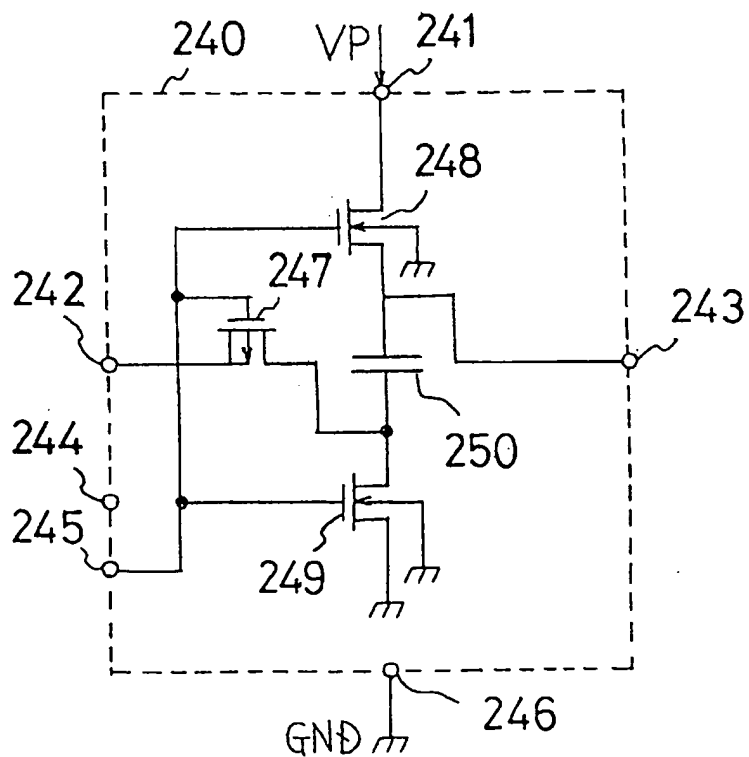


FIG. 20

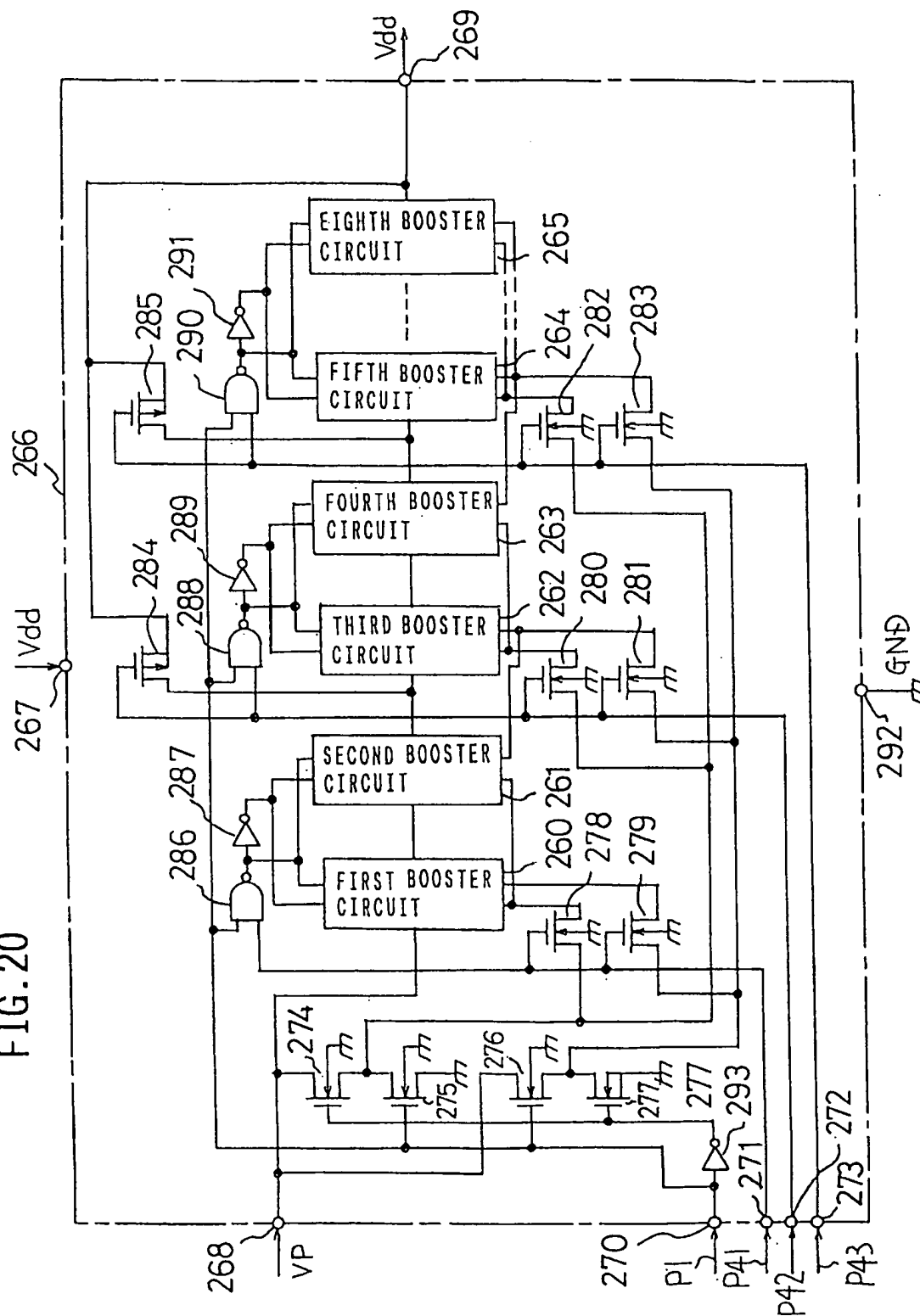


FIG. 21

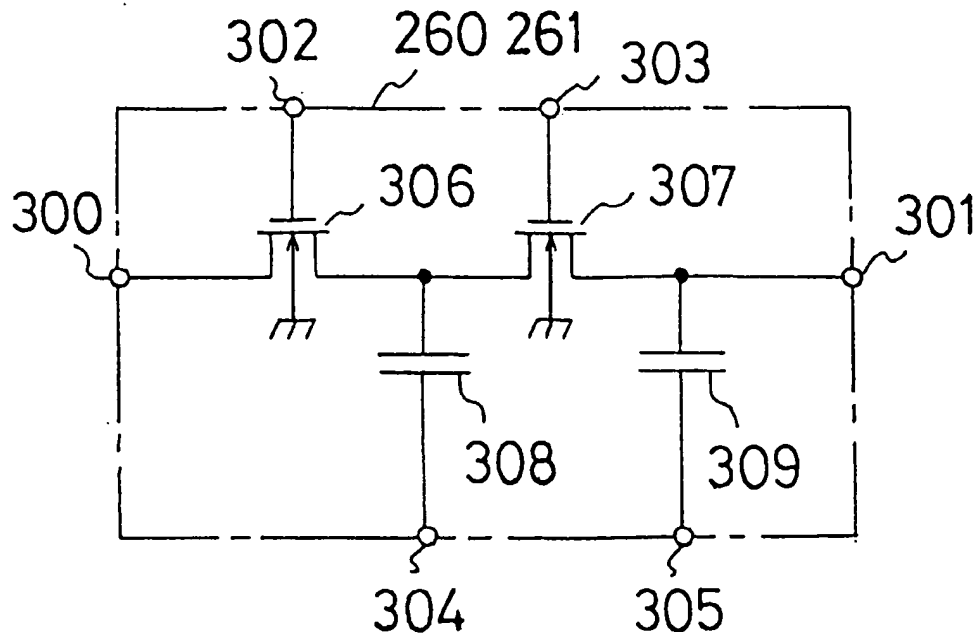


FIG. 22

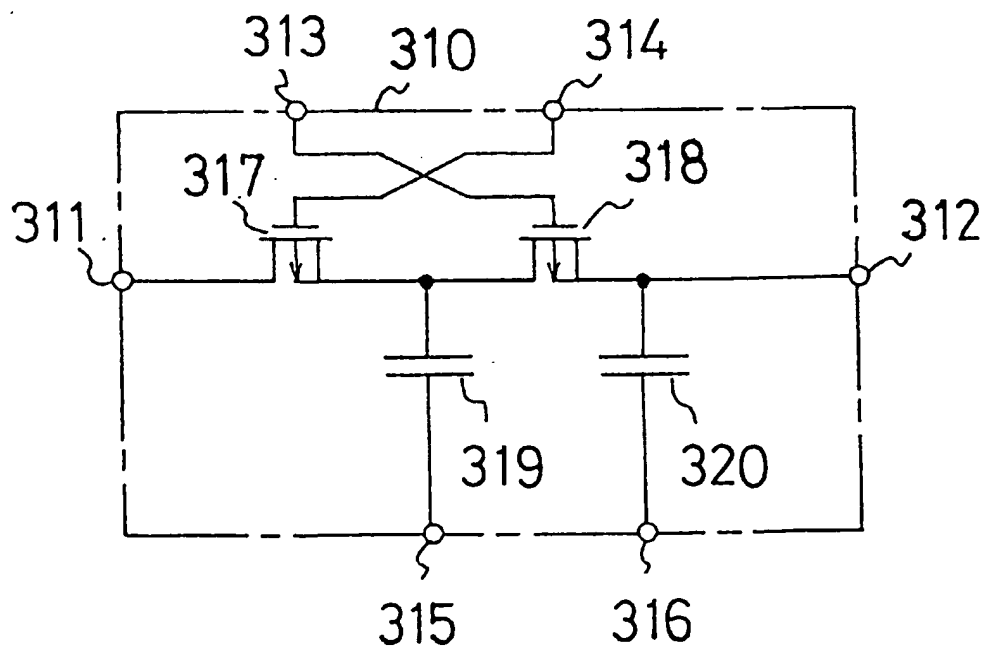


FIG. 23

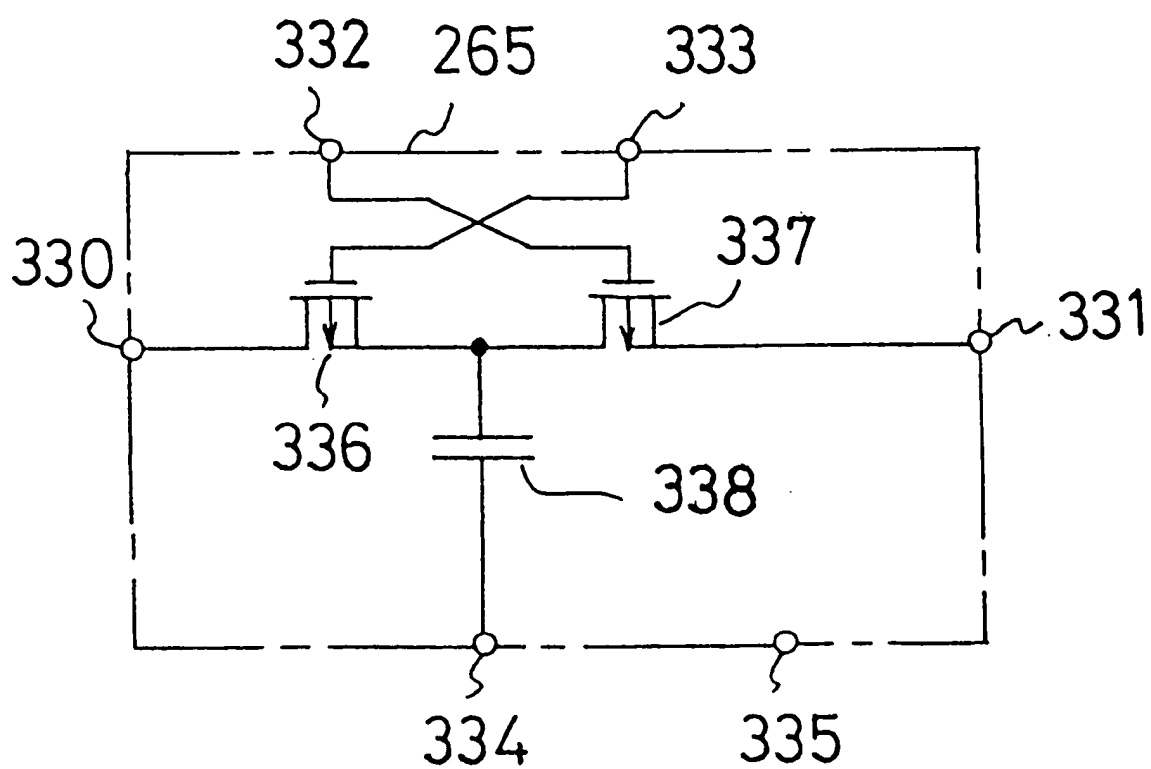


FIG. 24

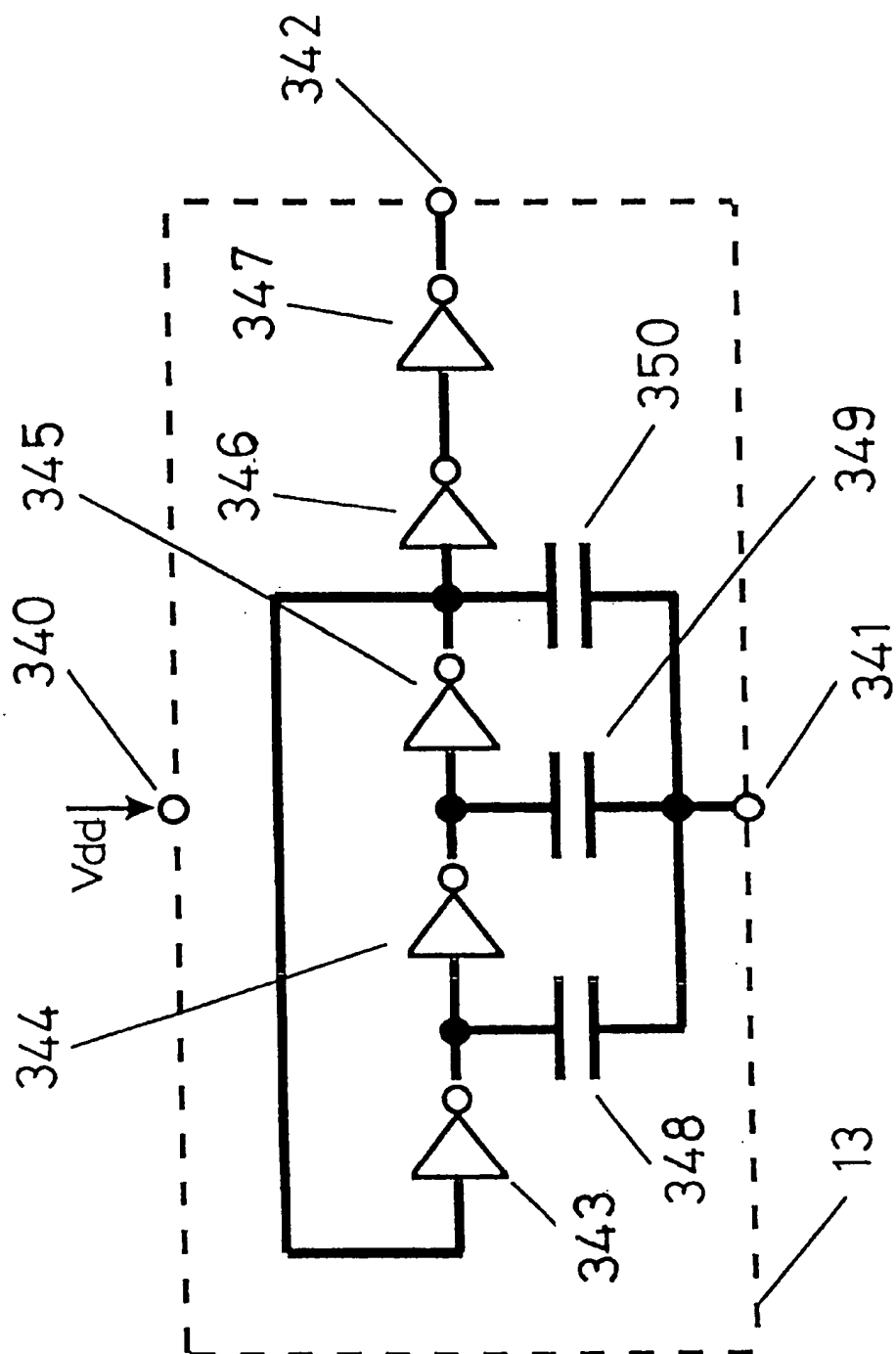




FIG. 25

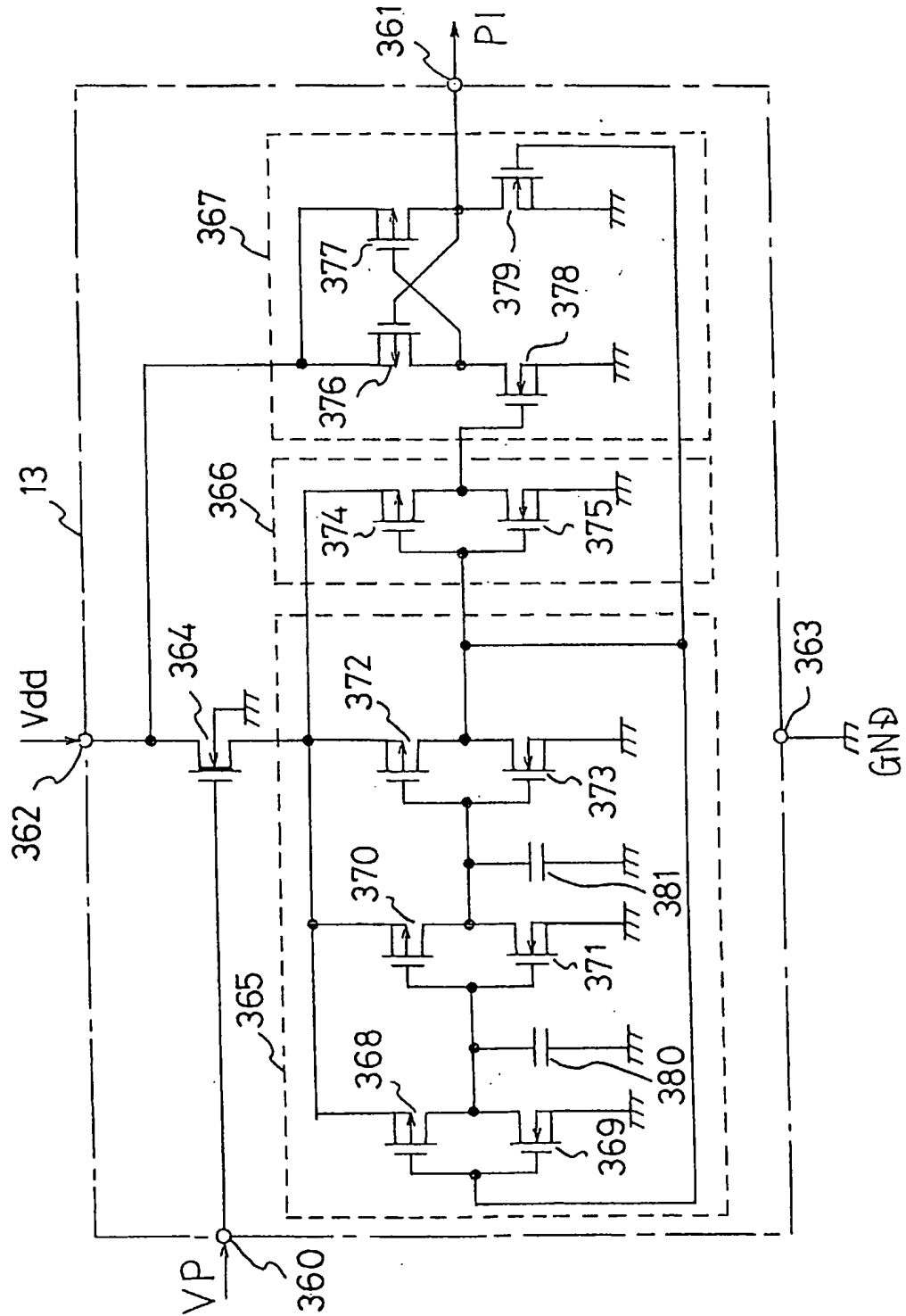


FIG. 26

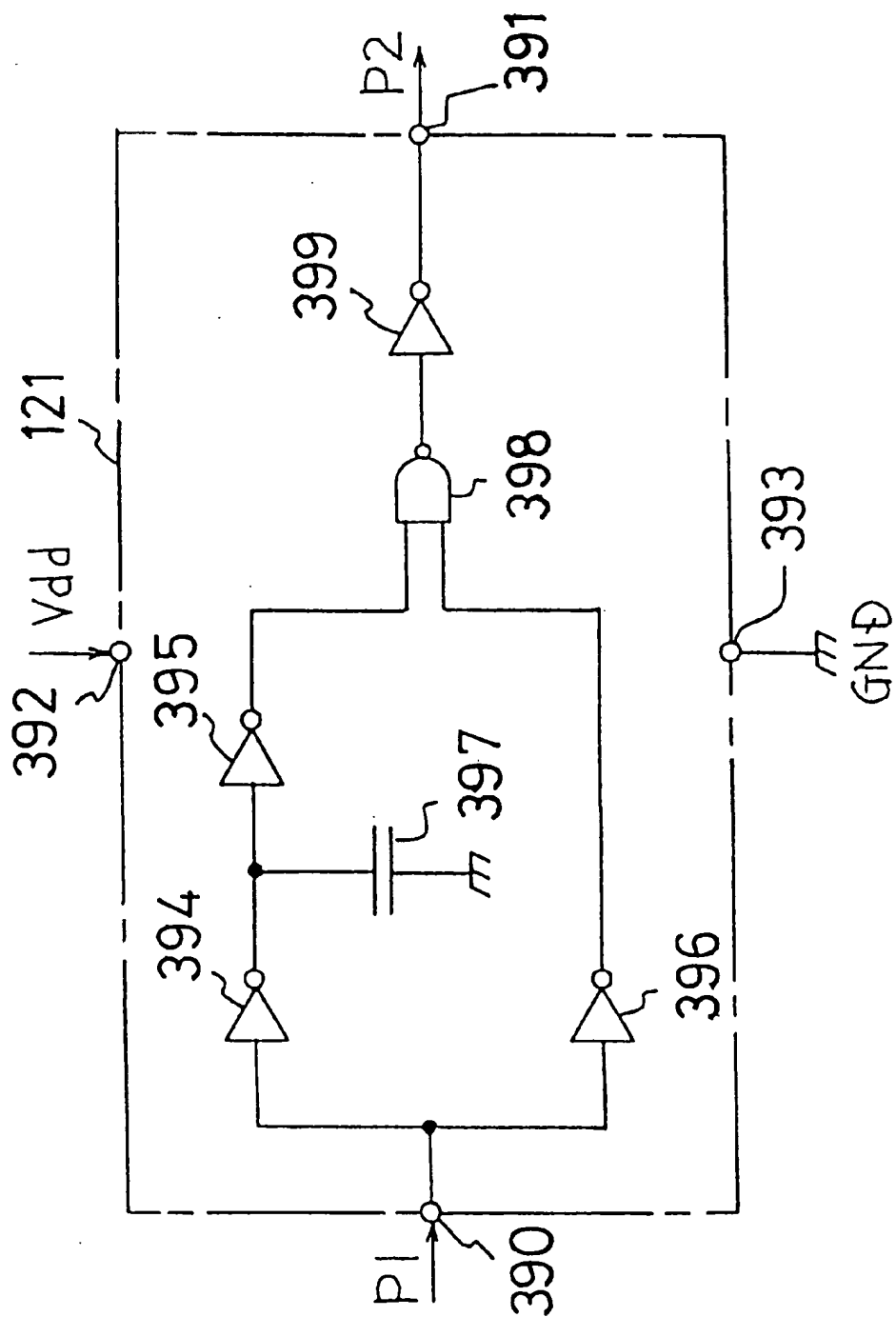


FIG. 27

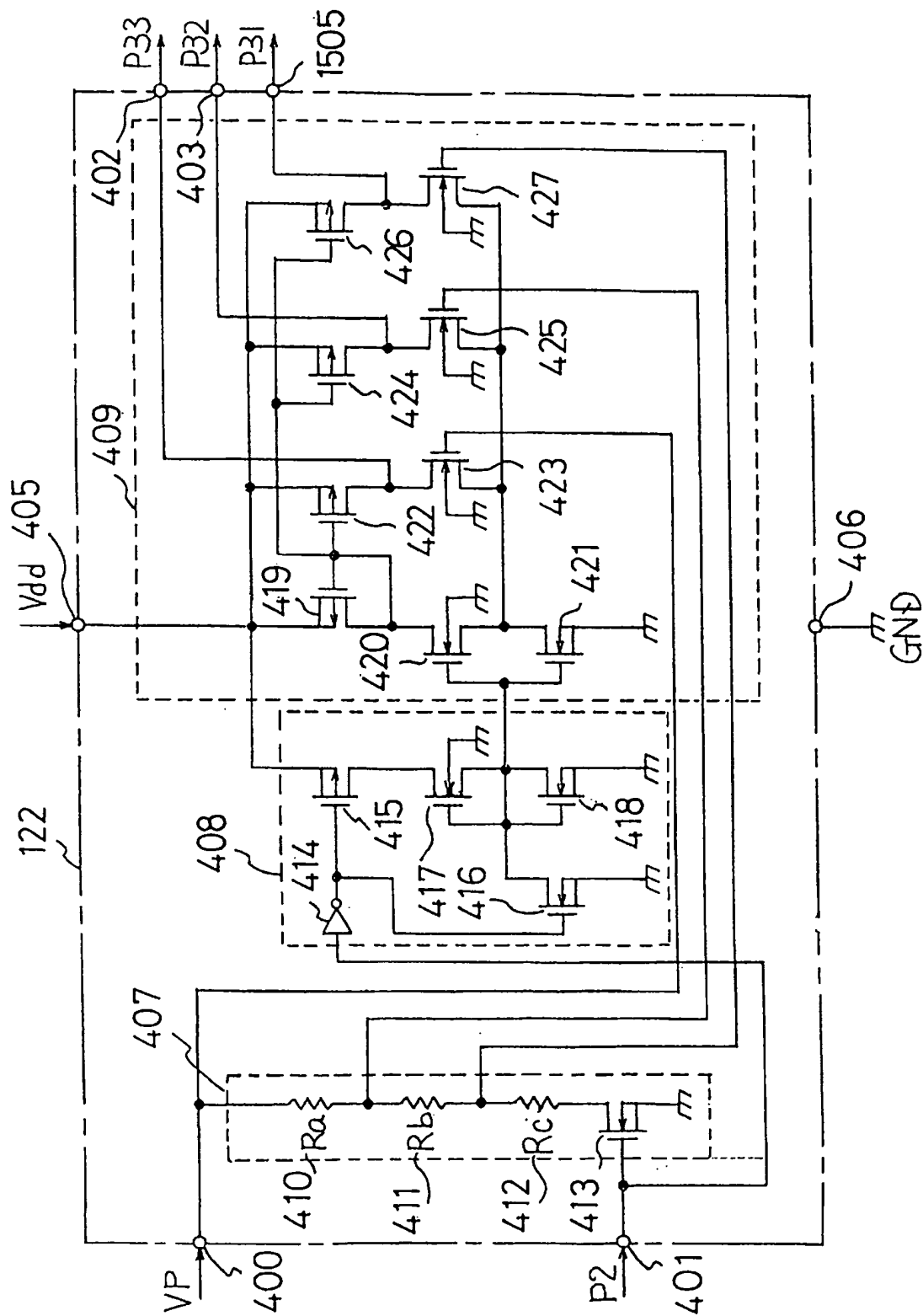




FIG. 29

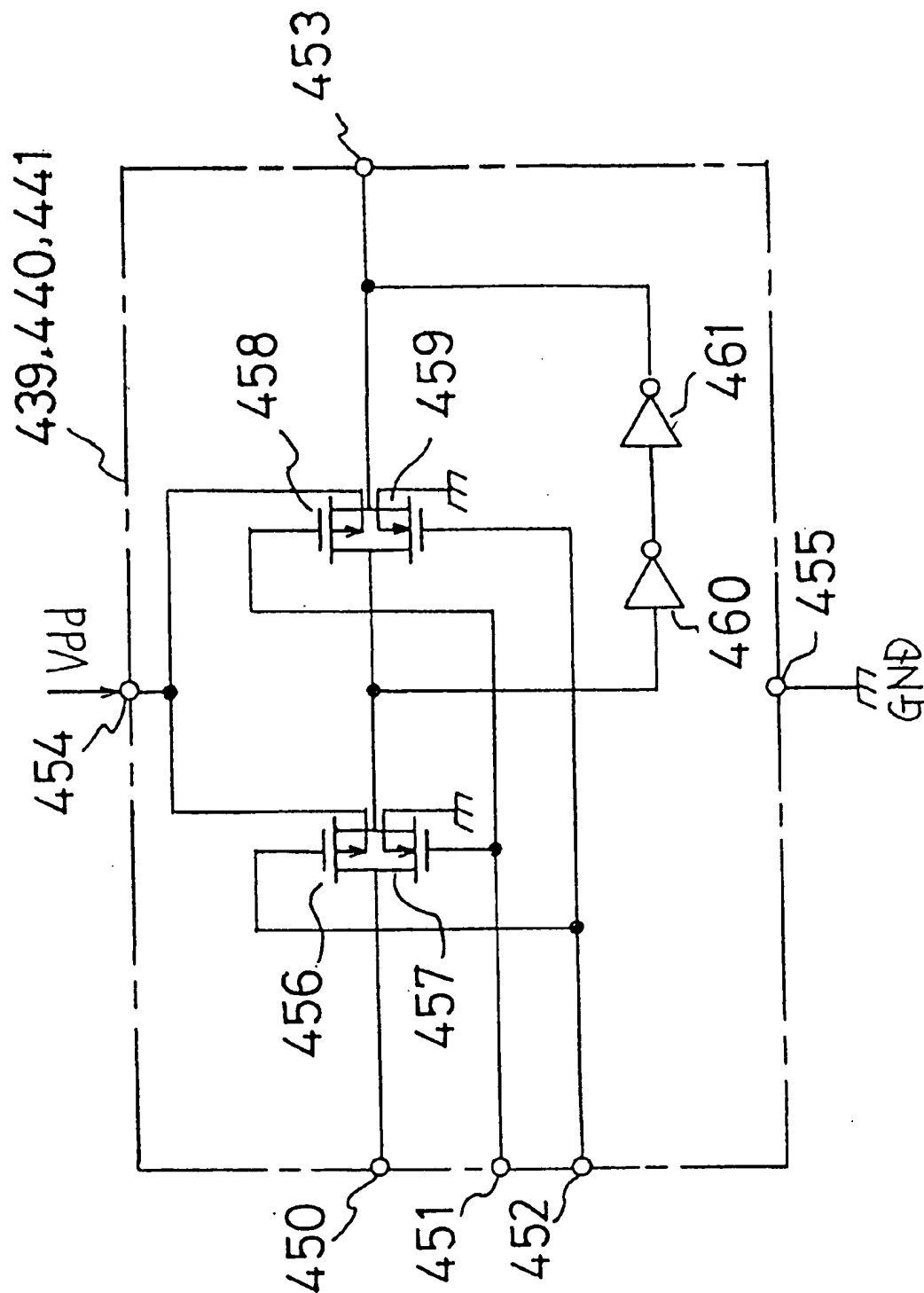
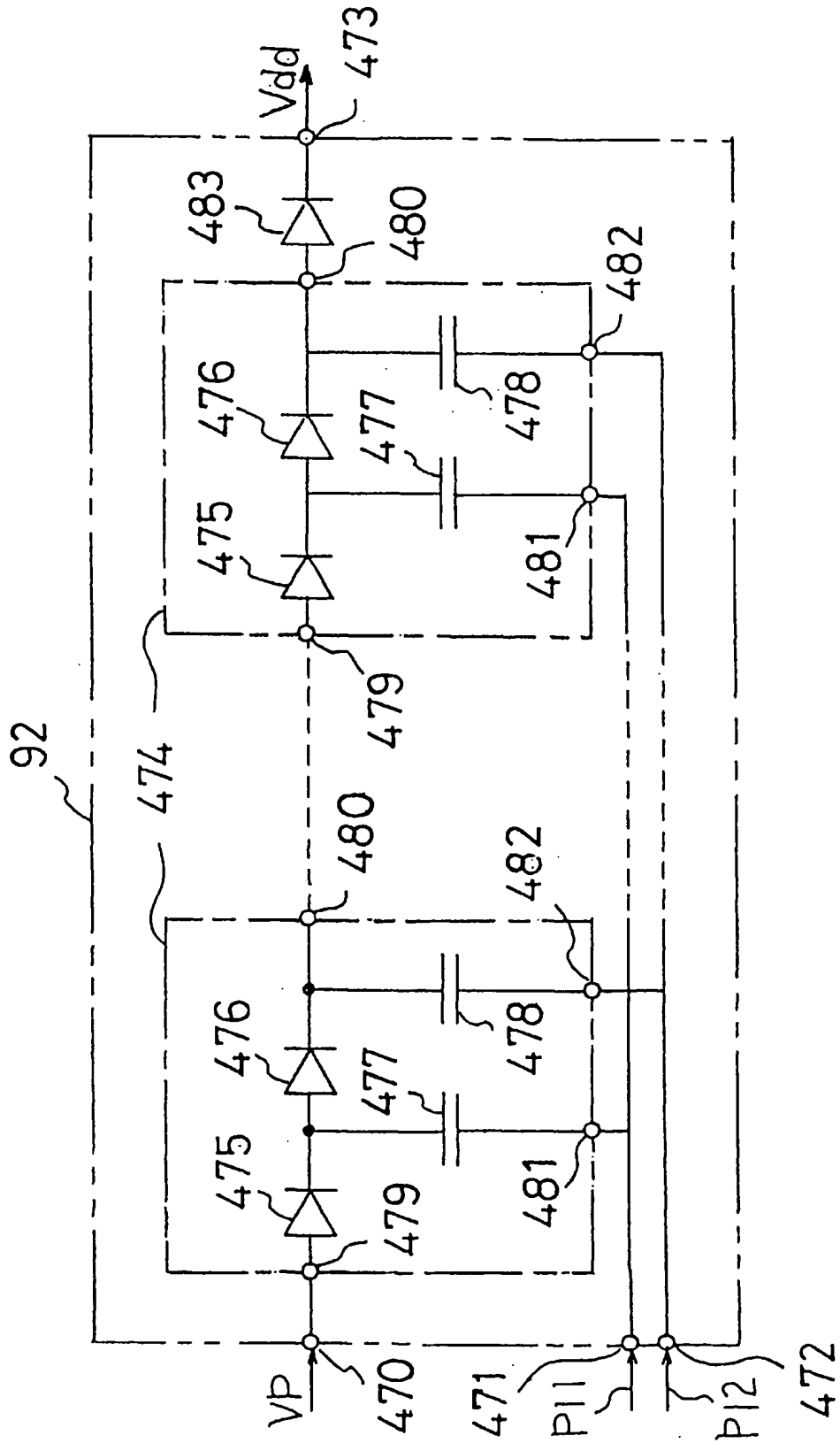


FIG. 30  
PRIOR ART



## ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present invention relates to an electronic apparatus that is driven by electric power of a generator in which a voltage of generated power changes as time elapses or a power supply in which the voltage thereof changes as time elapses, particularly to a portable electronic apparatus.

## 2. Description of the Related Art

Conventional electric apparatuses include a generator in which the voltage of generated power changes as time elapses or a power supply in which the voltage thereof changes as time elapses. In such electronic apparatuses, in order to continuously operate a driving circuit of the electronic apparatuses, a power supply capacity of the generator or the power supply is set so that the voltage of the generator or the power supply does not fall below the minimum driving voltage of the driving circuit of the electronic apparatuses even if the voltage changes as time elapses.

Also, as shown in FIG. 9, conventional electronic apparatuses include a generator in which the voltage of the generated power changes as time elapses or a power supply 90 in which the voltage changes as time elapses, a booster circuit 92 for boosting such generated power or the power of the power supply, and an oscillator circuit 91 that drives the booster circuit 92. In the electronic apparatus, the oscillator circuit 91 is driven by the generator in which the voltage of the generated power changes as time elapses or the power supply 90 in which the voltage changes as time elapses. Further, the booster circuit 92 is driven by an output clock of the oscillator circuit 91, and the power of the generator or the power supply 90 in which the voltage of the supplied power changes as time elapses is boosted by the booster circuit 92, to thereby drive a driving circuit of the electronic apparatus. Accordingly, in order to continuously operate the driving circuit of the electronic apparatus, a power supply capacity of the generator or the power supply 90 is set so that the voltage of the generator or the power supply 90 does not fall below the minimum driving voltage of the oscillator circuit 91 even if the voltage changes as time elapses.

Also, conventional electronic apparatuses include a generator in which the voltage of the generated power changes as time elapses or a power supply in which the voltage changes as time elapses, a booster circuit for boosting such generated power or the power of the power supply, an oscillator circuit that drives the booster circuit, and a capacitor for accumulating the boosted power and supplying power to a driving circuit of the electronic apparatus. In this electronic apparatus, the oscillator circuit is driven using the power accumulated in the capacitor, the booster circuit is driven by an output clock of the oscillator circuit, and the power of the generator or the power supply in which the voltage of supplied power changes as time elapses is boosted by the booster circuit. Then, the booster power is accumulated in the capacitor so that the driving circuit of the electronic apparatus is driven by the power of the capacitor. Accordingly, in order to continuously operate the driving circuit of the electronic apparatus, the capacitor is always charged so that the power accumulated in the capacitor does not become empty and that the voltage of the capacitor does not fall below the minimum driving voltage of the oscillator circuit.

Now, an example of an electronic apparatus using a thermoelectric conversion device as a generator is shown as a prior art. In the thermoelectric conversion device, a P-type

thermoelectric material element and an N-type thermoelectric material element are sandwiched between two substrates, a plurality of P-type thermoelectric material elements and N-type thermoelectric material elements form a p-n junction on the substrates through an electrically conductive material such as metal to be connected in series with one another. The thermoelectric conversion device produces electromotive power by a temperature difference between the two substrates, to thereby generate power. The power generated per thermoelectric material element is about  $200 \mu\text{V}/^\circ\text{C}$ . When, for example, a circuit that drives at 1.5 V is directly driven by the thermoelectric conversion device, assuming that the temperature difference between the substrates is  $2^\circ\text{C}$ ., at least 1,875 pairs of p-n junctions are required. Furthermore, since the thermoelectric conversion device is influenced by the atmospheric temperature, a large margin for generating power is allowed to thereby increase pairs of p-n junctions. Accordingly, the electronic apparatus using the thermoelectric conversion device requires a large heat radiating plate, because the size of the thermoelectric conversion device is increased and the number of heat-propagating paths is also increased.

FIG. 30 shows a conventional booster circuit. In FIG. 30, reference numeral 470 denotes an electromotive voltage input terminal for inputting the electromotive voltage  $V_p$  of the power supply 90, 471 denotes a first clock signal input terminal for inputting a first clock signal P11 which is one of clock signals P1 outputted from the oscillator circuit 91, 472 denotes a second clock signal input terminal for inputting a second clock signal P12 which is one of the clock signals P1, 473 denotes a boosted voltage output terminal for outputting a boosted voltage  $V_{dd}$ , 474 denotes a booster unit, and 483 denotes a diode.

The more the number of booster units 474 connected in series with one another is, the more the boosting factor is. In the booster unit 474, reference numeral 479 denotes an input terminal, 480 denotes a boosted voltage output terminal, 481 denotes a first clock signal input terminal for inputting a first clock signal P11, 482 denotes a second clock signal input terminal for inputting a second clock signal P12, 475 and 476 denote diodes, and 477 and 478 denote capacitors.

A signal obtained by inverting the first clock signal P1 is a second clock signal P2. Since operation of the circuit is already well known, it is omitted.

In the conventional electronic apparatuses, in order to continuously operate a driving circuit of the electronic apparatus, a power supply capacity of a generator or a power supply is set so that the voltage of the generator or the power supply does not fall below the minimum driving voltage of the driving circuit of the electronic apparatus even if the voltage changes as time elapses. For this reason, when the voltage of the generator or the power supply exceeds the minimum driving voltage of the driving circuit of the electronic apparatus, the electric power is wastefully used, whereby the efficiency of the whole system is deteriorated. Furthermore, since the power supply capacity is set so that the voltage of the generator or the power supply does not fall below the minimum driving voltage of the driving circuit of the electronic apparatus, the generator or the power supply is unpreferably enlarged. Particularly, in the case where the above-described electronic apparatus is used in a portable apparatus, there is such a problem that the size of the generator or the power supply is increased.

Furthermore, in the conventional electronic apparatus, an oscillator circuit is driven by the power of the generator or the power supply, and a booster circuit is driven by a clock

signal from the oscillator circuit. For this reason, even if the voltage of the generator or the power supply falls slightly below the minimum driving voltage of the oscillator circuit, the oscillator circuit, the booster circuit, and then the whole system stop their operations. At this time, the generator or the power supply supplies, to the booster circuit, electric power whose voltage is only slightly below the voltage of the minimum driving voltage of the oscillator circuit. Since the system is, however, in a non-operation state, the efficiency of the whole system is considerably deteriorated. Therefore, in order to continuously supply power to the driving circuit of the electronic apparatus, it is required that the voltage of the generator or the power supply does not fall below the minimum driving voltage of the oscillator circuit even if the voltage changes as time elapses. On the other hand, in the case where the voltage of the generator or the power supply greatly exceeds the minimum driving voltage of the oscillator circuit, the voltage after boosting operation greatly exceeds a voltage necessary for the driving circuit of the electronic apparatus. The thus generated excess power is changed into useless energy such as heat. Furthermore, since the power supply capacity is set so that the voltage of the generator or the power supply does not fall below the minimum driving voltage of the oscillator circuit, there is such a problem that the size of generator or the power supply is unpreferably increased.

Also, in the conventional electronic apparatus, power accumulated in the capacitor is used to drive the oscillator circuit and boost the output power of the generator or the power supply. The thus boosted power is accumulated in the capacitor to drive the driving circuit of the electronic apparatus by the power of the capacitor. Accordingly, in order to continuously operate the driving circuit of the electronic apparatus, the capacitor is always charged so that the power of the capacitor does not become empty and the voltage of the capacitor does not fall below the minimum driving voltage of the oscillator circuit. Therefore, since the power of the capacitor becomes empty if the charged power of the capacitor is less than the power that is consumed by the driving circuit of the electronic apparatus, the generator or the power supply requires large power supply capacity. Also, there is such a problem that when the voltage of the capacitor falls below the minimum driving voltage of the oscillator circuit, the operation of the whole system is stopped.

In the case where the thermoelectric conversion device is used as the generator of the above-described electronic apparatus, thermoelectric material elements must be connected in series with one another so that the output voltage of the thermoelectric conversion device always exceeds the minimum driving voltage of the driving circuit or oscillator circuit of the electronic apparatus. Further, since the thermoelectric conversion device generates power by a temperature difference and is influenced by the atmospheric temperature, a larger number of the thermoelectric material element are required to be connected in series with one another. For this reason, the thermoelectric conversion device is enlarged, and the number of heat-propagating paths is increased, so that a larger heat radiating plate is required. Accordingly, it is difficult to employ the above-described electronic apparatus for a portable apparatus.

The conventional voltage booster system has first a disadvantage that its booster circuit needs to have a plurality of diodes and has a loss caused by the diodes. A Schottky diode is often used as the diode in order to reduce a forward voltage drop. However, even using the Schottky diode cannot avoid a voltage loss and power loss caused by a

forward voltage loss, and there is a problem that a voltage of 0.2 V or so is lost in each of the Schottky diodes.

Next, since the conventional booster circuit does not have a means for detecting the voltage of a power supply, it cannot set the boosting factor of the booster circuit at an appropriate value according to the voltage of the power supply. Namely, there are problems that a charging efficiency is dropped by a fact that when a secondary battery is charged by a certain boosted voltage of the booster system, the trouble of charging a secondary battery through a booster circuit having a high boosting factor which is great in loss is taken even in case that the secondary battery can be charged by a booster circuit having a low boosting factor thanks to a sufficiently high voltage of the power supply, and that a boosted voltage exceeds the upper limit of a driving voltage for driving an IC or the like since the voltage of a power supply becomes higher in case that the IC or the like is driven by the boosted voltage.

#### SUMMARY OF THE INVENTION

The present invention has been made in view of the above-described problems, and therefore has an object to provide an electronic apparatus having a high power efficiency of the whole system, and to provide a system capable of boosting a lower voltage to thereby improve the boosting efficiency.

An electronic apparatus according to the present invention is comprised of: a generator in which the voltage of power generated by thermoelectric devices, etc. changes as time elapses or a power supply in which the voltage changes as time elapses; a booster circuit for boosting an output voltage of the generator or the power supply; and an oscillator circuit which drives the booster circuit. The oscillator circuit is operated and the booster circuit is driven by an output clock of the oscillator circuit, whereby the voltage generated from the generator or the power supply is boosted.

In the electronic apparatus, once the voltage for driving the oscillator circuit is inputted, the booster circuit is operated, and the oscillator circuit can continuously be operated by the output of the oscillator circuit. Accordingly, even if the voltage of the generator or the power supply changes as time elapses, and the voltage falls below the minimum driving voltage of the oscillator circuit, the voltage can be boosted to the minimum driving voltage of the oscillator circuit or higher.

Also, in the electronic apparatus according to the present invention, by providing a voltage detecting circuit for the power supply, the stages of the operation of the booster circuit are switched, or an oscillating frequency of the oscillator for generating a clock pulse for driving the booster circuit is varied, whereby the boosting rate can be varied. As a result, a constant output voltage can be efficiently obtained to the power supply in which the voltage is greatly varied.

Further, in the electronic apparatus of the present invention, the operation of the voltage detecting circuit is made intermittent, and a storage circuit for storing an output of the voltage detecting circuit is provided until a pulse for starting a subsequent operation is, whereby the current consumption of the voltage detecting circuit can be reduced.

Also, in at least one of MOS transistor used in the booster circuit, a gate and a channel are of the same conductive type, whereby an absolute value of the threshold voltage of MOS transistor can also be reduced.

By the above-described structure, a small-sized portable apparatus such as a wristwatch using as a power supply a thermoelectric conversion device or solar cell in which the voltage is greatly varied can be realized.



## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a system block diagram showing an electronic apparatus according a first embodiment of the present invention.

FIG. 2 is a system block diagram showing an electronic apparatus according a second embodiment of the present invention.

FIG. 3 is a system block diagram showing an electronic apparatus according a third embodiment of the present invention.

FIG. 4 is a system block diagram showing an electronic apparatus according a fourth embodiment of the present invention.

FIGS. 5A-B are a perspective plan view and a cross-sectional view showing a thermoelectric conversion device according to the present invention.

FIG. 6 is a graph showing characteristics of an output voltage of the thermoelectric conversion device in accordance with time-sequential changes.

FIG. 7 is a perspective plan view in which the thermoelectric conversion device of the electronic apparatus according to the present invention is provided in a wristwatch.

FIG. 8 is a cross-sectional view in which the thermoelectric conversion device of the electronic apparatus according to the present invention is provided in a wristwatch.

FIG. 9 is a block diagram showing a conventional booster system.

FIG. 10 is a booster circuit diagram showing a coil booster system of the electronic apparatus of the present invention.

FIG. 11 is a circuit diagram showing an oscillator circuit used in the coil-boosting operation of the electronic apparatus of the present invention.

FIG. 12 is a block diagram showing an embodiment of a booster system of the electronic apparatus of the present invention.

FIG. 13 is a block diagram showing a booster circuit in a switched capacitor system of the electronic apparatus of the present invention.

FIG. 14 is a circuit diagram showing a first booster circuit in the switched capacitor system of the electronic apparatus of the present invention.

FIG. 15 is a circuit diagram showing a second booster circuit in the switched capacitor system of the electronic apparatus of the present invention.

FIG. 16 is a circuit diagram showing third and fourth booster circuit in the switched capacitor system of the electronic apparatus of the present invention.

FIG. 17 is a circuit diagram showing an embodiment of the booster circuit of the electronic apparatus according to the present invention.

FIG. 18 is a circuit diagram showing a booster circuit of the electronic apparatus according to the present invention.

FIG. 19 is a circuit diagram showing a booster circuit of the electronic apparatus according to the present invention.

FIG. 20 is a circuit diagram showing a booster circuit of the electronic apparatus according to the present invention.

FIG. 21 is a circuit diagram showing an embodiment of the booster circuit of the electronic apparatus according to the present invention.

FIG. 22 is a circuit diagram showing an embodiment of the booster circuit of the electronic apparatus according to the present invention.

FIG. 23 is a circuit diagram showing an embodiment of the booster circuit of the electronic apparatus according to the present invention.

FIG. 24 is a circuit diagram showing an oscillator circuit used in the switched capacitor system of the electronic apparatus of the present invention.

FIG. 25 is a circuit diagram showing an embodiment of an oscillator circuit of the electronic apparatus according to the present invention.

FIG. 26 is a circuit diagram showing an embodiment of an intermittent pulse generator circuit of the electronic apparatus according to the present invention.

FIG. 27 is a circuit diagram showing an embodiment of a voltage detecting circuit of the electronic apparatus according to the present invention.

FIG. 28 is a circuit diagram showing an embodiment of a signal storage circuit of the electronic apparatus according to the present invention.

FIG. 29 is a circuit diagram showing an embodiment of a signal storage circuit of the electronic apparatus according to the present invention.

FIG. 30 is a circuit diagram showing a booster circuit in a conventional booster system.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

According to one aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; and an oscillator circuit 13 which drives the booster circuit 12. The oscillator circuit 13 is operated and the booster circuit 12 is driven by an output clock of the oscillator circuit 13, whereby the output voltage generated from the generator or the power supply 11 is boosted. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as times elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

Also, according to another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; and an oscillator circuit 13 which drives the booster circuit 12. When the voltage of the generator or the power supply 11 changes as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, the oscillator circuit 13 obtains power for starting oscillation

from the generator or the power supply 11. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Once the voltage exceeds the minimum driving voltage of the oscillator circuit, the booster circuit 12 can be driven, and therefore, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; and an oscillator circuit 13 which drives the booster circuit 12. When the voltage of the generator or the power supply 11 changes as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, the oscillator circuit 13 obtains power for starting oscillation from the generator or the power supply 11. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. The oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without any other power sources. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes

as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; and a power source 30 provided independently of the generator or the power supply 11. The oscillator circuit 13 obtains power necessary for starting oscillation from the power source 30 provided independently of the generator or the power supply 11. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Further, since the electronic apparatus 10 according to the present invention can continue operating even if the voltage of the generator or the power supply 11 cannot exceed the minimum driving voltage of the oscillator circuit as time elapses, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; and a power source 30 provided independently of the generator or the power supply 11. The oscillator circuit 13 obtains power necessary for starting oscillation from the power source 30 provided independently of the generator or the power supply 11. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. The oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Further, since the electronic apparatus 10 according to the present invention can continue operating even if the voltage of the generator or the power supply 11 cannot exceed the minimum driving voltage of the oscillator circuit as time elapses, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, once the output voltage of the power source 30

provided independently of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without any other power sources. Further, since it is not necessary for the power source 30 provided independently of the generator or the power supply 11 to always supply power to the oscillator circuit 13, the power source 30 can be downsized. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; a control circuit 40 for dividing the power into a driving circuit 42 of the electronic apparatus and a capacitor 41 or form the capacitor 41 to the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the driving circuit 42 of the electronic apparatus; and the driving circuit 42 of the electronic apparatus which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. The oscillator circuit 13 obtained power for starting when the voltage of the generator or the power supply 11 changes as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, or the oscillator circuit 13 obtains power from the capacitor 41. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. The oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, since the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without any other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole

system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is divided into the capacitor 41 or the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the generator or the power supply 11 can efficiently be consumed.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a thermoelectric conversion device 71 in which P-type thermoelectric material elements 52 and N-type thermoelectric material elements 53 are sandwiched between two substrates and form a p-n junction through an electrically conductive material such as metal to be connected in series with one another; a booster circuit 12 for boosting an output voltage of the thermoelectric conversion device 71; an oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; a control circuit 40 for dividing the power into a driving circuit 42 of the electronic apparatus and a capacitor 41 or from the capacitor 41 to the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the driving circuit 42 of the electronic apparatus; and the driving circuit 42 of the electronic apparatus which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. The oscillator circuit 13 obtains power for starting when the voltage of the thermoelectric conversion device 71 changes as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, or the oscillator circuit 13 obtains power from the capacitor 41. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. The oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the thermoelectric conversion device 71 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the driving circuit 42 of the electronic apparatus. Thus, in the case where the electronic apparatus 10 is continuously driven, since the output voltage of the thermoelectric conversion device 71 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the thermoelectric conversion device 71 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, once the output voltage of the thermoelectric conversion device 71 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without any other power sources. Particularly, since the output voltage of the thermoelectric conversion device 71 at a time instant when

a temperature difference generates is several times as large as the voltage in a constant state after time elapses, the thermoelectric conversion device 71 is suitable for the electronic apparatus 10 according to the present invention. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the convention electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the thermoelectric conversion device 71 can efficiently be consumed.

Also, according to still another aspect of the present invention, an electronic apparatus 10 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; and oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; a control circuit 40 for dividing the power into a watch movement 75 and a capacitor 41 or from the capacitor 41 to the watch movement 75 according to a value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the watch movement 75; and the watch movement 75 including a time display function, which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. The oscillator circuit 13 obtains power for starting when the voltage of the generator or the power supply 11 changes as time elapses to that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, or the oscillator circuit 13 obtains power from the capacitor 41. The oscillator circuit 13 that has started oscillation drives the booster circuit 12 to thereby boost the output voltage generated by the generator or the power supply 11. The oscillator circuit 13 after starting oscillation continuously performs oscillation using the power boosted by the booster circuit 12. At this time, the electronic apparatus 10 according to the present invention, even if the voltage of the generator or the power supply 11 changes as time elapses to be lower than the minimum driving voltage of the oscillator circuit, boosts the voltage to not lower than the minimum driving voltage of the oscillator circuit or the driving voltage of the watch movement 75. Thus, since the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to a broader application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the

watch movement 75 without any other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the watch movement 75 according to a value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the generator or the power supply 11 can efficiently be consumed.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, an input terminal 160 is connected to the drain of an N-channel type MOS transistor 164 and the source of an N-channel type MOS transistor 165, a first clock signal input terminal 162 is connected to the gates of the N-channel type MOS transistor 165 and an N-channel type MOS transistor 166, a second clock signal input terminal 163 is connected to the gates of the N-channel type MOS transistor 164 and an N-channel type MOS transistor 167, the source of the N-channel type MOS transistor 164 is connected to the drain of the N-channel type MOS transistor 166 and a second electrode of a capacitor 168, a first electrode of the capacitor 168 is connected to the drain of the N-channel type MOS transistor 165 and the source of the N-channel type MOS transistor 167, an output terminal 161 for outputting a boosted voltage is connected to the drain of the N-channel type MOS transistor 167, and a GND input terminal 169 is connected to the source of the N-channel type MOS transistor 166. A voltage is boosted by a factor of 2, by repeating the operation in which an input voltage is supplied to the second electrode of the capacitor 168 the first electrode of which is connected to the GND terminal and the input voltage is supplied to the first electrode to thereby output a boosted voltage two times higher than the input voltage generated at the second electrode. Thus, there is an effect that, in the case where a voltage to be boosted is low and each of these N-channel type MOS transistor has only to supply a voltage not higher than the maximum voltage of each N-channel type MOS transistor, it can efficiently boost the voltage and further can boost the voltage however low it is.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, an input terminal 170 is connected to the drain of an N-channel type MOS transistor 174 and the source of an N-channel type MOS transistor 175, a first clock signal input terminal 172 is connected to the gates of the N-channel type MOS transistor 175, 176, and 177, a second clock signal input terminal 173 is connected to the gate of the N-channel type MOS transistor 174, the source of the N-channel type MOS transistor 174 is connected to the drain of the N-channel type MOS transistor 176 and a second electrode of a capacitor 178, a first electrode of the capacitor 178 is connected to the drain of the N-channel type MOS transistor 175 and the drain of the P-channel type MOS transistor 177, an output terminal 171 for outputting a boosted voltage is connected to the source grounded on the substrate of the P-channel type MOS transistor 177, and a GND terminal

179 is connected to the source of the N-channel type MOS transistor 176. A voltage is boosted by a factor of 2, by repeating the operation in which an input voltage is supplied to the second electrode of the capacitor 178 the first electrode of which is connected to the GND terminal and the input voltage is then supplied to the first electrode to thereby outputs a boosted voltage two times higher than the input voltage generated at the second electrode. In the structure as described above, in the case where a voltage to be boosted is lower than the maximum voltage of the N-channel type MOS transistors 174 and 175 and a boosted voltage generated at the first electrode of the capacitor 178 is higher than the minimum voltage which the P-channel type MOS transistor 177 can supply, there is an effect that it can efficiently boost the voltage.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, an input terminal 180 is connected to the source grounded on the substrate of a P-channel type MOS transistor 184 and the drain of a P-channel type MOS transistor 185, a first clock signal input terminal 182 is connected to the gates of P-channel type MOS transistor 184 and 187, and the gate of an N-channel type MOS transistor 186, a second clock signal input terminal 183 is connected to the gate of the P-channel type MOS transistor 185, the drain of the P-channel type MOS transistor 184 is connected to the drain of the N-channel type MOS transistor 186 and a second electrode of a capacitor 188, a first electrode of a capacitor 188 is connected to the source grounded on the substrate of the P-channel type MOS transistor 185 and the drain of the P-channel type MOS transistor 187, an output terminal 181 for outputting a boosted voltage is connected to the source grounded on the substrate of the P-channel type MOS transistor 187, and a GND terminal 189 is connected to the source of the N-channel type MOS transistor 186. A voltage is boosted by a factor of 2, by repeating the operation in which an input voltage is supplied to the second electrode of the capacitor 188 and the input voltage is then supplied to the first electrode to thereby output a boosted voltage two times higher than the input voltage generated at the second electrode. In the structure as described above, the system has a feature that a high voltage can be also boosted if the voltage is not lower than the minimum voltage that each P-channel type MOS transistor can supply.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, a first input terminal 222 is connected to the drain of an N-channel type MOS transistor 227, an second input terminal 221 is connected to the source of an N-channel type MOS transistor 228, a first clock signal input terminal 224 is connected to the gate of the N-channel type MOS transistor 227, a second clock signal input terminal 225 is connected to the gates of the N-channel type MOS transistor 228 and 229, the source of the N-channel type MOS transistor 227 is connected to the drain of the N-channel type MOS transistor 229 and a second electrode of a capacitor 210, a first electrode of the capacitor 210 is connected to the drain of the N-channel type MOS transistor 228 and an output terminal 223 for outputting a boosted voltage, and a GND input terminal 226 is connected to the source of the N-channel type MOS transistor 229. Such a boosting operation is repeated that an input voltage is supplied to the first electrode of the capacitor 210 and then the input voltage is supplied to the second electrode, to thereby obtain a boosted voltage generated at the first electrode plus a voltage at the second electrode. In such a structure, there is an effect that, in the case where a voltage to be boosted is low and each of

these N-channel type MOS transistors has only to supply a voltage not higher than the maximum voltage of each N-channel type MOS transistor, it can efficiently boost the voltage and further can boost the voltage however low it is.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, a first input terminal 242 is connected to the drain of a P-channel type MOS transistor 247, a second input terminal 241 is connected to the source of an N-channel type MOS transistor 248, a first clock signal input terminal 244 is connected to the gate of the P-channel type MOS transistors 247, a second clock signal input terminal 245 is connected to the gates of N-channel type MOS transistors 248 and 249, the source of the P-channel type MOS transistor 247 is connected to the drain of the N-channel type MOS transistor 249 and a second electrode of a capacitor 250, a first electrode of a capacitor 250 is connected to the drain of the N-channel type MOS transistor 248 and an output terminal 243 for outputting a boosted voltage, and a GND input terminal 246 is connected to the source of the N-channel type MOS transistor 249. Such a boosting operation is repeated that an input voltage is supplied to the first electrode of the capacitor 250 and then the input voltage is supplied to the second electrode, to thereby obtain the input voltage generated at the first electrode plus the voltage generated at the second electrode. In the structure as described above, there is an effect that, in the case where a voltage to be inputted into the second input terminal 241 is lower than the maximum voltage which the N-channel type MOS transistor 248 can supply and a voltage to be inputted into the first input terminal 242 is not lower than the minimum voltage of the P-channel type MOS transistor 247, it can efficiently boost the voltage.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, an input terminal 300 is connected to the drain of an N-channel type MOS transistor 306, the gate of the N-channel type MOS transistor 306 is connected to a first clock signal input terminal 302, the source of the N-channel type MOS transistor 306 is connected to a first electrode of a capacitor 308 and the drain of an N-channel type MOS transistor 307, a second electrode of the capacitor 308 is connected to a third clock signal input terminal 304, the gate of the N-channel type MOS transistor 307 is connected to a second clock signal input terminal 303, the source of the N-channel type MOS transistor 307 is connected to a first electrode of a capacitor 309 and an output terminal 301, a second electrode of the capacitor 309 is connected to a fourth clock signal input terminal 305. Power is fed sequentially from the input terminal 300 to the capacitor 308 and the capacitor 309 to output the boosted power from the output terminal 301. In such a structure, there is an effect that, in the case where a voltage to be boosted is low or Vdd is high and the maximum voltage which each of the N-channel type MOS transistors can supply is also high, and each N-channel type MOS transistor has only to supply a voltage not higher than the maximum voltage of each N-channel type MOS transistor, it can efficiently boost the voltage and further can boost the voltage however low it is.

Also, according to still another aspect of the present invention, the structure to be described below is adopted. That is, an input terminal 311 is connected to the drain of a P-channel type MOS transistor 317, the gate of the P-channel type MOS transistor 317 is connected to a second clock signal input terminal 314, the source of the P-channel type MOS transistor 317 is connected to a first electrode of a capacitor 319 and the drain of a P-channel type MOS

transistor 318, a second electrode of the capacitor 319 is connected to a third clock signal input terminal 315, the gate of the P-channel type MOS transistor 318 is connected to a first clock signal input terminal 313, the source of the P-channel type MOS transistor 318 is connected to a first electrode of a capacitor 320 and an output terminal 312, a second electrode of the capacitor 320 is connected to a fourth clock signal input terminal 316. Power is fed sequentially from the input terminal 311 to the capacitor 319 and the capacitor 320 to output the boosted power from the output terminal 312. In such a structure, there is an effect that, in the case where a voltage to be boosted is high and each of these P-channel type MOS transistors supplies a voltage that is not lower than the minimum voltage which each P-channel type MOS transistor can supply, it can efficiently boost the voltage and further can boost the voltage however high it is.

A booster circuit of a booster system of the present invention boosts a voltage by charging and discharging a capacitor by means of the N-channel type MOS transistor or the P-channel type MOS transistor.

The booster circuit of a booster system of the present invention may have any circuit system basically having such an arrangement, but the following three circuit systems are recommended; a first circuit system which boosts a voltage by a factor of  $2n$  by means of a plurality of booster circuits connected in series with one another each of which boosts a voltage by a factor of 2, by repeating the operation in which an input voltage is supplied to a second electrode of the capacitor the first electrode of which is connected to a GND terminal and the input voltage is then supplied to the first electrode to thereby output a boosted voltage two times higher than the input voltage generated at the second electrode; or a second circuit system that boosts a voltage by a factor of  $(1+n)$  by charging a plurality of capacitors in parallel and then connecting the capacitors in series with one another; and furthermore a third circuit system which replaces a diode of the conventional booster circuit with an MOS transistor and thereby boosts a voltage by a factor of  $(1+n)$ .

In an oscillator circuit of a booster system of the present invention, it is recommended that its power source voltage is a boosted voltage in order to display to the utmost the ability of an MOS transistor receiving a clock signal from the oscillator circuit with its gate, namely in order to make the MOS transistor receive a clock signal having the highest voltage, namely, the wave height value of the boosted voltage. Moreover, in the case where the voltage of a power supply varies, in order to obtain the optimal voltage according to the voltage of the power source, it is preferable that a clock signal is made so as to vary according to the voltage of the power source. Namely, it is recommended that the oscillator circuit vary the frequency of its output clock signal according to the voltage of the power supply.

On the other hand, it is recommended that a booster system of the present invention is provided with a voltage detecting circuit for detecting the voltage of a power supply and changes the boosting factor of a booster circuit according to a detection signal outputted from the voltage detecting circuit according to the voltage of the power supply.

It is recommended that the voltage detecting circuit of the present invention operates intermittently in order to reduce its current consumption, and it is recommended that the booster system is provided additionally with an intermittent pulse generator circuit and a signal storage circuit in order to make the voltage detecting circuit operate intermittently,

and the voltage detecting circuit is operated intermittently by intermittent pulses generated by the intermittent pulse generator circuit, and a detection signal outputted at the time of operation of the voltage detecting circuit is inputted into the booster circuit through the signal storage circuit, and a detection signal at the time of operation of the voltage detecting circuit continues to be outputted to the booster circuit until the next operation.

Moreover, it is recommended that each of the circuits in a booster system of the present invention keeps low the absolute value of a threshold voltage of each MOS transistor forming each circuit in the booster system by making respectively a P-channel type MOS transistor have a P-type gate or an N-channel type MOS transistor have an N-type gate so as to operate at a lower voltage, namely, by making it possible to suppress an off-leak current even in case of lowering the absolute value of the threshold voltage.

Although a power supply of this booster system may be any power supply which generates an electromotive voltage, this system is effective to boost a voltage of a thermoelectric conversion device, a solar cell, a charged capacitor which vary in electromotive voltage, and particularly this booster system has features of making it possible to operate at a low voltage and boost a voltage in a high efficiency, and therefore it can make a thermoelectric conversion device small in volume and realize such a small-sized portable apparatus as a wristwatch and the like having a thermoelectric conversion device as a power supply by being used in boosting a voltage of the thermoelectric conversion device giving an insufficient electromotive voltage for its volume.

#### Embodiment 1

Embodiments of the present invention are described with reference to the drawings.

FIG. 1 is a block diagram showing a structure of the embodiment 1 according to the present invention.

An electronic apparatus 10 of this embodiment is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; and an oscillator circuit 13 which drives the booster circuit 12.

Connection of each circuit will now be described. An output terminal of the generator or the power supply 11 is connected to an electromotive force input terminal of the booster circuit 12. A clock signal input terminal of the booster circuit 12 is connected to a clock signal output terminal of the oscillator circuit 13. Then, a boosted power is taken out from a boosted voltage output terminal 14 of the booster circuit 12.

Next, the principle of operation of the electronic apparatus according to this embodiment will be described. First, a voltage is applied to a Vdd input terminal of the oscillator circuit 13 to operate the oscillator circuit 13 and output a clock signal having a desired frequency to the clock signal output terminal. This clock signal is inputted into the clock signal input terminal of the booster circuit 12 for boosting operation. The booster circuit 12 boosts the power of the generator or the power supply 11 inputted from the electromotive force input terminal according to a frequency and duty of the clock signal to output the boosted power to the boosted voltage output terminal 14.

Here, even if a voltage lower than the minimum driving voltage of the oscillator circuit 13 is inputted into the electromotive force input terminal of the booster circuit 12,

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the booster circuit 12 can boost the voltage up to a voltage by which all the circuits in the electronic apparatus can be operated. The electronic apparatus 10 operates using the boosted power.

By employing the above-described structure, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

## Embodiment 2

FIG. 2 is a block diagram showing a structure of the embodiment 2 according to the present invention.

An electronic apparatus 10 of this embodiment is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; and a Schottky diode 20 for rectifying the power generated by the generator or the power supply 11 and the power outputted from the booster circuit 12.

Connection of each circuit will now be described. An output terminal of the generator or the power supply 11 is connected to the electromotive force input terminal of the booster circuit 12; a P-type electrode of the Schottky diode 20 is connected to an output terminal of the generator or the power supply 11; an N-type electrode of the Schottky diode 20 is connected to a Vdd input terminal of the oscillator circuit 13; a clock signal input terminal of the booster circuit 21 is connected to a clock signal output terminal of the oscillator circuit 13; a boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13. Then, a boosted power is taken from the boosted voltage output terminal 14 of the booster circuit 12.

Next, the principle of operation of the electronic apparatus according to this embodiment will be described. When the output voltage of the generator or the power supply 11 changes from a non-output state (namely, the output voltage=0 V) as time elapses so that the voltage exceeds the minimum driving voltage of the oscillator circuit 13, the voltage of the generator or the power supply 11 is inputted into the Vdd input terminal of the oscillator circuit 13 via the Schottky diode 20 to drive the oscillator circuit 13 and start oscillation. The oscillator circuit 13 that has started oscillation outputs the clock signal to the clock signal output terminal and inputs the signal in the clock signal input terminal of the booster circuit 12. The booster circuit 12 receives the clock signal to start boosting the output voltage of the generator or the power supply 11. At this time, since the boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13, the boosted voltage is used as the power supply of the oscillator circuit 13. The Schottky diode 20 is connected between the output terminal of the generator or the power supply 11 and the Vdd input terminal of the oscillator circuit 13. Accordingly, once the oscillator circuit 13 operates to start boosting, the oscillator circuit 13 utilizes the voltage boosted by the booster circuit 12 as the power

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supply. For this reason, once the voltage of generator or power supply 11 exceeds the minimum driving voltage of the oscillator circuit 13, even if the voltage falls below the minimum driving voltage of the oscillator circuit as time elapses, the boosting operation can be continued and the electric apparatus 10 continuously is driven.

Conventionally, in the case where the oscillator circuit 13 is driven by the output voltage of the generator or the power supply 11, a large margin is required for outputting the voltage so that the output voltage of the generator or the power supply 11 does not fall below the minimum driving voltage of the oscillator circuit at any time. For this reason, the size of the generator or the power supply 11 has been increased. In the present invention, however, since the above-described structure is employed, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

## Embodiment 3

FIG. 3 is a block diagram showing a structure of the embodiment 3 of the present invention.

An electronic apparatus 10 according to the embodiment 3 is comprised of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 31 for rectifying the power generated by the generator or the power supply 11 and the power outputted by the booster circuit 12; and the power source 30 provided independently of the generator or the power supply 11.

Connection of each circuit will now be described. An output terminal of the generator or the power supply 11 is connected to an electromotive force input terminal of the booster circuit 12; a clock signal input terminal of the booster circuit 12 is connected to a clock signal output terminal of the oscillator circuit 13; a P-type electrode of the Schottky diode 31 is connected to an output terminal of the power source 30; an N-type electrode of the Schottky diode 31 is connected to a Vdd input terminal of the oscillator circuit 13; a boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13. Then, a boosted power is taken from the boosted voltage output terminal 14 of the booster circuit 12.

Next, the principle of operation of the electronic apparatus according to this embodiment will be described. First, the voltage exceeding the minimum driving voltage of the oscillator circuit 13 is inputted from the power source 30 provided independently of the generator or the power supply



11, via the Schottky diode 31, into the Vdd input terminal of the oscillator circuit 13 to drive the oscillator circuit 13 using the voltage from the power source 30 and start oscillation. The oscillator circuit 13 that has started oscillation outputs the clock signal to the clock signal output terminal and inputs the signal in the clock signal input terminal 36 of the booster circuit 12. The booster circuit 12 receives the clock signal to start boosting the output voltage of the generator or the power supply 11. At this time, since the boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13, the boosted voltage is used as the power supply of the oscillator circuit 13. Accordingly, once the oscillator circuit 13 operates to start boosting, the oscillator circuit 13 utilizes the voltage boosted by the booster circuit 12 as the power supply and it is not necessary to supply the power from the supply source 30. For this reason, even if the voltage of the generator or the power supply 11 falls below the minimum driving voltage of the oscillator circuit as time elapses, the boosting operation can be continued and the electric apparatus 10 continuously is driven. Thus, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Further, since the electronic apparatus 10 according to the present invention can continue operating even if the voltage of the generator or the power supply 11 cannot exceed the minimum driving voltage of the oscillator circuit as time elapses, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the power source 30 provided independently of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit 13, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit of the electronic apparatus without the other power sources. Further, since it is not necessary for the power source 30 provided independently of the generator or the power supply 11 to always supply power to the oscillator circuit 13, the power source 30 can be downsized. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

#### Embodiment 4

FIG. 4 is a block diagram showing a structure of the embodiment 4 according to the present invention.

An electronic apparatus 10 of this embodiment is comprises of: a generator in which the voltage of power generated changes as time elapses or a power supply 11 in which the voltage changes as time elapses; a booster circuit 12 for boosting an output voltage of the generator or the power supply 11; an oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; a control circuit 40 for dividing the power into a driving circuit 42 of the electronic apparatus and a capacitor 41 or from the capacitor 41 to the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the driving circuit 42 of the electronic apparatus; and the driving circuit 42 of the electronic apparatus which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41.

Connection of each circuit will now be described. An output terminal of the generator or the power supply 11 is connected to an electromotive force input terminal of the booster circuit 12; a P-type electrode of the Schottky diode 20 is connected to the output terminal of the generator or the power supply 11; an N-type electrode of the Schottky diode 20 is connected to a Vdd input terminal of the oscillator circuit 13; a clock signal input terminal of the booster circuit 12 is connected to a clock signal output terminal of the oscillator circuit 13; a boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13. The boosted voltage output terminal 14 of the booster circuit 12 is connected to an input terminal of a control circuit, a capacitor terminal of the control circuit is connected to an input terminal of the capacitor, and an output terminal of the control circuit is connected to a power terminal of the driving circuit 42 of the electronic apparatus. Herein, the voltage of the output terminal of the generator or power source 11 is represented as "Vp", the voltage of the boosted voltage output terminal 14 of the booster circuit 12 as "Vpp", the voltage of the power terminal of the driving circuit 42 of the electronic apparatus as "Vic", the voltage of the input terminal of the capacitor 41 as "Vca". Description will be made employing these symbols hereinafter.

Next, the principle of operation of the electronic apparatus according to this embodiment will be described. When the output voltage Vp of the generator or the power supply 11 changes from a non-output state (namely, the output voltage=0 V) as time elapses so that the output voltage Vp exceeds the minimum driving voltage of the oscillator circuit, the output voltage Vp of the generator or the power supply 11 is inputted into the Vdd input terminal of the oscillator circuit 13 via the Schottky diode 20 to drive the oscillator circuit 13 and start oscillation. The oscillator circuit 13 that has started oscillation outputs the clock signal to the clock signal output terminal and inputs the signal in the clock signal input terminal of the booster circuit 12. The booster circuit 12 receives the clock signal to start boosting the output voltage of the generator or the power supply 11. At this time, since the boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13, the boosted voltage is used as the power supply of the oscillator circuit 13. The Schottky diode 20 is connected between the output terminal of the generator or the power supply 11 and the Vdd input terminal of the oscillator circuit 13. Accordingly, once the oscillator circuit 13 operates to start boosting, the oscillator circuit 13 utilizes the voltage boosted by the booster circuit 12 as the power supply. For this reason, once the voltage of generator or power supply 11 exceeds the minimum driving voltage of the oscillator circuit 13, even if the voltage falls below the minimum driving voltage of the oscillator circuit as time elapses, the boosting operation can be continued. Also, in this system, the voltage of the capacitor 41 can be used as an oscillation starting voltage of the oscillator circuit 13. That is, the voltage is applied to the Vdd input terminal of the oscillator circuit 13 via the control circuit 40 to start oscillation. Once the oscillator circuit 13 operates to start boosting, the boosted voltage becomes the power supply for the oscillator circuit 13 similar to the above-described operation. The control circuit 40 that receives the boosted voltage Vpp distributes power into driving circuit 42 of the electronic apparatus and the capacitor 41 based upon a value of the boosted voltage Vpp. In the case where the boosted voltage Vpp is just equal to a voltage necessary for driving the driving circuit 42 of the electronic apparatus, the control



circuit 40 supplies the power boosted by the booster circuit 12 to the driving circuit 42 of the electronic apparatus. If the boosted voltage  $V_{pp}$  is sufficient for driving the driving circuit 42 of the electronic apparatus, the control circuit 40 supplies the boosted power to both the driving circuit 42 of the electronic apparatus and the capacitor 41. In the case where the boosted voltage  $V_{pp}$  is such a voltage that cannot drive the driving circuit 42 of the electronic apparatus, the control circuit 40 supplies power from the capacitor 41 to the driving circuit 42 of the electronic apparatus. By this operation, even if the boosted voltage drops and cannot drive the driving circuit 42 of the electronic apparatus, operation can be performed by the power from the capacitor 41. Therefore, the driving circuit 42 of the electronic apparatus can continuously be driven.

By employing the structure as described above, since the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the driving circuit 42 of the electronic apparatus according to a value of the voltage boosted by the booster circuit 12. Accordingly, it is possible for the driving circuit 42 of the electronic apparatus to operate immediately if the boosted voltage  $V_{pp}$  is equal to or higher than a voltage by which the driving circuit 42 can be driven. Therefore, there is obtained such an effect that the power supplied by the generator or the power supply can efficiently be consumed.

#### Embodiment 5

According to the embodiment 5 of the present invention, the generator or the power supply 11 is comprised of thermoelectric conversion devices 71. As shown in a top view and side view of the thermoelectric conversion devices 71 of FIG. 5, P-type thermoelectric material elements 52 and N-type thermoelectric material elements 53 are sandwiched between two substrates 50 and 51, and, on the substrate, P-type thermoelectric material elements 52 and N-type thermoelectric material elements 53 form a p-n junction through an electrically conductive material 54 and 55 such as metal to be connected in series with one another in a p-n-p-n manner. When the temperature difference is applied between p-n junctions, the thermoelectric conversion devices 71 generate a potential difference corresponding to the temperature difference. Therefore, when the number of p-n junctions is increased, a high voltage is generated.

Accordingly, when a temperature difference is applied between the substrate 50 and substrate 51, a potential difference is generated between electrodes 56 and 57 of the thermoelectric conversion device 71. In the present invention, power is generated with the substrate 50 as a high temperature side and with the substrate 51 as a low temperature side. FIG. 6 shows a time-sequential change of an electromotive voltage generated when a temperature difference is applied between substrates 50 and 51 of the thermoelectric conversion devices 71. As seen from the results of measurement, the voltage sharply increases immediately after the temperature difference is applied between the substrates of the thermoelectric conversion devices 71, but the voltage drops after passing a peak, and saturates at a certain value. Immediately after the temperature difference is given between the substrates, since the given temperature difference is directly applied to the thermoelectric conversion devices 71, a high voltage can be generated. As time elapses, however, heat is propagated from the substrate 50 to the substrate 51 through the P-type and N-type thermoelectric material elements 52 and 53, and the temperature difference between the substrates 50 and 51 is decreased. Accordingly, the generated voltage is also decreased. This phenomenon is an inevitable problem in using the thermoelectric conversion devices 71. For this reason, conventionally, thermoelectric material elements have to be connected in series so that the output voltage of the thermoelectric conversion devices 71 is always kept now lower than the minimum driving voltage of the driving circuit 42 of the electronic apparatus or the oscillator circuit 13 even if a saturated state. Further, since the thermoelectric conversion devices 71 generate power by a temperature difference, and are greatly influenced by the atmospheric temperature, a larger number of thermoelectric material elements are connected in series with one another. For this reason, the size of the thermoelectric conversion devices 71 is increased and the number of heat-propagating paths is also increased, which requires a larger heat radiating plate for the substrate 51. However, in the electronic apparatus 10 according to the present invention, when the output voltage of the thermoelectric conversion devices 71 changes from a non-output state (namely, the output voltage=0 V) as time elapses so that the output voltage exceeds the minimum driving voltage of the oscillator circuit, the voltage of the generator or the power supply 11 is inputted into the Vdd input terminal of the oscillator circuit 13 via a Schottky diode 20 to drive the oscillator circuit 13 and start oscillation. The oscillator circuit 13 that has started oscillation outputs the clock signal to the clock signal output terminal and inputs the signal in the clock signal input terminal of the booster circuit 12. The booster circuit 12 receives the clock signal to start boosting the output voltage of the generator or the power supply 11. The oscillator circuit 13 that has started oscillation continuously performs oscillation using the power boosted by the booster circuit 12. As this time, since the boosted voltage output terminal 14 of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13, the boosted voltage is used as the power supply of the oscillator circuit 13. The Schottky diode 20 is connected between the output terminal of the generator or the power supply 11 and the input terminal of the oscillator circuit 13. Accordingly, once the oscillator circuit 13 operates to start boosting, the oscillator circuit 13 utilizes the voltage boosted by the booster circuit 12 as the power supply. For this reason, once the output voltage of the thermoelectric conversion devices 71 exceeds the minimum driving voltage of the oscillator circuit 13, even if thermal

saturation occurs as time elapses and the voltage falls below the minimum driving voltage of the oscillator circuit, the boosting operation can be continued and the electronic apparatus 10 can continuously be driven. Therefore, if a peak value of the output voltage of the thermoelectric conversion devices 71 as shown in FIG. 6 is not lower than the minimum driving voltage of the oscillator circuit, the boosting operation is conducted to continuously drive the electronic apparatus 10 even if the output voltage of the thermoelectric conversion devices 71 is in a saturated state. The present invention enables the size of the thermoelectric conversion devices 71 to be decreased compared with conventional ones.

#### Embodiment 6

Description will be made of the case where the electronic apparatus 10 according to the embodiment 5 is employed for a wristwatch. Incidentally, this description can be applied to the case where the present embodiment is employed for the electronic apparatus 10 having another time display function.

The electronic apparatus 10 according to the embodiment 5 which is employed for the wristwatch is comprised of: a thermoelectric conversion device 71; a booster circuit 12 for boosting an output voltage of the thermoelectric conversion device 71; an oscillator circuit 13 which drives the booster circuit 12; a Schottky diode 20 for rectifying the power generated by the thermoelectric conversion device 71 and the power boosted by the booster circuit 12; a control circuit 40 for dividing the power into a watch movement 75 and a capacitor 41 or from the capacitor 41 to the watch movement 75 according to a value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the watch movement 75; and the watch movement 75 which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. Connection in the above-described structure is the same with the connection as described in the embodiment 4.

FIG. 7 is a cross-sectional view showing a case where the thermoelectric conversion devices 71 are incorporated into the wristwatch. The wristwatch is composed of: a case 70 made of a material that has a high thermal conductivity such as metal; a back cover 73; a plastic member 74 for preventing heat generated on a wrist surface from propagating to the case 70; a watch movement 75; a dial 72; a surface glass 76 covering the dial 72; and thermoelectric conversion devices 71. The circuits used in this embodiment are formed in the watch movement 75. The back cover 73 is brought into contact with a substrate 50 of the thermoelectric conversion devices 71 and the heat generated on the wrist surface is made to propagate to the substrate 50 of the thermoelectric conversion devices 71. Another substrate 51 of the thermoelectric conversion devices 71 is brought into contact with the case 70 of the wristwatch and serves as a heat radiating plate for radiating the heat to the atmosphere. The plastic member 74 is a heat insulating material for preventing the heat of the back cover 73 increased by the heat generated on the wrist surface from propagating to the case 70 of the wristwatch. When the wristwatch having the above-described structure is worn on a wrist, a temperature difference is generated between the two substrates of the thermoelectric conversion devices 71 to produce a voltage. In this case, in order to effectively generate a temperature difference between the substrates of the thermoelectric conversion devices 71, a difference is made between the heat capacities above and below the substrate. Namely, the total heat

capacity of the substrate 51 of the thermoelectric conversion devices and case 70 is made to be larger than the total heat capacity of the back cover 73 and the substrate 50 of the thermoelectric conversion devices. This prevents the heat of the substrate 50 from propagating to the substrate 51 via thermoelectric material elements and offsetting the temperature difference between the substrates to be saturated, so that the temperature difference is effectively produced between the substrates of thermoelectric conversion devices 71. Also, FIG. 8 is a perspective top view in which twelve modules that are devices each including a plurality of p-n junctions of the thermoelectric conversion devices 71 which are connected in series with one another are connected in series with one another in the wristwatch. (In this case, one of the above devices is considered as one module.) Such a connection enables gaining the output voltage of the thermoelectric conversion devices 71.

In the wristwatch according to this embodiment, twelve modules having fifty pairs of the p-n junctions of the thermoelectric conversion devices 71 are connected in series with one another, and threshold voltages of transistors in the oscillator circuit 13 and booster circuit 12 are set to 0.3 V. These values must be changed depending upon the size of the wristwatch and the endothermic/heating values.

In the thermoelectric conversion devices 71, the power generated per thermoelectric material element is about 200  $\mu\text{V}/^\circ\text{C}$ . When the watch movement 75 that drives at 1.5 V is directly driven by the thermoelectric conversion devices 71, assuming that the temperature difference between the substrates is  $2^\circ\text{C}$ ., at least 18,125 pairs of p-n junction pairs are required. However, it is difficult from the technical standpoint to contain about 2,000 pairs of devices in the wristwatch. Accordingly, the number of p-n junctions has to be decreased to thereby boost a voltage and gain 1.5 V. In this case, however, the voltage is a constant state, which is generated by the thermoelectric conversion devices 71, must exceed the minimum driving voltage of the oscillator circuit 13 that drives the booster circuit 12. To the contrary, in this embodiment, since characteristics of the thermoelectric conversion devices 71 as shown in FIG. 6 is utilized, when the generated voltage immediately after the wristwatch is worn on a wrist exceeds the minimum driving voltage of the oscillator circuit, the boosting operation is possible even if the generated voltage in a constant state (in a thermally saturated state) is lower than the minimum driving voltage of the oscillator circuit.

In this embodiment, the voltage immediately after the wristwatch is worn on the wrist is about 2 V, and a power generating ability in a constant state is about 0.5 V. Also, when the threshold voltage of the transistor is 0.3 V, the minimum driving voltage of the oscillator circuit 13 is about 0.7 V.

The principle of operation in this embodiment will be described. When the output voltage of the thermoelectric conversion devices 71 changes from a non-output state (namely, the output voltage=0 V) so that the output voltage exceeds the minimum driving voltage of the oscillator circuit after the wristwatch is worn on the wrist, the output voltage is inputted into the Vdd input terminal of the oscillator circuit 13 via the Schottky diode 20 to drive the oscillator circuit 13 and start oscillation. The oscillator circuit 13 that has started oscillation outputs a clock signal to a clock signal output terminal and inputs the signal in a clock signal input terminal of the booster circuit 12. The booster circuit 12 receives the clock signal to start boosting the output voltage of the thermoelectric conversion devices 71. At this time, since a boosted voltage output terminal 14

of the booster circuit 12 is connected to the Vdd input terminal of the oscillator circuit 13, the boosted voltage is used as the power supply of the oscillator circuit 13. The Schottky diode 20 is connected between an output terminal of the thermoelectric conversion device 71 and the input terminal of the oscillator circuit 13. Accordingly, once the oscillator circuit 13 operates to start boosting, the oscillator circuit 13 utilizes the voltage boosted by the booster circuit 12 as the power supply. For this reason, once the output voltage of the thermoelectric conversion devices 71 exceeds the minimum driving voltage of the oscillator circuit 13, even if the voltage in a constant state falls below the minimum driving voltage of the oscillator circuit, the boosting operation can be continued. Also, in this system, the voltage of the capacitor 41 can be used as an oscillation starting voltage of the oscillator circuit 13. That is, the voltage is supplied to a power terminal 22 of the oscillator circuit 13 via the control circuit 40 to start oscillation. Once the oscillator circuit 13 operates to start boosting, the boosted voltage becomes the power supply for the oscillator circuit 13 similar to the above-described operation. The control circuit 40 that receives the boosted voltage Vpp distributes power into the watch movement 75 and the capacitor 41 based upon a value of the boosted voltage Vpp. In the case where the boosted voltage Vpp is just equal to a voltage necessary for driving the watch movement 75, namely, 1.2 to 1.5 V, the control circuit 40 supplies the power boosted by the booster circuit 12 to the watch movement 75. If the boosted voltage Vpp is sufficient for driving the watch movement 75, namely, higher than 1.5 V, the control circuit 40 supplies the boosted power to both the watch movement 75 and the capacitor 41. In the case where the boosted voltage Vpp is such a voltage that cannot drive the watch movement 75, namely, lower than 1.2 V, the control circuit 40 supplies power from the capacitor 41 to the watch movement 75. By this operation, even if the boosted voltage drops and cannot drive the watch movement 75, operation can be performed by the power from the capacitor 41. Therefore, the watch movement 75 can continuously be driven.

By employing the structure as described above, since the output voltage of the thermoelectric conversion devices 71 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the thermoelectric conversion device 71 can be downsized. Downsizing of the thermoelectric conversion device 71 leads to broad application particularly to a portable watch apparatus. Also, once the output voltage of the thermoelectric conversion devices 71 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the watch movement 75 without the other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, the output voltage of the thermoelectric conversion devices 71 having a large internal resistance, in which devices are connected in series with one another, comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the watch movement 75 according to a value of the voltage boosted by

the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the thermoelectric conversion devices 71 can efficiently be consumed.

#### Embodiment 7

In the embodiment 7 according to the present invention, description will be made of a booster circuit 12 having a coil as shown in FIG. 10. So long as there is no particular description, the arrangement of an embodiment is described where a power supply has a GND terminal at the lower potential side and a Vdd terminal at the higher potential side, each circuit has a CMOS transistor made by a P-substrate N-well process and the P substrate is used as a GND terminal. Accordingly, the substrate is common to all N-channel type MOS transistors and is connected with a GND terminal. And "high" means a signal of the voltage a level of a boosted voltage Vdd and "low" means a signal of the GND level.

An electromotive force input terminal 103 for inputting a voltage of a generator or the power supply 11 is connected to one of electrodes of a boosting coil 100, and the other electrode of the boosting coil 100 is connected to the drain of an N-channel type MOS transistor 101 and to a P-type electrode of a Schottky diode 102. The source of the N-channel type MOS transistor 101 is connected to a GND terminal 118 which is an electrode at the lower potential side of the generator or the power supply 11. The gate of the N-channel type MOS transistor 101 is connected to a clock signal input terminal 105 that is connected to a clock signal output terminal of the oscillator circuit 13, and an N-type electrode of the Schottky diode 102 is connected to a boosted voltage output terminal 14. In the above-described structure, the output voltage of the generator or the power supply 11 is boosted using the clock signal from the oscillator circuit 13. In the case where the booster circuit 12 according to the present invention is manufactured by the same process with that for the oscillator circuit 13, assuming that threshold voltages of the N- and P-channel type transistors of the oscillator circuit 13 are 0.3 V, the threshold voltage of the N-channel type MOS transistor 101 in the booster circuit 12 is also 0.3 V. At this time, the minimum driving voltage of the oscillator circuit 13 is 0.7 V. In the booster circuit 12 according to the present invention, however, since the transistor, the drain of which is connected to one of the electrodes of the coil, is an N-channel type transistor, boosting operation is possible even if the voltage of the electromotive force input terminal 103 is 0.1 V. In the case where the frequency of the output clock signal of the oscillator circuit 13 is 1 to 5 kHz and a duty thereof is 67%, the voltage of the electromotive force input terminal input terminal 103 which is 0.1 V is boosted to 1.5 V.

FIG. 11 shows the oscillator circuit 13 that outputs a clock signal necessary for boosting the voltage of the coil. An output terminal of an inverter circuit 106 is connected to an input terminal of an inverter circuit 107 and a first electrode of a capacitor 114 and an input terminal of an inverter circuit 110, and an output terminal of an inverter circuit 107 is connected to an input terminal of an inverter circuit 108 and a first electrode of a capacitor 115. An output terminal of the inverter circuit 108 is connected to the input terminals of the inverter circuit 106 and 109 and a first electrode of a capacitor 116. Two-input NAND circuit 111 connects an output terminal of the inverter circuit 109 to a first input terminal of the two-input NAND circuit 111, and an output terminal of the inverter circuit 110 is connected to a second input terminal of the two-input NAND circuit 111. The output terminal of the two-input NAND circuit 111 is

connected to an input terminal of an inverter circuit 112, and an output terminal of the inverter circuit 112 is connected to an input terminal of an inverter circuit 113. An output terminal of the inverter circuit 113 is connected to a clock signal output terminal 119 for outputting a clock signal P1, and second electrodes of the capacitors 114, 115, and 116 are connected to the GND terminal 118 which is an electrode at the lower side of the generator or the power supply 11. In this case, the respective inverter circuits and a power supply of the two-input NAND circuit 111 is connected to a Vdd input terminal 117 of the oscillator circuit. The grounded terminals of the two-input NAND circuit 111 and the respective inverter circuits are connected to the GND terminal 118. By the above-described structure, the clock signal for about 67% of duty is obtained. Also, in the oscillator circuit 13 according to the present invention, assuming that threshold voltages of N-channel type transistors and P-channel type transistors in the inverter circuits are, for example, 0.3V, respectively, the minimum driving voltage of the oscillator 13 is 0.7 V.

The above-described structure enable effectively boosting a low voltage of the electromotive force input terminal 103 of the booster circuit 12. Particularly, this structure is more effective in the case where the voltage of the electromotive force input terminal 103 is lower than the threshold voltages of the MOS transistors.

#### Embodiment 8

FIG. 12 is a block diagram of a booster system of a thermoelectric conversion device according to an embodiment of the present invention. This system is composed of a thermoelectric conversion device 120, an oscillator circuit 13, an intermittent pulse generator circuit 121, a voltage detecting circuit 122, a signal storage circuit 123, a booster circuit 12, a diode 20, and smoothing capacitors 124 and 125.

The thermoelectric device 120 is a device for generating electricity based upon the principle of Seebeck effect and is composed of a plurality of devices connected in series with one another each of which is made, shown in FIG. 5, by connecting a P-type semiconductor and an N-type semiconductor with each other which are formed by introducing impurities into a material of Bi-Te system, wherein one electrode at the lower potential side is the GND terminal and is connected to the GND terminals of the oscillator circuit 13, the intermittent pulse generator circuit 121, the voltage detecting circuit 122, the signal storage circuit 123 and the booster circuit 12. The other electrode of the thermoelectric conversion device 120 is used to take out an electromotive voltage  $V_p$ , and characteristics in 500 pairs of p-n junctions are such that its internal resistance is about 2 k  $\Omega$  and its electromotive voltage is about 0.4 V at a temperature difference of 1° C.

The oscillator circuit 13 has a structure in which Vdd that is connected to an output terminal of the thermoelectric conversion device 120 via the Schottky diode 20 is connected to a Vdd input terminal of the oscillator circuit 13 and an oscillating frequency is varied according to the electromotive voltage  $V_p$  of the thermoelectric conversion device 120.

The intermittent pulse generator circuit 121 is a circuit which has its power terminal connected to Vdd and generates an intermittent pulse signal P2 based on a clock signal P1 outputted by the oscillator circuit 13.

The voltage detecting circuit 122, which has its power terminal connected to Vdd and detects the  $V_p$ , outputs a

detection signal P3 according to the  $V_p$  and intermittently operates based on an intermittent pulse signal P2 from the intermittent pulse generator circuit 121.

The signal storage circuit 123 is a circuit which has its power terminal connected to Vdd, stores a detection signal P3 at the time of operation of the voltage detecting circuit 122 until the next operation of the voltage detecting circuit 122, and outputs the stored detection signal P3 to the booster circuit 12 as a storage signal P4.

The booster circuit 12, which has its power terminal connected to Vdd and boosts the  $V_p$  to a boosted voltage Vdd higher than the  $V_p$ , generates the boosted voltage Vdd by turning on/off each MOS transistor according to a clock signal P1 to charge/discharge a capacitor, and switches over its boosting factor according to a storage signal P4.

The diode 20 is provided in order to use the electromotive voltage  $V_p$  of the thermoelectric conversion device 120 as a boosting power at the initial stage at which a boosted voltage is not stored to Vdd yet and in order to supply the  $V_p$  which is so high enough as to need no boosting operation to Vdd as it is, and in order to use boosted output voltage of boosted circuit 13 as a boosting power when electromotive voltage of the electronic conversion device 120 is low and is connected between the thermoelectric conversion device 120 and the Vdd so that the direction from the thermoelectric conversion device 120 to the Vdd is its forward direction.

Moreover, the smoothing capacitors 124 and 125 each of which has one side connected to GND terminal are provided on the output of the thermoelectric conversion device 120 and the Vdd.

Due to the above-mentioned arrangement the boosting factor of the booster circuit 13 can be switched over according to the electromotive voltage of the thermoelectric conversion device 120. Therefore, it is possible to efficiently boost the  $V_p$  to the boosted voltage Vdd, and to prevent the boosted voltage Vdd from becoming overvoltage caused by that the  $V_p$  has become too high.

Furthermore, it is possible to keep low power consumption of the voltage detecting circuit 122 by making the voltage detecting circuit 122 operate intermittently. Namely, since it is possible to keep low power required for boosting voltage, the boosting efficiency is improved.

As the diode 20, a Schottky diode which is small in voltage drop in its forward direction, or an MOS transistor which has a low (0.1 V) threshold voltage when diode-connected, or an MOS transistor which has a low (0.1 V) threshold voltage when diode-connected and whose gate and source or drain are P-typed or N-typed is recommended.

Although the present invention has been described using a thermoelectric conversion device as an example, it is a matter of course that the invention can be applied also to boost an electromotive voltage of a device which generates power by means of another external energy, or to boost a voltage of a capacitor or a capacitor element of a secondary battery or the like.

FIG. 13 is a circuit diagram of the booster circuit 13 shown in FIGS. 1, 2, 3, 4 and 12. It is composed of a first booster circuit 130, a second booster circuit 131, a third booster circuit 132, a fourth booster circuit 133, two-input NAND circuits 138, 140 and 142, inverter circuits 139, 141 and 143, P-channel type MOS transistors 152 and 153, smoothing capacitors 134, 135 and 136, and a diode 137.

First, a state of connection of the respective components is described.

An electromotive force input terminal 144 for inputting  $V_p$  which is the electromotive force of the thermoelectric

conversion device 120 is connected to an input terminal of the first booster circuit 130 and the electrode at the positive side of the diode 137.

An output terminal of the first booster circuit is connected to one electrode of the smoothing capacitor 134 the other electrode of which is connected to the GND terminal and an input terminal of the second booster circuit 131.

An output terminal of the second booster circuit 131 is connected to one electrode of the smoothing capacitor 135 the other electrode of which is connected to the GND terminal, the electrode at the negative side of the diode 137, the drain terminal of the P-channel type MOS transistor 152, and an input terminal of the third booster circuit 132.

An output terminal of the third booster circuit 132 is connected to one electrode of the smoothing capacitor 136 the other electrode of which is connected to the GND terminal, the drain terminal of the P-channel type MOS transistor 153, and an input terminal of the fourth booster circuit 133.

An output terminal of the fourth booster circuit 133 is connected to the source and N well of each of the P-channel type MOS transistors 152 and 153, and a boosted voltage output terminal 150 for outputting a boosted voltage Vdd.

A clock signal input terminal 145 for inputting a clock signal P1 from the oscillator circuit 13 is connected to one input terminal of each of two-input NAND circuits 138, 140 and 142.

A first detection signal input terminal 146 for inputting a first storage signal P41 storing a first detection signal which is one of detection signals from the voltage detecting circuit 122 is connected to the other input terminal, which is not connected to the clock signal input terminal, of the two-input NAND circuit 138.

A second detection signal input terminal 147 for inputting a second storage signal P42 storing a second detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal, which is not connected to the clock signal input terminal, of the two-input NAND circuit 140 and the gate terminal of the P-channel type MOS transistor 152.

A third detection signal input terminal 148 for inputting a third storage signal P43 storing a third detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal, which is not connected to the clock signal input terminal, of the two-input NAND circuit 142 and the gate terminal of the P-channel type MOS transistor 153.

An output terminal of the two-input NAND circuit 138 is connected to an input terminal of an inverter circuit 139 and respective second clock signal input terminals of the first booster circuit 130 and the second booster circuit 131.

An output terminal of the inverter circuit 139 is connected to the respective first clock signal input terminals of the first booster circuit 130 and the second booster circuit 131.

An output terminal of the inverter circuit 141 is connected to the first clock signal input terminal of the third booster circuit 132, and an output terminal of the inverter circuit 143 is connected to the first clock signal input terminal of the fourth booster circuit 133.

The respective power terminals of the two-input NAND circuits 138, 140, and 142, and the inverter circuits 139, 141, and 143 are connected to the Vdd input terminal 151 having the boosted voltage Vdd to be inputted, and the respective GND terminals of them are connected to a GND terminal 149 connected to the low voltage side electrode of the thermoelectric conversion device.

In case that all of the first storage signal P41, the second storage signal P42 and the third storage signal P43 are "low", since no clock signal is inputted to all of the first to the fourth booster circuits, all the booster circuits do not operate and perform no boosting operation. Although the P-channel type MOS transistors 152 and 153 are on, a leak current leaking through the both transistors from the boosted voltage output terminal 150 is only a charging current from a capacitance component dangling about the drains of both the transistors.

In case that the first storage signal P41 is "high" and the second storage signal P42 and the third storage signal P43 are "low", since a clock signal is inputted into the first booster circuit 130 and the second booster circuit 131, only the first booster circuit 130 and the second booster circuit 131 operate and the P-channel type MOS transistor 152 is turned on, and therefore the electromotive voltage Vp of the thermoelectric conversion device 120 is first boosted by a factor of about 2 by the first booster circuit 130 and further boosted by a factor of about 2 by the second booster circuit 131, and supplied through the P-channel type MOS transistor 152 to the Vdd. Namely, since the boosting factor is about 4, the Vdd becomes about 4 times higher than Vp. Although the P-channel type MOS transistor 153 is also on, a current leaking through the transistor from the boosted voltage output terminal 150 is only a charging current from a capacitance component dangling about the drain of the transistor.

In case that the first storage signal P41 and the second storage signal P42 are "high" and the third storage signal P43 is "low", since a clock signal is inputted into the first booster circuit 130 and the second booster circuit 131, the first booster circuit 130, the second booster circuit 131 and the third booster circuit 132 operate and the P-channel type MOS transistor 152 is turned off and the P-channel type MOS transistor 153 is turned on, and therefore the Vp is first boosted by a factor of about 2 by the first booster circuit 130 and then boosted by a factor of about 2 by the second booster circuit 131 and further boosted by a factor of about 2 by the third booster circuit 132, and then supplied through the P-channel type MOS transistor 153 to the booster voltage output terminal 150. Namely, since the boosting factor is about 8, the Vdd becomes about 8 times higher than Vp.

In case that the first storage signal P41, the second storage signal P42 and the third storage signal P43 are all "high", since the clock signal is inputted into all of the first to the fourth booster circuits, the P-channel type MOS transistors 152 and 153 are turned off and all of the first to fourth booster circuits operate, and therefore the Vp is first boosted by a factor of about 2 by the first booster circuit 130, and then boosted by a factor of about 2 by the second booster circuit 131 and further boosted by a factor of about 2 by the third booster circuit 132, and still further boosted by a factor of about 2 by the fourth booster circuit 133, and then outputted from the boosted voltage output terminal 150. Namely, since the boosting factor is about 16, the Vdd becomes about 16 times higher than Vp.

As described a diode 137 in detail later, the first booster circuit 130 and the second booster circuit 131 are characterized by being small in their boosting ability in case that the Vdd is low in voltage, and so the diode 137 is provided in order to improve the boosting speed at the initial stage where the Vdd voltage is low by using the third booster circuit 132 and the fourth booster circuit 133 without using the first booster circuit 130 and the second booster circuit 131.

Namely, by adopting the above-mentioned arrangement, it is possible to realize a booster circuit capable of varying

its boosting factor according to the output signals P41, P42, and P43 of the signal storage circuit 123 storing detection signals of the voltage detecting circuit 122 as described above.

FIG. 14 is a circuit diagram of the first booster circuit 130 shown in FIG. 13 according to the present invention.

First, its connection is described. An input terminal 160 to which an electromotive voltage  $V_p$  of the thermoelectric conversion device 120 is inputted is connected to the drain of an N-channel type MOS transistor 164 and the source of an N-channel type MOS transistor 165, a first clock signal input terminal 162 is connected to the gates of the N-channel type MOS transistor 165 and an N-channel type MOS transistor 166, a second clock signal input terminal 163 is connected to the gates of the N-channel type MOS transistor 164 and an N-channel type MOS transistor 167, the source of the N-channel type MOS transistor 164 is connected to the drain of the N-channel type MOS transistor 166 and a second electrode of a capacitor 168, a first electrode of the capacitor 168 is connected to the drain of the N-channel type MOS transistor 165 and the source of the N-channel type MOS transistor 167, an output terminal 161 for outputting a boosted voltage is connected to the drain of the N-channel type MOS transistor 167, and a GND input terminal 169 is connected to the source of the N-channel type MOS transistor 166.

Next, the principal of operation is described. First, when a first clock signal inputted from the first clock signal input terminal 162 is "high", a second clock signal inputted from the second clock signal input terminal 163 is "low" and the N-channel type MOS transistors 165 and 166 are turned on and the N-channel type MOS transistors 164 and 167 are turned off, and therefore since the first electrode of the capacitor 168 is supplied with a voltage supplied to the input terminal 160 through the N-channel type MOS transistor 165, the voltage of the first electrode rises to a certain voltage  $V_a$ , and since the second electrode of the capacitor is supplied with a voltage of GND through the N-channel type MOS transistor 166, it becomes "low".

Next, when the first clock signal inputted from the first clock signal input terminal 162 is "low", the second clock signal inputted from the second clock signal input terminal 163 is "high" and the N-channel type MOS transistors 165 and 166 are turned off and the N-channel type MOS transistors 164 and 167 are turned on, and therefore since the second electrode of the capacitor 168 is supplied with a voltage supplied to the input terminal 160 through the N-channel type MOS transistor 164, the second electrode rises to a certain voltage  $V_b$ . Accordingly, the first electrode of the capacitor rises to a voltage obtained by adding the  $V_a$  and the  $V_b$  to each other and since the voltage is supplied to the output terminal 161 through the N-channel type MOS transistor 167, the voltage of the output terminal 161 rises to a certain voltage  $V_c$ .

In this case, the values of  $V_a$ ,  $V_b$  and  $V_c$  are related to the maximum voltage value which can be supplied between the source and the drain when an N-channel type MOS transistor is turned on, and any low voltage can be supplied by the N-channel type MOS transistors so long as it is not higher than the maximum voltage value, but any high voltage can be supplied only up to the maximum voltage value, however high the voltage is, if it is higher than the maximum voltage value.

Namely, when a voltage supplied from the input terminal 160 is not higher than the maximum voltage value of the N-channel type MOS transistor 165,  $V_a$  becomes the same

voltage as the voltage supplied from the input terminal 160, but when the voltage supplied from the input terminal 160 is higher than the maximum voltage value of the N-channel type MOS transistor 165,  $V_a$  becomes the maximum voltage value of the N-channel type MOS transistor 165; and when a voltage supplied from the input terminal 160 is not higher than the maximum voltage value of the N-channel type MOS transistor 164,  $V_b$  becomes the same voltage as the voltage supplied from the input terminal 160, but when the voltage supplied from the input terminal 160 is higher than the maximum voltage value of the N-channel type MOS transistor 164,  $V_b$  becomes the maximum voltage value of the N-channel type MOS transistor 164; and when a value obtained by adding  $V_a$  and  $V_b$  to each other which are generated at the first electrode of the capacitor 168 is not higher than the maximum voltage value of the N-channel type MOS transistor 167,  $V_c$  becomes the same voltage value as the value obtained by adding  $V_a$  and  $V_b$  to each other, but when the thus obtained value is higher than the maximum voltage value of the N-channel type MOS transistor 167,  $V_c$  becomes the maximum voltage value of the N-channel type MOS transistor 167. The maximum voltage value of each of the above-mentioned N-channel type MOS transistors is, when each of the N-channel type MOS transistors is turned on, a voltage of "high" of a clock signal inputted to the gate of each of the N-channel type MOS transistors, namely, a value obtained by subtracting the threshold voltage from the voltage applied to each N-channel type MOS transistor.

Namely, the first booster circuit 130 has a feature that in case that a voltage to be boosted is low and each N-channel type MOS transistor can do with supplying only a voltage not higher than the maximum voltage of the N-channel type MOS transistor, it can efficiently boost the voltage and further can boost the voltage however low it is, and has a feature that in case that a voltage to be boosted is high or in case that the  $V_{dd}$  is low and any one of the respective N-channel type MOS transistors must supply a high voltage than the maximum voltage value of the N-channel type MOS transistor, its boosting efficiency becomes low and moreover in case that a voltage to be boosted is further higher or in case that the  $V_{dd}$  becomes further lower, conversely the voltage to be boosted may come to drop.

Accordingly, each of the above-mentioned N-channel type MOS transistors of the first booster circuit 130 is formed so as to suppress a leak current even when its threshold voltage is lowered by having an N-type gate, and can boost a voltage from a higher voltage even if  $V_{dd}$  is low by keeping its threshold voltage as low as possible (0.2 V or so).

Although the first booster circuit 130 turns on an MOS transistor being off at the same time when an MOS transistor being on in the first booster circuit 130 is turned off, it is possible to prevent a passing-through current and improve the boosting efficiency of the first booster circuit 130 by turning on the MOS transistor being off after turning off the MOS transistor being on.

FIG. 15 is a circuit diagram of the second booster circuit 131 shown in FIG. 13, according to the present invention.

The respective components are connected as follows. An input terminal 170 of the second booster circuit 131 which is connected to an output terminal 161 of the first booster circuit 130 is connected to the drain of an N-channel type MOS transistor 174 and the source of an N-channel type MOS transistor 175, a first clock signal input terminal 172 is connected to the gates of the N-channel type MOS

transistor 175, 176, and 177, a second clock signal input terminal 173 is connected to the gate of the N-channel type MOS transistor 174, the source of the N-channel type MOS transistor 174 is connected to the drain of the N-channel type MOS transistor 176 and a second electrode of a capacitor 178, a first electrode of the capacitor 178 is connected to the drain of the N-channel type MOS transistor 175 and the drain of the P-channel type MOS transistor 177, an output terminal 171 for outputting a boosted voltage is connected to the source grounded on the substrate of the P-channel type MOS transistor 177, and a GND terminal 179 is connected to the source of the N-channel type MOS transistor 176.

Next, the principle of operation thereof will be described. First, when a first clock signal inputted from the first clock signal input terminal 172 is "high", a second clock signal inputted from the second clock signal input terminal 173 is "low" and the N-channel type MOS transistors 175 and 176 are turned on and the N-channel type MOS transistor 174 and the P-channel type MOS transistor 177 are turned off, and therefore since the first electrode of the capacitor 178 is supplied with a voltage supplied to the input terminal 170 through the N-channel type MOS transistor 175, the voltage of the first electrode rises to a certain voltage  $V_{a1}$ , and since the second electrode of the capacitor 178 is supplied with a voltage of GND through the N-channel type MOS transistor 176, it becomes "low". Next, when the first clock signal inputted from the first clock signal input terminal 172 is "low", the second clock signal inputted from the second clock signal input terminal 173 is "high" and the N-channel type MOS transistor 175 and 176 are turned off and the N-channel type MOS transistor 174 and the P-channel type MOS transistor 177 are turned on, and therefore since the second electrode of the capacitor 178 is supplied with a voltage supplied to the input terminal 170 through the N-channel type MOS transistor 174, the voltage of the second electrode rises to a certain voltage  $V_{b1}$ . Accordingly, the first voltage of the first electrode of the capacitor 178 rises to a voltage obtained by adding the  $V_{a1}$  and the  $V_{b1}$  to each other and since the voltage is supplied to the output terminal 171 through the P-channel type MOS transistor 177, the voltage of the output terminal 171 rises to a certain voltage  $V_{c1}$ .

Herein, in the case where a voltage of the first electrode of the capacitor 178 is lower than the minimum voltage which can be supplied between the source and the drain, the P-channel type MOS transistor 177 has two operational modes. When the voltage of the first electrode of the capacitor 178 is lower than 0.6 V at which the current is fed in the forward direction from the drain of the P-channel type MOS transistor to the substrate, the voltage cannot be supplied to the output terminal 171. However, when the voltage of the first electrode of the capacitor 178 is 0.6 V or higher and is lower than the minimum voltage that can be supplied between the source and the drain, a voltage obtained by subtracting 0.6 V from the voltage of the first electrode of the capacitor 77 is supplied to the output terminal 171. On the other hand, when the voltage of the first electrode of the capacitor 178 is higher than the minimum voltage that can be supplied between the source and the drain of the P-channel type MOS transistor 177, however high the voltage of the first electrode of the capacitor 178 is, the voltage can be supplied to the output terminal 171.

Furthermore, a gate voltage of a transistor minus a threshold voltage of the transistor is a minimum voltage. In the minimum voltage, current can flow between source and drain of P-channel type MOS transistor.

Accordingly the minimum voltage of the P-channel type MOS transistor 177 of FIG. 15 is a value obtained by

subtracting the threshold voltage from a "low" voltage of the gate of the P-channel type MOS transistor 177, namely, the absolute value of the threshold voltage due to subtracting the threshold voltage value from the GND voltage.

Namely, the second booster circuit 131 has a feature that a voltage can be efficiently boosted in case that the voltage to be boosted is not higher than the maximum voltage of the N-channel type MOS transistors 174 and 175 and a boosted voltage generated at the first electrode of the capacitor 178 is not lower than the minimum voltage of the P-channel type MOS transistor 177, but has also a feature that its boosting efficiency is deteriorated or a voltage to be boosted drops in case that the voltage to be boosted is higher or in case that the  $V_{dd}$  is lower and a voltage to be boosted exceeds the maximum voltage of either one of the N-channel type MOS transistors 174 and 175, and no voltage is outputted to the output terminal 171 in case that the boosted voltage is lower than the minimum voltage of the P-channel type MOS transistor 177.

Accordingly, with regard to the respective MOS transistors of the second booster circuit 131, an N-channel type MOS transistor has an N-type gate formed therein and a P-channel type MOS transistor has a P-type gate formed therein so as to suppress a leak current even when the absolute value of its threshold voltage is lowered, and it has been possible to boost a voltage from a higher voltage even if  $V_{dd}$  is low and to boost a voltage from a lower voltage, by keeping the absolute value of its threshold voltage as low as possible (0.2 V or so).

Although the second booster circuit 131 turns on an MOS transistor being off at the same time when an MOS transistor being on in the second booster circuit 131 is turned off, it is possible to prevent a passing-through current and improve the boosting efficiency of the second booster circuit by turning on the MOS transistor being off after turning off the MOS transistor being on.

FIG. 16 is a circuit diagram of the third and fourth booster circuits. The respective components are connected as follows. An input terminal 180 of the third and the fourth booster circuits 132 and 133 which is connected to an output terminal 171 of the second booster circuit 131 or an output terminal 181 of the third booster circuit 132 is connected to the source grounded on the substrate of an P-channel type MOS transistor 184 and the drain of an P-channel type MOS transistor 185, a first clock signal input terminal 182 is connected to the gates of the P-channel type MOS transistors 184, 187, and N-channel type MOS transistor 186, a second clock signal input terminal 183 is connected to the gate of the P-channel type MOS transistor 185, the drain of the P-channel type MOS transistor 184 is connected to the drain of the N-channel type MOS transistor 186 and a second electrode of a capacitor 188, a first electrode of the capacitor 188 is connected to the source grounded on the substrate of the P-channel type MOS transistor 185 and the drain of the P-channel type MOS transistor 187, an output terminal 181 for outputting a boosted voltage is connected to the source grounded on the substrate of the P-channel type MOS transistor 187, and a GND terminal 189 is connected to the source of the N-channel type MOS transistor 186.

Next, the principle of operation thereof will be described. First, when a first clock signal inputted from the first clock signal input terminal 182 is "high", a second clock signal inputted from the second clock signal input terminal 183 is "low" and the N-channel type MOS transistor 186 and the P-channel type MOS transistor 185 are turned on and the P-channel type MOS transistors 184 and 187 are turned off.



Accordingly, since the first electrode of the capacitor 188 is supplied with a voltage supplied to the input terminal 180 through the P-channel type MOS transistor 185, the voltage of the first electrode rises to a certain voltage Va2. Since the second electrode of the capacitor 188 is supplied with a voltage of GND through the N-channel type MOS transistor 186, it becomes "low". Next, when the first clock signal inputted from the first clock signal input terminal 182 is "low", the second clock signal inputted from the second clock signal input terminal 183 is "high" and the N-channel type MOS transistor 186 and the P-channel type MOS transistor 185 are turned off and the P-channel type MOS transistors 184 and 187 are turned on, and therefore since the second electrode of the capacitor 188 is supplied with a voltage supplied to the input terminal 180 through the P-channel type MOS transistor 184, the voltage of the second electrode rises to a certain voltage Vb2. Accordingly, the voltage of the first electrode of the capacitor 188 rises to a voltage obtained by adding the Va2 and the Vb2 to each other and since the voltage is supplied to the output terminal 181 through the P-channel type MOS transistor 187, the voltage of the output terminal 181 rises to a certain voltage Vc2.

In case that a voltage is supplied to the first electrode of the capacitor 188 from the input terminal 180 when the P-channel type MOS transistor 185 is turned on, no voltage can be supplied to the capacitor 188 in case that the voltage of the input terminal 180 is lower than the minimum voltage which can be supplied by the P-channel type MOS transistor 185 and is lower than 0.6 V at which the forward direction from the P-type drain of the transistor to the substrate is turned on, and only a voltage obtained by subtracting 0.6 V from the voltage of the input terminal 180 can be supplied to the capacitor 188 in case that the input terminal 180 voltage is not lower than 0.6 V, but in case that the input terminal 180 voltage is not lower than the minimum voltage, the input terminal 180 voltage can be supplied to the capacitor 188 as it is, and in that in case that a voltage is supplied to the second electrode of the capacitor 188 from the input terminal 180 when the P-channel type MOS transistor 184 is turned on, no voltage can be supplied to the capacitor 188 in case that the voltage of the input terminal 180 is lower than the minimum voltage which can be supplied by the P-channel type MOS transistor 184, but in case that the voltage of the input terminal 180 is not lower than the minimum voltage of the transistor, the voltage of the input terminal 180 can be supplied to the capacitor as it is.

Namely, the third and fourth booster circuits have a feature that they cannot boost a voltage lower than the minimum voltage which can be supplied by the respective P-channel type MOS transistors but they can boost a voltage from a high voltage if it is not lower than the minimum voltage.

Accordingly, with regard to the respective P-channel type MOS transistors of the third booster circuit 132, each of which has a P-type gate formed therein so as to suppress a leak current even when the absolute value of its threshold voltage is lowered, and can boost a voltage from a lower voltage (0.2 V) by keeping the absolute value of its threshold voltage as low as possible (0.2 V or so).

Although each of the third and the fourth booster circuits turns on an MOS transistor being off at the same time when an MOS transistor being on in the booster circuit is turned off, it is possible to prevent a passing-through current and improve the boosting efficiency of the booster circuit by turning on the MOS transistor being off after turning the MOS transistor being on.

The booster circuit 12 of this embodiment shown in FIG. 13 has a feature that it is possible to boost a voltage in case that Vdd is not lower than 0.3 V and the Vp inputted from the electromotive force input terminal 144 is not lower than 0.05 V by composing the first to the fourth booster circuits so that the second booster circuit 131 boosts a voltage boosted by the first booster circuit 130, the third booster circuit 132 boosts a voltage boosted by the second booster circuit 131, and the fourth booster circuit 133 boosts a voltage boosted by the third booster circuit 132, and the second booster circuit 131 boosts a voltage up to a voltage which can be boosted by the third booster circuit 132 and the first booster circuit 130 boosts a voltage up to a voltage which can be boosted by the second booster circuit 131.

This embodiment has realized a thermoelectric conversion device booster system which can efficiently boost the electromotive voltage Vp of a thermoelectric conversion device 120 and further can boost the electromotive force Vp being low (0.5 V), by boosting the electromotive voltage Vp of the thermoelectric conversion device 120 by means of the booster circuit 12, as shown in FIG. 12.

Although the booster circuit of this embodiment shown in FIG. 13 is designed so that the electromotive voltage of the thermoelectric conversion device 120 having the performance is boosted up to a voltage capable of driving such an IC operating at about 1.5 V as used in a watch or the like, it is a matter of course that it is enough to perform such a design change that the booster circuit is additionally provided with a plurality of the first or the third booster circuits 130, 132 which are connected in series with one another, or a plurality of the first booster circuits 130 connected in series followed by a plurality of the third booster circuits 132 connected in series, or only a plurality of the third booster circuits 132 connected in series, in such case that a voltage to be boosted is different as a case of boosting the electromotive voltage of a thermoelectric conversion device different in performance or another power generating device or a case of boosting a voltage of such a capacitor element as a capacitor or a secondary battery, or in such case that a necessary voltage to be boosted is different as a case that a voltage necessary for an IC to be driven is different.

#### Embodiment 9

FIG. 17 is a circuit diagram of a booster circuit 12 of an embodiment according to the present invention in which another arrangement different from the booster circuit shown in FIG. 13 is adopted. It is composed of a total of 15 booster circuits of the first booster circuit 190 to the fifteenth booster circuit 195, two-input NAND circuits 206, 208 and 210, inverter circuits 205, 207 and 209, and a P-channel type MOS transistor 211.

First, a state of connection of the components is described.

An electromotive force input terminal 198 for inputting Vp which is the electromotive voltage of a thermoelectric conversion device is connected to a first input terminal of the first booster circuit 190 and a second input terminal of the first booster circuit 190 to the fifteenth booster circuit 195.

Each of output terminals of the respective booster circuits except the fifteenth booster circuit 195 is connected to the first input terminal of the booster circuit next thereto, and an output terminal of the fifteenth booster circuit 195 is connected to the drain of the P-channel type MOS transistor 211, and the source and substrates of the P-channel type MOS transistor 211 are connected to a boosted voltage output terminal 199 for outputting the boosted voltage Vdd.



A clock signal input terminal 200 for inputting a clock signal P1 from an oscillator circuit 13 is connected to one input terminal of each of the two-input NAND circuits 206, 208 and 210.

A first detection signal input terminal 201 for inputting a first storage signal P41 storing a first detection signal which is one of detection signals from a voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 210, which is not connected to the clock signal input terminal 200.

A second detection signal input terminal 202 for inputting a second storage signal P42 storing a second detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 208, which is not connected to the clock signal input terminal 200.

A third detection signal input terminal 203 for inputting a third storage signal P43 storing a third detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 206, which is not connected to the clock signal input terminal 200.

The output terminal of the two-input NAND circuit 206 is connected to the input terminal of the inverter circuit 205 and the second clock signal input terminals of the first booster circuit 190 to the eighth booster circuit 191.

The output terminal of the inverter circuit 205 is connected to the first clock signal input terminal of each of the first booster circuit 190 to the eighth booster circuit 191.

The output terminal of the two-input NAND circuit 208 is connected to the input terminal of the inverter circuit 207 and the second clock signal input terminals of the ninth booster circuit 192 to the twelfth booster circuit 193.

The output terminal of the inverter circuit 207 is connected to the first clock signal input terminal of each of the ninth booster circuit 192 to the twelfth booster circuit 193.

The output terminal of the two-input NAND circuit 210 is connected to the input terminal of the inverter circuit 209, the second clock signal input terminal of each of the thirteenth booster circuit 194 to the fifteenth booster circuit 195, and the gate of the P-channel type MOS transistor 211.

The output terminal of the inverter circuit 209 is connected to the first clock signal input terminals of the thirteenth booster circuit 194 to the fifteenth booster circuit 195.

The respective power terminals of the two-input NAND circuits 206, 208 and 210, and the inverter circuits 205, 207 and 209 are connected to a Vdd input terminal 197 to which a boosted voltage Vdd is inputted, and the respective GND terminals thereof are connected to a GND potential input terminal 204 connected to an electrode at the lower voltage side of the thermoelectric conversion device 120.

Next, its operation is described.

In case that all of the first storage signal P41, the second storage signal P42 and the third storage signal P43 are "low", since no clock signal is inputted to any of the first to the fifteenth booster circuits, any booster circuit does not operate and performs no boosting operation.

In case that the first storage signal P41 is "high" and the second storage signal P42 and the third storage signal P43 are "low", since a clock signal is inputted only to the booster circuits from the thirteenth booster circuit 194 to the fifteenth booster circuit 195, the booster circuits from the thirteenth booster circuit 194 to the fifteenth booster circuit 195 operate. Namely, the three booster circuits operate and each one of them boosts a voltage by Vp, a boosted voltage

of  $4 \times V_p$  obtained by adding  $3 \times V_p$  to the electromotive voltage Vp of the thermoelectric conversion device 120 is outputted from the output terminal of the fifteenth booster circuit 195.

In case that the first storage signal P41 and the second storage signal P42 are "high" and the third storage signal P43 is "low", since a clock signal is inputted only to the booster circuits from the ninth booster circuit 192 to the fifteenth booster circuit 195, the booster circuits from the ninth booster circuit 192 to the fifteenth booster circuit 195 operate. Namely, since the seven booster circuits operate, a boosted voltage of  $8 \times V_p$  obtained by adding  $7 \times V_p$  to the electromotive voltage Vp of the thermoelectric conversion device 120 is outputted from the output terminal of the fifteenth booster circuit 195.

In case that all of the first storage signal P41, the second storage signal P42 and the third storage signal P43 are "high", since a clock signal is inputted to all the first to the fifteenth booster circuits, all the booster circuits operate. Namely, the fifteen booster circuits operate, a boosted voltage of  $16 \times V_p$  obtained by adding  $15 \times V_p$  to the electromotive voltage Vp of the thermoelectric conversion device 120 is outputted from the output terminal of the fifteenth booster circuit 195.

Although a boosted voltage is outputted from the output terminal of the fifteenth booster circuit 195, the boosted voltage does not continue being always outputted, but is outputted only when the clock signal P1 is "high", and the electromotive voltage Vp of the thermoelectric conversion device 120 is outputted as it is from the output terminal when the clock signal is "low". Namely, in case of connecting the output terminal to the boosted voltage output terminal 199 as it is, when the clock signal P1 is "low" a boosted voltage which has been outputted with much effort results in dropping to the electromotive voltage Vp of the thermoelectric conversion device 120. Therefore, the above-mentioned problem has been solved by providing a P-channel type MOS transistor 211 and turning on the transistor when the clock signal P1 is "high" and turning it off when the clock signal P1 is "low".

As described above, by adopting an arrangement as shown in FIG. 17, a booster circuit 12 capable of varying its boosting factor according to a storage signal outputted by a signal storage circuit 123 storing a detection signal of a voltage detecting circuit 122 can be realized by another arrangement different from the booster circuit shown in FIG. 13.

FIG. 18 is a circuit diagram of the first to the third booster circuits shown in FIG. 17 in the present invention.

First, its connection state is described.

A first input terminal 222 is connected to the drain of an N-channel type MOS transistor 227, a second input terminal 221 is connected to the source of an N-channel type MOS transistor 228, a first clock signal input terminal 224 is connected to the gate of the N-channel type MOS transistor 227, a second clock signal input terminal 225 is connected to the gates of the N-channel type MOS transistors 228 and 229, the source of the N-channel type MOS transistor 227 is connected to the drain of the N-channel type MOS transistor 229 and a second electrode of a capacitor 210, a first electrode of the capacitor 210 is connected to the drain of the N-channel type MOS transistor 228 and an output terminal 223 for outputting a boosted voltage, and a GND input terminal 226 is connected to the source of the N-channel type MOS transistor 229.

Next, its operation is described.

First, when a first clock signal inputted from the first clock signal input terminal 224 is "low", a second clock signal inputted from the second clock signal input terminal 225 becomes "high" and then the N-channel type MOS transistors 228 and 229 are turned on and the N-channel type MOS transistor 227 is turned off, and therefore the voltage of the first electrode of the capacitor 210 is raised to a certain voltage Va by being supplied with the electromotive voltage Vp of the thermoelectric conversion device 120 supplied to the second input terminal 221 through the N-channel type MOS transistor 228, and the second electrode of the capacitor is made "low" by being supplied with a voltage of GND through the N-channel type MOS transistor 227.

Next, when the first clock signal inputted from the first clock signal input terminal 224 is "high", the second clock signal inputted from the second clock signal input terminal 225 becomes "low" and the N-channel type MOS transistors 228 and 229 are turned off and the N-channel type MOS transistor 227 is turned on, and so that the voltage of the second electrode of the capacitor 210 is raised to a certain voltage Vb by being supplied with a voltage supplied to the first input terminal 222 through the N-channel type MOS transistor 227. Accordingly, the voltage of the first electrode of the capacitor 210 is raised to a voltage obtained by adding the Va and the Vb to each other and outputs the voltage from the output terminal 223.

In this case, the values of Va and Vb are related to the maximum voltage value which can be supplied when an N-channel type MOS transistor is turned on, and the N-channel type MOS transistor can supply any voltage lower than the maximum voltage value however low it is, but it can supply any voltage only up to the maximum voltage value however high it is, if it is higher than the maximum voltage value.

Namely, when a voltage supplied from the second input terminal 221 is not higher than the maximum voltage value of the N-channel type MOS transistor 228, Va becomes the same voltage as the voltage supplied from the second input terminal 221, but when a voltage supplied from the second input terminal 221 is higher than the maximum voltage value of the N-channel type MOS transistor 228, Va becomes the maximum voltage value of the N-channel type MOS transistor 228; and when a voltage supplied from the first input terminal 222 is not higher than the maximum voltage value of the N-channel type MOS transistor 227, Vb becomes the same voltage as the voltage supplied from the first input terminal 222, but when the voltage supplied from the first input terminal 222 is higher than the maximum voltage value of the N-channel type MOS transistor 227, Vb becomes the maximum voltage value of the N-channel type MOS transistor 227.

The maximum voltage value of each of the above-mentioned respective N-channel type MOS transistors is a voltage of "high" of a clock signal inputted to the gate of each of the respective N-channel type MOS transistors when the N-channel type MOS transistor is on, namely, a value obtained by subtracting the threshold voltage of each N-channel type MOS transistor from Vdd.

Namely, the booster circuit shown in FIG. 18 has a feature that in case that a voltage to be boosted is low and each N-channel type MOS transistor can do with supplying only a voltage not higher than the maximum voltage of the N-channel type MOS transistor, it can efficiently boost a voltage and further can boost any low voltage however low it is, but has a feature that in case that a voltage to be boosted is high or in case that the Vdd is low and any one of the

respective N-channel type MOS transistors of the booster circuit must supply a higher voltage than the maximum voltage value of the N-channel type MOS transistor, its boosting efficiency becomes low. Further, in case that a voltage to be boosted is further higher or in case that the Vdd becomes further lower, conversely the boosted voltage may come to drop.

Accordingly, each of the above-mentioned N-channel type MOS transistors of the booster circuit shown in FIG. 18 has an N-type gate formed therein so as to suppress a leak current even when its threshold voltage is lowered, and can boost a voltage from a higher voltage even if Vdd is low, by keeping its threshold voltage as low as possible (0.2 V or so).

Although the booster circuit shown in FIG. 18 turns on an MOS transistor being off at the same time when an MOS transistor being on in the booster circuit is turned off, it is possible to prevent a passing-through current and improve the boosting efficiency of the booster circuit by turning on the MOS transistor being off after the MOS transistor being on has been turned off.

FIG. 19 is a circuit diagram of the fourth to fifteenth booster circuits shown in FIG. 17. Its arrangement is nearly the same as the booster circuit shown in FIG. 18, but is different from the booster circuit shown in FIG. 18 only in that the N-channel type MOS transistor 227 in the booster circuit of FIG. 18 is replaced with a P-channel type MOS transistor 247 in which the source and substrate are connected to a first input terminal 242, the drain is connected to a second electrode of the capacitor 250, and the gate is connected to a second clock signal input terminal 245.

Its operation is also nearly the same as the booster circuit shown in FIG. 18, but is different from that of the booster circuit in FIG. 18 in a relation between a voltage of the first input terminal 242 and a voltage Vb when the P-channel type MOS transistor 247 is turned on and the voltage Vb inputted to the first input terminal 242 is supplied to the second electrode of the capacitor 250 through the P-channel type MOS transistor 247, namely, in that no voltage can be supplied to the second electrode in case that the voltage of the first input terminal 242 is lower than the minimum voltage which can be supplied by the P-channel type MOS transistor 247, but the voltage of the first input terminal 242 can be supplied as it is in case that the voltage is not lower than the minimum voltage of the transistor.

The minimum voltage which the P-channel type MOS transistor 247 can supply is the minimum voltage which the P-channel type MOS transistor can supply through a channel from the drain of the transistor to the source or from the source to the drain, and is a value obtained by subtracting the threshold voltage of the transistor from a gate voltage of the transistor, and accordingly the minimum voltage of the P-channel type MOS transistor 247 is a value obtained by subtracting the threshold value from a "low" voltage of the gate of the P-channel type MOS transistor 247, namely, the absolute value of the threshold voltage because the threshold value having a negative value is subtracting from the GND voltage.

Namely, the booster circuit shown in FIG. 19 has a feature that a voltage can be efficiently boosted in case that a voltage inputted to the second input terminal 241 is not higher than the maximum voltage of the N-channel type MOS transistor 248 and a voltage inputted to the first input terminal 242 is not lower than the minimum voltage of the P-channel type MOS transistor 247. However, the above booster circuit has a feature that its boosting efficiency is deteriorated or a voltage to be boosted comes to be conversely dropped in

case that the voltage of the second input terminal 241 is not lower than the maximum voltage of the N-channel type MOS transistor 248, or no boosting operation cannot be performed in case that the voltage of the first input terminal 242 is lower than the minimum voltage of the P-channel type MOS transistor 247.

Accordingly, in the present invention, with regard to the respective MOS transistors of the booster circuit shown in FIG. 19, an N-channel type MOS transistor has an N-type gate formed therein and a P-channel type MOS transistor has a P-type gate formed therein, and thereby a leak current can be suppressed even when the absolute value of its threshold voltage is lowered, and by keeping the absolute value of its threshold voltage as low as possible (0.2 V or so) a voltage can be boosted from a higher voltage even if Vdd is low and further can be boosted from a lower voltage.

Although the booster circuit shown in FIG. 19 turns on an MOS transistor being off at the same time when an MOS transistor being on in the booster circuit is turned off, it is possible to prevent a passing-through current and improve the boosting efficiency of the booster circuit by turning on the MOS transistor being off after the MOS transistor being on has been turned off.

The booster circuit 12 of this embodiment shown in FIG. 17 has the first to third booster circuits having such a feature as described above arranged at the fore stage and has the fourth to fifteenth booster circuits having such a feature as described above arranged at the latter stage, and makes the first to third booster circuits perform a boosting operation from a low voltage, which is a weak point of the fourth to fifteenth booster circuits, and makes the fourth to fifteenth booster circuits perform a boosting operation from a high voltage, which is a weak point of the first to third booster circuits. Thus, the booster circuit 12 has been able to have a feature of making it possible to perform a boosting operation in case that Vdd is not lower than 0.3 V and the electromotive voltage Vp of a thermoelectric conversion device is not lower than 0.05 V.

As shown in FIG. 12, this embodiment has realized a thermoelectric conversion device booster system which can efficiently boost the electromotive voltage Vp of a thermoelectric conversion device 120 and further can boost even the electromotive force Vp being as low as 0.05 V, by boosting the electromotive voltage Vp of the thermoelectric conversion device 120 by means of the booster circuit 12 shown in FIG. 17.

Although the booster circuit of this embodiment shown in FIG. 17 is designed so that the electromotive voltage of a thermoelectric conversion device 120 having the above-described performance is boosted to a voltage capable of driving such an IC operating at about 1.5 V as an IC used in a watch or the like, it is a matter of course that it is enough to perform such a design change as increasing or decreasing the number of the booster circuits arranged at the fore stage shown in FIG. 18 or the number of the booster circuits arranged at the latter stage shown in FIG. 19, in such a case that a voltage to be boosted is different as a case of boosting an electromotive voltage of a thermoelectric conversion device different in performance or another power generating device or a case of boosting a voltage of such a capacitor element as a capacitor or a secondary battery, or in such case that a necessary voltage to be boosted is different as a case that a voltage necessary for an IC to be driven is different.

#### Embodiment 10

FIG. 20 shows the booster circuit 12 according to this embodiment of the present invention, which has a structure different from that of the booster circuit as shown in FIG. 13 or FIG. 17.

First, a state of connection of the components is described.

An electromotive force input terminal 268 for inputting Vp which is the electromotive voltage of a thermoelectric conversion device 120 is connected to an input terminal of a first booster circuit 260, the drain of an N-channel type MOS transistor 274 and the drain of an N-channel type MOS transistor 276.

Each of output terminals of the respective booster circuits except the eighth booster circuit 265 is connected to an input terminal of the booster circuit next thereto, and an output terminal of the eighth booster circuit 265 is connected to a boosted voltage output terminal 269.

A clock signal input terminal 270 for inputting a clock signal P1 from an oscillator circuit 12 is connected to one input terminal of each of two-input NAND circuits 286, 288 and 290, the input terminal of the inverter circuit 293, and the gates of the N-channel type MOS transistors 275 and 276.

A first detection signal input terminal 271 for inputting a first storage signal P41 storing a first detection signal which is one of detection signals from a voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 927, which is not connected to the clock signal input terminal 270, and the gates of the N-channel type MOS transistors 278 and 279.

A second detection signal input terminal 272 for inputting a second storage signal P42 storing a second detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 288, which is not connected to the clock signal input terminal 270, the gates of the N-channel type MOS transistors 280 and 281, and the gate of a P-channel type MOS transistor 284.

A third detection signal input terminal 273 for inputting a third storage signal P43 storing a third detection signal which is one of the detection signals from the voltage detecting circuit 122 is connected to the other input terminal of the two-input NAND 290, which is not connected to the clock signal input terminal 270, the gates of the N-channel type MOS transistors 282 and 283, and the gate of a P-channel type MOS transistor 285.

The output terminal of the two-input NAND circuit 286 is connected to the input terminal of the inverter circuit 287 and the second clock signal input terminals of the first booster circuit 260 and the second booster circuit 261.

The output terminal of the inverter circuit 287 is connected to the first clock signal input terminals of the first booster circuit 260 and the second booster circuit 261.

The output terminal of the two-input NAND circuit 288 is connected to the input terminal of the inverter circuit 289 and the second clock signal input terminals of the third booster circuit 262 and the fourth booster circuit 263.

The output terminal of the inverter circuit 289 is connected to the first clock signal input terminals of the third booster circuit 262 and the fourth booster circuit 263.

The output terminal of the two-input NAND circuit 290 is connected to the input terminal of the inverter circuit 291 and the second clock signal input terminals of the fifth booster circuit 264 to the eighth booster circuit 265.

The output terminal of the inverter circuit 291 is connected to the first clock signal input terminals of the fifth booster circuit 264 to the eighth booster circuit 265.

The output terminal of the inverter circuit 293 is connected to the gates of the N-channel type MOS transistors 274 and 277.

The source of the N-channel type MOS transistor 274 is connected to the drains of the N-channel type MOS transistors 275, 278, 280 and 282, and the source of the N-channel type MOS transistor 276 is connected to the drains of the N-channel type MOS transistors 277, 279, 281 and 283, and the source of the N-channel type MOS transistors 275 and 277 are connected to GND terminals.

The source of the N-channel type MOS transistor 278 is connected to the third clock signal input terminals of the first booster circuit 260 and the second booster circuit 261, and the source of the N-channel type MOS transistor 279 is connected to the fourth clock signal input terminal of the first booster circuit 260.

The source of the N-channel type MOS transistor 280 is connected to the third clock signal input terminals of the third booster circuit 262 and the fourth booster circuit 263, and the source of the N-channel type MOS transistor 281 is connected to the fourth clock signal input terminals of the third booster circuit 262 and the second booster circuit 261.

The source of the N-channel type MOS transistor 282 is connected to the third clock signal input terminals of the fifth booster circuit 264 to the eighth booster circuit 265, and the source of the N-channel type MOS transistor 283 is connected to the fourth clock signal input terminals of the fourth booster circuit 263 and the eighth booster circuit 265.

The sources and substrates of the P-channel type MOS transistors 284 and 285 are connected to the boosted voltage output terminal 269.

The power terminals of the two-input NAND circuits 286, 288 and 290, the inverter circuits 287, 289, 291 and 293 are connected to a Vdd input terminal 267 to which a boosted voltage Vdd is inputted, and the GND terminals thereof are connected to a GND potential input terminal 292 connected to an electrode at the lower voltage side of the thermoelectric conversion device 120.

Next, its operation is described. In case that all of the first storage signal P41, the second storage signal P42 and the third storage signal P43 are "low", since no clock signal is inputted to any of the first to eighth booster circuits 260 to 265 shown in FIG. 20, any booster circuit does not operate and performs no boosting operation. Although the P-channel type MOS transistors 284 and 285 are on, a current leaking through both the transistors from the boosted voltage output terminal 269 is only a charging current of a capacitance component dangling about the drains of both the transistors.

In case that the first storage signal P41 is "high" and the second storage signal P42 and the third storage signal P43 are "low", since clock signals are inputted to the respective clock signal input terminals of the first booster circuit 260 and clock signals are inputted to the other clock signal input terminals than the fourth clock signal input terminal of the second booster circuit 261, a voltage is boosted by Vp in the first booster circuit 260 and is boosted by Vp in the second booster circuit 261, and since the P-channel type MOS transistor 284 is turned on, a voltage of 4×Vp obtained by adding 3×Vp to Vp is supplied through the P-channel type MOS transistor 284 to the boosted voltage output terminal 269. Namely, the boosted voltage becomes 4 Vp. Although the P-channel type MOS transistor 285 is also turned on, a current leaking through the P-channel type MOS transistor 285 from the boosted voltage output terminal 269 is only a charging current of a capacitance component dangling about the drains of both the transistors.

In case that the first storage signal P41 and the second storage signal P42 are "high" and the third storage signal P43 is "low", since clock signals are inputted to the respec-

tive clock signal input terminals of the first booster circuit 260, the second booster circuit 261 and the third booster circuit 262 and clock signals are inputted to the other clock signal input terminals of the fourth booster circuit 263 than the fourth clock signal input terminal, a voltage is boosted by 2×Vp in each of the first booster circuit 260 to the third booster circuit 262 and is boosted by 4×Vp in the fourth booster circuit 263, and the P-channel type MOS transistor 284 is turned off and the P-channel type MOS transistor 285 is turned on, a voltage of 8 Vp obtained by adding 7 Vp to Vp is supplied through the P-channel type MOS transistors 285 to the boosted voltage output terminal 269. Namely, the boosted voltage Vdd becomes 8×Vp.

In case that all of the first storage signal P41, the second storage signal P42 and the third storage signal P43 are "high", since the clock signals are inputted to clock signal input terminals of all of the first to eighth booster circuits 260 to 265 shown in FIG. 20, a voltage is boosted by 2×Vp in each of the first to seventh booster circuits and is boosted by Vp in the eighth booster circuit 265, and so a voltage of 16×Vp obtained by adding 15 Vp to Vp is supplied to the boosted voltage output terminal 269. Namely, the boosted voltage Vdd becomes 16 Vp.

Although it has been described that a portion boosted in each booster circuit is 2×Vp or Vp, such a value can be obtained in case that Vp is not higher than the maximum voltage value of the N-channel type MOS transistors 274, 276, 278, 279, 280, 281, 282 and 283, namely, in case that the wave height value of a clock signal inputted to the third or fourth clock signal input terminal of each booster circuit is Vp. In case that Vp is higher than the maximum voltage value, the wave height value of a clock signal inputted to the third or fourth clock signal input terminal of each booster circuit becomes the maximum voltage value and a boosted portion in each booster circuit becomes two times the maximum voltage value or becomes the maximum voltage value. Namely, the boosted voltage results in dropping.

Therefore, in the booster circuit of this embodiment shown in FIG. 20, each of the N-channel type MOS transistors 274, 276, 278, 279, 280, 281, 282 and 283 has an N-type gate formed therein so as to suppress a leak current even if its threshold voltage is lowered and keeps its threshold voltage as low as possible (0.2 V or so), and thereby makes it possible to have a boosted portion of 2×Vp or Vp in each booster circuit even if the Vp is high to some degree.

As described above, by forming a booster circuit into the arrangement as shown in FIG. 20, the booster circuit 12 capable of varying its boosting factor according to a storage signal outputted by a signal storage circuit 123 storing a detection signal of a voltage detecting circuit 122 can be realized by another arrangement different from the booster circuit shown in FIG. 13 or 17.

FIG. 21 is a circuit diagram of the first and second booster circuits shown in FIG. 20 of the present invention.

First, its connection is described.

An input terminal 300 is connected to the drain of an N-channel type MOS transistor 306, the gate of the N-channel type MOS transistor 306 is connected to a first clock signal input terminal 302, the source of the transistor is connected to a first electrode of a capacitor 308 and the drain of an N-channel type MOS transistor 307, a second electrode of the capacitor 308 is connected to a third clock signal input terminal 304, the gate of the N-channel type MOS transistor 307 is connected to a second clock signal input terminal 303, the source of the transistor is connected

to a first electrode of a capacitor 309 and an output terminal 301, and a second electrode of the capacitor 309 is connected to a fourth clock signal input terminal 305.

Next, its operation is described. It is assumed that the higher voltage of the third and the fourth clock signal is  $V_h$  and the lower voltage is "low".

First, a case of inputting a clock signal to the fourth clock signal input terminal 305 is described.

A boosted voltage is outputted from the output terminal 301 by successively supplying electric charges from the input terminal 300 to the output terminal 301 as repeating alternately a first state and a second state as follows. The first state is such that a clock signal of the first clock signal input terminal 302 is "high", a clock signal of the second clock signal input terminal 303 is "low", a clock signal of the third clock signal input terminal 106 is "low", a clock signal of the fourth clock signal input terminal 305 is  $V_h$ , and the N-channel type MOS transistor 306 is turned on and the N-channel type MOS transistor 307 is turned off, and an electric charge is supplied from the input terminal 300 through the N-channel type MOS transistor 306 to the first electrode of the capacitor 308 by lowering the voltage of the first electrode of the capacitor 308 by  $V_h$  from its previous state and boosting the voltage of the first electrode of the capacitor 309 by  $V_h$  from its previous state and at the same time a boosted voltage is outputted from the first electrode of the capacitor 309 to the output terminal 301. The second state is such that a clock signal of the first clock signal input terminal 302 is "low", a clock signal of the second clock signal input terminal 303 is "high", a clock signal of the third clock signal input terminal 106 is  $V_h$ , a clock signal of the fourth clock signal input terminal 305 is "low", and the N-channel type MOS transistor 306 is turned off and the N-channel type MOS transistor 307 is turned on, and an electric charge is supplied from the first electrode of the capacitor 308 through the N-channel type MOS transistor 307 to the first electrode of the capacitor 309 by boosting the voltage of the first electrode of the capacitor 308 by  $V_h$  from its previous state and lowering that of the first electrode of the capacitor 309 by  $V_h$  from its previous state.

When the respective N-channel type MOS transistors are turned on, in case that electric charges have been able to be supplied from the drain to the source until a voltage difference between the drain and the source of each of the N-channel type MOS transistors is eliminated, a boosted voltage of the first electrode of the capacitor 308 becomes a value obtained by adding  $V_h$  to the voltage of an input terminal 300 and a boosted voltage of the first electrode of the capacitor 309 becomes a value obtained by adding  $V_h$  to the boosted voltage of the capacitor 308, and so a boosted voltage to be outputted from this output terminal 301 becomes a value obtained by adding 2  $V_h$  to the voltage of the input terminal 300. However, when the N-channel type MOS transistors 306 and 307 are turned on, in case that the source voltage of either one of the transistors has reached the maximum voltage value of the transistor, the boosted voltage to be outputted from this output terminal 301 becomes a lower value compared with a case where the source voltage does not reach the maximum voltage value, and it may become a voltage not higher than the voltage of the input terminal 300, namely, a lowered voltage according to circumstances.

Namely, the booster circuit 12 has a feature that a voltage can be efficiently boosted and furthermore can be boosted however low it is in case that a voltage to be boosted is low or in case that  $V_{dd}$  is high, as described above, and the

maximum voltage of each of the N-channel type MOS transistors is high and each of the transistors can do with supplying only a voltage not higher than the maximum voltage value, but has a feature that its boosting efficiency becomes low in case that a voltage to be boosted is high or in case that  $V_{dd}$  is low, as described above, and the maximum voltage of each of the N-channel type MOS transistors is low and any one of the transistors must supply a voltage higher than the maximum voltage value of the N-channel type MOS transistor, and a voltage to be boosted may result in conversely dropping in case that the voltage to be boosted is higher or the  $V_{dd}$  becomes further lower.

Accordingly, each of the above-mentioned N-channel type MOS transistors shown in FIG. 21 has an N-type gate formed therein so as to suppress a leak current even when its threshold voltage is lowered, and can boost a voltage from a higher voltage even if  $V_{dd}$  is low by keeping its threshold voltage as low as possible (0.2 V or so).

Next, a case where no clock signal is inputted to the fourth clock signal input terminal 305 is described.

This case is different from a case where a clock signal is inputted to the fourth clock signal input terminal 304 only in that the capacitor 309 is a smoothing capacitor and does not contribute to its boosting operation. Namely, a boosted voltage to be outputted to the output terminal 301 drops by the  $V_h$ , and so becomes a value obtained by adding the  $V_h$  to the voltage of the input terminal 300.

FIG. 22 is a circuit diagram of each of the third to seventh booster circuits shown in FIG. 20.

Its arrangement is nearly the same as the booster circuit shown in FIG. 21, and is different from the booster circuit only in that the N-channel type MOS transistor 306 in the booster circuit of FIG. 21 is replaced, as shown in FIG. 22, with a P-channel type MOS transistor 317 in which the drain is connected to an input terminal 311, the source and substrate are connected to a first electrode of a capacitor 319, and the gate is connected to a second clock signal input terminal, and the N-channel type MOS transistor 307 in the booster circuit of FIG. 21 is replaced, as shown in FIG. 22, with a P-channel type MOS transistor 318 in which the drain is connected to a first electrode of the capacitor 319, the source and substrate are connected to a first electrode of a capacitor 320, and the gate is connected to a first clock signal input terminal 313.

Its operation is also the same as the booster circuits 260 and 261 shown in FIG. 21 in the timing when the respective MOS transistors are turned on/off and in the timing when the level of a clock signal inputted to the second electrode of each capacitor becomes  $V_h$  or "low", and is different from the booster circuits of FIG. 21 in a voltage condition for efficiently boosting a voltage. Namely, while the booster circuits shown in FIG. 21 can efficiently boost a voltage in case that a voltage supplied by each N-channel type MOS transistor is not higher than the maximum voltage value of the transistor since each MOS transistor is formed out of an N-channel type MOS transistor, the booster circuit shown in FIG. 22 can efficiently boost a voltage in case that a voltage supplied by each P-channel type MOS transistor is not lower than the minimum voltage value of the transistor since each MOS transistor is formed out of a P-channel type MOS transistor.

Namely, the booster circuit shown in FIG. 22 has a feature that a voltage can be efficiently boosted and further can be boosted however high it is in case that the voltage to be boosted is high and each P-channel type MOS transistor supplies a voltage not lower than the minimum voltage value

of the transistor, but has a feature that its boosting efficiency becomes low or no voltage may be outputted from the output terminal 312 according to circumstances in case that the voltage to be boosted is low and any one of the N-channel type MOS transistors is to supply a voltage lower than the minimum voltage value of the transistor.

Accordingly, each of the P-channel type MOS transistors of the booster circuit shown in FIG. 22 has a P-type gate formed therein and thereby a leak current can be suppressed even when the absolute value of its threshold voltage is lowered, and a voltage can be boosted from a lower voltage by keeping the absolute value of its threshold voltage as low as possible (0.2 V or so).

FIG. 23 is a circuit diagram of the eighth booster circuit 265 shown in FIG. 20 in the present invention. Its arrangement is nearly the same as the booster circuit 310 shown in FIG. 22, and is different from the booster circuit 310 only in that it does not have a capacitor 320 corresponding to the capacitor of the booster circuit 310 shown in FIG. 22. As shown in FIG. 23, therefore, nothing is connected to a fourth clock signal input terminal 335 thereof.

Its operation is also nearly the same as the booster circuit 310 shown in FIG. 22, and is different from the booster circuit 310 in that since there is not the capacitor 320 shown in FIG. 22, a voltage to be outputted from an output terminal 331 drops lower by  $V_h$  than the boosted voltage outputted to the output terminal 312 of the booster circuit 310 of FIG. 22.

The booster circuit 266 of the embodiment shown in FIG. 20 has been able to have a feature capable of performing a boosting operation in case that  $V_{dd}$  is not lower than 0.3 V and the electromotive voltage  $V_p$  of a thermoelectric conversion device is not lower than 0.05 V, by forming each of the first booster circuit 260 and the second booster circuit 261 at the fore stage into the booster circuit shown in FIG. 21, forming each of the third to seventh booster circuits 265 at the latter stage into the booster circuit shown in FIG. 22 as described above, and forming the eighth booster circuit at the last stage into the booster circuit shown in FIG. 23 as described above, and by making the first and second booster circuits 260 and 261 perform a boosting operation from a low voltage, which is a weak point of the third to eighth booster circuits, and making the third to eighth booster circuits perform a boosting operation from a high voltage, which is a weak point of the first and second booster circuits.

As shown in FIG. 12, the embodiment has realized a thermoelectric conversion device booster system which can efficiently boost an electromotive voltage  $V_p$  of a thermoelectric conversion device 120 and further can boost even the electromotive force  $V_p$  being as low as 0.05 V by boosting the electromotive voltage  $V_p$  of the thermoelectric conversion device 120 by means of the booster circuit 266 shown in FIG. 20.

Although the booster circuit of the embodiment shown in FIG. 20 is designed so that the electromotive voltage of a thermoelectric conversion device having the above-described performance is boosted to a voltage capable of driving such an IC operating at about 1.5 V as used in a watch or the like, it is a matter of course that it is enough to perform such a design change as increasing or decreasing the number of the booster circuits arranged at the fore stage shown in FIG. 21, or the number of the booster circuits arranged at the latter stage shown in FIG. 22, in such a case that a voltage to be boosted is different as a case of boosting an electromotive voltage of a thermoelectric conversion device different in performance or another power generating device or a case of boosting a voltage of such a capacitor

element as a capacitor or a secondary battery, or in such case that a necessary voltage to be boosted is different as a case that a voltage necessary for an IC to be driven is different.

Moreover, it is a matter of course that a booster circuit having an aimed performance can be realized also by combining the features of the respective booster circuits shown in FIGS. 13, 17 and 20 as described above.

#### Embodiment 11

The oscillator circuit 13 according to this embodiment of the present invention will be described.

FIG. 24 shows an oscillator circuit diagram. An output terminal of an inverter circuit 343 is connected to an input terminal of an inverter circuit 344 and a first electrode of a capacitor 348, an output terminal of the inverter circuit 344 is connected to an input terminal of an inverter circuit 345 and a first electrode of a capacitor 349, an output terminal of the inverter circuit 345 is connected to input terminals of the inverter circuit 343 and 346 and a first electrode of a capacitor 350. An output terminal of the inverter circuit 346 is connected to an input terminal of the inverter circuit 347, and the output terminal of the inverter circuit 347 is connected to a clock signal output terminal 342 for outputting a clock signal P1. Second electrodes of capacitors 348, 349, and 350 are connected to a GND terminal 341 that is an electrode at the lower potential side of the generator or the power supply 11. Herein, the power supply of each inverter circuit is connected to a  $V_{dd}$  input terminal 340, and the grounded terminal of each inverter circuit is connected to the GND terminal 341. By employing the above-described structure, the clock signal for about 50% of duty is obtained. Also, in the oscillator circuit 13 according to the present invention, assuming that threshold voltages of N-channel type transistors and P-channel type transistors in the inverter circuits are 0.3 V, respectively, the minimum driving voltage of the oscillator circuit 13 is 0.7 V.

FIG. 25 shows a diagram of the oscillator circuit 13 according to this embodiment, which has a structure different from that of the oscillator circuit as shown in FIG. 24.

First, a state of connection thereof is described.

An electromotive voltage input terminal 360 for inputting the electromotive voltage  $V_p$  of a thermoelectric conversion device 120 is connected to the gate of an N-channel type MOS transistor 364 of a depletion type (normally-on type) and a  $V_{dd}$  input terminal 362 into which a boosted voltage  $V_{dd}$  is inputted, is connected to the drain of an N-channel type MOS transistor 364 and the sources and substrates of P-channel type MOS transistors 376 and 377.

The source of the depletion-type N-channel type MOS transistor 364 is connected to the sources and substrates of P-channel type MOS transistors 368, 370 and 372, and the source and substrate of a P-channel type MOS transistor 374 of an inverter circuit 366.

The drain of the P-channel type MOS transistor 368 is connected to the drain of an N-channel type MOS transistor 369, a first electrode of a capacitor 380 and the gates of the P-channel type MOS transistor 370 and an N-channel type MOS transistor 371.

The drain of the P-channel type MOS transistor 370 is connected to the drain of the N-channel type MOS transistor 371, a first electrode of a capacitor 381 and the gates of the P-channel type MOS transistor 372 and the N-channel type MOS transistor 373.

The drain of the P-channel type MOS transistor 372 is connected to the drain of the N-channel type MOS transistor

373, the gates of the P-channel type MOS transistor 368 and the N-channel type MOS transistor 369, the gates of the P-channel type MOS transistor 374 and the N-channel type MOS transistor 375, and the gate of the N-channel type MOS transistor 379.

The drain of the P-channel type MOS transistor 374 is connected to the drain of the N-channel type MOS transistor 375 and the gate of the N-channel type MOS transistor 378.

The drain of the P-channel type MOS transistor 376 is connected to the gate of the P-channel type MOS transistor 377 and the drain of the N-channel type MOS transistor 378.

The drain of the P-channel type MOS transistor 377 is connected to the gate of the P-channel type MOS transistor 376, the drain of the N-channel type MOS transistor 379 and a clock signal output terminal 361 for outputting a clock signal P1.

The sources of the N-channel type MOS transistors 369, 371, 373, 375, 378 and 379, and the second electrodes of the capacitors 380 and 381 are connected to a GND terminal.

The section 365 enclosed by a dotted line shows a ring oscillator circuit, the section 366 enclosed by a dotted line shows an inverter circuit, and the section 367 enclosed by a dotted line shows a level shift circuit.

And connecting to the GND terminal means connecting to a GND potential input terminal 363 connected with an electrode at the lower potential side of the thermoelectric conversion device 120.

Next, operation of the respective components is described. The depletion-type N-channel type MOS transistor 364 regulates a voltage of Vdd inputted from the Vdd input terminal 362. The regulated voltage of the transistor becomes a voltage obtained by adding a voltage of the gate of the transistor, namely, an electromotive voltage Vp of the thermoelectric conversion device 120 to the absolute value of the threshold voltage of the transistor. Namely, the regulated voltage of the transistor rises when the electromotive voltage Vp of the thermoelectric conversion device rises, and drops when the Vp drops.

The ring oscillator circuit 365 generates a clock signal. The frequency of the clock signal rises or drops, respectively, when the power voltage of the ring oscillator 365, namely, the regulated voltage rises or drops. Therefore, while the frequency of the clock signal rises when the electromotive voltage Vp of the thermoelectric conversion device 120 rises, the frequency of the clock signal drops when the Vp drops.

The inverter circuit 366 has the clock signal inputted therein and outputs a clock signal obtained by inverting the clock signal in phase.

The level shift circuit 367 takes in a clock signal from the ring oscillator circuit 365 and a clock signal from the inverter circuit 366, and outputs a clock signal obtained by converting the wave height value of the clock signal from the inverter circuit 366 into a boosted voltage Vdd to the clock signal output terminal 361.

Namely, by adopting the arrangement shown in FIG. 25 as described above, it is possible to realize an oscillator circuit capable of varying the frequency of a clock signal to be outputted according to the electromotive voltage Vp of a thermoelectric conversion device 120.

Moreover, the oscillator circuit of this embodiment shown in FIG. 25 has a feature that a clock signal can be outputted in a state where a boosted voltage Vdd or the electromotive voltage Vp of a thermoelectric conversion device is low (0.3 V or so) by making a P-channel type MOS transistor have

a P-type gate or making an N-channel type MOS transistor have an N-type gate so as to suppress a leak current even when the absolute value of its threshold voltage with regard to the other MOS transistors than a depletion-type N-channel type MOS transistor 364 and thereby making the absolute value of the threshold voltage of each of the MOS transistors as low as possible (0.2 V or so).

#### Embodiment 12

FIG. 26 is a circuit diagram of the intermittent pulse generator circuit 121 shown in FIG. 12.

First, its connection state is described.

A clock signal input terminal 390 for inputting a clock signal P1 from an oscillator circuit 13 is connected to the input terminals of inverter circuits 394 and 396, the output terminal of the inverter circuit 394 is connected to a first electrode of a capacitor 397, whose second electrode is connected to a GND terminal, and the input terminal of an inverter circuit 395, the output terminal of the inverter circuit 395 is connected to a first input terminal of a two-input NAND circuit 398, the output terminal of the inverter circuit 396 is connected to a second input terminal of the two-input NAND circuit 398, the output terminal of the two-input NAND circuit 398 is connected to the input terminal of an inverter circuit 399, and the output terminal of the inverter circuit 399 is connected to an intermittent pulse output terminal 391 for outputting an intermittent pulse signal P2.

In the respective inverter circuits and the two-input NAND circuit, their power terminals are connected to a Vdd terminal 392 to which a boosted voltage Vdd is inputted, and their GND terminals are connected to a GND potential input terminal 393 which is connected to an electrode at the lower potential side of the thermoelectric conversion device 120.

Next, its operation is described. The clock signal P1 inputted from the clock signal input terminal 390 is inputted to the first input terminal of the two-input NAND circuit 398 through the inverter circuit 394 and the inverter circuit 395. This clock signal inputted to the first input terminal of the two-input NAND circuit 398 is delayed in phase more than the clock signal P1 by a time necessary for charging/discharging the capacitor 397.

On the other hand, a clock signal inputted to the second input terminal of the two-input NAND circuit 398 through the inverter circuit 396 is inverse in phase to the clock signal P1.

In the two-input NAND circuit 398, since the clock signals as described above are inputted to the input terminals of the two-input NAND circuit, the output terminal of the two-input NAND circuit outputs a clock signal which is "low" only for a period from the time when the second input terminal of the two-input NAND circuit has been changed from "low" to "high" to the time when the first input terminal of the two-input NAND circuit is changed from "high" to "low," namely, only for a period of time necessary for charging the capacitor 397.

The inverter circuit 399 inverts a pulse signal outputted by the two-input NAND circuit 398 in phase and outputs a clock signal obtained by the phase inversion to the intermittent pulse signal output terminal 391.

The intermittent pulse signal output terminal 391 outputs a pulse signal outputted by the inverter circuit 399 as an intermittent pulse signal P2.

It is a matter of course that a period for which the intermittent pulse signal P2 is "high" can be varied by



varying the driving capability of the inverter circuit 394 or the capacity of the capacitor 397.

Moreover, the intermittent pulse generator circuit 121 of the embodiment shown in FIG. 26 has a feature that an intermittent clock signal can be outputted even in a state where a boosted voltage Vdd is low by making a P-channel type MOS transistor have a P-type gate or making an N-channel type MOS transistor have an N-type gate so as to suppress a leak current even when the absolute value of its threshold voltage is lowered with regard to the MOS transistors forming the respective circuits and thereby making the absolute value of the threshold voltage of each of the MOS transistors as low as possible (0.2 V or so).

#### Embodiment 13

FIG. 27 is a circuit diagram of the voltage detecting circuit 122 of the embodiment shown in FIG. 12. First, its connection state is described. An electromotive voltage input terminal 400 for inputting the electromotive voltage Vp of a thermoelectric conversion device 120 is connected to a first electrode of a resistor Ra 410 and the gate of an N-channel type MOS transistor 423.

A second electrode of the resistor Ra is connected to a first electrode of a resistor Rb and the gate of an N-channel type MOS transistor 425.

A second electrode of the resistor Rb is connected to a first electrode of a resistor Rc and the gate of an N-channel type MOS transistor 427, and a second electrode of the resistor Rc is connected to the drain of an N-channel type MOS transistor 413.

An intermittent pulse signal input terminal 401 for inputting an intermittent pulse signal P2 is connected to the gate of an N-channel type MOS transistor 413 and the input terminal of an inverter circuit 414.

The output terminal of the inverter circuit 414 is connected to the gate of a P-channel type MOS transistor 415 and the gate of an N-channel type MOS transistor 416.

In an N-channel type MOS transistor 417 of a depletion type (normally-on type), the drain of the transistor is connected to the drain of the P-channel type MOS transistor 415, and the gate of the transistor is connected to the source of the transistor, the drain and gate of an N-channel type MOS transistor 418, the drain of the N-channel type MOS transistor 416, and the gates of a P-channel type MOS transistor 420 and an N-channel type MOS transistor 421.

The gate of a P-channel type MOS transistor 419 is connected to the drain of the P-channel type MOS transistor 419, the gates of P-channel type MOS transistors 422, 424 and 426, and the drain of the N-channel type MOS transistor 420.

The source of the N-channel type MOS transistor 420 is connected to the drain of the N-channel type MOS transistor 421 and the sources of N-channel type MOS transistors 423, 425 and 427.

The drain of the P-channel type MOS transistor 422 is connected to the drain of the N-channel type MOS transistor 423 and a third output terminal 402 for outputting a third detection signal P33.

The drain of the P-channel type MOS transistor 424 is connected to the drain of the N-channel type MOS transistor 425 and a second output terminal 403 for outputting a second detection signal P32.

The drain of the P-channel type MOS transistor 426 is connected to the drain of the N-channel type MOS transistor 427 and a first output terminal 404 for outputting a first detection signal P31.

A Vdd input terminal 405 for inputting a boosted voltage Vdd is connected to the sources and substrates of the P-channel type MOS transistors 415, 419, 422, 424 and 426, and the power source of the inverter circuit 414.

The sources of the N-channel type MOS transistors 413, 416, 418 and 421 are connected to a GND terminal.

With regard to the sections enclosed by dotted lines shown in FIG. 27, reference numeral 407 denotes a voltage dividing resistor section, 408 denotes a reference voltage generator circuit section, and 409 denotes a comparator circuit section.

And connecting to the GND terminal means connecting to a GND potential input terminal 406 connected with an electrode at the lower potential side of the thermoelectric conversion device 120.

Next, operation of the respective components is described. The voltage dividing resistor section 407 outputs divided voltages of the electromotive voltage Vp of the thermoelectric conversion device. The divided voltages include a first divided voltage obtained by dividing the Vp with the resistor Ra 410 and a resistor in which the resistor Rb 411 and Rc 412 are connected in series with each other, and a second divided voltage obtained by dividing the Vp with a resistor in which the resistor Ra 410 and Rb 411 are connected in series with each other and the resistor Rc 412, and the first divided voltage and the second divided voltage are outputted, respectively, from the first electrode of the resistor Rb 411 and the first electrode of the resistor Rc 412. Furthermore, an intermittent operation is performed to reduce a current consumption by controlling the voltage dividing resistor section 407 so as to output the divided voltages only for a period when the intermittent pulse signal P2 is "high" and so as to output no divided voltage by cutting the current flowing through the resistors when the intermittent pulse signal P2 is "low" by means of the N-channel type MOS transistor 413 having the intermittent pulse signal P2 inputted into its gate.

The reference voltage generator circuit section 408 outputs a reference voltage. The reference voltage is outputted from the drain of the N-channel type MOS transistor 418. Furthermore, an intermittent operation is performed to reduce a current consumption by controlling the reference voltage generator section 408 so as to output the reference voltage only for a period when the intermittent pulse signal P2 is "high" and output the GND potential instead of the reference voltage by turning off the P-channel type MOS transistor 415 to cut an electric current from the Vdd and turning on the N-channel type MOS transistor 416 for a period when the intermittent pulse signal P2 is "low", by means of the P-channel type MOS transistor 415 and the N-channel type MOS transistor 416 having the intermittent pulse signal P2 inputted into the gates thereof through the inverter circuit 414.

The comparator circuit section 409 is a comparator circuit using a comparison method of a current mirror type, and performs an operation which compares with each other the reference voltage inputted to the gate of the N-channel type MOS transistor 420 with the electromotive voltage Vp of the thermoelectric conversion device 120 inputted to the gate of the N-channel type MOS transistor 423, and outputs a detection signal in three manners as follows. In a first manner, a signal of "high" is outputted as the third detection signal P33 from the third output terminal 402 in case that the Vp is lower than the reference voltage and a signal of "low" is outputted as the signal P33 in case that the Vp is higher than the reference voltage. In a second manner, the reference



voltage is compared with the first divided voltage inputted from the voltage dividing resistor section 407 to the gate of the N-channel type MOS transistor 425, and a signal of "high" is outputted as the second detection signal P2 from the second output terminal 403 in case that the first divided voltage is lower than the reference voltage and a signal of "low" is inputted as the signal P2 in case that the first divided voltage is higher than the reference voltage. In a third manner, the reference voltage is compared with the second divided voltage inputted from the voltage dividing resistor section 407 to the gate of the N-channel type MOS transistor 427, and as the first detection signal P31 a signal of "high" is outputted from the first output terminal 404 in case that the second divided voltage is lower than the reference voltage and a signal of "low" is outputted in case that the second divided voltage is higher than the reference voltage.

Furthermore, the comparator circuit section 409 performs a detecting operation by making an electric current flow to the GND terminal when the reference voltage is outputted, namely, when the intermittent pulse signal P2 is "high", and performs no detecting operation by making no electric current flow to the GND terminal when the reference voltage is not outputted and the GND potential is outputted, namely, when the intermittent pulse signal is "low", by means of the N-channel type MOS transistor 421 having the reference voltage inputted into its gate. Namely, it reduces a current consumption by intermittently performing a detecting operation.

This embodiment has been designed so that the first divided voltage is 0.4 V when the electromotive voltage  $V_p$  of the thermoelectric conversion device 120 is 0.8 V and the second divided voltage is 0.4 V when the electromotive voltage  $V_p$  of the thermoelectric conversion device 120 is 1.6 V, and the reference voltage is 0.4 V. Namely, the third detection voltage P33 is "low" when the electromotive voltage  $V_p$  of the thermoelectric conversion device is not lower than 0.4 V and the voltage P33 is "high" when the  $V_p$  is lower than 0.4 V, and the second detection signal P2 is "low" when the  $V_p$  is not lower than 0.8 V and the signal P2 is "high" when the  $V_p$  is lower than 0.8 V, and the first detection signal P31 is "low" when the  $V_p$  is not lower than 1.6 V and the signal P31 is "high" when the  $V_p$  is lower than 1.6 V.

Moreover, the voltage detecting circuit 122 of the embodiment shown in FIG. 27 has a feature that the respective detection signals can be outputted even in a state where a boosted voltage Vdd or the electromotive voltage  $V_p$  of the thermoelectric conversion device 120 is low by making a P-channel type MOS transistor have a P-type gate formed therein or making an N-channel type MOS transistor have an N-type gate formed therein so as to suppress a leak current even when the absolute value of its threshold voltage is lowered with regard to the MOS transistors forming the respective circuits and thereby making the absolute value of the threshold voltage of each of the MOS transistors as low as possible (0.2 V or so).

Namely, by forming the voltage detecting circuit 122 of the embodiment shown in FIG. 12 into such an arrangement as shown in FIG. 27, it is possible to realize a voltage detecting circuit having a little current consumption, the circuit performing an intermittent operation based upon an intermittent pulse signal P2.

#### Embodiment 14

FIG. 28 shows a circuit diagram of the signal storage circuit 123 of the embodiment shown in FIG. 12. First, its

connection state is described. A first input terminal 430 for inputting a first detection signal P31 outputted from the voltage detecting circuit 122 is connected to a signal input terminal of a first storage circuit 439, a second input terminal 431 for inputting a second detection signal P32 outputted from the voltage detecting circuit is connected to a signal input terminal of a second storage circuit 440, and a third input terminal 432 for inputting a third detection signal P33 outputted from the voltage detecting circuit is connected to a signal input terminal of a third storage circuit 441.

An intermittent pulse signal input terminal 433 for inputting an intermittent pulse signal P2 outputted from an intermittent pulse generator circuit 121 is connected to a first intermittent pulse signal input terminal of each of a first storage circuit 439, a second storage circuit 440 and a third storage circuit 441, and the input terminal of an inverter circuit 442 is connected to a second intermittent pulse signal input terminal of each of the first storage circuit 439, the second storage circuit 440 and the third storage circuit 441.

A Vdd input terminal 437 for inputting a boosted voltage Vdd is connected to a Vdd input terminal of each of the first storage circuit 439, the second storage circuit 440 and the third storage circuit 441, and a GND potential input terminal 438 connected with an electrode at the lower potential side of the thermoelectric conversion device 120 is connected to a GND potential input terminal of each of the first storage circuit 439, the second storage circuit 440 and the third storage circuit 441.

An output terminal of the first storage circuit 439 is connected to a first output terminal 434 for outputting a first storage signal P41, an output terminal of the second storage circuit 440 is connected to a second output terminal 435 for outputting a second storage signal P42, and an output terminal of the third storage circuit 441 is connected to a third output terminal 436 for outputting a third storage signal P43.

And a power terminal of the inverter circuit 442 is connected to a Vdd input terminal 437 for inputting a boosted voltage Vdd, and a GND terminal of the inverter circuit 442 is connected to a GND potential input terminal 438 connected with an electrode at the lower potential side of the thermoelectric conversion device 120.

Next, its operation is described. First, since the first intermittent pulse signal input terminal of each of the respective storage circuits is "high" and the second intermittent pulse signal input terminal of each of the respective storage circuits is "low" for a period when the intermittent pulse signal P2 is "high", the first storage circuit 439 outputs the same signal as the first detection signal P31 to the first output terminal 434, the second storage circuit 440 outputs the same signal as the second detection signal P32 to the second output terminal 435, and the third storage circuit 441 outputs the same signal as the third detection signal P33 to the third output terminal 436.

Next, since the first intermittent pulse signal input terminal of each of the respective storage circuits is "low" and the second intermittent pulse signal input terminal of each of the respective storage circuits is "high" for a period when the intermittent pulse signal P2 is "low" after "high", the first storage circuit 439 stores the voltage of the first detection signal P31 at the time when the intermittent pulse signal P2 becomes "low" from "high" and continues outputting the voltage of the stored first detection signal P31 to the first output terminal 434, the second storage circuit 440 stores the voltage of the second detection signal P32 at the time when

the intermittent pulse signal P2 becomes "low" from "high" and continues outputting the voltage of the stored second detection signal P32 to the second output terminal 435, and the third storage circuit 441 stores the voltage of the third detection signal P33 at the time when the intermittent pulse signal P2 becomes "low" from "high" and continues outputting the voltage of the stored third detection signal P33 to the third output terminal 436.

Namely, by forming the signal storage circuit 123 shown in FIG. 12 into the arrangement shown in FIG. 28, it is possible to realize a signal storage circuit which outputs a detection signal of the voltage detecting circuit 122 as a storage signal as it is for a period when the voltage detecting circuit performing an intermittent operation is operated, namely, for a period when an intermittent pulse signal is "high", and stores a detection signal for a period when the voltage detecting circuit is operated before a period when the voltage detecting circuit is not operated, for the period, namely, for a period when the intermittent pulse signal is "low", and outputs the stored detection signal as a storage signal.

FIG. 29 shows a circuit diagram of the first storage circuit 439, the second storage circuit 440 and the third storage circuit 441 as shown in FIG. 28. First, its connection state is described. A detection signal input terminal 450 for inputting a detection signal is connected to the source of a P-channel type MOS transistor 456 and the drain of an N-channel type MOS transistor 457.

A first intermittent pulse signal input terminal 451 to which an intermittent pulse signal P2 is inputted is connected to the gate of the N-channel type MOS transistor 457 and the gate of a P-channel type MOS transistor 458.

A second intermittent pulse signal input terminal 452 to which a signal obtained by inverting in phase the intermittent pulse signal P2 is inputted is connected to the gate of the P-channel type MOS transistor 456 and the gate of an N-channel type MOS transistor 459.

The drain of the P-channel type MOS transistor 456 is connected to the source of the N-channel type MOS transistor 457, the source of the P-channel type MOS transistor 458, the source of the N-channel type MOS transistor 459, and the input terminal of an inverter circuit 460, and the output terminal of the inverter circuit 460 is connected to the input terminal of an inverter circuit 461.

The output terminal of the inverter circuit 461 is connected to the drain of the P-channel type MOS transistor 458, the source of the N-channel type MOS transistor 459, and a storage signal output terminal 453 for outputting a storage signal.

A Vdd input terminal 454 for inputting a boosted voltage Vdd is connected to the substrates of the P-channel type MOS transistors 456 and 458, and the power terminals of the inverter circuits 460 and 461, and a GND potential input terminal 455 connected with an electrode at the lower potential side of the thermoelectric conversion device is connected to the GND terminals of the inverter circuits 460 and 461.

Next, its operation is described. First, since the first intermittent pulse signal input terminal 451 is "high" and the second intermittent pulse signal input terminal 452 is "low" when the intermittent pulse signal P2 is "high", the P-channel type MOS transistor 456 and the N-channel type MOS transistor 457 are turned on, and the P-channel type MOS transistor 458 and the N-channel type MOS transistor 459 are turned off, and since a detection signal inputted from the detection signal input terminal 450 is inputted to the

input terminal of the inverter circuit 460, the detection signal is outputted from the storage signal output terminal 453 as it is.

Next, since the first intermittent pulse signal input terminal 451 becomes "low" and the second intermittent pulse signal input terminal 452 becomes "high" when the intermittent pulse signal P2 has become "low" from "high" as described above, the P-channel type MOS transistor 456 and the N-channel type MOS transistor 457 are turned off, and the P-channel type MOS transistor 458 and the N-channel type MOS transistor 459 are turned on, and a detection signal inputted from the detection signal input terminal 450 is not inputted to the input terminal of the inverter circuit 460 and the last detection signal at the time when the intermittent pulse signal is "high" is left as it has been inputted, and therefore the last detection signal at the time when the intermittent pulse signal is "high" continues being outputted from the storage signal output terminal 453.

Namely, by adopting such an arrangement as shown in FIG. 29, it is possible to realize a storage circuit which outputs a detection signal as a storage signal as it is when an intermittent pulse signal is "high", namely, when the voltage detecting circuit operates and outputs the detection signal, and stores the last detection signal at the time when the intermittent pulse signal is "high", when the intermittent pulse signal has become "low" from "high", namely, when the voltage detecting circuit has stopped and a detection signal has not been outputted, and continues outputting the stored detection signal until the next intermittent pulse signal becomes "high."

In this embodiment, as described above, by making the signal storage circuit 123 shown in FIG. 12 into the arrangement as shown in FIG. 29 by using a storage circuit formed as shown in FIG. 28, it is possible to realize a signal storage circuit which outputs a detection signal of the voltage detecting circuit 122 performing an intermittent operation shown in FIG. 12 when the voltage detecting circuit 122 is operated, and stores a detection signal before the voltage detecting circuit 122 has stopped, namely, a detection signal at the time when the voltage detecting circuit 122 is in operation when the voltage detecting circuit 122 is stopped, and outputs the stored detection signal until the voltage detecting circuit 122 operates at the next time.

Moreover, the signal storage circuit of this embodiment has a feature that a storage signal cannot be outputted even in a state where a boosted voltage Vdd or the electromotive voltage Vp of a thermoelectric conversion device is low, by making a P-channel type MOS transistor have a P-type gate or making an N-channel type MOS transistor have an N-type gate with regard to the respective MOS transistors forming the signal storage circuit so as to suppress a leak current even when the absolute value of its threshold voltage is lowered and thereby making the absolute value of the threshold voltage of each of the MOS transistors as low as possible (0.2 V or so).

#### Embodiment 15

In this embodiment of the present invention, the circuit as described in the embodiments 7, 8, 9 and 10 is used as the booster circuit 12 of the electronic apparatus 10 as shown in FIG. 2, the circuit as described in the embodiment 11 is used as the oscillator circuit 13, and the thermoelectric conversion devices 71 are used instead of the generator or the power supply 11. The voltage of the thermoelectric conversion devices 71 sharply increases immediately after the temperature difference is applied between the substrates of the

thermoelectric conversion devices 71, but the voltage drops after passing a peak, and saturates at a certain value. Immediately after the temperature difference is given between the substrates, since the given temperature difference is applied to the thermoelectric conversion devices 71, a high voltage can be generated. As time elapses, however, the heat is propagated from the substrate 50 to the substrate 51 through the P-type and N-type thermoelectric material elements 52 and 53, and the temperature difference between the substrates 50 and 51 is decreased. Accordingly, the generated voltage is also decreased. In the conventional booster circuit 92, if it is attempted to boost the voltage generated by the thermoelectric conversion devices 71, the generated voltage is low so that it is impossible to boost the voltage by the loss in the switching elements at the initial stage. By employing the booster circuit 12 according to the present invention, however, the output voltage of the thermoelectric conversion devices 71 that are saturated can be boosted. In this embodiment, although the booster circuit 12 as described in embodiments 7, 8, 9 and 10 is incorporated into the electronic apparatus as shown in FIG. 2, when the booster circuit 12 is incorporated also into the electronic apparatus 10 as shown in FIGS. 1, 3 and 4, the object of the present invention will be attained more certainly.

As described above, the electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; and the oscillator circuit 13 which drives the booster circuit 12. Therefore, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; and the oscillator circuit 13 which drives the booster circuit 12. Therefore, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Once the voltage exceeds the minimum driving voltage of the oscillator circuit, the booster circuit 12 can be driven, and therefore, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; and the oscillator circuit

13 which drives the booster circuit 12. Therefore, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, so that the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 4 starts operating, boosts the voltage, and drives the oscillator circuit 4 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; the oscillator circuit 13 which drives the booster circuit 12; and the power source 30 provided independently of the generator or the power supply 11. Therefore, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Further, since the electronic apparatus 10 according to the present invention can continue operating even if the voltage of the generator or the power supply 11 cannot exceed the minimum driving voltage of the oscillator circuit as time elapses, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; the oscillator circuit 13 which drives the booster circuit 12; and the power source 30 provided independently of the generator or the power supply 11. Therefore, the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher. Further, since the electronic apparatus 10 according to the present invention can continue operating even if the voltage of the generator or the power supply 11 cannot exceed the minimum driving voltage of the oscillator circuit as time elapses, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the power source 30 provided independently of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Further, since it

is not necessary for the power source 30 provided independently of the generator or the power supply 11 to always supply power to the oscillator circuit 13, the power source 30 can be downsized. Also, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; the oscillator circuit 13 which drives the booster circuit 12; the Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; the control circuit 40 for dividing the power into the driving circuit 42 of the electronic apparatus and the capacitor 41 or from the capacitor 41 to the driving circuit 42 of the electronic apparatus according to the value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the driving circuit 42 of the electronic apparatus; and the driving circuit 42 of the electronic apparatus which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. Therefore, since the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the driving circuit 42 of the electronic apparatus according to the value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the generator or the power supply 11 can efficiently be consumed.

The electronic apparatus according to the present invention is comprised of: the thermoelectric conversion device 71 in which P-type thermoelectric material elements 52 and N-type thermoelectric material elements 53 are sandwiched between two substrates and form the p-n junction through the electrically conductive materials 54 and 55 such as metal to be connected in series with one another; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; the oscillator circuit 13 which drives the booster circuit 12; the Schottky diode 20 for rectifying

the power generated by the generator or the power supply and the power boosted by the booster circuit 12; the control circuit 40 for dividing the power into the driving circuit 42 of the electronic apparatus and the capacitor 41 or from the capacitor 41 to the driving circuit 42 of the electronic apparatus according to the value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the driving circuit 42 of the electronic apparatus; and the driving circuit 42 of the electronic apparatus which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. Therefore, in the case where the electronic apparatus 10 is continuously driven, since the output voltage of the thermoelectric conversion device 71 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the thermoelectric conversion device 71 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the thermoelectric conversion device 71 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the driving circuit 42 of the electronic apparatus without the other power sources. Particularly, since the output voltage of the thermoelectric conversion device 71 at a time instant when a temperature difference generates is several times as large as the voltage in a constant state after time elapses, the thermoelectric conversion device 71 is suitable for the electronic apparatus 10 according to the present invention. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the driving circuit 42 of the electronic apparatus according to the value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the thermoelectric conversion device 71 can efficiently be consumed.

The electronic apparatus according to the present invention is comprised of: the generator in which the voltage of power generated changes as time elapses or the power supply 11 in which the voltage changes as time elapses; the booster circuit 12 for boosting the output voltage of the generator or the power supply 11; the oscillator circuit 13 which drives the booster circuit 12; the Schottky diode 20 for rectifying the power generated by the generator or the power supply and the power boosted by the booster circuit 12; the control circuit 40 for dividing the power into the watch movement 75 and the capacitor 41 or from the capacitor 41 to the watch movement 75 according to the value of the voltage boosted by the booster circuit 12; the capacitor 41 for accumulating the boosted power to supply the power to the watch movement 75; and the watch movement 75 including a time display function, which operates using the power boosted by the booster circuit 12 or the power accumulated in the capacitor 41. Therefore,

since the output voltage of the generator or the power supply 11 is not required to be always kept at the minimum driving voltage of the oscillator circuit or higher, the generator or the power supply 11 can be downsized. Downsizing of the generator or the power supply 11 leads to broad application to a portable apparatus. Also, once the output voltage of the generator or the power supply 11 exceeds the minimum driving voltage of the oscillator circuit, the above-mentioned oscillator circuit 13 starts operating, boosts the voltage, and drives the oscillator circuit 13 using the boosted power. Therefore, it is possible to continuously drive the watch movement 75 without the other power sources. Further, since the voltage not higher than the minimum driving voltage of the oscillator circuit, which cannot be boosted in the conventional electronic apparatus, can be boosted, there is obtained an effect that the power efficiency of the whole system can be improved. Also, when it is attempted to charge the capacitor 41 that is not charged, in the case of the generator or the power supply having a large internal resistance, the output voltage of the generator or the power supply 11 comes to drop so that a considerably long period of time is required for charging the capacitor 41. In the electronic apparatus 10 according to the present invention, however, the power after boosting operation is distributed to the capacitor 41 or the watch movement 75 according to the value of the voltage boosted by the booster circuit 12. Therefore, there is obtained such an effect that the power supplied by the generator or the power supply 11 can efficiently be consumed.

Further, according to the present invention, since P-channel type MOS transistors and N-channel type MOS transistors are suitably arranged to charge and discharge capacitors in MOS transistors and boost the voltage, boosting efficiency is high and the boosting circuit capable of boosting a low voltage can be realized.

Since the P-type gate is formed in the P-channel type MOS transistor and the N-type gate is formed in the N-channel type MOS transistor, the absolute value of the threshold voltage of each MOS transistor can also be reduced. Accordingly, the boosting circuit capable of boosting a low voltage can be realized.

Also, the oscillator circuit 13 is provided, which is capable of varying a frequency of the clock signal that is outputted according to the electromotive voltage of the power source that generates power by an external energy, for example, the thermoelectric conversion device 120. And the booster circuit 12 boosts the electromotive voltage of the thermoelectric conversion device 120 by the clock signal that the oscillator circuit 13 outputs. By employing such a structure, the booster capable of converting the electromotive voltage of the thermoelectric conversion device 120 into a boosting power without wasteful consumption can be realized.

Further, the voltage detecting circuit 122 for detecting the electromotive voltage of the thermoelectric conversion device and outputting the detection signal corresponding to the electromotive voltage is provided, and a boosting factor of the booster circuit 12 is varied by the detection signal that the voltage detecting circuit 122 outputs. Such a structure makes it possible to realize the booster system capable of converting efficiently the electromotive voltage of the thermoelectric conversion device 120 into a boosting power even if the electromotive voltage of the thermoelectric conversion device 120 is changed.

The intermittent pulse generator circuit 121 for producing the intermittent pulse from the clock signal outputted from

the oscillator circuit 13 is provided, so that the voltage detecting circuit 122 is intermittently driven by the intermittent pulse signal. Also, there is provided the signal storage circuit 123 for outputting as a storage signal the detection signal outputted from the voltage detecting circuit 122 to the boosting circuit 12 while the voltage detecting circuit 122 is operated, and for storing, while the voltage detecting circuit 122 is not operated, the last detection signal that is outputted when the voltage detecting circuit 122 is operated, and for outputting as a storage signal the stored detection signal to the booster circuit until the voltage detecting circuit 122 is operated again. And the booster circuit varies the boosting factor according to the storage signal that the signal storage circuit 123 outputs. Such a structure makes it possible to reduce the current to be consumed in the voltage detecting circuit 122 and realize the booster system having a high boosting efficiency.

What is claimed is:

1. An electronic apparatus comprising:

- a power supply for producing an output power which changes as time elapses;
- a booster circuit for boosting an output voltage of the power supply and producing a boosted output voltage;
- an oscillator circuit for generating a periodic pulse signal for driving the booster circuit; and
- a load circuit having a minimum operating voltage higher than that of the oscillator circuit;

wherein the load circuit is driven by the boosted output voltage, and the oscillator circuit is driven by the output voltage of the power supply to start oscillation and is thereafter driven by the boosted output voltage of the booster circuit.

2. An electronic apparatus according to claim 1; further comprising a diode that connects in a forward direction an output of the power supply and an input of the oscillator circuit, and inputs the output voltage of the power supply as the driving voltage of the oscillator circuit.

3. An electronic apparatus according to claim 1; further comprising a second power supply, and a diode that connects in a forward direction an output of the second power source and an input of the oscillator circuit, and inputs an output voltage of the second power source as the driving voltage of the oscillator circuit.

4. An electronic apparatus according to claim 1; further comprising a capacitor, and a control circuit for switching an output of the capacitor with the boosted output voltage of the booster circuit.

5. An electronic apparatus according to claim 1; wherein the load circuit comprises a time display unit driven by the boosted output voltage of the booster circuit.

6. An electronic apparatus according to claim 4; wherein the load circuit comprises a time display unit connected to an output of the control circuit.

7. An electronic apparatus according to any one of claims 1 to 6; wherein the power supply comprises a plurality of substrates, and a thermoelectric device comprising a plurality of pairs of P-type thermoelectric material and an N-type thermoelectric material which form a p-n junction through an electrically conductive material connected in series with one another.

8. In a miniature electronic apparatus having an electric load circuit and a boosting power supply for driving the load circuit, the boosting power supply comprising:

- a power source for producing an output power which varies with time;
- a voltage detecting circuit for detecting a voltage of the power source; and

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a booster circuit having a boosting factor which is varied based on an output of the voltage detecting circuit.

9. A miniature electronic apparatus comprising:

a power source for producing an output power which varies with time;

a voltage detecting circuit for detecting an output voltage of the power source;

a booster circuit for boosting the output voltage of the power source and producing a boosted output voltage;

a load circuit driven by the boosted output voltage; and an oscillator circuit for generating a clock signal for driving the booster circuit, the clock signal having a frequency which varies depending upon the detected output voltage of the power source.

10. An electronic apparatus according to claim 8 or 9; comprising an intermittent pulse generator circuit for intermittently generating pulses for driving the voltage detecting circuit in an intermittent manner, and a storage circuit for storing an output signal of the voltage detecting circuit until a subsequent pulse is generated by the intermittent pulse generator circuit.

11. An electronic apparatus comprising: an electronic load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the boosting circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the said electrode of the third switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, and the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the input terminal, and wherein

each of the first to fourth switching elements of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

12. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the second electrode of the

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third switching element, the second electrode of the first switching element is connected to the second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the input terminal, and wherein

each of the first to third switching elements of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal, and the fourth switching element of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the source electrode.

13. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the second electrode of the third switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the input terminal, and wherein

each of the first, third, and fourth switching elements of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and

having a substrate electrode connected to the source electrode, and the second switching element of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

14. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the said first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, and the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first switching element is off and an operation of turning on the first switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the input terminal, and wherein

each of the first to third switching elements of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

15. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, and the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first switching element is off and an operation of turning on the first switching element while the second and third switching elements are off, and out-

puts from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the input terminal, and wherein

the first switching element of the booster unit comprises a P-channel type MOS transistor in which the second electrode is a source electrode and the first electrode is a drain electrode and having a substrate electrode connected to the source electrode, and the second and third switching elements of the booster unit each comprise an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

16. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising first and second input terminals, an output terminal, a GND terminal, a capacitor, a plurality of switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the first input terminal is connected to the first electrode of a first switching element, the second electrode of the first switching element is connected to a first electrode of the capacitor and the output terminal, a second electrode of the capacitor is connected to the second input terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of inputting a voltage below a predetermined value to the second input terminal while the switching element is on and an operation of inputting a voltage above the predetermined value while the switching element is off, and outputs from the output terminal a boosted voltage obtained by boosting further positively a positive voltage inputted from the first input terminal each time a voltage above the predetermined value is inputted to the second input terminal, and wherein

the respective switching elements of the booster unit each comprise an N-channel type MOS transistor in which the first electrode is a drain electrode and the second electrode is a source electrode and having a substrate electrode connected to the GND terminal.

17. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising first and second input terminals, an output terminal, a GND terminal, a capacitor, a plurality of switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the first input terminal is connected to the first electrode of the first switching element, the second electrode of the first switching element is connected to a first electrode of the capacitor and the output terminal, a second electrode of the capacitor is connected to the second input terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of inputting a voltage below a predetermined value to the second input terminal while the switching element is on and an operation of inputting a voltage above the predetermined value while the switching element is off, and outputs from the output terminal a boosted voltage obtained by



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boosting further positively a positive voltage inputted from the first input terminal each time a voltage above the predetermined value is inputted to the second input terminal, and wherein

the respective switching elements of the booster unit each comprise a P-channel type MOS transistor in which the first electrode is a drain electrode and the second electrode is a source electrode and having a substrate electrode connected to the source electrode.

18. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the second electrode of the third switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, and the first electrode of the fourth switching element is connected to an output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the input terminal, and wherein

each of the first to fourth switching elements of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

19. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the second electrode of the third switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to

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alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the input terminal, and wherein

each of the first to third switching elements of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal, and the fourth switching element of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having the substrate electrode connected to the source electrode.

20. An electronic apparatus comprising: an electrode load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element and the second electrode of the third switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, and the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first and fourth switching elements are off and an operation of turning on the first switching element and the fourth switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the input terminal, and wherein

each of the first, third, and fourth switching elements of the booster unit comprise an N-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the source electrode, and the second switching element of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

21. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein



the input terminal is connected to the first electrode of the first switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first switching element is off and an operation of turning on the first switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the input terminal, and wherein each of the first to third switching elements of the booster unit comprises a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

22. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising an input terminal, an output terminal, a GND terminal, a capacitor, first through fourth switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the input terminal is connected to the first electrode of the first switching element, the second electrode of the first switching element is connected to a second electrode of the capacitor and the second electrode of the second switching element, the first electrode of the second switching element is connected to the GND terminal, a first electrode of the capacitor is connected to the first electrode of the third switching element and the second electrode of the fourth switching element, the first electrode of the fourth switching element is connected to the output terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of turning on the second switching element and the third switching element while the first switching element is off and an operation of turning on the first switching element while the second and third switching elements are off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the input terminal, and wherein the first switching element of the booster unit comprises an N-channel type MOS transistor in which the first electrode is a drain electrode and the second electrode is a source electrode and having a substrate electrode connected to said source electrode, and the second and third switching elements of said booster unit each comprise a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having the substrate electrode connected to the GND terminal.

23. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a

booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising first and second input terminals, an output terminal, a GND terminal, a capacitor, a plurality of switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the first input terminal is connected to the first electrode of a first switching element, the second electrode of the first switching element is connected to a first electrode of the capacitor and the output terminal, a second electrode of the capacitor is connected to the second input terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of inputting a voltage above a predetermined level to the second input terminal while the switching element is on and an operation of inputting a voltage below the predetermined level while the switching element is off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the first input terminal each time a voltage below the predetermined level is inputted to the second input terminal, and wherein

the respective switching elements of the booster unit each comprise a P-channel type MOS transistor in which the first electrode is a source electrode and the second electrode is a drain electrode and having a substrate electrode connected to the GND terminal.

24. An electronic apparatus comprising: an electric load; a power supply for producing an output voltage; and a booster circuit for boosting the output voltage, the booster circuit including a booster unit comprising first and second input terminals, an output terminal, a GND terminal, a capacitor, a plurality of switching elements each comprising a MOS transistor having a gate electrode and a first and a second electrode, wherein

the first input terminal is connected to the first electrode of a first switching element, the second electrode of the first switching element is connected to a first electrode of the capacitor and the output terminal, a second electrode of the capacitor is connected to the second input terminal, wherein

the booster unit is receptive of control signals at the gate electrodes of the respective switching elements so as to alternately repeat an operation of inputting a voltage above a predetermined value to the second input terminal while the switching element is on and an operation of inputting a voltage below the predetermined value while the switching element is off, and outputs from the output terminal a boosted voltage obtained by boosting further negatively a negative voltage inputted from the first input terminal each time a voltage below the predetermined value is inputted to the second input terminal, and wherein

the respective switching elements of the booster unit each comprise an N-channel type MOS transistor in which the first electrode is a drain electrode and the second electrode is a source electrode and having a substrate electrode connected to the source electrode.

25. An electronic apparatus comprising a booster circuit according to any one of the claims 11 to 24; wherein the booster circuit includes at least one MOS transistor as a switching element in which a gate and a channel thereof have the same conductivity type.

26. An electronic apparatus according to any one of claims 11 to 24; further comprising a thermoelectric device

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for generating a thermoelectric power in response to a temperature difference; and an oscillator circuit for generating a pulse signal for driving the booster circuit, wherein an output voltage of the booster circuit is supplied as a driving voltage of the oscillator circuit, and the output 5 voltage of the power supply which is lower than a minimum driving voltage of said oscillator circuit is boosted to the minimum driving voltage of said oscillator circuit or higher.

27. An electronic apparatus according to any one of claims 11 to 24; further comprising a time display unit 10 connected to an output of the booster circuit.

28. A method of boosting an input voltage comprising the steps of:

supplying an output voltage of a power supply to drive an oscillator;

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driving a booster circuit with a clock pulse which is generated by the oscillator in response to the output voltage of the power supply; and

supplying a boosted output voltage of the booster circuit to the oscillator, so that the oscillator is initially driven by the output voltage of the power supply to start oscillation and is thereafter driven by the boosted output voltage, whereby the output voltage of the power supply need not be maintained at a level at least as great as a minimum operating voltage of the oscillator in order to maintain operation of a device driven by the boosted voltage.

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(54) **PULSE FREQUENCY OPERATION OF  
REGULATED CHARGE PUMPS**

(75) **Inventor:** **Charles R. Thurber, Jr., Sunnyvale,  
CA (US)**

(73) **Assignee:** **MAXIM Integrated Products, Inc.,  
Sunnyvale, CA (US)**

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(58) **Field of Search** ..... **327/536, 538,  
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(56) **References Cited**

**U.S. PATENT DOCUMENTS**

6,040,736 \* 3/2000 Milanese et al. .... 327/540  
6,052,022 \* 4/2000 Lee ..... 327/536

**OTHER PUBLICATIONS**

Dual-Output Power-Supply Controller for Notebook Com-  
puters; Data Sheets for MAX786; Rev. 2; Apr. 97; Maxim  
Integrated Products.

Switched-Capacitor Voltage Doublers; Data Sheets for  
MAX1682/MAX1683; Rev. 1; Aug. 98; Maxim Integrated  
Products.

Regulated, 125mA-Output, Charge-Pump DC-DC  
Inverter; Data Sheets for MAX1673; Rev. 0; Jan. 98; Maxim  
Integrated Products.

3.3V-Input to Regulated 5V-Output Charge Pumps; Data  
Sheets for MAX682/MAX683/MAX684; Rev. 1; Aug.  
1998; Maxim Integrated Products.

\* cited by examiner

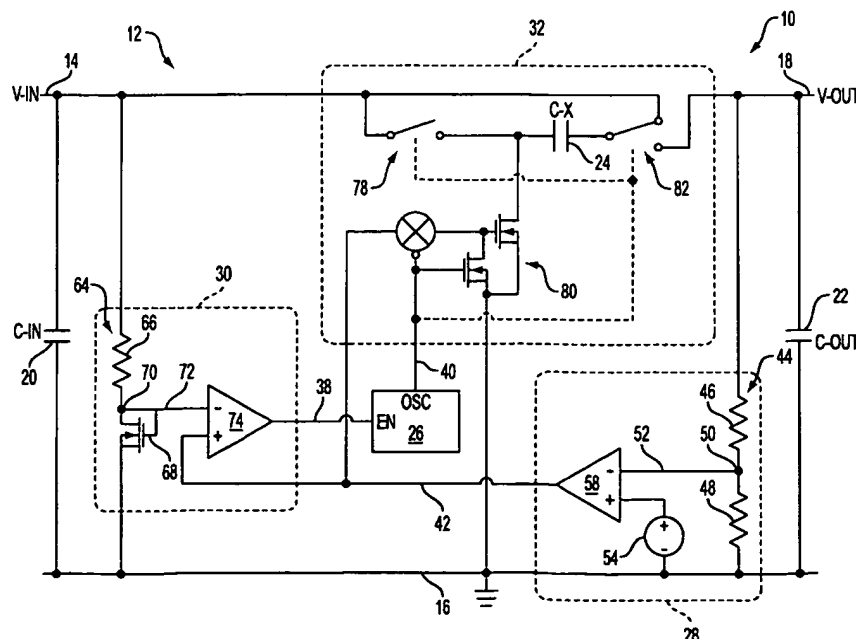
*Primary Examiner*—Jung Ho Kim

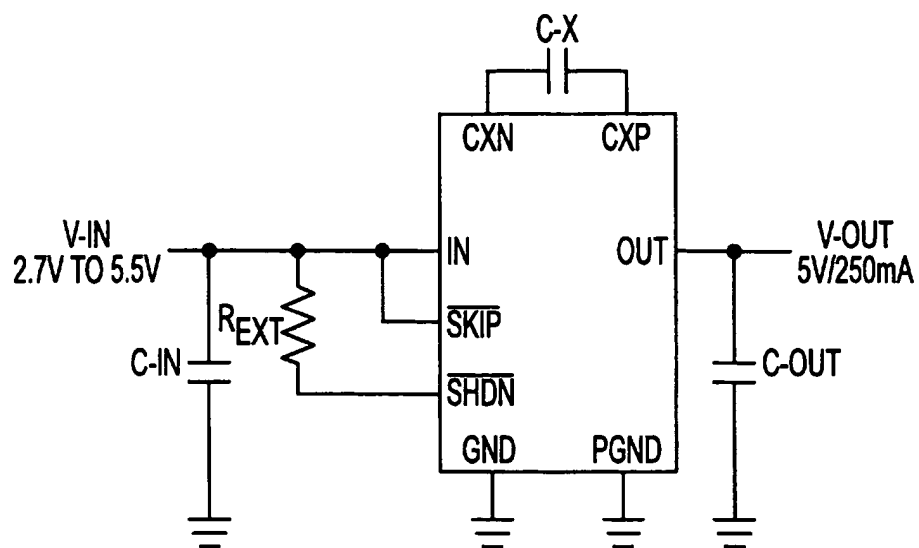
(74) *Attorney, Agent, or Firm*—Hickman Coleman &  
Hughes LLP

(57) **ABSTRACT**

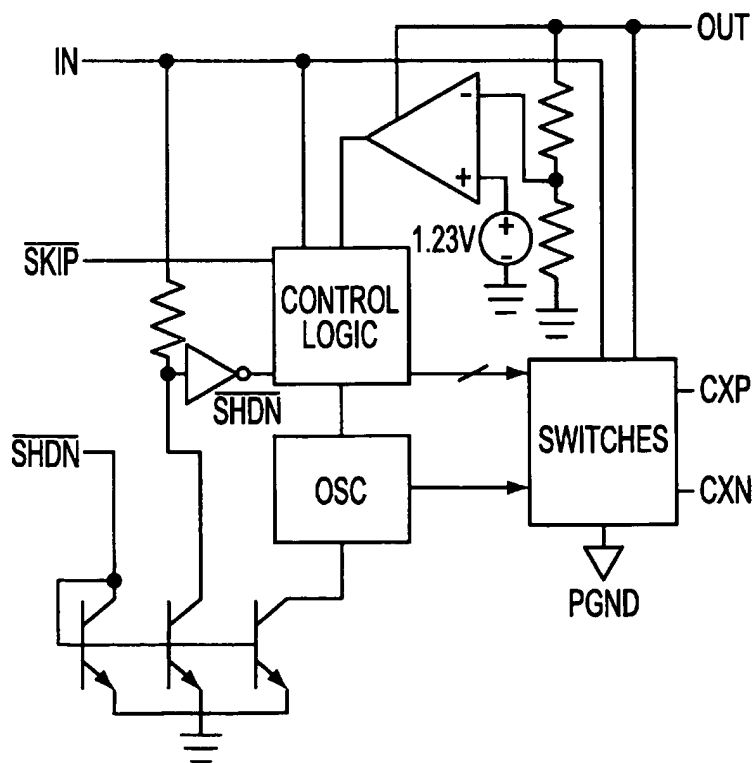
A regulating system (10) for a charge pump (12) employing  
a detection sub-circuit (28) and an enable sub-circuit (30) to  
operate an oscillator (26) and a channel-switching sub-  
circuit (32) in an automatic manner producing many of the  
advantages of previously unreconcilable skip mode and  
constant frequency mode type regulation. The detection  
sub-circuit (28) compares a feedback signal (52) from the  
output terminal (18) of the charge pump (12) to a reference  
signal (56) and produces an error signal (42) representative  
of output voltage deviation. Concurrently, the enable sub-  
circuit (30) compares a threshold signal (72) set for a  
minimum energy quanta which it is efficient for the flying  
capacitor (24) of the charge pump (12) to transfer to the error  
signal (42) and produces an enable signal (38) to enable the  
oscillator (26). An oscillator signal (40) then controls  
switching within the channel-switching sub-circuit (32) to  
set when the energy quanta are transferred and the error  
signal (42) further is used to control resistance in the charge  
path to the flying capacitor (24) to set the magnitude of the  
quanta.

**20 Claims, 5 Drawing Sheets**





**FIG. 1**  
(PRIOR ART)



**FIG. 2**  
(PRIOR ART)

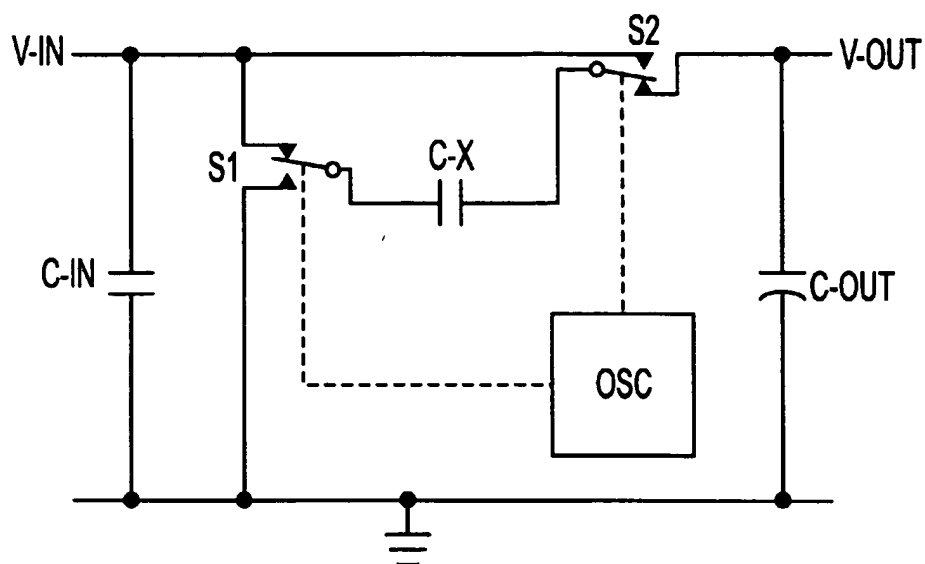


FIG. 3  
(PRIOR ART)

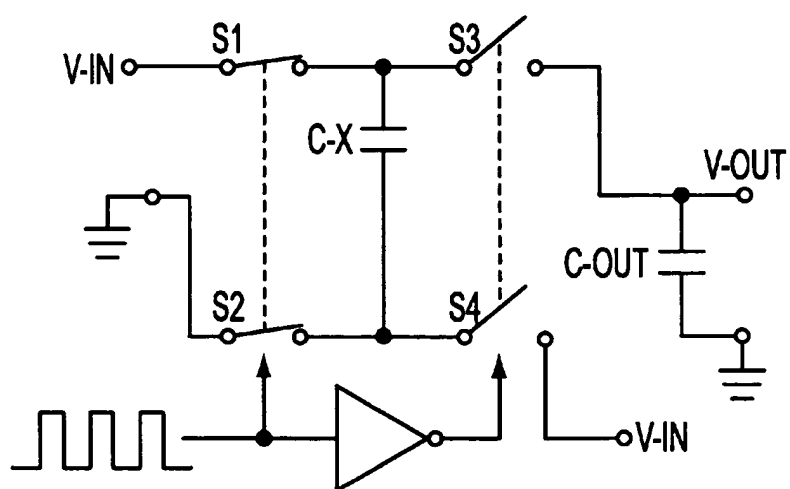


FIG. 4  
(PRIOR ART)

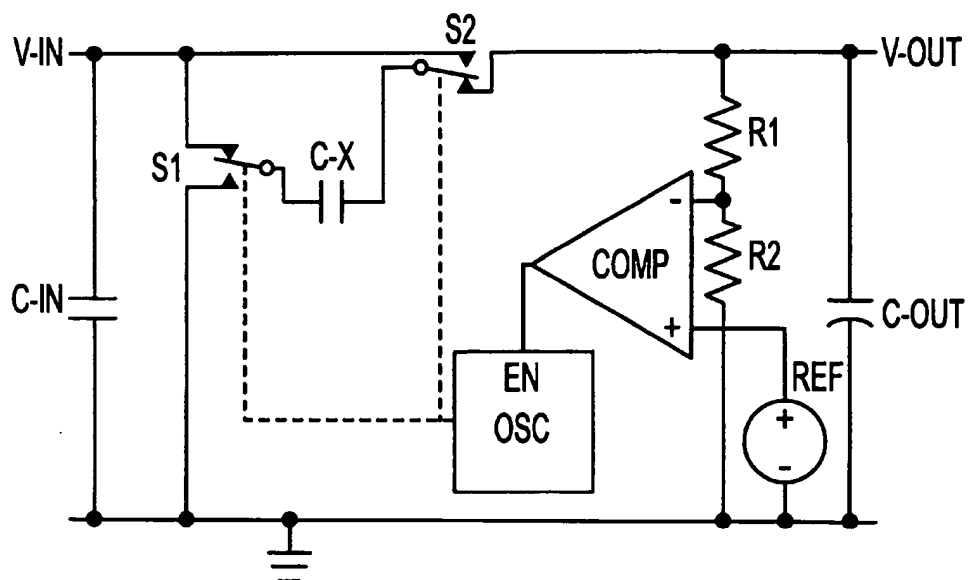


FIG. 5  
(PRIOR ART)

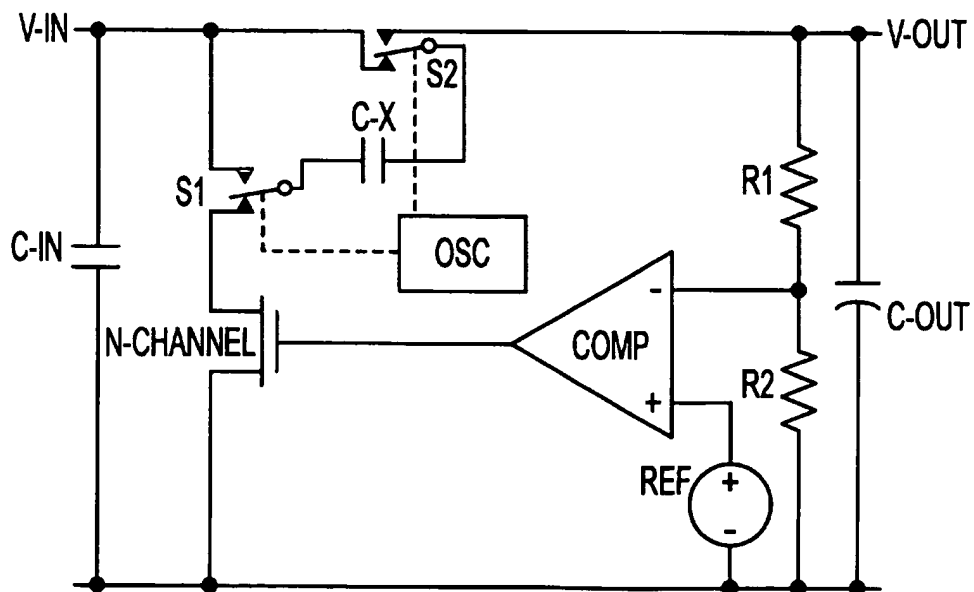


FIG. 6  
(PRIOR ART)

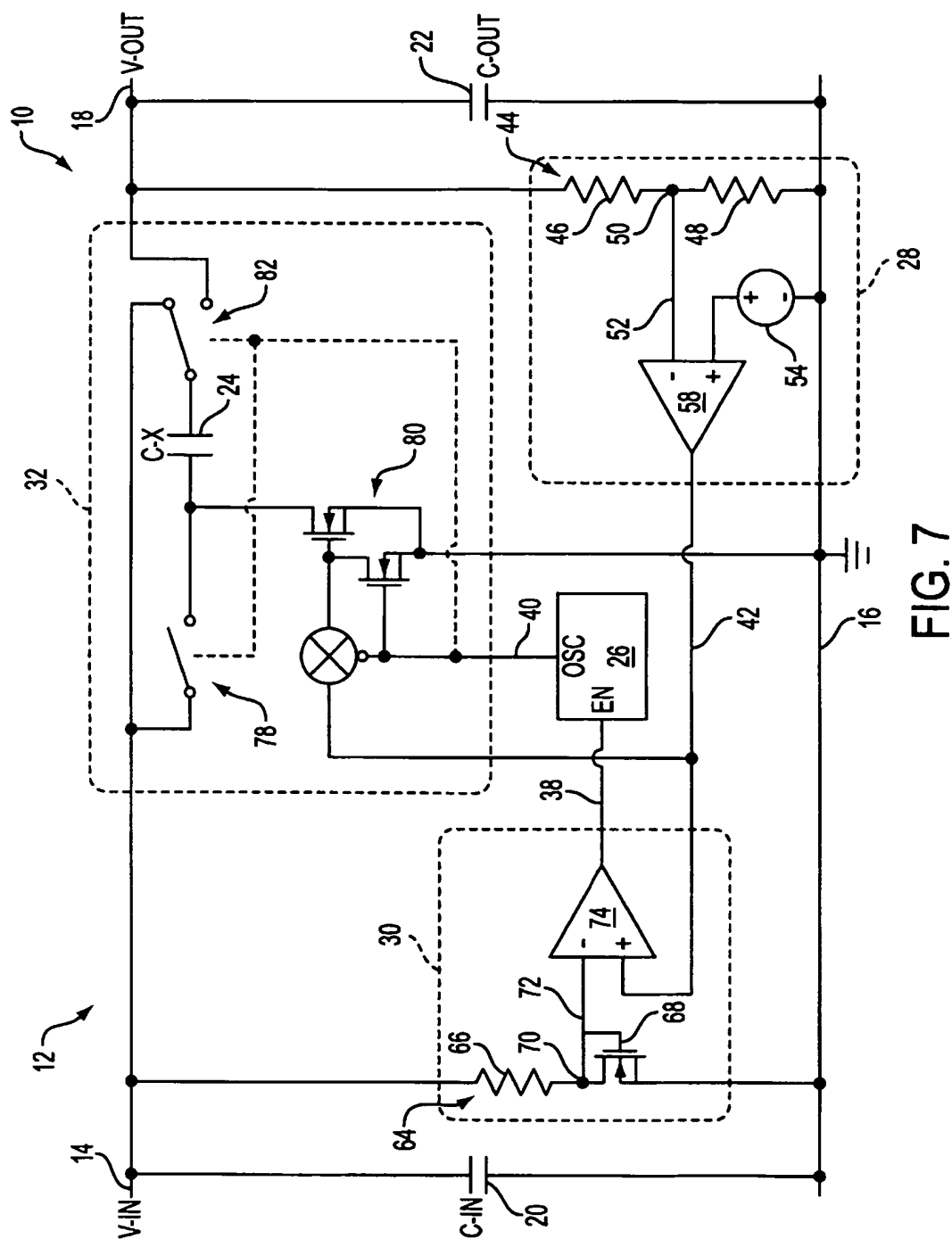


FIG. 7

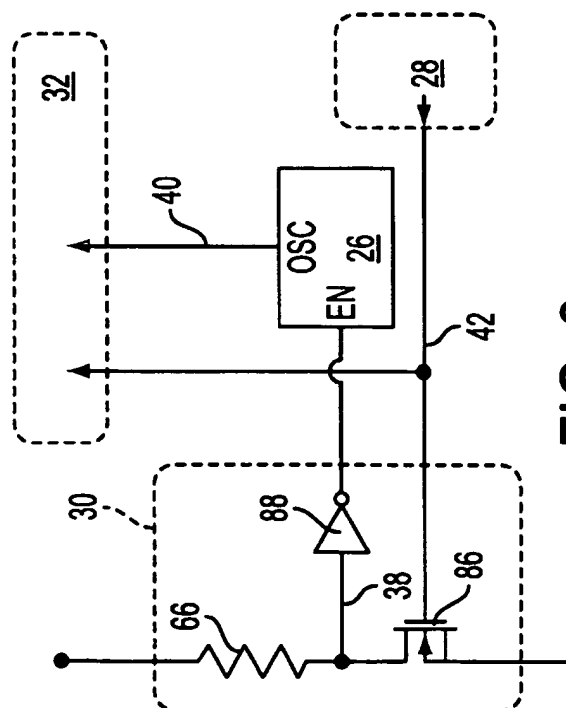


FIG. 8

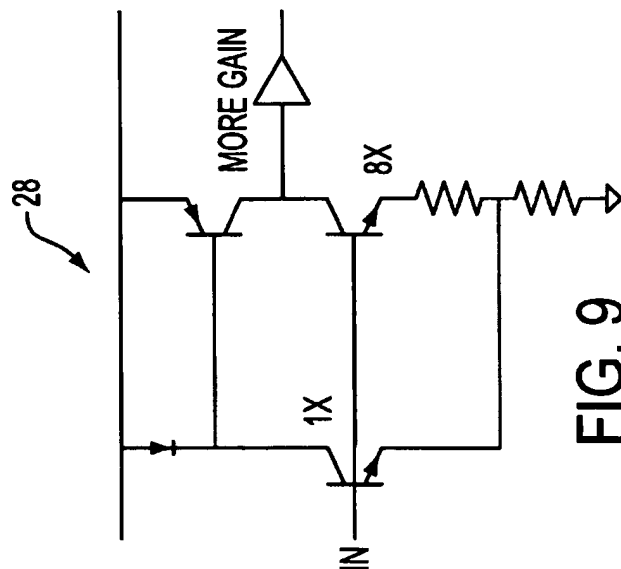


FIG. 9



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## PULSE FREQUENCY OPERATION OF REGULATED CHARGE PUMPS

### TECHNICAL FIELD

The present invention relates generally to electronic circuits for conversion of direct current power, and more particularly to systems for regulating high-efficiency charge pump circuits.

### BACKGROUND ART

Electronic circuits today often require power in one or more specific direct current (DC) voltage ranges. Supplying such, however, can pose a number of problems. If only one supply voltage is needed, it may not be of a value easily obtainable from available sources, like standard battery cells. Source-requirements mating can therefore be one problem encountered, and source voltage conversion may thus be desirable or necessary. A source also may not supply voltage which is consistently in a desired range. Batteries again provide a good example. Battery voltage varies with load, charge, temperature, etc. Such source voltage variation therefore can also be a problem, and source voltage regulation may thus also be desirable or necessary. Of course, when multiple supply voltages are needed, such power source problems increase accordingly.

For many electronic circuits it is particularly desirable to use only one power source, and to increase, decrease, or invert the voltage from it, and to also regulate the power from it for all needs. This is the case for portable electronic devices, such as cellular telephones, personal digital assistants, global position sensors etc. But even for non portable devices this is often desirable, since it permits construction of circuits which are smaller, more reliable, cheaper, etc.

Various power conversion and regulation systems currently exist. Of present interest is the charge pump. It is one of the most widely used such systems today. A charge pump is a capacitor and oscillator based circuit which converts a DC input to a DC output which is either higher, lower, or alternately both, or inverted in voltage value. Charge pumps can be regulated using a number of schemes, and they can include options, such as extreme condition detection and circuit shut-down capability, which adds to their versatility and commercial acceptance.

On initial consideration, the charge pump seems to be a perfect solution to many power conversion needs. But unfortunately that is not the case. Contrary to a somewhat popular belief, charge pumps are not particularly efficient at power conversion, and they are especially not so when used for supplying varying loads. This can severely limit their use with battery and other limited power sources where power must be used efficiently. Further, even when power availability is not a concern, the use of charge pumps can be limited because inefficiency is ultimately manifested as heat which must be dissipated. Still further, since charge pumps are inherently oscillator based systems, unacceptable "artifacts" such as output voltage ripple and electromagnetic radiation can be present from the conversion process they use. Charge pumps can be implemented using integrated circuits (ICs), but the number, size, and types of external components used may then be areas of concern. This is particularly the case for capacitors used with charge pumps, where any capacitance value and physical size reduction is usually highly desirable.

This discussion now turns to some specific charge pump examples. To avoid confusion, the following will generally

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be limited to coverage of charge pumps which increase voltage, i.e. step-up charge pumps. However, as skilled practitioners of the electronic arts should readily appreciate, these principles are easily extended to other types of charge pumps as well, such as voltage inverting and step-down types.

FIG. 1 (prior art) is a block diagram of a charge pump circuit employing an IC (specifically, the current version of part MAX682 by Maxim Integrated Products of Sunnyvale, Calif.). Input power is supplied across an input capacitor (C-IN) to appropriate terminals of the IC device. A flying capacitor (C-X) (often also called a transfer capacitor) is connected to other IC terminals (CXP and CXN) to operate in concert with the IC's internal components, discussed presently. Output power is then produced by the IC across an output capacitor (C-OUT). Other components may be present for optional features.

FIG. 2 (prior art) is a functional block diagram of the IC of FIG. 1. Of particular interest are an oscillator (OSC), switches which control power flow to the terminals (CXP and CXN) for the external flying capacitor, and control logic and sensing and tailoring elements used for signals to that control logic.

FIG. 3 (prior art) is a block diagram of an unregulated voltage doubler, i.e. a very simple charge pump. The oscillator (OSC) is free running and the charge and discharge paths to the flying capacitor (C-X) are merely switched (via S1 and S2). Actually, FIG. 3 depicts a simplistic switching scheme, and FIG. 4 depicts a more common case using four switches S1, S2, S3, and S4). The input capacitor (C-IN) and the output capacitor (C-OUT) respectfully act as input and output reservoirs, smoothing out fluctuations as conversion proceeds (e.g., ripple). Unless the output is overloaded, the output voltage (V-OUT) from the circuit in FIG. 3 is almost double the input voltage (V-IN). A voltage doubler is too inflexible for use in most applications, and most charge pumps today employ one of two common regulation schemes to permit adjustment of the output voltage to either a value at initial circuit design or to one which a user can pick by using appropriate components later. Modern IC based systems, such as that in FIG. 1, can often be configured to use either of these common regulation schemes.

FIG. 5 (prior art) is a block diagram illustrating a skip mode charge pump regulation scheme being used to increase or "step-up" the voltage. Each cycle of the oscillator (OSC) results in the output voltage (V-OUT) being increased as the charge in the flying capacitor (C-X), which can be termed a "quanta," is "stacked" onto the output capacitor (C-OUT). The flying capacitor (C-X) is chosen to have a lower capacitance than the output capacitor (C-OUT) so that the output voltage (V-OUT) is increased a small amount during each oscillator cycle. Regulation is accomplished in this scheme by enabling the oscillator with feedback from the output (V-OUT). A sample is taken from resistors (R1 and R2) forming a voltage divider across the circuit's output. This sample from the feedback is compared to the voltage from a reference (REF) with a comparator (COMP). When the output voltage (V-OUT) is determined in this manner to be below a desired value the oscillator operates the switches (S1 and S2) to charge the flying capacitor (C-X) from the input with a new quanta during a first half-cycle and to transfer that quanta to the output during the next half-cycle. When the output voltage (V-OUT) increases to the desired level the oscillator (OSC) is turned off, i.e., dis-enabled. As the output voltage drops, due to power use by the ultimate load (not shown), the oscillator is re-enabled and additional quanta are transferred.

Skip mode regulation is simple but it has some disadvantages. Voltage ripple in the output can be high, and this can be very difficult to filter out because of the varying frequency as the oscillator "skips." The values needed for the external component can also be large, and for the capacitors this particularly means that they may be more sizable and expensive than desired. For this mode of regulation the ratio for values between the flying capacitor and the output capacitor is typically about 1:20. The MAX682 component provides an example. This widely used IC can step-up a 3.3 volt input to a regulated 5.0 volt output for loads up to 250 milli amps (mA). Configured for skip mode, the output voltage ripple rating is 100 milli volts (mV) and the recommended capacitor values are: 2.2 micro farads (uF) for the input capacitor (C-IN), 1 uF for the flying capacitor (C-X), and 10 uF for a ceramic type output capacitor. In view of the large output capacitance needed, a tantalum type may be preferable, and then a 47 uF unit is recommended.

FIG. 6 (prior art) is a block diagram illustrating a constant-frequency mode charge pump regulation scheme. Here the oscillator is allowed to free run, i.e., to run at a constant frequency, and feedback from the output (V-OUT) is instead here used to control a variable resistance device (N-CHANNEL) in the charge path of the flying capacitor (C-X). Due to the resistance of this resistance device, the flying capacitor is not able to fully charge within an oscillator half-cycle, and thus the size of each quanta of power transferred is regulated. In actual practice the variable resistance device is typically combined with the switches (S1 and S2), using appropriate transistors to perform both functions.

Constant frequency mode has a number of advantages over skip mode regulation. Voltage ripple in the output is lower and, if necessary, it can be filtered out more easily because it has a fixed frequency. The external component values can also be much smaller. In constant frequency mode the ratio of the flying capacitor to the output capacitor is typically only about 1:4. Continuing with the MAX682 as an example, when this IC is configured for constant frequency mode its rated output voltage ripple is only 80 mV and the recommended capacitor values are: 1 uF for the input capacitor (C-IN), 0.47 uF for the flying capacitor (C-X), and 2.2 uF for a ceramic output capacitor.

However, even constant frequency mode also has some disadvantages. When an output load is small or non-existent the oscillator is still running, switching at a high, constant frequency and consuming a substantial quiescent current. The term "substantial" is, of course, relative. But for many applications any unnecessary use of current is a severe disadvantage. Battery powered applications suffer particularly, but even for line powered applications such energy waste is often undesirable.

Accordingly, what is needed is a new scheme for regulating charge pumps, one which optimally combines the advantages, but not the disadvantages, of existing skip mode and constant frequency mode regulation schemes.

#### DISCLOSURE OF INVENTION

Accordingly, it is an object of the present invention to provide charge pump regulation which is efficient at all appropriate loads.

Another object of the invention is to provide charge pump regulation which remains efficient as load is dynamically varied.

Another object of the invention is to provide charge pump regulation which employs components, particularly including capacitors, having small values.

And another object of the invention is to provide charge pump regulation which produces low output voltage ripple.

Briefly, one preferred embodiment of the present invention is a circuit for regulating a charge pump. The charge pump has an input, output, and common terminals and receives an input signal having an input voltage and produces an output signal having an output voltage. Included in the charge pump are an input capacitor connected across the input and common terminals, an output capacitor connected across the output and common terminals, and a flying capacitor having first and second sides. The inventive regulating system for the charge pump includes an oscillator, a detection sub-circuit, a channel-switch sub-circuit, and an enable sub-circuit. When enabled by an enable signal, the oscillator produces an oscillator signal that alternates between a first state and a second state. The detection sub-circuit produces an error signal when the output voltage is less than a desired output voltage. This error signal has a voltage representative of how much the output voltage differs from said desired output voltage. In embodiments to step up voltage, the channel-switch sub-circuit connects the first side of the flying capacitor to the common terminal when the oscillator signal is in its first state and connects to the input terminal when the oscillator signal is in its second state. The channel-switch sub-circuit further connects the second side of the flying capacitor to the input terminal when the oscillator signal is in its first state and to the output terminal when the oscillator signal is in its second state. Alternate embodiments may employ alternate connection arrangements to achieve step up voltage conversion or voltage inversion, such switching arrangements for flying capacitors being essentially conventional. The channel-switch sub-circuit further controllably sets resistance to the flying capacitor in response to the voltage in the error signal when the oscillator signal is in its first state. The enable sub-circuit produces the enable signal when the error signal has voltage differing from said desired output voltage by a preset amount, for regulating the charge pump by enabling the oscillator to operate the channel-switch sub-circuit to alternately charge the flying capacitor at a rate controlled by the resistance set by said channel-switch sub-circuit and to discharge it via the output terminal into the output capacitor of the charge pump.

An advantage of the present invention is that it provides charge pump regulation having efficiency at light loads which is comparable to that of skip mode regulation, yet also provides efficiency at heavy loads which is comparable to that of constant frequency mode regulation. Furthermore, the invention provides such regulation even while automatically, dynamically adjusting to efficiently accommodate varying load.

Another advantage of the invention is that it may be implemented with capacitors having relatively low values, which are accordingly physically smaller and cheaper, and in some cases also may be of more preferable alternate types.

And other advantages of the invention are that it provides regulation which produces low output voltage ripple and low radiation emission, thus minimizing any undesired effects of such on associated loads or proximate other circuitry.

These and other objects and advantages of the present invention will become clear to those skilled in the art in view of the description of the best presently known mode of carrying out the invention and the industrial applicability of the preferred embodiment as described herein and as illustrated in the several figures of the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

The purposes and advantages of the present invention will be apparent from the following detailed description in conjunction with the appended drawings in which:

FIG. 1 (prior art) is a block diagram of a typical regulated charge pump circuit employing an integrated circuit which is a suitable candidate for use of the invention;

FIG. 2 (prior art) is a functional block diagram of the integrated circuit of FIG. 1;

FIG. 3 (prior art) is a block diagram of an unregulated voltage doubler;

FIG. 4 (prior art) is a block diagram illustrating in more detail a flying capacitor switching scheme more typically used in implementations such as that of FIG. 3;

FIG. 5 (prior art) is a block diagram illustrating a skip mode charge pump regulation scheme;

FIG. 6 (prior art) is a block diagram illustrating a constant-frequency mode charge pump regulation scheme;

FIG. 7 is a block diagram illustrating a preferred embodiment of the present invention;

FIG. 8 is a block diagram illustrating an alternate enable sub-circuit for the embodiment of FIG. 7; and

FIG. 9 is a block diagram illustrating an alternate detection sub-circuit for the embodiment of FIG. 7.

## BEST MODE FOR CARRYING OUT THE INVENTION

A preferred embodiment of the present invention is a system for regulating a charge pump. As illustrated in the various drawings herein, and particularly in the view of FIG. 7, a form of this preferred embodiment of the invention is depicted by the general reference character 10.

FIG. 7 is a block diagram illustrating a preferred embodiment of the inventive regulating system 10 in a charge pump 12. A suitable DC input voltage (V-IN) is applied across an input terminal 14 and a common terminal 16, and a regulated output voltage (V-OUT) is produced across an output terminal 18 and the common terminal 16. For use as an input reservoir an input capacitor 20 is connected across the input terminal 14 and the common terminal 16, and for use as an output reservoir an output capacitor 22 is connected across the output terminal 18 and the common terminal 16. (The input capacitor 20 is theoretically optional, but in practice one is almost always used, and the circuit input always has some intrinsic capacitance, anyway.) For providing the distinctive capability of a charge pump, a flying capacitor 24 and an oscillator 26 are included. For controlling and particularly regulating the charge pump 12 in the manner of the invention a detection sub-circuit 28, an enable sub-circuit 30, and a switching sub-circuit 32 are also provided.

The oscillator 26 used is an enabled type, but otherwise may be essentially the same as typically used in prior art systems. The oscillator 26 requires an enable signal 38 and it produces an oscillator signal 40 which alternates between two states at roughly a 50% duty cycle.

The detection sub-circuit 28 provides an error signal 42 which includes a characteristic that is representative of how much the desired output and the actual output voltage differ at the output terminal 18 of the charge pump 12. This is also much as in prior art charge pumps, and essentially similar components can be used. However, as will be discussed in more detail, below, the error signal 42 produced by the inventive regulating system 10 is used much differently.

In the embodiment illustrated in FIG. 7, the detection sub-circuit 28 includes a voltage divider network 44 formed

by a first resistor 46 which is series connected with a second resistor 48 at a feedback node 50. This divider network 44 is connected across the output terminal 18 and the common terminal 16 of the charge pump 12. For example, if the first resistor 46 is nominally 30 kilo ohms (k $\Omega$ ) and the second resistor 48 is nominally 10 k $\Omega$ , a quarter of the actual output voltage of the charge pump 12 is provided as a feedback signal 52 from the feedback node 50. A voltage reference 54 is further provided to supply a reference signal 56. A 1.23 volt bandgap device may be used as the voltage reference 54. An error amplifier 58, say one providing a gain of 20 $\times$ , receives both the feedback signal 52 and the reference signal 56, as its inputs, and from them creates the error signal 42.

The enable sub-circuit 30 provides the enable signal 38 to the oscillator 26. While one method of prior art charge pump regulation (skip mode) does use enabled oscillation, as contrasted with free running oscillation, and thus does employ an enable signal, the circuitry used here and particularly when this enable signal 38 is actually produced are key distinctions of the inventive regulating system 10 over the prior art.

In the embodiment illustrated in FIG. 7, the enable sub-circuit 30 includes a replica branch 64 formed by a resistor 66 which is series connected with a replica device 68 at a replica node 70. The replica branch 64 is connected across the input terminal 14 and the common terminal 16, and produces a threshold signal 72 from the replica node 70. The "threshold" here is representative of the minimum efficient energy quanta for operation of the charge pump 12. The nature and purpose of the threshold signal 72 produced here are discussed further below. The "replica" here is a characteristic which we want to replicate. Since the switching sub-circuit 32 will typically employ transistors, the replica device 68 used here is a suitable diode connected device for replicating junction characteristics in the switching sub-circuit 32. Replica transistors and diode connection are conventional arts, and general discussion of such is therefore not appropriate here.

Those skilled in the electronics arts will readily appreciate that it is the ratios of components which can be controlled precisely and which are therefore important; precise actual values are usually difficult to obtain in integrated circuit embodiments. Thus replica principles are useful and actual values for components such as the first resistor 46 and the second resistor 48 are not important, as contrasted to their ratio, which is.

In FIG. 7 the replica device 68 is an n-channel MOSFET transistor with its gate directly connected to its source. An enable amplifier 74, say one providing a 100 $\times$  gain, receives both the error signal 42 and the threshold signal 72, and creates from these inputs the enable signal 38. Departing from FIG. 7 briefly, FIG. 8 is a block diagram of an alternate enable sub-circuit 30, depicting implementation in a physically simpler manner. As can be seen in FIG. 8, the replica device and the enable amplifier may be combined in some implementations, particularly in integrated circuits, but FIG. 7 better conceptually depicts the key aspects of operation of the regulating system 10.

The switching sub-circuit 32 performs two concurrent functions. First, responsive to the oscillator signal 40, it switches the flying capacitor 24 alternately to the input terminal 14 and the output terminal 18 of the charge pump 12. Second, responsive to the error signal 42, it controls the series resistance of the charge path to the flying capacitor 24. The first function, switching, is essentially the same as that of oscillator switching sub-circuits used in all charge pumps,

see e.g., FIG. 3-5 (prior art). The second function, resistance control, is conceptually similar to what occurs in constant frequency mode regulation, see e.g., FIG. 5. However, the manner of controlling the charging rate of the flying capacitor 24 in the charge pump 12 is different here. This is also discussed further below.

In the embodiment illustrated in FIG. 7, the switching sub-circuit 32 includes a first switch 78, a channel unit 80, and a second switch 82 (depicted to emphasize conceptual operation; as previously noted with respect to FIG. 4 (prior art) and as should be readily appreciated by those skilled in the electronic arts, various embodiments are possible based on particular characteristics of the materials used, e.g., integrated circuit semiconductor material or electrolytic capacitor nature). The oscillator signal 40 operates these components in switch-like manner, and the error signal 42 further operates the channel unit 80 in a variable resistance-like manner.

In such operation, when a heavy load (not shown) is connected across the output terminal 18 and the common terminal 16 of the charge pump 12 the inventive regulating system 10 performs much as prior art charge pumps do. The oscillator 26 is enabled and runs continuously to operate the first switch 78, the channel unit 80, and the second switch 82 in the manner of switches. Concurrently, the error signal 42 is present and due to the heavy load is of sufficient magnitude that the channel unit 80 is directed to apply minimum resistance in the charging path to the flying capacitor 24. Accordingly, continuous, maximum sized quanta of energy are transferred from the input to the output of the charge pump 12.

In contrast, when a light load is present at the output the inventive regulating system 10 operates the charge pump 12 much differently. As the output load (I-OUT) gets smaller and smaller, say once the load is reduced (start up situations initially appear as a "heavy" load), the output voltage (V-OUT) gets higher and higher. At some point in this scenario the error signal 42 becomes less than the threshold signal 72, and the enable amplifier 74 ceases producing the enable signal 38. The output voltage is then held without any charge being distributed to the output capacitor 22 until such time as the load on the output (or the very small current through the divider network 44) draws the output voltage down again. Eventually this happens and the error signal 42 is once again produced. However, since the load is light the discrepancy between the actual and desired output voltages is initially quite small, and the error signal 42 initially has too small a magnitude to cause the enable signal 38 to immediately be produced, i.e., it is still less than the threshold signal 72. Thus the oscillator 26 is not quite yet enabled. But the continuing draw of the load on the reservoir in the output capacitor 22 at some point does soon cause the error signal 42 to exceed the threshold signal 72, and the enable signal 38 is then produced. The oscillator 26 then cycles once. But only once in this light load scenario, because the quanta transferred into the output capacitor 22 in this single cycle is enough to cause the output voltage to increase enough that the error signal 42 either again ceases or its magnitude drops again below that of the threshold signal 72. Thus the first function of the switching sub-circuit 32 has occurred.

The second function of the switching sub-circuit 32 occurs concurrently. During the single cycle noted above, the magnitude of the error signal 42 controls the channel unit 80 such that the charge path to the flying capacitor 24 has a high resistance. Therefore the quanta transferred into the output capacitor 22 here is appropriately small.

The above process can be summarized by analogy to maintaining the level in a swimming pool when one has to carry water to the pool in a bucket. On some days evaporation will be high, i.e., high load, and a lot of water will need to be added. And on other days evaporation will be low, i.e., low load. Carrying whole buckets of water works well when there is high evaporation, and when there is low evaporation one can wait until a whole bucket is needed. This is skip mode regulation. Quiescent load is low, i.e., one has to make few trips to and from the water source. In contrast, one can constantly run back and forth between the pool and the water source, taking buckets full when the load is high and mere drops of water in the bucket when the load is light. This is constant frequency mode regulation. Quiescent load is high, i.e., one is constantly making trips, regardless of whether much water is needed. What is needed is a more controlled approach, one adding sensing at the pool of when a predetermined, efficient minimum quanta of water is needed.

Returning now to discussion of the inventive regulating system 10 for charge pumps, the voltage of the threshold signal 72 (FIG. 7) is ideally some threshold voltage plus a small voltage determined to be the right amount to set a pulse skipping threshold. While the replica network 64 described above is the inventor's presently preferred approach to accomplish this, others means may be used. The goal is any mechanism that minimizes the amount of energy expended to transfer the flying capacitor energy over to the output. Techniques other than just the modulated resistance approach of FIG. 7 are therefore possible.

FIG. 8 is a block diagram illustrating one suitable substitute for the enable sub-circuit 30 of the embodiment in FIG. 7. As can be appreciated there, the enable amplifier 74 of FIG. 7 can be eliminated by using a transistor 86 and an inverter 88.

FIG. 9 is a block diagram illustrating one suitable substitute for the detection subcircuit 28 of the embodiment in FIG. 7. Detecting when a voltage deviates from its desired value can be accomplished in many ways, and many substitutes for the detection sub-circuit 28 are therefore possible.

In the Background Art section it was noted that charge pumps can convert input voltages to output voltages which are either higher, lower, alternately both, or inverted in voltage value. FIG. 7 depicts a "boost" embodiment, one which produces a higher output voltage. Once the principle of the inventive regulating system 10 is appreciated, it may be applied as well to "buck" embodiments (for producing a lower output voltage) and also to embodiments producing an inverted output voltage. Alternately producing boost or buck requires determining which is desired and then merely switching an appropriate embodiment accordingly.

In addition to the above mentioned examples, various other modifications and alterations of the inventive regulating system 10 may be made without departing from the invention. Accordingly, the above disclosure is not to be considered as limiting and the appended claims are to be interpreted as encompassing the true spirit and the entire scope of the invention.

#### INDUSTRIAL APPLICABILITY

The present regulating system 10 is well suited for application in a wide variety of charge pump applications. While the above discussion has focused on charge pumps suitable for stepping up an input voltage to a desired output voltage, the regulating system 10 may also be used for

stepping down an input voltage, either to a voltage having the same polarity or to a voltage having inverted polarity.

The regulating system 10 provides particular benefits over existing charge pump regulating schemes. It operates efficiently yet automatically across a range from light to maximum loads. When supplying heavy and maximum loads, it has efficiency equal to that of conventional constant frequency mode regulation. Yet when supplying light loads, it operates with efficiency equal to conventional skip mode regulation. And unlike these conventional modes, which cannot be dynamically switched between during operation because external components must be changed, the present regulating system 10 automatically adapts to the load which is actually present.

Furthermore, the regulating system 10 can employ more desirable electrical components. This is so with respect to the physical size, type, cost and yet other factors which motivate component selection. For example, to step-up a 3.3 volt input to a 5.0 volt output with conventional skip mode regulation a charge pump would typically require a 2.2 uF input capacitor, a 1 uF flying capacitor, and a 10 uF ceramic type output capacitor (for which a 47 uF tantalum type might well have to be substituted). In contrast, achieving the same voltage conversion with conventional constant frequency mode regulation typically would require only a 1 uF input capacitor, a 0.47 uF flying capacitor, and a 2.2 uF ceramic output capacitor (likely avoiding the expense and other problems associated with tantalum capacitors, such as voltage ripple due to high equivalent series resistance). The smaller value components may also provide direct cost savings and indirect savings as well, such as use of less circuit board space. Obviously, using components sized for conventional constant frequency mode regulation is preferable. The inventive regulating system 10 can use such components, yet not suffer from the performance limitations of the prior art regulation schemes.

For the above, and other, reasons, it is expected that the regulating system 10 of the present invention will have widespread industrial applicability, and it is therefore expected that the commercial utility of the present invention will be extensive and long lasting.

**PULSE FREQUENCY OPERATION OF REGULATED CHARGE PUMPS** Inventor: THURBER Jr., Charles R. Atty. ref.: MAX1P048

THIS CORRESPONDENCE CHART IS FOR EASE OF UNDERSTANDING AND INFORMATIONAL PURPOSES ONLY, AND DOES NOT FORM A PART OF THE FORMAL PATENT APPLICATIONS.

10	regulating system
12	charge pump
14	input terminal
16	common terminal
18	output terminal
20	input capacitor
22	output capacitor
24	flying capacitor
26	oscillator
28	detection sub-circuit
30	enable sub-circuit
32	switching sub-circuit
38	enable signal
40	oscillator signal
42	error signal
44	divider network
46	first resistor

-continued

48	second resistor
50	feedback node
52	feedback signal
54	voltage reference
56	reference signal
58	error amplifier
64	replica branch
66	resistor
68	replica device
70	replica node
72	threshold signal
74	enable amplifier
78	first switch
80	channel unit
82	second switch
86	transistor
88	inverter

What is claimed is:

1. A circuit for regulating a charge pump receiving an input signal across an input terminal and a common terminal and producing an output signal across an output terminal and the common terminal, wherein the input signal has an input voltage and the output signal has an output voltage and the charge pump includes an input capacitor connected across the input terminal and the common terminal, and an output capacitor connected across the output terminal and the common terminal, and a flying capacitor having a first side and a second side, the circuit comprising:

an oscillator which, when enabled by an enable signal, produces an oscillator signal that alternates between a first state and a second state;

a detection sub-circuit producing an error signal when the output voltage deviates from a desired output voltage, wherein said error signal has voltage representative of how much the output voltage differs from said desired output voltage;

a channel-switch sub-circuit suitable for connecting the flying capacitor across the common terminal and the input terminal when said oscillator signal is in said first state, and alternately connecting the flying capacitor across the common terminal and the output terminal when said oscillator signal is in said second state;

said channel-switch sub-circuit further suitable for controllably setting resistance to the flying capacitor responsive to voltage in said error signal when said oscillator signal is in said first state; and

an enable sub-circuit producing said enable signal when said error signal has voltage exceeding said desired output voltage by a preset amount, for regulating the charge pump by enabling said oscillator to operate said channel-switch sub-circuit to alternately charge the flying capacitor at a rate controlled by resistance set by said channel-switch sub-circuit from the input terminal and to discharge the flying capacitor via the output terminal into the output capacitor.

2. The circuit of claim 1, wherein said detection sub-circuit includes:

a reference unit suitable for producing a reference signal having said desired output voltage; and

an error comparator suitable for producing said error signal when said output voltage differs from said desired output voltage.

3. The circuit of claim 1, wherein said detection sub-circuit includes:

a voltage divider connected across said output terminal and said common terminal, wherein said voltage

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divider produces a feedback signal having voltage related to the output voltage;

a reference unit suitable for producing a reference signal having voltage related to said desired output voltage; and

an error comparator suitable for producing said error signal when a relationship between said feedback signal and said reference signal indicates that the output voltage differs from said desired output voltage.

4. The circuit of claim 1, wherein:

said channel-switch sub-circuit connects the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state; and

said channel-switch sub-circuit alternately connects the first side of the flying capacitor to the input terminal and the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to operate the charge pump such that the output voltage produced is of same polarity and of higher value than the input voltage received by the charge pump.

5. The circuit of claim 1, wherein:

said channel-switch sub-circuit connects the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state; and

said channel-switch sub-circuit alternately connects the first side of the flying capacitor to the output terminal and the second side of the flying capacitor to the common terminal when said oscillator signal is in said second state, to operate the charge pump such that the output voltage produced is of opposite polarity and of lower value than the input voltage received by the charge pump.

6. The circuit of claim 1, wherein:

the first side of the flying capacitor is connected to the common terminal;

said channel-switch sub-circuit connects the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state; and

said channel-switch sub-circuit alternately connects the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to operate the charge pump such that the output voltage produced is of same polarity and of lower value than the input voltage received by the charge pump.

7. The regulated charge pump of claim 1, wherein said enable sub-circuit includes:

a resistance series connected with a replica device at a node and together connected across the input terminal and the common terminal such that a threshold signal is produced at said node; and

an enable comparator suitable for producing said enable signal when voltage in said error signal is greater than voltage in said threshold signal.

8. The circuit of claim 5, wherein said replica unit is a diode connected device.

9. The circuit of claim 6, wherein said diode connected device is a MOSFET transistor with gate and drain connected together.

10. The circuit of claim 1, wherein said channel sub-circuit includes at least one n-channel MOSFET transistor.

11. The circuit of claim 1, wherein said switch sub-circuit is a plurality of transistors operating in a double pole single throw manner.

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12. A method for regulating a charge pump receiving an input signal having an input voltage and producing an output signal having an output voltage, wherein the charge pump is of the type having an input capacitor connected across an input terminal and a common terminal, an output capacitor connected across an output terminal and the common terminal, and a flying capacitor having a first side and a second side, the method comprising the steps of:

(a) producing an error signal when the output voltage of the charge pump deviates from a desired output voltage;

(b) comparing said error signal with a desired enable threshold to produce an enable signal when said error signal exceeds said desired enable threshold;

(c) enabling an oscillator, responsive to presence of said enable signal, to produce an oscillator signal alternating between a first state and a second state;

(d) charging the flying capacitor from the input terminal of the charge pump when said oscillator signal is in said first state and discharging the flying capacitor into the output capacitor when said oscillator signal is in said second state;

(e) setting a resistance, responsive to magnitude of said error signal, controlling at what rate the flying capacitor charges and discharges, thereby regulating the charge pump.

13. The method of regulating of claim 12, wherein said step (a) includes:

producing a feedback signal having voltage related to the output voltage;

producing a reference signal having voltage related to said desired output voltage; and

comparing said feedback signal to said reference signal, to produce said error signal when the output voltage is less than said desired output voltage.

14. The method of regulating of claim 12, wherein said step (b) includes:

producing a threshold signal having magnitude representative of a minimum level for efficient operation of the charge pump; and

comparing said threshold signal to said error signal, to produce said enable signal when said error signal exceeds said desired enable threshold.

15. The method of regulating of claim 12, wherein said step (d) includes:

switching connection of the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state, to charge the flying capacitor; and

switching connection of the first side of the flying capacitor to the input terminal and the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to discharge the flying capacitor such that the charge pump operates to produce the output voltage of same polarity and of higher value than the input voltage received by the charge pump.

16. The method of regulating of claim 12, wherein said step (d) includes:

switching connection of the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state, to charge the flying capacitor; and

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switching connection of the first side of the flying capacitor to the output terminal and the second side of the flying capacitor to the common terminal when said oscillator signal is in said second state, to discharge the flying capacitor such that the charge pump operates to produce the output voltage of opposite polarity and of lower value than the input voltage received by the charge pump. 5

17. The method of regulating of claim 12, wherein said step (d) includes: 10

connecting the first side of the flying capacitor to the common terminal;

switching connection of the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state, to charge the flying capacitor; and 15

switching connection of the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to discharge the flying capacitor such that the charge pump operates to produce the output voltage of same polarity and of lower value than the input voltage received by the charge pump. 20

18. The method of regulating of claim 12, wherein said step (d) includes: 25

determining whether the input voltage is lower or higher than said desired output voltage;

if the input voltage is lower than said desired output voltage, then: 30

switching connection of the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal

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when said oscillator signal is in said first state, to charge the flying capacitor; and

switching connection of the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to discharge the flying capacitor such that the charge pump operates to produce the output voltage of same polarity and of lower value than the input voltage received by the charge pump; and

if the input voltage is higher than said desired output voltage, then:

switching connection of the first side of the flying capacitor to the common terminal and the second side of the flying capacitor to the input terminal when said oscillator signal is in said first state, to charge the flying capacitor; and

switching connection of the first side of the flying capacitor to the input terminal and the second side of the flying capacitor to the output terminal when said oscillator signal is in said second state, to discharge the flying capacitor such that the charge pump operates to produce the output voltage of same polarity and of higher value than the input voltage received by the charge pump.

19. The method of regulating of claim 12, wherein said step (e) includes setting said resistance by controllably biasing at least one transistor to control charging current to the flying capacitor.

20. The method of regulating of claim 19, wherein at least one said transistor is of an n-channel MOSFET type.

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Yoshida et al.

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(45) Date of Patent: **Apr. 12, 2005**

(54) **POWER SOURCE INVERTER CIRCUIT**

(75) Inventors: Yoshifumi Yoshida, Chiba (JP);  
Fumiyasu Utsunomiya, Chiba (JP)

(73) Assignee: Seiko Instruments Inc., Chiba (JP)

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(52) U.S. Cl. .... 363/60; 363/62

(58) Field of Search ..... 323/222, 271,  
323/282, 285; 363/59, 60, 62

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,581,454 A \* 12/1996 Collins ..... 363/59

5,656,870 A \* 8/1997 Turnbull ..... 307/64  
5,973,944 A \* 10/1999 Nork ..... 363/60  
6,522,558 B2 \* 2/2003 Henry ..... 363/60

\* cited by examiner

Primary Examiner—Jeffrey Sterrett  
(74) Attorney, Agent, or Firm—Adams & Wilks

(57) **ABSTRACT**

A power source inverter circuit is provided which, when a feeding unit generates enough electric power, puts a load circuit into operation while storing electric power in a storage unit and, when the power feeding unit stops generating power, efficiently uses up the electric power stored in the storage unit. The power source inverter circuit is composed of: a variable DC—DC converter for raising or dropping a voltage of electric power that is supplied from the power feeding unit; the storage unit; MOSFET switches for connecting the power feeding unit and the storage unit to an input of the variable DC—DC converter and for connecting an output of the variable DC—DC converter to the storage unit and the load circuit; a control circuit for controlling gates of the MOSFET switches; and a voltage detector for monitoring output of the power feeding unit, the voltage of the storage unit, the input voltage of the load circuit, and for outputting voltage information to the variable DC—DC converter as well as to the control circuit.

5 Claims, 12 Drawing Sheets

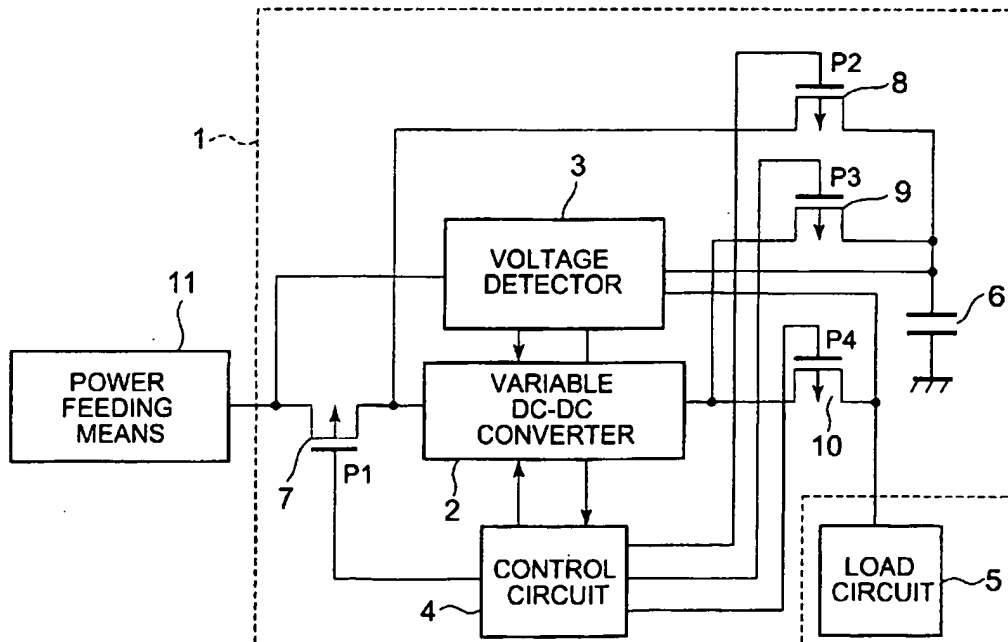




FIG.1

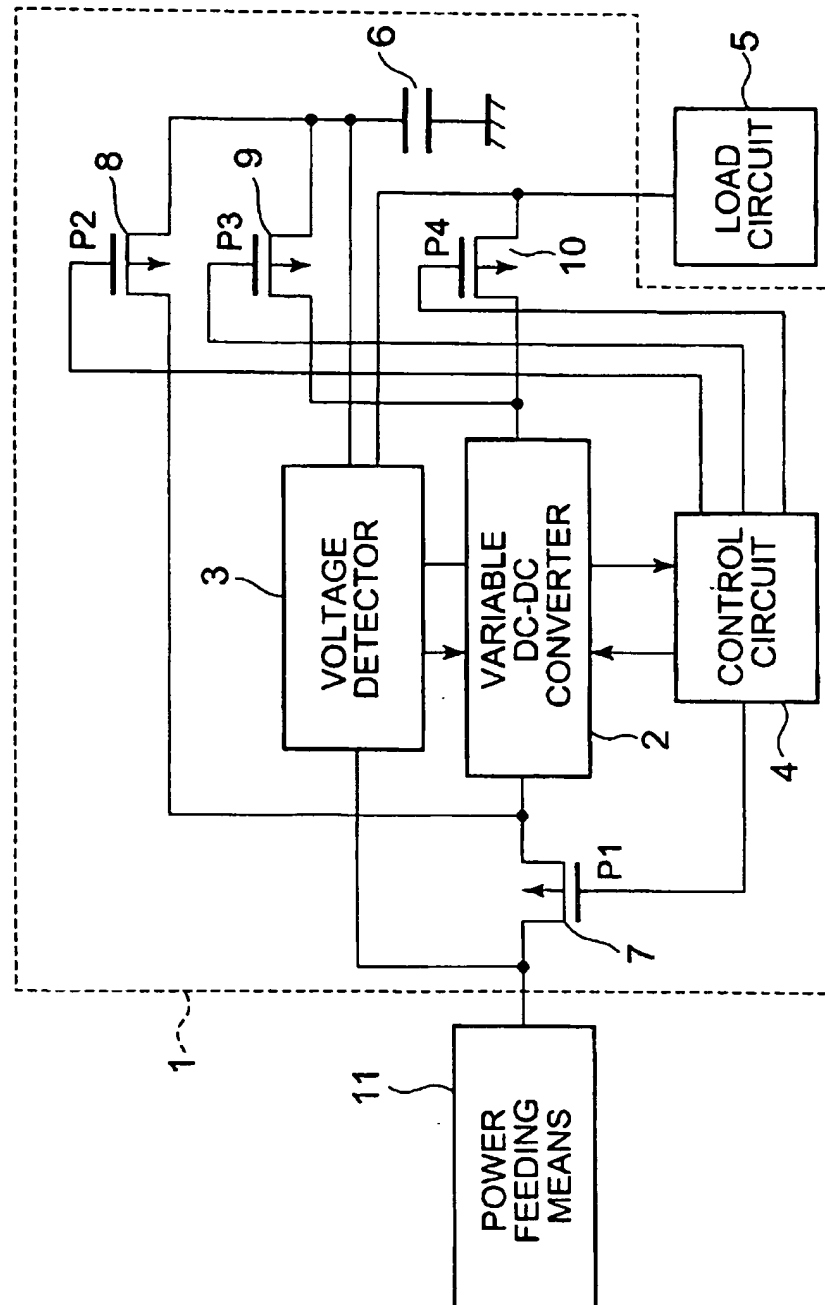


FIG.2

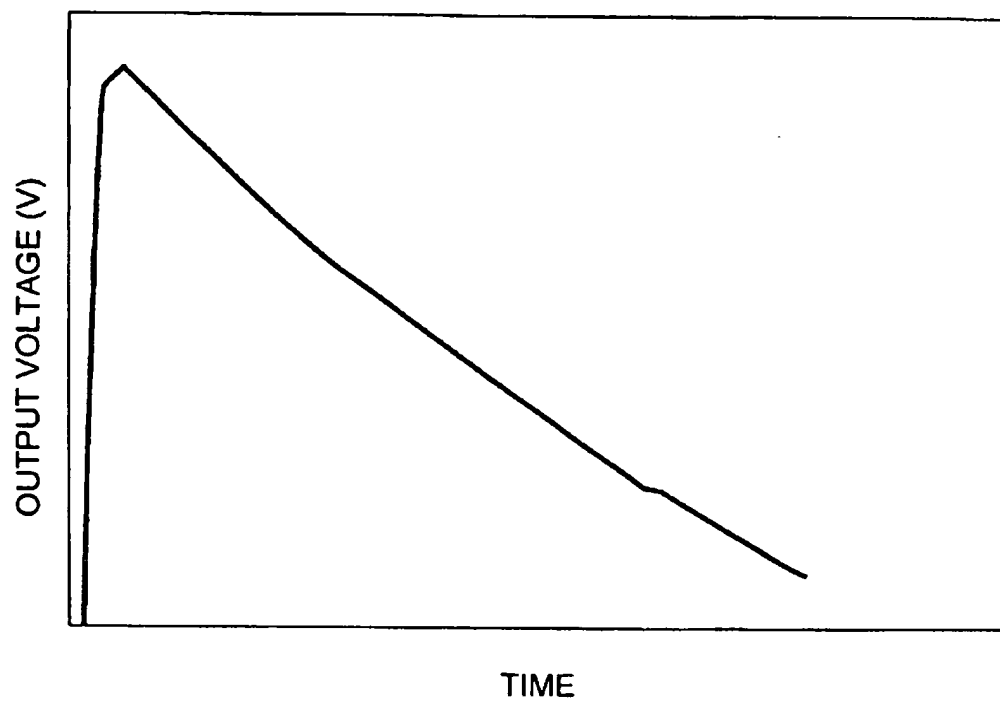


FIG.3A

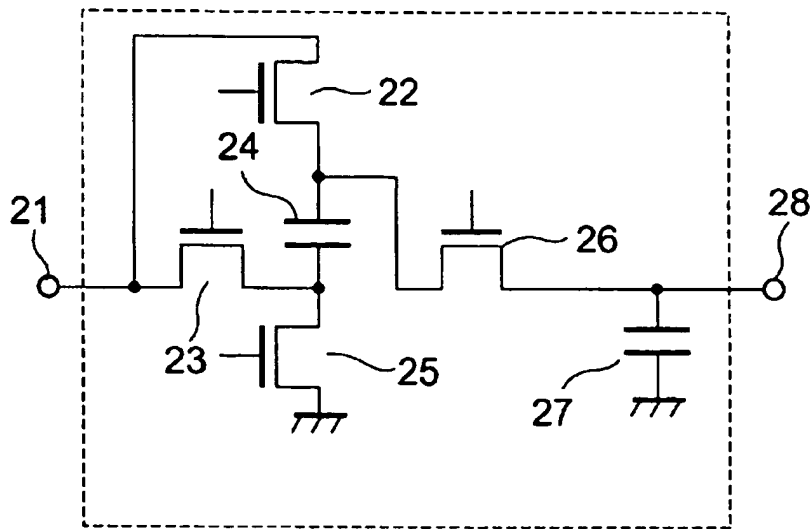


FIG.3B

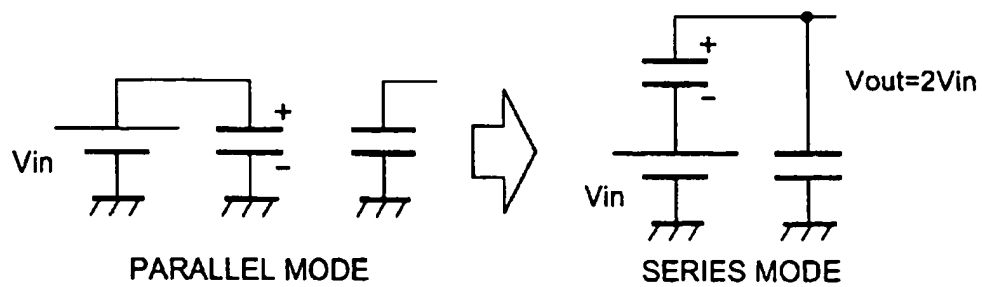




FIG.5

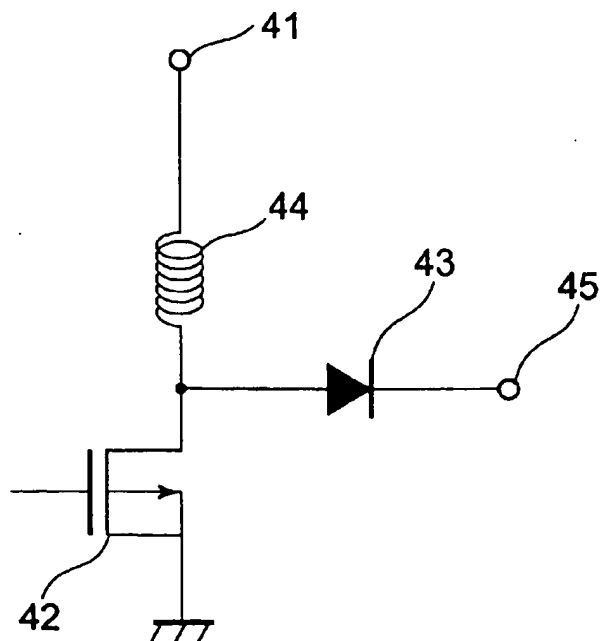
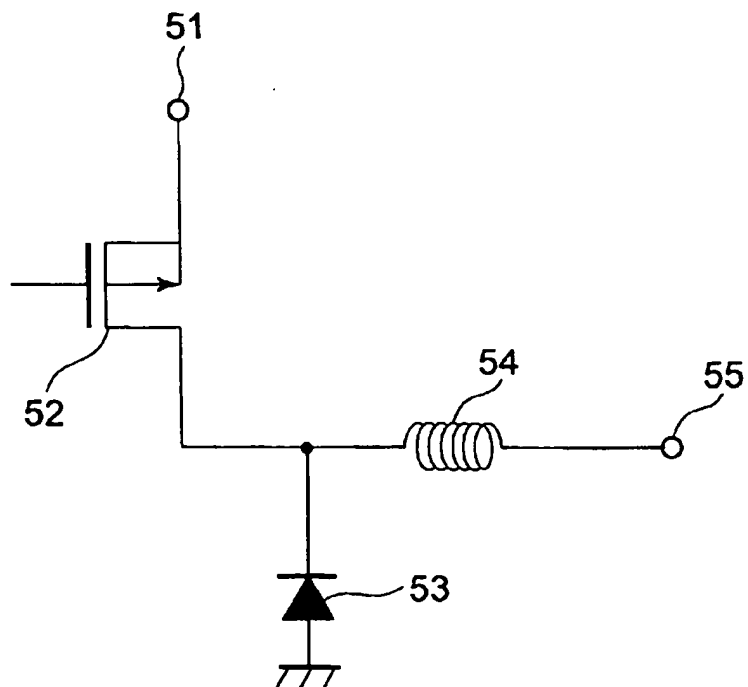


FIG.6



**FIG. 7**

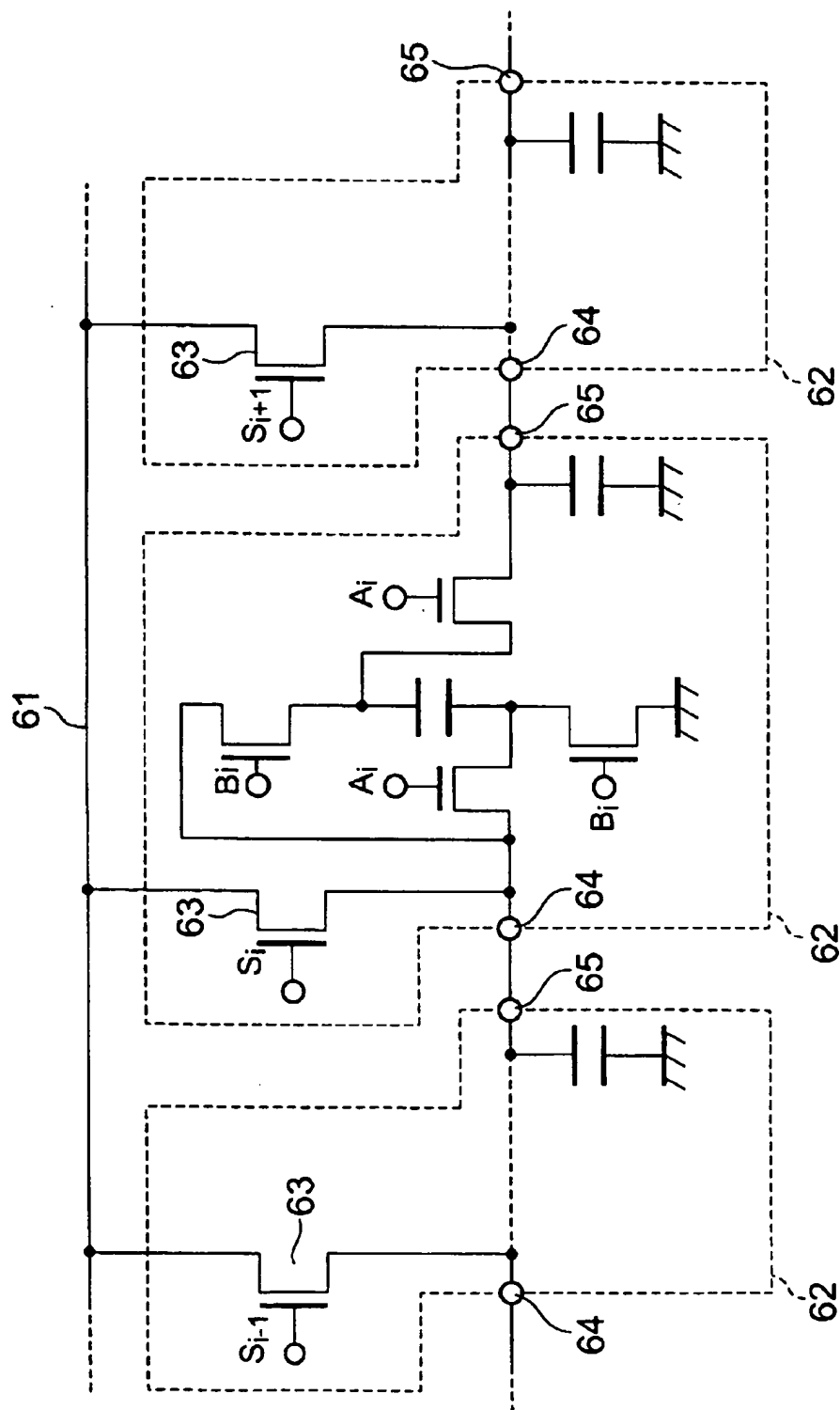


FIG. 8

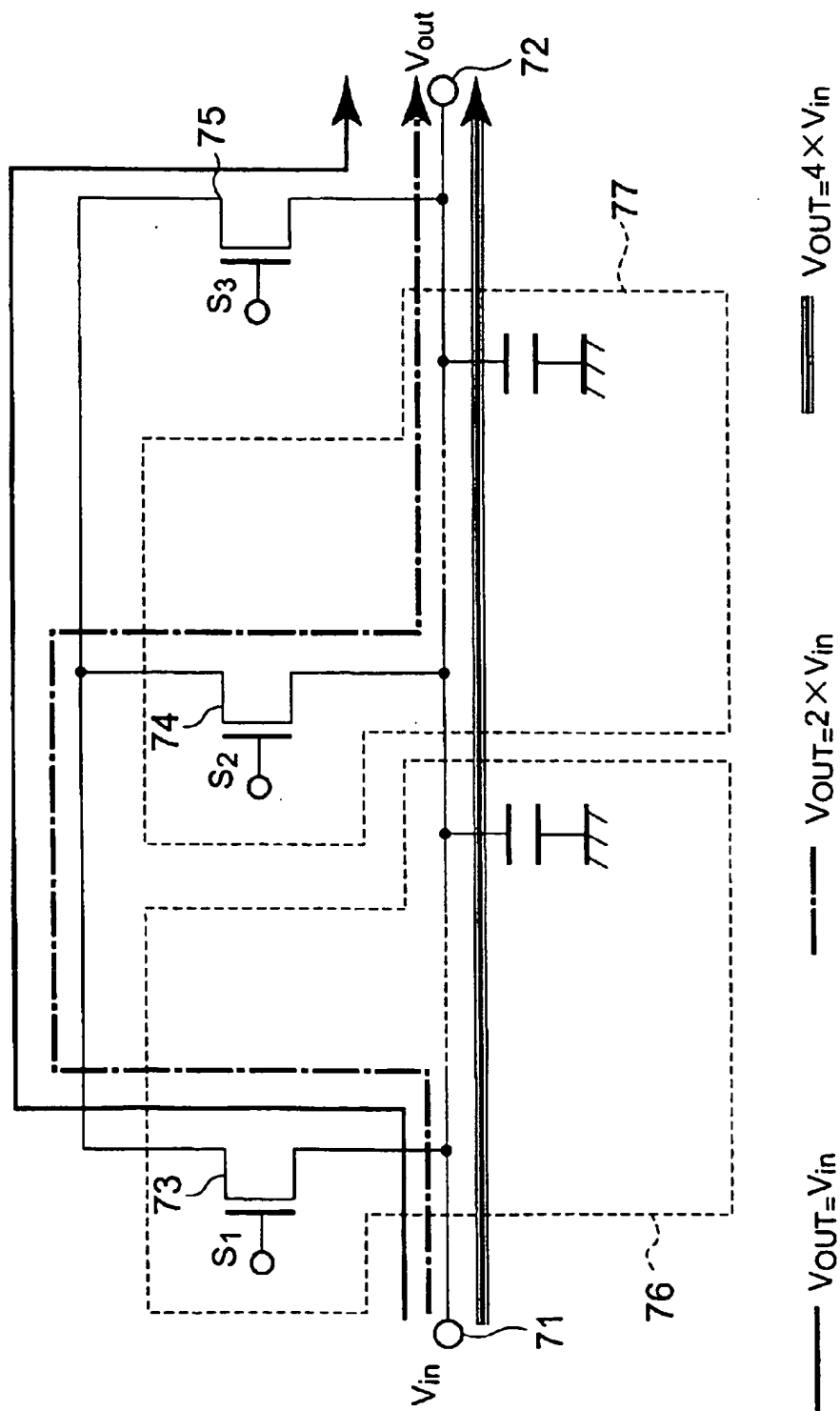


FIG.9A

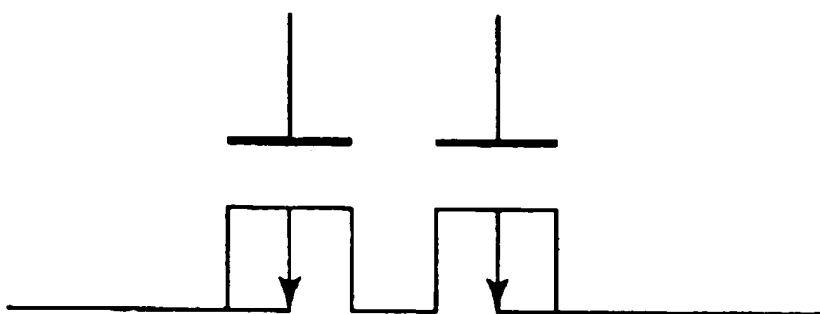


FIG.9B

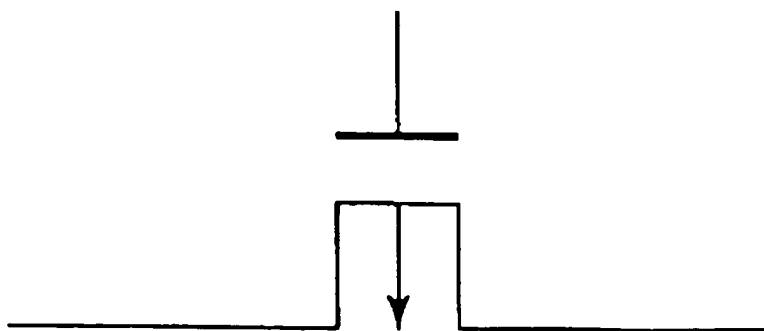




FIG.10

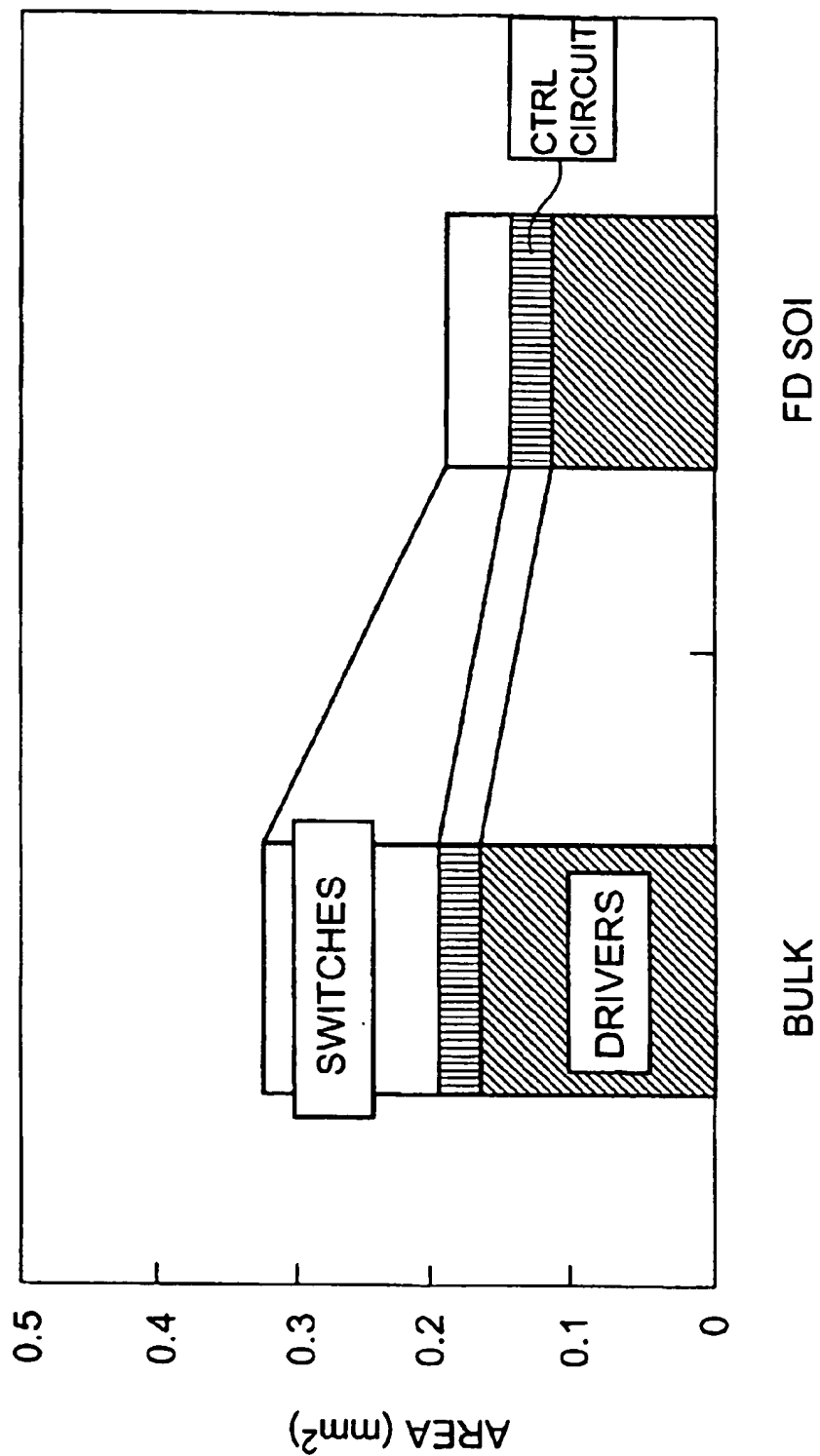


FIG. 11

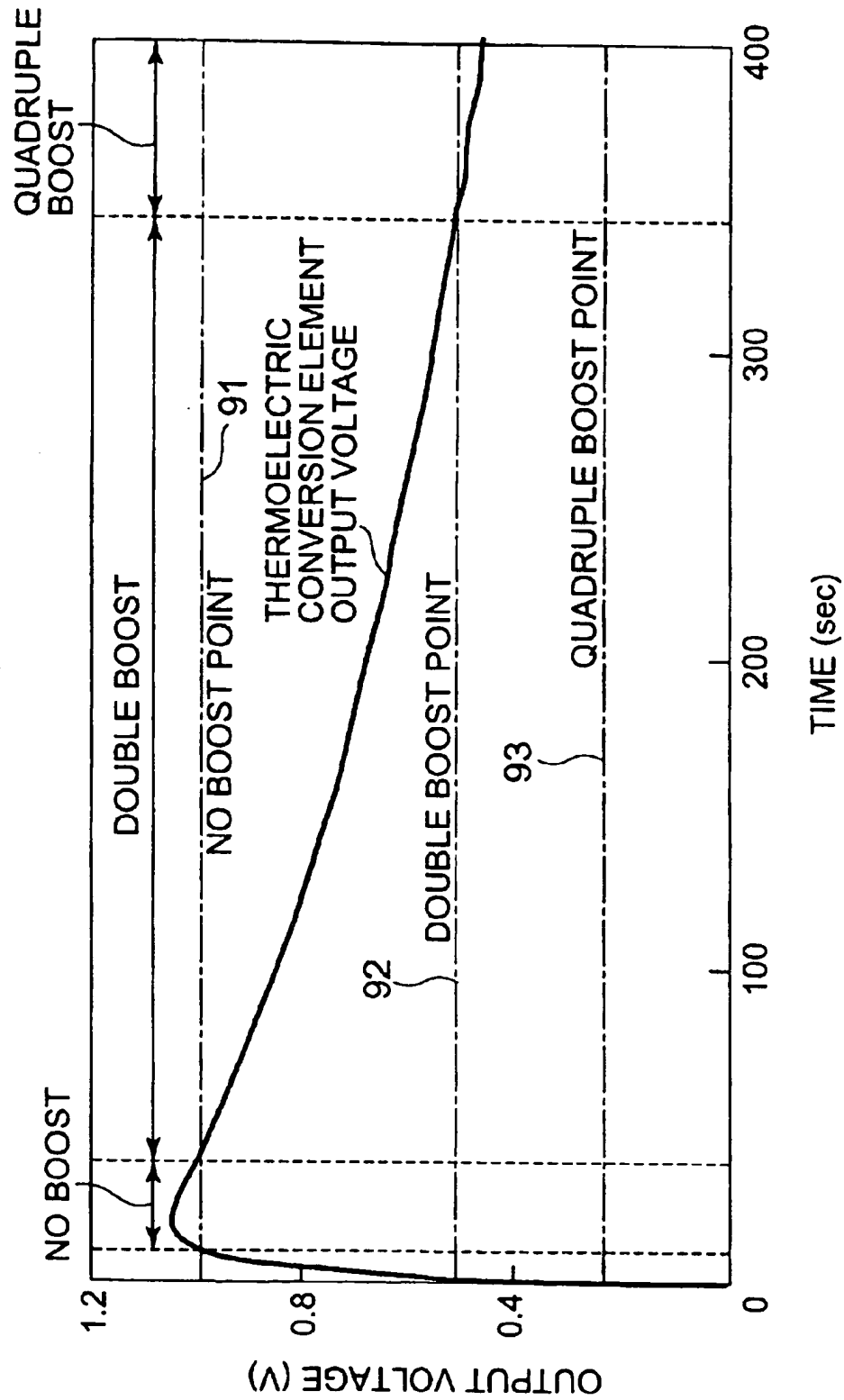


FIG. 12

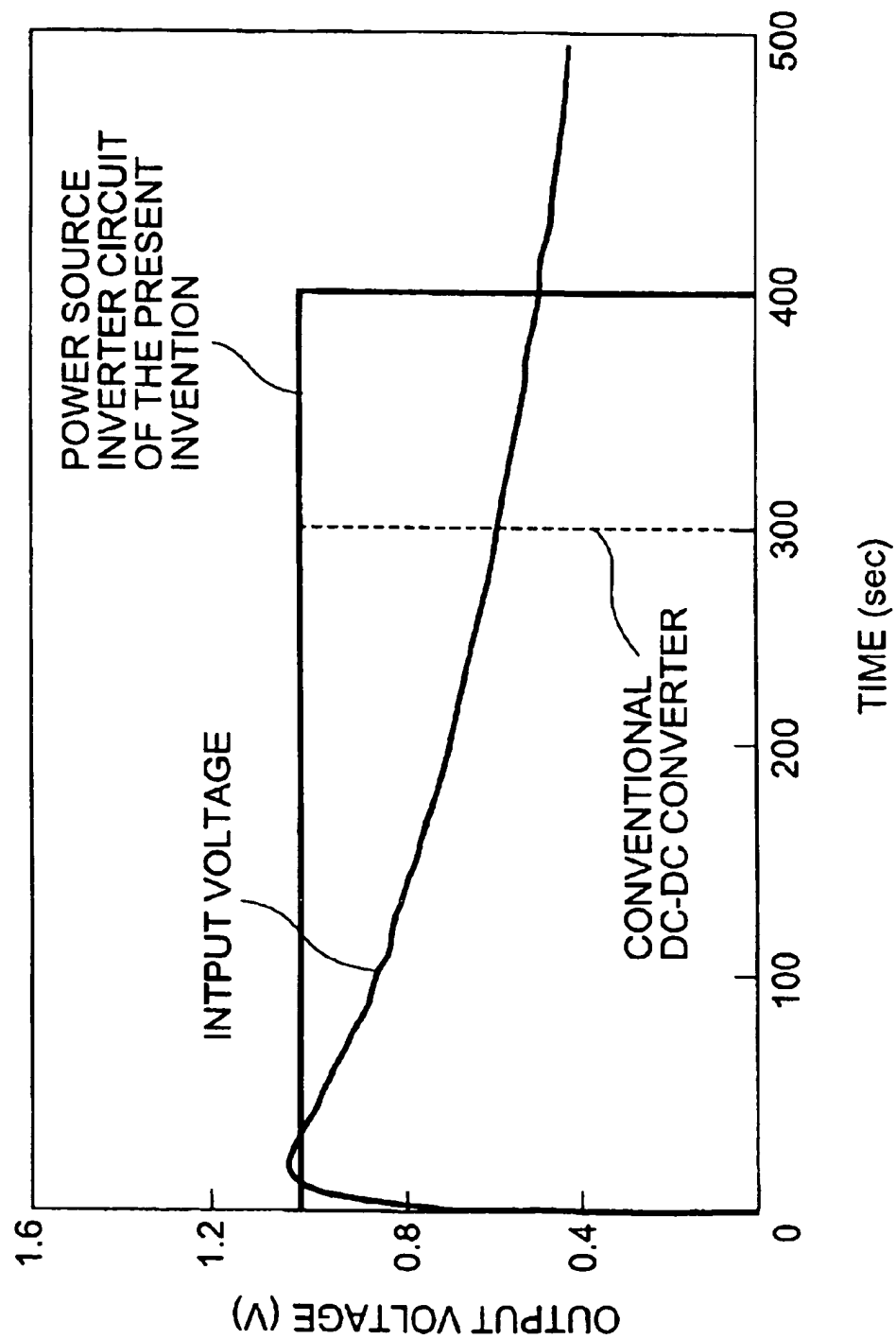
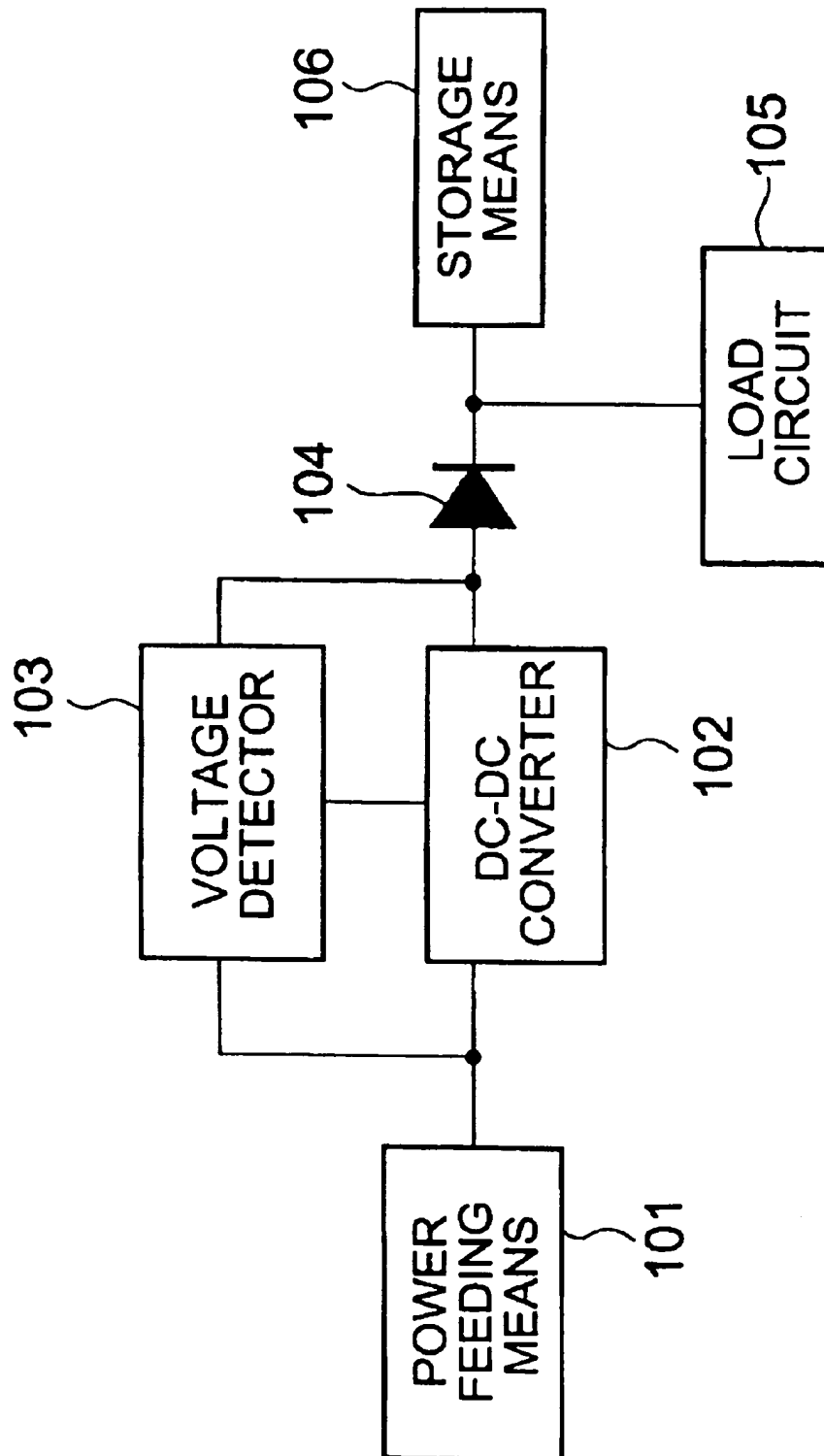


FIG. 13



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**POWER SOURCE INVERTER CIRCUIT****BACKGROUND OF THE INVENTION****1. Field of the Invention**

The present invention relates to a power source inverter circuit, more specifically, a power source inverter circuit for electronic instruments driven by use of output of a solar module or a thermoelectric conversion element in which electric power generated is supplied to a load circuit with efficiency and excess electric power is stored in storage means.

**2. Description of the Related Art**

Conventional power source inverter circuits supply a load circuit with electric power of power feeding means which changes its voltage and current with time or with a change in environment and have, as shown in FIG. 12, a DC—DC converter, a rectifier element for rectifying electric power outputted from the DC—DC converter, a voltage detector for detecting the voltage of the storage means, storage means for storing rectified electric power, and a load circuit. In such conventional power source inverter circuits where a load circuit is supplied with electric power of a solar module, a thermoelectric conversion circuit, or other similar power feeding means which changes its voltage and current with time or with a change in environment, operation of a DC—DC converter is controlled by monitoring the voltage with a voltage detector such that the DC—DC converter is put into operation when electric power supplied from the power feeding means has a voltage equal to or higher than the minimum operation voltage of the DC—DC converter and that the voltage of the storage means reaches a given output voltage. For instance, if the DC—DC converter is a switched capacitor type DC—DC converter, the output voltage is kept constant by turning the DC—DC converter on and off for intermittent operation.

The electric power that has undergone voltage conversion is rectified by a rectifier element such as a Schottky diode, and then stored in the storage means through charging. At this point, the electric power stored in the storage means is supplied to the load circuit since the charging means and the load circuit are connected in parallel to each other. The load circuit is put into operation as the stored voltage of the charging means reaches the minimum drive voltage of the load circuit or higher. Accordingly, when the storage means has large capacity, the voltage of the storage means is slow to rise and activation takes extremely long. Thus prior art requires, for continuous operation of the load circuit, efficient charging of the storage means without exhausting the storage means of electric power and without allowing the voltage of the storage means to drop lower than the minimum drive voltage of the load circuit.

In addition, the step-up and step-down multiple numbers are fixed in conventional power source inverter circuits in the case of using switched capacitor type DC—DC converters as the DC—DC converters. In this case, charging cannot be conducted when there is a change in output voltage of the power feeding means and either raising or lowering the voltage cannot help the output voltage of the DC—DC converter from dropping below the output of the storage means.

Furthermore, the load circuit, which operates on electric power stored in the storage means after output of the power feeding means becomes unavailable, stops its operation once the voltage of the storage means drops below the minimum operation voltage of the load circuit. At this point, there are still electric charges left in the storage means.

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Examples of the above-described means for feeding electric power that changes its voltage with time include thermoelectric conversion elements and solar panels for use in portable electronic instruments that are relatively small in power consumption. For instance, thermoelectric conversion elements, which employ PN junction between a P type semiconductor and an N type semiconductor to generate electric power from an electromotive force created by a temperature difference, change their electromotive forces (voltage) as the temperature difference changes with time.

In such conventional power source inverter circuits, supplying the load circuit with a constant voltage requires stopping the operation of the DC—DC converter or adjusting the amount of electric power taken out. The amount of electric power taken out is accordingly no larger than the amount of electric power needed by the load circuit even when the power feeding means is capable of generating and outputting more. This means that the excess electric power goes to waste. In particular, power feeding means such as a solar module or a thermoelectric conversion circuit is quick to change its output voltage in response to a change in environment or with time, thereby making it difficult to maintain the same level of output performance. Accordingly, it is necessary to take as much electric power as possible out of the power feeding means while the power feeding means has high power generation ability, namely, when the amount of light is very large or when there is a heat source.

In addition, in power feeding means that uses a natural energy source, such as a solar module or a thermoelectric conversion circuit, the relation between the output voltage and the output current has a local maximal value which equals to the maximum power generation efficiency. Since power feeding means that uses a natural energy source is small in energy amount, it is desirable to take out electric power always with the maximum power generation efficiency. Here lies another inconvenience because, in conventional power source inverter circuits where the amount of electric power to be taken out of the power feeding means is determined in accordance with power consumption of the load circuit, electric power is rarely taken out with the maximum power generation efficiency and the excess power is wasted.

Conventional power source inverter circuits, where the storage means and the load circuit are connected in parallel to the output of the rectifier element, have still another inconvenience: the storage empty of electric charges induces a voltage drop even when the output of the DC—DC converter is equal to or higher than the operation voltage of the load circuit and it is not until some electric charges are stored in the storage means that the load circuit can start its operation.

Furthermore, in conventional power source inverter circuits that use switched capacitor type DC—DC converters, the step-up multiple number or the step-down multiple number is fixed and therefore electric power cannot be stored once the output voltage of the DC—DC converter becomes lower than the voltage of the storage means irrespective of power conversion performed on the output power of the power feeding means which changes its output voltage with time or with a change in environment.

Yet another inconvenience is that the load circuit, which operates on electric power stored in the storage means when the power feeding means no longer generates power which changes its output voltage with time or with a change in environment, stops its operation as the voltage of the storage means drops below the minimum operation voltage of the

load circuit. A mere voltage drop renders the load circuit ineffective even though there are enough electric power left in the storage means. Accordingly, the remaining electric power goes to waste.

#### SUMMARY OF THE INVENTION

The present invention has been made in view of the above-mentioned inconveniences of prior art, and an object of the present invention is therefore to provide a power source inverter circuit which, when power feeding means generates enough electric power, puts a load circuit into operation while storing electric power in storage means and, when the power feeding means stops generating power, efficiently uses up the electric power stored in the storage means.

In order to attain the above-mentioned object a power source inverter circuit according to the present invention includes: a variable DC—DC converter for raising or dropping a voltage of electric power which is supplied from power feeding means; storage means for storing electric power whose voltage has been raised or dropped by the variable DC—DC converter; a MOSFET switch for connecting an output of the power feeding means to an input of the variable DC—DC converter; a MOSFET switch for connecting an output of the variable DC—DC converter to an input of the storage means; a MOSFET switch for connecting the output of the variable DC—DC converter to an input of a load circuit; a MOSFET switch for connecting the input of the variable DC—DC converter to the input of the storage means; a control circuit for controlling gates of the respective MOSFET switches; and a voltage detector for monitoring an output voltage of the power feeding means, a voltage of the storage means, and an input voltage of the load circuit, and for outputting voltage information to the variable DC—DC converter and to the control circuit.

According to the power source inverter circuit of the present invention, when the voltage detector detects that the power feeding means is generating and supplying electric power, the control circuit turns on the MOSFET switch that connects the output of the power feeding means and the input of the variable DC—DC converter to each other, so that the generated electric power is inputted to the variable DC—DC converter. The voltage detector further monitors the output voltage of the power feeding means and determines the step-up multiple number and step-down multiple number of the DC—DC converter, which operates based on these multiple numbers. The control circuit next turns on the MOSFET switch that connects the output of the variable DC—DC converter and the input of the load circuit to each other, so that output of the variable DC—DC converter which has been raised or dropped in voltage is supplied to the load circuit. At this point, if the electric power supplied from the variable DC—DC converter is larger than the one used in the load circuit, the control circuit turns off the MOSFET switch that connects the output of the variable DC—DC converter and the input of the load circuit to each other whereas the MOSFET switch that connects the output of the variable DC—DC converter and the input of the storage means to each other is turned on to supply the electric power to the storage means. The load circuit is thus supplied with electric power with a constant voltage.

Moreover, electric power can always be taken out with the maximum power generation efficiency since the number of step-up and step-down stages of the variable DC—DC converter is determined by monitoring the output voltage of the power feeding means. In addition, as much electric

power as possible is taken out of the power feeding means and stored in the storage means while the power feeding means has high power generation ability.

Furthermore, the load circuit can immediately be put into operation as long as the output voltage of the variable DC—DC converter is equal to or higher than the minimum operation voltage of the load circuit even when no electric charges are in the storage means. This is because the power source inverter circuit of the present invention has the MOSFET switch that connects the output of the variable DC—DC converter and the input of the storage means to each other and the MOSFET switch that connects the output of the variable DC—DC converter and the input of the load circuit to each other.

When the power feeding means stops generating and supplying electric power, the voltage detector detects this fact and the control circuit turns off the MOSFET switch that connects the output of the power feeding means and the input of the variable DC—DC converter to each other whereas the MOSFET switch that connects the input of the variable DC—DC converter and the input of the storage means to each other is turned on to input electric charges stored in the storage means to the variable DC—DC converter. The voltage detector monitors the voltage of the storage means and determines the step-up multiple number and step-down multiple number of the DC—DC converter, which operates based on these multiple numbers. The control circuit next turns on the MOSFET switch that connects the output of the variable DC—DC converter and the input of the load circuit to each other, so that output of the variable DC—DC converter which has been raised or dropped in voltage is supplied to the load circuit. At this point also, if the electric power supplied from the variable DC—DC converter is larger than the one used in the load circuit, the control circuit turns off the MOSFET switch that connects the output of the variable DC—DC converter and the input of the load circuit to each other, so that the load circuit is supplied with electric power with a constant voltage. In this way, an inconvenience of the load circuit being halted in its operation as the voltage of the storage means drops lower than the minimum operation voltage of the load circuit is eliminated and every bit of electric power stored in the storage means can be put into use.

#### BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a block diagram showing an outline of the structure of a power source inverter circuit according to an embodiment of the present invention;

FIG. 2 is a graph showing a power generation output characteristic of a thermoelectric conversion element;

FIGS. 3A and 3B are a schematic circuit diagram of a step-up switched capacitor type DC—DC converter according to a mode of the present invention and an operation schematic diagram thereof, respectively;

FIGS. 4A and 4B are a schematic circuit diagram of a step-down switched capacitor type DC—DC converter according to a mode of the present invention and an operation schematic diagram thereof, respectively;

FIG. 5 is a schematic circuit diagram of a step-up LC type DC—DC converter according to a mode of the present invention;

FIG. 6 is a schematic circuit diagram of a step-down LC type DC—DC converter according to a mode of the present invention;

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FIG. 7 is a schematic structural diagram of a variable DC—DC converter according to a mode of the present invention;

FIG. 8 is a diagram showing an operation of the variable DC—DC converter according to a mode of the present invention;

FIGS. 9A and 9B are circuit diagrams of a MOSFET switch according to a mode of the present invention;

FIG. 10 is a graph showing an area effect of the MOSFET switch according to a mode of the present invention;

FIG. 11 is a graph showing a step-up stage number switching operation of a variable DC—DC converter according to a mode of the present invention;

FIG. 12 is a graph showing the duration of operation of a load circuit in a case where a power source inverter circuit according to a mode of the present invention is used; and

FIG. 13 is a diagram showing a conventional power source inverter circuit.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the accompanying drawings, a detailed description will be given below on embodiments of a power source inverter circuit according to the present invention. A power source inverter circuit of this embodiment is for use in a portable instrument having as power feeding means a solar module, a thermoelectric conversion element, or a generator using a motor, which generates electric power varying in voltage and amount depending on environment and time, and aims at efficiently storing electric power generated and consuming the electric power with efficiency.

FIG. 1 is a block diagram showing an outline of a structure of a power source inverter circuit 1 according to this embodiment. The power source inverter circuit 1 of the present invention is composed of: a variable DC—DC converter 2 for raising or dropping the voltage of electric power which is supplied from power feeding means 11; a capacitor 6 for storing electric power whose voltage has been boosted or dropped by the variable DC—DC converter 2; a MOSFET switch (P1) 7 for connecting an output of the power feeding means 11 of a solar module, a thermoelectric conversion element, a generator that uses a motor, or the like to an input of the variable DC—DC converter 2; a MOSFET switch (P3) 9 for connecting an output of the variable DC—DC converter 2 to an input of the capacitor 6; a MOSFET switch (P4) 10 for connecting the output of the variable DC—DC converter 2 to an input of a load circuit 5; a MOSFET switch (P2) 8 for connecting the input of the variable DC—DC converter 2 to the capacitor 6; a control circuit 4 for controlling the above four MOSFET switches; and a voltage detector 3 for monitoring the output voltage of the power feeding means 11, the voltage of the capacitor 6, and the input voltage of the load circuit 5, and for outputting voltage information to the variable DC—DC converter 2 and to the control circuit 4. The effect the power source inverter circuit of the present invention provides is greater particularly when its circuits are configured using semiconductor devices that are formed on a semiconductor film formed through an insulating film on a supporting substrate, namely, fully-depleted SOI devices.

The power feeding means 11 is a solar module, or a thermoelectric conversion element, or a generator that uses a small-sized rotor to convert a rotational energy into electric power. Such power feeding means is varied in voltage and amount of electric power generated or in power generation

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duration depending on its environment including light, heat, and motion, and therefore requires a power source inverter circuit which makes it possible to fully utilize the electric power generated. A solar module and a small-sized rotor generator can output an almost constant voltage as long as there is no change in intensity of light or in dynamic. On the other hand, the output voltage of a thermoelectric conversion element changes greatly even when the heat quantity is constant. The power source inverter circuit 1 of the present invention is particularly effective for such power feeding means as a thermoelectric conversion element.

In a thermoelectric conversion element, for example, a P type thermoelectric material element and an N type thermoelectric material element are sandwiched between two substrates and are joined on the substrates through a metal or other conductive substance forming a PN junction. The plural P type and N type elements are alternately connected in series (P, N, P, N . . . ). When there is a temperature difference between one PN junction and another PN junction of the thermoelectric conversion element, an electric potential difference (electromotive force) according to the temperature difference is created. Therefore higher voltage is obtained by increasing the number of PN junctions. FIG. 2 shows a change with time of the voltage generated as a temperature difference is created between the above two substrates. The voltage abruptly rises immediately after a temperature difference is created between the substrates of the thermoelectric conversion element and then, past a certain peak, the voltage gradually drops until it reaches saturation at a certain level. The initial abrupt voltage rise takes place because, immediately after the temperature difference is created between the substrates, the thermoelectric conversion element can generate a high voltage from the temperature difference. The subsequent voltage drop takes place because the heat of one of the substrates is transmitted with time to the other substrate through the P type and N type thermoelectric material elements to thereby reduce the temperature difference and resultantly reduce the voltage generated. For that reason, in a conventional thermoelectric conversion element, the output voltage is secured by connecting thermoelectric material elements in series in order to ensure that a load circuit continues to operate after the output voltage reaches saturation, namely, past the voltage peak of the generated electric power in FIG. 2. However, connecting elements in series leads to an increase in internal resistance of the thermoelectric conversion element, making it difficult to secure enough current. Moreover, increasing serial connection results in an increase in size of the thermoelectric conversion element, which causes a problem in that the thermoelectric conversion element is undesirable for portable terminals. In contrast, the power source inverter circuit of the present invention can output a constant voltage to the load circuit 5 because the circuit has the variable DC—DC converter 2, which raises the voltage of electric power generated by the power feeding means 11 when the voltage becomes lower than the operation voltage of the load circuit 5.

The variable DC—DC converter 2 is either a switched capacitor type DC—DC converter which uses a capacitor, or an LC type DC—DC converter which uses a coil.

The switched capacitor type DC—DC converter determines the step-up number or step-down number based on voltage detection information sent from the voltage detector 3, and outputs power after voltage conversion. The switched capacitor type DC—DC converter can raise or drop the voltage inputted by repeating parallel connection or serial connection among capacitors or between capacitors and a

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power supply. FIG. 3A shows a basic step-up circuit of the switched capacitor type DC—DC converter. FIG. 3B is a schematic diagram showing the operation thereof. According to the wire connection of the switched capacitor type DC—DC converter, an input terminal 21 is connected to drains of transistors 22 and 23 while a source of the transistor 22, one of terminals of a capacitor 24, and a drain of a transistor 26 are connected to one another. The other terminal of the capacitor 24 is connected to a source of the transistor 23 and to a drain of a transistor 25. A source of the transistor 25 is grounded. A source of the transistor 26 is connected to one of terminals of a capacitor 27 and to an output terminal 28. The other terminal of the capacitor 28 is grounded.

In raising the voltage, a voltage twice the input voltage can be obtained by connecting the power supply and the capacitors in parallel to each other and then switching it to serial connection between the capacitors and the power supply. Although the description here deals with double boost using capacitors and a power supply, triple or quadruple boost is possible if the number of capacitors is increased. It is also possible to drop the input voltage by using a circuit shown in FIG. 4A and by operating the circuit in a manner illustrated in FIG. 4B. According to the wire connection in the step-down circuit of the switched capacitor type DC—DC converter, an input terminal 31 is connected to a drain of a transistor 32. A source of the transistor 32 is connected to one of terminals of a capacitor 34 and to a drain of a transistor 33. The other terminal of the capacitor 34 is connected to a drain of a transistor 35 and to a drain of a transistor 36. A source of the transistor 35 is grounded. A source of the transistor 36 is connected to a source of the transistor 33, one of terminals of a capacitor 37, and an output terminal 38. The other terminal of the capacitor 37 is grounded.

The LC type DC—DC converter outputs electric power after performing voltage conversion thereon by changing switching timing of internal transistors on the basis of voltage detection information sent from the voltage detector 3. FIG. 5 is a diagram showing a basic step-up circuit of the LC type DC—DC converter. An input terminal 41 is connected to one of terminals of an inductor 44. The other terminal of the inductor 44 is connected to a drain of a transistor 42 and to an anode of a diode 43. A source of the transistor 42 is grounded. A cathode of the diode 43 is connected to an output terminal 45. A voltage is applied to a gate of the transistor 42 to cause a current flow between the source and the drain of the transistor 42, which in turn causes a current flow into the inductor 44. Thereafter, a gate of the transistor 42 is turned off to cut the current flow between the source and the drain. This causes electromagnetic induction and the boosted voltage is outputted through the diode 43. PWM control or PFM control is employed as a control method for turning on and off the gate of the transistor 42. The LC type DC—DC converter is advantageous in that it can output an arbitrary voltage by changing the gate on/off control frequency. On the other hand, the LC type DC—DC converter is disadvantageous in that external parts such as an inductor are needed and that the power conversion efficiency drops when the voltage output is low.

FIG. 6 is a diagram showing a basic step-down circuit of the LC type DC—DC converter. An input terminal 41 is connected to a source of a transistor 52. A drain of the transistor 52 is connected to one of terminals of an inductor 54 and to a cathode of a diode 53. An anode of the diode is grounded. The other terminal of the inductor 54 is connected to an output terminal 55. Similar to the step-up circuit, a gate

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of the transistor 52 is turned on and off by PWM control or PFM control. The thus dropped voltage is applied to cause a current flow between the source and the drain of the transistor 42, which in turn causes a current flow into the inductor 44. Thereafter, the gate of the transistor 42 is turned off to cut the current flow between the source and the drain. This causes electromagnetic induction and the dropped voltage is outputted through the diode 43. PWM control or PFM control is employed as a control method for turning on and off the gate of the transistor 42.

In the case where a switched capacitor type DC—DC converter is employed for the variable DC—DC converter, the switched capacitor type DC—DC converter circuit shown in FIG. 3A or FIG. 4A is combined with a bypass transistor 63 to form a basic block (SC block) 62, and then an input terminal 64 of this SC block 62 is connected to an output terminal 65 of another SC block 62 forming cascade connection as shown in FIG. 7.

Now, the role of the bypass transistor 63 is described. The bypass transistor connects the input terminal 64 of the SC block 62 and a bypass line 61 between its source and drain. A gate electrode of the transistor 63 is connected to a control circuit that is placed inside the variable DC—DC converter circuit. When the bypass transistor 63 is turned on, the input terminal 64 of the SC block 62 is connected to the bypass line 61 and output of the SC block 65 of the preceding stage flows into the bypass line. Therefore, the current is sent to the SC block 62 of the subsequent stage skipping the SC block 62 of this stage.

FIG. 8 shows an example of the operation of the variable DC—DC converter when a switched capacitor type DC—DC converter is employed. For instance, in order to output the voltage of an input terminal 71 to an output terminal 72 as it is, bypass transistors (S1) 73 and (S3) 75 are turned on to bypass two SC blocks 76 and 77. In order to output a voltage twice the voltage of the input terminal 71 to the output terminal 72, the bypass transistor (S1) 73 and a bypass transistor (S2) 74 are turned on to operate one stage of SC block, the step-up SC block 76. In order to output a voltage four times the voltage of the input terminal 71, all the bypass transistors are turned off to operate two stages of SC blocks, the step-up SC blocks 76 and 77.

On the other hand, in the case where an LC type DC—DC converter is employed for the variable DC—DC converter 2, variable output is obtained by connecting the input terminal of the variable DC—DC converter 2 to the input terminal 41 (51) of the LC type DC—DC converter shown in FIG. 5 (FIG. 6) and by connecting the output terminal of the variable DC—DC converter 2 to the output terminal 45 (55) of the LC type DC—DC converter shown in FIG. 5 (FIG. 6). This is advantageous in terms of circuit scale because there is no need to form cascade connection of plural blocks unlike the case where a switched capacitor type DC—DC converter is used for the variable DC—DC converter 2.

The voltage detector 3 is for continuously monitoring the output voltage of the power feeding means 11, the voltage of the capacitor 6, and the input voltage of the load circuit 5, and for sending voltage detection information to the variable DC—DC converter 2 and to the control circuit 4.

The control circuit 4 receives the information from the voltage detector 3 and controls switching of the MOSFET switches (P1) 7 to (P4) 10 that are connected between the blocks of the power feeding means 11, the variable DC—DC converter 2, the load circuit 5, and the capacitor 6.

The transistors of the MOSFET switches (P1) 7 to (P4) 10 connect the blocks to one another and conduct switching



operation upon receiving control signals from the control circuit 4. Here, these transistors are desirably P type transistors. If they are N type transistors, a gate voltage higher than a voltage inputted to a source is required in order to cause a current flow between the source and a drain and therefore another high voltage is necessary to control a gate of each transistor. In contrast, P type transistors can be turned on and off by using the output voltage of the variable DC—DC converter 2 for a gate control signal and accordingly there is no need to generate a high voltage specially for gate control.

The MOSFET switches of the present invention exert even greater effects if fully-depleted SOI devices are used. In a bulk device, a substrate is usually connected to a source of a transistor and, if a MOSFET is used to build a switch in which a current flows in two directions, it is impossible to avoid countercurrent upon inversion of the source side voltage and the drain side voltage. For that reason, a bulk device prevents countercurrent by connecting two transistors as shown in FIG. 9A. In contrast, a fully-depleted SOI device can operate while a substrate (body region) is in a floating state and therefore, as shown in FIG. 9B, is capable of preventing countercurrent with one transistor when a current flows in two directions in the MOSFET switch. Accordingly, the number of transistors can be reduced by employing fully-depleted SOI devices for the MOSFET switches of the present invention.

If the threshold voltage is equal, a fully-depleted transistor is lower in leak current than a bulk device by one digit. Therefore, the threshold voltage can be lowered and the transistor size of the MOSFET switches and an output driver can be reduced. FIG. 10 shows a chip area comparison between a power source inverter circuit of the present invention that is configured using bulk devices and a power source inverter circuit of the present invention that is configured using fully-depleted SOI devices. The graph shows that the use of fully-depleted SOI devices greatly reduces the areas of the MOSFET switches and of the output driver.

The capacitor 6 has a function of storing electric power outputted from the variable DC—DC converter 2 and a function of supplying the input of the variable DC—DC converter 2 with electric power when the power feeding means 11 stops generating electric power.

The load circuit 5 is an application circuit capable of operating on very low electric power. Since the system using the power source inverter circuit 1 of the present invention can operate solely on electric power generated by natural energy, the load circuit 5 is also designed to consume as little power as possible. One of techniques for limiting power consumption as much as possible is a circuit technique that uses a fully-depleted SOI device. Next, a description is given on the operation of the power source inverter circuit 1 according to the present invention. The description given here deals with the operation in the case where a thermoelectric conversion element is used as the power feeding means 11, but the operation also applies to the case where electric power is generated by other power feeding means such as a solar cell or a spiral spring. In this example, it is assumed that the variable DC—DC converter 2 uses a switched capacitor type DC—DC converter and that the voltage is stepped up four times at maximum.

A heat source is put on the thermoelectric conversion element, causing the output voltage to rise. As shown in FIG. 11, when the output voltage of the thermoelectric conversion circuit rises past the quadruple boost point, the voltage detector circuit 3 detects the voltage and sends signals to the

variable DC—DC converter 2 and to the control circuit 4. Receiving the signals, the control circuit 4 turns on the MOSFET switch (P1) 7 out of all the MOSFET switches which have initially been off. This sends electric power to the variable DC—DC converter 2. The variable DC—DC converter 2 starts, upon receiving the signals from the voltage detector circuit 3, power conversion for quadruple boost and outputs the boosted power. Then, the control circuit 4 turns the MOSFET switch (P4) 10 on to send the electric power to the load circuit 5. During this, the voltage detector circuit 3 monitors the voltage of the load circuit 5, and in the case where the voltage exceeds the operation voltage of the load circuit 5, sends a signal to the control circuit 4, which turns the MOSFET switch (P4) 10 off and the MOSFET switch (P3) 9 on. This sends excess electric power which is not used to operate the load circuit 5 to the capacitor 6 to be stored therein. By alternately turning on and off the MOSFET switches (P3) 9 and (P4) 10, a constant voltage is outputted to the load circuit 5 and excess electric power is stored in the capacitor 6.

Next, when the output voltage of the thermoelectric conversion circuit further rises past the double boost point 92, the voltage detector circuit 3 detects the voltage and sends signals to the variable DC—DC converter 2 and to the control circuit 4. The variable DC—DC converter 2 starts, upon receiving the signals from the voltage detector circuit 3, power conversion for double boost and outputs the boosted power. As to the operation of the MOSFET switch, in a manner similar to that in the case of the above quadruple boost, the MOSFET switches (P3) 9 and (P4) 10 are alternately turned on and off, whereby a constant voltage is outputted to the load circuit 5 and excess electric power is stored in the capacitor 6.

Further, when the output voltage of the thermoelectric conversion circuit rises past the no boost point 91, the voltage detector circuit 3 detects the voltage and sends signals to the variable DC—DC converter 2 and to the control circuit 4. The variable DC—DC converter 2 starts, upon receiving the signals from the voltage detector circuit 3, power conversion for Non boost and outputs the power. The operations of the MOSFET switch (P3) 9 and (P4) 10 are similar to those in the case of the above double boost and quadruple boost.

Thereafter, when the output voltage of the thermoelectric conversion circuit becomes lower than the no boost point 91, the variable DC—DC converter carries out power conversion for double boost and outputs the boosted power. When the output voltage becomes lower than the double boost point 92, the variable DC—DC converter carries out power conversion for quadruple boost and outputs the boosted power.

Then, when the output voltage of the thermoelectric conversion circuit becomes lower than the quadruple boost point 93, the voltage detector circuit 3 detects the voltage and sends signals to the variable DC—DC converter and to the control circuit 4. Receiving the signals, the control circuit 4 turns the MOSFET switches (P1) 7, (P3) 9, and (P4) 10 off and the MOSFET switch (P2) 8 on to send the electric power that has been stored in the capacitor 6 to the input of the variable DC—DC converter 2. Receiving the voltage information of the capacitor 6 from the voltage detector circuit 3, the variable DC—DC converter 2 determines the step-up multiple number, conducts power conversion, and outputs the boosted power. At this point, the control circuit 4 turns the MOSFET switch (P4) 10 on to send the electric power to the load circuit 5. During this, the voltage detector circuit 3 monitors the voltage of the load circuit 5, and in the

case where the voltage exceeds the operation voltage of the load circuit 5, sends a signal to the control circuit 4, which turns the MOSFET switch (P4) 10 off. This causes the voltage of the load circuit 5 to start its descent and the voltage detector circuit 3 sends a detection signal to the control circuit 4 to turn the MOSFET switch (P4) 10 on once more. By alternately turning the MOSFET switch (P4) 10 on and off, a constant voltage is supplied to the load circuit 5.

In a power source inverter circuit structured in a manner similar to that of the present invention, it is more often than not that a load circuit is continuously connected to a capacitor. In this case, it takes time to store electric charges in the capacitor after power feeding means begins to output electric power and send it to a variable DC—DC converter. Since the load circuit does not start its operation until electric charges are stored in the capacitor, it is very inconvenient. The power source inverter circuit of the present invention, on the other hand, has the MOSFET switches (P3) 9 and (P4) 10 between the variable DC—DC converter 2 and the capacitor 6 and between the variable DC—DC converter 2 and the load circuit 5, and the MOSFET switches (P3) 9 and (P4) 10 are switched between on and off in accordance with the voltage level of the load circuit 5. Therefore, the power source inverter circuit of the present invention is advantageous in that the load circuit 5 can be put into operation as soon as the power feeding means 11 outputs electric power.

In the case where the power feeding means 11 is a natural energy source, the amount of electric power outputted from the power feeding means 11 is greatly affected by a change in its surroundings. Accordingly, there is no assurance that maximum electric power can be taken out when necessary. The present invention is characterized by a concept that as much electric power as possible should be taken out and stored in the capacitor 6 while the power feeding means has high power generation ability.

The relation between the output voltage of a natural energy source and the current thereof has a local maximal value which leads to the maximum power generation efficiency. When a thermoelectric conversion element is employed, the maximum power generation efficiency is obtained by taking out a current such that the output voltage equals to half the open-circuit output voltage. In a conventional power source inverter circuit where the amount of electric power outputted from power feeding means is determined in accordance with power consumption of a load circuit, electric power is not always taken out with maximum power generation efficiency. In contrast, the power source inverter circuit of the present invention can set the voltage conversion multiple number of the variable DC—DC converter 2 in accordance with the input voltage, and in addition, can store excess electric power in the capacitor 6 when more electric power than is needed by the load circuit 5 is generated. The power source inverter circuit of the present invention thus can always take out electric power with the maximum power generation efficiency of a natural energy source.

The power source inverter circuit 1 of the present invention thus makes it possible to use up every bit of electric power generated by the power feeding means 11 by varying the step-up and step-down multiple numbers of the DC—DC converter and by returning electric power that has been stored in the capacitor to the variable DC—DC converter 2 to send it to the load circuit 5. FIG. 12 shows comparison between the power source inverter circuit of the present invention and a conventional power source inverter circuit where the multiple number is fixed regarding how long the

load circuit 5 continues to operate. The graph shows that the power source inverter circuit of the present invention can hold the operation voltage 1.3 times longer than the conventional DC—DC converter of fixed multiplying factor if the electric power generated is equal.

As has been described, according to the present invention, the power source inverter circuit is provided with: the variable DC—DC converter for raising or dropping the voltage of electric power which is supplied from the power feeding means; the storage means for storing electric power whose voltage has been raised or dropped by the variable DC—DC converter; the MOSFET switch for connecting an output of the power feeding means to an input of the variable DC—DC converter; the MOSFET switch for connecting an output of the variable DC—DC converter to an input of the storage means; the MOSFET switch for connecting the output of the variable DC—DC converter to an input of a load circuit; the MOSFET switch for connecting the input of the variable DC—DC converter to the input of the storage means; the control circuit for controlling gates of the MOSFET switches; and the voltage detector for monitoring the output voltage of the power feeding means, the voltage of the storage means, and the input voltage of the load circuit, and for outputting voltage information to the variable DC—DC converter and to the control circuit. Therefore, the present invention has an effect of outputting a constant voltage to the load circuit even when the output voltage of the feeding means fluctuates.

When the power feeding means is a natural energy source, the relation between the output voltage and the current has a local maximal value which is the maximum power generation efficiency. In contrast to a conventional power source inverter circuit where the amount of electric power outputted from power feeding means is determined in accordance with power consumption of a load circuit, the power source inverter circuit of the present invention structured as above can always take out electric power with the maximum power generation efficiency of a natural energy source and can store excess electric power in the capacitor while consuming the generated electric power in the load circuit.

Moreover, the present invention makes it possible to use up every bit of electric power generated by the power feeding means since excess electric power is stored in the capacitor when more electric power than is needed by the load circuit is generated and outputted from the power feeding means so that the stored electric power is used after the power feeding means stops outputting electric power.

Unlike prior art where electric power stored in storage means is directly connected to a load circuit, the power source inverter circuit of the present invention returns electric power that has been stored in the storage means to the DC—DC converter for voltage conversion. The present invention thus makes it possible to use up electric power without wasting any.

Another effect of the present invention is that the load circuit can start its operation as soon as the power feeding means outputs electric power by placing the MOSFET switches between the output of the variable DC—DC converter and the load circuit and between the output of the variable DC—DC converter and the storage means.

The variable DC—DC converter is composed of cascade connection of blocks each of which is a combination of a switched capacitor type DC—DC converter and a bypass transistor. Accordingly, a higher power conversion efficiency is obtained in a low power consumption IC region.

Another effect of the present invention is that the number of transistors can be reduced by using fully-depleted SOI

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devices for the MOSFET switches. This is because the use of fully-depleted SOI devices makes it possible to prevent countercurrent with one transistor as opposed to a usual bulk device where two transistors are connected in order to avoid countercurrent upon inversion of the source side voltage and the drain side voltage.

The use of fully-depleted SOI transistors provides another effect that the transistor size of the MOSFET switches and the output driver can be reduced. This is because a fully-depleted SOI device is lower in leak current than a bulk device by one digit and the threshold voltage can be lowered.

FIG. 1

POWER FEEDING MEANS  
VOLTAGE DETECTOR  
VARIABLE DC—DC CONVERTER  
CONTROL CIRCUIT  
LOAD CIRCUIT

FIG. 11

NO BOOST

DOUBLE BOOST

QUADRUPLE BOOST

THERMOELECTRIC CONVERSION ELEMENT OUTPUT VOLTAGE

NO BOOST POINT

DOUBLE BOOST POINT

QUADRUPLE BOOST POINT

FIG. 12

CONVENTIONAL DC—DC CONVERTER

POWER SOURCE INVERTER CIRCUIT OF THE PRESENT INVENTION

FIG. 13

POWER FEEDING MEANS  
VOLTAGE DETECTOR  
DC—DC CONVERTER  
STORAGE MEANS  
LOAD CIRCUIT

What is claimed is:

1. A power source inverter circuit comprising:

a variable DC—DC converter for raising or dropping a voltage of electric power which is supplied from power feeding means;

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storage means for storing electric power whose voltage has been raised or dropped by the variable DC—DC converter;

a MOSFET switch for connecting an output of the power feeding means to an input of the variable DC—DC converter;

a MOSFET switch for connecting an output of the variable DC—DC converter to an input of the storage means;

a MOSFET switch for connecting the output of the variable DC—DC converter to an input of a load circuit;

a MOSFET switch for connecting the input of the variable DC—DC converter to the input of the storage means; a control circuit for controlling gates of the MOSFET switches; and

a voltage detector for monitoring an output voltage of the power feeding means, a voltage of the storage means, and an input voltage of the load circuit, and for outputting voltage information to the variable DC—DC converter and to the control circuit.

2. A power source inverter circuit according to claim 1, wherein the variable DC—DC converter is composed of a switched capacitor type DC—DC converter and a bypass transistor, the switched capacitor type DC—DC converter being constituted of four MOSFET transistors and two capacitors, and the bypass transistor having a source terminal connected to an input terminal of the switched capacitor type DC—DC converter and having a drain terminal connected to a bypass line.

3. A power source inverter circuit according to claim 2, wherein the variable DC—DC converter has a plurality of blocks each including the switched capacitor DC—DC converter and the bypass transistor, the blocks being connected through a cascade connection.

4. A power source inverter circuit according to claim 1, wherein the variable DC—DC converter is composed of a MOSFET transistor, an inductor, a capacitor, and a diode.

5. A power source inverter circuit according to claim 1, wherein the MOSFET switches are each composed of a fully-depleted SOI device.

\* \* \* \* \*

# United States Patent [19]

Arakawa

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[45] Date of Patent: Oct. 27, 1987

[54] HIGH VOLTAGE PRECHARGING CIRCUIT

[75] Inventor: Hideki Arakawa, Yokohama, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[21] Appl. No.: 763,628

[22] Filed: Aug. 8, 1985

[30] Foreign Application Priority Data

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[51] Int. Cl.<sup>4</sup> ..... H03K 17/56; H03K 3/01

[52] U.S. Cl. .... 307/246; 307/296 R;  
307/304

[58] Field of Search ..... 307/246, 444, 607, 582,  
307/297, 296 A, 296 R, 304

[56] References Cited

## U.S. PATENT DOCUMENTS

4,390,798	6/1983	Kurafuji	307/297
4,439,692	3/1984	Beekmans et al.	307/297
4,463,273	7/1984	Dingwall	307/443
4,503,345	3/1985	Yamamura	307/605

Primary Examiner—Stanley D. Miller

Assistant Examiner—B. P. Davis

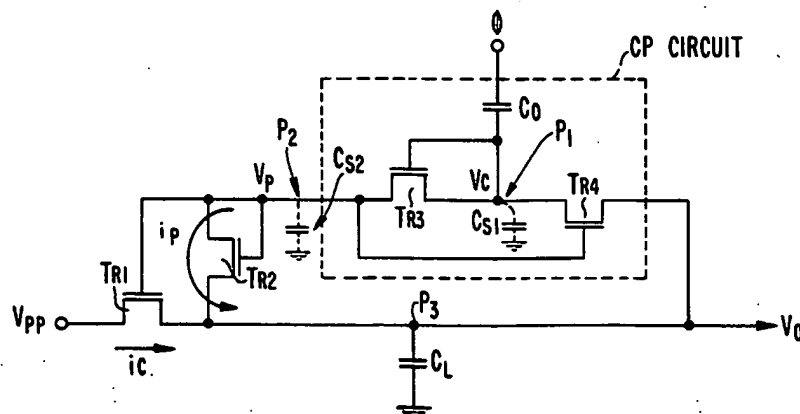
Attorney, Agent, or Firm—Staas & Halsey

[57] ABSTRACT

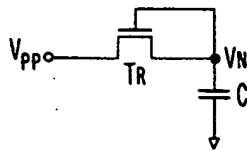
A precharging circuit employing ordinary enhancement (E) types MIST'S produces erasing and writing (E-W) voltages to change the data stored in an EE-

PROM fabricated in a common memory chip with the circuit. The E-W voltage increases gradually from a low level to a high level over a long time interval determined substantially by a long time constant RC circuit, the voltage charge developed on the capacitor C comprising the E-W voltage. The resistor R is implemented by a first MIST connected between a high voltage source and the capacitor C, the gate thereof being controlled by a charge-pump (CP) circuit and a second MIST. The CP circuit is connected between the capacitor C and the gate of the first MIST and is rendered operative during successive clock pulses of a series of clock pulses applied thereto. The CP circuit, during each clock interval, produces a voltage output applied to the first MIST which exceeds the threshold voltage  $V_{th}$  thereof, whereby the first MIST periodically is turned ON for conducting a charging current which flows into the capacitor C. The second MIST is connected between the gate of the first MIST and the capacitor C for suppressing the gate voltage of the first MIST thereby limiting the interval during which the charging current flows therethrough, to a limited portion of each clock pulse interval. The intermittent charging current establishes a long time interval for charging the capacitor C to a value substantially equal to the high voltage source.

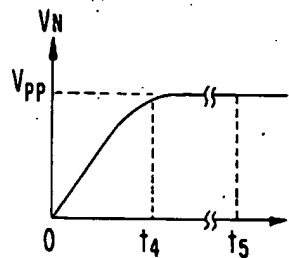
12 Claims, 7 Drawing Figures



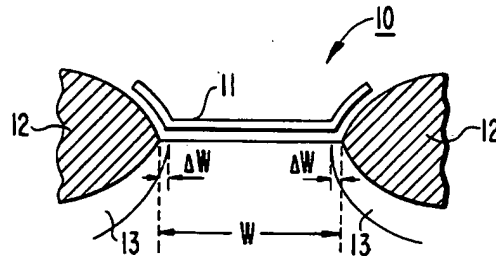
**FIG. 1(a)**  
PRIOR ART



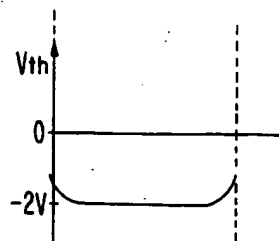
**FIG. 1(b)**  
PRIOR ART



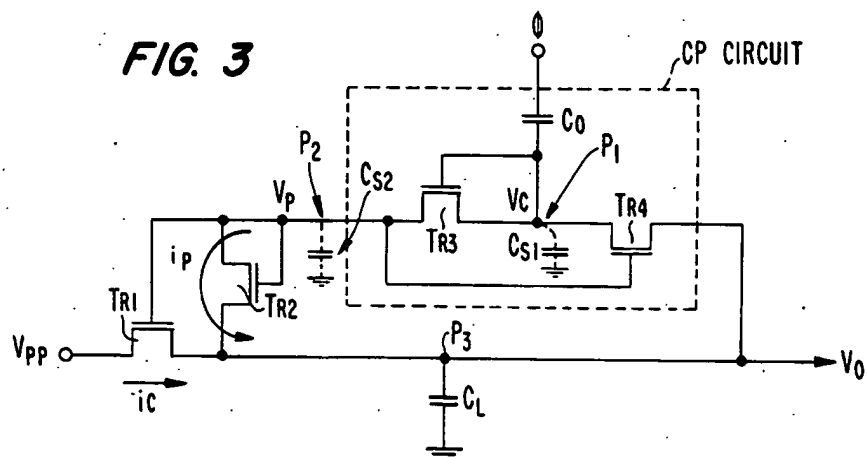
**FIG. 2(a)**



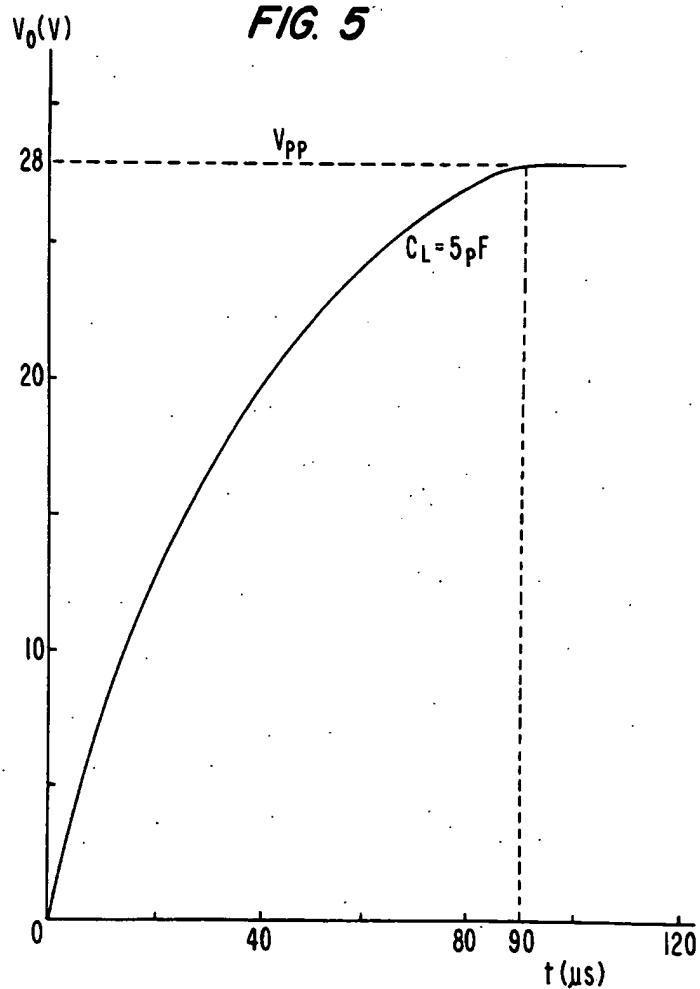
**FIG. 2(b)**



**FIG. 3**



**FIG. 5**



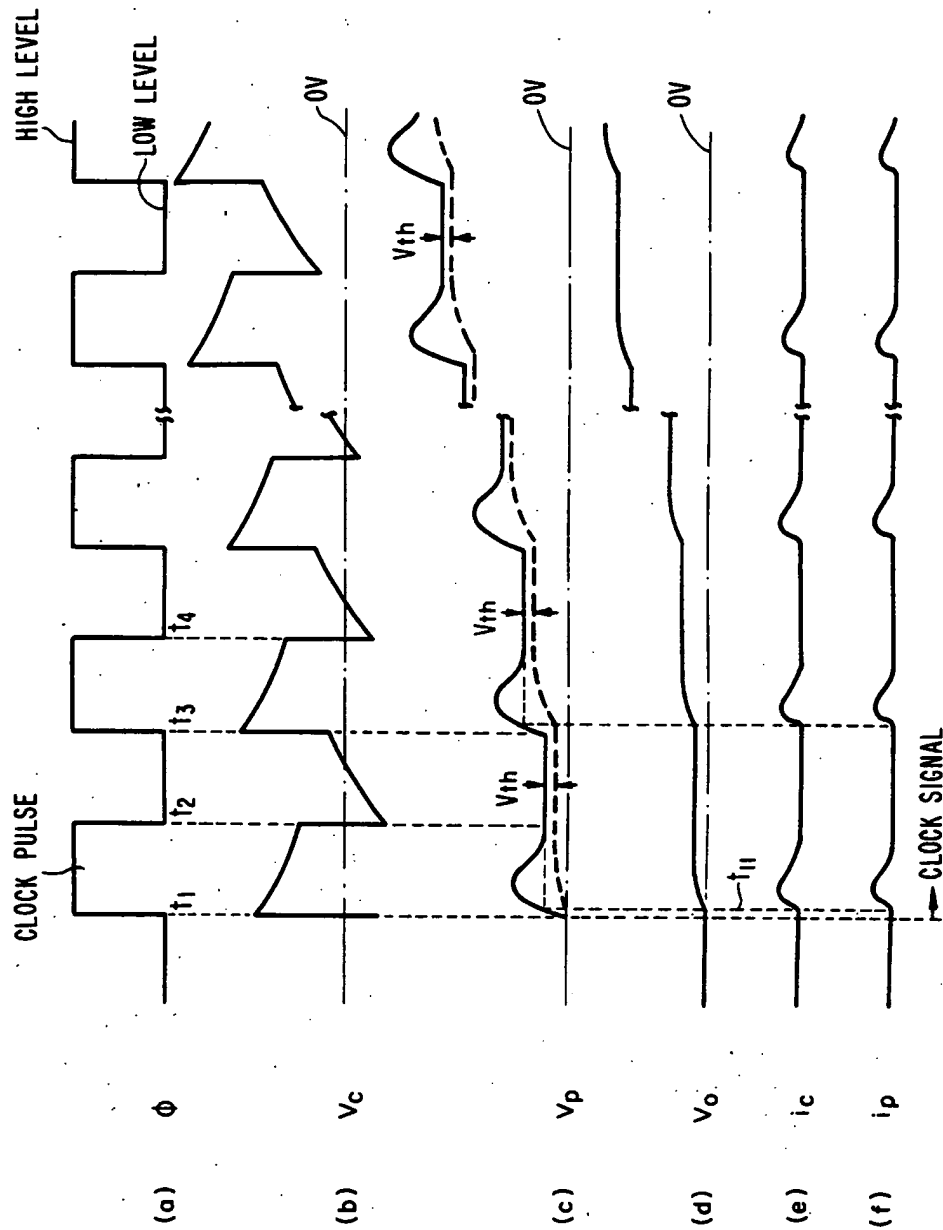


FIG. 4

## HIGH VOLTAGE PRECHARGING CIRCUIT

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present invention relates to a precharging circuit fabricated in an IC (integrated circuit) chip or die, and, more particularly, to such a precharging circuit which may be fabricated using conventional MIST devices and which is small in size, yet affords a long charging time interval.

## 2. State of the Prior Art

A precharging circuit having an extremely large time constant charging characteristic often is required in IC devices. A typical example of the use of such a circuit is for generating an E-W (erasing and writing) voltage, which has a characteristic that it gradually rises in voltage over a long time interval from a low level to a high level, for example, 20-30 volts, in contrast to the ordinary power supply voltage of 5 volts for IC devices. The E-W voltage is used for changing the data stored in an EEPROM (electrically erasable programmable read only memory) or a NOVRAM (nonvolatile random access memory), such as may be fabricated in a common memory chip with the precharging circuit. Typically, the E-W voltage is generated in response to a change command applied to the memory chip from a computer system in which the memory chip is incorporated.

The NOVRAM combines the functions of a static RAM (SRAM) and an EEPROM, so that it operates as a SRAM when the computer system is operating; however, the data in the SRAM is transferred to the EEPROM and stored therein when the power supply for the computer system is turned off. Since the NOVRAM is a special type of EEPROM and since the precharging circuit of the present invention is equally applicable thereto, for convenience, further reference herein shall be limited solely to EEPROM devices, it being understood that such reference encompasses NOVRAM and other similar such devices.

EEPROM devices are used extensively in computer systems, because the data stored therein can easily be changed, particularly by comparison with other EPROM (erasable programmable read only memory) devices. For example, whereas UV-EPROM (ultraviolet rays-controlled EPROM) devices as well have been employed extensively in computer systems, they present certain inconveniences. Particularly, a UV-EPROM memory chip, or a board on which such a memory chip is mounted, must be removed from the computer system to permit irradiating same with ultraviolet rays for erasing the data stored therein when the data must be changed. By contrast, in an EEPROM device, the data can easily be changed electrically, by a program previously provided for that purpose, thus eliminating any need to remove the associated memory chip, or a board on which the chip is mounted, from the computer system.

EEPROM devices, however, present a different problem, namely that the E-W voltage must be applied to the EEPROM for a lengthy time interval, in the range of from 100 micro-sec ( $\mu$ S) to 10 mill-sec (mS), for changing the data therein. Such a time interval is extraordinarily great, particularly in the context of the nanosecond speeds of operation common in the computer field today. Thus, it is difficult to provide such a long time interval, in a computer system. Moreover, the means for establishing the requisite time interval of the

E-W voltage usually are provided in a memory chip; absent that provision, for example, if means external to the chip are employed, the processing speed of the computer system almost invariably will be reduced. As a specific example, if the CPU (central processing unit) of the computer system is employed for this purpose, it would be occupied for an extensive period in generating the lengthy time interval of the E-W voltage for changing the data in the EEPROM, with the result that the overall processing speed of the computer system necessarily would be significantly decreased. Conversely, if the time interval determining means is provided directly on the memory chip, the problem is presented that a significant amount of space on the chip is required therefor, contributing to increased fabricating costs for the chip.

When an E-W voltage having the described, requisite waveform is applied to the EEPROM, electrons or holes are injected into the EEPROM, functioning in accordance with the well known tunneling phenomenon, for erasing or writing data therein; however, if the E-W voltage were to increase rapidly to the high level, the tunnel effect layer fabricated within the EEPROM would break down. Thus, it is critical that the E-W voltage waveform have a gradually rising leading edge, to achieve accurate operations. Consistent therewith, the E-W voltage for an EEPROM typically must have a waveform which rises gradually from a low to a high level over a lengthy time interval, such as from 100  $\mu$ S to 500  $\mu$ S, and then remains at the high level for an extremely long time interval, such as from 5 mS to 10 mS, both for erasing the stored data and for writing new data into the EEPROM.

Typically, a high voltage waveform generator is employed to generate the E-W voltage of the requisite waveform including the gradual leading or rising edge, and a timer circuit controls the long time interval, as is required for erasing and writing operations. Both the waveform generator and the timer circuit are fabricated in the IC chip and have respectively associated therewith a precharging circuit. The typical precharging circuit comprises, essentially, an RC (resistor and capacitor) circuit having a long time constant; moreover, in the timer circuit, the long time interval is determined by the time period from the initiation of the precharging operation to the completion thereof, at which the voltage level of the precharging node (i.e., a circuit node at which the requisite precharging voltage is developed) reaches a predetermined value. A high voltage source establishes the predetermined value for the precharging operation, in order to prolong the time interval.

FIG. 1(a) is a circuit schematic of a prior art precharging circuit. A depletion (D)-type MIST (metal insulator semiconductor transistor)  $T_R$  functions as the resistor (R) of the RC time constant charging circuit, and is connected between a high voltage source  $V_{pp}$  and a capacitor C. A charging current flows from the high voltage source  $V_{pp}$  through transistor  $T_R$  to the capacitor C, producing a precharging voltage  $V_n$  at the circuit node, or connection, between transistor  $T_R$  and capacitor C, which voltage  $V_n$  increases with time, as shown in FIG. 1(b). In particular, the precharging voltage  $V_n$  increases from essentially zero volts (0 V) to a value slightly less than that of the high voltage source  $V_{pp}$  over the time interval  $t=0$  to  $t=t_4$ . The voltage  $V_n$  thereafter asymptotically approaches that of the high voltage source  $V_{pp}$  over the time interval  $t=t_4$  to  $t=t_5$ .



For purposes of erasing data stored in an EEPROM, the time interval  $t=0$  to  $t=t_4$  is approximately from 100  $\mu$ S to 500  $\mu$ S; for the case of writing new data into an EEPROM, the time interval  $t=0$  to  $t=t_5$  is 5 mS to 10 mS. The specific time intervals employed for the respective erasing and writing operations, within the indicated ranges, are dependent upon the characteristics of the particular EEPROM.

As before noted, a precharging circuit as shown in FIG. 1(a) may be associated with each of a high voltage waveform generator and a timer circuit, which respectively function as hereinbefore set forth. Each of the high voltage waveform generator and the timer circuit are triggered by the E-W control signals applied externally to the EEPROM chip by the computer system. Typically, a high voltage in the range of 25 V (volts) is required for generating the long time interval in the RC circuit, and typically is supplied from a high voltage source fabricated in the IC chip. Particularly, the high voltage source comprises a clock oscillator and a charge-pumping circuit, the clock oscillator generating a clocking signal, or train, comprising series of clock pulses, the charge-pumping circuit functioning under the control of the clock pulses to produce the requisite high voltage.

Prior art precharging circuits of the type shown in FIG. 1(a) however, present problems as to the fabrication of the capacitor C and the transistor  $T_R$ , with associated operational problems. Particularly, capacitor C must have a quite large value of capacitance, such as greater than 10 picofarad (pF) for obtaining a sufficiently long time constant, such as in the range of from 10  $\mu$ S to 10 mS; further, since the dielectric material of the capacitor C is afforded by an insulating layer (typically silicon dioxide), the layer must be of substantial thickness so as to withstand the high voltage to be developed. As a result, the capacitor must be of substantial size, for example, from a minimum of  $100 \times 100 \mu\text{m}^2$  to  $400 \times 400 \mu\text{m}^2$  ( $\mu\text{m}$ =micro meter).

The transistor  $T_R$  as well presents problems in its fabrication, in view of its operating characteristics in relation to the conditions imposed by the RC precharging circuit, as illustrated in FIG. 1(a). Particularly, as the precharge voltage  $V_n$  increase in amplitude, it imposes an increasing level of back bias voltage on transistor  $T_R$  which functions to turn transistor  $T_R$  OFF (i.e., render it nonconducting), prior to the precharging voltage  $V_n$  increasing to the level of the high voltage source  $V_{pp}$ , if transistor  $T_R$  is an ordinary depletion (D) type transistor having an ordinary threshold voltage  $V_{th}$ . Accordingly, conventional D type MIST devices cannot be used in a precharging circuit as shown in FIG. 1(a), since the precharging voltage  $V_n$  cannot increase to the requisite level approaching  $V_{pp}$ ; thus, the required long time interval as well cannot be achieved.

Accordingly, a modified transistor  $T_R$  must be employed, known as a special D type MIST (or, also, as a modified MIST), which has a very low threshold voltage  $V_{th}$ —meaning a threshold  $V_{th}$  of a large absolute, but negative polarity, value. Such a modified MIST is very expensive, because its fabrication requires use of a special mask and ion implantation processes, for isolating it from other, conventional MIST's which may be adjacent to it in a memory chip. Particularly, the ion implantation is required for lowering the threshold voltage  $V_{th}$ .

The use of a modified MIST, moreover, presents additional problems in view of the necessary relation-

ship between channel width (W) and channel length (L). Particularly, as is well known, the current-voltage characteristic of a MIST (i.e., the characteristic relationship between the source-drain current and the gate-source voltage of the MIST) is such that the ratio of the source-drain current to the gate-source voltage is in proportion to the ratio W/L. Since the size (i.e., area on the chip) of a MIST depends mostly on the required channel length (L), to maintain a given current-voltage characteristic, factors affecting the channel width (W) correspondingly will affect the channel length (L) so as to maintain the required W/L ratio, and accordingly affect the required size of a MIST.

Thus, to minimize the size of the MIST, it is desirable to minimize the channel width (W)—i.e., to employ a narrow channel width (W). However, it is difficult to reduce the channel width (W) of a modified MIST to a value less than, or more narrow than, approximately 4  $\mu\text{m}$ . In general, this difficulty is presented in view of the necessary process steps performed in fabricating a MIST. Particularly, a channel cut is formed around the MIST by implanting boron ions ( $B^+$ ) around the field oxide layer (FOX) used as the source and the drain of the MIST, to avoid producing parasitic transistors in the chip. The boron ions thus implanted, however, tend to diffuse out beyond the channel cut and into surrounding portions of the chip, during thermal diffusion process steps.

The problems attendant fabrication of a modified MIST are more fully understood with reference to FIGS. 2(a) and 2(b), FIG. 2(a) comprising a cross-sectional view, in somewhat simplified schematic form, of such a modified MIST and FIG. 2(b) illustrating the corresponding threshold voltage  $V_{th}$  characteristic, in relation to the configuration of the MIST and its channel width (W) as shown in FIG. 2(a). Particularly, the modified MIST 10 of FIG. 2(a) comprises a gate electrode 11, FOX layer 12, and boron doped regions 13 associated with the FOX layer 12. The channel width (W) of the MIST 10 schematically is illustrated to extend between the boundaries between the portions of the FOX 12 and the substrate underlying the gate electrode 11. The boron doped regions 13, however, overlap the peripheral portions of the channel width (W), which overlapped portions are designated  $\Delta W$ . The threshold voltage  $V_{th}$  of modified MIST 10 is higher in the overlapped portions  $\Delta W$  of the channel width (W), than in the central or nonoverlapped portions ( $W-2\Delta W$ ). Stated alternatively, and with reference to the designations in FIG. 2(a), the combined overlapped portions ( $2\Delta W$ ) presents a high threshold voltage  $V_{th}$  relative to the nonoverlapped portion ( $W-2\Delta W$ ) having the desired, low threshold voltage  $V_{th}$ . FIG. 2(b) illustrates the voltage threshold characteristic  $V_{th}$  in relation to the channel width (W); as is readily seen therein, the threshold  $V_{th}$  increases in the regions corresponding to the overlapped portions  $\Delta W$ .

Thus, since the size of the overlapped portions,  $2\Delta W$ , is a function of the required level of ion implantation represented by the boron doped regions 13, if the total width W is too narrow, the resulting threshold voltage  $V_{th}$  is too high. Particularly, the portion  $2\Delta W$  having the high threshold voltage  $V_{th}$  becomes superior to, or predominates, the central, nonoverlapped portion ( $W-2\Delta W$ ) having the low threshold voltage  $V_{th}$ , out of the total channel width (W). Thus, it is difficult to fabricate a modified MIST which has a low threshold

voltage  $V_{th}$ , unless the channel width (W) is of substantial width.

For the reasons above explained, therefore, the channel width (W) of a modified MIST cannot be made narrow and as a result, to maintain a required ratio W/L to provide the requisite current-voltage characteristic, the channel length (L) as well must be large. Typically, the channel length (L) of a modified MIST must be in the range of from 100  $\mu\text{m}$  to 1,000  $\mu\text{m}$ , to achieve a time constant greater than 100  $\mu\text{s}$  for the RC precharging circuit. Thus, it has been impossible in the prior art to fabricate a capacitor C and a transistor  $T_R$  which are small in size and yet satisfy the requirements of a precharging circuit as in FIG. 1(a) above discussed; in fact, it has been difficult to achieve a long time interval, such as 10 mS, even where a transistor  $T_R$  has a channel length as great as 100  $\mu\text{m}$  and the capacitor C is of a size, or area, as great as 400  $\times$  400  $\mu\text{m}^2$ .

The channel length (L), moreover, presents yet another problem imposing practical limitations on successful implementation of the prior art circuits. Particularly, when the temperature of a memory chip increases, as is typical in normal operation, a leakage current which flows in a junction of the MIST correspondingly tends to increase. The leakage current must be compensated by causing a compensating current flow through the channel of the MIST. However, an adequate compensating current cannot be made to flow when the channel length (L) is as great as 1,000  $\mu\text{m}$ . As a result, to obtain the requisite long time interval, the only possibility is to increase the capacitance of capacitor C. However, increasing the capacitance imposes the necessary requirement of increasing the size of the capacitor C, and therefore the size of the memory chip.

Thus, precharging circuits of the prior art present serious problems in implementation, both as to cost and as to size; moreover, such prior art precharging circuits do not afford the high degree of reliability in operation which is desired.

#### SUMMARY OF THE INVENTION

An object of the present invention, therefore, is to provide a precharging circuit having a relatively slow charging rate characteristic with respect to its size.

A further object of the invention is to provide an improved precharging circuit having a long charging time interval, for use in an erase-write voltage generator or a timing circuit, such as are employed to change the data of an EEPROM or an NOVRAM and which are fabricated in a common memory chip therewith.

A further object of the present invention is to provide a precharging circuit for charging a capacitor to a relatively high voltage, without employing a special depletion type MIST.

Yet another object of the present invention is to provide an improved precharging circuit which enables use of a charging capacitor of conventional capacitance value, but which affords a relatively slow charging rate characteristic.

Still another object of the present invention is to provide a precharging circuit of decreased size, yet which provides a relatively slow charging rate characteristic.

Still a further object of the present invention is to provide an improved precharging circuit of decreased fabrication cost.

Still a further object of the present invention is to provide a precharging circuit affording improved accu-

racy in the control of a long time interval produced thereby.

Still another object of the present invention is to provide a precharging circuit having a circuit configuration and related physical implementation which afford improved reliability in operation.

The precharging circuit of the present invention comprises, as basic components, a charge-storing capacitor, a first MIS transistor (MIST 1) for precharging the capacitor, a charge-pump circuit, and a voltage suppressing means which, in cooperation with the charge-pump circuit, controls the gate voltage of the MIST 1. The charge-pump circuit is driven by a series of clock pulses and generates a succession of incrementally higher voltage levels with reference to the voltage level developed at a precharging node to which the capacitor is connected. Each such incrementally higher voltage level thus obtained is applied to the gate of the MIST 1 to turn it on and thereby causes a small precharging current to flow through the MIST 1 to the precharging capacitor. During the precharging operation, the voltage at the gate of the MIST 1 is increased along with the increase of the precharging voltage as produced by the charge-pump circuit under control of the series of clock pulses which is applied thereto.

The voltage suppressing means preferably comprises a second MIS transistor (MIST 2) having both its gate and source connected to the gate of the MIST 1, and a drain connected to the precharging node. Advantageously, both MIST 1 and MIST 2 are produced in a common IC chip and thus have substantially the same threshold voltage characteristic. In this configuration, MIST 2 suppresses the voltage applied to the gate of MIST 1 from the charge-pump circuit, so that the charging current flows only during short time intervals corresponding to the timing of the clock pulses.

Since the charge-pump circuit uses the precharging voltage developed on the precharging capacitor as a source voltage, as each clock pulse is applied, the output voltage applied to the gate of MIST 1 always exceeds the threshold voltage of MIST 1. Thus, MIST 1 may comprise an ordinary or conventional enhancement type MIST, even as the level of the precharging voltage undergoes a substantial increase, from a low level to a high level, over a long time interval. Since the charging current which flows intermittently through MIST 1 is limited to a small value, the precharging circuit can generate an erase-write voltage having a long time interval, even though employing a precharge capacitor having a small capacitance value.

Thus, in accordance with the present invention, the precharging circuit may afford a very long time interval while using only a capacitor of small capacitance value and ordinary enhancement MIS transistors (i.e., MIST 1 and MIST 2). Further, through association of the charge-pump circuit with the precharging circuit, MIST 1 is effective for controlling the charging current, even though the MIST 1 is subjected to a substantial reverse bias voltage.

These and other objects and advantages of the present precharging circuit of the present invention will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings, to which reference is now made.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a circuit schematic of a prior art precharging circuit;

FIG. 1(b) is a plot of the increasing precharging voltage level developed on a storage capacitor of the prior art precharging circuit of FIG. 1(a);

FIG. 2(a) is a cross-sectional, simplified and schematic view of a MIS transistor;

FIG. 2(b) is an illustrative plot of the threshold voltage across the channel width (W) of the illustrative MIST of FIG. 2(a);

FIG. 3 is a circuit schematic of a precharging circuit in accordance with the present invention;

FIGS. 4(a) through 4(f) are plots of waveforms of clock pulses, voltages developed at specific nodes of the circuit of FIG. 3, and of currents flowing within various branches of the circuit of FIG. 3 during operation; and

FIG. 5 is a plot of the increase in level of the precharging voltage relative to time, as produced by the precharging circuit of the invention in accordance with the circuit schematic of FIG. 3.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 3 is a circuit schematic of a precharging circuit in accordance with the present invention, as may be fabricated in a memory chip which incorporates therein, as well, an EEPROM or a NOVRAM. As before noted, since a NOVRAM incorporates the functions of an EEPROM, reference hereinafter shall be limited to an EEPROM but shall be understood to include and encompass a NOVRAM or other equivalent device implemented in a memory chip, as well. Consistent with a significant object of this invention, transistors  $T_{R1}$  through  $T_{R4}$  are conventional enhancement (E) type N channel MIS transistors.

Transistor  $T_{R1}$  and precharging capacitor  $C_L$  comprise a long time constant RC circuit. A charging current  $i_c$  flows from a high voltage source  $V_{pp}$  through transistor  $T_{R1}$  to the precharging (i.e., charge storing) capacitor  $C_L$ , producing a precharging output voltage  $V_o$  at the precharging node  $P_3$ . Node  $P_3$  comprises the common junction of transistor  $T_{R1}$ , capacitor  $C_L$ , and also the voltage output of the circuit; more particularly, the output voltage  $V_o$  developed at node  $P_3$  may comprise an erase-write (E-W) voltage.

Components of the charge-pump (CP) circuit of FIG. 3 are enclosed in a dotted line rectangle and include a coupling capacitor  $C_0$ , and transistors  $T_{R3}$  and  $T_{R4}$  connected together at a common node  $P_1$ . Consistent with conventional notation, a capacitor  $C_{S1}$  connected by phantom lines between the node  $P_1$  and ground represents stray capacitance which exists, for example, due to the gate capacitance of transistor  $T_{R3}$ . The CP circuit is connected between the precharging node  $P_3$  and through node  $P_2$  to the gate of transistor  $T_{R1}$ , the transistors  $T_{R3}$  and  $T_{R4}$  being series connected at node  $P_1$  therebetween. Further, a transistor  $T_{R2}$  is connected at its source and gate to node  $P_2$  and at its drain to node  $P_3$ . The precharging voltage  $V_o$  developed at node  $P_3$  is applied to the CP circuit as a source voltage, and the output voltage,  $V_p$ , of the CP circuit is applied to node  $P_2$ .

The function of the CP circuit will be explained with reference to FIGS. 4(a) through 4(f) which show various waveforms of the timing pulses applied to, and the resultant voltages and currents produced within, the circuit of FIG. 3. Particularly, FIG. 4(a) is a waveform of a train of clock pulses  $\phi$  which is applied to the capacitor  $C_0$  of the CP circuit as seen in FIG. 3. FIG. 4(b) is a plot of the waveform of voltage  $V_c$  developed at

node  $P_1$  in the CP circuit. FIG. 4(c) is a plot of the waveform of the output voltage  $V_p$  of the CP circuit, produced at node  $P_2$ . FIG. 4(d) is a plot of the precharging voltage  $V_o$  produced at node  $P_3$ , constituting the output voltage of the precharging circuit of FIG. 3. FIG. 4(e) is a plot of the waveform of the current  $i_c$  comprising the charging current which flows intermittently through the transistor  $T_{R1}$  for charging capacitor  $C_L$ , in FIG. 3. Finally, FIG. 4(f) is a plot of the waveform of the source-drain current  $i_p$  of the transistor  $T_{R2}$  of FIG. 3.

The precharging circuit of the invention, including the CP circuit, remains inoperative as long as data stored in the associated EEPROM is not to be changed. However, when the memory chip incorporating the EEPROM and the precharging circuit of the invention receives a command from its associated computer system to change data stored therein, the clock pulse train, or signal,  $\phi$  is applied to the CP circuit, which then initiates operation. The clock signal  $\phi$  may be supplied by a conventional clock pulse oscillator which is fabricated in the memory chip in accordance with well known prior art techniques.

In the initial condition of the circuit of FIG. 3, the voltage  $V_p$  at node  $P_2$  is low, e.g., zero volts (0 V); as a result, transistors  $T_{R3}$  and  $T_{R4}$  are cut off. With concurrent reference to the waveforms of FIGS. 4(a) through 4(f), when a first clock pulse  $\phi$  of FIG. 4(a) is applied, at time  $t_1$ , the voltage  $V_c$  at node  $P_1$  simultaneously rises, as shown in FIG. 4(b), to a level approaching the amplitude of the clock pulse—for example,  $V_c$  may reach the voltage level of +4.8 V for a clock pulse amplitude of +5 V. The ratio between the level attained by voltage  $V_c$  and the clock pulse  $\phi$  amplitude is determined by the ratio of the capacitance of capacitor  $C_0$  to the stray capacitance  $C_{S1}$  which exists at node  $P_1$  due to the gate capacitance of transistor  $T_{R3}$ , for example. The result is that transistors  $T_{R3}$  and  $T_{R4}$ , respectively, are switched ON and OFF, the ON transistor  $T_{R3}$  then conducting, or transferring, the charge on stray capacitance  $C_{S1}$  to stray capacitance  $C_{S2}$ , the latter existing at node  $P_2$  because of the gate capacitance of transistors  $T_{R1}$  and  $T_{R2}$ , for example. Likewise, beginning at time  $t_1$ , the voltage  $V_p$  at node  $P_2$  begins to increase, as shown in FIG. 4(c), and correspondingly the voltage  $V_c$  at node  $P_1$  begins to decrease, as seen by comparison of FIGS. 4(b) and 4(c). The rates of increase of voltage  $V_p$  and of decrease of the voltage  $V_c$  are relatively slow because of the source-drain resistance of transistor  $T_{R3}$ .

When voltage  $V_p$  increases to a level exceeding the threshold voltage  $V_{th}$  of transistor  $T_{R1}$ , transistor  $T_{R1}$  turns ON and permits the charging current  $i_c$  to flow from high voltage source  $V_{pp}$  to the precharging capacitor  $C_L$ . More particularly, with reference to FIGS. 4(c) through 4(f), the rising level of the voltage  $V_p$  is shown to exceed the threshold voltage level  $V_{th}$  at time  $t_{11}$ , whereupon the charging current  $i_c$  begins to flow. The resultant charging of the precharging capacitor  $C_L$  correspondingly causes the voltage  $V_o$  at node  $P_3$  to increase, as seen in FIG. 4(d). Transistor  $T_{R2}$ , however, suppresses the extent of, or limits, the increase in the voltage  $V_p$ . Particularly, when the level of voltage  $V_p$  exceeds the threshold voltage  $V_{th}$  of transistor  $T_{R2}$ , transistor  $T_{R2}$  turns ON, causing a source-drain current  $i_p$  to flow through transistor  $T_{R2}$  to the precharging capacitor  $C_L$ , as shown in FIG. 4(f). Correspondingly, as the current  $i_p$  flows, the voltage  $V_p$  at node  $P_2$  decreases, as shown in FIG. 4(c), thereby turning transis-

tors  $T_{R1}$  and  $T_{R2}$  OFF. When OFF, transistor  $T_{R1}$  no longer permits the flow of current  $i_c$  which then terminates, as seen in FIG. 4(e). Thus, as seen by comparison of FIG. 4(a) and FIG. 4(f), the current  $i_c$  flows only during the limited conducting period of transistor  $T_{R1}$  corresponding to a portion of the duration of the positive clock pulse between  $t_1$  and  $t_2$ .

The trailing edge of the positive clock pulse occurring at time  $t_2$  causes the voltage  $V_c$  at node  $P_1$  to fall rapidly, as shown in FIG. 4(b), with the result that transistors  $T_{R3}$  and  $T_{R4}$  are switched OFF and ON, respectively. The rapid drop in the level of voltage  $V_c$  is accompanied by a rapid negative charge being developed on stray capacitance  $C_{s1}$ , which then is gradually discharged by a discharge current which flows from the charging capacitor  $C_L$  through transistor  $T_{R4}$ . As seen in FIG. 4(b), however, voltage  $V_c$  has a mean value which increases gradually during the successive clock pulses. This results because the discharging current flowing through transistor  $T_{R4}$  is supplied from the precharging capacitor  $C_L$  which, likewise in successive clock pulses, produces the precharging voltage  $V_o$  which incrementally increases with successive clock pulses.

On the other hand, the rapid drop in the level of voltage  $V_c$ , such as at time  $t_2$ ,  $t_4$ , etc., causes transistor  $T_{R3}$  to be rapidly turned OFF. As a result, the rapid drop in the level of voltage  $V_c$  has almost no influence on the voltage  $V_p$  which therefore remains substantially at its value established during the preceding clock pulse, as seen by comparison of the waveform of voltage  $V_p$  in FIG. 4(c) during time interval  $t_2$  with that during time interval  $t_1$ , during time interval  $t_4$  with that of time interval  $t_3$ , and so forth. While, in fact, the rapid drop in the level of voltage  $V_c$  is transferred to node  $P_2$  through the gate capacitance of transistor  $T_{R3}$ , that gate capacitance is insignificant in comparison with the stray capacitance  $C_{s2}$ , such that the drop in voltage  $V_c$  has no meaningful effect on the value of voltage  $V_p$  at node  $P_2$ . Thus, the voltage  $V_p$  maintains transistors  $T_{R1}$  and  $T_{R2}$  OFF, such as during time interval  $t_2$ , until the next clock pulse occurs at time  $t_3$ .

During the next clock pulse initiating at time  $t_3$ , and correspondingly for each successive clock pulse, the precharging circuit operates in the manner hereinbefore described. Accordingly, the precharging voltage  $V_o$  incrementally increases in level for the successive clock pulses, as shown in FIG. 4(d), until the level of  $V_o$  approaches that of the high voltage source  $V_{pp}$ . Thus, a long time interval is obtained for the charging function, even though the capacitance of the precharging capacitor  $C_L$  is small.

When the precharging circuit of the invention is employed as a timer circuit, the end point, or completion, of the precharging operation is determined in accordance with the voltage  $V_o$  at node  $P_1$  reaching a predetermined voltage level, as may readily be achieved by any suitable prior art voltage level detecting circuit. When this condition is detected, a reset circuit (not shown), which may be of a conventional prior art design, resets the voltage  $V_p$  at node  $P_2$  and  $V_o$  at node  $P_1$  to the initial level of substantially 0 V, such as by discharging the associated capacitor.

The precharging circuit of the invention functions to assure that transistors  $T_{R1}$  and  $T_{R2}$  are always turned ON at the leading edge of each successive clock pulse, because the voltage  $V_p$  is always adjusted to a level just less than the sum of the voltages  $V_o + V_{th}$  during the

low level of the clock signal (e.g., at the time interval  $t_2$ ). Therefore, a special D type MIST requiring an ion implantation mask for its fabrication, as before described, is not necessary for implementing the function of transistors  $T_{R1}$  and  $T_{R2}$  and instead an ordinary E type MIST is sufficient. Likewise, ordinary E type MIST devices may be employed as transistors  $T_{R3}$  and  $T_{R4}$  in the CP circuit.

FIG. 5 is a graph representing a simulation of the charging operation of the precharge circuit of the invention. The results are indicated for the circuit in a simulated implementation wherein:  $V_{pp} = 28$  V; precharging capacitor  $C_L$  has a capacitance of 5 pF; the clocking signal has a frequency of 8 MHz (mega-Hertz) and an amplitude of 5 V; the ratio of channel width to length,  $W/L$ , for transistors  $T_{R1}$ ,  $T_{R3}$  and  $T_{R4}$ , is 4  $\mu\text{m}/4 \mu\text{m}$  and for transistor  $T_{R2}$  is 4  $\mu\text{m}/16 \mu\text{m}$ ; and the ratio of width to length of the coupling capacitor  $C_0$  is 20  $\mu\text{m}/20 \mu\text{m}$ . These conditions are consistent with the use of ordinary E type MIST's for all transistors of the precharging circuit of FIG. 3, as before noted. Further, the value of 5 pF for the precharging capacitor  $C_L$  is standard and thus a MIST having a channel dimension of 100  $\mu\text{m}$  width ( $W$ )  $\times$  100  $\mu\text{m}$  length ( $L$ ) and employing a capacitor having a dielectric of silicon dioxide ( $\text{SiO}_2$ ) and a thickness of 600 Å (Angstroms) may be employed. FIG. 5 more specifically is a plot of the precharging voltage  $V_o$  relative to time, in microseconds, for these conditions and reveals that a precharging time of 90  $\mu\text{s}$  is afforded, at which time the voltage  $V_o$  developed on the charging capacitor  $C_L$ , of only 5 pF, approaches substantially the level of the high voltage  $V_{pp} = 28$  V. Moreover, the time required for completion of the precharging function can be controlled by varying the characteristics of the transistors  $T_{R1}$  and  $T_{R2}$  and/or the capacitance of the coupling capacitor  $C_0$  in accordance with conventional RC time constant circuit determinations.

Numerous modifications and adaptations of the precharging circuit of the invention will be apparent to those of skill in the art and thus is intended by the appended claims to cover all such modifications and adaptations which fall within the true spirit and scope of the invention.

What is claimed is:

1. A precharging circuit for charging a precharging node to a high voltage level, relative to ground potential, from a high voltage source under control of a series of clock pulses, successive clock pulses being separated by corresponding interim time intervals and each clock pulse having a leading edge and a trailing edge defining therebetween a corresponding clock pulse time interval, comprising:

- a precharging capacitor connected between said precharging node and ground for developing a voltage at the precharging node having a level which incrementally increases to a high voltage level approaching that of the high voltage source;
- a first MIS transistor having a gate, a source and a drain, one of said source and drain being operatively connected to the high voltage source and the other of said source and drain being operatively connected to said precharging node, said first MIS transistor having a predetermined threshold voltage for conduction;
- a further node;
- a charge-pump circuit operatively connected between said precharging node and through said

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further node to said gate of said first MIS transistor;

means for applying a series of clock pulses to said charge-pump circuit, said charge-pump circuit responding to each of said clock pulses to generate a voltage at said further node which has a higher level than the predetermined threshold voltage for conduction of said first MIS transistor, relative to the currently existing voltage level at said precharging node, thereby to turn said first MIS transistor on and permit a flow of charging current therethrough from said high voltage source to said precharging capacitor thereby to produce an increase in the voltage level at the precharging node; and

voltage suppressing means having a predetermined threshold value for operation and operatively connected between said further node and said precharging node and responsive to said higher level voltage at said further node exceeding the voltage at said precharging node by said predetermined threshold value for operation of said voltage suppressing means so as to reduce the voltage level at said further node and turn said first MIS transistor off, said first MIS transistor thus being turned on only for a portion of the respective clock pulse time interval of each of successive clock pulses applied to said charge-pump circuit to permit corresponding, incremental flows of charging current to said precharging capacitor for charging said precharging node to a voltage level approaching that of said high voltage source.

2. A precharging circuit as recited in claim 1, wherein said first MIS transistor is of the enhancement type.

3. A precharging circuit as recited in claim 1, wherein said voltage suppressing means comprises a second MIS transistor having a gate, a source and a drain, said gate and drain of said second MIS transistor being operatively connected to said further node and said source of said second MIS transistor being operatively connected to said precharging node.

4. A precharging circuit as recited in claim 1, wherein said first and second MIS transistors are of the enhancement type.

5. A precharging circuit for charging a precharging node to a high voltage level, relative to ground potential, from a high voltage source under control of a series of clock pulses, successive clock pulses being separated by corresponding interim time intervals and each clock pulse having a leading edge and a trailing edge defining therebetween a corresponding clock pulse time interval, comprising:

- a precharging capacitor connected between said precharging node and ground for developing a voltage at said precharging node having a level which incrementally increases to a high voltage level approaching that of the high voltage source;
- a first MIS transistor having a gate, a source and a drain, one of said source and drain being operatively connected to the high voltage source and the other of said source and drain being operatively connected to said precharging node, said first MIS transistor having a predetermined threshold voltage for conduction;
- a further node;
- a charge-pump circuit operatively connected between said precharging node and through said further node to said gate of said first MIS transistor;

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tor, said charge pump circuit comprising a coupling capacitor having first and second terminals, first means connected between said second terminal of said coupling capacitor and said further node and second means operatively connected between said precharging node and said second terminal of said coupling capacitor;

means operatively connected to said first terminal of said coupling capacitor for applying a series of clock pulses to said charge-pump circuit, said first means of said charge-pump circuit responding to each said clock pulse for permitting a current to flow from said second terminal of said coupling capacitor to said further node during the corresponding clock pulse interval and said second means being responsive to the trailing edge of each said clock pulse for permitting a current to flow from said precharging node to said second terminal of said coupling capacitor during the interim time interval preceding a next successive clock pulse, to generate a voltage at said further node which has a higher level than the voltage level at said precharging node and thereby to turn said first MIS transistor on and permit a flow therethrough of charging current from said high voltage source to said precharging capacitor thereby to produce an increase in the voltage level at the precharging node; and

voltage suppressing means having a predetermined threshold value for operation and operatively connected between said further node and said precharging node and responsive to said higher level voltage at said further node exceeding the voltage level at said precharging node by said predetermined threshold value for operation of said voltage suppressing means so as to reduce the voltage level at said further node and turn said first MIS transistor off, said first MIS transistor thus being turned on only for a portion of the clock pulse time interval of each of successive clock pulses applied to said charge-pump circuit to permit corresponding, incremental flows of charging current to said precharging capacitor for charging said precharging node to a voltage level approaching that of said high voltage source.

6. A precharging circuit as recited in claim 5, wherein said first means comprises a third MIS transistor having a gate operatively connected to said second terminal of said capacitor, a source and a drain, one of said source and drain being connected to said second terminal of said capacitor and the other of said source and drain being connected to said further node.

7. A precharging circuit as recited in claim 5, wherein said second means comprises a fourth MIS transistor having a gate connected to said further node, a source and a drain, one of said source and drain of said fourth MIS transistor being connected to said second terminal of said capacitor and the other of said source and drain of said fourth MIS transistor being connected to said precharging node.

8. A precharging circuit as recited in claim 6, wherein said second means comprises a fourth MIS transistor having a gate connected to said further node, a source and a drain, one of said source and drain of said fourth MIS transistor being connected to said second terminal of said capacitor and the other of said source and drain of said fourth MIS transistor being connected to said precharging node.

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9. A precharging circuit as recited in claim 8, wherein each of said third and fourth MIS transistors is of the enhancement type.

10. A precharging circuit implemented in a semiconductor memory chip for charging a precharging node to a high voltage level from a high voltage source under control of a series of clock pulses, successive clock pulses being separated by corresponding interim time intervals and each clock pulse having a leading edge and a trailing edge defining therebetween a corresponding clock pulse time interval, comprising:

- a first terminal for connection to the high voltage source;
  - a precharging node defining an output terminal of said precharging circuit;
  - a charge storage capacitor connected between said precharging node and a reference potential for developing a voltage at said precharging node having a level which incrementally increases to a high voltage level approaching that of the high voltage source;
  - a second node;
  - a first MIS transistor having source, drain and gate terminals and operatively connected at said source, drain and gate terminals thereof respectively to the high voltage source terminal, to said precharging node and to said second node, said first MIS transistor having a predetermined threshold voltage for conduction;
  - a charge pump circuit operatively connected between said precharging node and through said second node to said gate of said first MIS transistor, said charge pump circuit comprising a third node therein, first and second means connected in series at said third node and respectively to said second node and to said precharging node, a clock pulse input terminal to which the series of clock pulses is applied, and a coupling capacitor connected between said clock pulse input terminal and said third node;
- means for applying the series of clock pulses to said charge pump circuit, each said clock pulse being

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applied to said third node through said coupling capacitor for developing a charge thereon and producing an increase in the voltage level of said third node;

said first means being responsive to the leading edge of each said clock pulse for transferring the charge at said third node to said second node thereby to produce an increase in the voltage level at said second node and thereby to render said first MIS transistor conductive when the voltage level at said second node exceeds the predetermined threshold voltage for conduction of said first MIS transistor, relative to the voltage level of said precharging node;

said charge-pump circuit responding to the trailing edge of each said clock pulse to lower the voltage level of said third node, said first means being rendered nonconductive thereby and said second means being rendered conductive thereby so as to increase the voltage level of said third node in accordance with the voltage level of said precharging node during the interim time interval preceding a next successive clock pulse; and

third means having a predetermined threshold voltage for operation and connected between said gate and said drain of said first MIS transistor and responsive to the voltage level at said second node exceeding said predetermined threshold voltage for operation of said third means, relative to the voltage level of said precharging node, for permitting a charging current to flow from said second node to said precharging node and thereby reduce the voltage level at said second node for terminating conduction of said first MIS transistor within the clock pulse time interval of each clock pulse.

11. A precharging circuit as recited in claim 10, wherein each of said first, second and third means comprises a MIS transistor.

12. A precharging circuit as recited in claim 11, wherein each of said MIS transistors is of the enhancement type.

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## United States Patent [19]

Dufour

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[45] Date of Patent: Nov. 7, 1995

[54] LOW-CONSUMPTION LOW-NOISE  
CHARGE-PUMP CIRCUIT4,115,710 9/1978 Lou ..... 307/296.2  
4,847,519 7/1989 Wahl et al. .

[75] Inventor: Yves Dufour, Caen, France

[73] Assignee: U.S. Philips Corporation, New York,  
N.Y.

Primary Examiner—Timothy P. Callahan

Assistant Examiner—Jung H. Kim

Attorney, Agent, or Firm—Bernard Franzblau

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[22] Filed: Feb. 25, 1994

[30] Foreign Application Priority Data

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[51] Int. Cl.<sup>6</sup> ..... H03K 17/66[52] U.S. Cl. .... 327/112; 327/111; 327/405;  
327/403; 327/108[58] Field of Search ..... 307/296.6, 296.7,  
307/254, 255, 270, 296.2; 327/108, 484,  
534, 538, 542, 112, 111, 405, 403

[56] References Cited

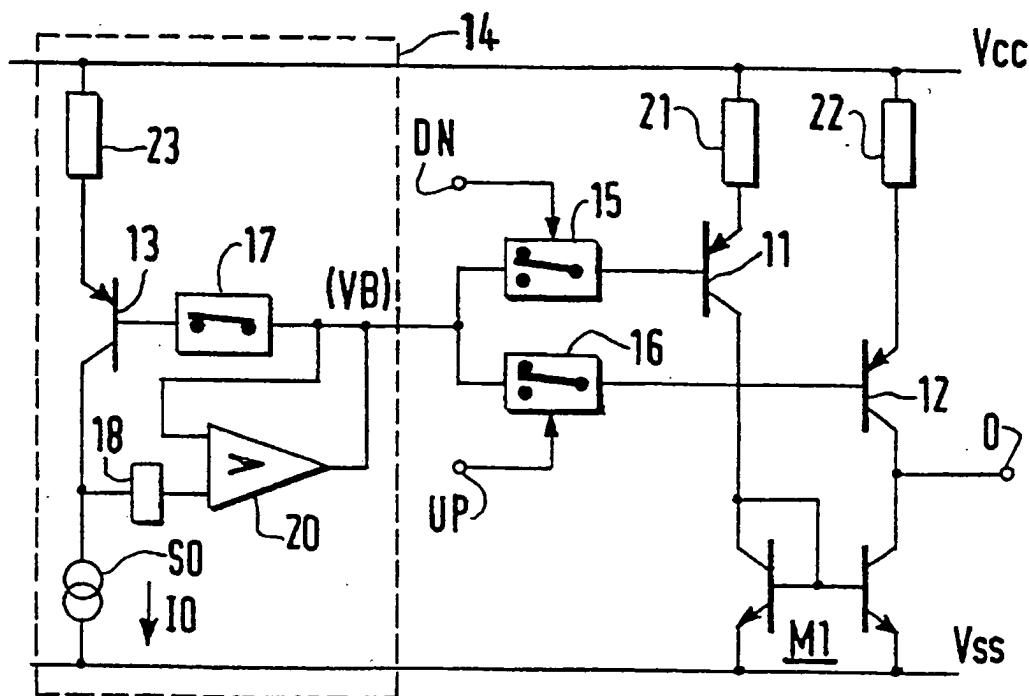
U.S. PATENT DOCUMENTS

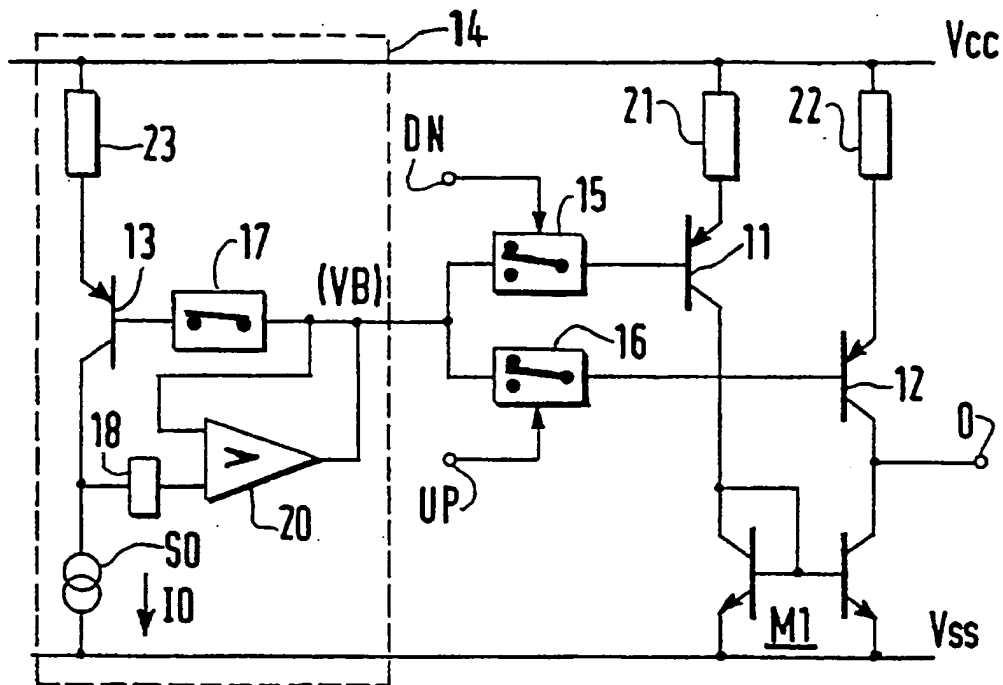
3,009,070 11/1961 Barnes ..... 307/254

21 Claims, 2 Drawing Sheets

## [57] ABSTRACT

A low noise charge-pump circuit with low power consumption and operating in a cyclic mode comprises two current sources connected in parallel, and a current mirror for transforming the current supplied by one of the current sources and coupling it to the output of the other current source. Each of the current sources essentially comprises a transistor controlled from the output (VB) of a reference voltage generator via a respective transistor switch. The reference voltage generator essentially comprises a third transistor similar to the two first-mentioned transistors and in series with a further current source supplying a current  $I_0$ , and means for making the current through the third transistor equal to the current  $I_0$ .





**FIG.1**

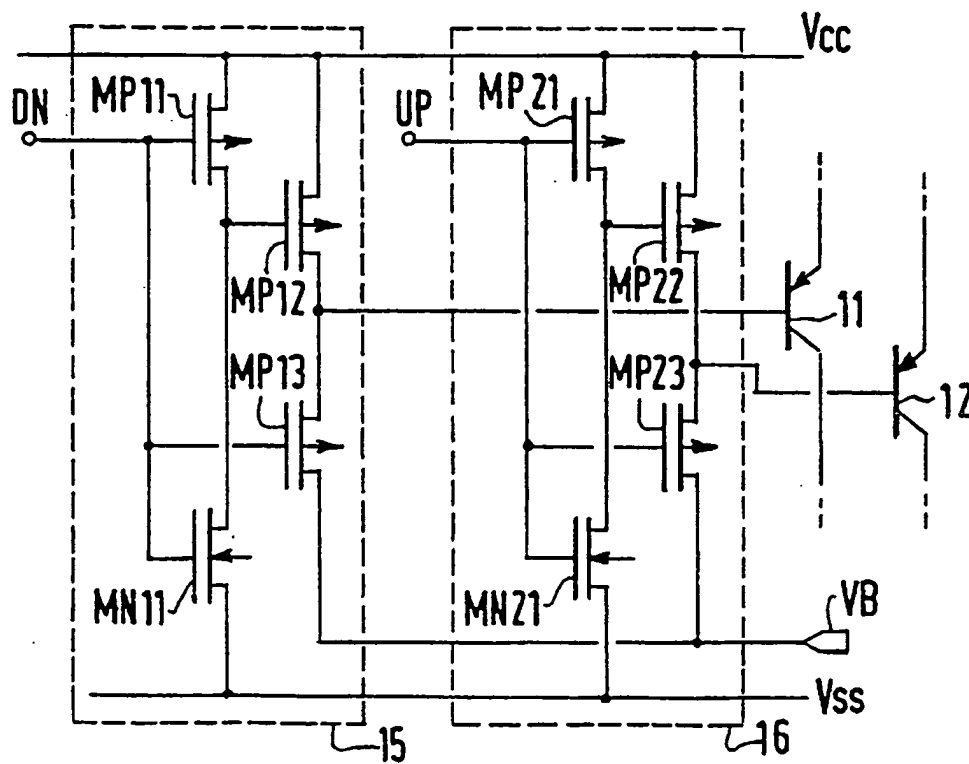
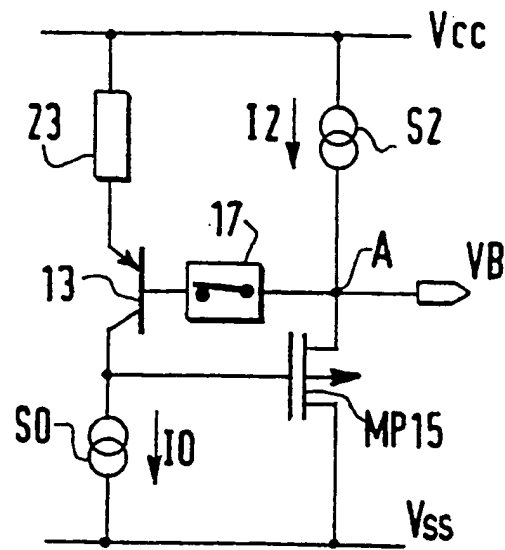


FIG.2





**FIG. 3**

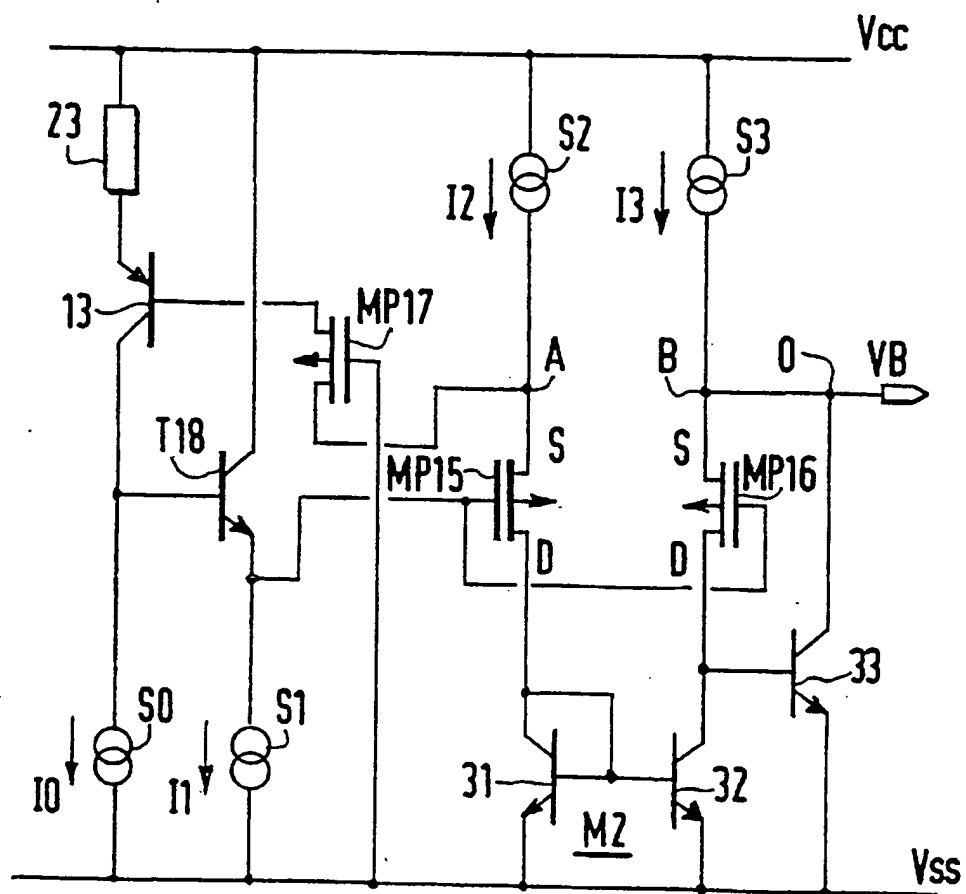


FIG. 4

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## LOW-CONSUMPTION LOW-NOISE CHARGE-PUMP CIRCUIT

### FIELD OF THE INVENTION

This invention relates to a charge-pump circuit which, starting from a first supply terminal, comprises a first current source and a second current source of similar construction, whose current supplied to a second supply terminal is nominally identical, said current sources being activated independently and cyclically by control signals, i.e. a so-called down signal and a so-called up signal, which circuit also comprises a current mirror having an input arranged in the connection between the first current source and the second supply terminal, and having an output connected to the output of the second current source to form an output terminal of the charge-pump circuit.

### BACKGROUND OF THE INVENTION

Such a charge-pump circuit is known from the U.S. Pat. No. 4,847,519. The circuit known from this document comprises two current sources formed by two differential stages operating under cyclic control of up and down signals, a charge pulse being supplied at the output during a time interval in which only one of the two current sources is active. During the remainder of a cycle of the cyclic control signal the current sources are either inactive or simultaneously active, as a result of which no charge is supplied to the output of the circuit. The charge pulses at the output of the circuit are stored in a storage capacitance.

Although the known circuit arrangement has the advantage that it uses two current sources which can be very much alike and can therefore be paired in a suitable manner, it has the serious drawback of permanently consuming the total current of the two current sources owing to the use of the differential circuit.

With respect to the noise characteristics at the output of a charge-pump circuit of this type, a detailed analysis of the situation will show that the average noise is substantially proportional to the duty cycle of the control signals, the noise being substantially zero during the part of the cycle in which both current sources are inactive. To reduce the average noise at the output it is therefore advantageous to use control signals whose duty cycle is as small as possible. Moreover, if the current sources supply a large current, for example, several milliamperes or even some tens of milliamperes, this will improve the ability of a charge-pump circuit to rapidly change the value at the output in response to a sudden variation of the phase of an oscillator to be controlled.

Therefore, the prior-art charge-pump circuit is not suitable for uses in which the current consumption should be minimal, as in the case of battery-powered portable apparatuses.

It is an object of the invention to mitigate the above-mentioned problems. The invention features a charge-pump circuit whose power consumption is substantially smaller than that of the known circuit and whose noise at the output is reduced considerably.

### SUMMARY OF THE INVENTION

According to the invention a charge-pump circuit of the type defined in the opening paragraph is characterized in that the first and the second current source essentially comprise a first and a second transistor, respectively, the control electrode of each of said transistors being coupled to the output of a reference voltage generator common to the two

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transistors via a first transistor switch, controlled by the down signal, for the first transistor, and via a second transistor switch, controlled by the up signal, for the second transistor, and the reference voltage generator comprises a third transistor of a construction similar to that of the two first-mentioned transistors, a reference current source in series with the third transistor, and means for making the current through the third transistor equal to the current of said reference current source. The control electrode of the third transistor carries said reference voltage to be applied to the control electrodes of the first and the second transistor.

Thus, in accordance with the invention the first and the second current source only supply current during the time in which they are activated, which time is defined by the duty cycles of the control signals, which can be as small as  $1/10^4$ , whereas the third transistor alone permanently supplies the reference current produced by the reference current source. In practice, a reference-voltage generator as defined can be used to feed a plurality of first and second current sources in a manner such that the average current consumption remains very moderate.

Since the control electrodes of the first and the second transistors are driven by the same reference voltage generator, the noise which can appear on the output of this generator is substantially eliminated at the output of the circuit in the phase of the cycle in which both current sources are active simultaneously.

In a preferred embodiment the charge-pump circuit in accordance with the invention is characterized in that the reference voltage generator comprises a feedback amplifier having a first input coupled to a node between the reference current source and the output electrode of the third transistor, having a second input coupled to the control electrode of said third transistor, and having an output supplying said reference voltage.

Depending on the field of use the feedback amplifier can be adapted to the number of current sources fed by this generator and the current supplied by these current sources. Since the output electrode of the third transistor is coupled to one of the inputs of the feedback amplifier, the third transistor will operate with a well-defined and constant voltage.

In order for operating conditions of the third transistor to be, as far as possible, similar to those of the first and the second transistor, it is advantageous if a fourth transistor, serving as a permanently closed switch, is arranged between the second input of the feedback amplifier and the control electrode of the third transistor. The fourth transistor is of a construction similar to that of the transistors of the first and the second switch which control the cyclic activation of the first and the second transistor of the charge pump.

In this way the current sources supply a current which is a most accurate replica of the reference current produced in the reference voltage generator. The current supplied by the first and the second current source can thus be predicted very precisely.

In accordance with the invention a charge-pump circuit may also comprise a voltage shifter included at the first input of the feedback amplifier. This arrangement makes it possible to select an operating voltage for the third transistor which is compatible with the supply voltages and which is close to the operating voltages of the first and the second transistor.

The charge-pump circuit in accordance with the invention can be implemented by means of MOS field effect transistors, by means of bipolar transistors, or suitably by means of

a combination of transistors of both types.

The invention also relates to a frequency synthesizer including at least one charge-pump circuit as defined above. A frequency synthesizer which could use the defined charge-pump circuit is described in U.S. Pat. No. 4,814,726, hereby incorporated by reference.

### BRIEF DESCRIPTION OF THE DRAWINGS

Further characteristic features and advantages of the invention will become apparent upon perusal of the following description with reference to the accompanying drawings given by way of non-limitative examples, in which:

FIG. 1 is a partly block-schematic circuit diagram of a charge-pump circuit in accordance with the invention,

FIG. 2 shows a detailed example of two switches used in the circuit shown in FIG. 1,

FIG. 3 is a simplified circuit diagram of a feedback amplifier used in the charge-pump circuit in accordance with the invention, and

FIG. 4 shows a preferred version of such a feedback amplifier.

### DESCRIPTION OF EMBODIMENTS

FIG. 1 shows the basic diagram of a charge-pump circuit in accordance with the invention.

Arranged in parallel between the positive supply terminal  $V_{cc}$  and the negative supply terminal  $V_{ss}$  are a first bipolar pnp transistor 11, whose emitter is coupled to the terminal  $V_{cc}$  via an emitter resistor 21, and a second pnp transistor 12, whose emitter is coupled to the terminal  $V_{cc}$  via an emitter resistor 22 of the same value as the resistor 21. The collector of the first transistor 11 is connected to the input of a current mirror M1 which comprises bipolar npn transistors and has its output connected to the collector of the second transistor 12 to form a node constituting the output terminal O of the charge-pump circuit. The respective transistor and emitter resistor 11, 21 and 12, 22 form the first current source and the second current source, respectively, of the charge pump. The base of the first transistor 11 is coupled to the output of a reference voltage generator 14, which supplies a reference voltage VB at its output, via a transistor switch 15 which is controlled by a down signal DN. Likewise, the second transistor 12 has its base coupled to the same output of the reference voltage generator 14 via another transistor switch 16 which is controlled by an up signal UP. The down signal DN and the up signal UP are both supplied by a phase comparator associated with the charge-pump circuit in order to form a phase-locked loop, which phase comparator is of a known type and is not shown in the Figure. These signals are pulse-shaped signals with small duty cycles and they are pulse-width modulated.

The reference voltage generator 14 basically comprises a third transistor 13 of a construction similar to that of the first and the second transistors 11, 12. The third transistor has its emitter coupled to the supply terminal  $V_{cc}$  via an emitter resistor 23 of the same resistance value as the emitter resistors 21 and 22 of the first and the second transistors. The third transistor 13 is coupled to the supply terminal  $V_{ss}$  via a reference current source So supplying a fixed reference current  $I_o$ .

In addition, means have been provided for making the current through the third transistor 13 equal to the current  $I_o$  of said reference current source So. Said means essentially comprise a feedback amplifier 20. A first input of this

amplifier 20 is coupled to the node between the collector of the third transistor 13 and the current source So, suitably via a voltage shifter 18. A second input of the amplifier 20 is coupled to the base of the third transistor 13, suitably via a permanently closed transistor switch 17. As will be explained in more detail hereinafter, the switch 17 is formed by a transistor of the same type and of a construction similar to that of the transistors of the switches 15 and 16 effecting the cyclic activation of the first transistor 11 and the second transistor 12. The output of the amplifier 20 is connected to the second input of this amplifier and carries said reference voltage VB, which should be applied cyclically to the first transistor 11 and the second transistor 12 of the charge pump. Thus, such a reference voltage generator 14 comprises means which are entirely similar to the first and the second transistors 11 and 12 of the charge pump, such that when these transistors are activated they exactly reproduce the reference current  $I_o$ .

Reference is now made to FIG. 2, which shows a preferred example of the switches 15 and 16, shown diagrammatically in FIG. 1. Here, the switches 15 and 16 are implemented by means of MOS field-effect transistors. The switch 15 receives at its input the down command DN, which is applied to the gate of a pair of transistors MP11 and MN11 arranged in series between the supply terminals  $V_{cc}$  and  $V_{ss}$ . MP11 is a p-channel transistor and MN11 is an n-channel transistor. This transistor pair supplies a logic output signal which is the inverse of the down command DN. Another pair of p-channel MOS transistors MP12 and MP13 is arranged in series between the supply terminal  $V_{cc}$  and the node carrying the reference voltage VB.

The transistor MP12, which is referred to the supply terminal  $V_{cc}$ , receives at its gate the inverted down signal from the output of the pair of transistors MP11 and MN11. The transistor MP13, which is referred to the reference voltage VB, receives at its gate the down signal DN. Thus, the transistors MP12 and MP13 form a switch, the node common to these two transistors being either at the voltage  $V_{cc}$  or at the voltage VB depending on the down signal DN. The node is connected to the base of the first transistor 11 of the charge pump.

The switch 16 is of a construction entirely similar to that of the switch 15. At its input it receives the up command UP applied to the gate of a pair of MOS transistors MP21 and MN21 forming an inverter for the up signal UP. Likewise, a second pair of transistors MP22 and MP23 are arranged between the terminal  $V_{cc}$  and the line carrying the reference voltage VB and have an output formed by the node between these transistors. This node is coupled directly to the base of the second transistor 12 of the charge pump.

When the first transistor 11 of the charge pump is activated, the transistor MP13 conducts and supplies the reference voltage VB to the base of the transistor 11. Likewise, when the second transistor 12 of the charge-pump is activated the transistor MP23 conducts and transfers the reference voltage VB to the base of this transistor 12. As stated above, the transistor forming the normally closed switch 17 in the reference voltage generator 14 is a p-channel MOS transistor of a construction identical to that of the transistors MP13 and MP23 such that the reference voltage VB allows for the voltage drop across each of these transistors. Thus, the reference current  $I_o$  is reproduced exactly in the first transistor 11 and the second transistor 12 when they are activated.

When activated simultaneously, the first and the second transistor 11 and 12 of the charge pump are biased with the

same reference voltage VB, as a result of which the noise caused by this voltage at the output O of the charge pump is substantially eliminated.

FIG. 3 shows very diagrammatically an example of a feedback amplifier such as the amplifier 20 in FIG. 1. Here, the feedback amplifier is essentially formed by means of a p-channel MOS field-effect transistor MP15 having a gate connected to the node between the collector of the third transistor 13 and the reference current source So. The main current path of the transistor MP15 is disposed between the supply terminal Vss and a node A forming the output carrying the reference voltage VB, which node is also connected to the base of the third transistor 13 via the switch 17 and is coupled to the supply terminal Vcc via a current source S2. The base-collector voltage of the third transistor 13 is therefore determined by the threshold voltage of the transistor MP15 plus the voltage drop across the switch 17. The transistor MP15 absorbs the current from the current source S2 to bring the node A at the voltage VB in a manner such that the third transistor 13 supplies the current I<sub>o</sub> of the reference current source So. The reference voltage VB appears across an impedance which decreases as the current I<sub>2</sub> supplied by the current source S2 increases. It can respond to any demand for base current of the first and the second transistors 11 and 12 of the charge pump.

FIG. 4 shows a preferred example of the entire reference voltage generator 14 shown in FIG. 1. The third transistor 13 is again shown with its emitter resistor 23 and with the reference current source So in series with this transistor.

A bipolar npn transistor T18 has its base connected to the collector of the third transistor 13, has its emitter coupled to the supply terminal Vss via another current source S1 supplying a current I<sub>1</sub>, and has its collector connected directly to the supply terminal Vcc. Here, the transistor T18 forms the voltage shifter 18 shown in FIG. 1. The base of the third transistor 13 is connected to an electrode of the main current path of a p-channel MOS transistor MP17, whose gate is connected to the supply terminal Vss. The transistor MP17 forms a permanently closed switch referenced 17 in FIGS. 1 and 3. The feedback amplifier now comprises a first p-channel MOS input transistor MP15 and a second p-channel MOS input transistor MP16 whose gates are interconnected and connected to the emitter of the transistor T18. The source S of the first input transistor MP15 receives the output voltage of the transistor MP17 forming the permanently closed switch and is also coupled to the supply terminal Vcc via the current source S2, which is as described with reference to FIG. 3 and which supplies a current I<sub>2</sub>. The source S of the second input transistor MP16 forms the output terminal of the amplifier and is also coupled to the supply terminal Vcc via a current source S3 supplying a current I<sub>3</sub>. The drain D of the first input transistor MP15 is coupled to the supply terminal Vss via the input of a current mirror comprising bipolar npn transistors 31 and 32. The output of the current mirror M2, which output is formed by the collector of the transistor 32, is coupled to the drain D of the second input transistor MP16 and to the base of a bipolar npn output transistor 33 having its emitter connected to the supply terminal Vss and its collector connected to the output terminal O of the amplifier. The node A is as described with reference to FIG. 3. A node similar to the node A is referenced B and couples the current source S3 to the source S of the second input transistor MP16. The feedback amplifier thus formed has a higher power gain than the amplifier shown diagrammatically in FIG. 3. The node A, in contradistinction to that in the arrangement shown in FIG. 3, is now separated from the amplifier output (node B) but the

voltage appearing on the node A is exactly reproduced on the node B across an even lower impedance. The current I<sub>2</sub> supplied by the current source S2 is selected depending on the requirements and need not have a high accuracy. The current I<sub>3</sub> supplied by the current source S3 is selected to be larger than the current I<sub>2</sub>. The comparator comprising the transistors MP15, MP16, and the current mirror M2 require that identical currents equal to I<sub>2</sub> flow in the two input transistors MP15 and MP16. At the node B the output transistor 33 absorbs the difference between the currents I<sub>3</sub>-I<sub>2</sub> (in the absence of current consumption at the output). The voltage obtained on the node B is therefore a precise reproduction of the voltage on the node A so that the reference voltage VB appears across a low impedance.

The principal elements of the feedback amplifier comprising p-channel MOS transistors and bipolar npn transistors respond very rapidly to any demand for current from the reference voltage generator at terminal VB. Such a generator can therefore feed a plurality of first and second current sources which are operated in parallel and may be programmable to suit the needs of the user. It is evident that the current consumed permanently by a reference voltage generator of this type remains comparatively moderate as compared with that of several tens of first and second current sources operated in parallel.

Whereas the examples described above use a combination of bipolar transistors and MOS field-effect transistors, alternative constructions are possible using only bipolar transistors or only field-effect transistors. However, the examples described herein represent a preferred construction.

I claim:

1. A charge-pump circuit comprising: a first supply terminal and a second supply terminal, a first current source and a second current source of similar construction coupled to the first and second supply terminals so that currents supplied to the second supply terminal from the first and second current sources are nominally identical, said current sources being activated independently and with a cyclic activation by down and up control signals, a current mirror having an input branch in a connection between the first current source and the second supply terminal and having an output connected to an output of the second current source to form an output terminal of the charge-pump circuit, wherein the first and the second current source essentially comprise a first and a second transistor, respectively, a control electrode of each of said transistors being coupled to an output of a reference voltage generator common to the two transistors via a first transistor switch, controlled by the down signal, for the first transistor, and via a second transistor switch, controlled by the up signal, for the second transistor, and the reference voltage generator comprises a third transistor of a construction similar to that of the first and second transistors, a reference current source connected in series with the third transistor, and means for making current through the third transistor equal to current of said reference current source, a control electrode of the third transistor carrying a reference voltage to be applied to the control electrodes of the first and the second transistors.

2. A charge-pump circuit as claimed in claim 1, wherein the reference voltage generator comprises a feedback amplifier having a first input coupled to a node between the reference current source and an output electrode of the third transistor, having a second input coupled to the control electrode of said third transistor, and having an output supplying said reference voltage.

3. A charge-pump circuit as claimed in claim 2, further comprising a fourth transistor, serving as a permanently

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closed switch, coupled between the second input of the feedback amplifier and the control electrode of the third transistor, wherein said fourth transistor is of a construction similar to that of the transistors of the first and the second transistor switches and which control the cyclic activation of the first and the second transistors of the charge pump.

4. A charge-pump circuit as claimed in claim 2, wherein a voltage shifter is coupled to the first input of the feedback amplifier.

5. A charge-pump circuit as claimed in claim 3, wherein the first, the second and the third transistors are of the bipolar pnp type, and the current mirror comprises bipolar npn transistors.

6. A charge-pump circuit as claimed in claim 5, wherein the first and the second switch each comprise complementary MOS field-effect transistors.

7. A charge-pump circuit as claimed in claim 6, wherein the feedback amplifier comprises a first and a second input transistor of the p-channel MOS type, having interconnected gates, a source of the first input transistor receiving an output voltage of the fourth transistor and being coupled to a first associated current source fed by the first supply terminal, a source of the second input transistor forming the output of the amplifier and being coupled to a second associated current source which is also fed by the first supply terminal, a drain of the first input transistor being coupled to an input of a further current mirror comprising bipolar npn transistors, said further current mirror having an output connected to a drain of the second input transistor and to an input of a bipolar npn output transistor having its emitter connected to the second supply terminal and having its collector connected to the output of the amplifier.

8. A charge-pump circuit as claimed in claim 3, wherein a voltage shifter is coupled to the first input of the feedback amplifier.

9. A charge-pump circuit as claimed in claim 1, wherein the first, second and third transistors are of a bipolar pnp type, and the current mirror comprises bipolar npn transistors.

10. A charge-pump circuit as claimed in claim 3, wherein the feedback amplifier comprises a first and a second input transistor of the p-channel MOS type, having interconnected gates, a source of the first input transistor receiving an output voltage of the fourth transistor and being coupled to a first associated current source fed by the first supply terminal, a source of the second input transistor forming the output of the amplifier and being coupled to a second associated current source which is also fed by the first supply terminal, a drain of the first input transistor being coupled to an input of a further current mirror comprising bipolar npn transistors, said further current mirror having an output connected to a drain of the second input transistor and to an input of a bipolar npn output transistor having its emitter connected to the second supply terminal and having its collector connected to the output of the amplifier.

11. The charge-pump circuit as claimed in claim 1 wherein the first transistor switch comprises first and second complementary MOS transistors serially coupled between said first and second supply terminals and with a common node therebetween coupled to the control electrode of the first transistor, and

the second transistor switch comprises third and fourth complementary MOS transistors serially coupled between said first and second supply terminals and with a common node therebetween coupled to the control electrode of the second transistor.

12. A charge-pump circuit comprising:

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first and second supply terminals,

a current mirror having an input terminal, an output terminal, and a common terminal connected to said second supply terminal,

a first current source including a first transistor coupled to said first supply terminal and to said input terminal of the current mirror,

a second current source including a second transistor coupled to said first supply terminal and to said output terminal of the current mirror,

an output terminal coupled to a node between the second transistor and the output terminal of the current mirror,

a reference voltage generator having an output coupled to respective control electrodes of the first and second transistors via first and second controlled switches, respectively,

means for supplying first and second control signals to respective control terminals of the first and second controlled switches so as to actuate the first and second transistors cyclically by means of a reference voltage produced at the output of the reference voltage generator, and wherein

the reference voltage generator comprises;

a third transistor of a type similar to that of the first and second transistors,

a source of reference current connected in series with the third transistor to said first and second supply terminals, and

a feedback circuit coupled to the third transistor so as to make a current flowing through the third transistor equal to the current of said reference current source.

13. The charge-pump circuit as claimed in claim 12 wherein the feedback circuit of the reference voltage generator comprises a feedback amplifier having a first input coupled to a node between the reference current source and an output electrode of the third transistor, having a second input coupled to a control electrode of said third transistor, and having an output coupled to said output of the reference voltage generator so as to supply said reference voltage to said reference voltage generator output.

14. The charge-pump circuit as claimed in claim 13 wherein said first and second controlled switches comprise transistor switches and said reference voltage generator further comprises a fourth transistor coupled between the second input of the feedback amplifier and the control electrode of the third transistor, said fourth transistor being of the same type as the transistor switches.

15. The charge-pump circuit as claimed in claim 12 wherein said control signals supplying means supplies pulse-shaped signals with a short duty cycle and said first and second current sources supply respective currents that are determined by the source of reference current of said reference voltage generator.

16. The charge-pump circuit as claimed in claim 12 wherein the third transistor comprises a bipolar transistor and the feedback circuit comprises;

a MOS transistor having its gate coupled to a node between the third transistor and the reference current source and a first main electrode coupled to a base of the third transistor and to the first supply terminal via a second source of reference current.

17. The charge-pump circuit as claimed in claim 16 wherein a second main electrode of said MOS transistor is coupled to the output of the reference voltage generator via a further current mirror comprising bipolar transistors.

18. The charge-pump circuit as claimed in claim 17 wherein an output of the further current mirror is coupled to a further MOS transistor and a further bipolar transistor each of which is coupled to said output of the reference voltage generator, and all in a manner whereby the reference voltage 5 at said output of the reference voltage generator reproduces a voltage at the first main electrode of said MOS transistor, said first main electrode of said MOS transistor being separated from said reference voltage generator output at least by said further current mirror.

19. The charge-pump circuit as claimed in claim 12 wherein said reference voltage controls said first and second transistors and said third transistor so that the first and second current sources supply respective currents that are

determined by the source of reference current of said reference voltage generator.

20. The charge-pump circuit as claimed in claim 19 wherein said first and second controlled switches comprise transistor switches and said output of the reference voltage generator is coupled to a control electrode of the third transistor via a conductive fourth transistor of the same type as said transistor switches.

21. The charge-pump circuit as claimed in claim 1 wherein said first and second supply terminals are energized by a DC battery and said first and second current sources are coupled in parallel to the first supply terminal.

\* \* \* \* \*



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Nork et al.

(10) **Patent No.:** US 6,411,531 B1  
(45) **Date of Patent:** Jun. 25, 2002

(54) **CHARGE PUMP DC/DC CONVERTERS WITH REDUCED INPUT NOISE**

(75) Inventors: Samuel H. Nork, Andover; William L. Walter; Steven L. Martin, both of Lowell, all of MA (US)

(73) Assignee: Linear Technology Corporation, Milpitas, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: Nov. 21, 2000

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(52) U.S. Cl. .... 363/60

(58) Field of Search ..... 323/222, 282;  
307/110; 363/59, 60

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

4,809,152 A 2/1989 Bingham et al.  
4,812,961 A 3/1989 Essaff et al.  
4,897,774 A 1/1990 Bingham et al.  
6,157,180 A \* 12/2000 Kuo ..... 323/282

6,188,212 B1 \* 2/2001 Larson et al. .... 323/281  
6,201,717 B1 \* 3/2001 Grant ..... 363/60

**OTHER PUBLICATIONS**

"Switched-Capacitor Voltage Converter with Regulation," LT1054 DataSheet, 1994, pp. 4-26-4-37.

\* cited by examiner

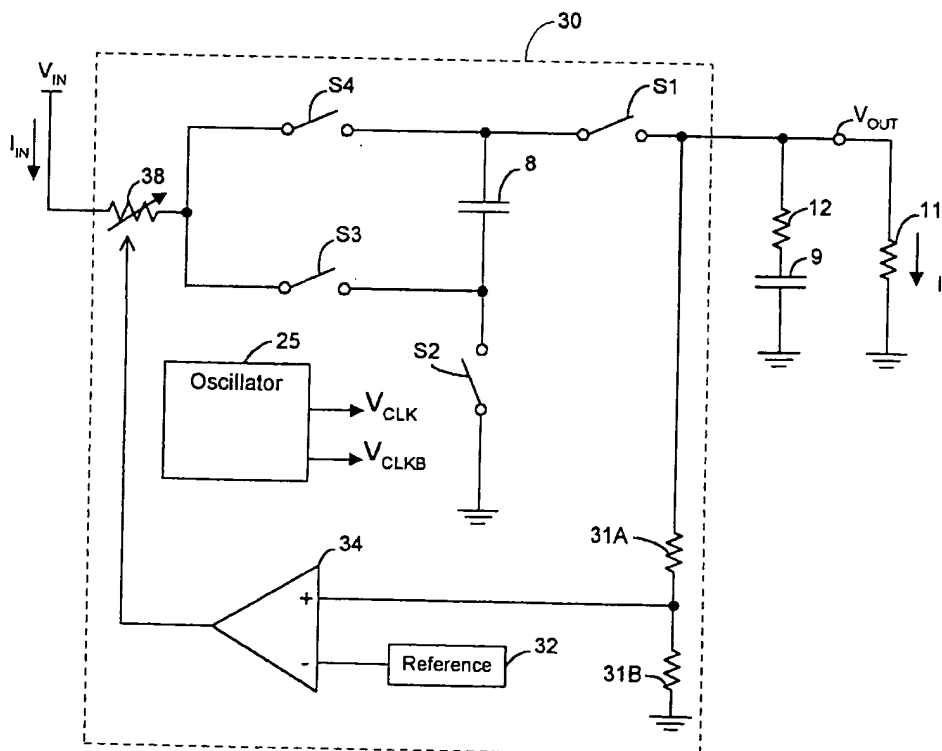
Primary Examiner—Adolf Deneke Berhane

(74) Attorney, Agent, or Firm—Fish & Neave; Robert W. Morris

(57) **ABSTRACT**

A charge pump DC/DC converter with reduced noise at the input voltage source is provided. The present invention includes buck and boost DC/DC converters with added circuitry coupled between the input voltage and the switches which maintains a substantially constant input current on both phases of the charge pump clock. The added circuitry reduces input current variations to provide reduced noise at the input voltage source. Feedback loop circuitry coupled between the output node and the added circuitry varies the current through the switches to control the output current of the DC/DC converter in order to maintain the output voltage at the regulated value. The added circuitry may comprise a variable resistor, current mirror, or current mirrors.

44 Claims, 9 Drawing Sheets



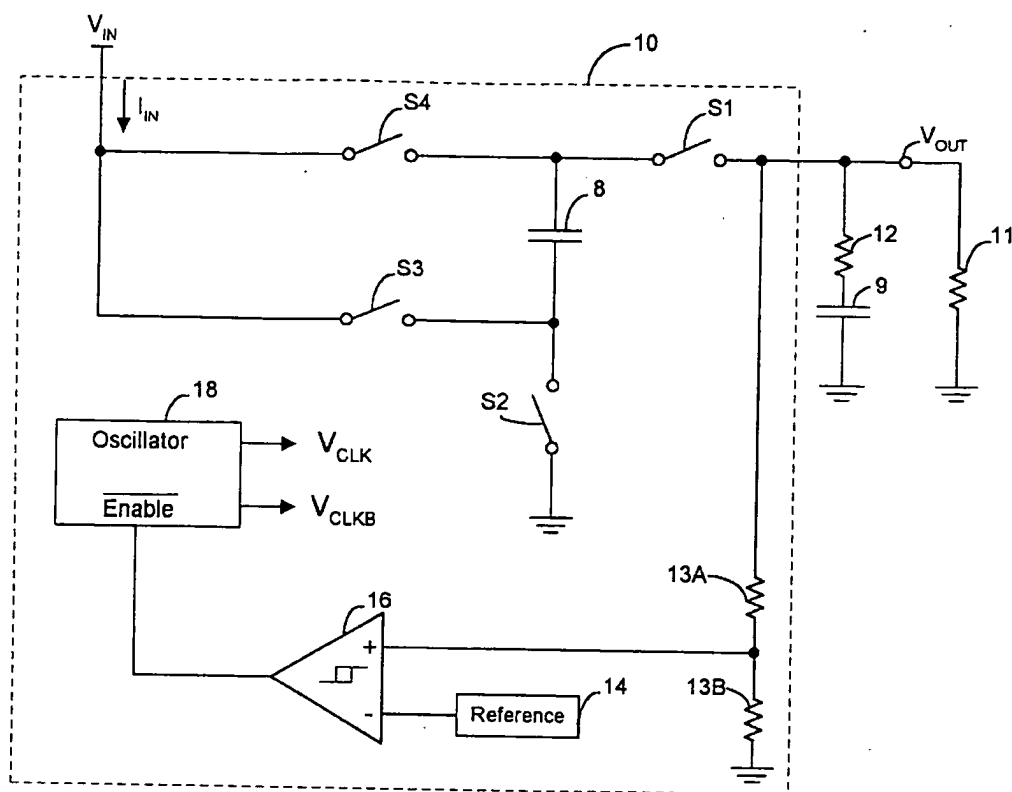


FIG. 1A (PRIOR ART)

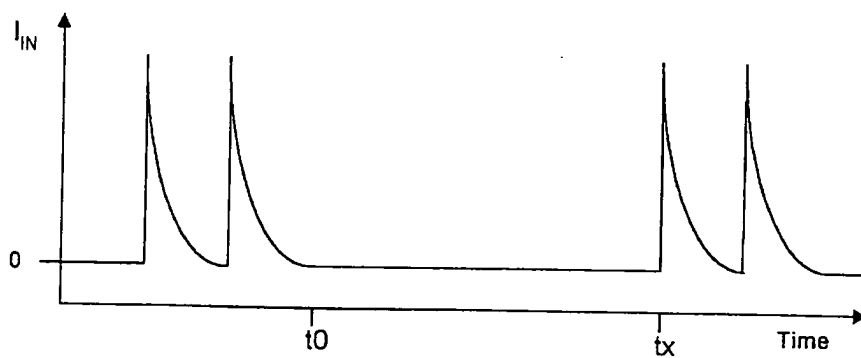


FIG. 1B (PRIOR ART)



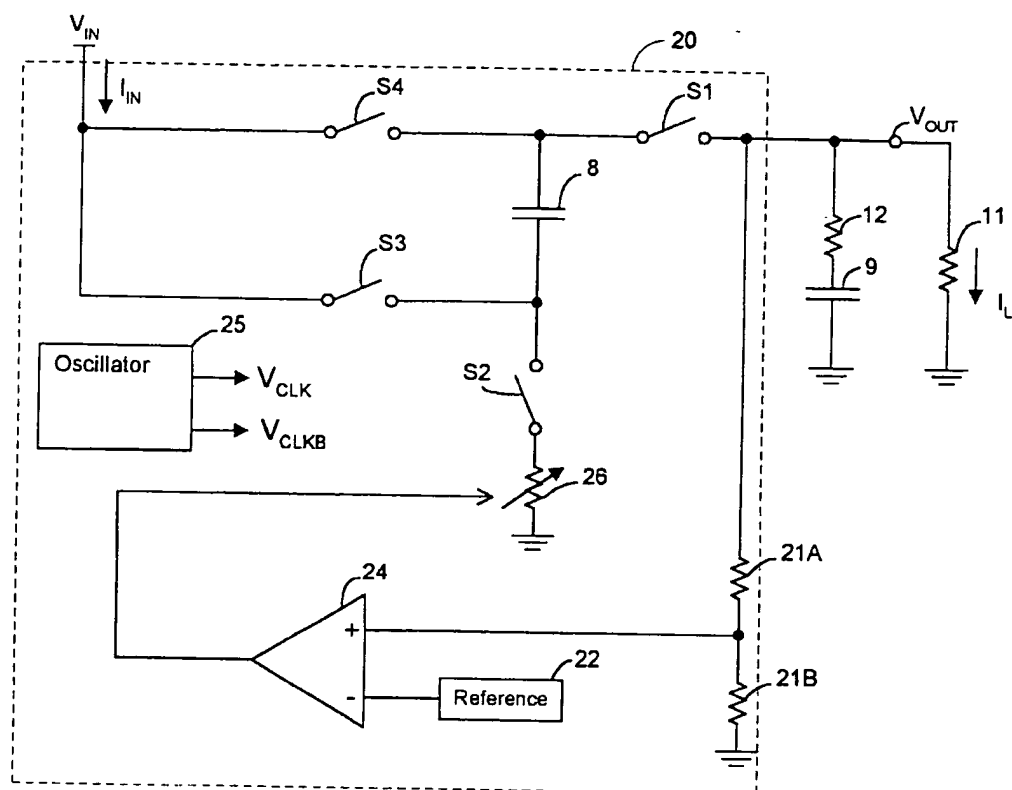


FIG. 2A (PRIOR ART)

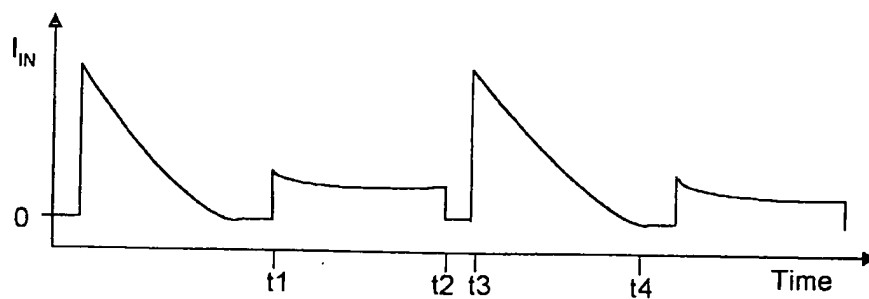


FIG. 2B (PRIOR ART)

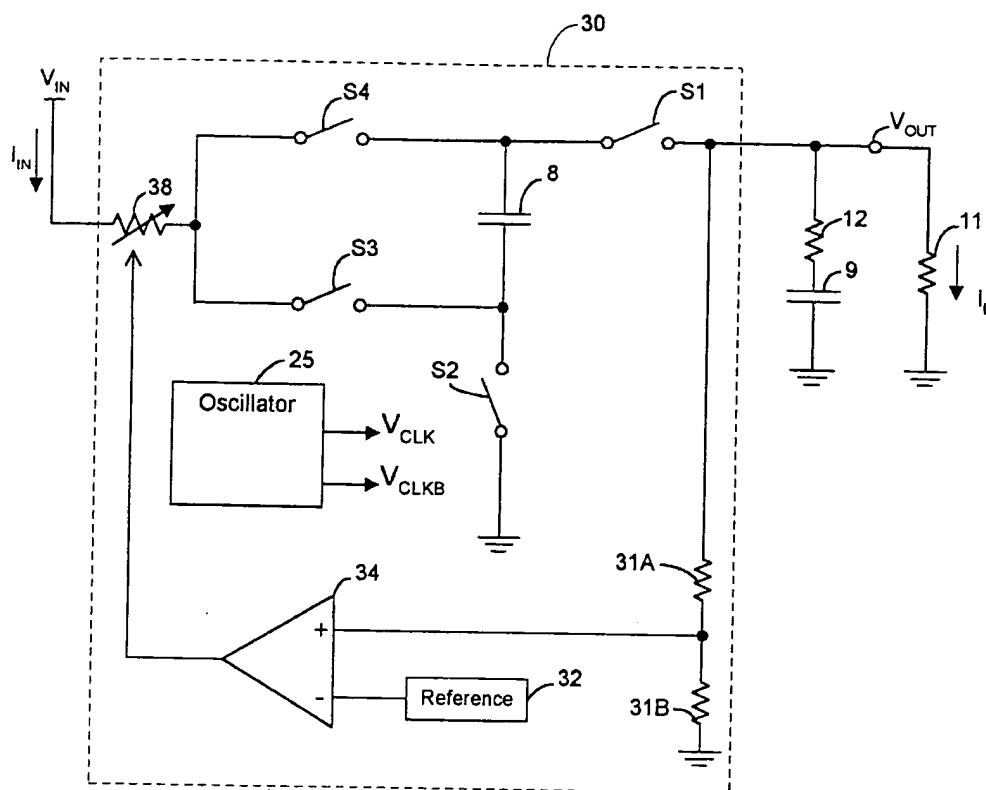


FIG. 3A

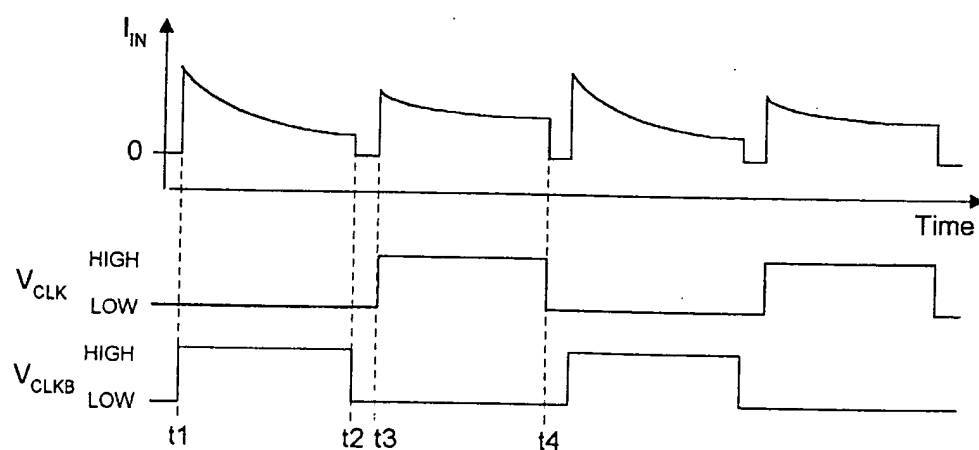


FIG. 3B

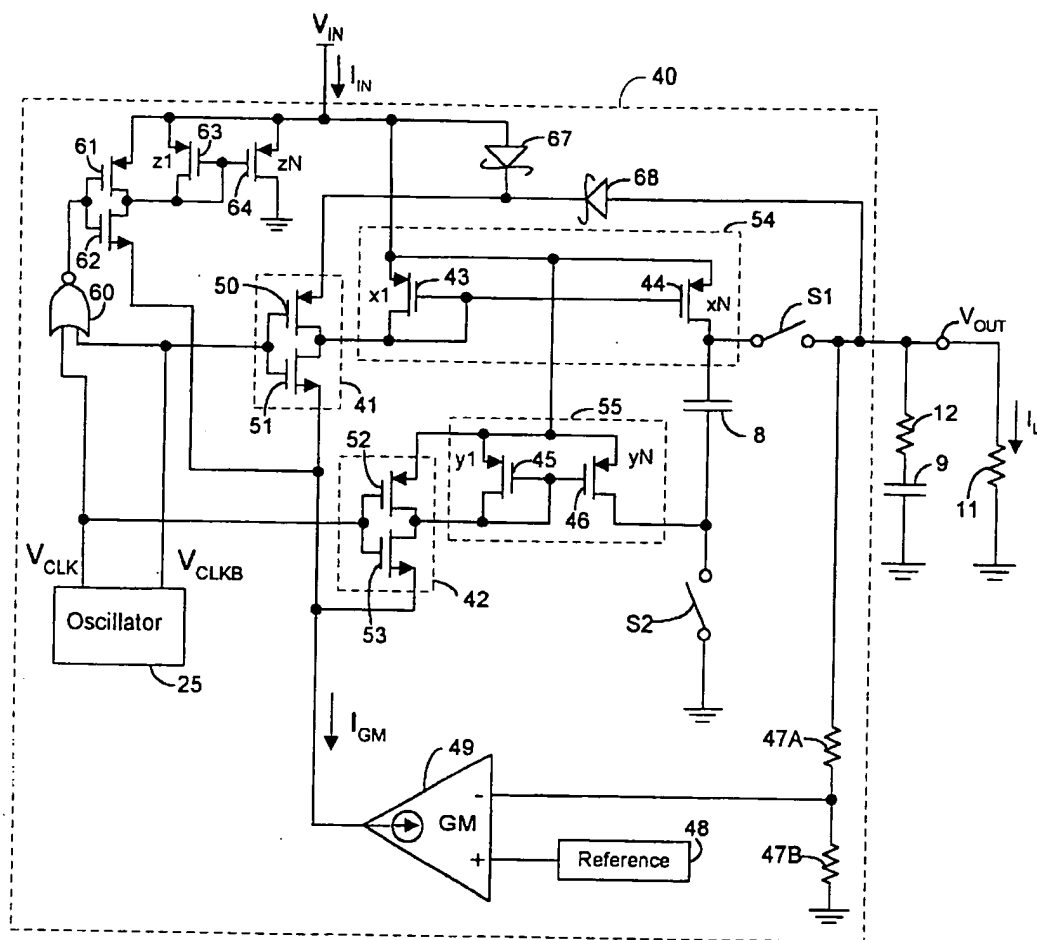


FIG. 4A

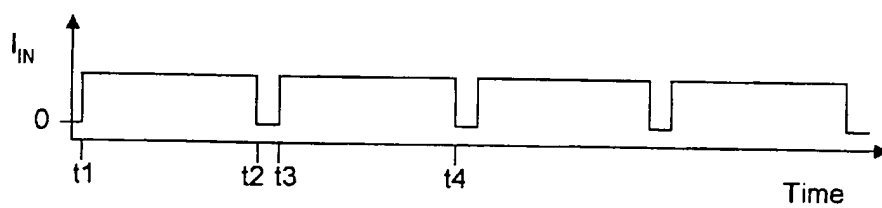


FIG. 4B

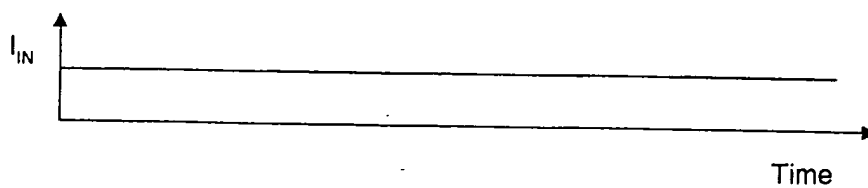


FIG. 4C

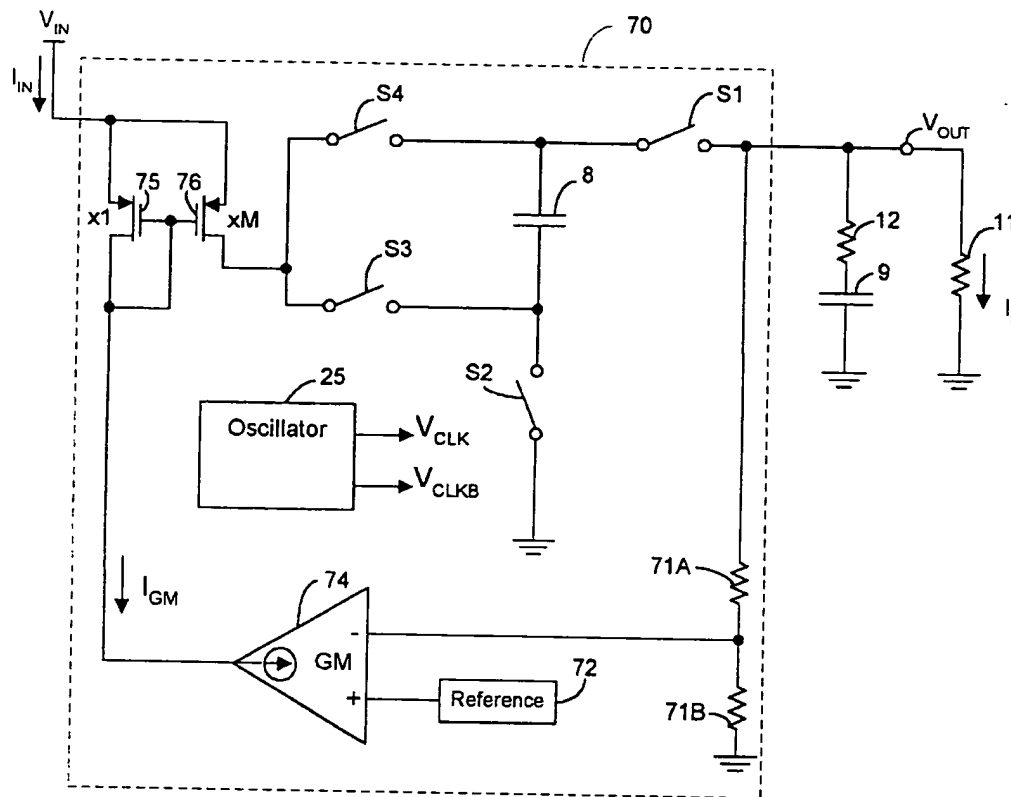


FIG. 5A

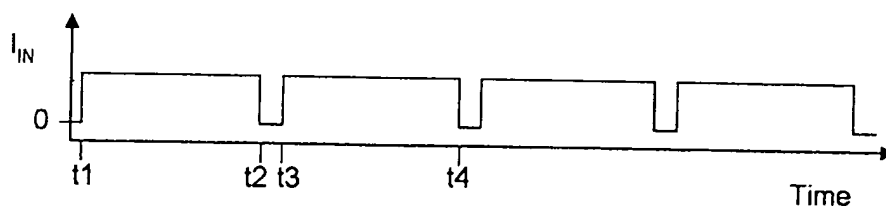


FIG. 5B

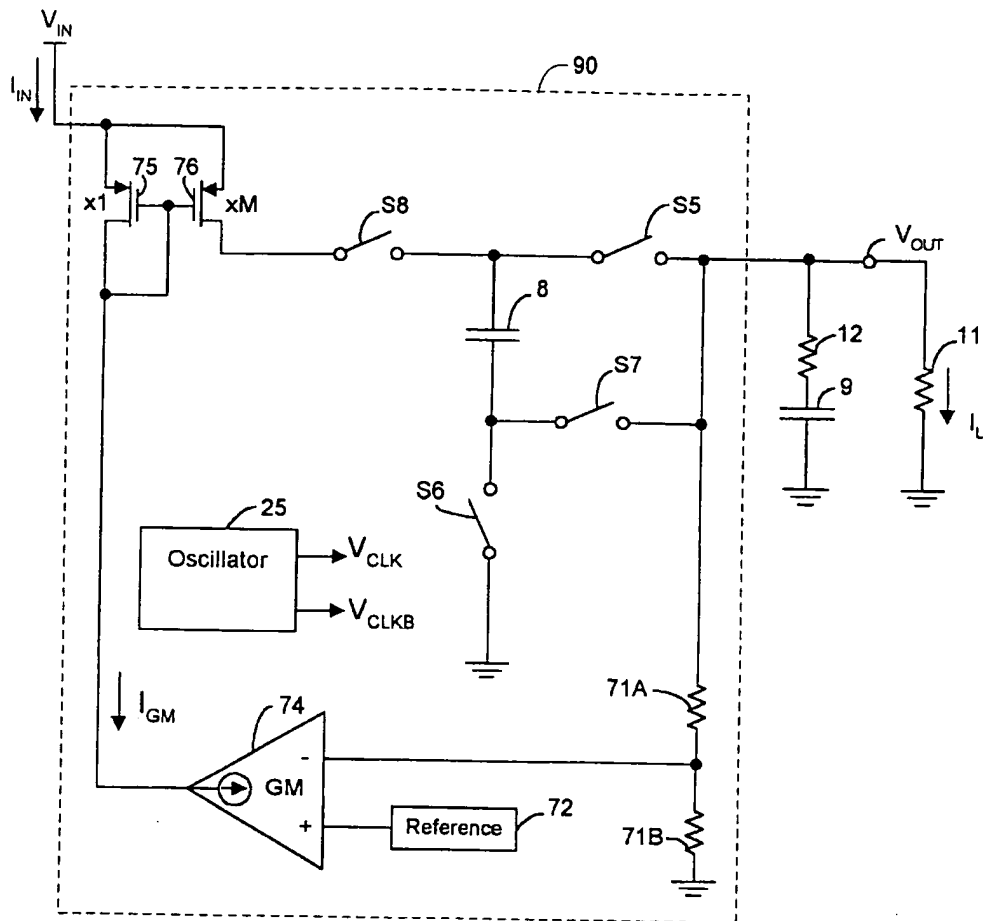


FIG. 6A

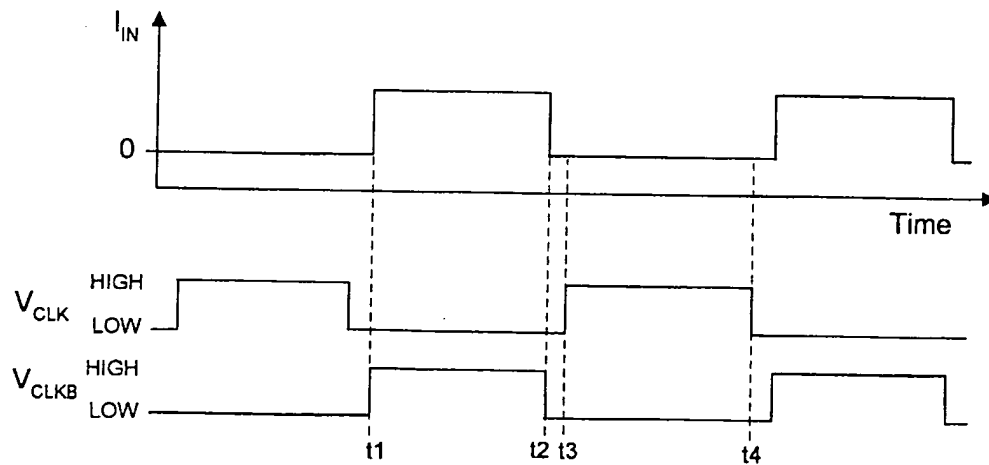


FIG. 6B

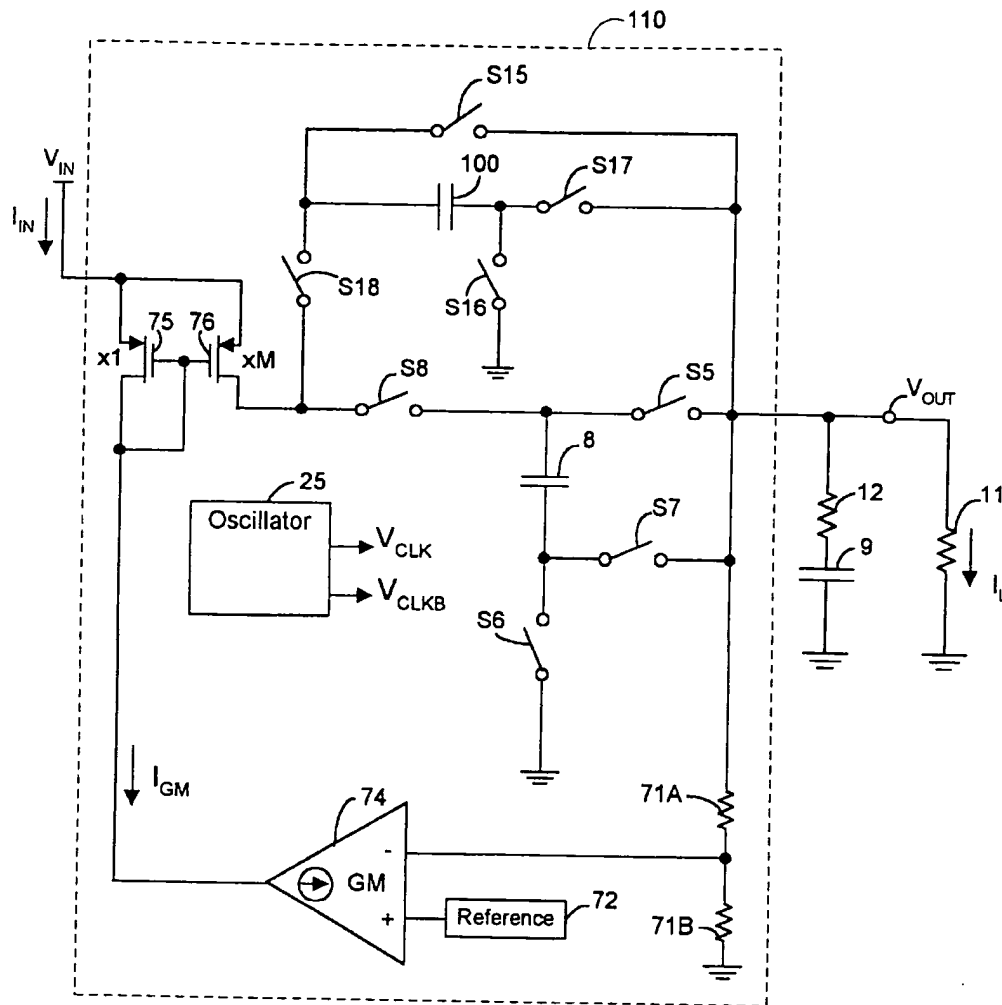


FIG. 7A

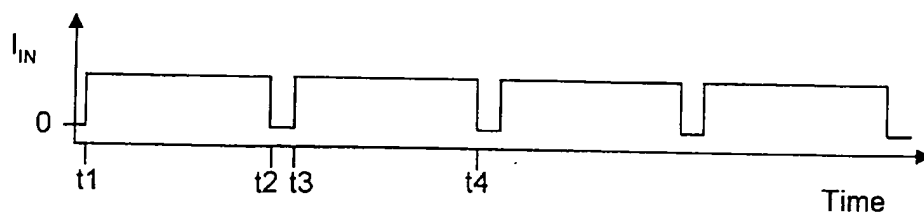


FIG. 7B

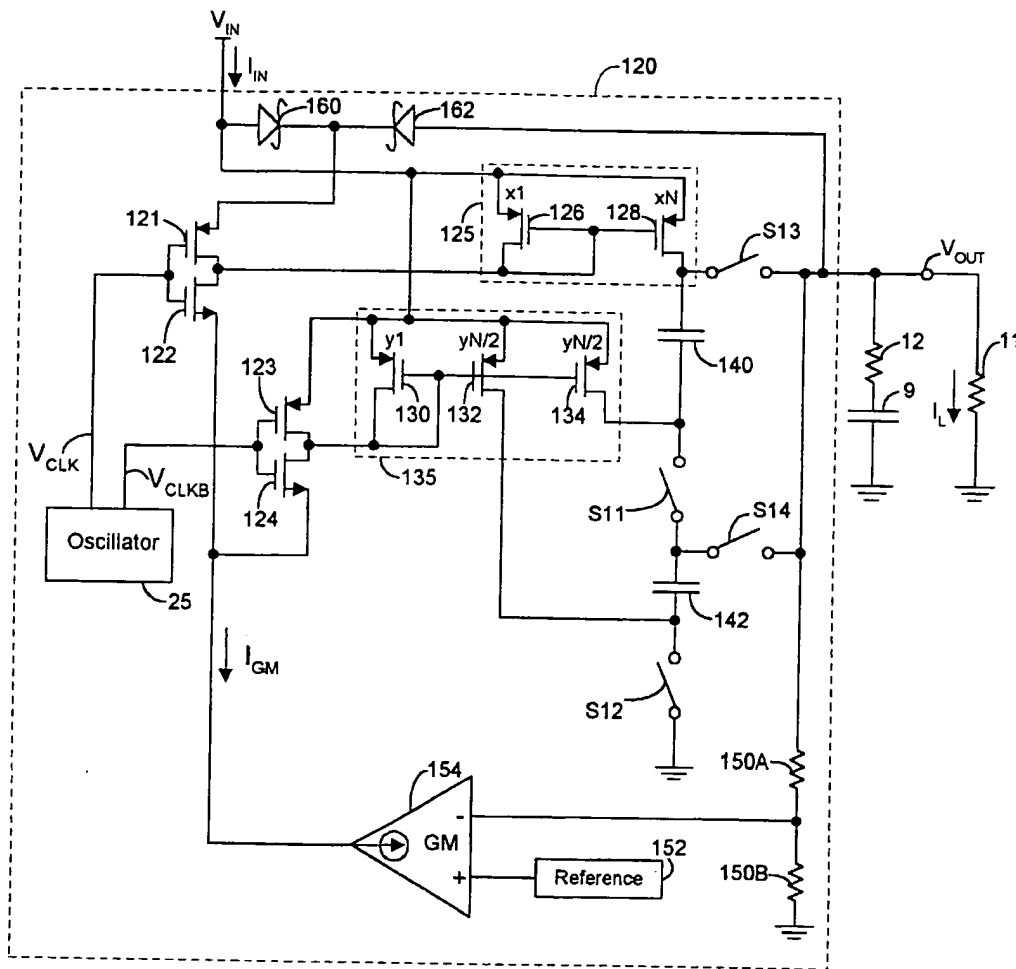


FIG. 8A

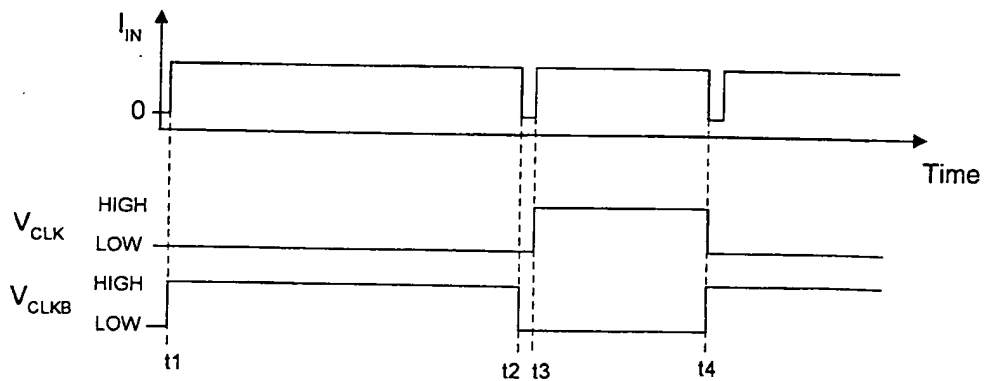


FIG. 8B

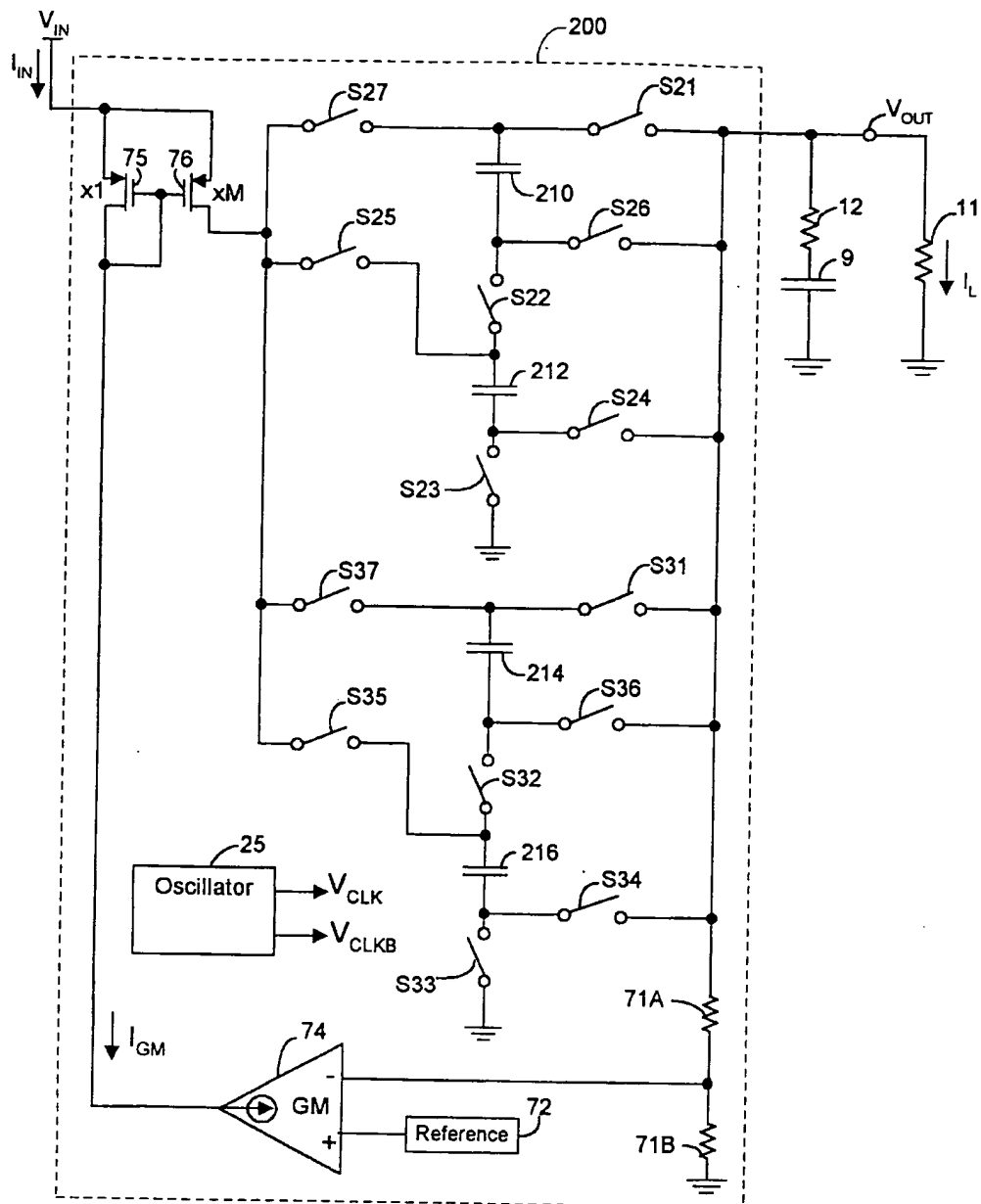


FIG. 9A

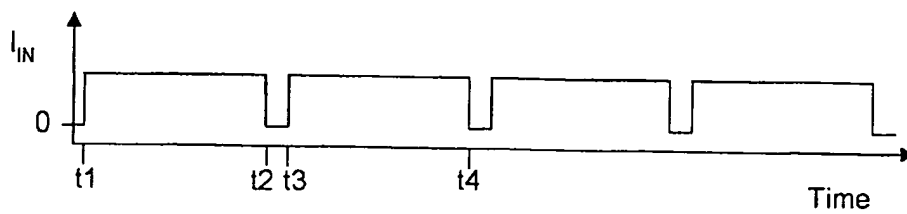


FIG. 9B



## CHARGE PUMP DC/DC CONVERTERS WITH REDUCED INPUT NOISE

### BACKGROUND OF THE INVENTION

This invention relates to charge pump DC/DC converters. More specifically, this invention relates to charge pump DC/DC converters with reduced noise at the input voltage source.

A charge pump DC/DC converter is a power supply circuit that provides a regulated output voltage to a load from an input voltage source. One type of charge pump DC/DC converter is a switching DC/DC converter power supply that uses switches to convert the input voltage to a regulated output voltage. The switches are operated in sequence to first charge a capacitor from the input voltage and then transfer the charge to the output.

However, one of the most common drawbacks of switching power supplies is the noise induced on the input voltage source due to fluctuations or variations in the current drawn by the converter power supply. When current flows from the input voltage to the capacitor, the input voltage is loaded causing it to decrease slightly. When the capacitor is decoupled from the input voltage, the input voltage rises. These voltage changes appear as noise on the input voltage bus. The magnitude of these changes in the input voltage level depends upon the equivalent series resistance of the input voltage source and the magnitude of the changes in the input current.

Certain applications such as cellular telephones, precision instrumentation, etc. are sensitive to noise generated on the input voltage. Therefore, noise on the input voltage caused by a power supply must be filtered to prevent degraded electrical performance in other circuitry that is powered from the same input voltage source.

It would therefore be desirable to provide a charge pump DC/DC converter that has reduced noise on the input voltage source.

It would therefore be desirable to provide a charge pump DC/DC converter with a substantially constant input current.

### SUMMARY OF THE INVENTION

It is an object of the present invention to provide a charge pump DC/DC converter that has reduced noise on the input voltage source.

It is an object of the present invention to provide a charge pump DC/DC converter with a substantially constant input current.

These and other objects of the present invention are provided by charge pump DC/DC converters including circuitry to reduce variations in the input current, and methods for using the same. The circuitry may include an adjustable resistor, current mirror, or current mirrors coupled to the input voltage, and feedback loop circuitry. The feedback loop circuitry is coupled to the output voltage, and responds to changes in the output voltage to control the output current of the charge pump to maintain the output voltage at the regulated value. Additional circuitry may be added to charge pumps of the present invention to provide a substantially constant input current during the blanking intervals when all of the switches are open. Charge pump DC/DC converters of the present invention include buck and boost converters.

### BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned objects and features of the present invention can be more clearly understood from the following

detailed description considered in conjunction with the following drawings, in which the same reference numerals denote the same structural elements throughout, and in which:

FIG. 1A is a schematic diagram of a prior art charge pump DC/DC converter;

FIG. 1B is a graph of the input current for the charge pump DC/DC converter shown in FIG. 1A;

FIG. 2A is a schematic diagram of another prior art charge pump DC/DC converter;

FIG. 2B is a graph of the input current for the charge pump DC/DC converter of FIG. 2A;

FIG. 3A is a schematic of a boost charge pump DC/DC converter of the present invention;

FIG. 3B is a graph of the input current and clock signals for the boost charge pump DC/DC converter of FIG. 3A;

FIG. 4A is a schematic of another boost charge pump DC/DC converter of the present invention;

FIG. 4B is a graph of the input current for the boost charge pump DC/DC converter of FIG. 4A;

FIG. 4C is another graph of the input current for the boost charge pump DC/DC converter of FIG. 4A;

FIG. 5A is a schematic of another boost charge pump DC/DC converter of the present invention;

FIG. 5B is a graph of the input current for the boost charge pump DC/DC converter of FIG. 5A;

FIG. 6A is a schematic of a buck charge pump DC/DC converter;

FIG. 6B is a graph of the input current and clock signals for the buck charge pump DC/DC converter of FIG. 6A;

FIG. 7A is a schematic of a buck charge pump DC/DC converter of the present invention;

FIG. 7B is a graph of the input current for the buck charge pump DC/DC converter of FIG. 7A;

FIG. 8A is a schematic of another boost charge pump DC/DC converter of the present invention;

FIG. 8B is a graph of the input current and clock signals for the boost charge pump DC/DC converter of FIG. 8A;

FIG. 9A is a schematic of another buck charge pump DC/DC converter of the present invention; and

FIG. 9B is a graph of the input current for the buck charge pump DC/DC converter of FIG. 9A.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One previously known charge pump DC/DC converter 10 is shown in FIG. 1A. Charge pump 10 has capacitor 8 and switches S1, S2, S3, and S4. Charge pump 10 supplies a regulated voltage  $V_{OUT}$  at an output node from input voltage  $V_{IN}$ . The equivalent series resistance of output capacitor 9 is represented by resistor 12, and resistor 11 represents a load. Switches S1/S3 are switched out of phase with switches S2/S4 by clock signals  $V_{CLK}$  and  $V_{CLKB}$ , respectively.

Circuit 10 also has resistors 13A and 13B, reference voltage source 14, and hysteretic comparator 16. When comparator 16 senses that  $V_{OUT}$  has risen to a voltage threshold set by reference 14, the output of comparator 16 goes HIGH causing oscillator 18 to stop so that switches S1-S4 remain open and no charge is transferred to  $V_{OUT}$  from  $V_{IN}$ . When  $V_{OUT}$  falls below the threshold of comparator 16, its output goes LOW, and oscillator 18 resumes the switching of switches S1-S4.

The input current into circuit 10 is represented by  $I_{IN}$  and is shown in graphical form in FIG. 1B.  $I_{IN}$  varies substan-

tially as switches S1-S4 are opened and closed, and is zero between times t0 and tx when the output of comparator 16 is HIGH. The large variations in  $I_{IN}$  caused by circuit 10 as shown in FIG. 1B produce variations in  $V_{IN}$  that correspond to undesirable low frequency noise. Low frequency noise tends to be very difficult and impractical to filter because very large and expensive filter components are needed to remove low frequency noise.

Previously known charge pump DC/DC converter is shown in FIG. 2A. Circuit 20 has capacitor 8, adjustable resistor 26, oscillator 25, and switches S1, S2, S3, and S4. Oscillator 25 provides clock signals  $V_{CLK}$  and  $V_{CLKB}$  that control the opening and closing of switches S1-S4 as discussed above with respect to FIG. 1A. Circuit 20 also has resistor divider 21A/21B, amplifier 24, and reference voltage source 22. Amplifier 24 varies the resistance of adjustable resistor 26 in response to the voltage at its non-inverting input to maintain  $V_{OUT}$  at the regulated voltage. Adjustable resistor 26 may be a field effect transistor (such as an N-channel MOSFET) that is operated in its linear region.

Input current  $I_{IN}$  is shown in FIG. 2B for circuit 20. At time t1, switches S2/S4 are closed and  $I_{IN}$  flows through adjustable resistor 26. Resistor 26 limits the current and reduces the spike input current  $I_{IN}$ . The charge stored in capacitor 8 is limited by resistor 26 when switches S2/S4 are conducting. However, at time t3 when switches S2/S4 are open and S1/S3 are closed, the current spike is still undesirably large. Circuit 20 has less noise on the input voltage source because of the reduced input current when S2/S4 conduct. Nevertheless, the variations in  $I_{IN}$  caused by circuit 20 still produce undesirably large input voltage noise characteristics in the low frequency range (i.e., at the switching frequency). Undesirable higher frequency noise is caused by variations in the input current during each blanking interval (e.g., between times t2 and t3) when all of the switches are open. Another previous known charge pump converter is the LT1054 discussed in LTC's (Linear Technology Corporation's) 1994 databook.

Charge pump DC/DC converters of the present invention may include control circuitry coupled to the input voltage that reduces variations in the input current. The control circuitry controls the input current during each phase of a switching cycle in order to reduce voltage fluctuations on the input voltage source that cause low frequency noise. A control circuit including an amplifier and a resistor divider coupled to the output voltage adjusts the current through the control circuitry so that the output current of the converter matches the load current and the output voltage remains at the regulated value. The control circuitry may include an adjustable resistor, a current mirror, or current mirrors.

Charge pump DC/DC converter 30 of the present invention is shown in FIG. 3A. Converter 30 has capacitor 8, oscillator 25, adjustable resistor 38, and switches S1, S2, S3, and S4. Switches S1-S4 (and all other switches discussed with respect to the present invention) may comprise FETs (such as MOSFETs) or BJTs (bipolar junction transistors). The circuit components are coupled in a boost arrangement so that converter 30 regulates an output voltage  $V_{OUT}$  that is higher than  $V_{IN}$ . Circuit 30 provides an output current to load 11 and maintains  $V_{OUT}$  at the regulated voltage. Output capacitor 9 is coupled to  $V_{OUT}$ . Oscillator outputs clock signals  $V_{CLK}$  and  $V_{CLKB}$  which are digital periodic pulse waveforms that control the opening and closing of switches S1, S2, S3, and S4. Clock signals  $V_{CLK}$  and  $V_{CLKB}$  are out of phase with each other, and include brief blanking intervals when both clock signals are LOW and all four switches are open (e.g.,

between times t2 and t3) to prevent shorting  $V_{IN}$  or capacitor 8 to ground or  $V_{OUT}$ .

Switches S2/S4 are closed (i.e., conducting current) when  $V_{CLKB}$  is HIGH, for example, between times t1 and t2. Switches S2/S4 are open (i.e., not conducting current) when  $V_{CLKB}$  is LOW. Switches S1/S3 are closed (i.e., conducting current) when  $V_{CLK}$  is HIGH, for example, between times t3 and t4. Switches S1/S3 are open (i.e., not conducting current) when  $V_{CLK}$  is LOW. When switches S2/S4 are closed and switches S1/S3 are open, input current  $I_{IN}$  flows from input voltage  $V_{IN}$  through adjustable resistor 38 and switch S4 to capacitor 8. An illustrative graph of the input current  $I_{IN}$  for circuit 30 is shown in FIG. 3B, wherein switches S2/S4 are closed between times t1 and t2. When switches S2/S4 close at time t1,  $I_{IN}$  increases rapidly (i.e., spikes). Between times t1 and t2, current  $I_{IN}$  ramps down according to the time constant determined by capacitor 8 and the series resistance of switches S2/S4 and resistor 38. By limiting current  $I_{IN}$ , adjustable resistor 38 reduces the input current spikes at time t1, so that variations in input current  $I_{IN}$  are reduced during the first half of each switching cycle between t1 and t2, thereby reducing undesirable low frequency noise on the input voltage.

When switches S1/S3 are closed and switches S2/S4 are open, input current  $I_{IN}$  flows from input voltage  $V_{IN}$  through adjustable resistor 38 and switch S3 to capacitor 8, and current flows from capacitor 8 through switch S1 to the load. Switches S1 and S3 are closed between times t3 and t4 in FIG. 3B. When switches S1/S3 close at time t3,  $I_{IN}$  spikes. Between times t3 and t4, current  $I_{IN}$  ramps down according to the time constant determined by capacitor 8 and the series resistance of switches S1/S3 and resistor 38. Adjustable resistor 38 reduces the input current spike at time t3 relative to circuit 20, so that variations in input current  $I_{IN}$  are reduced between times t3 and t4 during the second half of each switching cycle, thereby reducing undesirable low frequency noise at the input voltage. Thus, adjustable resistor 38 controls the input current through capacitor 8 and all four switches during each phase of the clock cycle.

The current through a capacitor is determined by the following standard equation:

$$I = C \frac{dV}{dt} \quad (1)$$

The current through a capacitor is determined by the following standard equation:

$$I = C \frac{dV}{dt} \quad (1)$$

The charge that is added to capacitor 8 from  $V_{IN}$  when switches S2 and S4 are closed equals the charge that is transferred to the load when switches S1 and S3 are closed, during a steady state condition (i.e., constant load current). The change in voltage across capacitor 8 ( $dV_C$ ) when S2 and S4 are closed equals the change in voltage across capacitor 8 ( $dV_C$ ) when S1 and S3 are closed during a steady state. Setting these quantities equal to each other from equation (1) it can be seen that:

$$dV_{IX} = dV_{IX} = \frac{I_{RX}}{C_8} t_x = \frac{I_{RX}}{C_8} t_y \quad (2)$$

where  $C_8$  is the capacitance of capacitor 8,  $t_x$  is the time period that switches S2 and S4 are closed in each switching

cycle, and  $t_{\phi}$  is the time period that switches S1 and S3 are closed in each switching cycle.  $I_{R38}$  is the average current through resistor 38, which is about the same during both time periods. Solving equation (2), it can be seen that  $t_x = t_{\phi}$ . Therefore, the optimum duty cycle for switches S1-S4 is 50% (ignoring the relatively brief blanking interval). Times  $t_x$  and  $t_{\phi}$  are determined by clock signals  $V_{CLKB}$  and  $V_{CLK}$ , respectively.

The average output current  $I_{OUT}$  of converter (i.e., the average current through switch S1) equals the load current  $I_L$  during steady state operation. Current flowing through resistor 38 is only sent to  $V_{OUT}$  for one half of each switching cycle when S1 is closed. During the other half of the switching cycle, the output current of converter 30 equals zero, because S1 is open. Therefore, the average current  $I_{R38}$  through adjustable resistor 38 must be twice the average output current  $I_{OUT}$ .

The average current through resistor 38 when switches S2 and S4 are closed is shown in the following equation:

$$I_{R38} = \frac{V_{IN} - V_{C8}}{R_{38}} \quad (3)$$

where  $R_{38}$  is the resistance of adjustable resistor 38, and  $V_{C8}$  is the average voltage across capacitor 8. The average current through resistor 38 when switches S1 and S3 are closed is shown in the following equation:

$$I_{R38} = \frac{V_{IN} + V_{C8} - V_{OUT}}{R_{38}} \quad (4)$$

The current through resistor 38 equals the current through capacitor 8, because the two elements are coupled in series during both switching states. Therefore, the average current through resistor 38 when switches S2 and S4 are closed as shown by equation (3) equals the average current through resistor 38 when S1 and S3 are closed as shown by equation (4), during a steady state. Solving equations (3) and (4), it can be shown that  $V_{C8}$  equals one half of  $V_{OUT}$ .

Substituting  $I_{R38} = 2I_{OUT} = 2I_L$  and  $V_{C8} = V_{OUT}/2$  into equation (3), one can derive the following equation:

$$R_{38} = \frac{V_{IN} - \frac{V_{OUT}}{2}}{2I_L} \quad (5)$$

The resistance value  $R_{38}$  of resistor 38 can be adjusted (by amplifier 34 as discussed below) according to equation (5) to supply the load current  $I_L$ , for selected values of  $V_{IN}$  and  $V_{OUT}$ .

For the following discussion, equation (5) can be rearranged so that  $V_{OUT} = 2V_{IN} - 4I_L R_{38}$ . Assuming for purposes of illustration that  $R_{38}$  equals zero,  $V_{IN}$  is applied across capacitor 8 when switches S2/S4 are closed. The voltage across a capacitor does not change instantaneously. Thus, when switches S1/S3 close, the voltage across capacitor 8 ( $V_{IN}$ ) plus  $V_{IN}$  is applied to  $V_{OUT}$ . Therefore,  $V_{OUT}$  equals  $2V_{IN}$  in the illustrative case where  $R_{38}$  equals zero for boost converter 30. This is the maximum value for  $V_{OUT}$ . When  $R_{38}$  has a positive non-zero value,  $V_{OUT}$  becomes less than twice  $V_{IN}$  according to the load current as shown by equation (5).

Charge pump 30 also includes a feedback loop that comprises a resistor divider including resistors 31A and 31B, reference voltage source 32, and amplifier 34. The feedback loop is used to control the resistance of variable

resistor 38 and thereby control current delivered to output capacitor 9 and load 11 to regulate output voltage  $V_{OUT}$ . The resistance of resistor 38 is set by the feedback loop circuitry to be a function of the output current. Resistor divider 31A/31B provides a voltage feedback signal proportional to  $V_{OUT}$  at the non-inverting input of amplifier 34. Reference voltage source 32 provides a constant reference voltage signal at the inverting input of amplifier 34. Amplifier 34 amplifies the difference between the feedback signal and the reference voltage, and provides an amplified signal at its output to control the resistance of adjustable resistor 38. Adjustable resistor 38 may be a field effect transistor (such as an N-channel MOSFET) that is operated in its linear region.

When load current  $I_L$  is less than the average output current delivered to load 11 by circuit 30, the excess charge is stored on output capacitor 9 and  $V_{OUT}$  increases by a small amount. The voltage feedback signal increases proportionally with  $V_{OUT}$ , causing the voltage output signal of amplifier 34 to increase. This increases the resistance of adjustable resistor 38 causing the average output current of circuit 30 to decrease so that  $V_{OUT}$  is maintained at the regulated voltage.

When load current  $I_L$  is greater than the average output current delivered to load 11 by circuit 30, charge is removed from output capacitor 9 by load current  $I_L$  and  $V_{OUT}$  decreases by a small amount. The voltage feedback signal also decreases proportionally with  $V_{OUT}$ , causing the voltage output signal of amplifier 34 to decrease. The resistance of adjustable resistor 38 now decreases, causing the average output current of circuit 30 to increase so that  $V_{OUT}$  is maintained at the regulated voltage.

Instead of variable resistor 38, DC/DC charge pump converters of the present invention may include one or more current mirrors coupled to the input voltage that conduct a substantially constant input current in a steady state condition during each phase of the switching cycle. The current mirrors control the input current during each phase of the clock cycle (except during the blanking intervals) to reduce voltage fluctuations on the input voltage source that cause noise. A feedback loop including a transconductance amplifier and a resistor divider coupled to the output voltage adjusts the current through the current mirrors so that the output current of the converter matches the load current and the output voltage stays regulated.

An embodiment of the present invention using current mirrors is shown in FIG. 4A, wherein charge pump DC/DC converter 40 includes switches S1 and S2, flying capacitor 8, inverters 41 and 42, oscillator 25, and a current mirrors 54 and 55. Converter 40 also has feedback circuitry that includes a resistor divider formed by resistors 47A and 47B, reference voltage source 48, and transconductance amplifier 49. Converter 40 also includes NOR gate 60, n-channel FET 62, p-channel FETs 61, 63 and 64, and schottky diodes 67 and 68. Transistors 43-46, 50-53, and 61-64 may be, for example, MOSFETs. Switches S1 and S2 are coupled in a boost arrangement so that converter 40 regulates an output voltage  $V_{OUT}$  that is higher than  $V_{IN}$ .

In circuit 40, switch S4 has been replaced by inverter 41 and current mirror 54, and switch S3 has been replaced by inverter 42 and current mirror 55. Transistors 43 and 44 form current mirror 54, because their gates are coupled together. Transistors 45 and 46 form current mirror 55, because their gates are coupled together. Transistors 44 and 46 may each comprise a single transistor or multiple transistors coupled together in parallel that have effective gate width-to-length areas that are N times the gate width-to-length areas of

transistors 43 and 45, respectively. This provides current mirrors 54 and 55 with a current gain of  $N$ . Current mirror transistors 43-46 and other current mirror transistors discussed with respect to the present invention may be FETs or BJTs.

Oscillator 25 outputs digital clock signals  $V_{CLK}$  and  $V_{CLKB}$  as with the previous embodiment of FIG. 3A. Clock signals  $V_{CLK}$  and  $V_{CLKB}$  oscillate out of phase with a 50% duty cycle (and may have a blanking interval) as shown in FIG. 3B. Clock signal  $V_{CLK}$  controls the opening and closing of switch S1, and clock signal  $V_{CLKB}$  controls the opening and closing of switch S2.

In the first half of a switch cycle,  $V_{CLK}$  is LOW and  $V_{CLKB}$  is HIGH. When  $V_{CLKB}$  is LOW, transistor 52 is ON, transistor 53 is OFF, and switch S1 is open. When transistor 52 is ON, the output of inverter 42 and the gates of transistors 45 and 46 are HIGH (at  $V_{IN}$ ), causing transistors 45 and 46 to be OFF. This turns OFF current mirror 55. Because  $V_{CLKB}$  is HIGH, transistor 50 is OFF, transistor 51 is ON, and switch S2 is closed. When transistor 51 is ON, the gates of transistors 43 and 44 are pulled down by the transconductance amplifier 49 output current  $I_{GM}$ , turning ON current mirror 54. Transconductance amplifier 49 sinks current  $I_{GM}$  through its output. Thus, when transistor 51 is ON, transistor 43 is ON and current  $I_{GM}$  flows from  $V_{IN}$  through transistors 43 and 51 to ground through the output of transconductance amplifier 49. Transistor 44 is also ON when transistor 51 is ON, and current flows from  $V_{IN}$  through transistor 44 charging up capacitor 8.

Because the gate width-to-length area of transistor 44 is  $N$  times the gate width-to-length area of transistor 43, the current that flows through transistor 44 equals  $N$  times the current  $I_{GM}$  that flows through transistor 43. So long as transconductance amplifier 49 sinks a constant current  $I_{GM}$  during a steady state load current, the current through transistors 43 and 44, and the input current  $I_{IN}$  remains constant while switch S2 is closed.  $I_{IN}$  is defined by the following equation when switch S2 is closed:

$$I_{IN} = I_{M43} + I_{M44} = I_{GM}(1+N) \quad (6)$$

where  $I_{M43}$  is the current through transistor 43,  $I_{M44}$  is the current through transistor 44,  $I_{GM}$  is the output current of amplifier 49, and  $I_{M43}$  equals  $I_{GM}$  when transistor 43 is ON.

The source of transistor 50 is coupled to the cathodes of schottky diodes 67 and 68 as shown in FIG. 4A. The anode of diode 67 is coupled to  $V_{IN}$ , and the anode of diode 68 is coupled to  $V_{OUT}$ . Thus, when transistor 50 is ON, the source of transistor 50 is coupled to the larger of  $V_{IN}$  or  $V_{OUT}$  through diodes 67 or 68. In circuit 40,  $V_{OUT}$  is generally larger than  $V_{IN}$ , because it is a boost converter.

During the second half of a switch cycle,  $V_{CLK}$  is HIGH and  $V_{CLKB}$  is LOW. When  $V_{CLKB}$  is LOW, transistor 50 is ON, transistor 51 is OFF, and switch S2 is open. When transistor 50 is ON, the output of inverter 41 and the gates of transistors 43 and 44 are HIGH (at  $V_{OUT}$ ), causing transistors 43 and 44 to be OFF. This turns OFF current mirror 54. Because  $V_{CLK}$  is HIGH, transistor 52 is OFF, transistor 53 is ON, and switch S1 is closed. When transistor 53 is ON, the gates of transistors 45 and 46 are pulled LOW by the transconductance amplifier 49 output current  $I_{GM}$ , turning ON current mirror 55. Thus, when transistor 53 is ON, transistor 45 is ON and current  $I_{GM}$  flows from  $V_{IN}$  through transistors 45 and 53 to ground through the output of transconductance amplifier 49. Transistor 46 is also ON when transistor 53 is ON, causing current to flow from  $V_{IN}$  through transistor 46 to capacitor 8, and from capacitor 8 through switch S1 to  $V_{OUT}$ .

Because the gate width-to-length area of transistor 46 is  $N$  times the gate width-to-length area of transistor 45, the current that flows through transistor 46 equals  $N$  times the current  $I_{GM}$  that flows through transistor 45. So long as transconductance amplifier 49 sinks a constant current  $I_{GM}$  during a steady state load current, the current through transistors 45 and 46, and the input current  $I_{IN}$  remain constant while switch S1 is closed.  $I_{IN}$  is defined by equation (7) when switch S1 is closed:

$$I_{IN} = I_{M45} + I_{M46} = I_{GM}(1+N) \quad (7)$$

where  $I_{M45}$  is the current through transistor 45,  $I_{M46}$  is the current through transistor 46,  $I_{GM}$  is the output current of amplifier 49, and  $I_{M45}$  equals  $I_{GM}$  when transistor 45 is ON. As shown by equations (6) and (7), current  $I_{IN}$  when switch S2 is closed equals current  $I_{IN}$  when S1 is closed.

If transconductance amplifier 49 sinks a constant current  $I_{GM}$ ,  $I_{IN}$  remains constant when either of switches S1 or S2 are closed and conducting current. Thus, current mirrors 54 and 55 control the current through capacitor 8 and the switches during each phase of the clock signal. During the blanking interval when  $V_{CLK}$  and  $V_{CLKB}$  are LOW concurrently, and switches S1 and S2 are open,  $I_{IN}$  is zero (without NOR gate 60 and transistors 61-64 which are discussed below). Therefore,  $I_{IN}$  varies between a constant value and zero every half cycle of  $V_{CLK}$  during a steady state as shown, for example, in the graph of FIG. 4B. The circuit of FIG. 4A, therefore, reduces low frequency noise on the input voltage source by maintaining the input current  $I_{IN}$  at a constant value when switches S1 and S2 are closed.

The average output current  $I_{OUT}$  of converter 40 (i.e., the average current through switch S1 over time) equals the load current  $I_L$  during a steady state. When switch S1 is open, the instantaneous output current of converter 40 equals zero. During the other half of the switching cycle, output current flows to  $V_{OUT}$  through transistor 46 when S1 is closed. Therefore, the current through transistor 46 must equal twice the load current  $I_L$ . The current through transistor 46 equals  $N$  times  $I_{GM}$ , as discussed above. The relationship between the load current and  $I_{GM}$  is shown by the following equation:

$$I_L = 2N \cdot I_{GM} \quad (8)$$

As the load current changes,  $I_{GM}$  can be adjusted by amplifier 49 (discussed below) to match the load current according to equation (8).

The charge that is added to capacitor 8 from  $V_{IN}$  when switch S2 is closed equals the charge that is transferred to the load when switch S1 is closed, during a steady state condition. Assuming for purposes of illustration that  $R_{DS(on)}$  of transistors 44 and 46 equals zero,  $V_{IN}$  is applied across capacitor 8 when switch S2 is closed. When switch S1 closes, the voltage across capacitor 8 ( $V_{IN}$ ) plus  $V_{IN}$  is applied to  $V_{OUT}$ . Therefore,  $V_{OUT}$  equals  $2V_{IN}$  in the illustrative case where the  $R_{DS(on)}$  for transistors 44 and 46 equals zero for boost converter 40. This is the maximum value for  $V_{OUT}$ . As  $R_{DS(on)}$  is increased above zero in a steady state,  $V_{OUT}$  becomes less than twice  $V_{IN}$ . Thus,  $V_{OUT} < 2V_{IN}$ .

The change in voltage across capacitor 8 ( $dV_{\alpha}$ ) when S2 is closed equals the change in voltage across capacitor 8 ( $dV_{\beta}$ ) when S1 is closed. Setting these quantities equal to each other from equation (1) it can be seen that:

$$dV_{IX} = dV_{IY} = \frac{N \cdot I_{GM}}{C_8} t_x = \frac{N \cdot I_{GM}}{C_8} t_y \quad (9)$$

where  $C_8$  is the capacitance of capacitor 8,  $I_{GM}$  is the output current of transconductance amplifier 49,  $t_x$  is the time period that switch S2 is closed in each switching cycle, and  $t_y$  is the time period that switch S1 is closed in each switching cycle. Solving equation (9), it can be seen that  $t_x = t_y$ . Therefore, the optimum duty cycle for switches S1 and S2 is 50%. Times  $t_x$  and  $t_y$  are determined by clock signals  $V_{CLKB}$  and  $V_{CLK}$ , respectively.

Circuit 40 regulates the output voltage  $V_{OUT}$  to a predetermined value using the feedback loop comprising resistors 47A and 47B, reference voltage source 48, and transconductance amplifier 49. Resistor divider 47A/47B outputs a voltage feedback signal at the inverting input of amplifier 49, and voltage source 48 outputs a constant reference voltage at the non-inverting input of amplifier 49. When  $V_{OUT}$  varies from the predetermined value by a certain amount (e.g., due to changes in the load current), the feedback voltage at the inverting input of amplifier 49 varies proportionally to  $V_{OUT}$ . Amplifier 49 then varies the current  $I_{GM}$  and sinks it to ground in response to the changes in the feedback voltage at its inverting input.

When  $V_{OUT}$  increases in response to a decrease in the load current, the output current of amplifier 49 decreases so that the current through current mirrors 43/44 and 45/46 decreases in each subsequent cycle. The output current of converter 40 is reduced in each cycle to match the load current and to maintain  $V_{OUT}$  at a regulated voltage. When  $V_{OUT}$  decreases in response to an increase in the load current, the output current of amplifier 49 increases so that the current through current mirrors 43/44 and 45/46 increases in each subsequent cycle. The output current of converter 40 increases in each cycle to match the load current and to maintain  $V_{OUT}$  at a regulated voltage.

Because charge is only transferred to output capacitor 9 every half cycle of  $V_{CLK}$  when switch S1 is closed,  $V_{OUT}$  oscillates up and down during every cycle due to the presence of equivalent series resistance 12 and the charging and discharging of capacitor 9 in the output circuit. If the switching frequency is not much higher than the pole set by output capacitor 9 and load 11, the output current of amplifier 49 also ripples up and down with the output voltage in each switching cycle. This causes a triangle shaped waveform of input current  $I_{IN}$  which increases noise at the input voltage source. To reduce this ripple current effect, the output capacitor 9 or the switching frequency can be increased to reduce output voltage ripple. Reducing the output voltage ripple can provide a substantially constant input current when switches S1 or S2 are closed (during a steady state), as shown in FIG. 4B.

Charge pump DC/DC converters of the present invention may also shunt input current  $I_{IN}$  to ground during the blanking intervals to produce a more constant  $I_{IN}$  during each cycle. An example of circuitry that may be added to a DC/DC converter of the present invention is shown in FIG. 4A. NOR gate 60 and FET transistors 61–64 may be added to charge pump 40 as shown in FIG. 4A to shunt current to ground during the blanking intervals.

Blanking intervals occur twice during each period of the clock signals when both  $V_{CLK}$  and  $V_{CLKB}$  are LOW concurrently as shown in FIG. 3B. When either  $V_{CLK}$  and  $V_{CLKB}$  are HIGH, the output of NOR gate 60 is LOW causing transistor 61 to be ON and transistor 62 to be OFF. Transistors 61 and 62 form an inverter. When p-channel

transistor 61 is ON, p-channel transistors 63 and 64 are OFF, because the gates of transistors 63 and 64 are pulled HIGH. Transistors 63 and 64 form a current mirror, because their gates are coupled together.  $N$  is the current gain ratio of transistor 64 to transistor 63. Thus,  $N$  is the gate width-to-length ratio of transistor pairs 64 to 63, 44 to 43, and 46 to 45.

The source of transistor 62 is coupled to the output of transconductance amplifier 49. When both  $V_{CLK}$  and  $V_{CLKB}$  are LOW concurrently, the output of NOR gate 60 is HIGH, causing N-channel FET 62 to be ON and p-channel FET 61 to be OFF. When transistor 62 is ON, amplifier 49 sinks current to ground through transistor 62, turning transistors 63 and 64 ON. When transistor 62 is ON,  $I_{GM}$  flows from  $V_{IN}$  through transistors 63 and 62 and to ground through the output of amplifier 49. Also, when transistor 62 is ON, current flows from  $V_{IN}$  through transistor 64 to ground. Therefore,  $I_{IN}$  is defined by the following equation during the blanking intervals with circuitry 60–64:

$$I_{IN} = I_{M63} + I_{M64} = I_{GM}(1+N) \quad (10)$$

where  $I_{M63}$  is the current through transistor 63 and  $I_{M64}$  is the current through transistor 64. Therefore  $I_{IN}$  during the blanking interval equals  $I_{IN}$  when S1 is closed and when S2 is closed. Current  $I_{IN}$  flows continuously throughout each switching cycle and is substantially constant during a steady state as shown in FIG. 4C (with circuitry 60–64). The gate capacitance of transistors 63 and 64 should not be too large so that these transistors can turn ON quickly during the relatively brief blanking intervals.

A further embodiment of the present invention is illustrated in FIG. 5A. Charge pump DC/DC converter 70 includes oscillator 25, p-channel FETs 75 and 76, resistors 71A and 71B, reference voltage source 72, transconductance amplifier 74, capacitor 8, and switches S1, S2, S3, and S4. Switches S1–S4 are coupled in a boost arrangement so that converter 70 regulates an output voltage  $V_{OUT}$  that is higher than  $V_{IN}$ . Transistors 75 and 76 form a current mirror, because their gates are coupled together and to the output of transconductance amplifier 74. Transistor 76 conducts  $M$  times the current conducted by transistor 75, because  $M$  is the current gain ratio of transistors 76 to 75.

Switches S2 and S4 are switched out of phase with switches S1 and S3 in each switching cycle by oscillator 25 as with the previous embodiments. The time that switches S2/S4 are ON equals the time that switches S1/S3 are ON, as with the previous embodiment. Thus, switches S1–S4 each have a 50% duty cycle.

When switches S4 and S2 are closed, current flows from  $V_{IN}$  to capacitor 8 through transistor 76 and switch S4. When switches S3 and S1 are closed, current flows from  $V_{IN}$  to capacitor 8 through transistor 76 and switch S3, and from capacitor 8 through switch S1 to  $V_{OUT}$ . Input current  $I_{IN}$  equals the current through transistor 75 plus the current through transistor 76. A continuous current flows through transistor 75 that equals the output current  $I_{GM}$  of transconductance amplifier 74. The current through transistor 75 is independent of the switch states of switches S1–S4. When either of switches S3 or S4 are closed, a current flows through transistor 76 from  $V_{IN}$ . That current equals  $M$  times the current  $I_{GM}$  through transistor 75.

The current through transistor 76 is substantially constant as long as the current  $I_{GM}$  through transistor 75 is constant, because  $M$  is a constant. Transconductance amplifier 74 sinks a constant current  $I_{GM}$  to ground during a steady state as long as the switching frequency is much higher than the pole caused by capacitor 9 and load 11. Therefore, the

current through transistors 75 and 76 and  $I_{IN}$  remains constant during a steady state. The current through transistor 75 is typically a small fraction ( $1/M$ ) of the current through transistor 76 (e.g.,  $M=100$ ). Therefore,  $I_{IN}$  equals approximately  $M$  times  $I_{GM}$ , except during the blanking intervals when  $I_{IN}$  equals zero. An example  $I_{IN}$  waveform during a steady state is shown in FIG. 5B. Current mirror 75/76 controls the current through capacitor 8 and the four switches during each phase of the clock cycle.

The average output current  $I_{OUT}$  of converter 70 (i.e., the average current through switch S1 over time) equals the load current  $I_L$  during a steady state. When switch S1 is open, the instantaneous output current of converter 70 equals zero. During the other half of the switching cycle, output current flows to  $V_{OUT}$  through transistor 76 when S1/S3 are closed. Therefore, the average current through transistor 76 must equal twice the average output current  $I_{OUT}$ . The relationship between the load current and  $I_{GM}$  is shown by the following equation:

$$I_L = 2M I_{GM} \quad (11)$$

The maximum value for  $V_{OUT}$  in converter 70 equals  $2V_{IN}$  in the illustrative case where the  $R_{DS(on)}$  for transistor 76 equals zero, as with the previous embodiment.

Resistors 71A and 71B form a resistor divider that outputs a voltage feedback signal proportional to  $V_{OUT}$  at the inverting input of transconductance amplifier 74. Reference voltage source 72 outputs a constant voltage at the non-inverting input of amplifier 74. Transconductance amplifier 74 varies the amount of current it sinks to ground through transistor 75 as the voltage feedback signal at its inverting input changes in order to regulate  $V_{OUT}$ .

The output current of DC/DC converter 70 varies with output current  $I_{GM}$  of amplifier 74 to match the load current. When  $V_{OUT}$  increases, transconductance amplifier 74 decreases  $I_{GM}$ , causing the current through transistor 76 and the output current of converter 70 to decrease. When  $V_{OUT}$  decreases, transconductance amplifier 74 increases  $I_{GM}$ , causing the current through transistor 76 and the output current of converter 70 to increase. Amplifier 74 causes the current through transistors 75 and 76 to increase or decrease so that the average output current of converter 70 equals the load current by monitoring the voltage feedback signal.

A further charge pump DC/DC converter is shown in FIG. 6A. Charge pump DC/DC converter 90 includes oscillator 25, current mirror transistors 75 and 76, reference voltage source 72, transconductance amplifier 74, capacitor 8, resistors 71A and 71B, and switches S5, S6, S7, and S8. Switches S5-S8 are coupled in a buck arrangement so that DC/DC converter 90 provides an output voltage  $V_{OUT}$  that is lower than input voltage  $V_{IN}$ . Resistors 71A/71B, reference 72, transconductance amplifier 74, and mirror transistors 75 and 76 operate to regulate  $V_{OUT}$  as discussed above with respect to boost converter 70 in FIG. 5A. Transconductance amplifier 74 sets its output current  $I_{GM}$  to adjust the output current of converter 90 based on the voltage feedback signal at its inverting input.

In buck charge pump DC/DC converter 90, switches S5 and S6 are closed together while switches S7 and S8 are open in the first phase of each switching cycle, and switches S7 and S8 are closed together while switches S5 and S6 are open in the second phase of each switching cycle. Switches S5-S8 each have a 50% duty cycle. Switches S5 and S6 are closed when  $V_{CLK}$  is HIGH and open when  $V_{CLK}$  is LOW. Switches S7 and S8 are closed when  $V_{CLKB}$  is HIGH and open when  $V_{CLKB}$  is LOW. The clock signals are shown in FIG. 6B.

When switches S5 and S6 are closed, capacitor 8 is coupled to  $V_{OUT}$  through switch S5 and to ground through switch S6. Therefore, the voltage on capacitor 8 equals  $V_{OUT}$ . Switches S7 and S8 are closed after switches S5 and S6 open. Capacitor 8 is then coupled to the drain of transistor 76 through switch S8 and to  $V_{OUT}$  through switch S7. Current flows from  $V_{IN}$  to capacitor 8 through switch S8 and transistor 76, and current flows from capacitor 8 through switch S7 to load 11. The voltage drop across capacitor 8 is still at  $V_{OUT}$  when switches S7 and S8 close. The voltage on the upper plate of capacitor 8 (coupled to switch S8) rises to  $2V_{OUT}$ , because the lower plate of capacitor 8 is coupled to  $V_{OUT}$  through switch S7. The voltage across transistor 76 is now  $V_{IN} - 2V_{OUT}$ . Therefore, the regulated value of  $V_{OUT}$  must be less than or equal to one half of  $V_{IN}$  so that current does not flow from  $V_{OUT}$  to  $V_{IN}$  ( $V_{OUT} \leq V_{IN}/2$ ).

The current through transistor 76 is substantially constant as long as the current through transistor 75 ( $I_{GM}$ ) is constant, and the switching frequency is much higher than the pole caused by capacitors 9 and 11, as discussed above. Therefore, the current through transistor 76 and  $I_{IN}$  remains constant during a steady state when S8 is closed. An example  $I_{IN}$  waveform during a steady state is shown in FIG. 6B.  $I_{IN}$  is approximately zero when  $V_{CLKB}$  is LOW, because switch S8 is open, transistor 76 is OFF, and the current through transistor 75 is negligible (e.g., between t2 and t4).

The average output current  $I_{OUT}$  of converter 90 equals the load current  $I_L$  during a steady state. Output current flows to  $V_{OUT}$  from capacitor 8 during each half of the switching cycle when S5 is closed and when S7 is closed. The output current of converter 90 equals the current through transistor 76 when it is ON ( $V_{CLKB}$  HIGH). The current through transistor 76 when it is ON equals approximately  $M$  times  $I_{GM}$ , as discussed above. The relationship between the load current and  $I_{GM}$  is shown by equation (12):

$$I_L = M I_{GM} \quad (12)$$

The feedback loop (comprising amplifier 74, resistor divider 71A/71B, and reference 72) determines the output current of converter 90 by varying output current  $I_{GM}$  according to equation (12) so that the current through transistor 76 when it is ON equals  $I_L$ .

Current mirror transistor 76 sets the amount of current that flows to capacitor 8 when switches S7 and S8 are closed, thereby providing a substantially constant current  $I_{IN}$ , as shown in FIG. 6B between times t1 and t2. Converter 90 therefore reduces noise at the input voltage by providing a more constant input current when switch S8 is closed.

A further embodiment of the present invention is illustrated in FIG. 7A. Charge pump DC/DC converter 110 in FIG. 7A supplies output current to load 11 to regulate output voltage  $V_{OUT}$ . Charge pump 110 includes resistors 71A and 71B, transconductance amplifier 74, reference voltage source 72, current mirror transistors 75 and 76, oscillator 25, capacitors 8 and 100, and switches S5, S6, S7, S8, S15, S16, S17, and S18. Switches S5-S8 and switches S15-S18 comprise two buck DC/DC converters that are coupled in parallel with each other between the drain of transistor 76 and  $V_{OUT}$ . In buck charge pump DC/DC converter 110, switches S5-S8, oscillator 25, transconductance amplifier 74, reference 72, and resistor divider 71A/71B operate as discussed above with respect to FIG. 6A.

Switches S15/S16 are switched out of phase with switches S5/S6, and switches S17/S18 are switched out of phase with switches S7/S8. Switches S7, S8, S15 and S16 are closed when  $V_{CLKB}$  is HIGH and open when  $V_{CLKB}$  is LOW. Switches S5, S6, S17, and S18 are closed when  $V_{CLK}$  is

HIGH, and open when  $V_{CLK}$  is LOW. Switches S15–S18 each have a 50% duty cycle.

When switches S15 and S16 are closed, capacitor 100 is coupled to  $V_{OUT}$  through switch S15 and to ground through switch S16. Therefore the voltage on capacitor 100 equals  $V_{OUT}$ . Switches S17 and S18 are closed after switches S15 and S16 open. Capacitor 100 is then coupled to transistor 76 through switch S18 and to  $V_{OUT}$  through switch S17. Current flows from  $V_{IN}$  to capacitor 100 through transistor 76 and switch S18, and current flows from capacitor 100 through switch S17 to load 11. Because the voltage drop across a capacitor cannot change instantaneously, the voltage drop across capacitor 100 is still  $V_{OUT}$  at the moment that switches S17 and S18 close. The voltage on the left plate of capacitor 100 (coupled to switch S18) rises to  $2V_{OUT}$  because the right plate of capacitor 100 is coupled to  $V_{OUT}$  through switch S17. Therefore,  $V_{OUT}$  must be less than or equal to one half of the voltage of  $V_{IN}$  for DC/DC converter 110 to properly regulate  $V_{OUT}$  ( $V_{OUT} \leq V_{IN}/2$ ), as with converter 90.

By inspection, it can be seen that converter 110 has two charge pump DC/DC converters working in parallel: switches S5–S8 and switches S15–S18. Each converter provides one half of the required load current  $I_L$ . The current through transistor 76 ( $M \cdot I_{GM}$ ) charges up capacitor 8 with one half of the load current when S8 is closed (S18 open). The current through transistor 76 ( $M \cdot I_{GM}$ ) charges up capacitor 100 with one half of the load current when S18 is closed (S8 open). Thus, the load current is determined by the following equation:

$$I_L = \frac{M \cdot I_{GM}}{2} \quad (13)$$

The input current  $I_{IN}$  is continuously flowing from  $V_{IN}$  through transistor 76 during each half cycle except during the blanking intervals. The input current  $I_{IN}$  is constant as long as  $I_{GM}$  is constant as shown by the following equation:

$$I_{IN} = (M+1) \cdot I_{GM} \quad (14)$$

A graph of  $I_{IN}$  is shown in FIG. 7B. Current mirror transistors 75/76 provide a constant input current  $I_{IN}$  during each phase of the switching cycle thereby reducing noise at the input voltage source.

A further embodiment of a boost charge pump DC/DC converter of the present invention is illustrated in FIG. 8A. Converter 120 in FIG. 8A includes oscillator 25, an inverter formed by P-channel FET 121 and N-channel FET 122, an inverter formed by P-channel FET 123 and N-channel FET 124, current mirror 125 that includes P-channel FETs 126 and 128, current mirror 135 that includes P-channel FETs 130, 132 and 134, capacitors 140 and 142, switches S11, S12, S13, and S14, resistors 150A and 150B, reference voltage source 152, transconductance amplifier 154, and schottky diodes 160 and 162.

Transistors 126 and 128 form a current mirror because their gates are coupled together. Transistors 130, 132, and 134 form a current mirror because their gates are coupled together.  $N$  is the current gain ratio of transistor 128 to transistor 126.  $N/2$  is the current gain ratio of transistors 132 and 134 to transistor 130.

The source of transistor 121 is coupled to the cathodes of schottky diodes 160 and 162 as shown in FIG. 8A. The anode of diode 160 is coupled to  $V_{IN}$ , and the anode of diode 162 is coupled to  $V_{OUT}$ . Thus, when transistor 121 is ON, the source of transistor 121 is coupled to the larger of  $V_{IN}$

or  $V_{OUT}$  through diodes 160 or 162. In circuit 120,  $V_{OUT}$  is generally larger than  $V_{IN}$ , because it is a boost converter so that transistor 121 is coupled to  $V_{OUT}$  when it conducts current.

Oscillator 25 outputs digital clock signals  $V_{CLK}$  and  $V_{CLKB}$ . Clock signals  $V_{CLK}$  and  $V_{CLKB}$  may have a blanking interval as shown in FIG. 8B. Clock signal  $V_{CLK}$  controls the opening and closing of switches S11 and S12, and clock signal  $V_{CLKB}$  controls the opening and closing of switches S13 and S14. When  $V_{CLKB}$  is LOW, transistor 123 is ON, transistor 124 is OFF, and switches S13 and S14 are open. When transistor 123 is ON, the output of inverter 123/124 and the gates of P-channel transistors 130, 132, and 134 are HIGH (at  $V_{IN}$ ), causing transistors 130, 132, and 134 to be OFF. When  $V_{CLK}$  is HIGH, transistor 121 is OFF, transistor 122 is ON, and switches S11 and S12 are closed. When transistor 122 is ON, the gates of transistors 126 and 128 are pulled down by the output current  $I_{GM}$  of transconductance amplifier 154. Thus, when transistor 122 is ON, transistor 126 is ON and current  $I_{GM}$  flows from  $V_{IN}$  through transistors 126 and 122 to ground through the output of transconductance amplifier 154.  $I_{GM}$  is the output current of amplifier 154. Transistor 128 is also ON when transistor 126 is ON, causing current  $N \cdot I_{GM}$  to flow from  $V_{IN}$  through transistor 128 and charging up capacitors 140 and 142.

When  $V_{CLK}$  is LOW, transistor 121 is ON, transistor 122 is OFF, and switches S11 and S12 are open. When transistor 121 is ON, the output of inverter 121/122 and the gates of transistors 126 and 128 are HIGH (at  $V_{OUT}$ ), causing transistors 126 and 128 to be OFF. When  $V_{CLKB}$  is HIGH, transistor 123 is OFF, transistor 124 is ON, and switches S13 and S14 are closed. When transistor 124 is ON, the gates of transistors 130, 132, and 134 are pulled down by the output current  $I_{GM}$  of transconductance amplifier 154. Thus, when transistor 124 is ON, transistor 130 is ON and current  $I_{GM}$  flows from  $V_{IN}$  through transistors 130 and 124 to ground through the output of transconductance amplifier 154. Transistors 132 and 134 are also ON when transistor 130 is ON. A current equal to  $N \cdot I_{GM}/2$  flows from  $V_{IN}$  through transistor 132 and capacitor 142 to  $V_{OUT}$ . A current equal to  $N \cdot I_{GM}/2$  also flows from  $V_{IN}$  through transistor 134 and capacitor 140 to  $V_{OUT}$ .

Because the gate width-to-length ratio of transistor 128 is  $N$  times the gate width-to-length ratio of transistor 126, the current that flows through transistor 128 equals  $N$  times the current  $I_{GM}$  that flows through transistor 126. So long as transconductance amplifier 154 sinks a constant current during a steady state load current, the current through transistors 126 and 128, and the input current  $I_{IN}$  remains constant while switches S11 and S12 are closed.  $I_{IN}$  is defined by the following equation when switches S11 and S12 are closed, where  $I_{GM}$  is the current through transistor 126 and  $I_{M128}$  is the current through transistor 128:

$$I_{IN} = I_{GM} + I_{M128} = I_{GM}(1+N) \quad (15)$$

Because the gate width-to-length area of transistors 132 and 134 are each  $N/2$  times the gate width-to-length area of transistor 130, the current that flows through each of transistors 132 and 134 equals  $N/2$  times the current  $I_{GM}$  that flows through transistor 130. So long as transconductance amplifier 154 sinks a constant current during a steady state load current, the current through transistors 130, 132 and 134, and the input current  $I_{IN}$  remain constant while switches S13 and S14 are closed.  $I_{IN}$  is defined by equation (16) when switches S13 and S14 are closed, where  $I_{GM}$  is the current through transistor 130,  $I_{M132}$  is the current through transistor 132, and  $I_{M134}$  is the current through transistor 134:



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$$I_{IN} = I_{GM} + I_{M132} + I_{M134} = I_{GM}(1+N) \quad (16)$$

Thus, if transconductance amplifier 154 sinks a constant current  $I_{GM}$ ,  $I_{IN}$  remains constant when switches S11/S12 or S13/S14 are closed.

During the blanking interval when  $V_{CLK}$  and  $V_{CLKB}$  are LOW concurrently, and switches S1 and S2 are open,  $I_{IN}$  is zero. Therefore,  $I_{IN}$  varies between a constant value and zero twice during every cycle of the clock signals during a steady state as shown, for example, in the graph of FIG. 8B. The circuit of FIG. 8A, therefore, reduces low frequency noise at the input voltage source by maintaining the input current  $I_{IN}$  at a constant value when switches S11/S12 or S13/S14 are closed.

The charge that is added to capacitor 140 from  $V_{IN}$  when switches S11 and S12 are closed equals the charge that is transferred to the load when switches S13 and S14 are closed, during a steady state condition. Therefore, the change in voltage across capacitor 140 ( $dV_{1A}$ ) when S11 and S12 are closed equals the change in voltage across capacitor 140 ( $dV_{1B}$ ) when S13 and S14 are closed. Setting these quantities equal to each other from equation (1) it can be seen that:

$$dV_{1A} = dV_{1B} = \frac{N \cdot I_{GM}}{C_{140}} t_A = \frac{N}{2} \cdot \frac{I_{GM}}{C_{140}} t_B \quad (17)$$

where  $C_{140}$  is the capacitance of capacitor 140,  $t_A$  is the time period that switches S11 and S12 are closed in each switching cycle, and  $t_B$  is the time period that switches S13 and S14 are closed in each switching cycle. Times  $t_A$  and  $t_B$  are determined by clock signals  $V_{CLK}$  and  $V_{CLKB}$ , respectively, that are shown for example, in FIG. 8B. Solving equation (17), it can be seen that  $T_B = 2T_A$ . Therefore, switches S13 and S14 are closed twice as long as switches S11 and S12 are closed in each switching cycle.

Assuming for purposes of illustration that the  $R_{DS(on)}$  of transistors 128, 132 and 134 equals zero,  $V_{IN}$  is applied across capacitors 140 and 142 when switches S11 and S12 are closed. One half of  $V_{IN}$  drops across capacitor 140, and one half of  $V_{IN}$  drops across capacitor 142. When switch S13 and S14 close, the voltage across capacitor 140 ( $V_{IN}/2$ ) plus  $V_{IN}$  is applied to  $V_{OUT}$ . Also, the voltage across capacitor 142 ( $V_{IN}/2$ ) plus  $V_{IN}$  is applied to  $V_{OUT}$ . Therefore,  $V_{OUT}$  equals  $3/2$  times  $V_{IN}$  in the illustrative case where the  $R_{DS(on)}$  for transistors 128, 132, and 134 equals zero for boost converter 120. This is the maximum value for  $V_{OUT}$ . When  $R_{DS(on)}$  is increased above zero in a steady state,  $V_{OUT}$  becomes less than  $3V_{IN}/2$ . Thus,  $V_{OUT} \leq 3V_{IN}/2$ . As the load current changes,  $I_{GM}$  can be adjusted by amplifier 154 (discussed below) to maintain the same input-to-output voltage ratio.

To achieve a constant input current in each phase of the clock signal in boost converters of the present invention, the duty cycle ratio of at least one of the switches is selected to be equal to the minimum input-to-output voltage ratio. For example, minimum input-to-output voltage ratio of circuit 20 is  $2/3$  of that in circuit 120 of FIG. 8A. The duty cycle ratio of switches S13/S14 is also  $2/3$  with respect to the switching period. The duty cycle ratio of the switches may be selected to obtain a different input-to-output voltage ratio and to achieve constant input current.

The average output current  $I_{OUT}$  of converter 120 equals the load current  $I_L$  during a steady state condition. The output current of converter 120 is zero when switches S13 and S14 are open, because there is no current path to the

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output node. The output current of converter 120 equals  $N$  times  $I_{GM}$  (the current through transistor 132 plus the current through transistor 134) when switches S13 and S14 are closed. Switches S13 and S14 are closed during  $2/3$  of the time period of each cycle as stated above. Therefore, the load current  $I_L$  is defined by the following equation:

$$I_L = \frac{2}{3} N \cdot I_{GM} \quad (18)$$

where  $N$  is substantially larger than 1 (e.g.,  $N=100$ ), and thus  $I_{IN}$  equals  $N$  times  $I_{GM}$ .

Circuit 120 regulates the output voltage  $V_{OUT}$  to a predetermined value using the feedback loop circuitry comprising resistors 150A and 150B, reference voltage source 152, and transconductance amplifier 154. The feedback loop in converter 120 operates to adjust the output current to match  $I_L$  by varying  $I_{GM}$  in response to changes in  $V_{OUT}$  in the same fashion as the feedback loop comprising resistors 71A/71B, reference 72, and transconductance amplifier 74 in the previous embodiments.

A further embodiment of a buck charge pump DC/DC converter of the present invention is illustrated in FIG. 9A. Converter 200 in FIG. 9A includes oscillator 25, current mirror transistors 75/76, two buck charge pumps coupled in parallel, and feedback loop circuitry that comprises resistors 71A and 71B, reference voltage source 72, and transconductance amplifier 74. The first buck charge pump comprises capacitors 210 and 212, and switches S21, S22, S23, S24, S25, S26, and S27. The second buck charge pump comprises capacitors 214 and 216, and switches S31, S32, S33, S34, S35, S36, and S37. Switches S21/S22/S23 are switched out of phase with switches S24/S25/S26/S27, and switches S31/S32/S33 are switched out of phase with switches S34/S35/S36/S37 by the clock signals. Switches S21/S22/S23 are switched out of phase with switches S31/S32/S33, and switches S24/S25/S26/S27 are switched out of phase with switches S34/S35/S36/S37. Each of switches S21–S27 and S31–S37 have a 50% duty cycle.

Oscillator 25 outputs digital clock signals  $V_{CLK}$  and  $V_{CLKB}$ . Clock signals  $V_{CLK}$  and  $V_{CLKB}$  may have a blanking interval. Clock signal  $V_{CLKB}$  controls the opening and closing of switches S21/S22/S23 and switches S34/S35/S36/S37. Clock signal  $V_{CLK}$  controls the opening and closing of switches S24/S25/S26/S27 and switches S31/S32/S33. Switches S21/S22/S23 and S34/S35/S36/S37 are closed when  $V_{CLK}$  is HIGH and open when  $V_{CLK}$  is LOW. Switches S24/S25/S26/S27 and S31/S32/S33 are closed when  $V_{CLKB}$  is HIGH and open when  $V_{CLKB}$  is LOW. Switches S24/S25/S26/S27 are closed during one phase of the clock signals and switches S34/S35/S36/S37 are closed during the other phase of the clock signals. Thus, the two buck charge pumps S21–S27 and S31–S37 coupled in parallel provide a constant input current  $I_{IN}$  during each phase of the clock signals as shown, for example, in FIG. 9B (except during the blanking intervals). Illustrative waveforms for clock signals  $V_{CLK}$  and  $V_{CLKB}$  in converter 200 are shown in FIG. 9B.

The input current through current mirror transistors 75 and 76 is constant and is set by output current  $I_{GM}$  of transconductance amplifier 74, as discussed above with respect to FIG. 5A. Because each charge pump S21–S27 and S31–S37 provides one half of the required load current  $I_L$ , the load current for converter 200 is defined by equation (13) during a steady state.

$V_{OUT}$  is applied across capacitors 210 and 212 when switches S21, S22, and S23 are closed. One half of  $V_{OUT}$  drops across capacitor 210 and one half of  $V_{OUT}$  drops across capacitor 212. When switches S21–S23 open and switches S24–S27 close, capacitors 210 and 212 are both



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coupled between  $V_{IN}$  and  $V_{OUT}$ . A voltage equal to  $V_{OUT}/2$  now drops across capacitors 210 and 212 relative to  $V_{OUT}$ . Therefore, the voltage across transistor 76 equals  $V_{IN} - 3V_{OUT}/2$ . Thus, the regulated value of  $V_{OUT}$  for converter 200 must be related to  $V_{IN}$  according to the following equation so that current does not flow from  $V_{OUT}$  to  $V_{IN}$ :

$$V_{OUT} \leq \frac{2V_{IN}}{3} \quad (19)$$

Persons skilled in the art further will recognize that the circuitry of the present invention may be implemented using circuit configurations other than those shown and discussed above. For example, a variable resistance may be used in place of current mirror 75/76 in the buck embodiments of FIGS. 7A and 9A. All such modifications are within the scope of the present invention, which is limited only by the claims which follow.

What is claimed is:

1. A method for regulating a voltage at an output node of a boost voltage regulator, the method comprising:
  - providing a first capacitor;
  - providing a first switch coupled between the first capacitor and the output node;
  - providing a second switch coupled to the first capacitor;
  - controlling the first and second switches to alternately charge the first capacitor from an input voltage and discharge the first capacitor to the output node;
  - monitoring the voltage at the output node to generate a control signal; and
  - controlling the current flowing through the first capacitor in response to the control signal when the first switch is closed.
2. The method of claim 1 wherein:
  - monitoring the voltage at the output node to generate the control signal comprises monitoring the voltage at the output node using a resistor divider to generate a voltage feedback signal.
3. The method of claim 2 wherein:
  - controlling the current flowing through the first capacitor in response to the control signal comprises controlling the current flowing through the first capacitor when the first switch is closed in response to the output signal of an amplifier that compares the voltage feedback signal to a reference signal.
4. The method of claim 1 further comprising:
  - controlling the current through the first capacitor in response to the control signal when the second switch is closed.
5. The method of claim 1 further comprising:
  - providing a third switch coupled to the first capacitor, wherein the third switch is closed when the first switch is closed; and
  - providing a fourth switch coupled to the first capacitor, wherein the fourth switch is closed when the second switch is closed, wherein the first switch is switched out of phase with the second switch.
6. The method of claim 1 further comprising a current mirror that conducts current from the input voltage during a blanking interval when the first and the second switches are open.
7. A method for regulating a voltage at an output node of a boost voltage regulator, the method comprising:
  - providing a first capacitor;

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- providing a first switch coupled between the first capacitor and the output node;
- providing a second switch coupled to the first capacitor;
- controlling the first and second switches to alternately charge the first capacitor from an input voltage and discharge the first capacitor to the output node;
- monitoring the voltage at the output node to generate a control signal; and
- controlling the current flowing through the first capacitor in response to the control signal when the first switch is closed, by providing a variable resistance in series between the input voltage and the first capacitor when the first switch is closed, wherein the variable resistance is responsive to the control signal.
8. The method of claim 7 wherein the variable resistance comprises a transistor.
9. A method for regulating a voltage at an output node of a boost voltage regulators the method comprising:
  - providing a first capacitor;
  - providing a first switch coupled between the first capacitor and the output node;
  - providing a second switch coupled to the first capacitor;
  - controlling the first and second switches to alternately charge the first capacitor from an input voltage and discharge the first capacitor to the output node;
  - monitoring the voltage at the output node to generate a control signal;
  - controlling the current flowing through the first capacitor in response to the control signal when the first switch is closed; and
  - controlling the current through the first capacitor in response to the control signal when the second switch is closed, by providing a variable resistance in series between the input voltage and the first capacitor when the second switch is closed.
10. A method for regulating a voltage at an output node of a boost voltage regulator, the method comprising:
  - providing a first capacitor;
  - providing a first switch coupled between the first capacitor and the output node;
  - providing a second switch coupled to the first capacitor;
  - controlling the first and second switches to alternately charge the first capacitor from an input voltage and discharge the first capacitor to the output node;
  - monitoring the voltage at the output node to generate a control signal;
  - controlling the current flowing through the first capacitor in response to the control signal when the first switch is closed,
  - by providing a current mirror, wherein current flows from the input voltage through the current mirror to the first capacitor.
11. The method of claim 10 further comprising:
  - controlling the current through the first capacitor when the second switch is closed by providing the current mirror which is responsive to the control signal.
12. A method for regulating a voltage at an output node of a boost voltage regulator, the method comprising:
  - providing a first capacitor;
  - providing a first switch coupled between the first capacitor and the output node;

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providing a second switch coupled to the first capacitor;  
controlling the first and second switches to alternately  
charge the first capacitor from an input voltage and  
discharge the first capacitor to the output node;  
monitoring the voltage at the output node to generate a  
control signal;

controlling the current flowing through the first capacitor  
in response to the control signal when the first switch  
is closed;

controlling the current through the first capacitor in  
response to the control signal when the second switch  
is closed by providing a first current mirror that con-  
ducts current when the second switch is closed; and

wherein controlling the current flowing through the first  
capacitor in response to the control signal when the first  
switch is closed comprises providing a second current  
mirror that conducts current when the first switch is  
closed.

13. The method of claim 12 wherein the current con-  
ducted by the first and second current mirrors is responsive  
to the control signal.

14. The method of claim 12 further comprising:

providing a second capacitor coupled to the second  
switch;

providing a third switch coupled between the second  
capacitor and the output node that is closed when the  
first switch is closed; and

providing a fourth switch coupled between the second  
capacitor and ground that is closed when the second  
switch is closed,

wherein the first switch is switched out of phase with  
the second switch.

15. A method for regulating a voltage at an output node of  
a buck voltage regulator, the method comprising:

providing first and second capacitors;

providing a first switch coupled to the first capacitor and  
a second switch coupled to the second capacitor;

switching the first switch to charge the first capacitor from  
an input voltage;

switching the second switch out of phase with the first  
switch to charge the second capacitor from the input  
voltage;

monitoring the voltage at the output node to generate a  
control signal; and

controlling the current flowing through the first capacitor  
in response to the control signal when the first switch  
is closed and controlling the current flowing through  
the second capacitor in response to the control signal  
when the second switch is closed.

16. The method of claim 15 wherein:

monitoring the voltage at the output node to generate a  
control signal comprises providing an amplifier that  
compares a voltage feedback signal to a reference  
signal.

17. The method of claim 15 further comprising:

providing a third and fourth switches that are each  
coupled between the first capacitor and the output node;  
and

providing a fifth switch coupled to the first capacitor.

18. A method for regulating a voltage at an output node of  
a buck voltage regulator, the method comprising:

providing first and second capacitors;

providing a first switch coupled to the first capacitor and  
a second switch coupled to the second capacitor;

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switching the first switch to charge the first capacitor from  
an input voltage;

switching the second switch out of phase with the first  
switch to charge the second capacitor from the input  
voltage;

monitoring the voltage at the output node to generate a  
control signal; and

controlling the current flowing through the first capacitor  
in response to the control signal when the first switch  
is closed and controlling the current flowing through  
the second capacitor in response to the control signal  
when the second switch is closed,  
by providing a current mirror.

19. The method of claim 18 wherein:

monitoring the voltage at the output node to generate the  
control signal comprises providing a transconductance  
amplifier that controls the current through the current  
mirror in response to a voltage feedback signal from the  
output node.

20. A method for regulating a voltage at an output node of  
a buck voltage regulator, the method comprising:

providing first and second capacitors;

providing a first switch coupled to the first capacitor and  
a second switch coupled to the second capacitor;

switching the first switch to charge the first capacitor from  
an input voltage;

switching the second switch out of phase with the first  
switch to charge the second capacitor from the input  
voltage;

monitoring the voltage at the output node to generate a  
control signal;

controlling the current flowing through the first capacitor  
in response to the control signal when the first switch  
is closed and controlling the current flowing through  
the second capacitor in response to the control signal  
when the second switch is closed;

providing third and fourth switches that are each coupled  
between the first capacitor and the output node;

providing a fifth switch coupled to the first capacitor;

providing sixth and seventh switches that are each  
coupled between the second capacitor and the output  
node; and

providing an eighth switch coupled to the second capaci-  
tor.

21. The method of claim 20 further comprising:

providing a third capacitor coupled to the fifth switch;

providing a ninth switch coupled between the third  
capacitor and the output node;

providing a tenth switch coupled between the third  
capacitor and ground; and

providing an eleventh switch coupled to the third capaci-  
tor.

22. The method of claim 21 further comprising:

providing a fourth capacitor coupled to the eighth switch;

providing a twelfth switch coupled between the fourth  
capacitor and the output node;

providing a thirteenth switch coupled between the fourth  
capacitor and ground; and

providing a fourteenth switch coupled to the fourth  
capacitor.

23. A boost voltage regulator that regulates a voltage at an  
output node, comprising:

a first capacitor;

a first switch coupled between the first capacitor and the output node;

a second switch coupled to the first capacitor, wherein current alternately flows from an input voltage to the first capacitor and from the first capacitor to the output node;

feedback loop circuitry that monitors the voltage at the output node and generates a control signal; and

a transistor that controls the current flowing through the first switch in response to the control signal when the first switch is closed.

24. The regulator of claim 23 wherein:  
the feedback loop circuitry comprises a resistor divider that generates a voltage feedback signal and an amplifier that compares the voltage feedback signal with a reference signal.

25. The regulator of claim 23 wherein:  
the transistor comprises a variable resistance in series between the input voltage and the first capacitor when the first switch is closed, wherein the variable resistance is responsive to the control signal.

26. The regulator of claim 23 wherein:  
the transistor controls the current through the second switch in response to the control signal when the second switch is closed.

27. The regulator of claim 23 further comprising:  
a third switch coupled to the first capacitor, wherein the third switch is closed when the first switch is closed; and  
a fourth switch coupled to the first capacitor, wherein the fourth switch is closed when the second switch is closed, wherein the first switch is switched out of phase with the second switch.

28. The regulator of claim 23 wherein:  
the transistor is part of a current mirror that controls the current through the first switch in response to the control signal when the first switch is closed.

29. The regulator of claim 28 wherein the current mirror controls the current through the second switch when it is closed.

30. A boost voltage regulator that regulates a voltage at an output node, comprising:  
a first capacitor;  
a first switch coupled between the first capacitor and the output node;  
a second switch coupled to the first capacitor, wherein current alternately flows from an input voltage to the first capacitor and from the first capacitor to the output node;  
feedback loop circuitry that monitors the voltage at the output node and generates a control signal; and  
a transistor that controls the current flowing through the first switch in response to the control signal when the first switch is closed, wherein the transistor controls the current through the second switch in response to the control signal when the second switch is closed, wherein the transistor comprises a variable resistance coupled in series between the input voltage and the first capacitor when the second switch is closed, and wherein the variable resistance is responsive to the control signal.

31. A boost voltage regulator that regulates a voltage at an output node, comprising:

a first capacitor;  
a first switch coupled between the first capacitor and the output node;  
a second switch coupled to the first capacitor, wherein current alternately flows from an input voltage to the first capacitor and from the first capacitor to the output node;  
feedback loop circuitry that monitors the voltage at the output node and generates a control signal;  
a transistor that controls the current flowing through the first switch in response to the control signal when the first switch is closed, wherein the transistor is part of a first current mirror that controls the current through the first switch in response to the control signal when the first switch is closed; and the regulator further comprises:  
a second current mirror that controls the current through the second switch in response to the control signal when the second switch is closed.

32. The regulator of claim 31 wherein the current conducted by the first and second current mirrors is responsive to the control signal.

33. The regulator of claim 32 further comprising:  
a second capacitor coupled to the second switch;  
a third switch coupled between the second capacitor and the output node that is closed when the first switch is closed; and  
a fourth switch coupled between the second capacitor and ground that is closed when the second switch is closed, wherein the first switch is switched out of phase with the second switch.

34. The regulator of claim 23 further comprising a current mirror that conducts current in response to the control signal from the input voltage during a blanking interval when the first and the second switches are open.

35. The regulator of claim 23 wherein duty cycle of the first and second switches is proportional to the input-to-output voltage conversion ratio.

36. A buck voltage regulator that regulates a voltage at an output node, comprising:  
first and second capacitors;  
a first switch coupled to the first capacitor;  
a second switch coupled to the second capacitor that is switched out of phase with the first switch, wherein current alternately flows from an input voltage to the first capacitor and from the input voltage to the second capacitor;  
feedback loop circuitry that monitors the voltage at the output node to generate a control signal; and  
a transistor that controls the current through the first switch when it is closed and the current through the second switch when it is closed in response to the control signal.

37. The regulator of claim 36 wherein:  
the transistor is part of a current mirror coupled between the input voltage and the first and second switches.

38. The regulator of claim 36 wherein the feedback loop circuitry comprises:  
an amplifier that compares a voltage feedback signal from the output node to a reference signal.

39. The regulator of claim 38 wherein the feedback loop circuitry further comprises:  
a resistor divider coupled to the output node and the amplifier, the resistor divider generating the voltage feedback signal.

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40. The regulator of claim 36 further comprising:  
 a third and fourth switches that are each coupled between the first capacitor and the output node; and  
 a fifth switch coupled to the first capacitor.
41. The regulator of claim 40 further comprising:  
 a sixth and seventh switches that are each coupled between the second capacitor and the output node; and  
 an eighth switch coupled to the second capacitor.
42. A buck voltage regulator that regulates a voltage at an output node, comprising:  
 first and second capacitors;  
 a first switch coupled to the first capacitor;  
 a second switch coupled to the second capacitor that is switched out of phase with the first switch, wherein current alternately flows from an input voltage to the first capacitor and from the input voltage to the second capacitor;  
 feedback loop circuitry that monitors the voltage at the output node to generate a control signal;  
 a transistor that controls the current through the first switch when it is closed and the current through the second switch when it is closed in response to the control signal,  
 wherein the transistor comprises a variable resistance.
43. A buck voltage regulator that regulates a voltage at an output node, comprising:  
 first and second capacitors;  
 a first switch coupled to the first capacitor;  
 a second switch coupled to the second capacitor that is switched out of phase with the first switch, wherein

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- current alternately flows from an input voltage to the first capacitor and from the input voltage to the second capacitor;  
 feedback loop circuitry that monitors the voltage at the output node to generate a control signal;  
 a transistor that controls the current through the first switch when it is closed and the current through the second switch when it is closed in response to the control signal;  
 third and fourth switches that are each coupled between the first capacitor and the output node;  
 a fifth switch coupled to the first capacitor;  
 sixth and seventh switches that are each coupled between the second capacitor and the output node;  
 an eighth switch coupled to the second capacitor; and  
 a third capacitor coupled to the fifth switch;  
 a ninth switch coupled between the third capacitor and the output node;  
 a tenth switch coupled between the third capacitor and ground; and  
 an eleventh switch coupled to the third capacitor.
44. The regulator of claim 43 further comprising:  
 a fourth capacitor coupled to the eighth switch;  
 a twelfth switch coupled between the fourth capacitor and the output node;  
 a thirteenth switch coupled between the fourth capacitor and ground; and  
 a fourteenth switch coupled to the fourth capacitor.

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UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,411,531 B1  
DATED : June 25, 2002  
INVENTOR(S) : Nork et al.

Page 1 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,

Item [56], OTHER PUBLICATIONS, change "4-26-4-37" to -- 4-26 - 4-37 --.

Column 2,

Line 24, change "SA" to -- 5A --.

Line 29, change "C/DC" to -- DC/DC --.

Column 3,

Line 9, change "converter is" to -- converter 20 is --.

Line 61, change "Oscillator outputs" to -- Oscillator 25 outputs --.

Column 4,

Lines 45-50, delete "The current through a capacitor is determined by the following standard equation:

$$I = C \frac{dV}{dt}."$$

Line 56, change "(dV<sub>tx</sub>)" to -- (dV<sub>tx</sub>) --.

Line 58, change "(dV<sub>ty</sub>)" to -- (dV<sub>ty</sub>) --.

Line 63, change  $"dV_{tx} = dV_{ty} = \frac{I_{R38}}{C_8} t_x = \frac{I_{R38}}{C_8} t_y"$   
to  $--dV_{tx} = dV_{ty} = \frac{I_{R38}}{C_8} t_x = \frac{I_{R38}}{C_8} t_y--$ .

Line 66, change "t<sub>x</sub>" to --t<sub>x</sub>--.

Column 5,

Line 1, change "t<sub>y</sub>" to --t<sub>y</sub>--.

Line 4, change "t<sub>x</sub>=t<sub>y</sub>" to --t<sub>x</sub>=t<sub>y</sub>--.

Line 7, change "t<sub>x</sub> and t<sub>y</sub>" to --t<sub>x</sub> and t<sub>y</sub>--.

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Page 2 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,

Line 53, change "n-channel" to -- N-channel --.

Line 54, change "p-channel" to -- P-channel --.

Column 8,

Line 63, change "<" to -- ≤ --.

Line 64, change " $(dV_{tx})$ " to --  $(dV_{tx})$  --.

Line 66, change " $(dV_{ty})$ " to --  $(dV_{ty})$  --.

Column 9,

Line 2, change " $dV_{tx} = dV_{tx} = \frac{N \cdot I_{GM}}{C_8} t_x = \frac{N \cdot I_{GM}}{C_8} t_x$ "  
to --  $dV_{tx} = dV_{tx} = \frac{N \cdot I_{GM}}{C_8} t_x = \frac{N \cdot I_{GM}}{C_8} t_x$  --.

Line 6, change " $(t_x)$ " to --  $(t_x)$  --.

Line 8, change " $(t_y)$ " to --  $(t_y)$  --.

Line 10, change " $t_x = t_y$ " to --  $t_x = t_y$  --.

Line 11, change " $t_x$  and  $t_y$ " to --  $t_x$  and  $t_y$  --.

Line 56, change "IN" to --  $I_{IN}$  --.

Line 67, change "p-channel" to -- P-channel --.

Column 10,

Line 1, change "p-channel" to -- P-channel --.

Line 11, change "p-channel" to -- P-channel --.

Line 33, change "p-channel" to -- P-channel --.

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Page 3 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,

Line 16, change " $\leq$ " to --  $\leq$  --.

Column 13,

Line 19, change " $\leq$ " to --  $\leq$  --.

Column 14,

Line 55, change " $I_{IN} = I_{GM} + I_{M28} = I_{GM} (1+N)$ " to --

$$I_{IN} = I_{GM} + I_{M128} = I_{GM} (1 + N) \text{ --.}$$

Column 15,

Line 19, change " $(dV_{tA})$ " to --  $(dV_{t_A})$  --.

Line 21, change " $(dV_{tB})$ " to --  $(dV_{t_B})$  --.

Line 32, change " $T_A$  and  $T_B$ " to --  $t_A$  and  $t_B$  --.

Line 35, change " $T_B = 2T_A$ " to --  $t_B = 2t_A$  --.

Line 50, change " $\leq$ " to --  $\leq$  --.

Column 16

Line 19, change "pervious" to -- previous --.

Signed and Sealed this

Twenty-fifth Day of February, 2003



JAMES E. ROGAN  
*Director of the United States Patent and Trademark Office*



US006518829B2

(12) **United States Patent**  
**Butler**

(10) Patent No.: **US 6,518,829 B2**  
(45) Date of Patent: **Feb. 11, 2003**

(54) **DRIVER TIMING AND CIRCUIT  
TECHNIQUE FOR A LOW NOISE CHARGE  
PUMP CIRCUIT**

(75) Inventor: **Douglas Blaine Butler**, Colorado  
Springs, CO (US)

(73) Assignees: **United Memories, Inc.**, Colorado  
Springs, CO (US); **Sony Corporation**,  
Tokyo (JP)

(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 56 days.

(21) Appl. No.: **09/730,207**

(22) Filed: **Dec. 4, 2000**

(65) **Prior Publication Data**

US 2002/0067201 A1 Jun. 6, 2002

(51) Int. Cl.<sup>7</sup> ..... **G05F 1/10**

(52) U.S. Cl. .... **327/536; 363/60**

(58) Field of Search ..... **327/536; 307/110;**  
**363/59, 60**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,703,511 A \* 12/1997 Okamoto ..... 327/536  
5,801,578 A \* 9/1998 Bereza ..... 327/536

6,008,690 A \* 12/1999 Takeshima et al. .... 327/536  
6,018,264 A \* 1/2000 Jin ..... 327/536  
6,097,161 A \* 8/2000 Takano et al. .... 327/536  
6,107,862 A \* 8/2000 Mukainakano et al. .... 327/536  
6,147,519 A \* 11/2000 Krynski ..... 327/536  
6,198,340 B1 \* 3/2001 Ting et al. .... 327/536

\* cited by examiner

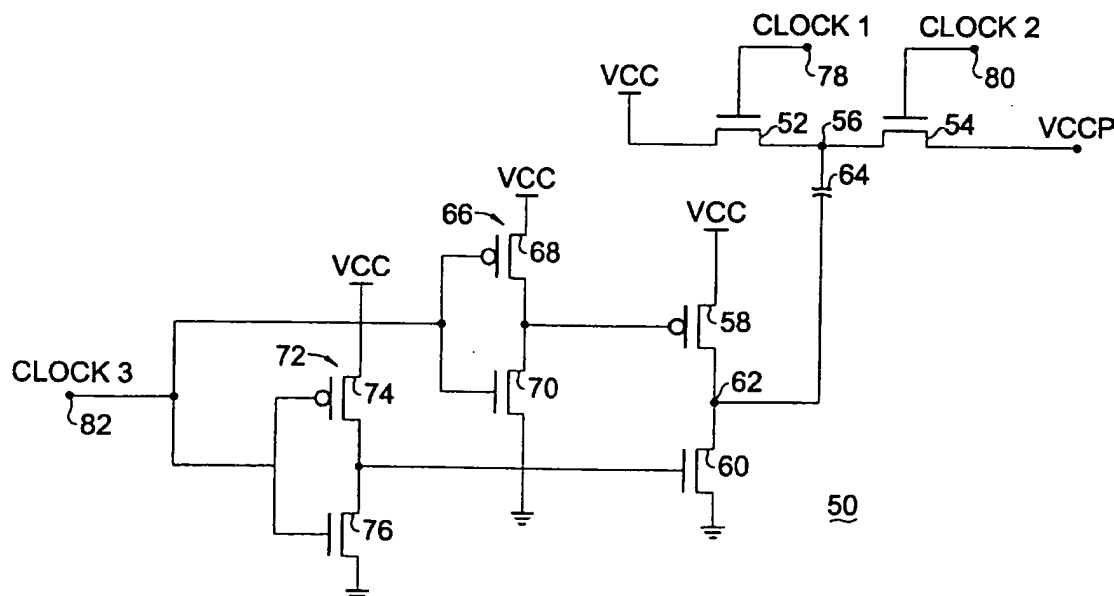
*Primary Examiner*—Kenneth B. Wells

(74) *Attorney, Agent, or Firm*—William J. Kubida; Peter J.  
Meza; Hogan & Hartson LLP

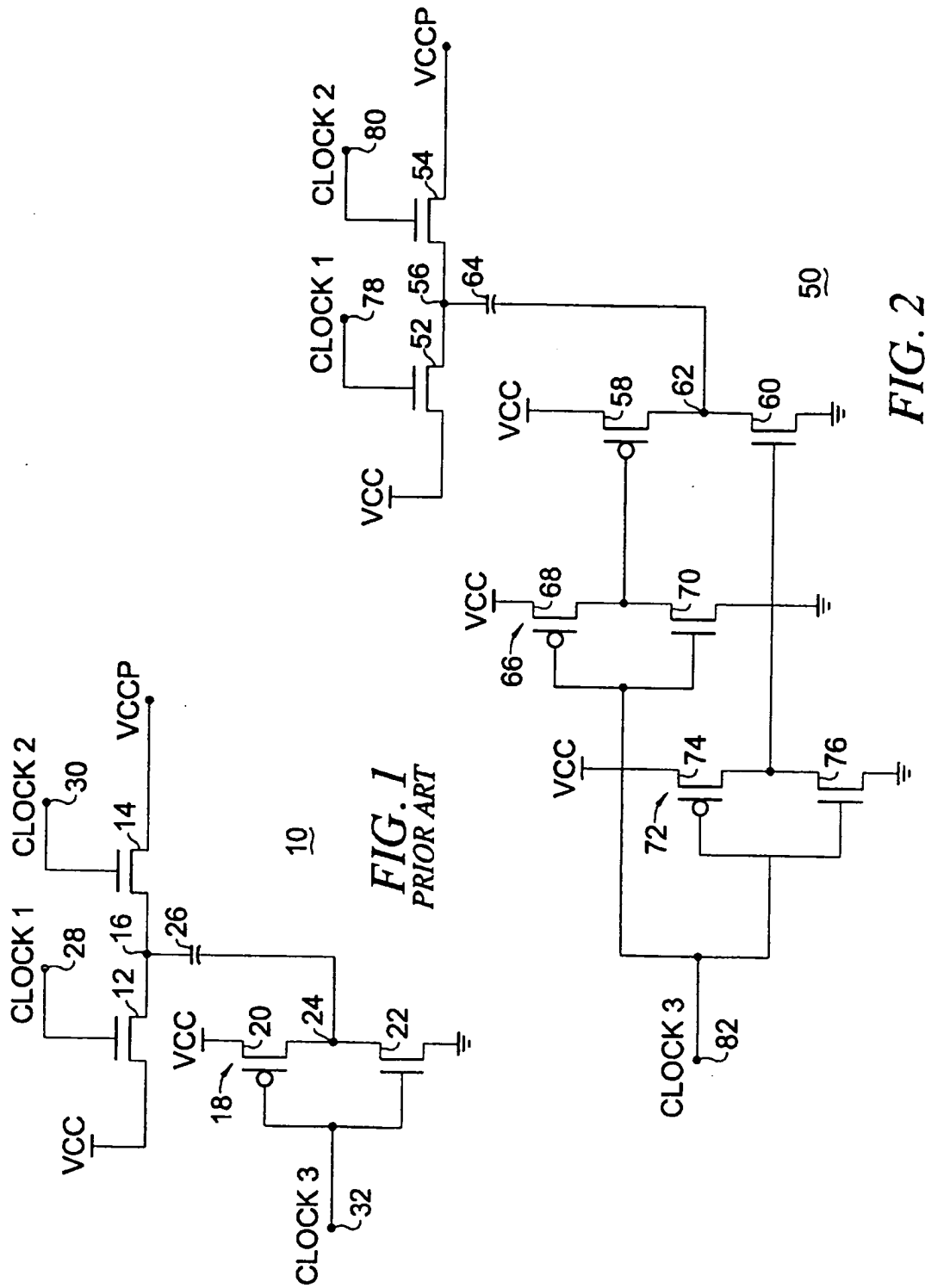
(57) **ABSTRACT**

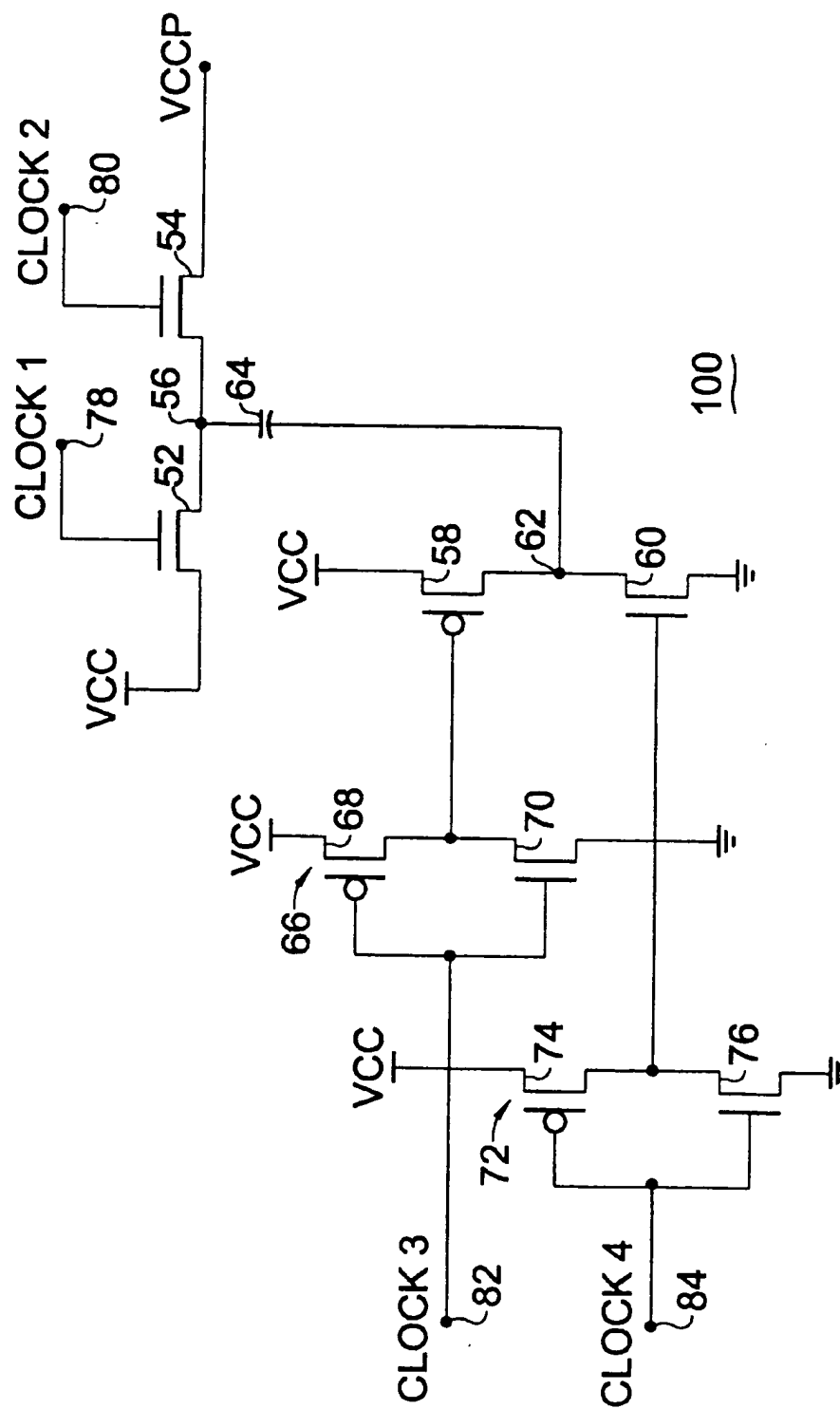
A driver timing and circuit technique for a low noise charge pump circuit of particular applicability with respect to integrated circuit devices requiring voltage levels either more positive than or more negative than, externally supplied voltages. In accordance with the technique of the present invention, the pump capacitor is driven "high" by one transistor and "low" by another. By correctly sizing the devices driving them, each transistor can be turned "off" quickly and "on" slowly and, in an alternative embodiment, both transistors may be "off" at the same time resulting in "tri-state" operation. Timing is set such that both transistors are "off" when a third transistor connecting the intermediate node to the power supply is turned "on" and when a fourth transistor connecting the intermediate node to the pumped supply is turned "on" thereby preventing large  $dI/dt$  and resultant noise on the power supply sources.

**24 Claims, 8 Drawing Sheets**









**FIG. 3**

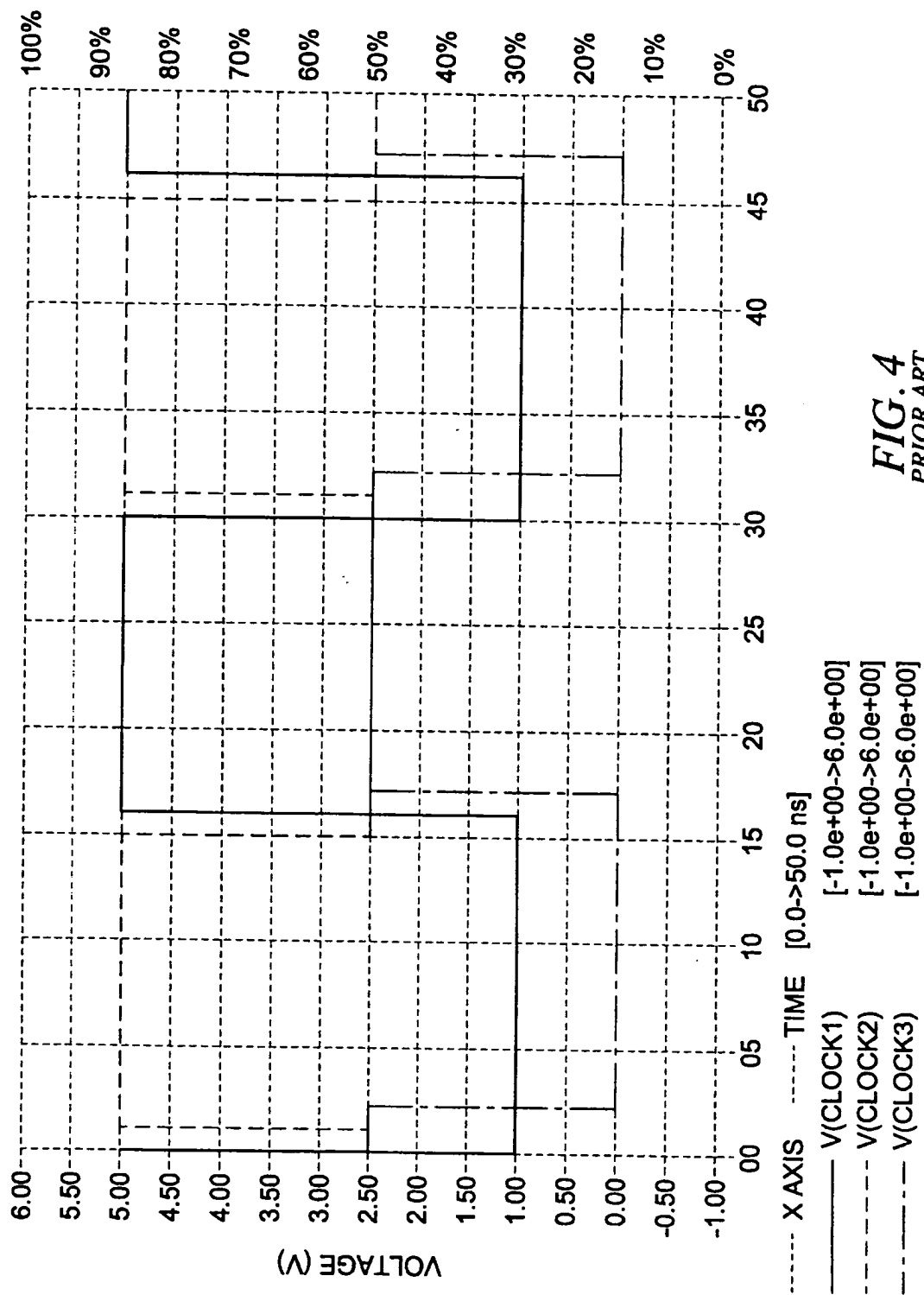


FIG. 4  
PRIOR ART

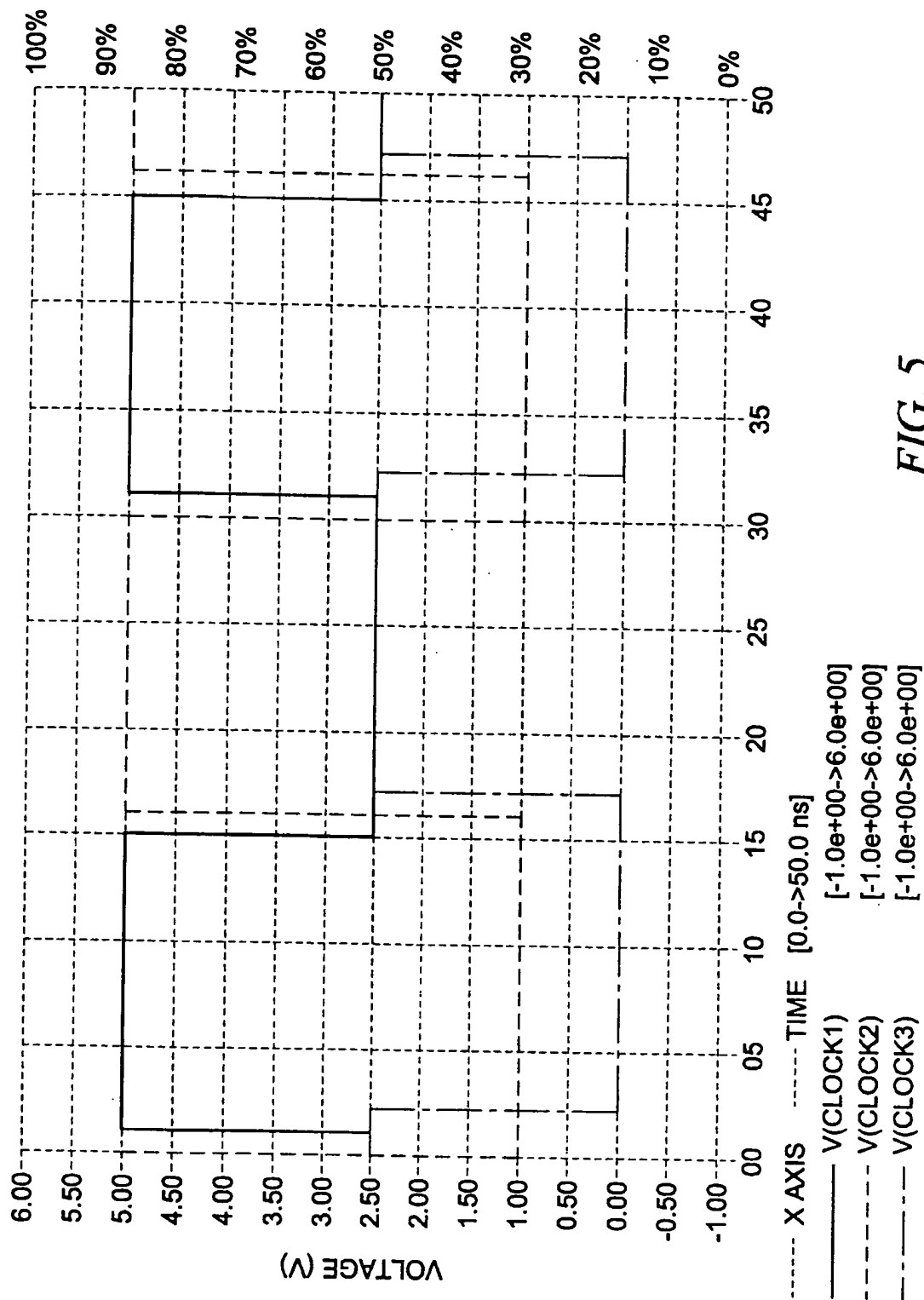


FIG. 5

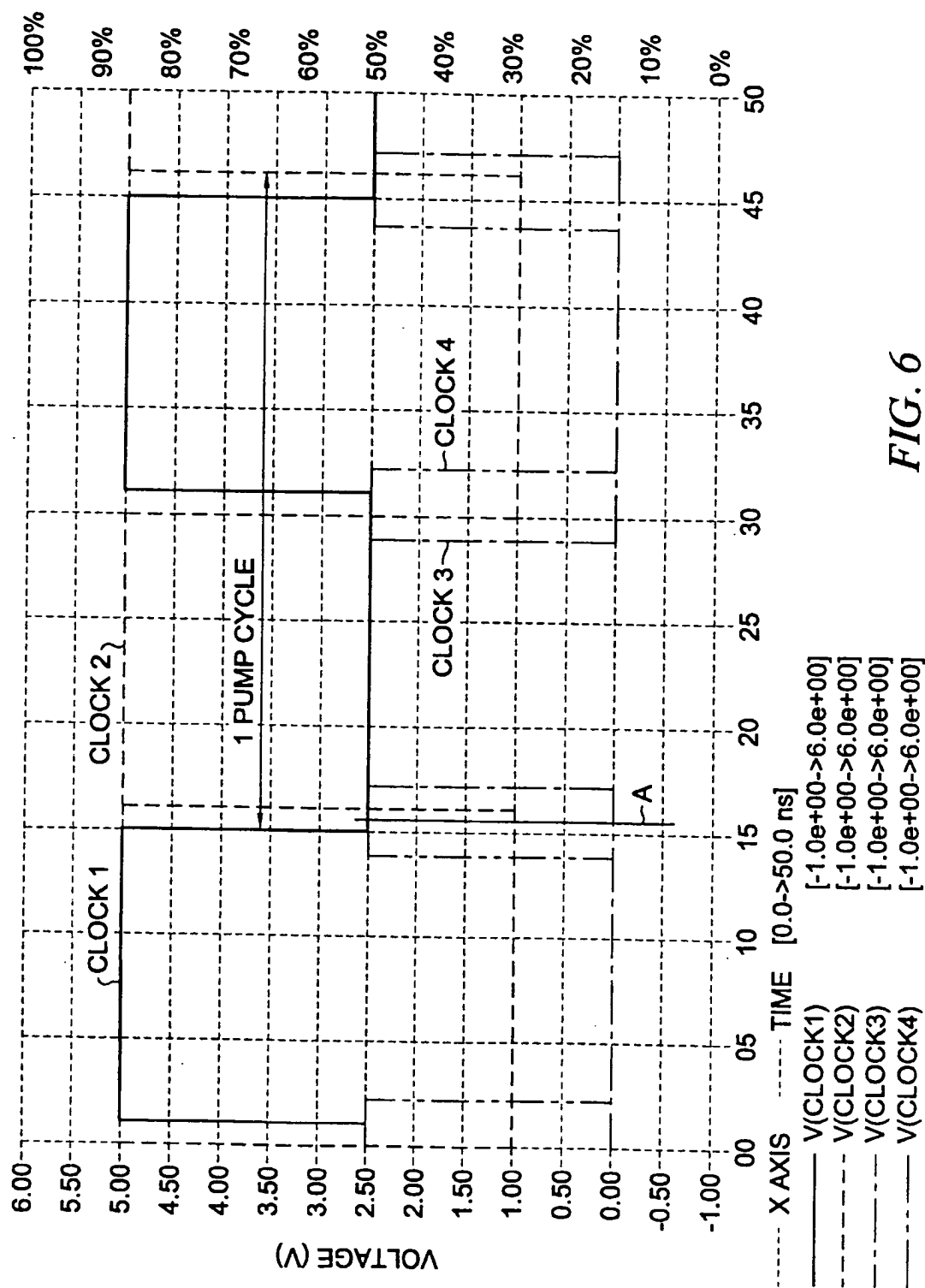
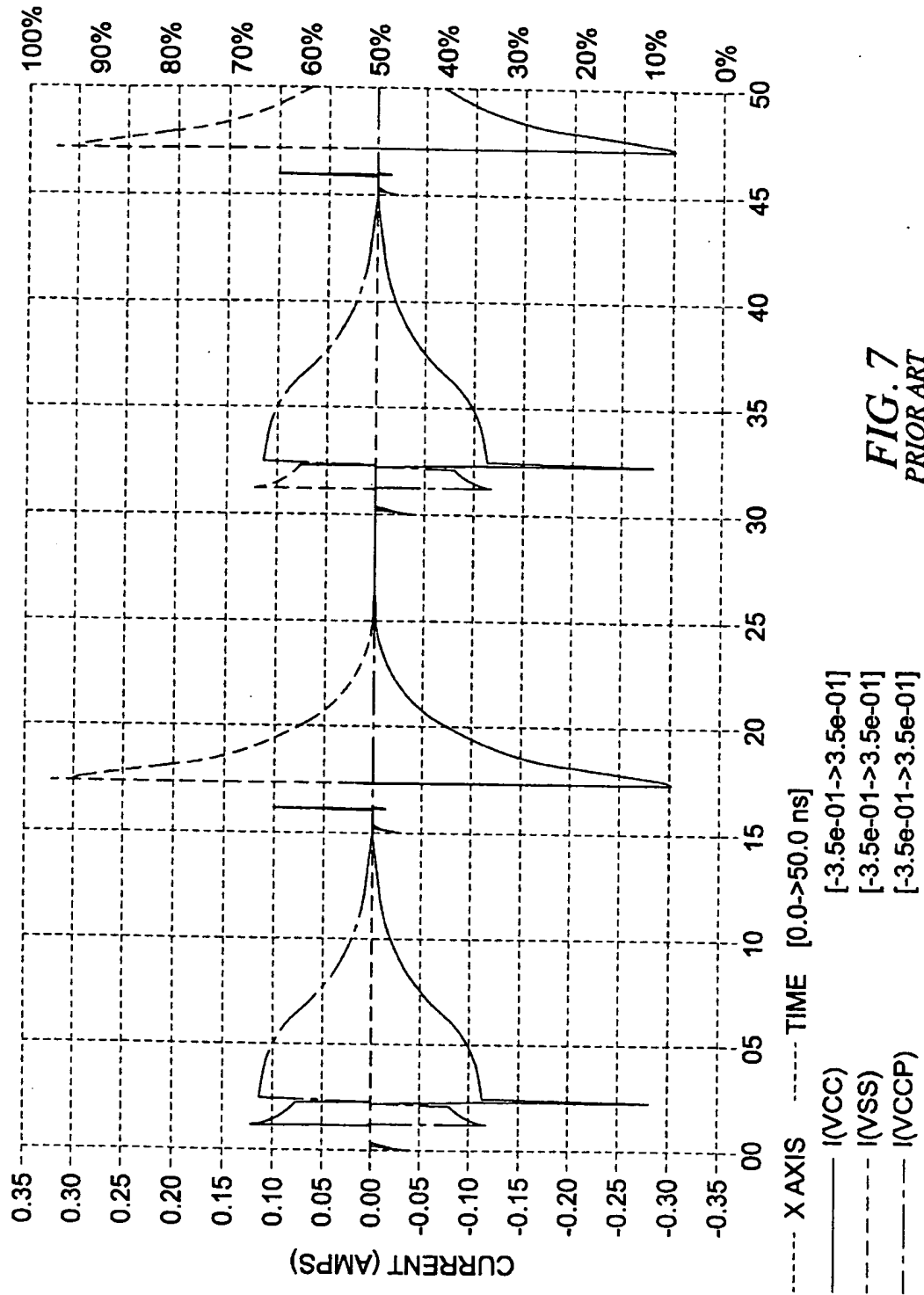
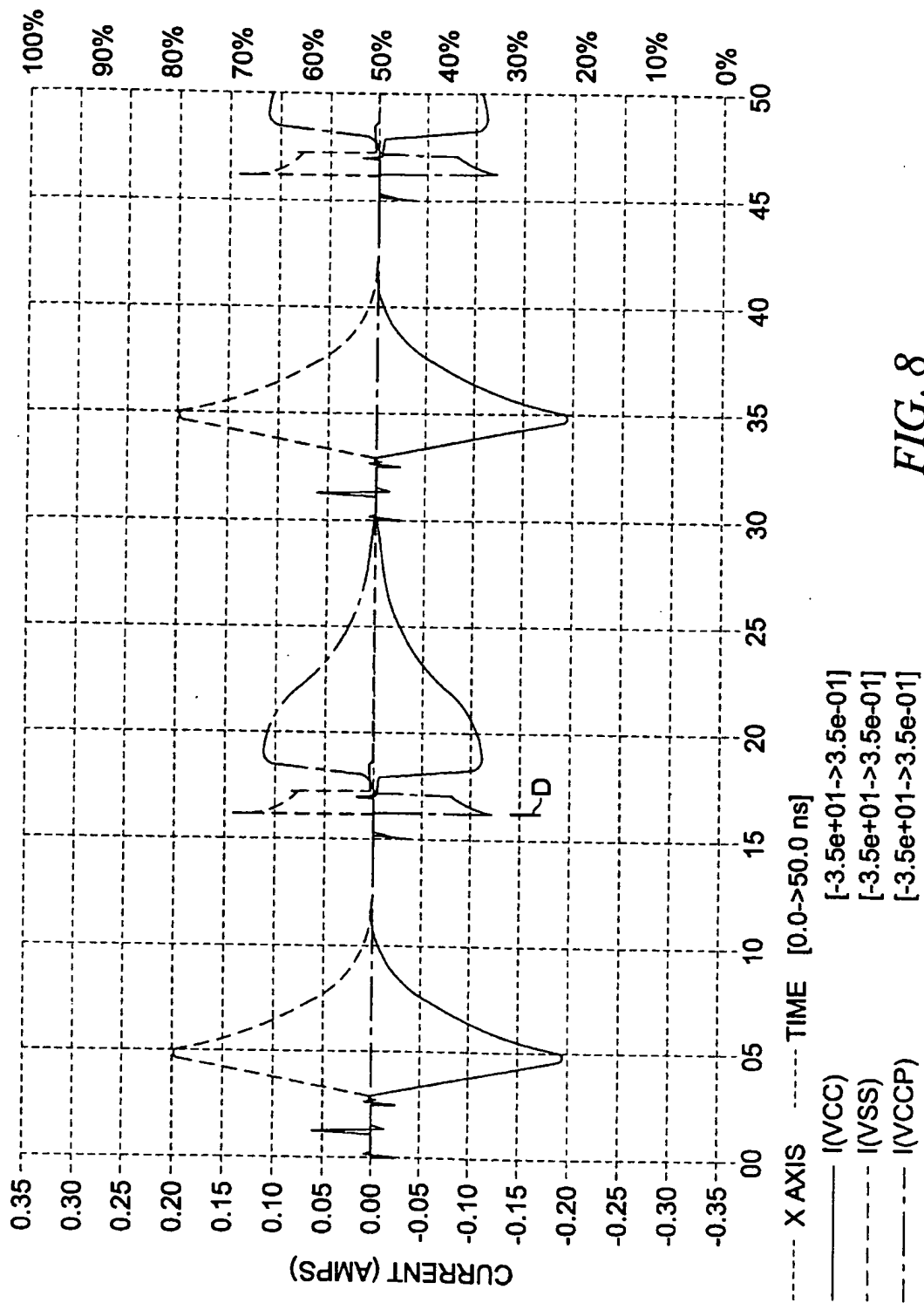


FIG. 6





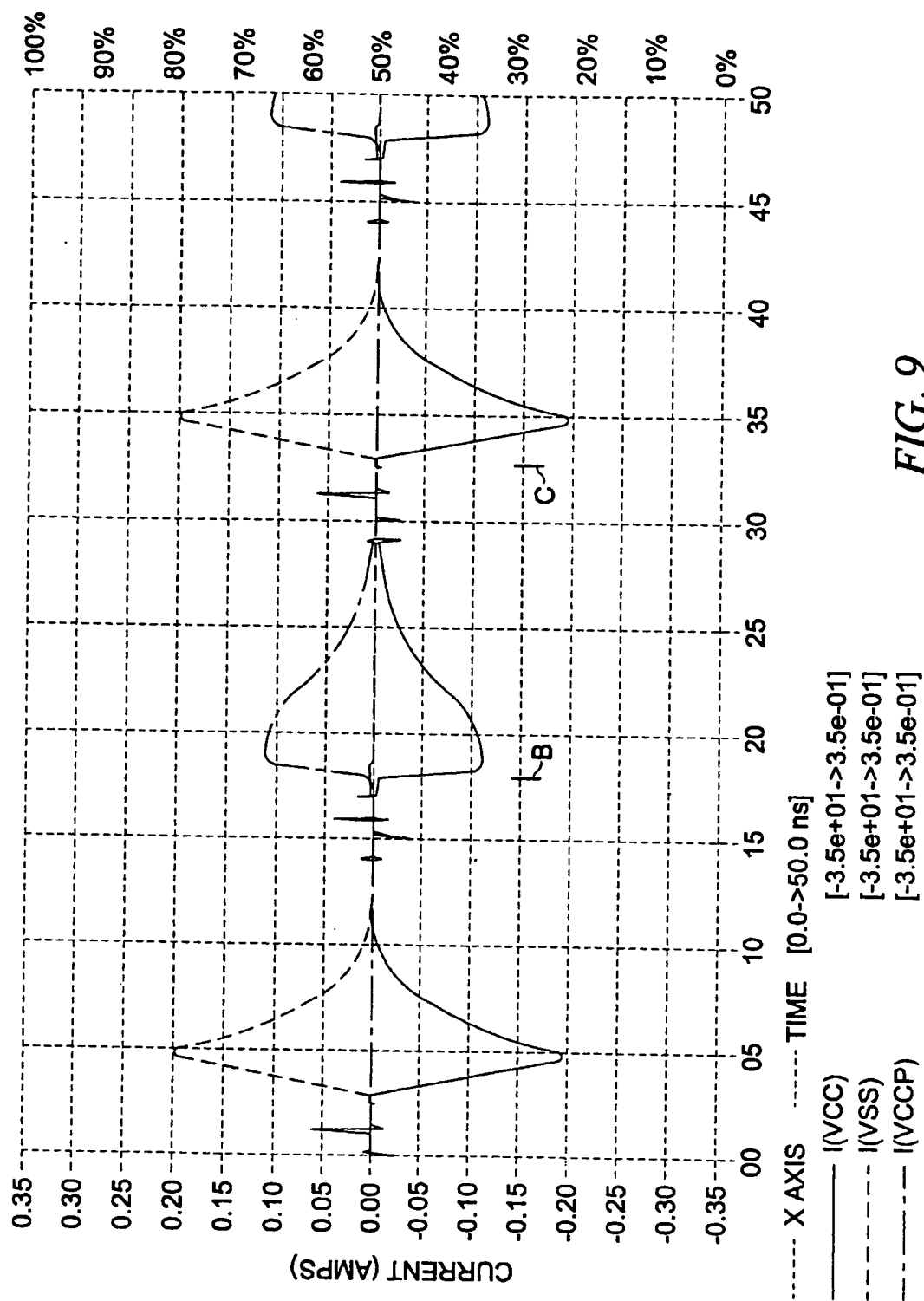


FIG. 9



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# DRIVER TIMING AND CIRCUIT TECHNIQUE FOR A LOW NOISE CHARGE PUMP CIRCUIT

## BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of integrated circuit ("IC") devices. More particularly, the present invention relates to a driver timing and circuit technique for a low noise charge pump circuit of particular applicability with respect to IC devices requiring voltage levels either in excess of, or lower than, externally supplied voltages.

IC devices are typically designed to require only a power ("VCC") and a relative circuit ground ("VSS") voltage supplies. This increases the ease of use of the IC device in a system. Nevertheless, in some cases subcircuits of these devices require voltage supply levels above or below these levels for proper operation.

Current dynamic random access memory ("DRAM") devices frequently require a voltage supply level above VCC to drive the memory access transistor gate or row decoder logic to sufficiently high levels such that a full VCC level can be written into the memory cell. DRAMs also frequently require a voltage level below VSS which is used to bias the substrate to prevent minority carrier injection from peripheral circuits. In addition, electrically erasable programmable read-only memory devices ("EEPROMs") frequently require a voltage supply level higher than VCC in order to program or erase memory cells.

In this regard, voltage levels higher than VCC are often generated on the IC device itself (i.e. "on-chip") by means of charge pump circuits. A charge pump circuit utilized to derive a voltage above the level of VCC generally operates by connecting a first node of a capacitor to VCC while the second node is connected to VSS; disconnecting the first node of the capacitor from VCC and connecting it to a pumped node ("VCCP"); disconnecting the second node of the capacitor from VSS and driving it to VCC thereby driving the first node above VCC and coupling the first node of the capacitor to the pumped node transferring charge to it; disconnecting the first node of the capacitor from the pumped node and reconnecting it to VCC; disconnecting the second node from VCC and connecting again to VSS thereby restoring the initial state of the capacitor and repeating the steps resulting in charge being "pumped" from VCC to VCCP.

In those applications wherein VCCP is required to provide relatively large amounts of current, the capacitor and transistors in the charge pump must also be large in size. When the transistors switch "on" and "off" to drive the capacitor nodes "high" or "low", large amounts of current flow and the rate of change of the current ("di/dt") flow is also large. Because the voltage supplies VCC and VSS are sourcing and sinking this current, the VCC and VSS voltage levels vary as a result of the charge pump operation. This voltage variation constitutes undesired "noise" and this noise on the VSS and VCC supplies can cause an IC device to fail to function properly in a system. The amount of noise is determined by the resistance and inductance of the VCC and VSS supplies, and for IC devices, the most difficult source of noise to control is that due to the di/dt factor because the die bond wires present significant levels of inductance.

In conventional charge pump circuits, the pump capacitor is driven by an inverter causing a relatively large change in current over time ("di/dt") to occur when the capacitor node

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is driven and when the transistor connecting the intermediate node to the power supply is turned "on". A similar di/dt also occurs when the transistor connecting the intermediate node to the pumped node is turned "on". These di/dt changes at the capacitor and intermediate nodes result in undesired and sometimes unacceptable noise in the circuit.

## SUMMARY OF THE INVENTION

In accordance with the technique of the present invention, the pump capacitor of a driver circuit for an integrated circuit device is driven "high" by one transistor and "low" by another. By correctly sizing the devices driving them, each transistor can be turned "off" quickly and "on" slowly and, in an alternative embodiment, both transistors may be "off" at the same time resulting in "tri-state" operation. Timing may be set such that both transistors are "off" when the transistor connecting the intermediate node to the power supply is turned "on" thereby preventing a large di/dt and resultant noise on the power supply sources.

Particularly disclosed herein is an integrated circuit device including a charge pump circuit which comprises a capacitive element having first and second terminals coupled to an intermediate and capacitor 62 nodes respectively. A first switching device is 52 provided for selectively coupling the intermediate node to a supply voltage line in response to a first clocking signal together with a second switching 54 device for selectively coupling the intermediate node to a pumped voltage line in response to a second clocking signal. A first inverter 66 has an input coupled to receive a third clocking signal and an output coupled to a third switching device 58 for selectively coupling the capacitor node to the supply voltage line in response to the third clocking signal; and a second inverter 72 has an input coupled to also receive the third clocking signal and an output coupled to a fourth switching device 60 for selectively coupling the capacitor node to a ground voltage line in response to the same third clocking signal. In an alternative "tri-state" embodiment, the second inverter has its input coupled to receive a separate fourth clocking signal and is operative to cause the fourth switching device to couple the capacitor node to the ground voltage line in response thereto independently of the third clocking signal.

Also particularly disclosed herein is a method for operating a charge pump in an integrated circuit device which comprises the steps of coupling a first terminal of a capacitive element to a supply voltage line while a second terminal of the capacitive element is coupled to a ground voltage line. The first terminal is firstly decoupled from the supply voltage line while substantially concurrently coupling the first terminal to a pumped voltage line. The second terminal is secondly decoupled from the ground voltage line while substantially concurrently coupling the second terminal to the supply voltage line. The first terminal is thirdly decoupled from the pumped voltage line while substantially concurrently coupling the first terminal to the supply voltage line. The second terminal is then fourthly decoupled from the supply voltage line while substantially concurrently coupling the second terminal to the ground voltage line. In operation, the step of secondly decoupling the second terminal from the ground voltage line occurs relatively more quickly than the corresponding step of substantially concurrently coupling the second terminal to the supply voltage line. Also, the step of fourthly decoupling the second terminal from the supply voltage line may also occur relatively more quickly than the corresponding step of substantially concurrently coupling the second terminal to the ground voltage line.

## BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic diagram of a conventional charge pump circuit utilizing a CMOS inverter activated by a clock signal ("CLOCK3") to drive a first capacitor terminal and having an opposite second terminal coupled to a node intermediate a series string of transistors for selectively coupling the intermediate node to either VCC or VCCP depending on the clock signals ("CLOCK1" and "CLOCK2") applied to their respective gates;

FIG. 2 is a schematic diagram of an embodiment of a "fast-off/slow-on" charge pump circuit in accordance with the present invention wherein the capacitor may be driven "high" by one transistor and "low" by another transistor as controlled by a corresponding pair of CMOS inverters having their inputs common coupled to the receive the CLOCK3 signal;

FIG. 3 is a schematic diagram of an alternative "tri-state" embodiment of a charge pump circuit in accordance with the present invention wherein each of the CMOS inverters illustrated in the preceding figure in this instance respectively receive a separate CLOCK3 and CLOCK4 input signal;

FIG. 4 is a timing diagram of the CLOCK1, CLOCK2 and CLOCK3 signal inputs to the conventional charge pump circuit of FIG. 1;

FIG. 5 is a corresponding timing diagram of the CLOCK1, CLOCK2 and CLOCK3 signal inputs to the "fast-off/slow-on" charge pump circuit of FIG. 2 in accordance with that particular embodiment of the present invention;

FIG. 6 is a similar corresponding timing diagram of the CLOCK1, CLOCK2, CLOCK3 and CLOCK4 signal inputs to the "tri-state" charge pump circuit of FIG. 3 in accordance with that alternative embodiment of the present invention;

FIG. 7 is a timing diagram illustrative of the current flow on the VCC, VSS and VCCP sources for the conventional charge pump circuit shown in FIG. 1 and particularly pointing out the resultant current spikes generated by its operation as depicted in FIG. 4;

FIG. 8 is a timing diagram illustrative of the current flow on the VCC, VSS and VCCP sources for the "fast-off/slow-on" embodiment of the charge pump circuit shown in FIG. 2 and particularly pointing out the relative decrease in the slope ( $di/dt$ ) of the current spikes generated by its operation as depicted in FIG. 5; and

FIG. 9 is a similar timing diagram illustrative of the current flow on the VCC, VSS and VCCP sources for the alternative "tri-state" embodiment of the charge pump circuit shown in FIG. 3 and also particularly pointing out the relative decrease in the slope ( $di/dt$ ) of the current spikes generated by its operation as depicted in FIG. 6 when compared to the conventional charge pump circuit of FIG. 1.

## DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

With reference now to FIG. 1, a conventional charge pump circuit 10 is shown. The conventional charge pump circuit 10 comprises a first N-channel transistor 12 for coupling an intermediate node 16 to a supply voltage source

("VCC") and a second N-channel transistor 14 for coupling the intermediate node 16 to a pumped supply voltage source ("VCCP").

A CMOS inverter 18 comprising series connected P-channel transistor 20 and N-channel transistor 22 is coupled between VCC and circuit ground ("VSS"). The output of the inverter 18 defines a capacitor node 24 which is coupled to a first terminal (or node) of a capacitor 26 which has its second terminal coupled to the intermediate node 16. A clock signal ("CLOCK1") on line 28 is furnished to the gate of transistor 12 while another clock signal ("CLOCK2") on line 30 is furnished to the gate of transistor 14. Another clock signal ("CLOCK3") on line 32 is furnished to the input of the inverter 18.

In the embodiment of the charge pump circuit 10 illustrated, transistors 12, 14 and 22 may have a channel width of  $1000\mu$  and a length of  $0.34\mu$ , with transistor 20 having a width of  $2000\mu$  and a corresponding length of  $0.34\mu$  as well. The capacitor 26 may have a typical value of substantially 300 pf.

With reference additionally now to FIG. 2, a charge pump circuit 50 in accordance with one embodiment of the present invention is shown. The charge pump circuit 50 comprises a first N-channel transistor 52 for coupling an intermediate node 56 to VCC and a second N-channel transistor 54 for coupling the intermediate node 16 to the pumped supply voltage source VCCP.

Series connected P-channel transistor 58 and N-channel transistor 60 are coupled between VCC and VSS. A capacitor node 62 is defined between transistors 58 and 60 and is coupled to a first terminal (or node) of a capacitor 64 which has its second terminal coupled to the intermediate node 56.

A first CMOS inverter 66 comprising series connected P-channel transistor 68 and N-channel transistor 70 is coupled between VCC and VSS and has its output coupled to the gate terminal of transistor 58. Similarly, a second CMOS inverter 72 comprising series connected P-channel transistor 74 and N-channel transistor 76 is also coupled between VCC and VSS and has its output coupled to the gate terminal of transistor 60. The inputs of the first and second inverters 66, 72 are coupled to a common input line 82 which receives a CLOCK3 input signal. The CLOCK1 signal on line 78 is furnished to the gate of transistor 52 while the CLOCK2 signal on line 80 is furnished to the gate of transistor 54.

With reference additionally now to FIG. 3, an alternative embodiment of a charge pump circuit 100 in accordance with the present invention is shown. As previously disclosed with respect to the charge pump circuit 50 of FIG. 2, the charge pump circuit 100 comprises a first N-channel transistor 52 for coupling an intermediate node 56 to VCC and a second N-channel transistor 54 for coupling the intermediate node 16 to the pumped supply voltage source VCCP.

As before, series connected P-channel transistor 58 and N-channel transistor 60 are coupled between VCC and VSS. A capacitor node 62 is defined between transistors 58 and 60 and is coupled to a first terminal (or node) of a capacitor 64 which has its second terminal coupled to the intermediate node 56.

A first CMOS inverter 66 comprising series connected P-channel transistor 68 and N-channel transistor 70 is coupled between VCC and VSS and has its output coupled to the gate terminal of transistor 58. Similarly, a second CMOS inverter 72 comprising series connected P-channel transistor 74 and N-channel transistor 76 is also coupled between VCC and VSS and has its output coupled to the gate terminal of transistor 60.

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With respect to the embodiment of the charge pump circuit 100, the inputs of the first and second inverters 66, 72 are herein not coupled to a common input line for receiving the CLOCK3 input signal. Rather, the input of the inverter 66 is coupled to an input line 82 for receiving the CLOCK3 signals while the input of the inverter 72 is separately coupled to another input line 84 for receiving a CLOCK4 signal. As before, however, the CLOCK1 signal on line 78 is furnished to the gate of transistor 52 while the CLOCK2 signal on line 80 is furnished to the gate of transistor 54.

With respect to the embodiments of the charge pump circuit 50 (FIG. 2) and the charge pump circuit 100 (FIG. 3), transistors 52, 54 and 60 may also have a channel width of  $1000\mu$  and a length of  $0.34\mu$ , with transistor 58 having a width of  $2000\mu$  and a corresponding length of  $0.34\mu$  as well. The capacitor 64 may have a typical value of substantially 300 pf. Transistors 70, 74 may have a channel width of  $10\mu$  and a length of  $0.34\mu$  while transistor 68 has a width of  $400\mu$  and transistor 76 has a width of  $100\mu$ , both having a channel length of  $0.34\mu$ . As can be seen, transistor 68 is larger than transistor 74 while transistor 76 is larger than transistor 70. This relative device sizing facilitates the "fast-off/slow-on" operation of the charge pump circuits 50 (FIG. 2) and 100 (FIG. 3) which will be described in more detail hereinafter.

With reference additionally now to FIG. 4, a timing diagram of the CLOCK1, CLOCK2 and CLOCK3 signal inputs to the conventional charge pump circuit 10 of FIG. 1 is shown. In operation, the various clock signals function to couple the capacitor node 24 to VSS through the operation of transistor 22 in response to the CLOCK3 signal while transistor 12 couples the intermediate node 16 to VCC in response to the CLOCK1 signal. Transistor 12 is then turned "off" in response to CLOCK1. At this point, the capacitor node 24 is then decoupled from VSS by turning off transistor 22 and turning on transistor 24 in response to the CLOCK3 signal to couple the capacitor node 24 to VCC. This drives the voltage on the intermediate node 16 above VCC. Transistor 14 is then turned "on" in response to the CLOCK2 signal to connect the intermediate node 16 to VCCP and charge is transferred to VCCP. The intermediate node 16 is then disconnected from VCCP by turning "off" transistor 14 in response to the CLOCK2 signal. The capacitor node 24 is then disconnected from VCC and connected to VSS by turning "off" transistor 20 and turning "on" transistor 22 in response to the CLOCK3 signal. Transistor 12 is then turned on in response to the CLOCK1 signal coupling the intermediate node 16 to VCC thereby restoring the state of the capacitor 26. Repeating the foregoing steps results in charge being "pumped" from a level of VCC to the higher voltage supply VCCP.

With reference additionally now to FIG. 5, a corresponding timing diagram of the CLOCK1, CLOCK2 and CLOCK3 signal inputs to the charge pump circuit 50 of FIG. 2 is shown. As previously described, the various clock signals function to couple the capacitor node 62 to VSS through the operation of transistor 60 in response to the CLOCK3 signal applied through inverter 72 while transistor 52 couples the intermediate node 56 to VCC in response to the CLOCK1 signal. Transistor 52 is then turned "off" in response to CLOCK1 signal. At this point, the capacitor node 62 is then decoupled from VSS by turning off transistor 60 and turning on transistor 58 in response to the CLOCK3 signal coupled through inverters 72 and 66 respectively to couple the capacitor node 62 to VCC. This drives the voltage on the intermediate node 56 above VCC. Transistor 54 is then turned "on" in response to the CLOCK2 signal to connect the intermediate node 56 to VCCP and charge is

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transferred to VCCP. The intermediate node 56 is then disconnected from VCCP by turning "off" transistor 54 in response to the CLOCK2 signal. The capacitor node 62 is then disconnected from VCC and connected to VSS by turning "off" transistor 58 and turning "on" transistor 60 in response to the CLOCK3 signal and inverters 66 and 72 respectively. Transistor 52 is then turned on in response to the CLOCK1 signal coupling the intermediate node 56 to VCC thereby restoring the state of the capacitor 64. Repeating the foregoing steps results in charge being "pumped" from a level of VCC to the higher voltage supply VCCP.

With reference additionally now to FIG. 6, the operation of the alternative embodiment of the charge pump circuit 100 of FIG. 3 is shown. At time A in FIG. 6, Transistor 58, 60, 52, and 54 are all in the "off" state. CLOCK2 then goes high connecting node 56 to VCCP. Since node 62 is "tristate" (i.e. not held either VCC or VSS) little charge is required to bring 56 to the same potential as VCCP therefore little noise results. CLOCK3 then goes high causing the output of inverter 66 to go low. Transistor 70 of inverter 66 is sized (small) to slowly pull the gate of transistor 58 low causing 62 to be pulled slowly to VCC causing charge to be transferred from 56 through transistor 54 to VCCP. The slow  $dV/dt$  of 62 results in lowered  $dI/dt$  as shown at time B in FIG. 9. CLOCK3 then goes low causing the gate of transistor 58 to go high shutting transistor 58 off. This transistor is fast but little  $dI/dt$  is seen in FIG. 9 because transistor 58 has little current flowing by the time CLOCK3 goes low as can be seen in FIG. 9. CLOCK2 then goes low shutting off transistor 54 and CLOCK1 goes high turning on transistor 78. As before, when transistor 52 is turned on node 62 is tristate and there is little charge required to equilibrate node 56 to VCC and hence little  $dI/dt$  is seen. CLOCK4 then goes low causing the gate of transistor 60 to be turned on. Transistor 74 is sized (small) to pull the gate of transistor 60 up slowly to reduce the  $dI/dt$  at time C in FIG. 9.

With reference additionally now to FIG. 7, in those applications wherein VCCP is required to provide relatively large amounts of current, the capacitor 26 and transistors 12, 14, 20 and 22 in the conventional charge pump circuit 10 of FIG. 1 must also be large in size. When the transistors switch "on" and "off" to drive the capacitor 26 nodes "high" or "low", large amounts of current flow and the rate of change of the current (" $dI/dt$ ") is also large. The voltage supplies VCC and VSS are sourcing and sinking this current so VCC and VSS voltage levels vary as a result of the charge pump operation. This voltage variation is "noise" and this noise on VSS and VCC can cause an IC device to fail to function properly in a system. The amount of noise is determined by the resistance and inductance of VCC and VSS and for IC devices, the most difficult source of noise to control is  $dI/dt$  because the die bond wires present significant levels of inductance.

In the conventional charge pump circuit 10, the pump capacitor is driven by the inverter 18 causing a relatively large change in current over time (" $dI/dt$ ") to occur when the capacitor node 24 is driven and when the transistor connecting the intermediate node 16 to the power supply is turned "on". A similar  $dI/dt$  also occurs when the transistor connecting the intermediate node 16 to the VCCP pumped node is turned "on". These rapid changes in current ( $dI/dt$ ) result in undesired and sometimes unacceptable noise in the circuit as indicated by the slope of the current spikes shown in FIG. 7.

With reference additionally now to FIG. 8, a timing diagram illustrative of the current flow on the VCC, VSS and VCCP sources for the "fast-off/slow-on" embodiment of the

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charge pump circuit depicted in FIG. 2 is shown. This figure shows clearly, in comparison to that of the preceding figure, that the  $dl/dt$  at 2.0, 17.0, 32.0 and 47.0 nanoseconds have been dramatically reduced.

With reference additionally now to FIG. 9 a similar timing diagram illustrative of the current flow on the VCC, VSS and VCCP sources for the alternative "tri-state" embodiment of the charge pump circuit depicted in FIG. 3 is shown. Note the absence of the current spike present at time D in FIG. 8. This is due to the "tristate" modification of FIG. 3. This diagram shows that there are but relatively small current spikes at 0.0, 1.0, 15.0, 16.0, 30.0, 31.0, 45.0 and 46.0 nanoseconds. These current spikes have a relatively high  $dl/dt$  but are also of very short duration such that they will not generate appreciable VCC or VSS noise.

The embodiments disclosed have been single stage type charge pumps. It is understood that these inventions could as easily be applied to charge pumps containing multiple stages. While there have been described above the principles of the present invention in conjunction with specific circuits and transistor technology, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

What is claimed is:

1. An integrated circuit device including a charge pump circuit comprising:

- a capacitive element having first and second terminals thereof coupled to an intermediate and capacitor nodes respectively;
- a first switching device for selectively coupling said intermediate node to a supply voltage line in response to a first clocking signal;
- a second switching device for selectively coupling said intermediate node to a pumped voltage line in response to a second clocking signal;
- a first inverter having an input coupled to receive a third clocking signal and an output coupled to a third switching device for selectively coupling said capacitor node to said supply voltage line in response to said third clocking signal; and
- a second inverter having an input coupled to receive said third clocking signal and an output coupled to a fourth switching device for selectively coupling said capacitor node to a ground voltage line in response to said third clocking signal.

2. The integrated circuit of claim 1 wherein said capacitive element comprises a capacitor having a capacitance of substantially 300 pf.

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3. The integrated circuit of claim 1 wherein said first switching device comprises an N-channel MOS transistor.

4. The integrated circuit of claim 1 wherein said second switching device comprises an N-channel MOS transistor.

5. The integrated circuit of claim 1 wherein said third switching device comprises a P-channel MOS transistor.

6. The integrated circuit of claim 1 wherein said fourth switching device comprises an N-channel MOS transistor.

7. The integrated circuit of claim 1 wherein said first and second inverters comprise first and second CMOS inverters.

8. The integrated circuit of claim 7 wherein said first and second CMOS inverters comprise series connected P-channel and N-channel transistor pairs.

9. The integrated circuit of claim 8 wherein said P-channel transistor of said first CMOS inverter is larger than said P-channel transistor of said second CMOS inverter.

10. The integrated circuit of claim 8 wherein said N-channel transistor of said second CMOS inverter is larger than said N-channel transistor of said first CMOS inverter.

11. An integrated circuit device including a charge pump circuit comprising:

- a capacitive element having first and second terminals thereof coupled to an intermediate and capacitor nodes respectively;
- a first switching device for selectively coupling said intermediate node to a supply voltage line in response to a first clocking signal;
- a second switching device for selectively coupling said intermediate node to a pumped voltage line in response to a second clocking signal;
- a first inverter having an input coupled to receive a third clocking signal and an output coupled to a third switching device for selectively coupling said capacitor node to said supply voltage line in response to said third clocking signal; and
- a second inverter having an input coupled to receive a fourth clocking signal and an output coupled to a fourth switching device for selectively coupling said capacitor node to a ground voltage line in response to said fourth clocking signal.

12. The integrated circuit of claim 11 wherein said capacitive element comprises a capacitor having a capacitance of substantially 300 pf.

13. The integrated circuit of claim 11 wherein said first switching device comprises an N-channel MOS transistor.

14. The integrated circuit of claim 11 wherein said second switching device comprises an N-channel MOS transistor.

15. The integrated circuit of claim 11 wherein said third switching device comprises a P-channel MOS transistor.

16. The integrated circuit of claim 11 wherein said fourth switching device comprises an N-channel MOS transistor.

17. The integrated circuit of claim 11 wherein said first and second inverters comprise first and second CMOS inverters.

18. The integrated circuit of claim 17 wherein said first and second CMOS inverters comprise series connected P-channel and N-channel transistor pairs.

19. The integrated circuit of claim 18 wherein said P-channel transistor of said first CMOS inverter is larger than said P-channel transistor of said second CMOS inverter.

20. The integrated circuit of claim 18 wherein said N-channel transistor of said second CMOS inverter is larger than said N-channel transistor of said first CMOS inverter.

21. The integrated circuit of claim 11 wherein said third and fourth switching devices may be switched between

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states independently of each other in response to said third and fourth clocking signals respectively.

22. A method for operating a charge pump in an integrated circuit device comprising:

coupling a first terminal of a capacitive element to a  
supply voltage line while a second terminal of said  
capacitive element is coupled to a ground voltage line;  
firstly decoupling said first terminal from said supply  
voltage line;

secondly decoupling said second terminal from said  
ground around line and coupling said second terminal  
to said supply voltage line;

thirdly coupling said first terminal to a pumped voltage  
line;

fourthly decoupling said first terminal from said pumped  
voltage line;

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fifthly decoupling said second terminal from said supply  
voltage line and subsequently coupling said second  
terminal to a reference voltage line; and

sixthly coupling said first terminal to said supply voltage  
line.

23. The method of claim 22 wherein said step of secondly  
decoupling said second terminal from said reference voltage  
line occurs relatively more quickly than said corresponding  
step of coupling said second terminal to said supply voltage  
line.

24. The method of claim 22 wherein said step of fifthly  
decoupling said second terminal from said supply voltage  
line occurs relatively more quickly than said corresponding  
step of coupling said second terminal to said reference  
voltage line.

\* \* \* \* \*



US005446418A

**United States Patent** [19]

Hara et al.

[11] **Patent Number:** 5,446,418[45] **Date of Patent:** Aug. 29, 1995[54] **RING OSCILLATOR AND CONSTANT VOLTAGE GENERATION CIRCUIT**[75] **Inventors:** Motoko Hara; Takeshi Kajimoto,  
both of Hyogo, Japan[73] **Assignee:** Mitsubishi Denki Kabushiki Kaisha,  
Tokyo, Japan[21] **Appl. No.:** 147,268[22] **Filed:** Nov. 5, 1993[30] **Foreign Application Priority Data**

Nov. 6, 1992 [JP] Japan ..... 4-296945

[51] **Int. Cl.<sup>6</sup>** ..... H03K 3/353[52] **U.S. Cl.** ..... 331/57; 331/108 B;  
365/189.09[58] **Field of Search** ..... 331/57, 108 B, 135,  
331/46, 49; 365/189.06, 189.07, 189.09;  
327/535, 536, 537, 538, 540, 545[56] **References Cited****U.S. PATENT DOCUMENTS**

4,536,720 8/1985 Cranford, Jr. et al. .... 331/57

4,853,654 8/1989 Sakurai ..... 331/57

4,891,609 1/1990 Eilley ..... 331/108 B

**FOREIGN PATENT DOCUMENTS**

0383549A2 8/1990 European Pat. Off. .

3001428A1 7/1980 Germany .

3042323C2 6/1981 Germany .

3321553A1 12/1983 Germany .

61-147614 7/1986 Japan .

3-259619 11/1991 Japan .

*Primary Examiner*—Robert J. Pascal*Assistant Examiner*—David Vu*Attorney, Agent, or Firm*—Lowe, Price, LeBlanc &  
Becker[57] **ABSTRACT**

A ring oscillator according to the invention includes a plurality of inverters cascade-connected between an input node and an output node. Each inverter includes four transistors connected in series between a power supply node and a ground node. A first pair of transistors each have a channel sized to have an input capacitance for delaying the signal of a preceding stage inverter for a prescribed time period. A second pair of transistors are coupled to a current mirror circuit and limits current flowing through the first pair of transistors. Thus, power consumption for obtaining a signal in a prescribed cycle is reduced.

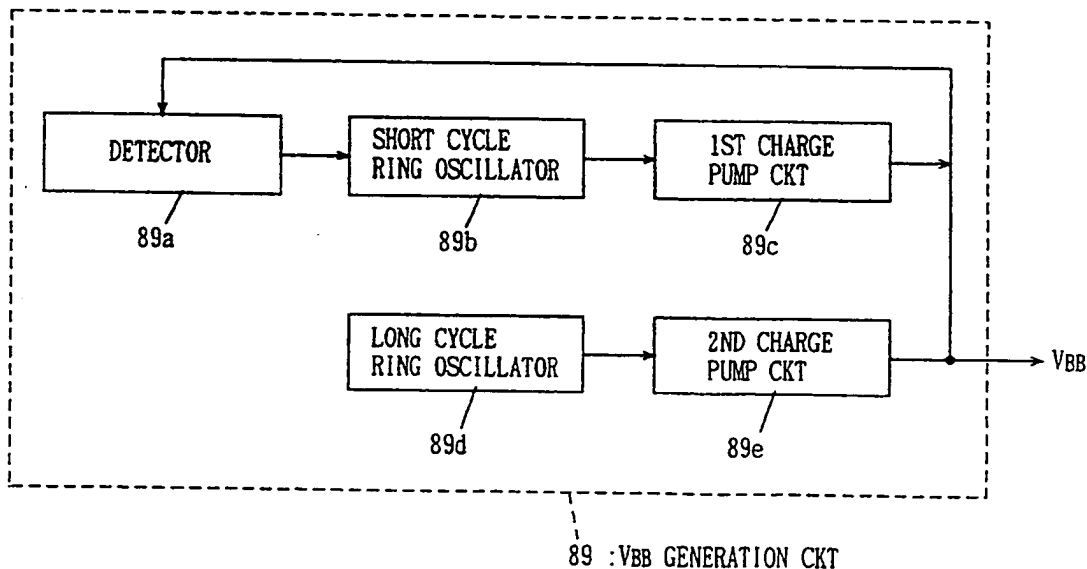
**5 Claims, 17 Drawing Sheets**

FIG. 1

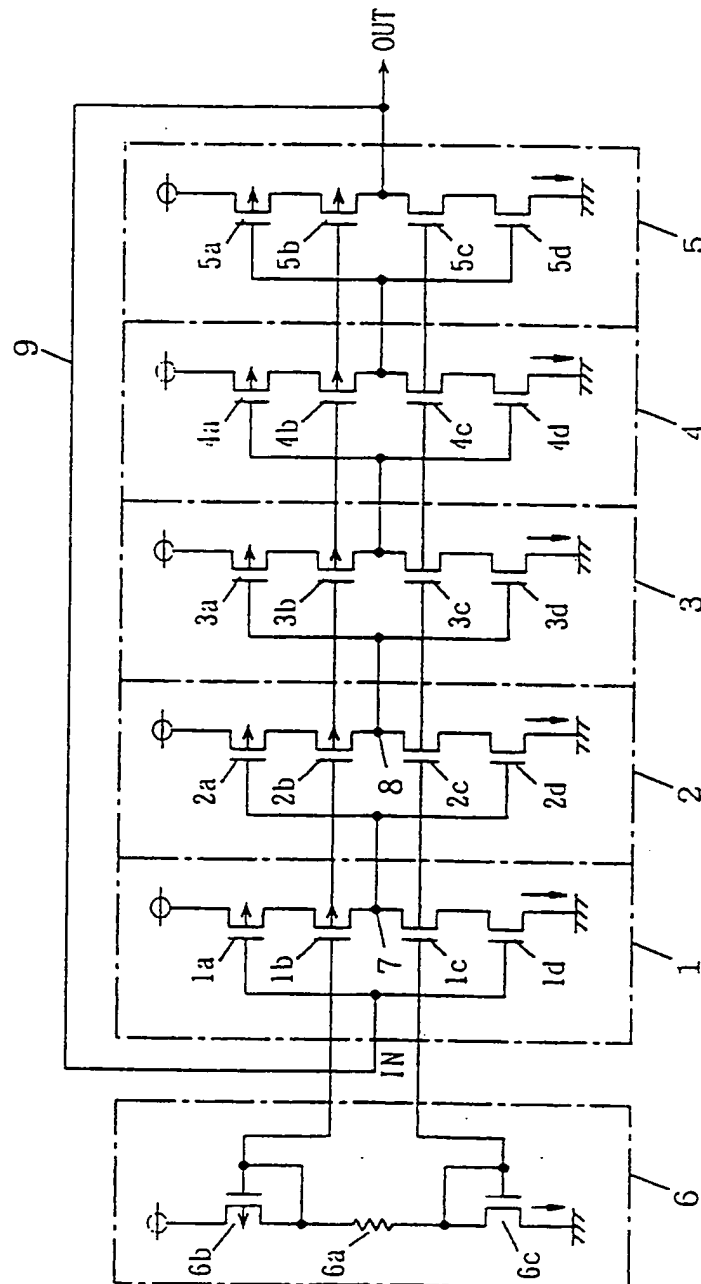


FIG. 2

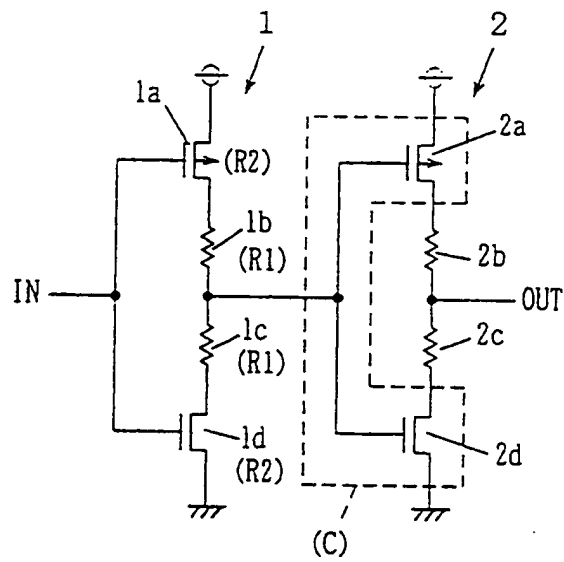


FIG. 3

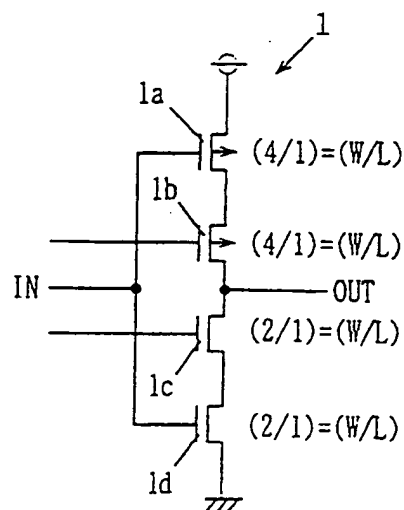




FIG. 4

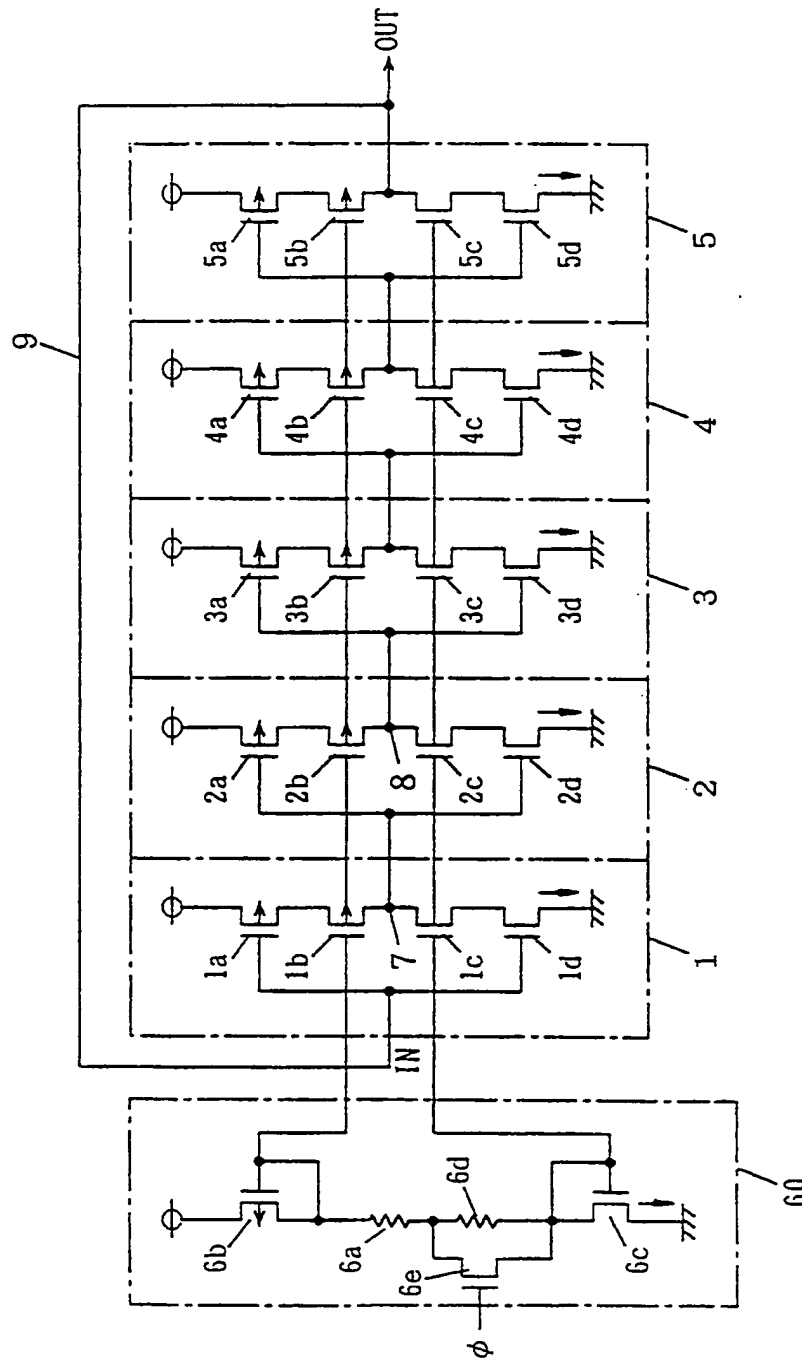


FIG. 5

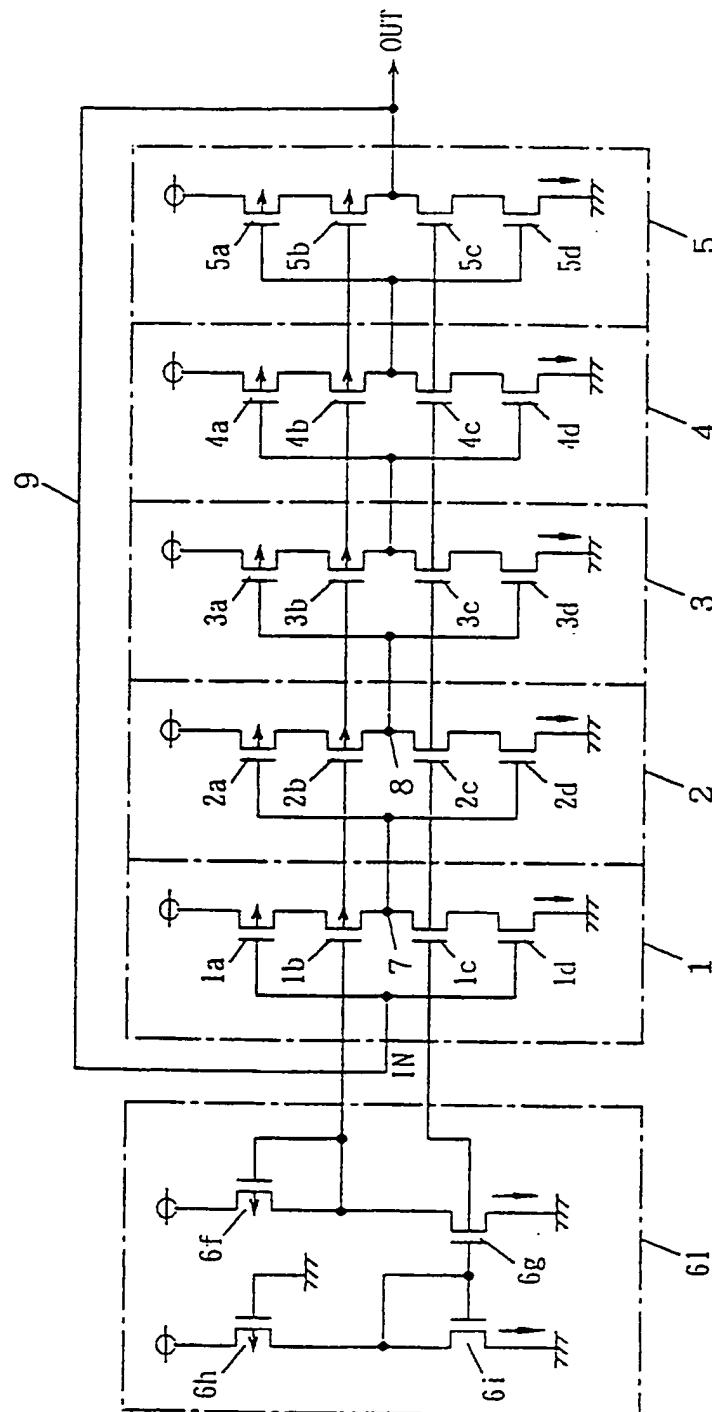


FIG. 6

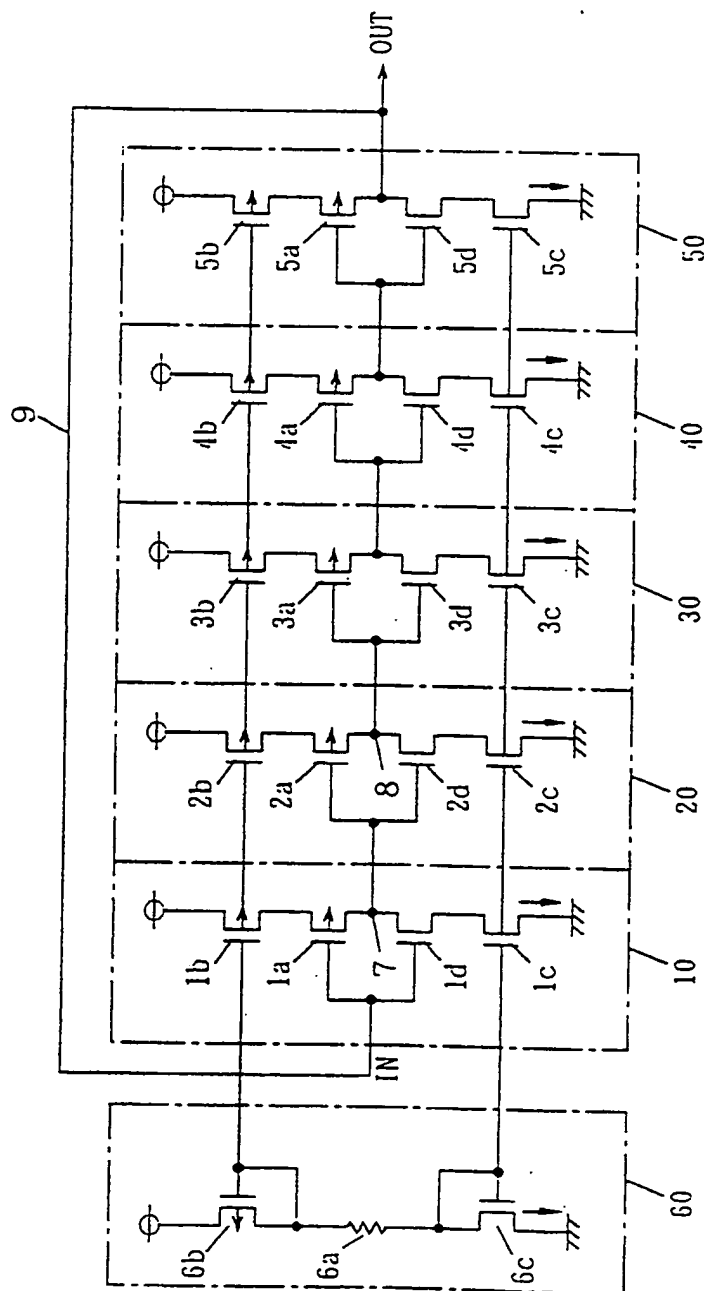


FIG. 7

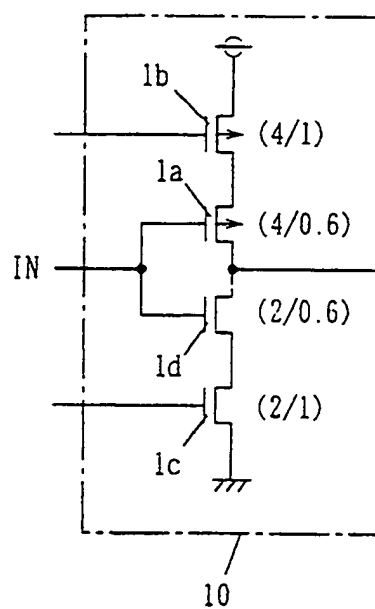


FIG. 8

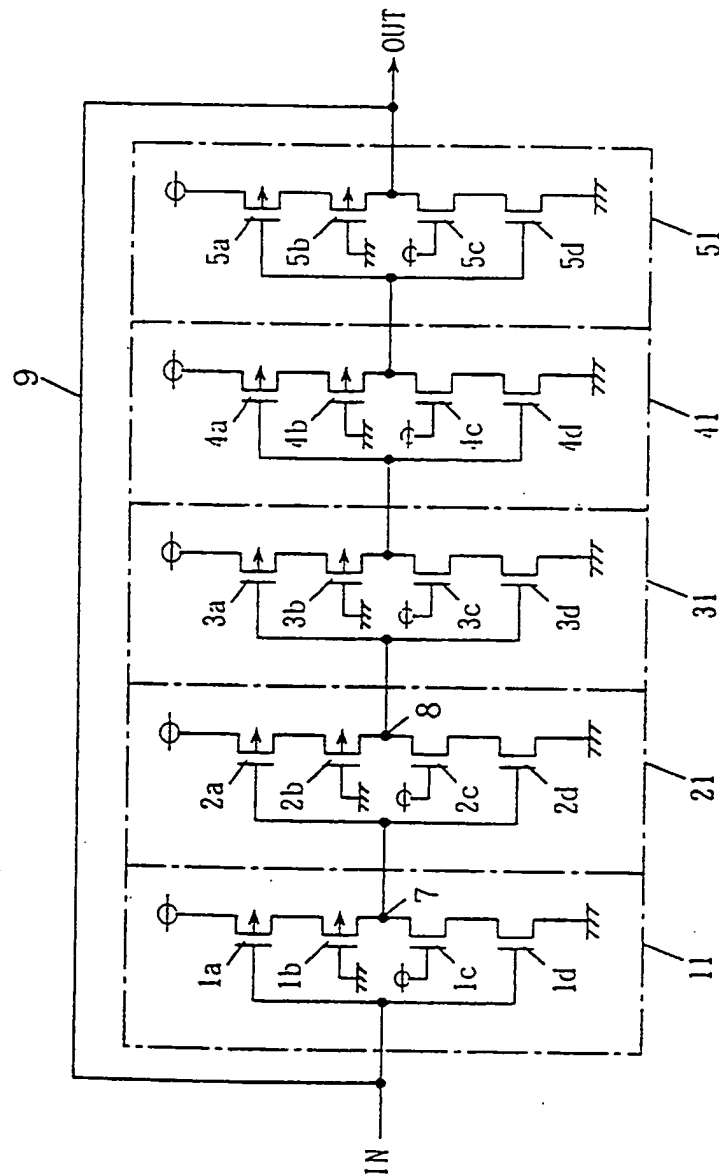


FIG. 9

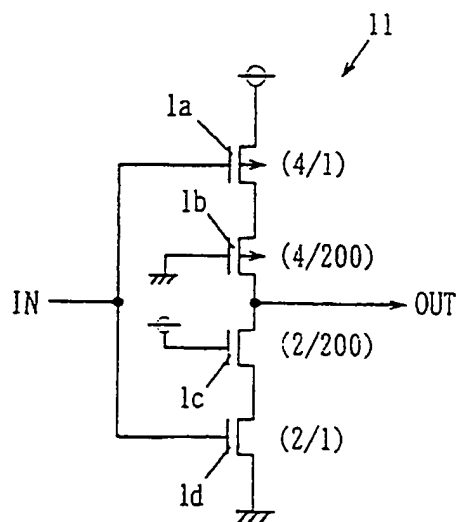


FIG. 10

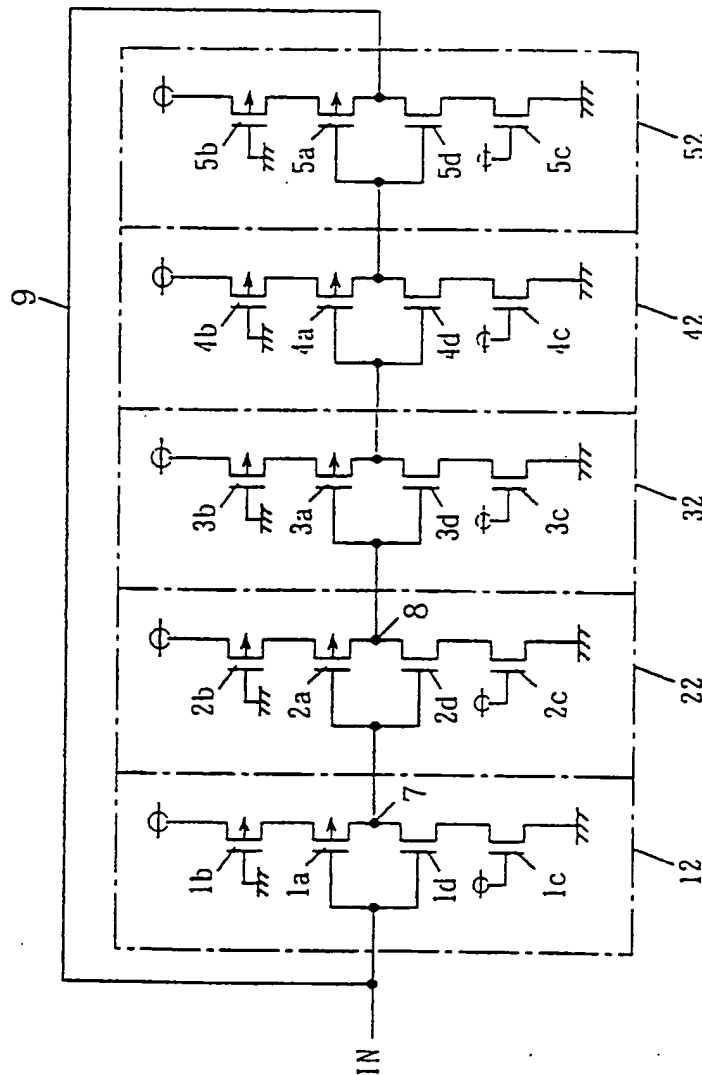
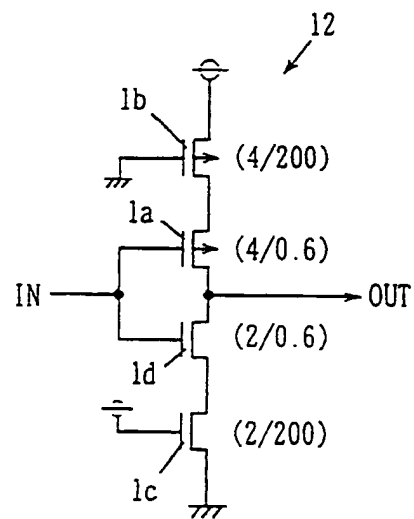


FIG. 11





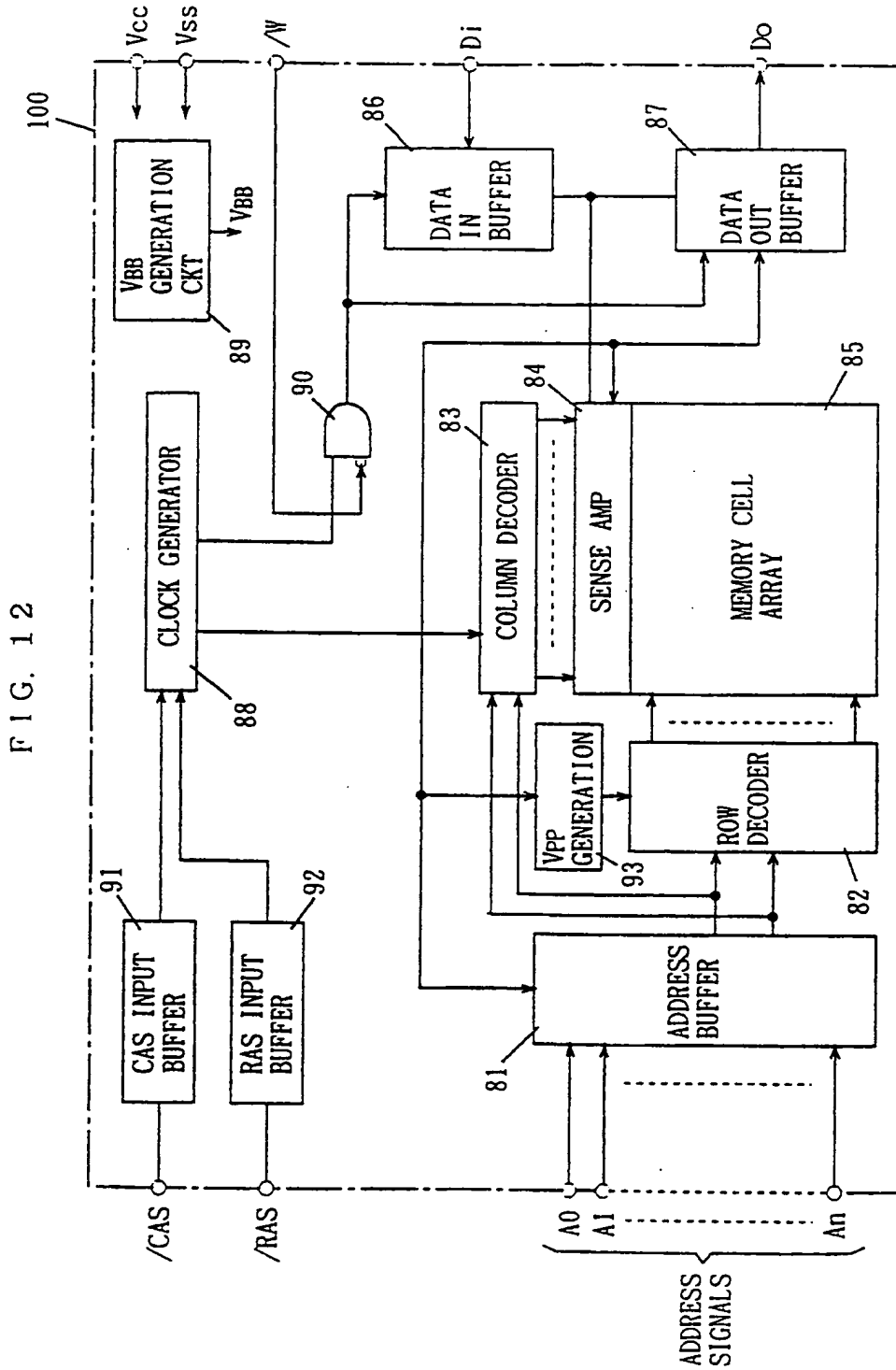
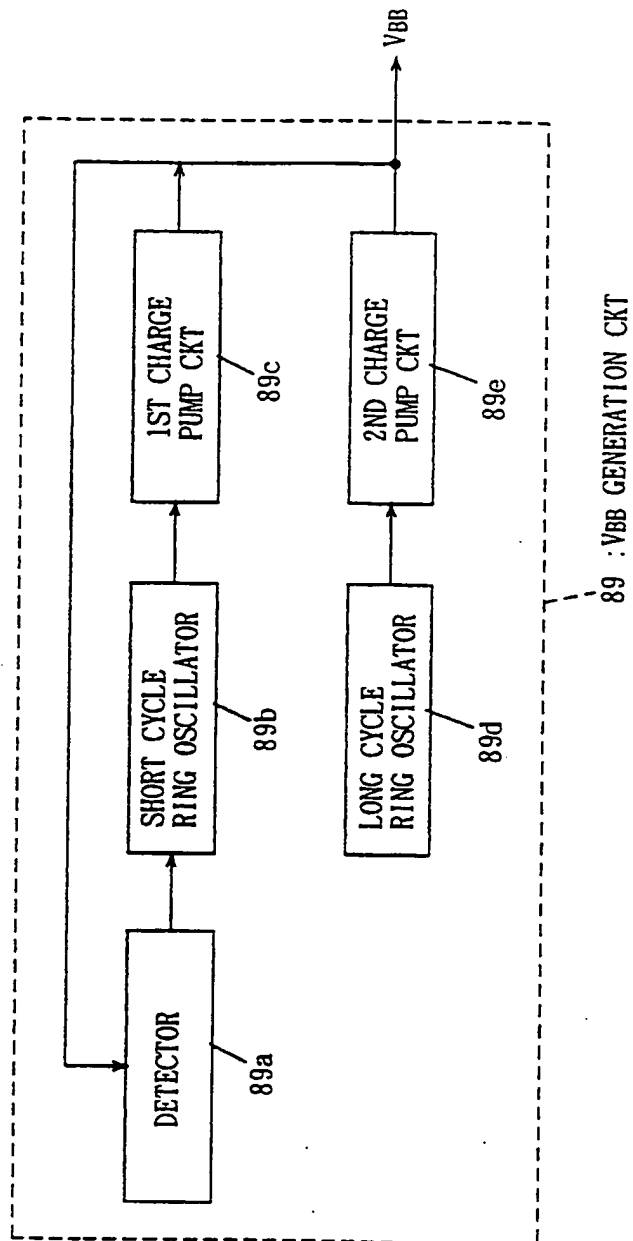


FIG. 13



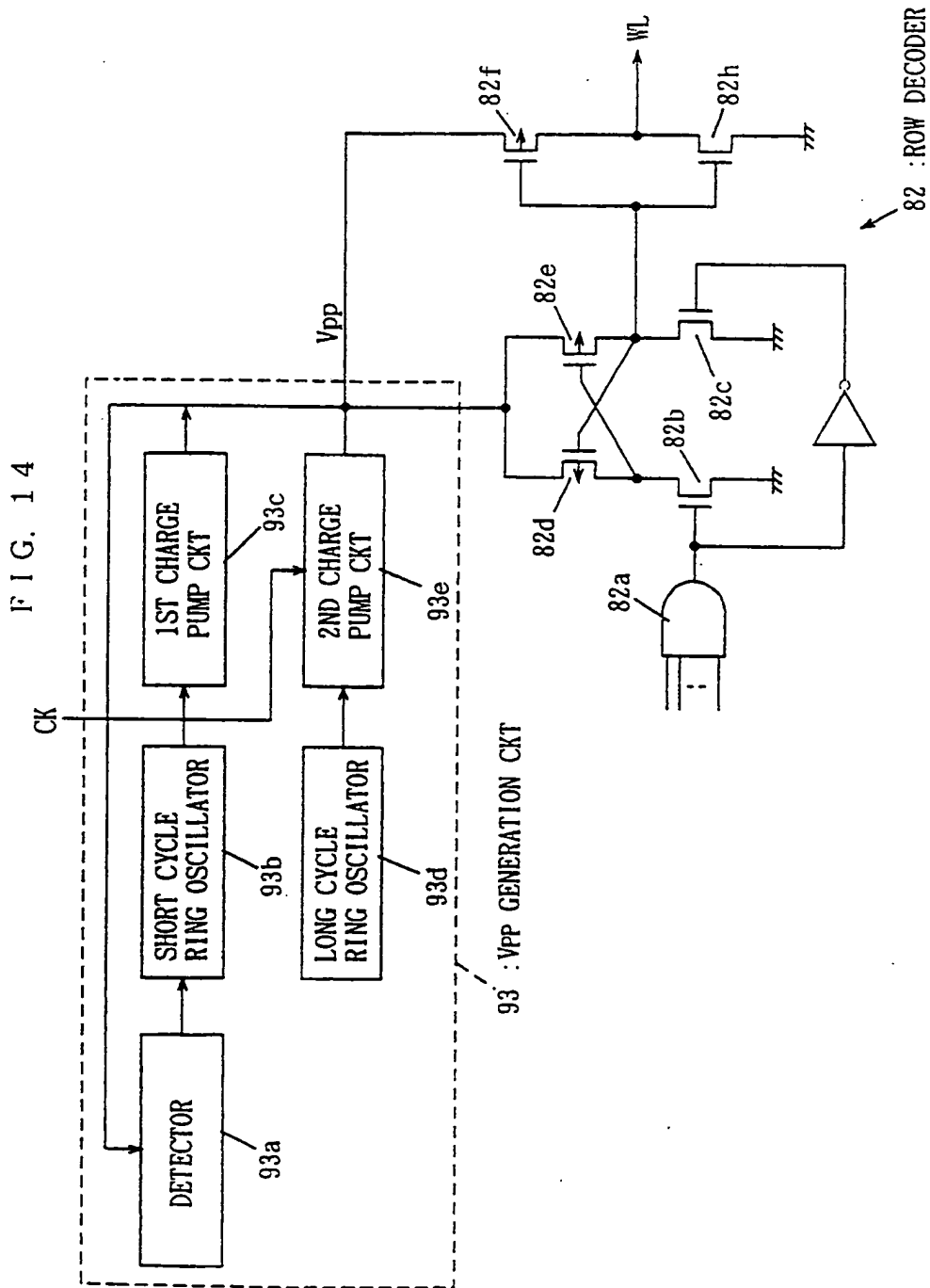


FIG. 15 PRIOR ART

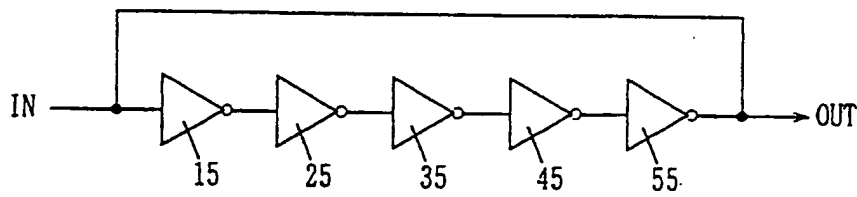


FIG. 16 PRIOR ART

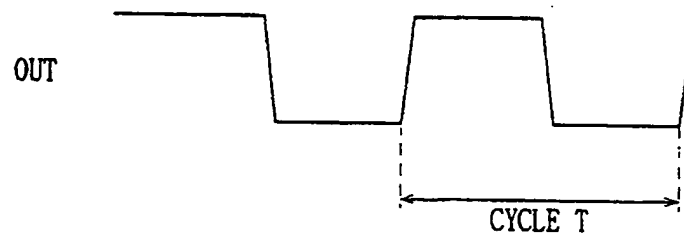


FIG. 17A PRIOR ART

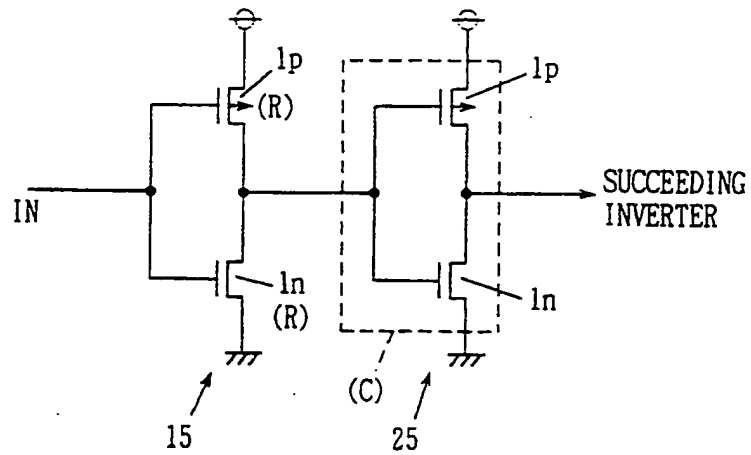


FIG. 17B PRIOR ART

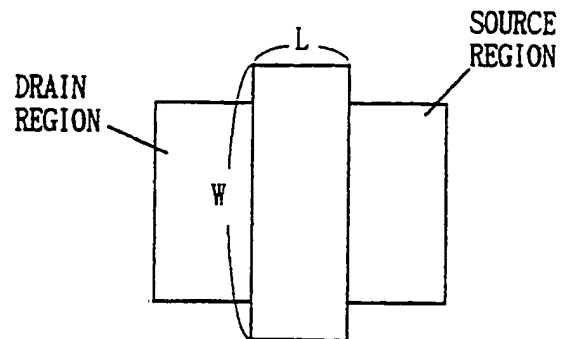


FIG. 18 PRIOR ART

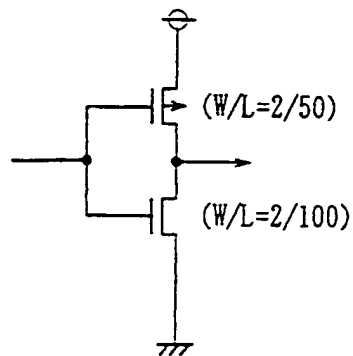


FIG. 19 PRIOR ART

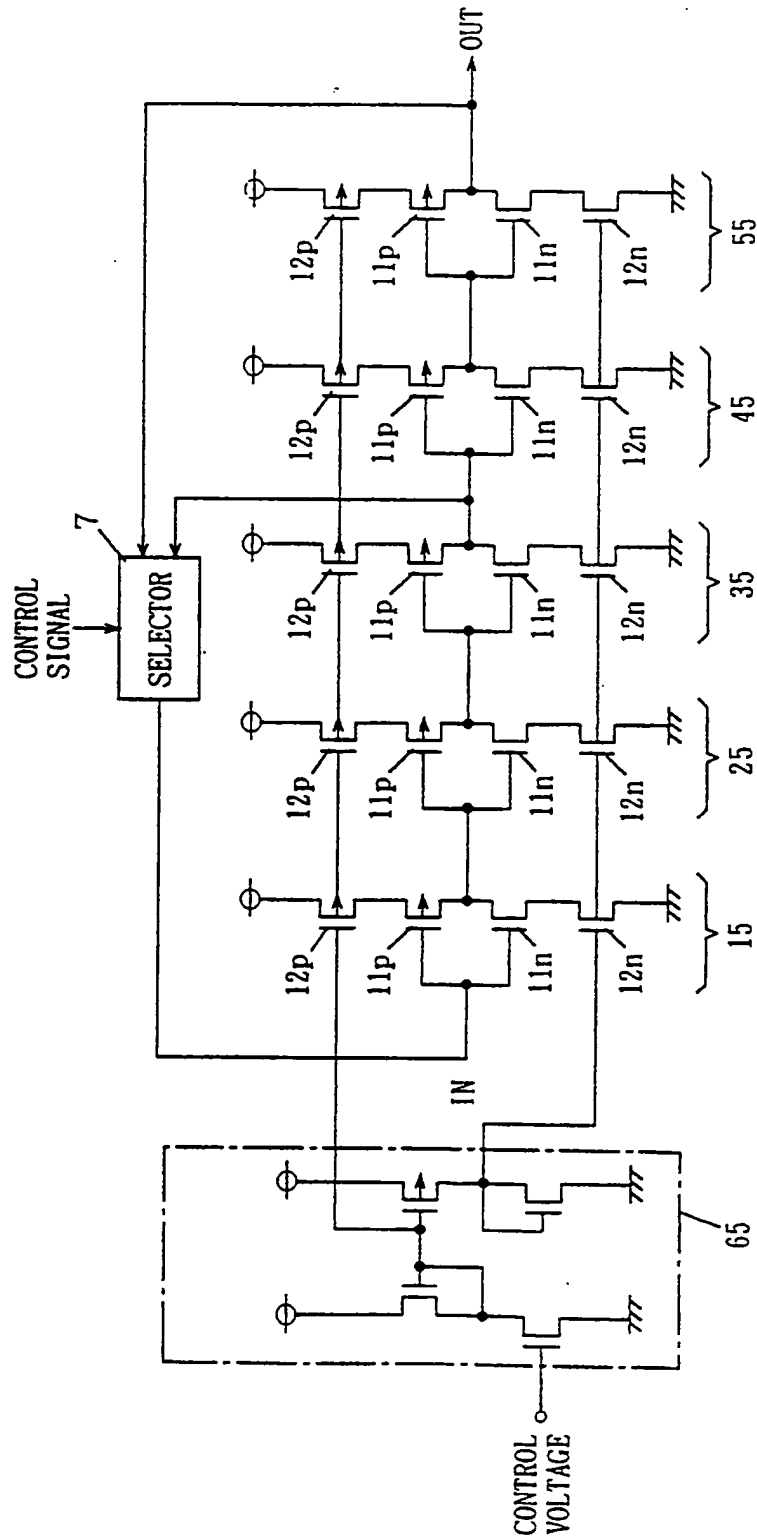
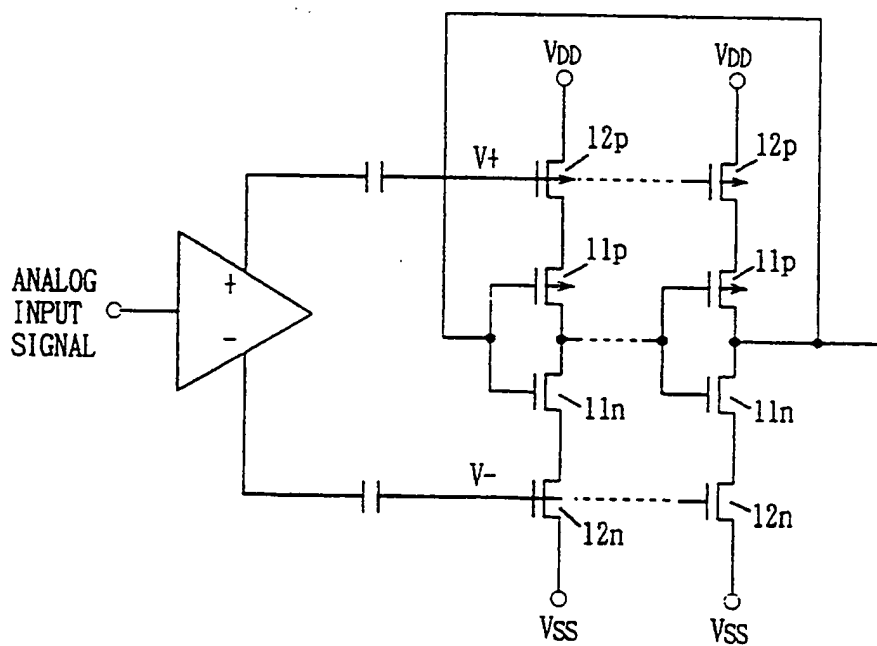


FIG. 20 PRIOR ART



# RING OSCILLATOR AND CONSTANT VOLTAGE GENERATION CIRCUIT

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a ring oscillator having a plurality of cascade-connected inverters for generating an output signal of a prescribed cycle by feeding back a signal on an output terminal to an input terminal, and a constant voltage generation circuit incorporating such a ring oscillator.

### 2. Description of the Background Art

FIG. 15 is a circuit diagram showing a conventional ring oscillator. Referring to FIG. 15, the ring oscillator includes inverters 15, 25, 35, 45, and 55. First stage inverter 15 has its input node connected to the output node of final stage inverter 55, and its output node connected to the input node of second stage inverter 25. The second to fourth stage inverters each have an input node connected to the output node of a preceding stage inverter, and an output node connected to the input node of a succeeding stage inverter.

Although in FIG. 15 the number of stages of the inverters is five, odd-number stages, at least three stages may be provided.

Operation of the ring oscillator in FIG. 15 will be described. When an input signal is input to inverter 15, an output signal OUT which is the inverse of input signal IN is output from final stage inverter 55. Output signal OUT is fed back to the input node of first stage inverter 15, so that output signal OUT becomes a signal inverted in a fixed cycle T as illustrated in FIG. 16.

Now, a description follows in conjunction with FIGS. 17A and 17B on how an oscillation cycle for the ring oscillator is determined. FIG. 17A is a circuit diagram showing in detail first stage inverter 15 and second stage inverter 25 in the ring oscillator in FIG. 15. FIG. 17B is a plan view showing a transistor forming each inverter in FIG. 17A.

Referring to FIGS. 17A and 17B, inverters 15 and 25 each include a PMOS transistor 1p and an NMOS transistor in connected in a complementary manner. PMOS transistor 1p and NMOS transistor in each have an ON resistance value R. Inverters 15 and 25 each have a capacitance C determined by the channel length L and channel width W of each of PMOS transistor 1p and NMOS transistor 1n.

The oscillation cycle T of the ring oscillator is the sum of time delays t of the inverters, and time delay t is represented as follows:

$$t \propto R \times C$$

$$R \propto L/W, C \propto W \times L$$

$$t \propto L^2$$

From expression (2), the time delay t of each inverter is determined by the channel length L of an MOS transistor. Accordingly, in order to prolong the cycle of the output signal, approaches such as (1) to increase the channel length, (2) increase the number of stages of inverters, and (3) to decrease the amount of current supply to the inverters can be considered.

However, increase of R (=L/W) decreases charge/discharge current to/from the gate, but increases C (=W×L) as well, and therefore charge/discharge current to/from the gate is conversely increased. Such

increase of charge/discharge current increases power consumption by the semiconductor integrated circuit.

Accordingly, in order to reduce power consumption, two approaches, i.e. to increased R and to decrease C are considered.

For example, in order to set 200 ns for the cycle of the ring oscillator shown in FIG. 15, the channel width W/channel length L ratios of PMOS transistor 1p and NMOS transistor 1n are formed to be  $\frac{1}{2}$ ,  $\frac{1}{2}$ , respectively. Meanwhile, in order to set 7.6μs for the cycle and 1.7μA for consumption current, as illustrated in FIG. 18, the W/L of PMOS transistor 1p and NMOS transistor in are formed to be 2/50, 2/100, respectively.

FIG. 19 is a circuit diagram showing a ring oscillator incorporated in a PLL circuit disclosed in Japanese Patent Laying-Open No. 3-259619. The ring oscillator serially changes the oscillation cycle by controlling the number of stages of inverters and the amount of current supply to the inverters.

Referring to FIG. 19, the ring oscillator includes a buffer 65, inverters 15-55, and a selector 7. Selector 7 selects the output of third stage inverter 35 or fifth stage inverter 55 in response to a control signal, and feeds back the output to first stage inverter 15. Inverters 15, 25, 35, 45, and 55 each includes PMOS transistors 11p and 12p, and NMOS transistors 11n and 12n connected in series between a power supply node and a ground node. PMOS transistor 11p and NMOS transistor 11n are turned on/off in a complementary manner in response to an input signal. PMOS transistor 12p and NMOS transistor 12n have their ON resistance values changed in response to the output of buffer 65.

In operation, the number of stages of inverters is selected in response to a control signal, and the oscillation cycle is changed. In response to a control voltage, buffer 65 controls the ON resistance values of PMOS transistor 12p and NMOS transistor 12n, and therefore the oscillation cycle can be changed.

In the ring oscillator shown in FIGS. 15-18, transistors with an increased channel length L are used when an output signal of a long cycle is generated, and therefore resistance value R increases, current flowing from the power supply terminal to the output node and current flowing from the output node to the ground node decrease, thus decreasing current consumption by the ring oscillator.

However, capacitance C increases, and therefore current consumption by the capacitor increases. A ring oscillator with such a large current consumption is not suitable for application to a circuit for generating backup voltage for a memory device, such as to a substrate bias voltage generation circuit.

Transistors 12p and 12n for current limiting shown in FIG. 19 are applied only for a PLL circuit device and used only for serially controlling the oscillation cycle. Accordingly, the oscillation frequency changes around a reference clock signal, and therefore the size of the ring oscillator mostly depends on the gate lengths L of transistors 11p and 11n for switching. Accordingly, in order to provide a ring oscillator with an oscillating cycle of 7.6μs and a current consumption of 1.91μA, for example, the gate lengths L of transistors 11p and 11n for switching must be the same as those shown in FIG. 18. Therefore, the current consumption by input capacitance C cannot be reduced.

FIG. 20 is a circuit diagram showing a ring oscillator for FM-modulating an analog input signal. The circuit is



disclosed in Japanese Patent Laying-Open No. 61-147614 (laid open on Jul. 15, 1986).

The ring oscillator shown in FIG. 20 is different from the ring oscillator in FIG. 19 in that PMOSFET 12p and NMOSFET 12n control current in response to an analog input signal.

The circuit shown in FIG. 20 can provide a pulse signal having a frequency corresponding to the level of an analog input signal.

The longest cycle for the pulse signal is about at most ten times as long as the shortest cycle. Accordingly, in order to provide a ring oscillator having a large cycle (7.6 $\mu$ s) and current consumption of 1.91 $\mu$ A, the gate lengths L of transistors 11p and 11n for switching must be the same as those in FIG. 18. Therefore, current consumption due to input capacitance C cannot be reduced.

### SUMMARY OF THE INVENTION

It is an object of the invention to restrain current consumption in a ring oscillator generating an output signal of a prescribed cycle.

Another object of the invention is to restrain current consumption in a constant voltage generation circuit using a ring oscillator.

Briefly stated, a ring oscillator according to the invention includes a plurality of inverters and a feedback interconnection. The plurality of inverters are cascade-connected between input and output nodes. Each inverter includes first and second transistors and a current limiting element. The first and second transistors each have a channel sized so as to have an input capacitance component for delaying the output signal of a preceding stage inverter for a prescribed time period, and are turned on/off in a complementary manner in response to the output signal of the preceding stage inverter. The current limiting element has a mutual conductance sized corresponding to a resistance component for delaying the output signal of a preceding stage inverter for a prescribed time period together with the above-described input capacitance component, and limits current flowing from the power supply node and the ground node to the first and second transistors. The feedback interconnection feeds back the signal of the output node to the input node.

In operation, the input capacitance component is determined by the sizes of the channels of the first and second transistors, the resistance component is determined by limiting current with the current limiting element, and therefore the input capacitance component and the resistance component for delaying the signal of a preceding stage inverter can independently be determined. Accordingly, if, for example, a ring oscillator having a short oscillation cycle of about 200 nsec can be made into a ring oscillator having a long cycle of about 7 $\mu$ sec such as a substrate potential generation circuit by limiting current. Furthermore, since the input capacitance component is small, charge/discharge current attributable to the input capacitance component is small, and power consumption is reduced as compared to a ring oscillator used in a conventional substrate potential generation circuit.

When the current limiting element is formed of third and fourth transistors and a current determining element coupled operatively to the control electrodes of third and fourth transistors, the ON resistance values of the third and fourth transistors can be controlled, and therefore an output signal having a prescribed cycle

(cycle for substrate voltage) can be generated even with the gate lengths of the third and fourth transistors being reduced, thus reducing the area of the ring oscillator.

Furthermore, when first, third, fourth, and first transistors are serially connected in the order between the power supply node and the ground node, through current flowing from the power supply node to the ground node can further be reduced.

Briefly stated, the constant voltage generation circuit according to the invention includes a first ring oscillator, a first voltage generator, a level drop detector, a second ring oscillator, and a second voltage generator.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing one embodiment of a ring oscillator according to the invention;

FIG. 2 is a circuit diagram for use in illustration of operation of one stage of inverter shown in FIG. 1;

FIG. 3 is a circuit diagram showing a specific example for operating the inverter shown in FIG. 1 in a prescribed cycle and with prescribed consumption current;

FIG. 4 is a circuit diagram showing a ring oscillator according to a second embodiment of the invention;

FIG. 5 is a circuit diagram showing a ring oscillator according to a third embodiment of the invention;

FIG. 6 is a circuit diagram showing a ring oscillator according to a fourth embodiment of the invention;

FIG. 7 is a circuit diagram showing a specific example for operating the ring oscillator shown in FIG. 6 in a prescribed cycle and with a prescribed current consumption;

FIG. 8 is a circuit diagram showing a ring oscillator according to a fifth embodiment of the invention;

FIG. 9 is a circuit diagram showing a specific example for operating the inverter in FIG. 8 in a prescribed cycle and with a prescribed current consumption;

FIG. 10 is a circuit diagram showing a ring oscillator according to a sixth embodiment of the invention;

FIG. 11 is a circuit diagram showing a specific example for operating the inverter shown in FIG. 10 in a prescribed cycle and with a prescribed current consumption;

FIG. 12 is a block diagram showing a DRAM including a VBB generation circuit and a Vpp generation circuit;

FIG. 13 is a block diagram showing the VBB generation circuit shown in FIG. 12;

FIG. 14 is a block diagram showing the Vpp generation circuit shown in FIG. 12;

FIG. 15 is a circuit diagram showing a conventional ring oscillator;

FIG. 16 is a waveform chart showing the output of the ring oscillator shown in FIG. 15;

FIG. 17A is a circuit diagram showing in detail first stage inverter 15 and second stage inverter 25 shown in FIG. 15;

FIG. 17B is a plan view showing a transistor constituting each inverter shown in FIG. 17A;

FIG. 18 is a circuit diagram showing a specific example for operating the ring oscillator shown in FIG. 15 for 7.6 $\mu$ s, and 1.91 $\mu$ A;

FIG. 19 is a circuit diagram showing another example of a conventional ring oscillator; and

FIG. 20 is a circuit diagram showing yet another example of a conventional ring oscillator.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a circuit diagram showing a ring oscillator according to one embodiment of the invention. Referring to FIG. 1, the ring oscillator includes inverters 1-5, and a circuit 6 constituting part of a current mirror circuit. Inverter 1 includes P channel transistors 1a and 1b, and N channel transistors 1c and 1d. P channel transistor 1a has its one electrode connected to a power supply node, the other electrode connected to one electrode of P channel transistor 1b, and its gate electrode connected together with the gate electrode of N channel transistor 1d to an input node IN. P channel transistor 1b has its other electrode connected together with the other electrode of N channel transistor 1c to an output node 7, and its gate electrode connected to circuit 6 constituting part of the current mirror circuit. N channel transistor 1d has its one electrode connected to the ground node, and its other electrode connected to one electrode of N channel transistor 1c. N channel transistor 1c has its control electrode connected to circuit 6 constituting part of current mirror circuit. The above-described P channel transistor 1b and circuit 6, and N channel transistor 1c and circuit 6 constitute a current mirror circuit. P channel transistor 1a and N channel transistor 1d constitute a switching circuit. Inverters 2, 3, 4, and 5 have the same structure as inverter 1.

Now, operation of the ring oscillator shown in FIG. 1 will be described. It is assumed that input signal IN rises from 0 volt to power supply voltage  $V_{CC}$ . When input signal IN rises from 0 volt to power supply voltage  $V_{CC}$ , N channel transistor 1d is turned on. When N channel transistor 1d is completely turned on, and the gate-source voltage  $V_{GS}$  of N channel transistor 1c for limiting current is larger than a threshold voltage  $V_{TH}$ , N channel transistor 1c is turned on. In response, the voltage of node 7 decreases to GND, and the output of inverter 1 attains an "L" level. P channel transistor 2a among transistors 2a and 2d included in the second stage inverter receives the output of the "L" level and is turned on. When P channel transistor 2a is completely turned on and the gate-source voltage  $V_{GS}$  of P channel transistor 2b for limiting current is smaller than threshold voltage  $V_{TH}$ , P channel transistor 1b is turned on and the voltage of node 8 rises to  $V_{CC}$ . In response, the output of inverter 2 attains an "H" level.

The output of inverter 3 similarly attains an "L" level, the output of inverter 4 attains an "H" level, and the output of inverter 5, in other words output signal OUT attains an "L" level. Output signal OUT is used for the next input signal IN and output signal OUT is inverted in a cycle corresponding to delay time for the five stages of inverters.

Herein, the five stages of inverters are used to constituting the ring oscillator by way of illustration, but odd number stages more than five may be employed.

FIG. 2 is a diagram for use in illustration of operation of one stage of inverter for the ring oscillator shown in FIG. 1.

Referring to FIG. 2, P channel transistor 1a and N channel transistor 1d each have an ON resistance value  $R_2$ , and P channel transistor 1b and N channel transistor

1c each have an ON resistance value  $R_1$ . Capacitance created by the gates of P channel transistor 2a and N channel transistor 2d is referred to as C. Under the above-described condition, a time delay for one stage of inverter is given as follows:

$$t \propto f \quad (3)$$

As can be seen from expression (3), to decrease  $i$  can prolong the oscillation cycle with capacitance C corresponding to a reduced cycle, and consumption current can be reduced. The use of capacitance C corresponding to the reduced cycle means that the gate lengths and gate widths of P channel transistor 1a and N channel transistor 1d are small.

FIG. 3 is a diagram showing the gate width/gate length of inverter 1 shown in FIG. 1. The relation between oscillation cycle and current consumption by the inverter shown in FIG. 3 is set forth in Table 1.

TABLE 1

Cycle	Current Consumption
200 ns	7.84 $\mu A$
6.2 $\mu s$	0.57 $\mu A$

As described above, the inverter includes transistors 1a and 1d for switching, and transistors 1b and 1c for current limiting whose current conductance is determined in relation to the sizes of transistors 1a and 1d for switching. Since these transistors 1a-1d are connected in series between the power supply node and the ground node, the W and L sizes (in other words capacitance C) of transistors constituting inverter 2 which is to be a succeeding stage load can be reduced, and therefore current by charge/discharge at gate electrode can be reduced. As a result, current consumption can be reduced.

Transistors 1b and 1c limiting current are formed of a current mirror circuit, current flowing across gate electrodes can be controlled by voltage from circuit 6 constituting part of the current mirror circuit without reducing W/L (without increasing the size of gate length L).

Furthermore, since the other electrodes of transistors 1b and 1c for limiting current (drain electrodes) are used as the output node of an inverter, transistors 1b and 1c for limiting current will not be turned on unless transistors 1a and 1d for switching are completely turned on. Accordingly, time for a leading edge and a trailing edge of a waveform can be reduced even in a long cycle (6.2  $\mu s$ ), and therefore through current can be restrained.

FIG. 4 is a circuit diagram showing another embodiment of the invention. The ring oscillator in FIG. 4 is different from the ring oscillator in FIG. 1 in that a resistor 6d and an NMOS transistor 6e are additionally provided between one end of resistor 6a and the drain electrode of NMOS transistor 6c. Resistor 6a has a resistance value  $R_a$ , and resistor 6d has a resistance value  $R_b$ .

Now, operation will be described. When an input signal  $\phi$  attains an "H" level, N channel transistor 6e is turned on and the resistance value  $R_a$  of resistor 6a is reached. At the time, current  $i$  flowing through circuit 6 is  $i_1 = V/R_a$ . If input signal  $\phi$  attains an "L" level, N channel transistor 6e is turned off, the composite value  $R_a + R_b$  of resistors 6a and 6d is obtained, and current  $I$  flowing through circuit 6 is  $I_2 = V/(R_a + R_b)$ . Thus,

$i_1 > i_2$  holds,  $T_1 < T_2$  is established for the cycle, because  $i = C \cdot V / T$ .

More specifically, increase of the resistance decreases the current and prolongs the cycle, and therefore the cycle of the ring oscillator can be changed by selecting the values for the resistors in circuit 6 in response to input signal  $\phi$ .

Note that although in the embodiment shown in FIG. 4, N channel transistor 6e is used as a switch for selecting a resistance value, a P channel transistor controlled by an input signal  $\phi$  may be used.

FIG. 5 is a circuit diagram showing another embodiment of the invention. The ring oscillator shown in FIG. 5 is different from the ring oscillator shown in FIG. 1 in that the circuit constituting part of the current mirror circuit is formed of P channel transistors 6h and 6f and N channel transistors 6d and 6i. The structure of the other circuit portions is the same as the circuit shown in FIG. 1.

Circuit 6 shown in FIG. 1 decreases from power supply voltage  $V_{CC}$  by  $2 V_{TH}$  to attain an operation state. In contrast, circuit 6i shown in FIG. 5 decreases by a  $V_{TH}$  from power supply voltage  $V_{CC}$  to attain an operation state, and therefore a wide range for operation can be secured as compared to the first embodiment.

FIG. 6 is a circuit diagram showing a ring oscillator according to another embodiment of the invention. In the oscillator shown in FIG. 1, the drain side of transistors 1b and 1c for limiting current is connected to the output of the next stage, but in the ring oscillator shown in FIG. 6, the drain side of transistors 1a and 1d constituting the switching circuit is connected to the output of the next stage. Note that in FIG. 6 the drains of transistors 1a and 1d constituting a switching circuit function as a node 7 which is an output to the next stage.

FIG. 7 is a diagram showing a specific example of gate width/gate length when the ring oscillator shown in FIG. 6 is operated in an oscillation cycle; 200 ns, with a current consumption; 9.55  $\mu A$ .

FIG. 8 is a circuit diagram showing a ring oscillator according to yet another embodiment of the invention. In the ring oscillators shown in FIGS. 1, 4, 5, and 6, transistors 1b and 1c for limiting current are formed of a current mirror circuit, but in the ring oscillator shown in FIG. 8, the gate electrode of P channel transistor 1b is connected to GND, while the gate electrode of N channel transistors 1c is connected to power supply potential  $V_{CC}$ , so that constant resistance is always generated. Second to fifth stage inverters 21, 31, 41, and 51 have the same configuration as that of first stage inverter 11.

FIG. 9 is a view showing a specific example of gate width/gate length for each of transistors 1a-1d in the first stage of the ring oscillator shown in FIG. 8. In the inverter shown in FIG. 9, the W/L's of transistors 1b and 1c for limiting current are 4/200 and 2/200, respectively, and considerably large compared to the first to fourth embodiments. The ratios of gate width/gate length of switching circuits 1a and 1d are the same as the first to fourth embodiments. More specifically, in the fifth embodiment, the amount of current consumption can be reduced without changing the size of the switching circuit. For the size of each of transistor shown in FIG. 9, charge/discharge current is minimized in a cycle of 7.6  $\mu sec$ .

FIG. 10 is a circuit diagram showing a ring oscillator according to yet another embodiment of the invention.

The ring oscillator shown in FIG. 10 is different from the ring oscillator shown in FIG. 8 in that instead of connecting P channel transistors 1a, 1b, N channel transistors 1c, 1d in series between power supply node  $V_{CC}$  and ground node, P channel transistor 1b, P channel transistor 1a, N channel transistor 1b, and N channel transistor 1c are connected in the order between power supply node  $V_{CC}$  and ground node.

In operation, the ring oscillator shown in FIG. 10 cannot restrain through current as opposed to the inverter shown in FIG. 8, but performs the same operation as the ring oscillator shown in FIG. 8 for the other functions.

FIG. 11 is a diagram showing a specific example of the gate width/gate length of inverter 12 shown in FIG. 10.

As illustrated in FIG. 11, prolonging the gate lengths of transistors 1b and 1c for limiting current increases the resistance value between the drain electrodes of transistors 1a and 1d for switching, and therefore it will not be necessary to control transistors 1b and 1d for limiting current with the externally provided circuit 6 as in the first embodiment.

FIG. 12 is a block diagram showing a DRAM including a VBB generation circuit and a  $V_{pp}$  generation circuit.

Referring to FIG. 12, DRAM 100 includes a memory cell array 85 including a number of memory cells, an address buffer 81 receiving externally applied address signals A0 to An, a row decoder 82 and a column decoder 83 for addressing a row and a column in memory cell array 85 in response to a received address signal, and a sense amplifier 84 for amplifying a data signal read out from a memory cell. Input data Di is applied through a data in buffer 86. Output data Do is output through a data out buffer 87. DRAM 100 includes a clock signal generator 83 for generating a clock signal to control various circuits provided therein. DRAM 100 includes a VBB generation circuit 89 for generating a substrate bias voltage VBB, and a  $V_{pp}$  generation circuit 93 for generating voltage  $V_{pp}$  higher than power supply voltage  $V_{CC}$  when a word line is activated.

FIG. 13 is a block diagram showing VBB generation circuit 89. VBB generation circuit 89 includes a detector 89a, a short cycle ring oscillator 89b, a first charge pump circuit 89c, a long cycle ring oscillator 89d and a second charge pump circuit 89e. Detector 89a detects the output voltage of second charge pump circuit 89e decreasing below fixed voltage VBB (-2 V), and activates short cycle ring oscillator 89b. Short cycle ring oscillator 89b cascade-connects unit inverters 15-35 each including two switching transistors 1p and 1n. First charge pump circuit 89c responds to the output of short cycle ring oscillator 89b and generates voltage for biasing the substrate terminal to a negative voltage (-3 V) so that a transistor included in a memory cell is not activated.

Long cycle ring oscillator 89d cascade-connects inverters illustrated in the above-described first to sixth embodiments, and always oscillates in a fixed cycle. Short cycle ring oscillator 89b oscillates in a cycle of 200 ns, for example, while long cycle ring oscillator 89d has an oscillation cycle of 7.6  $\mu s$ .

Second charge pump circuit 89e responds to the output of long cycle ring oscillator 89d and generates voltage for biasing the substrate terminal to a negative potential (-3 V) as in the case of second charge pump

circuit 89c. The output node of second charge pump circuit 89e is connected together with the output node of first charge pump circuit 89c to the substrate terminal and detector 89a.

In operation, long cycle ring oscillator 89d is always activated. Second charge pump circuit 89e responds to the output of long cycle ring oscillator 89d and generates substrate bias voltage VBB. The oscillation cycle of long cycle ring oscillator 89d is set longer than the cycle of short cycle ring oscillator 89b, current consumption is reduced. Furthermore, since the structure shown in the first to sixth embodiments is implemented, current consumption is further reduced from the conventional long cycle ring oscillator (FIG. 18).

As in the foregoing, the VBB generation circuit shown in FIG. 13 can greatly reduce power consumption and therefore very much effective when used for generating backup voltage for a DRAM device.

FIG. 14 is a block diagram showing Vpp generation circuit 93 shown in FIG. 12. Vpp generation circuit 93 as in the case of VBB generation circuit 89 shown in FIG. 13 includes a detector 93a, a short cycle ring oscillator 93b, a first charge pump circuit 93c, a long cycle ring oscillator 93d, and a second charge pump circuit 93e. The Vpp generation circuit is different from the VBB generation circuit in that first and second charge pump circuits 93c and 93e generate positive voltage Vpp. The positive voltage Vpp is voltage for setting a word line WL to a slightly higher potential (5.8 V, for example) than power supply voltage Vcc during a writing cycle period. A row decoder 82 includes a multi-input NAND circuit 82a, PMOS transistors 82d, 82e, and 82f, and NMOS transistors 82b, 82c, and 82h. Row decoder 82 decodes a row address signal, and supplies constant potential Vpp generated from Vpp generation circuit 93 to word line WL.

In operation, an output signal in a long cycle is generated by long cycle ring oscillator 93d, and in response to the long cycle output signal, second charge pump circuit 93e generates positive voltage Vpp. When voltage Vpp decreases, detector 93a detects the decrease of voltage Vpp, and activates short cycle ring oscillator 93b. Thus, voltage generated by first charge pump circuit 93 is added to voltage Vpp generated by second charge pump circuit 93e, and the potential of word line WL rises.

As in the foregoing, the use of Vpp generation circuit 93 shown in FIG. 14 provides a constant voltage generation circuit with a reduced power consumption.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. Constant voltage generation circuit, comprising:

a first ring oscillator including a plurality of cascade-connected first inverters for generating a first signal in a first cycle;

first voltage generation means responsive to the first signal in the first cycle generated by said first ring oscillator for generating a first voltage;

detection means for detecting an amount by which an absolute magnitude of the first voltage is less than a prescribed absolute magnitude and generating a detection signal;

a second ring oscillator including a plurality of cascade-connected second inverters and responsive to the detection signal received from said detection means, for generating a second signal in a second cycle shorter than said first cycle by feeding back the output of a final stage inverter to a second stage inverter, each of said second inverters including (i) first and second transistors each having a channel sized to delay an output signal of a preceding stage inverter for a first time period corresponding to said second cycle and being turned on/off in a complementary manner in response to the output signal of said preceding stage inverter, and (ii) current limiting means having a mutual conductance whose size is selected corresponding to a resistance component for achieving said first time delay together with said input capacitance component for limiting current flowing from the power supply node and the ground node to said first and second transistors; and

second voltage generating means responsive to the second signal in the second cycle generated by said second ring oscillator for generating a second voltage.

2. Constant voltage generation circuit as recited in claim 1, wherein each said second inverter includes first and second transistors each channel of which is sized so as to have an input capacitance component and a resistance component for delaying the output signal of a preceding stage inverter for a second time period corresponding to said second cycle.

3. Constant voltage generation circuit as recited in claim 2, wherein

said first and second voltages are provided to a semiconductor substrate as a substrate bias voltage.

4. Constant voltage generation circuit as recited in claim 2, wherein

said constant voltage generation circuit is provided in as a semiconductor memory device, and said first and second voltages are provided to a word line driver circuit.

5. Constant voltage generation circuit, comprising:

a first ring oscillator including a plurality of cascade-connected first inverters for generating a first signal in a first cycle;

first voltage generation means responsive to the first signal in the first cycle generated by said first ring oscillator for generating a first voltage;

detection means for detecting an amount by which an absolute magnitude of the first voltage is less than a prescribed absolute magnitude and generating a detection signal;

a second ring oscillator including a plurality of cascade-connected second inverters and responsive to the detection signal received from said detection means, for generating a second signal in a second cycle shorter than said first cycle by feeding back an output of a final stage inverter to a first stage inverter, each of said second inverters including (i) first and second transistors each having a channel sized to delaying an output signal of a preceding stage inverter for a first time period corresponding to said first cycle, and being turned on/off in a complementary manner in response to the output signal of said preceding stage inverter, (ii) a third transistor having an ON resistance value corresponding to a resistance component for achieving a first time delay together with said input capaci-

11

tance component for limiting current flowing from  
a power supply node to said first transistor, and (iii)  
a fourth transistor having an ON resistance value 5  
corresponding to said resistance component for

12

limiting current flowing from said second transis-  
tor to the ground node; and  
second voltage generating means responsive to the  
second signal in the second cycle generated by said  
second ring oscillator for generating a second volt-  
age.

\* \* \* \* \*

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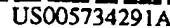
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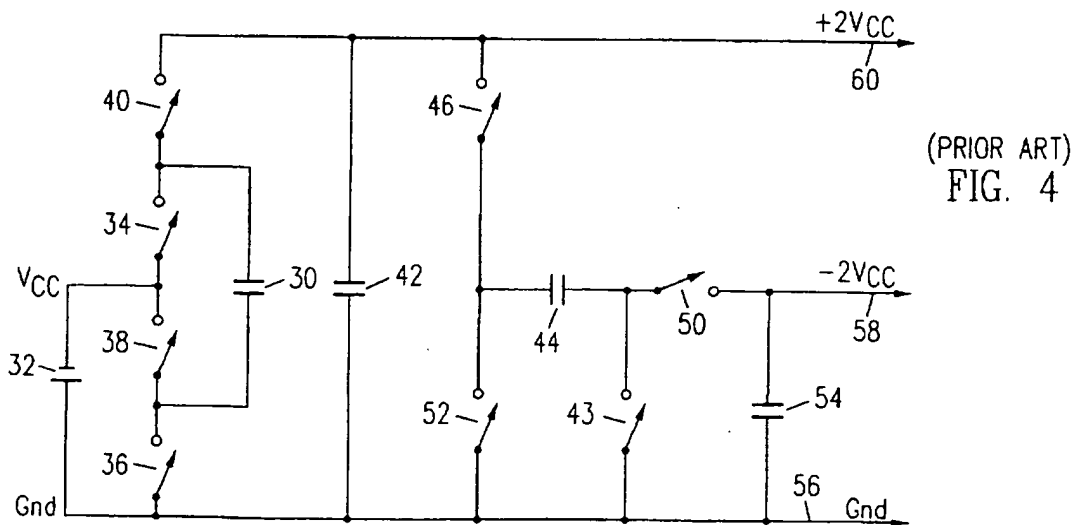
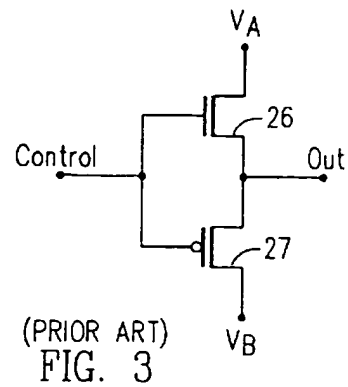
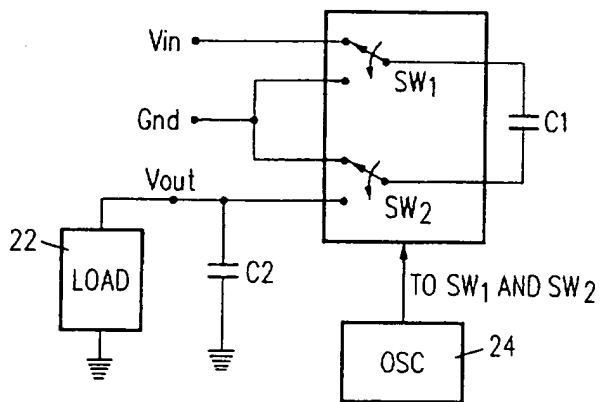
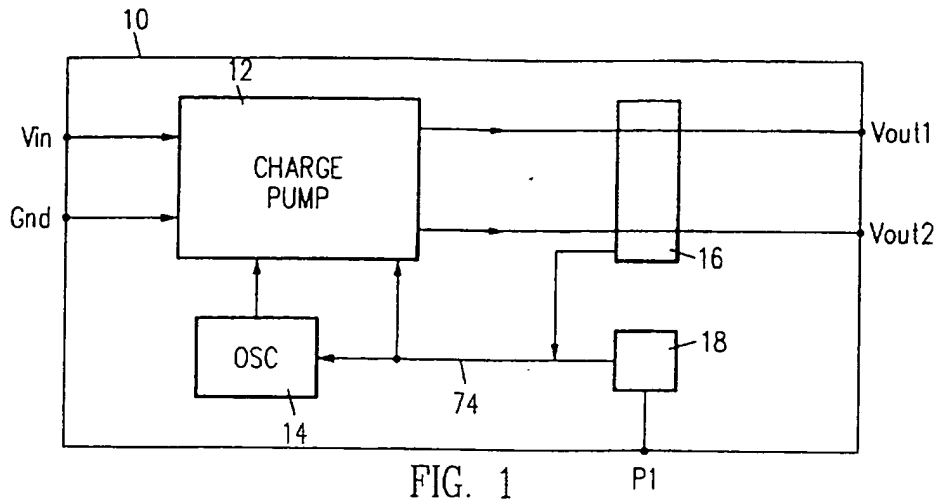


## Tasdighi et al.

[45] **Date of Patent:** Mar. 31, 1998

- "MAXIM, +5v rs-232 Transceivers With 0.1 $\mu$ F External Capacitors MAX200-MAX211/MAX213". data sheet published by Maxim Integrated Products. Sunnyvale, CA. Jan. 93. pp. 2-5.

An integrated circuit voltage converter containing a capacitive charge pump performing DC to DC conversion is disclosed which detects, either automatically or by an external signal, the onset of a low power consumption situation and switches to a low power consumption mode. In one embodiment, the low power consumption mode is accomplished by reducing the operating frequency of the charge pump. In another embodiment, the switching transistors used to switch the capacitors in the charge pump during a low power consumption mode are smaller than those transistors used to switch the capacitors during its normal operating mode. In another embodiment, the DC to DC converter switches back and forth between a high frequency (burst) mode and a low frequency (low power) mode at intervals. In another embodiment, a combination of the power reduction techniques is used. Various techniques for detecting when a low power consumption mode is appropriate are also described.



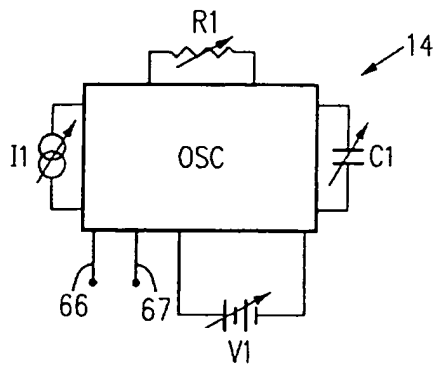


FIG. 5

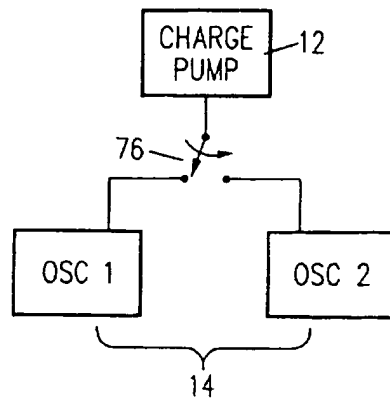


FIG. 6

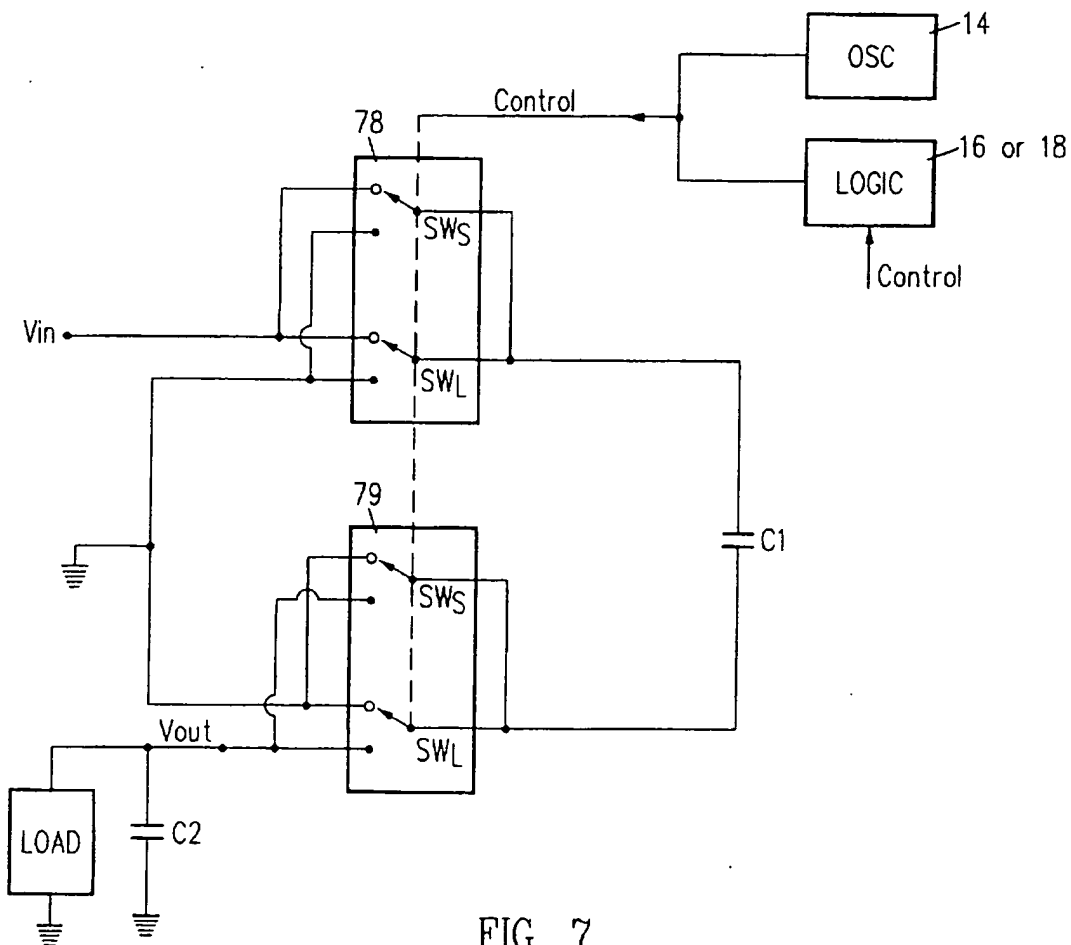


FIG. 7



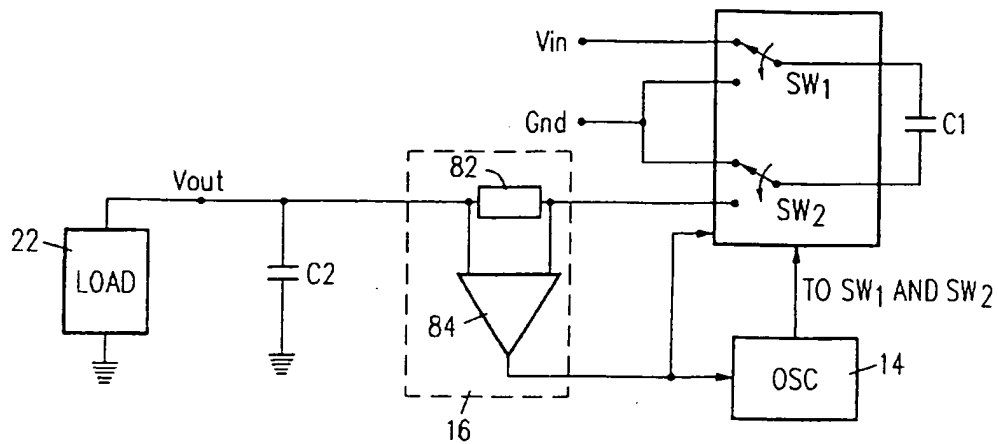


FIG. 8

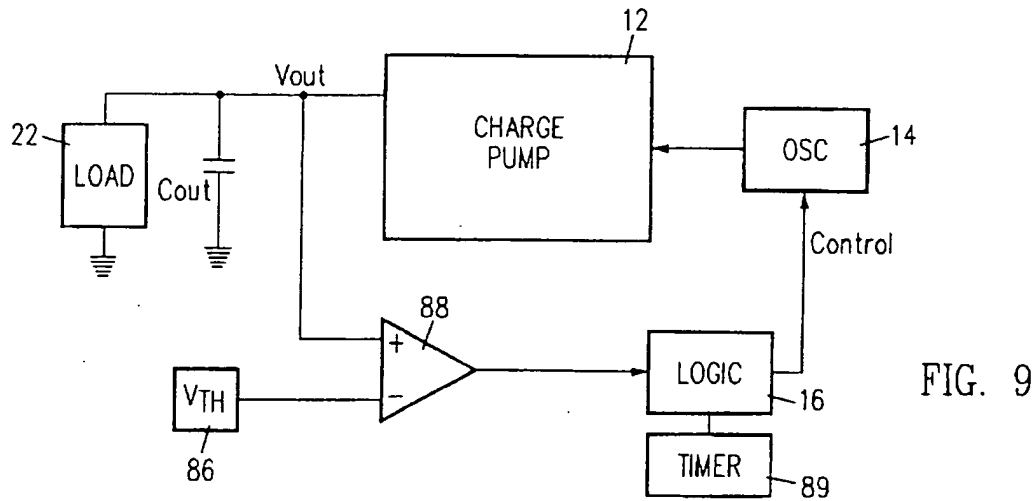


FIG. 9

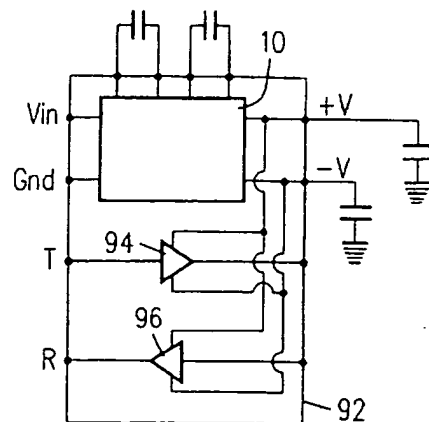


FIG. 10

## POWER SAVING TECHNIQUE FOR BATTERY POWERED DEVICES

### FIELD OF THE INVENTION

This invention relates to battery powered electronic devices and, more particularly, to a DC to DC converter having a low power consumption mode.

### BACKGROUND OF THE INVENTION

Converters which convert a DC battery voltage to a different DC voltage for connection to circuitry within a device, such as a laptop computer or a portable telephone, are commonly used. The prolonging of battery life is a constant challenge to the designers of such devices.

In such a device powered by a battery connected to a DC to DC converter, battery current is consumed by both the converter and the circuitry connected to the converted voltage. Frequently, the circuitry powered by the converted voltage can be operated in a low-power standby mode, whereby the circuitry is controlled in some fashion to consume low power. Such a standby mode is used in portable telephones while not actively transmitting or receiving and used in laptop computers after a period of nonuse. However, it is common that the voltage converter in these devices continues to operate in its normal fashion and thus still uses considerable power during its operation. Such power consumption in a switching type charge pump is primarily due to the switching transistors' parasitic capacitance charging and discharging at the operating frequency of the converter.

Even during a no-load condition, where the load is disconnected from the charge pump, it is often not desirable to completely shut down the charge pump circuitry due to the relatively long start-up time for the converter to provide a steady state voltage.

What is needed is an integrated DC to DC converter containing a charge pump, where the converter has a low power consumption mode while still providing a converted voltage at its output.

### SUMMARY

An integrated circuit voltage converter containing a charge pump performing DC to DC conversion is disclosed which detects, either automatically or by an external signal, the onset of a low power consumption situation and switches to a low power consumption mode.

In one embodiment, the low power consumption mode is accomplished by reducing the operating frequency of the charge pump. In another embodiment, the switching transistors used to switch the capacitors in the charge pump during a low power consumption mode are smaller than those transistors used to switch the capacitors during its normal operating mode. This may be accomplished by switching fewer transistors in parallel in the low power consumption mode. In another embodiment, a combination of the two power reduction techniques is used.

Various techniques for detecting when a low power consumption mode is appropriate are also described.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of one embodiment of the DC to DC converter having a low power consumption mode.

FIG. 2 is a schematic diagram of a known charge pump circuit for generating a negative voltage.

FIG. 3 is a conventional CMOS circuit for outputting one of two voltages.

FIG. 4 is a schematic diagram of a known charge pump providing a positive and negative output voltage at double the battery voltage.

FIG. 5 is a diagram of an oscillator whose frequency may be adjusted by changing any one of a number of parameters.

FIG. 6 is a block diagram illustrating the switching between a high frequency and a low frequency oscillator.

FIG. 7 illustrates a transistor switch which may be used as a transistor switch in the charge pump of FIG. 2 which, in one setting, operates in a normal operating mode and, in another setting, operates in a low power consumption mode.

FIG. 8 is a schematic diagram of a DC to DC converter illustrating automatic detection circuitry which triggers the onset of a low power consumption mode of the converter.

FIG. 9 illustrates another embodiment of the converter which automatically selects either a normal operating mode or the low power consumption mode depending on whether the output voltage is below a threshold voltage.

FIG. 10 is a block diagram of an integrated circuit incorporating the novel converter and transmit/receive buffers for use as an RS-232 transceiver.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a block diagram illustrating one embodiment of the invention. In the preferred embodiment, the DC to DC converter 10 is formed as a packaged integrated circuit. The number of pins will depend upon the particular application of the converter. For example, if converter 10 were intended for use in an RS-232 interface application, a separate voltage output pin may be provided for +V and -V. If the capacitors needed in converter 10 were sufficiently large and could not be formed on-chip, then converter 10 would include pins for connection to external capacitors. Such a resulting converter 10 using external capacitors would still be classified as a single chip converter for purposes of this disclosure. Additionally, a battery voltage  $V_{IN}$  pin and a battery ground pin are provided on the package. In one embodiment, a low power consumption signal pin P1 is also provided on the package.

If the package contained additional circuitry powered by the battery or the converter 10, additional pins may also be needed. Such a package containing converter 10 and additional circuitry may be used as an RS-232 transceiver. The additional circuitry may include buffers which receive an input signal and output the charge pump voltage at an output terminal of the package as illustrated in FIG. 10, to be described later.

The converter 10 of FIG. 1 contains a charge pump 12 whose basic switching operation may be conventional. Examples of two charge pumps are described with respect to FIGS. 2 and 4.

An oscillator 14, whose frequency can be changed in one embodiment, is connected to the charge pump 12 and controls the switching transistors within charge pump 12.

A first detection and logic circuit 16 is shown coupled to the outputs of charge pump 12 to either detect the current being provided by converter 10 or to detect the output voltage of converter 10. Upon detection of a low power consumption condition, logic circuit 16 either controls the switching transistors in charge pump 12 to operate in a low power consumption mode and/or lowers the switching frequency of oscillator 14, as described in greater detail later.

A second detection and logic circuit 18 has a control input connected to an external pin P1 of converter 10. A predetermined logic level signal is applied to pin P1 to signal that converter 10 should be placed into a low power consumption mode. Logic circuit 18 then either controls the switching transistors in charge pump 12 to operate in a low power consumption mode or lowers the switching frequency of oscillator 14. Either or both of logic circuits 16 and 18 may be used while still achieving the purpose of this invention.

FIG. 2 is a prior art charge pump whose basic circuitry may be used in charge pump 12 in FIG. 1. The charge pump of FIG. 2 generates an output voltage  $V_{OUT}$  which is a negative of the input battery voltage  $V_{IN}$ . An external load 22 is powered by the  $-V_{IN}$  voltage.

An oscillator 24 operating at virtually any operating frequency, such as 15 KHz to 100 KHz, produces a train of pulses which are applied to control terminals of switching transistors SW1 and SW2. The switching transistors described in this disclosure may be MOS or bipolar transistors. The operation of the charge pump of FIG. 2 is as follows. In a first switch position, illustrated in FIG. 2, capacitor C1 is charged to voltage  $V_{IN}$  with its upper terminal connected to  $V_{IN}$  and its lower terminal coupled to ground. In a next switching position, under control of oscillator 24, the top terminal of capacitor C1 is connected to ground, and the bottom terminal of capacitor C1 is connected to the top terminal of capacitor C2. The bottom terminal of capacitor C2 is connected to ground. Since the top terminal of capacitor C1 is connected to ground and capacitor C1 is charged to  $V_{IN}$ , the bottom terminal of capacitor C1 is at a voltage of  $-V_{IN}$  and, thus, capacitor C2 becomes charged to this voltage. Capacitor C2 now provides the relatively constant voltage of  $-V_{IN}$  to the load 22. Switching transistors SW1 and SW2 are cycled at the frequency of oscillator 24 so that the charge in capacitor C2 is repeatedly replenished as current is drawn by load 22.

Switches SW1 and SW2 may each be a conventional CMOS inverter as shown in FIG. 3, comprising an NMOS transistor 26 and a PMOS transistor 27. As the oscillator 24 voltage applied to the gates of transistors 26 and 27 alternates between a high and low voltage, transistors 26 and 27 couple either a  $V_A$  voltage or a  $V_B$  voltage to the output of the CMOS circuit.

FIG. 4 illustrates a charge pump circuit which is the subject of U.S. Pat. No. 4,897,774, assigned to Maxim Integrated Products, incorporated herein by reference. The charge pump of FIG. 4 is useful in an RS-232 receiver and transmitter which requires both a positive voltage and a negative voltage to be generated. Referring first to the positive voltage doubler portion of the circuit of FIG. 4, transfer capacitor 30 is charged from voltage source 32 (having a value  $V_{cc}$ ) by closing switches 34 and 36 while switches 38 and 40 remain open during a first phase. During a second phase, switches 34 and 36 are opened and switches 38 and 40 are closed.

When switches 38 and 40 are closed during the second phase, the voltage source 32 is effectively placed in series with the voltage stored across the transfer capacitor 30 and thus the sum of the voltage across voltage source 32 and capacitor 30 is placed across reservoir capacitor 42.

The inverting portion of the voltage doubler circuit operates as follows. Transfer capacitor 44 is charged to the voltage across reservoir capacitor 42 via the switches 46 and 43, which are closed during the first phase of operation of the circuit while switches 50 and 52 remain open. During the second phase of circuit operation, switches 46 and 43 are

opened, and the voltage across transfer capacitor 44 is placed across reservoir capacitor 54 via the closing of switches 50 and 52. When the voltage across transfer capacitor 44 is placed across reservoir capacitor 54, the positive end of transfer capacitor 44 is connected to ground line 56 through switch 52, and the negative end of capacitor 44 is connected to the side of reservoir capacitor 54 connected to  $-2V_{cc}$  output line 58. The polarity of the voltage across reservoir capacitor 54 with respect to ground line 56 is such that the voltage across reservoir capacitor 54 is negative. The output of reservoir capacitor 42 is connected to  $+2V_{cc}$  output line 60.

The first and second phases of the circuit operation described above are repeated at a typical frequency which may range from approximately 100 Hz to greater than 100 KHz for a metal gate 10 volt charge pump device.

In the charge pumps of FIGS. 2 and 4, it takes several phase cycles before the desired output voltage is achieved.

The anticipated load connected to the outputs of the charge pumps of FIGS. 2 and 4 affects the design of the charge pump in that larger capacitors may be used to provide a higher current to the load. Such capacitors may be connected external to the integrated circuit converter 10. Higher switching frequencies also supply a higher current to the load.

In the present invention, the charge pumps of FIGS. 2 and 4, as well as any other conventional charge pump, may generally be used as charge pump 12 in FIG. 1, as modified by the teachings herein to allow the charge pump to be operated in both a normal operating mode and a low power consumption mode. FIGS. 5-9 illustrate modifications to the conventional charge pumps which enable these charge pumps to operate in either a normal operating mode or a low power consumption mode.

FIG. 5 illustrates an oscillator circuit 14 which can be used in FIG. 1. Oscillator 14 may use conventional techniques to generate an oscillating frequency across terminals 66 and 67. One skilled in the art would understand the numerous varieties of oscillators which may be used in this invention. In conventional oscillators, the frequency of oscillation can be changed by changing the value of a resistor, a capacitor, a current source, a voltage source, or a combination of these components of the oscillator. In oscillators which use an RC feedback path to control the frequency of oscillation, the frequency is related to  $1/RC$ .

In FIG. 5, the output frequency of oscillator 14 may be lowered by changing the value of either capacitance C1, resistor R1, current source I1, or voltage source V1. These parameter values can be changed by making any one of the components variable or by placing additional components in parallel or in series with the components shown in FIG. 5. It should be understood that changing any parameter of oscillator 14 to adjust the oscillator frequency is envisioned for this invention.

Any one of the parameters in oscillator 14 is controllable by a control signal, as shown in FIG. 1 on line 74, which is generated by either logic circuit 16 or logic circuit 18. The parameters are controlled to place oscillator 14 in a low frequency mode when logic circuit 16 or logic circuit 18 detects that a low power consumption mode for the DC to DC converter 10 should be initiated. The reduction in the oscillator frequency reduces the switching frequency of all the switching transistors in charge pump 12, such as those switching transistors in the charge pumps of FIGS. 2 and 4. Hence, the frequency of the charging and discharging of the parasitic capacitances in the various switching transistors is

reduced. This reduces the power consumption of the charge pump 12, but also reduces the amount of current the charge pump 12 can deliver to a load.

In one embodiment, the control signal on line 74 controls oscillator 14 to reduce its output frequency to 1/100 the normal operating frequency of the oscillator; however, other ratios are also suitable, depending on the expected load during the low power mode. The low power frequency and normal operating frequency should be set depending on the particular application. In one embodiment, the frequency of oscillator 14 is switched from a frequency of 10 KHz-100 KHz in the normal mode to 100 Hz to 1 KHz in the low power consumption mode.

In another embodiment of oscillator 14, shown in FIG. 6, two oscillators, OSC1 and OSC2, are used, and the control signal on line 74 controls a switch 76 which connects the charge pump 12 switching transistors to either the high frequency signals provided by OSC1 (for the normal operating mode) or the low frequency signals generated by OSC2 (for the low power consumption mode).

Oscillator 14 could be a ring oscillator or any other known form of oscillator. If oscillator 14 were a ring oscillator, one or more inverters in the ring would be bypassed for high frequency operation.

Techniques to detect whether a low power consumption mode should be initiated are described later.

Another method to reduce the power consumption of charge pump 12 is to lower the effective capacitances of one or more of the switches used within charge pump 12. This is illustrated in FIG. 7. FIG. 7 depicts switches 78 and 79 which may substitute for switches  $SW_L$  and  $SW_S$ , respectively, in the charge pump of FIG. 2 or in any conventional charge pump. Switches 78 and 79 consist of a large switching transistor  $SW_L$  and a small switching transistor  $SW_S$ , where the larger transistor has a parasitic capacitance which is larger than that of the smaller transistor. Thus, the larger transistor draws more current from the battery than the small transistor when their respective gates are charged, assuming the transistors are MOS transistors. Switches  $SW_L$  and  $SW_S$  may also be bipolar transistors whose parasitic capacitances are also related to their sizes.

In a normal operating mode, both switches  $SW_S$  and  $SW_L$  are operated in parallel to connect the terminals of capacitor C1 to either  $V_{IN}/\text{ground}$  or  $\text{ground}/V_{OUT}$ .

When a low power consumption mode is initiated, logic circuit 16 or 18 in FIG. 1 disconnects the control terminal of switch  $SW_L$  from the oscillator 14, or otherwise disables switch  $SW_L$ , to cause switch  $SW_L$  to act as an open circuit. The switch  $SW_L$  may be disabled by a switch connected between the control terminal of switch  $SW_L$  and oscillator 14 or by any other suitable technique. If switch  $SW_L$  is normally closed, then logic circuit 16 or 18 would also act to disconnect switch  $SW_L$  from the circuit so that only the smaller switch  $SW_S$  operates to couple the terminals of capacitor C1 to the proper nodes. In one embodiment, the larger switches  $SW_L$  are 10 to 20 times greater in size (channel width) than the smaller switches  $SW_S$ ; however, other ratios would also be suitable. In one embodiment, the larger switches  $SW_L$  have a channel width of 6000 microns and a channel length of 6 microns, for PMOS switches, and a width of 3000 microns and a length of 6 microns for the NMOS switches. Many factors determine the preferred size of the transistors for a particular application, such as:

Technology choice:  $L_{min}=5\mu$  for high voltage CMOS vs.

$L_{min}=1\mu$  mid-voltage CMOS;

Voltage requirement: e.g., 10 volt vs. 25 volt;

Output reservoir capacitors: e.g., 0.1  $\mu\text{F}$  vs. 10  $\mu\text{F}$ .

In another embodiment, switches  $SW_L$  and  $SW_S$  do not operate in parallel but operate in an either/or configuration where only one or the other is used to couple the voltage to the top terminal of capacitor C1. This may be accomplished by placing another switch in series between the oscillator 14 and the control terminal of switch  $SW_S$  to selectively disable either switch  $SW_L$  or  $SW_S$ .

FIG. 8 illustrates one construction of logic circuit 16 which automatically detects a low output current being drawn by load 22 connected to one output of the converter 10 of FIG. 1. An impedance 82, such as a resistor, is connected in series between the load 22 and charge pump 12 such that the current drawn by load 22 flows through the impedance 82. Impedance 82 may instead be on the left side of capacitor C2 but would then be outside of the integrated circuit and require extra pins.

A comparator 84 senses if the differential across the terminals of impedance 82 is below a threshold level, indicating that the current through impedance 82 is low enough to allow the charge pump 12 to provide the required power to load 22 even in the low power consumption mode. The logic state then output by comparator 84 is applied to oscillator 14 to lower the frequency of oscillator 14, as previously described with respect to FIGS. 5 and 6, or applied to charge pump 12 to cause the switching transistors to be in their low power consumption mode, as previously described with respect to FIG. 7. Various other logic circuits are envisioned which detect a current through impedance 82 and generate a predetermined logic signal if this current is below a threshold amount.

Logic circuit 18 in FIG. 1 may be a simple circuit which receives a predetermined voltage at terminal P1 and converts this signal, if necessary, to the appropriate logic level on control line 74 to cause oscillator 14 to be operated at a low frequency or to cause the switching transistors in charge pump 12 to be in their low power consumption mode. In one embodiment, logic circuit 18 may be eliminated, and the control signal to oscillator 14 or charge pump 12 may be obtained directly from terminal P1.

FIG. 9 illustrates another embodiment of the invention where the output voltage  $V_{OUT}$  across the output capacitor  $C_{OUT}$  is sensed and compared to a threshold voltage 86 by a comparator 88. If the output voltage is above or at the threshold voltage, indicating that the charge pump 12 is providing the required current to the load 22, the output of comparator 88 provides a logic level to logic circuit 16 signifying that a low power consumption mode may be appropriate. After any predetermined time delay (including zero delay) provided by timer 89, logic circuit 16 then controls oscillator 14 to decrease its frequency or controls the switching transistors in charge pump 12 to be in their low power consumption mode.

If the current provided by charge pump 12 is insufficient to power load 22, the output voltage  $V_{OUT}$  will become lower than the threshold voltage 86, and comparator 88 will signal logic circuit 16 to place oscillator 14 or charge pump 12 in its normal operating mode. Converting to the normal operating mode will then raise the output voltage  $V_{OUT}$  above the threshold voltage, and the necessary current will be provided to the load 22. After a predetermined amount of time, such as zero to one millisecond, depending on the application requirement as well as loading and supply conditions, logic circuit 16 will then automatically cause converter 10 to operate in its low power consumption mode. The cycling between the normal operating mode and the low power consumption mode then continues.

The threshold voltage may be obtained from any node in charge pump 12 which is related to the output voltage. A divider circuit may be inserted between  $V_{OUT}$  and comparator 88 to divide  $V_{OUT}$  into a suitable range for comparison with the threshold voltage.

In one embodiment, the oscillating frequency provided by oscillator 14 is continuously variable to cause the output voltage to just meet the threshold voltage.

The circuit of FIG. 9 operating in the normal operating mode for a predetermined time may be referred to as a burst mode of operation. Generally, it is envisioned that this burst mode will be operated for a relatively short time compared to the low power consumption mode.

In another embodiment, the time delay incurred before logic circuit 16 switches to a low power consumption mode is variable and is based on the time it takes for the output voltage to fall below the threshold voltage when converter 10 is in the low power consumption mode. If the time span is short, indicating that load 22 is drawing a relatively high current, then the time delay between cyclings between modes can be increased.

The techniques described herein can reduce the operating current of converter 10 significantly, such as by greater than 99%. For a typical converter, the normal operating current may be 1 mA to 10 mA, while the low power consumption operating current may be as low as 5  $\mu$ A to 50  $\mu$ A.

In an alternative embodiment, a reduced power consumption mode and a low power consumption mode are made available to converter 10, depending on the load requirements, by using an oscillator with multiple selectable frequencies (e.g., three or more) or by using switching transistors with multiple selectable power consumption modes (e.g., three or more).

FIG. 10 is a block diagram of a packaged integrated circuit 92 containing converter 10 of FIG. 1 as well as buffers 94 and 96. Buffers 94 and 96 receive an input signal on transmit pin T and receive pin R and output a voltage +V or -V on output pins of the integrated circuit 92. The various transfer and reservoir capacitors used by converter 10 are shown external to package 92. The various circuits described in FIGS. 1-9 or a combination of such circuits may be incorporated into converter 10 to provide both a normal operating mode and a low power consumption mode. The circuit of FIG. 10 may be used as an RS-232 family of transceivers.

Accordingly, various embodiments of an integrated circuit DC to DC converter having a low power consumption mode have been described. The low power consumption mode may be initiated automatically or by an externally generated signal. Such automatic detection or externally generated signal may designate a low power consumption mode, a complete shut down mode, or other mode.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

What is claimed is:

1. An integrated single-chip circuit comprising:

a switching charge pump which receives a first voltage from a power supply and outputs a second voltage different from said first voltage, said charge pump incorporating switching transistors which draw an operating current from said power supply;

an oscillator connected to said switching transistors within said charge pump for controlling an operating frequency of said charge pump; and

a low power consumption detection circuit for detecting when a low power consumption mode of said charge pump is appropriate and, in response to such detecting, for causing said switching transistors in said charge pump to draw less current from said power supply, said low power consumption detection circuit comprising: an impedance in series between a load and a terminal of said charge pump, wherein a current through said load is reflected by a current through said impedance; and a detector for determining a voltage drop across said impedance and for generating a signal reflecting whether a current into said load is below a threshold current.

2. The circuit of claim 1 wherein said low power consumption detection circuit receives a first signal and causes an operating frequency of said charge pump to be lowered.

3. The circuit of claim 1 wherein said low power consumption detection circuit is connected to said charge pump and controls said switching transistors within said charge pump to have a lower effective capacitance so as to draw less current from said power supply during each switching cycle of said charge pump.

4. The circuit of claim 3 wherein said charge pump comprises two or more capacitors controllably connected together by said switching transistors operating at the operating frequency of said charge pump, wherein one or more of said switching transistors comprise:

a first switching transistor and a second switching transistor connected in parallel during a normal operating mode and not connected in parallel during said low power consumption mode, said first switching transistor being larger than said second switching transistor.

5. The circuit of claim 3 wherein said charge pump comprises two or more capacitors controllably connected together by said switching transistors operating at the operating frequency of said charge pump, wherein one or more of said switching transistors comprise:

a first transistor and a second transistor, said first switching transistor being larger than said second switching transistor, said first switching transistor being enabled when providing a switching function at said operating frequency in a normal mode of said charge pump, said second switching transistor being enabled, while said first switching transistor is disabled, for providing a switching function at said operating frequency during said low power consumption mode of said charge pump.

6. The circuit of claim 1 wherein said charge pump comprises two or more capacitors controllably connected together by said switching transistors operating at said operating frequency of said charge pump, wherein said two or more capacitors are connected external to an integrated circuit package housing said switching transistors.

7. The circuit of claim 1 wherein said low power consumption detection circuit receives a first signal and causes an operating frequency of said charge pump to be lowered to less than one tenth of the operating frequency of said charge pump during a normal mode of said charge pump.

8. The circuit of claim 7 wherein said low power consumption detection circuit also receives a second signal and causes said operating frequency of said charge pump to be lowered to a frequency lower than said operating frequency during said low power consumption mode.

9. The circuit of claim 1 wherein said low power consumption detection circuit receives a first signal and causes an operating frequency of said charge pump to be lowered

to less than one hundredth of the operating frequency of said charge pump during a normal mode of said charge pump.

10. The circuit of claim 1 wherein said switching transistors are MOS transistors.

11. The circuit of claim 1 wherein causing said switching transistors in said charge pump to draw less current from said power supply comprises lowering said operating frequency of said charge pump.

12. The circuit of claim 1 further comprising one or more buffers on the same integrated circuit chip as said charge pump, said one or more buffers being powered by an output voltage of said charge pump, said one or more buffers having an input pin and an output pin extending from an integrated circuit package housing said charge pump.

13. The circuit of claim 12 wherein said circuit is configured as an RS-232 transceiver.

14. The circuit of claim 1 wherein said oscillator comprises two or more oscillators, each of said oscillators generating a different frequency.

15. The circuit of claim 1 wherein said low power consumption detection circuit comprises:

a comparator for comparing a first voltage representative of an output voltage of said charge pump with a threshold voltage and, upon detection of said first voltage being greater than said threshold voltage, controlling said switching transistors in said charge pump to draw less current from said power supply.

16. The circuit of claim 15 further comprising a timer for causing said charge pump to be switched into said low power consumption mode after a period of time after said first voltage is detected as being above said threshold voltage.

17. The circuit of claim 16 where said period of time is based on a time it takes for said first voltage to fall below said threshold voltage when said charge pump is in said low power consumption mode.

18. A method for lowering the power consumption of a switching type charge pump comprising the steps of:

receiving a voltage from a power supply into said charge pump;

detecting the onset of a low power consumption mode by passing current flowing from said charge pump into a load through an impedance in series between said load and a terminal of said charge pump, wherein the current through said load is reflected by the current through said impedance, determining a voltage drop across said impedance and generating a signal reflecting whether said current into said load is below a threshold current; controlling an oscillator to output an operating frequency in response to said detecting;

driving switching transistors within said charge pump with said operating frequency; and

causing said switching transistors within said charge pump to draw less current from said power supply connected to said charge pump by changing said operating frequency of said oscillator.

19. The method of claim 18 wherein said step of causing said switching transistors within said charge pump to draw less current from said power supply comprises of the step of: lowering an operating frequency of said switching transistors.

20. The method of claim 19 wherein said step of lowering said operating frequency of said switching transistors comprises the step of reducing said operating frequency of said switching transistors to less than one-tenth the operating frequency in a normal mode of operation to place said charge pump in said low power consumption mode.

21. The method of claim 18 wherein said switching transistors comprise first type switching transistors and second type switching transistors, said first type being larger than said second type, and wherein said step of causing said switching transistors within said charge pump to draw less current from said power supply comprises the step of disabling said first type switching transistors in said charge pump while allowing said second type switching transistors in said charge pump to controllably connect together two or more capacitors in said charge pump for generating a charge pump output voltage.

\* \* \* \* \*



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Yokomizo et al.

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(54) **DC/DC CONVERTER**

(75) Inventors: **Ichiro Yokomizo; Sachito Horiuchi; Mayuka Matsumae**, all of Kyoto (JP)

(73) Assignee: **Rohm Co., Ltd.**, Kyoto (JP)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(52) U.S. Cl. .... **327/536; 330/297**

(58) Field of Search ..... **363/60; 327/536; 330/297, 202**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

6,011,440 A \* 1/2000 Bell et al. .... 330/202  
6,107,862 A \* 8/2000 Mukainakano et al. .... 327/536

\* cited by examiner

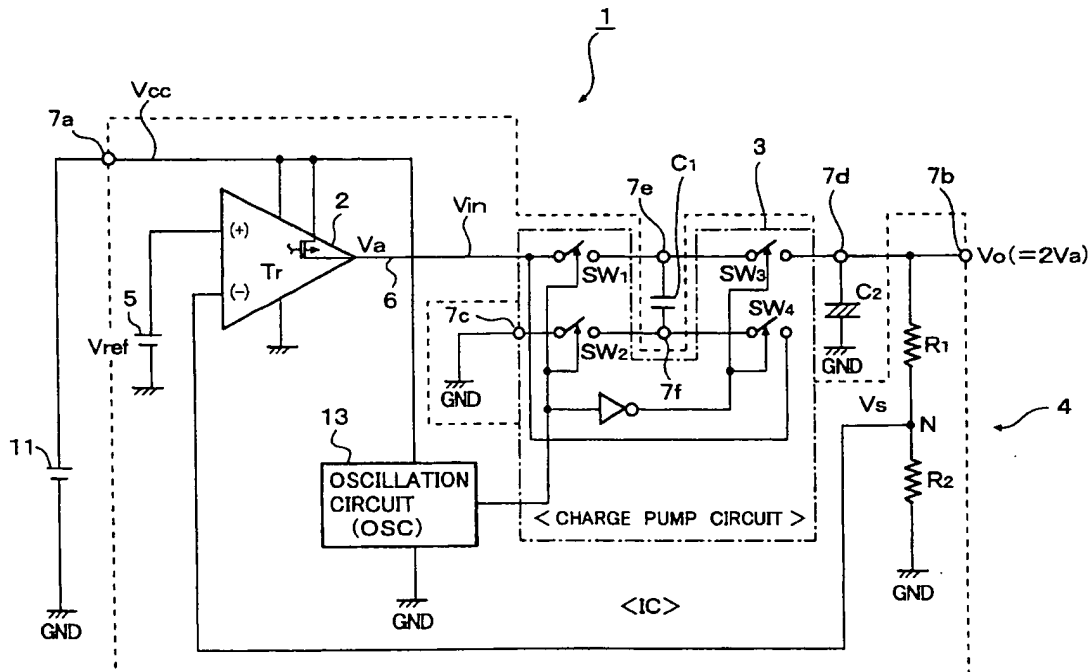
Primary Examiner—Shawn Riley

(74) Attorney, Agent, or Firm—Mattingly, Stanger & Malur, P.C.

(57) **ABSTRACT**

A DC/DC converter is provided with a DC power source; a reference voltage generating circuit; an amplifier which receives an electric power from the DC power source and outputs an electric power of which voltage is controlled so as to assume a target voltage value by stepping down the voltage of the electric power from the DC power source depending on a difference between the reference voltage and a detection voltage; an oscillation circuit which generates signals having a specific frequency; a voltage boosting circuit which receives the output of the amplifier and the output of the oscillation circuit, causes switching of the output of the amplifier at the specific frequency to charge a first capacitor, and performs voltage boosting by transferring the electric charges-charged in the first capacitor through complementary ON/OFF switching with respect to the former switching into a second capacitor after raising substantially upto  $n/m$  time voltage (wherein  $n > m$  and  $n$  and  $m$  are integers equal to or more than 2) and charging the same therewith; and an output voltage detection circuit which generates the detection voltage depending on the output voltage of the boosting circuit, whereby a voltage of substantially  $n/m$  times of the target voltage value is generated from the voltage boosting circuit.

15 Claims, 5 Drawing Sheets



**FIG. 1**

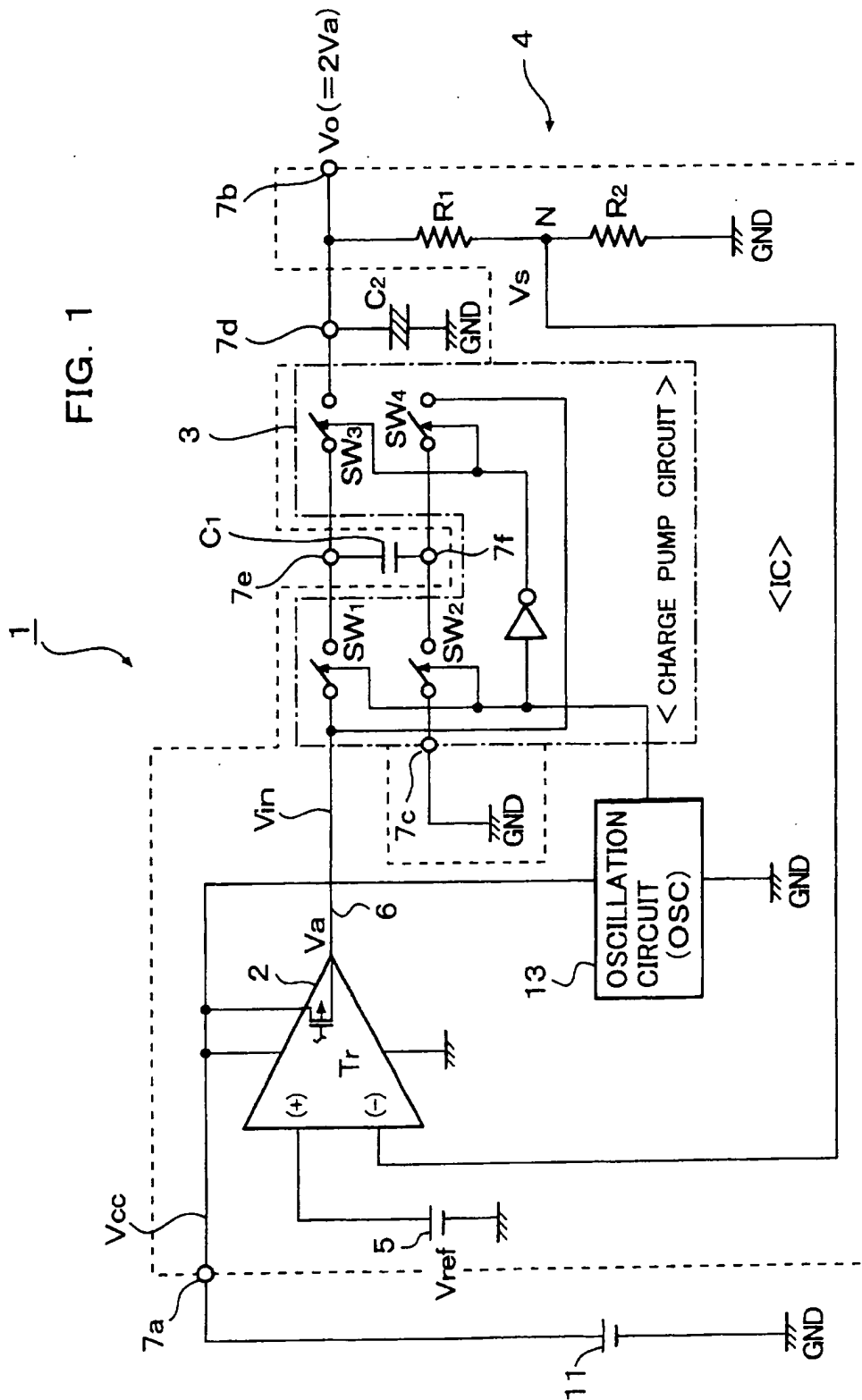




FIG. 2

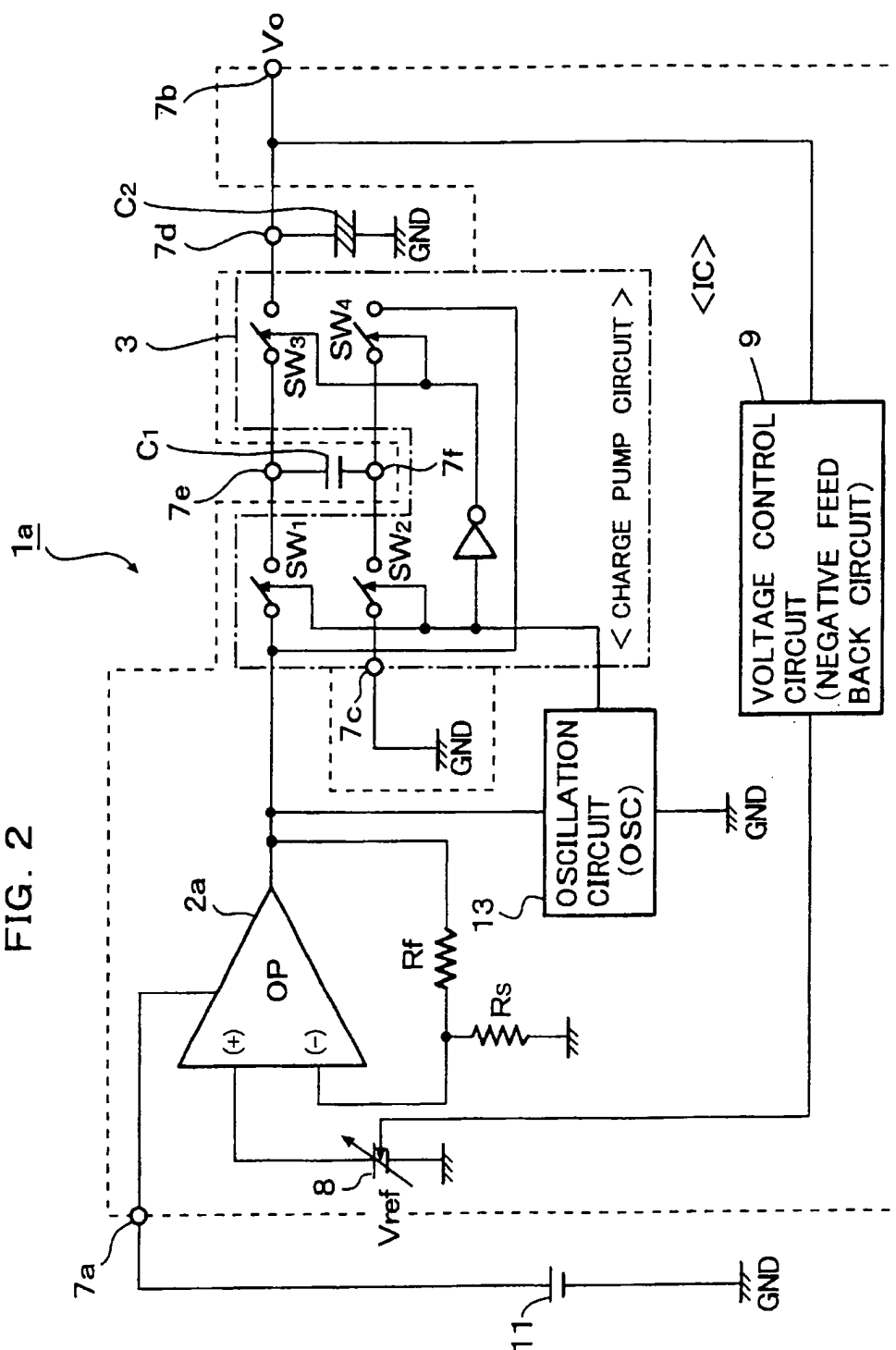


FIG. 3

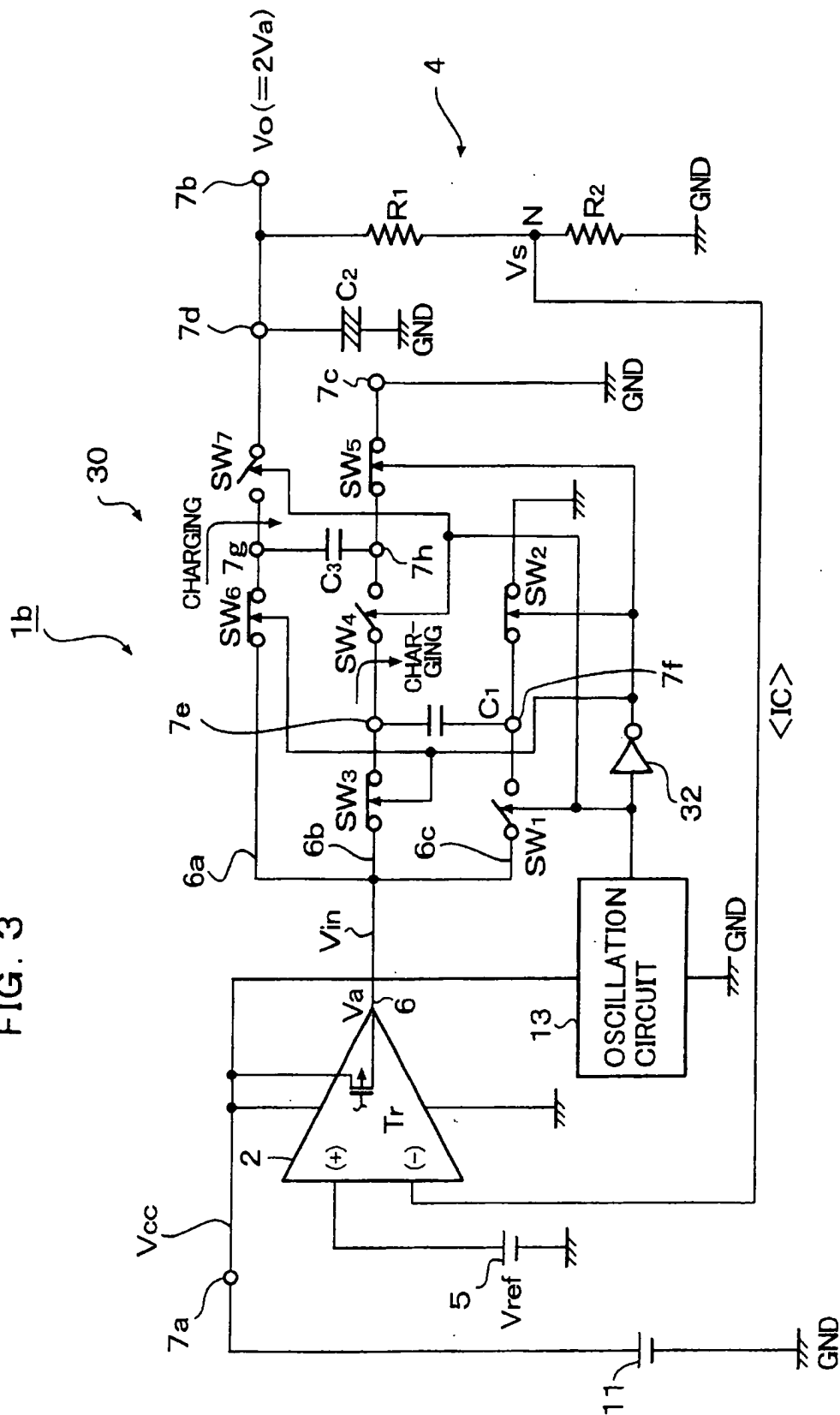


FIG. 4

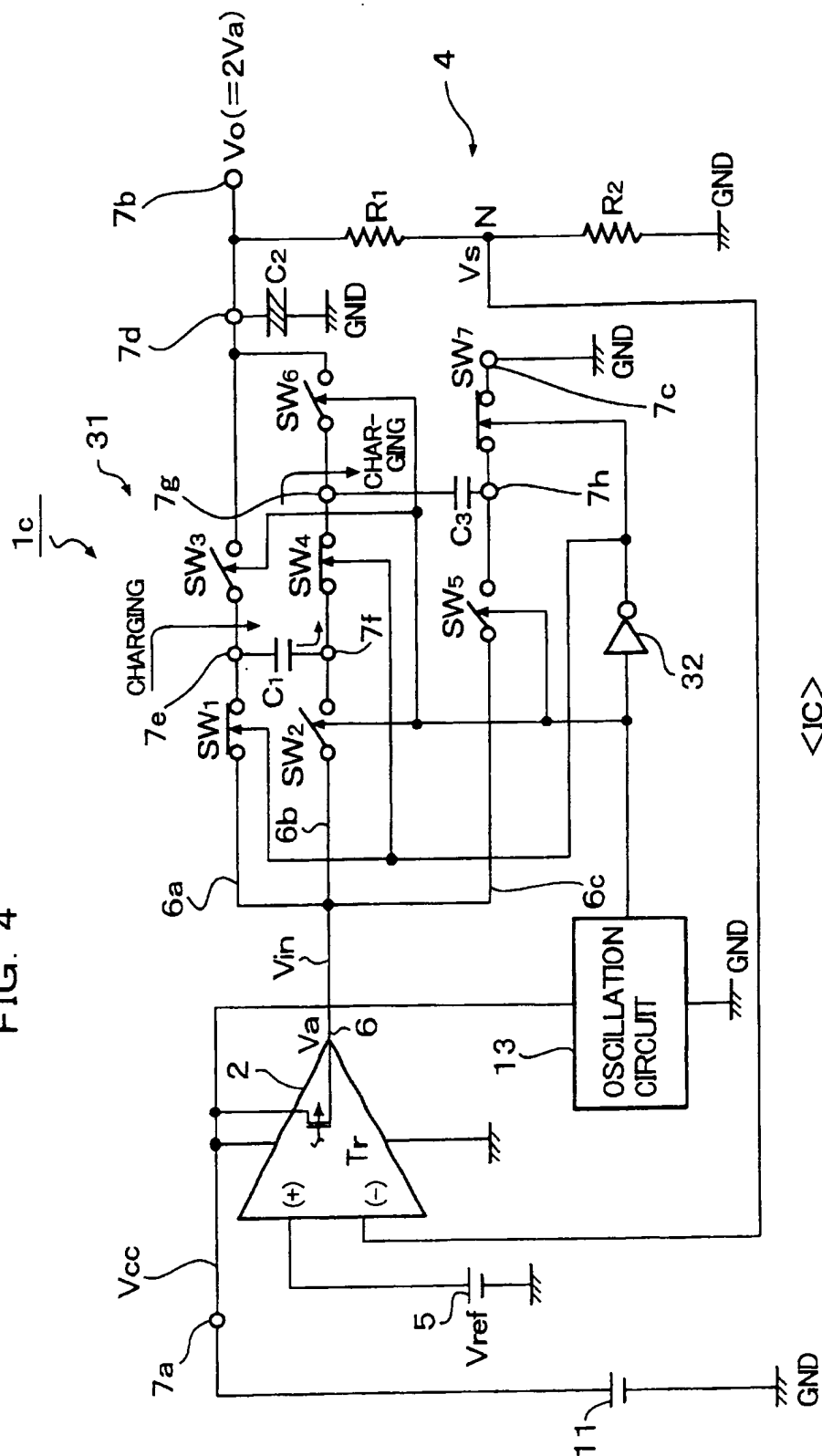
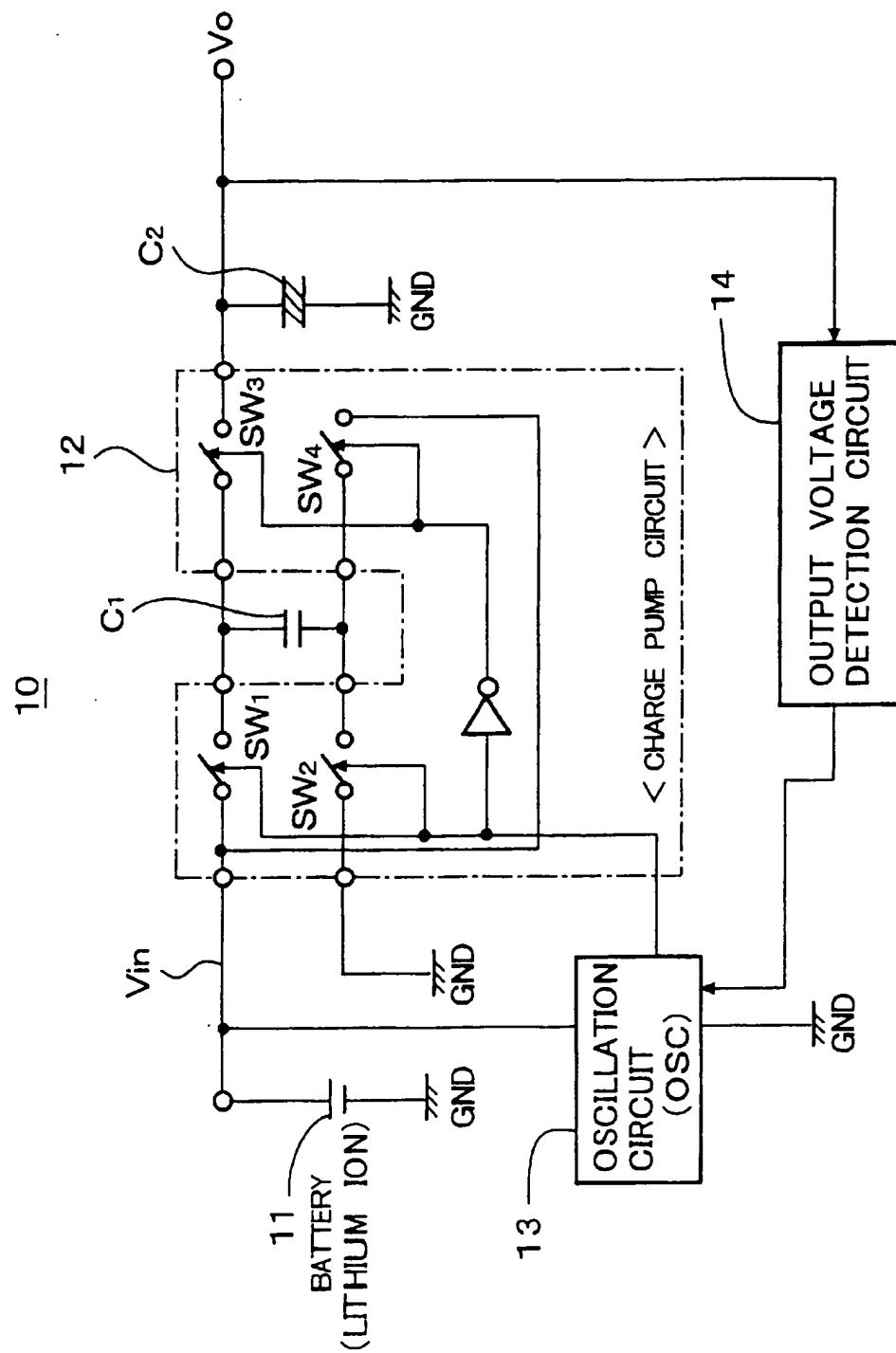


FIG. 5



## DC/DC CONVERTER

## BACKGROUND OF THE INVENTION

## 1. Field of Invention

The present invention relates to a DC/DC converter, and, more specifically, relates to a DC/DC converter which suppresses noise generation during switching in a switched capacitor type DC/DC converter which is used for a battery driven power source circuit for a portable telephone set such as for PHS (Personal Handyphone System) and portable telephone system and a battery driven power source circuit for a portable type electronic device such as an electronic book and a PDA.

## 2. Background Art

In a conventional electronic device driven by a battery such as the portable telephone set for such as PHS and portable telephone system and the portable type electronic device, a circuit which is driven by a higher voltage than a normal battery voltage is incorporated. For example, an LED element drive circuit used as a back light in a liquid crystal display device and a signal transmission circuit are such examples. In order to operate these sorts of circuits a DC/DC converter for boosting the battery voltage is frequently provided as a power source circuit within these devices.

On the other hand, with regard to these sorts of battery driven electronic devices, a size reduction and light weighting of the devices themselves have been advanced, and the size of power source circuit itself has been reduced and correspondingly a circuit with a low power consumption has been demanded. In response thereto, in these sorts of devices and apparatuses, a DC/DC converter, which transfers charged electric charges to a capacitor by means of a switched capacitor such as a charge pump circuit and boosts up to an  $n$  times voltage corresponding to a so called  $n$  times voltage rectification, is provided, for example, as a part of an LED element drive circuit and a power source circuit therefor. In these sorts of devices and apparatus, the voltage boosted by such DC/DC converter is further regulated and stabilized at a constant voltage by a regulator to produce an LED drive voltage. Thereby, a size reduction and a low power consumption of the devices is realized.

Although there are a variety of DC/DC converters of different types, however, in view of the LED element drive circuit in which voltage boosting is performed by making use of such as the charge pump circuit, it has been proposed to utilize a so called switched capacitor type DC/DC converter of which entire power source circuit is also an  $n$  times voltage rectification type.

FIG. 5 is an example of such power source circuits.

In FIG. 5, a DC/DC converter 10 includes, regardless to the LED element drive circuit, a charge pump circuit (a double voltage boosting circuit) 12 which performs switching at an oscillating frequency of an oscillation circuit (OSC) 13.

Respective terminals of a capacitor C1 of the charge pump circuit 12 are connected between an input side power source line (a positive electrode side of a lithium ion battery 11) Vin and the ground GND via respective switch circuits SW1 and SW2. Further, the respective terminals of the capacitor C1 are again connected to a charging side terminal of a power output use capacitor C2 and to the input side power source line Vin via respective switch circuits SW3 and SW4.

The charging side terminal of the capacitor C2 is connected to an output terminal Vo and the other terminal of the capacitor C2 is connected to the ground GND.

The DC/DC converter receives from the lithium ion battery 11 an electric power of a voltage of, for example, about 3.6V (usually, a certain voltage in a range of 3.0V-4.2V) and performs a boosting operation by turning ON/OFF the switch circuits SW1-SW4 in response to pulses having a predetermined frequency being outputted from the oscillation circuit (OSC) 13.

Namely, the DC/DC converter 10 turns ON the switch circuits SW1 and SW2 and OFF the switch circuits SW3 and SW4 to charge the capacitor C1 (a first capacitor), further performs a complementary switching (switching of reversing ON/OFF state of the respective switch circuits) of turning OFF the switch circuits SW1 and SW2 and ON the switch circuits SW3 and SW4 to transfer the electric charges having been charged in the capacitor C1 to the power output use capacitor. C2 (a second capacitor) after boosting substantially to doubled voltage and to charge the same.

As a result, the DC/DC converter repeats a so called double voltage rectification and generates a voltage of about 7.2V at the capacitor C2. Further, the switch circuits SW1-SW4 receive output pulses from the oscillation circuit 13 and are turned ON/OFF in response to High level thereof (hereinbelow, will be referred to as "H") and Low level thereof (hereinbelow, will be referred to as "L"). Since the switch circuits SW3 and SW4 receive the output pulses from the oscillation circuit 13 via an inverter, the switch circuit SW3 and SW4 perform the complementary switching operation with respect to the switching circuit SW1 and SW2.

The oscillation circuit 13 performs oscillation upon receipt of electric power from the lithium ion battery 11 and outputs pulses of 50% duty ratio having a predetermined frequency to the charge pump circuit 12. Then, the DC/DC converter detects the voltage Vo at the output side which is boosted by the charge pump circuit 12 at an output voltage detection circuit 14 to feed back the same to the oscillation circuit 13 and controls the oscillation frequency of the oscillation circuit 13 so that the output voltage Vo is kept at a constant voltage.

However, in such switched capacitor type DC/DC converter, since the capacitor C1 is connected to the input side power source line Vin at the time of ON/OFF switching of the switches, noises with a high level are induced on the input side power source line Vin at the time of switching the switches. Further, in order to stabilize the output voltage Vo the oscillation frequency of the oscillation circuit 13 is controlled in which when the output voltage Vo rises, in order to lower the same the switching of the switches is performed before completing charging of the capacitor C1, therefore, noises are also induced on the output line of the output voltage Vo.

Such noises reduces electric power conversion efficiency as well as causes adverse effects to the surrounding circuits. In particular, since the frequency of the oscillation circuit varies, the frequency of the noises likely varies which makes difficult to remove the noises by a filter. Especially, such is problematic to battery driven portable type electronic devices and apparatuses.

## SUMMARY OF THE INVENTION

An object of the present invention is to resolve the above problems in the conventional art and to provide a DC/DC converter which can suppress noises induced at the time of switching.

A DC/DC converter of a first aspect of the present invention which achieves the above object is characterized in that, the DC/DC converter comprises a DC power source;

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a reference voltage generating circuit; an amplifier which receives an electric power from the DC power source and outputs an electric power of which voltage is controlled so as to assume a target voltage value by stepping down the voltage of the electric power from the DC power source depending on a difference between the reference voltage and a detection voltage; an oscillation circuit which generates signals having a specific frequency; a voltage boosting circuit which receives the output of the amplifier and the output of the oscillation circuit, causes switching of the; output of the amplifier at the specific frequency to charge a first capacitor, and performs voltage boosting by transferring the electric charges charged in the first capacitor through complementary ON/OFF switching with respect to the former switching into a second capacitor after raising substantially upto  $n/m$  time voltage (wherein  $n > m$  and  $n$  and  $m$  are integers equal to or more than 2) and charging the same therewith; and an output voltage detection circuit which generates the detection voltage depending on the output voltage of the boosting circuit, whereby a voltage of substantially  $n/m$  times of the target voltage value is generated from the voltage boosting circuit.

Further, according to a DC/DC converter of a second aspect of the present invention, in place of the reference voltage generating circuit a variable voltage generating circuit is provided and in place of the output voltage detection circuit a voltage control circuit is provided which controls the variable voltage generating circuit depending on the output voltage of the voltage boosting circuit, whereby, the voltage control circuit controls the output voltage of the variable voltage generating circuit depending on the output voltage of the voltage boosting circuit, so that the output voltage of the amplifier assumes the target voltage value and causes the amplifier to generate an electric power having the target voltage value.

As has been explained in the above, according to the first aspect of the present invention, since the output voltage of the voltage boosting circuit is detected, the detected voltage is fed back to the amplifier and the output voltage of the amplifier is controlled so as to assume the target voltage value, the voltage boosting circuit which performs voltage boosting upon receipt of the output voltage of the amplifier can generate an electric power having a voltage of  $n/m$  times of the target voltage value. Thereby, the voltage boosting circuit can output an electric power having a stabilized voltage of substantially  $n/m$  times with respect to the target voltage value.

In this instance, since the voltage boosting circuit produces the boosted voltage through the switching control with the specific constant frequency, even when the boosted voltage rises above the voltage of  $n/m$  times of the target voltage value, the switching change-over during charging in the voltage boosting operation never happens to thereby suppress the noise generation. Moreover, since the switching frequency is kept constant, a circuit which facilitates noise removal in the surrounding circuits can be realized.

As a result, in the switched capacitor type DC/DC converter, the noise generation at the time of switching for voltage boosting can be suppressed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a switched capacitor type DC/DC converter representing one embodiment to which a DC/DC converter of the present invention is applied;

FIG. 2 is a block diagram of another embodiment of a DC/DC converter of the present invention;

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FIG. 3 is a block diagram of one embodiment of a three time voltage boosting DC/DC converter to which the present invention is applied;

FIG. 4 is a block diagram of one embodiment of 1.5 time voltage boosting DC/DC converter to which the present invention is applied; and

FIG. 5 is a block diagram showing an example of conventional switched capacitor type DC/DC converters.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, 1 is a switched capacitor type DC/DC converter in an IC form which is driven by an electric power from a lithium ion battery 11 and includes a power supply use error amplifier 2, a charge pump circuit 3, a resistor voltage divider circuit 4 for output voltage detection and a reference voltage generating circuit 5, and these circuits excluding the battery 11 and capacitors C1 and C2 are formed into a single IC. The portion surrounded by the dotted frame shows the range of the IC and terminals 7a-7f are ones of the IC.

7a is an input terminal of the DC/DC converter 1, 7b is the output terminal thereof and 7c is the ground terminal thereof. The capacitor C1 is connected between the terminals 7e and 7f and the power output use capacitor C2 is connected between the terminal 7d and the ground GND. Further, the same constitutional elements in FIG. 1 as in FIG. 5 are designated by the same reference numerals as in FIG. 5.

The power supply use error amplifier 2 is an inverted amplifier constituted by a differential amplifier and which receives at the power source line Vcc thereof an electric power from the positive electrode side of the lithium ion battery 11 via the terminal 7a to operate the same, steps down the voltage of the power source line Vcc through an output transistor Tr therein and sends out the output to an output line 6. The power supply use error amplifier 2 compares the detection voltage (a divided voltage) Vs of the resistor divider circuit 4 and the reference voltage Vref of the reference voltage generating circuit 5 and generates an electric power of a voltage for canceling the difference depending on the difference at the output line 6.

Further, the voltage of the output line 6 is in a range lower than the voltage Vcc of the power source line Vcc (which corresponds to the voltage of the lithium ion battery 11) by about 0.4V-1.5V and is herein determined as the target voltage value Va.

For example, when assuming that the voltage of the lithium ion battery 11 is 3.6V (a certain voltage in a range of 3.0V-4.2V) and the target voltage Va is 3.2V, the power supply use error amplifier 2 steps down the voltage of the power source Vcc by about 0.4V by means of the output transistor Tr and performs a control so that when the voltage Vs coincides with the reference output voltage Vref, the output voltage thereof assumes the target voltage Va of 3.2V. Further, for example, when assuming the target voltage Va as 2.5V, the power supply use error amplifier 2 steps down the voltage of the power source line Vcc by about 1.1V by means of the output transistor Tr and performs a control so that when the voltage Vs coincides with the reference voltage Vref, the output voltage assumes the target voltage Va of 2.5V.

The charge pump circuit 3 is a double voltage boosting circuit corresponding to the charge pump circuit 12 as shown in FIG. 5, the input side power source line Vin thereof is connected to the output line 6, the connection change-over (switching) of the capacitors C1 and C2 is performed by the

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pulses from the oscillation circuit (OSC) 13 like in FIG. 5 and generates the output voltage  $V_o (=2V_a)$  at the output terminal 7b (or at terminal 7d) after boosting the voltage of the output line 6 upto a double voltage. Further, since the oscillation frequency is not controlled by the oscillation circuit 13, a constant oscillation frequency is given here.

When applying the example where the target voltage  $V_a$  is assumed as 3.2V, the output voltage assumes 6.4V which is two times of the target voltage  $V_a$  under the regulation condition. In this instance, the output voltage  $V_o$  boosted in double at the output terminal 7b under a normal operating condition falls in a range of about 4.8V–7.2V as a regulation range.

The resistor divider circuit 4 is constituted by resistors R1 and R2 connected in series between the output terminal 7b and the ground GND, and generates the divided voltage (detection voltage)  $V_s$  at the junction N of the resistors R1 and R2.

An operation, where the target voltage  $V_a$  is 3.2V, will be explained, if the voltage of the divider voltage  $V_s$  at the junction N is high, the current output voltage of the power supply use error amplifier 2 is higher than the target voltage  $V_a$  of 3.2V. In this instance, the power supply use error amplifier 2 performs an inverted amplification depending on the difference voltage  $V_s - V_{ref}$  from the reference output voltage  $V_{ref}$  to increase the internal impedance in the output transistor Tr, generates a reduced voltage at the output line 6 to lower the output voltage  $V_o$  to be boosted to double voltage by the charge pump circuit 3 and performs a control to assume  $V_s = V_{ref}$ . Thereby, the output voltage  $V_o$  is controlled to assume 6.4V, two times of the target voltage.

Contrary thereto, when the voltage of the divided voltage  $V_s$  at the junction N is low, the current output voltage of the power supply use error amplifier 2 is lower than the target voltage  $V_a$  of 3.2V. In this instance, the power supply use error amplifier 2 performs an inverted amplification depending on the difference voltage  $-(V_{ref} - V_s)$  from the reference output voltage  $V_{ref}$  to decrease the internal impedance in the output transistor Tr, generates a higher voltage at the output line 6 to raise the output voltage  $V_o$  to be boosted to double voltage by the charge pump circuit 3 and performs a control to assume  $V_s = V_{ref}$ . Thereby, the output voltage  $V_o$  is controlled to assume 6.4V, two times of the target voltage.

In the above, the oscillation frequency of the oscillation circuit (OSC) 13 is kept constant and is set to a periodic value in which the change-over timing is determined in such a manner that after completing charging of the capacitor C1 the connection for boosting the terminal voltage of the capacitor C1 is started. Therefore, the charge pump circuit 3 always performs an accurate double voltage boosting operation after completing the charging of the capacitor C1. Thereby, the switching noises induced on the output line of the output voltage  $V_o$  are suppressed. Further, the oscillation frequency of the oscillation circuit 13 falls in a range of 300 kHz–700 kHz. When the oscillation frequency is assumed, for example, as 650 kHz, each capacitance of the capacitors C1 and C3 is about 0.22  $\mu$ F and the capacitance of the output use capacitor C2 is about 1  $\mu$ F. If the output voltage  $V_o$  is selected in a range of 5.0V–6.4V, the output power thereof is about 100 mA.

Further, in the present embodiment as shown in the drawing, the input side power source line  $V_{in}$  of the charge pump circuit 3 is connected not to the positive electrode of the battery 11, but to the output line of the power supply use error amplifier 2 and, in that connected to the positive electrode of the battery 11 via the output stage transistor Tr. Thereby, the noise generation at the input side is also suppressed.

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In both instances, since the generated noise frequency corresponds to the oscillation frequency of the oscillation circuit (OSC) 13, the noises in the surrounding circuits are easily removed by a noise removing filter and the surrounding circuits are hardly affected by the noises.

FIG. 2 shows a switched capacitor type DC/DC converter 1a representing another embodiment of the present invention, in which in place of the reference voltage generating circuit 5 in FIG. 1 a variable voltage generating circuit 8 is provided, in place of the differential amplifier 2 an operational amplifier (OP) 2a is provided and further, in place of the resistor divider circuit 4 a voltage control circuit (a negative feed back circuit) 9 is provided. Further, in the present embodiment, the electric power for the oscillation circuit 13 is supplied from the output of the operation amplifier (OP) 2a. A resistor Rf and a resistor Rs in the operation amplifier 2a are respectively a feed back resistor and a reference resistor.

With regard to the operation of the present embodiment, the output voltage of the variable voltage generating circuit 8 is controlled by generating a negative feed back control signal (a control signal which suppresses the output voltage  $V_o$  when the same rises, and raises the same when drops) which varies the output voltage of the variable voltage generating circuit 8 depending on the output voltage  $V_o$  by the voltage control circuit 9. The output voltage is amplified and controlled by the operation amplifier 2a so that the output voltage of the operation amplifier 2a assumes the target voltage value  $V_a$ . Thereby, the output voltage  $V_o$  is stabilized.

In this instance too, the oscillation frequency of the oscillation circuit (OSC) 13 is kept constant and the charge pump circuit 3 always performs an accurate double voltage boosting operation after completing the charging of the capacitor C1.

FIG. 3 shows a DC/DC converter 1b in which the charge pump 3 in FIG. 1 is replaced by a three time voltage boosting charge pump circuit 30. Like FIG. 1 embodiment, the circuit other than the battery 11 and capacitors C1–C3 are formed into a single IC, however, the dotted line frame indicating the IC region is omitted.

In connection with the three time voltage boosting, a third capacitor C3 is provided which is charged together with the capacitor C1. Further, the charge pump circuit 30 includes seven switches (or switch circuit, the same is true in the following) SW1–SW7, and charges the three capacitors C1–C3 therewith. Further, the capacitor C3 is connected between terminals 7g and 7h.

When explaining specifically, the output line 6 of the power supply use error amplifier 2 is branched into three power lines 6a, 6b and 6c. The capacitor C1 is connected between the power lines 6b and 6c via the respective switches SW3 and SW1. The capacitor C3 is connected between the terminal (terminal 7e) at the side connected to the power line 6b of the capacitor C1 and the power line 6a via the respective switches SW4 and SW6. Further, the terminal (terminal 7h) of the capacitor C3 at the side being connected to the capacitor C1 is connected to the ground GND via the m switch SW5, and the terminal (terminal 7f) of the capacitor C1 at the side being connected to the power line 6c is connected to the ground GND via the switch SW2.

The terminal (terminal 7d) at the charging side of the capacitor C2 is connected to the terminal (terminal 7g) of the capacitor C3 at the side being connected to the power line 6a via the switch SW7, and the other terminal of the capacitor C2 is connected to the ground GND.

Herein, the switches SW1, SW4 and SW7 perform a complementary switching operation with respect to the switches SW2, SW3 and SW6 by receiving the output pulses from the oscillation circuit 13 via the inverter 32.

In the embodiment circuit, during the interval when the output pulse from the oscillation circuit 13 assumes "H", as illustrated in the drawing, the respective switches SW2, SW3, SW5 and SW6 are turned ON, the respective switches SW1, SW4 and SW7 are turned OFF and the capacitors C1 and C2 are connected in parallel and are charged. During the interval when the output pulse of the oscillation circuit 13 assumes "L", contrary thereto, the respective switches SW2, SW3, SW5 and SW6 are turned OFF, the respective switches SW1, SW4 and SW7 are turned ON and the capacitors C1 and C3 are connected in series to the output line 6 ( $V_{in}$ ) and the terminal 7d, further the terminal 7f is connected to the output line 6, thereby, the voltage of the capacitors C1 and C3 is boosted by  $V_{in}$ . As a result, the terminal voltage of the capacitor C3 assumes the three time voltage of  $V_{in}$  and the electric charges thereof are transferred to the capacitor C2.

FIG. 4 shows a DC/DC converter 1c in which the charge pump circuit 30 in FIG. 3 is replaced by a 1.5 time voltage boosting charge pump 31. Like FIG. 1 embodiment, the circuit other than the battery 11 and capacitors C1-C3 are formed into a single IC, however, the dotted line frame indicating the IC region is omitted.

The charge pump circuit 31, likely, includes seven switches SW1-SW7 and three capacitors C1-C3. However, the connecting condition of the capacitors C1 and C3 is different from that in FIG. 3 embodiment.

Namely, the capacitor C1 is connected between the power lines 6a and 6b via the respective switches SW1 and SW2. The capacitor C3 is connected between the terminal (terminal 7f) of the capacitor C1 at the side being connected to the power line 6b and the power line 6c via the respective switches SW4 and SW5. Further, the terminal (terminal 7g) of the capacitor C3 to which the switch SW4 is connected is connected to the terminal (terminal 7d) at the charging side of the capacitor C2 via the switch SW6, and the terminal (terminal 7h) of the capacitor C3 at the side being connected to the power line 6c is connected to the ground GND. Further, the terminal (terminal 7e) of the capacitor C1 at the side being connected to the power line 6a is connected to the terminal (terminal 7d) at the charging side of the capacitor C2 via the switch SW3.

Like the previous embodiment, the switches SW1, SW4 and SW7 perform a complementary switching operation with respect to the switches SW2, SW3 and SW6 by receiving the output pulses from the oscillation circuit 13 via the inverter 32.

Now, in the present embodiment circuit, during the interval when the output pulse from the oscillation circuit 13 assumes "H", as illustrated in the drawing, the respective switches SW2, SW3, SW5 and SW6 are turned OFF, the respective switches SW1, SW4 and SW7 are turned ON and the capacitors C1 and C2 are connected in series and are charged. During the interval when the output pulse of the oscillation circuit 13 assumes "L", contrary thereto, the respective switches SW2, SW3, SW5 and SW6 are turned ON, the respective switches SW1, SW4 and SW7 are turned OFF and the capacitors C1 and C3 are connected in parallel to the output line 6 ( $V_{in}$ ) and the terminal 7d, further the terminals 7f and 7h are connected to the output line 6, thereby, the voltage of the capacitors C1 and C3 is boosted by  $V_{in}$ . As a result, the terminal voltage of the capacitors C1 and C3 assumes the 1.5 time voltage of  $V_{in}$  and the electric

charges thereof are transferred to the capacitor C2, and the voltage of the capacitor C2 assumes 1.5 time voltage. Herein, the capacitances of the respective capacitors C1 and C2 are the same.

The above is an embodiment in which the voltage is boosted by adding 0.5 times of  $V_{in}$ , however, in the same manner if n times voltage is added to 0.5 time voltage of  $V_{in}$ , boosted voltage of 2.5 times, 3.5 times . . . can be generated. After obtaining n times voltage (wherein, n is an integer of equal to or more than 3) by connecting two capacitors in series, it is easy to generate n/2 time voltage by connecting these capacitors in parallel. Further, in the above embodiment at first two capacitors are connected in series, thereafter, the connection of the capacitors is changed over to a parallel connection to obtain the voltage  $V_{in}/2$  with respect to the power source voltage  $V_{in}$ , therefore, in the like manner, at first k pieces (k is an integer equal to or more than 2) of capacitors are connected in series, thereafter, the k pieces of capacitors are connected in parallel to thereby obtain the voltage of  $V_{in}/k$ , and when the voltage  $V_{in}$  is added to the obtained voltage, the boosted voltage  $V_{in}(k+1)/k$  can be generated. Further, if voltage of  $nV_{in}$  which is boosted to n times voltage is added to the above boosted voltage, a further boosted voltage can be generated. Further, a boosted voltage of  $nV_{in}(k+1)/k$  also can be generated.

As will be understood from the above, voltage boosting to n/m time voltage is generally possible. Wherein  $n > m$  and n and m are integers more than 2.

In the embodiments as has been explained hitherto, the use of the lithium battery is exemplified, however, the power source is not limited to the lithium battery, but a power source by means of a ferroelectric capacitor and a power source in which an AC commercial power source is converted into a DC can also be used. In other words, any power sources of DC power source can be applied to the present invention.

What is claimed is:

1. A DC/DC converter characterized in that, the DC/DC converter comprises a DC power source; a reference voltage generating circuit; an amplifier which receives an electric power from the DC power source and outputs an electric power of which voltage is controlled so as to assume a target voltage value by stepping down the voltage of the electric power from the DC power source depending on a difference between the reference voltage and a detection voltage; an oscillation circuit which generates signals having a specific frequency; a voltage boosting circuit which receives the output of the amplifier and the output of the oscillation circuit, causes switching of the output of the amplifier at the specific frequency to charge a first capacitor, and performs voltage boosting by transferring the electric charges charged in the first capacitor through complementary ON/OFF switching with respect to the former switching into a second capacitor after raising substantially upto n/m time voltage (wherein  $n > m$  and n and m are integers equal to or more than 2) and charging the same therewith; and an output voltage detection circuit which generates the detection voltage depending on the output voltage of the boosting circuit, whereby a voltage of substantially n/m times of the target voltage value is generated from the voltage boosting circuit.

2. A DC/DC converter of claim 1, wherein the DC power source is a battery, the amplifier is a differential amplifier at the inputs of which the reference voltage and the detection voltage are respectively received, and the boosting circuit includes a charge pump circuit for charging the first and second capacitors.

3. A DC/DC converter of claim 2, wherein the differential amplifier is to perform an inverted amplification, the oscil-



lation circuit is to generate a pulse for the switching operation, the specific frequency is a frequency having a period which permits the complementary switching after substantially completing the charging of the first capacitor, and the differential amplifier, the charge pump circuit, the oscillation circuit, the output voltage detection circuit and the reference voltage generating circuit are formed in an IC.

4. A DC/DC converter of claim 3, wherein the duty ratio of the pulse is substantially 50%, the charge pump circuit includes a plurality of switch circuits which permit selective ON/OFF switching, and the selective ON/OFF switching of the plurality of switch circuits is performed in response to the pulse.

5. A DC/DC converter of claim 4, wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits, and after charging the first capacitor by grounding one terminal of the first capacitor and by supplying at the other terminal thereof an electric power from the differential amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, and the one terminal of the first capacitor is connected to the output terminal of the differential amplifier to generate a boosted voltage at the other terminal thereof and to thereby charge the second capacitor.

6. A DC/DC converter of claim 4, further comprises a third capacitor wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits to connect the first and third capacitors in series, and after charging the first and third capacitors by grounding one terminal of the series connection and by supplying at the other terminal thereof an electric power from the differential amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, and the one terminal of the series connection circuit is connected to the output terminal of the differential amplifier to generate a substantially three times boosted voltage at the other terminal thereof and to thereby charge the second capacitor.

7. A DC/DC converter of claim 4, further comprises a third capacitor wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits to connect the first and third capacitors in series, and after charging the first and third capacitors by grounding one terminal of the series connection and by supplying at the other terminal thereof an electric power from the differential amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, the series connected first and third capacitors are connected in parallel, and the grounded one terminal is connected to the output terminal of the differential amplifier to generate a substantially 1.5 times boosted voltage at the other terminal thereof and to thereby transfer the electric charges in the first and third capacitors to the second capacitor.

8. A DC/DC converter of claim 1, wherein in place of the reference voltage generating circuit a variable voltage generating circuit is provided and in place of the output voltage detection circuit a voltage control circuit is provided, whereby, the voltage control circuit controls the output voltage of the variable voltage generating circuit depending on the output voltage of the voltage boosting circuit so that the output voltage of the amplifier assumes the target voltage value and causes the amplifier to generate an electric power having the target voltage value.

9. A DC/DC converter characterized in that, the DC/DC converter comprises a DC power source; a variable voltage generating circuit; an amplifier which receives an electric power from the DC power source, amplifies the output voltage of the variable voltage generating circuit and outputs the same; an oscillation circuit which generates signals having a specific frequency; a voltage boosting circuit which receives the output of the amplifier and the output of the

oscillation, circuit, causes switching of the output of the amplifier at the specific frequency to charge a first capacitor, and performs voltage boosting by transferring the electric charges charged in the first capacitor through complementary ON/OFF switching with respect to the former switching into a second capacitor after raising substantially upto  $n/m$  time voltage (wherein  $n > m$  and  $n$  and  $m$  are integers equal to or more than 2) and charging the same therewith; and a voltage control circuit which controls the output voltage of the variable voltage generating circuit depending on the output voltage of the boosting circuit so that the output voltage of the amplifier assumes the target voltage value, whereby a voltage of substantially  $n/m$  times of the target voltage value is generated from the voltage boosting circuit.

10. A DC/DC converter of claim 9, wherein the DC power source is a battery, and the boosting circuit includes a charge pump circuit for charging the first and second capacitors.

11. A DC/DC converter of claim 10, wherein the oscillation circuit is to generate a pulse for the switching operation, the specific frequency is a frequency having a period which permits the complementary switching after substantially completing the charging of the first capacitor, and the amplifier, the charge pump circuit, the oscillation circuit, the voltage control circuit and the variable voltage generating circuit are formed in an IC.

12. A DC/DC converter of claim 11, wherein the duty ratio of the pulse is substantially 50%, the charge pump circuit includes a plurality of switch circuits which permit selective ON/OFF switching, and the selective ON/OFF switching of the plurality of switch circuits is performed in response to the pulse.

13. A DC/DC converter of claim 12, wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits, and after charging the first capacitor by grounding one terminal of the first capacitor and by supplying at the other terminal thereof an electric power from the amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, and the one terminal of the first capacitor is connected to the output terminal of the amplifier to generate a boosted voltage at the other terminal thereof and to thereby charge the second capacitor.

14. A DC/DC converter of claim 12, further comprises a third capacitor wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits to connect the first and third capacitors in series, and after charging the first and third capacitors by grounding one terminal of the series connection and by supplying at the other terminal thereof an electric power from the amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, and the one terminal of the series connection circuit is connected to the output terminal of the amplifier to generate a substantially three times boosted voltage at the other terminal thereof and to thereby charge the second capacitor.

15. A DC/DC converter of claim 12, further comprises a third capacitor wherein the charge pump circuit performs the selective ON/OFF switching of the plurality of switch circuits to connect the first and third capacitors in series, and after charging the first and third capacitors by grounding one terminal of the series connection and by supplying at the other terminal thereof an electric power from the amplifier, the ON/OFF switching of the plurality of switch circuits is inverted, the series connected first and third capacitors are connected in parallel, and the grounded one terminal is connected to the output terminal of the amplifier to generate a substantially 1.5 times boosted voltage at the other terminal thereof and to thereby transfer the electric charges in the first and third capacitors to the second capacitor.



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Ito et al.

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(45) **Date of Patent:** Sep. 9, 2003

(54) **VCO CIRCUIT WITH WIDE OUTPUT  
FREQUENCY RANGE AND PLL CIRCUIT  
WITH THE VCO CIRCUIT**

5,936,478 A 8/1999 Lee et al.  
6,072,345 A 6/2000 Ooishi  
6,157,180 A • 12/2000 Kuo ..... 323/282

(75) **Inventors:** Yoshiaki Ito, Hyogo (JP); Yoshiyuki  
Ota, Hyogo (JP)

(73) **Assignee:** Mitsubishi Denki Kabushiki Kaisha,  
Tokyo (JP)

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(51) **Int. Cl.<sup>7</sup>** ..... H03L 7/00

(52) **U.S. Cl.** ..... 331/25; 331/74; 331/34

(58) **Field of Search** ..... 331/25, 18, 74,  
331/34, 57

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,175,512 A 12/1992 Self  
5,233,314 A • 8/1993 McDermott et al. .... 327/157  
5,412,349 A • 5/1995 Young et al. .... 331/1 A  
5,426,398 A • 6/1995 Kuo ..... 331/57  
5,666,088 A 9/1997 Penza

**FOREIGN PATENT DOCUMENTS**

JP 7-321649 12/1995  
JP 9-200001 7/1997  
JP 10-200382 7/1998  
TW 364664 7/1999

**OTHER PUBLICATIONS**

"Adaptive Bandwidth DLLs and PLLs Using Regulated Supply CMOS Buffers", Sidiropoulos et al., 2000 Symposium on VLSI Circuits Digest of Technical Papers.

\* cited by examiner

*Primary Examiner*—Robert Pascal

*Assistant Examiner*—Kimberly E Glenn

(74) *Attorney, Agent, or Firm*—Burns, Doane, Swecker & Mathis, LLP

(57) **ABSTRACT**

A voltage-controlled oscillating circuit according to the present invention includes: a bias voltage generating circuit outputting a bias voltage according to a control voltage; and a ring oscillator circuit receiving supply of the bias voltage to operate. The bias voltage generating circuit generates the bias voltage using a feedback circuit formed by an operational amplifier receiving supply of a power source voltage to operate. Therefore, an influence of a high frequency component overlapped on the power source voltage, that is an influence of noise, is suppressed, thereby enabling stable generation of an output clock having a small variation in phase.

20 Claims, 8 Drawing Sheets

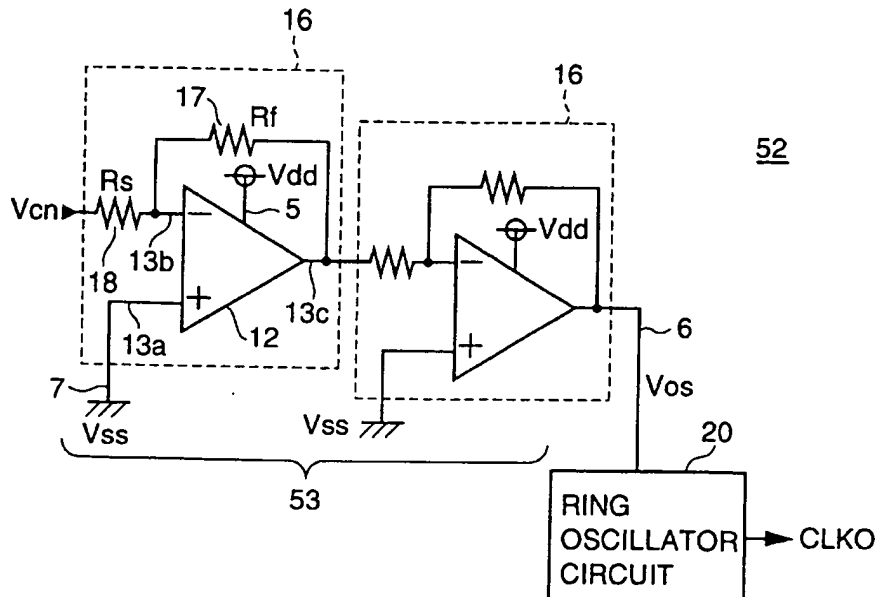


FIG. 1

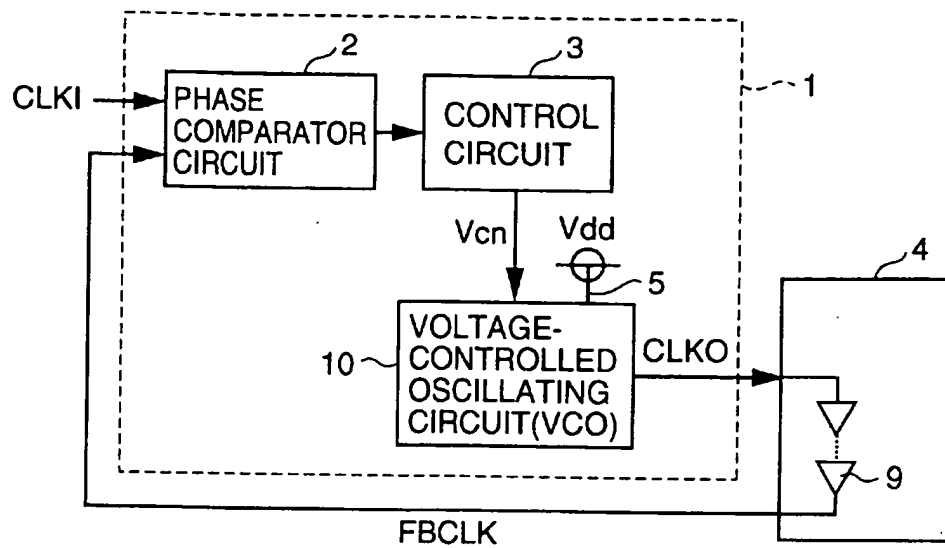


FIG. 2

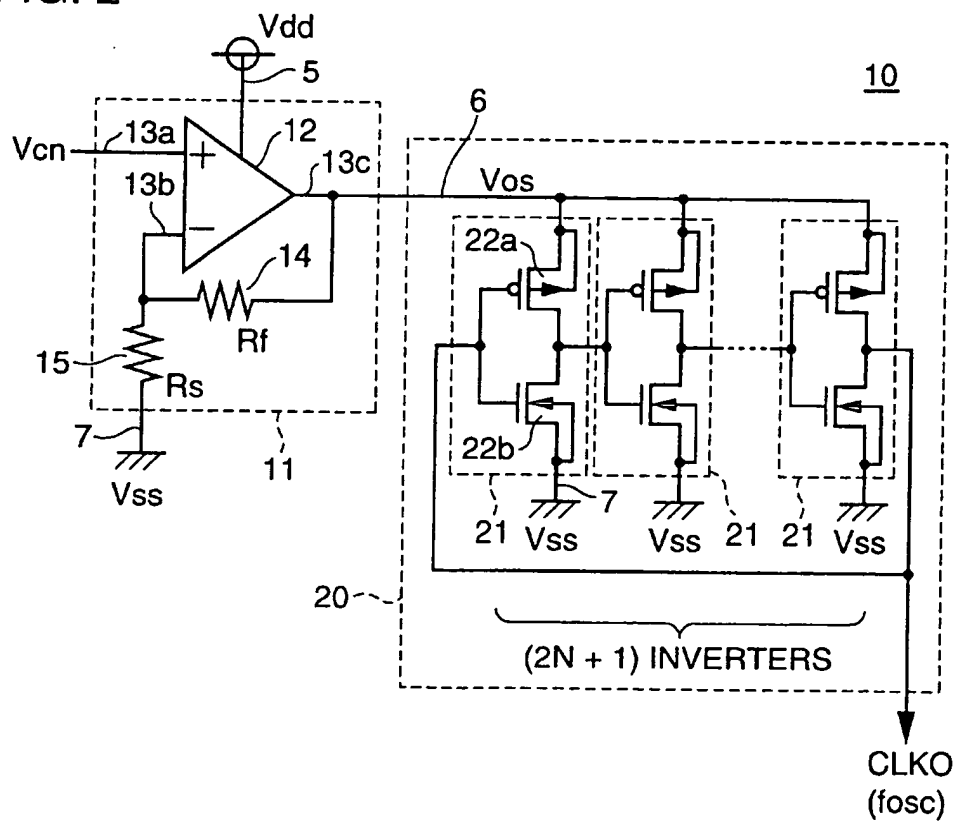


FIG. 3

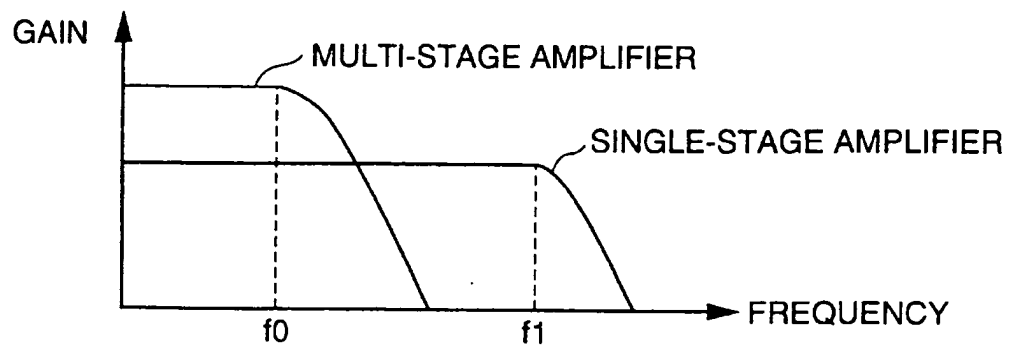


FIG. 4

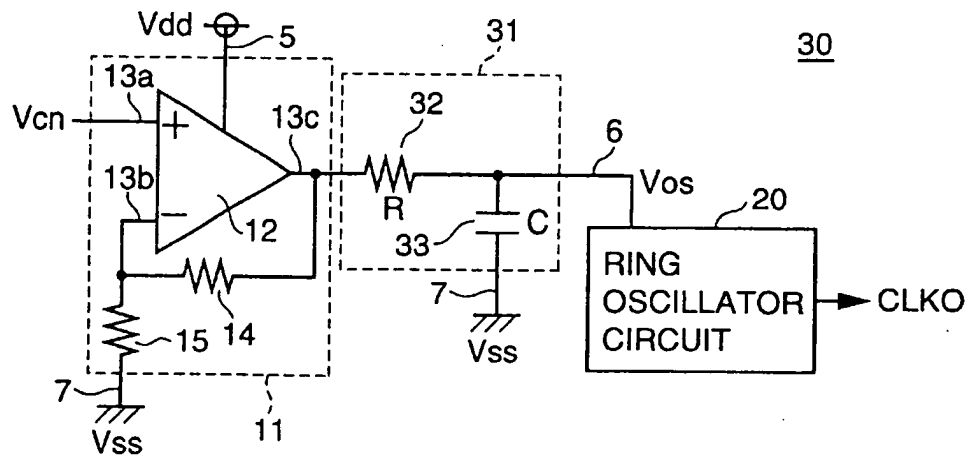


FIG. 5

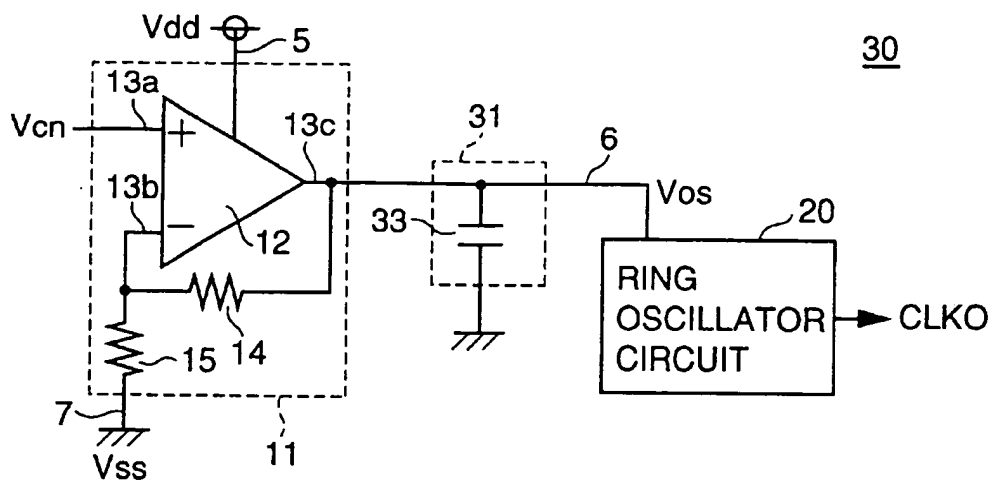


FIG. 6

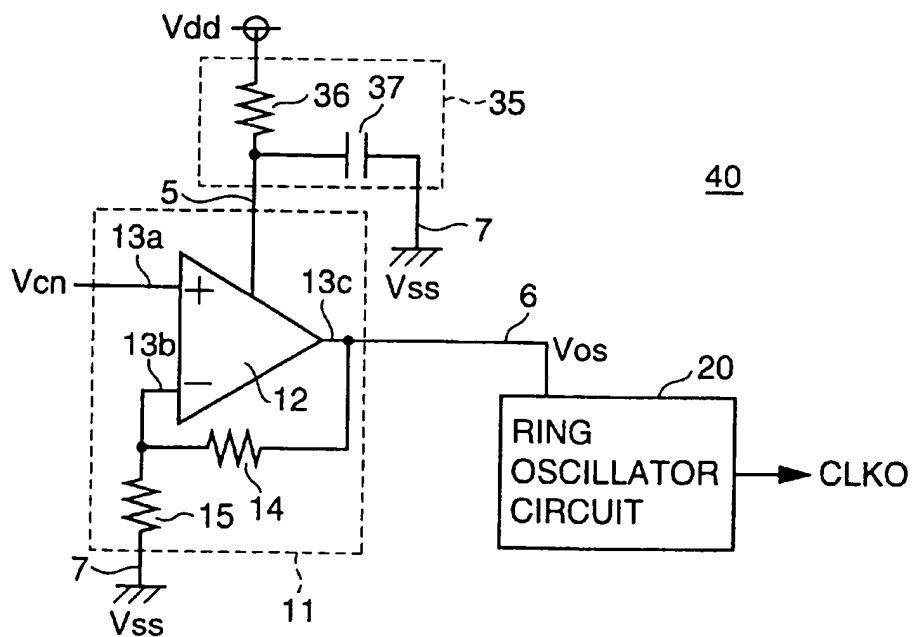


FIG. 7A

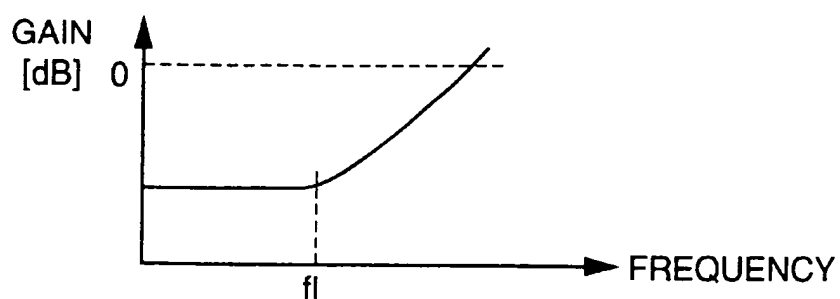


FIG. 7B

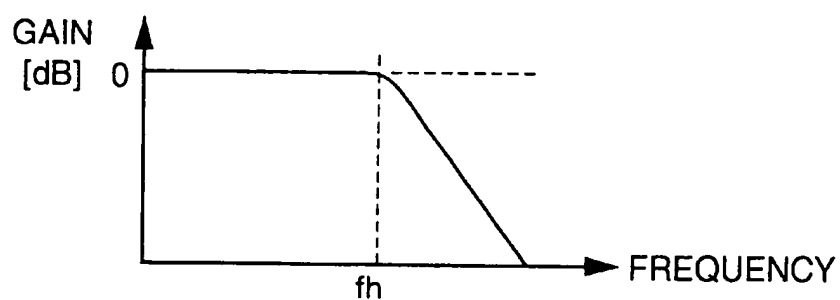


FIG. 7C

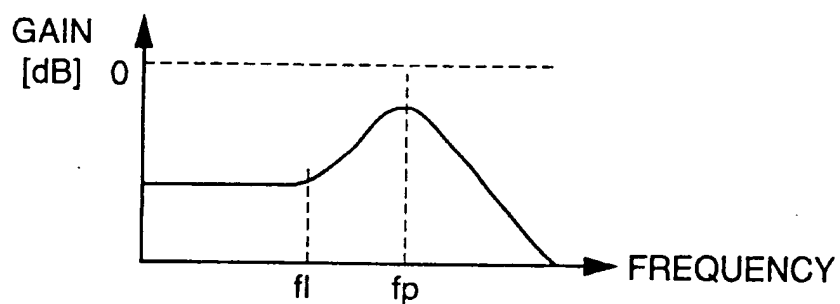


FIG. 7D

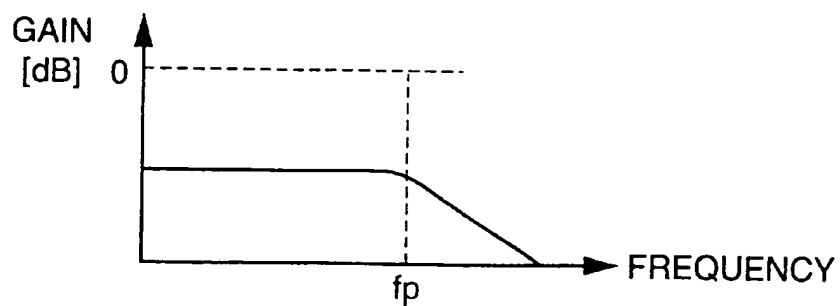


FIG. 8

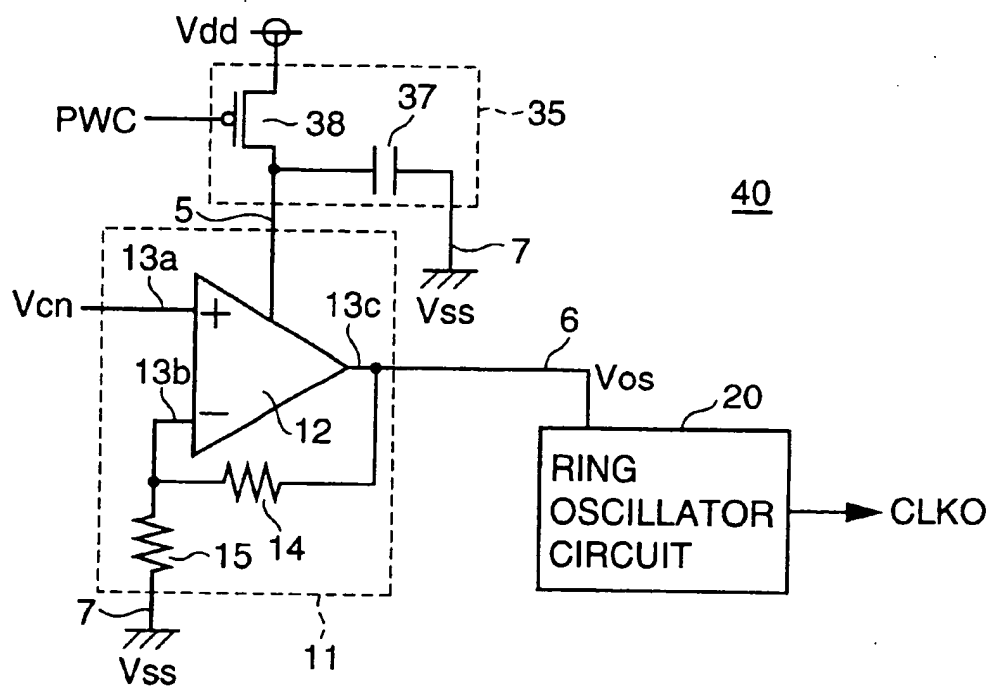


FIG. 9

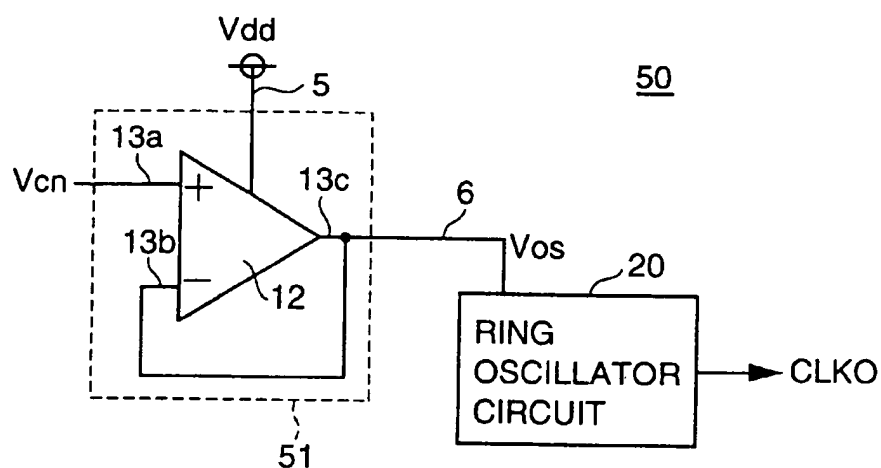


FIG. 10

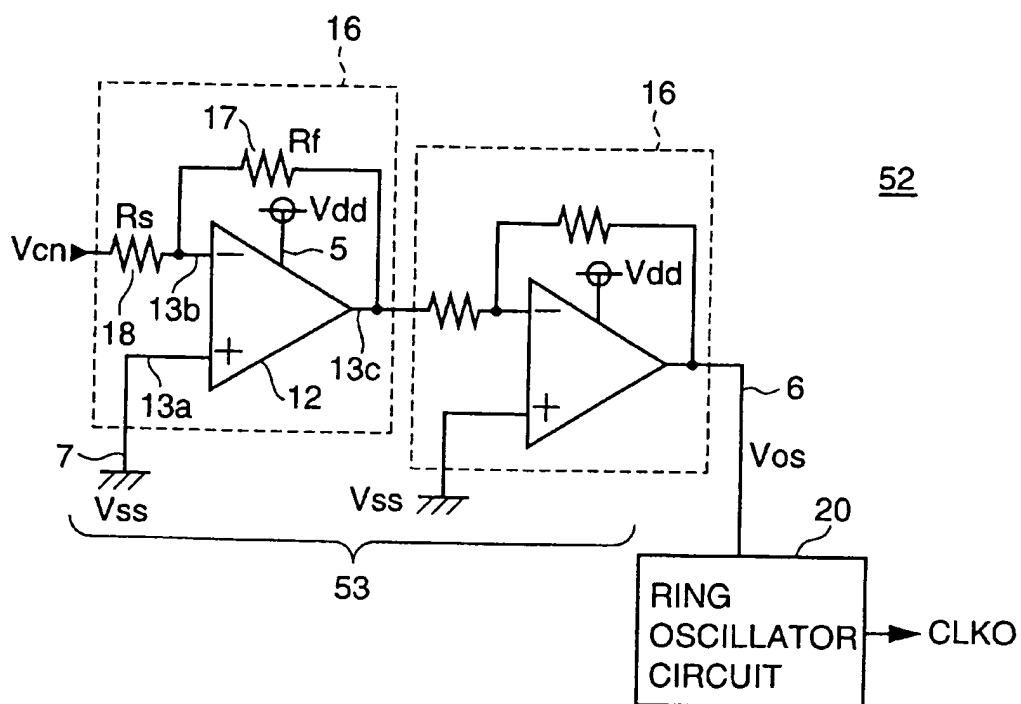




FIG. 11

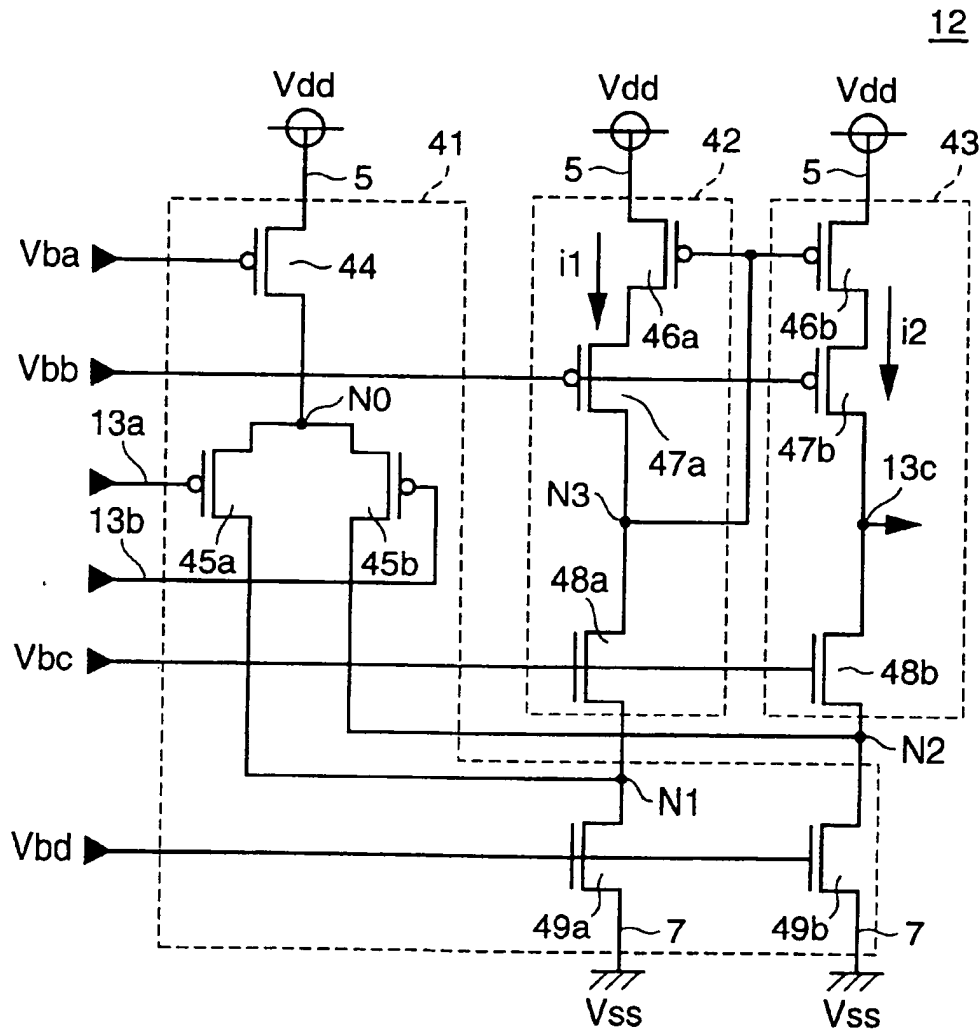


FIG. 12 PRIOR ART

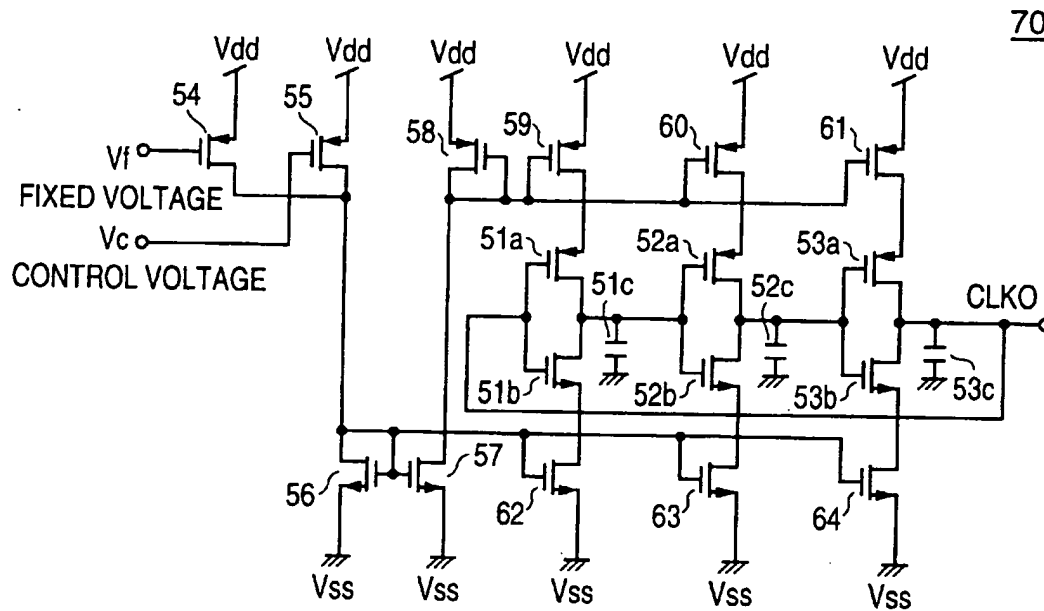
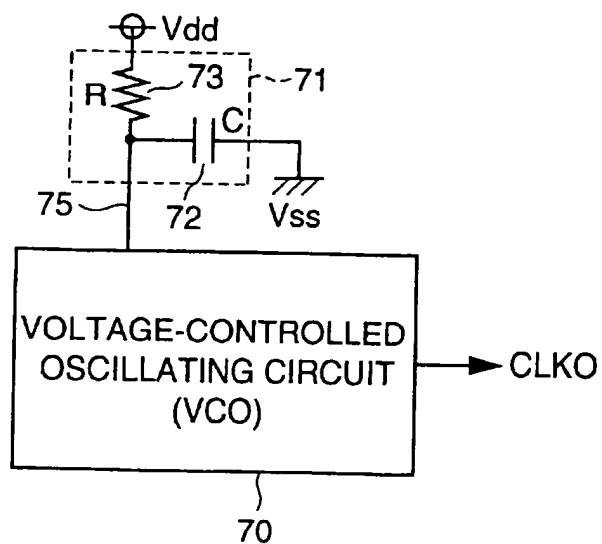


FIG. 13 PRIOR ART



# VCO CIRCUIT WITH WIDE OUTPUT FREQUENCY RANGE AND PLL CIRCUIT WITH THE VCO CIRCUIT

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a voltage-controlled oscillating circuit, and more particularly, to a voltage-controlled oscillating circuit capable of altering an oscillating frequency according to a control voltage and to a phase-locked loop circuit, a so-called PLL circuit, equipped with the voltage-controlled oscillating circuit.

### 2. Description of the Background Art

In order to cooperatively operate a plurality of internal circuits implemented on the same system, employed are phase-locked loop circuits (PLL circuit) each generating a synchronized clock. Especially, in recent years, an LSI (Large Scale Integrated Circuit) has experienced progress toward its higher speed operation in company with miniaturization; as a result, a margin in phase shift between a clock of the entire system on which an LSI is implemented and an internal clock of the LSI has become narrowed, which in turn, has enhanced a chance of usage of a PLL circuit to compensate a phase shift.

As a result, many of PLL circuits are required to be incorporated, which leads to increase in design load in order to output synchronized clocks corresponding to a wide frequency range. Accordingly, it is important to make an output frequency range (lock range) of a PLL circuit as wide as possible and thereby, cover a necessary frequency range with a single PLL circuit.

Since a lock range of a PLL circuit is largely dependent on an output frequency range of a voltage-controlled oscillator included, it is important to ensure a wide output frequency range of the voltage-controlled oscillating circuit. A general configuration of such a voltage-controlled oscillating circuit is shown, for example in FIG. 2 of Japanese Patent Laying-Open No. 9-200001(1997). The general configuration of a voltage-controlled oscillating circuit disclosed in the publication is hereinafter referred to the prior art.

FIG. 12 is a circuit diagram representing a configuration of the prior art voltage-controlled oscillating circuit 70.

Referring to FIG. 12, the voltage-controlled oscillating circuit 70 has a ring oscillator constructed from inverters at three stages. The ring oscillator includes: an inverter formed of a P-channel transistor 51a and an N-channel transistor 51b; an inverter formed of a P-channel transistor 52a and an N-channel transistor 52b; and an inverter formed of a P-channel transistor 53a and an N-channel transistor 53b. Capacitors 51c, 52c and 53c to determine a delay value of the ring oscillator are coupled with output nodes of the respective inverters.

The voltage-controlled oscillating circuit 70 includes: a P-channel transistor 54 receiving a fixed voltage Vf at the gate thereof; a P-channel transistor 55 receiving a control voltage Vc at the gate thereof; and N-channel transistors 56 and 57 constituting a current mirror circuit.

The voltage-controlled oscillating circuit 70 further includes: P-channel transistors 59, 60 and 61 each, coupled between a corresponding one of the inverters at three stages and a power source node supplying a power source voltage Vdd, and for controlling operating currents supplied to the respective inverters; and a transistor 58 constituting a current mirror circuit together with the transistor 59.

The voltage-controlled oscillating circuit 70 still further includes: N-channel transistors 62, 63 and 64 each, coupled between a corresponding one of ground nodes supplying a ground voltage Vss and a corresponding one of the inverters.

In the voltage-controlled oscillating circuit 70, the ring oscillator constituted of the inverters at three stages performs an oscillating operation. An oscillating frequency of the ring oscillator is determined in the following way.

Into the transistor 56, there flows the sum of a current flowing between the drain and source of the transistor 54 receiving the fixed voltage Vf at the gate thereof and a current flowing between the drain and source of the transistor 55 receiving the control voltage Vc at the gate thereof. The current flowing between the drain and source of the transistor 55 is controlled by the controlled voltage Vc.

Since the transistors 56 and 57 constitute a current mirror circuit, currents equal to each other flow through the respective transistors 56 and 57 and the current of the transistor 57 flows through the transistor 58. Since the transistors 58 and 59 constitute a current mirror circuit, duplicated current flows through the transistor 59. Furthermore, into the P-channel transistors 60 and 61 for current controlling, there flow currents proportional to respective size ratios of the transistors 60 and 61 to the transistor 59 (or the transistor 58). Likewise, into the N-channel transistors 62, 63 and 64 for current controlling, there flow currents proportional to respective size ratios of the transistors 62, 63 and 64 to the transistor 57 (or the transistor 56).

In such a configuration, an oscillating frequency is determined by operating currents flowing through the respective inverters at three stages constituting the ring oscillator and values of the delay capacitors 51c, 52c and 53c. The capacitors 51c, 52c and 53c determine delay times at the respective stages as load capacitances of the respective inverters constituting the ring oscillator.

Hence, an oscillating frequency of the voltage-controlled oscillating circuit 70 is altered by changing the control voltage Vc inputted to the gate of the transistor 55 to change each of operating currents flowing through the respective inverters constituting the ring oscillator. Furthermore, since operating currents flowing through the respective inverters of the ring oscillator are also altered by changing a set value of the fixed voltage Vf inputted to the transistor 54; therefore, an oscillating frequency differs under the same control voltage Vc applied. In other words, obtained are a plurality of oscillating frequency vs. control voltage Vc characteristics with a fixed voltage Vf as a parameter.

However, the prior art voltage-controlled oscillating circuit 70 determines operating currents for the respective inverters constituting the ring oscillator through voltage to current conversion according to the inputted control voltage Vc. As a result, a clock CLK0 having an oscillating frequency corresponding to operating currents of the inverters is outputted from the ring oscillator.

Therefore, since a configuration is adopted of controlling an oscillating operation of the ring oscillator by a current value, it is difficult to broaden an oscillating frequency range. For this reason, it is also difficult to realize a PLL with a wide lock range even if a PLL circuit is constructed using such as voltage-controlled oscillating circuit.

Moreover, as a typical cause for jitter (phase deviation) occurring in a clock generated by the PLL circuit, there can be named noise on a power source voltage pulse (hereinafter simply referred to as power source noise).

At this point, referring again to FIG. 12, when noise occurs in the power source voltage Vdd supplied by the

power source node, source voltages of the current control P-channel transistors 58, 59, 60 and 61 are directly varied; therefore, an influence of the power source noise is directly exerted on operating currents for the inverters constituting the ring oscillator, with the result that an oscillating frequency of the voltage-controlled oscillating circuit 70 is also affected directly by the power source noise.

Therefore, a regulator circuit or a filter circuit for reducing power source noise was required for use of the prior art voltage control oscillating circuit 70.

FIG. 13 is a circuit diagram representing a configuration of a filter circuit provided correspondingly to a power source voltage of the voltage-controlled oscillating circuit 70.

Referring to FIG. 13, a filter circuit 71 includes: a smoothing capacitance 72 coupled between the power source node 75 and the ground node supplying the ground voltage Vss; and a resistance element 73 coupled in series with the power source node 75. The filter circuit 71 prevents a high frequency component superimposed on the power source Vdd, that is noise, from being transmitted to the power source node 75 using a low pass filter formed by the smoothing capacitance 72 and the resistance element 73.

However, in the case where such a filter circuit 71 is employed, a voltage level of the power source node 75 drops when a value of the resistance element 73 is large. Hence, in order that a cut-off frequency determined by a product of a resistance value of the resistance element 71 and a capacitance value of the smoothing capacitance 72 is made sufficiently low, a capacitance value of the smoothing capacitance 72 has to be larger. As a result, an occupancy area of the smoothing capacitance 72 increases, which produces a problem that layout design becomes limited.

#### SUMMARY OF THE INVENTION

It is an object of the present invention to provide configurations of a voltage-controlled oscillating circuit having a wide output frequency range and capable of suppressing an influence of power source noise and of a phase-locked loop circuit equipped with the voltage-controlled oscillating circuit.

The present invention will be summarized as follows: According to a first aspect of the present invention, the present invention is directed to a voltage-controlled oscillating circuit receiving supply of a power source voltage to operate and comprises: a voltage generating circuit; and a ring oscillator circuit. The voltage generating circuit sets a voltage level of a bias voltage according to a control voltage inputted from outside. The voltage generating circuit includes: an operational amplifier, which is an amplifier of a single-stage configuration, and receiving supply of the power source voltage to operate. The operational amplifier has: first and second input terminals electrically coupled with one of the control voltage and a reference voltage and the other of the voltages, respectively; and an output terminal outputting the bias voltage. The voltage generating circuit further includes: a feedback circuit coupled between the output terminal and one of the first and second input terminals. The ring oscillator circuit generates a clock having a frequency corresponding to the bias voltage. The ring oscillator circuit has an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of the bias voltage to operate.

Hence, a main advantage of the present invention is in that an oscillating frequency of the ring oscillator is controlled by the bias voltage generated by the voltage generating circuit including a single-stage operational amplifier excel-

lent in frequency characteristics; therefore, there can be realized a voltage-controlled oscillating circuit excellent in frequency characteristics and capable of generating a clock with a small variation in phase in a stable way.

According to a second aspect of the present invention, the present invention is directed to a voltage-controlled oscillating circuit receiving a power source voltage to operate and comprises: a voltage generating circuit; and a ring oscillator circuit. The voltage generating circuit receives a control voltage and amplifies the control voltage at a prescribed amplification factor to generate a bias voltage of a voltage level different from that of the control voltage. The ring oscillator circuit generates a clock having a frequency according to that of the bias voltage. The ring oscillator circuit has an odd number of inverters interconnected in a closed ring and receives supply of the bias voltage at each of the converters to operate.

Hence, in the voltage-controlled oscillating circuit according to the present invention, an oscillating frequency of the ring oscillator is controlled by the bias voltage generated by the voltage shifting circuit including the operational amplifier. Therefore, an adverse influence due to power source noise can be suppressed to perform stable generation of a clock having a small variation in phase.

According to a third aspect of the present invention, the present invention is directed to a phase-locked loop circuit generating an output clock for operating an internal circuit in synchronism with a reference clock and comprises: a phase comparator circuit; a control circuit; and a voltage-controlled oscillating circuit. The phase comparator circuit compares the reference clock with a feedback clock from the internal clock. The control circuit sets a voltage level of a control voltage based on a phase comparison result of the phase comparator circuit. The voltage-controlled oscillating circuit receives supply of a power source voltage to operate and supply the output clock having a frequency according to the control voltage to the internal circuit. The voltage-controlled oscillating circuit includes: a voltage generating circuit setting a voltage level of a bias voltage according to the control voltage. The voltage generating circuit has: an operational amplifier, which is an amplifier of a single-stage configuration, and receiving supply of the power source voltage to operate. The operational amplifier has: first and second input terminals electrically coupled with one of the control voltage and a reference voltage and the other of the voltages, respectively; and an output terminal outputting the bias voltage. The voltage generating circuit further includes: a feedback portion coupled between the output terminal and one of the first and second terminals. The voltage-controlled oscillating circuit further includes: a ring oscillator circuit generating a clock, as the output clock, having a frequency according to that of the bias voltage. The ring oscillator circuit has: an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of the bias voltage to operate.

Furthermore, a phase-locked loop circuit according to the present invention controls an oscillating frequency of an output clock of the voltage-controlled oscillating circuit with the bias voltage generated by the voltage generating circuit including the operational amplifier excellent in frequency characteristics. Therefore, an adverse influence can be suppressed that would otherwise be exerted on the output clock by power source noise without affecting stability of the entire phase-locked loop circuit.

The foregoing and other objects, features, aspects and advantages of the present invention will become more

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apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram showing a configuration of a phase-locked loop circuit 1 according to an embodiment of the present invention;

FIG. 2 is a circuit diagram representing a configuration of a voltage-controlled oscillating circuit 10 in the embodiment;

FIG. 3 is a conceptual diagram representing frequency characteristics of operational amplifiers;

FIG. 4 is a block diagram representing a configuration of a voltage-controlled oscillating circuit 30 according to a second embodiment of the present invention;

FIG. 5 is a circuit diagram for representing another example configuration of a filter circuit 31;

FIG. 6 is a block diagram representing a configuration of a voltage-controlled oscillating circuit 40 according to a third embodiment of the present invention;

FIGS. 7A to 7D are conceptual diagrams describing an influence of power source noise in operation of an operational amplifier 12;

FIG. 8 is a diagram for representing another example configuration of a filter circuit 35;

FIG. 9 is a block diagram representing a configuration of a voltage-controlled oscillating circuit 50 according to a fourth embodiment of the present invention;

FIG. 10 is a block diagram representing a configuration of a voltage-controlled oscillating circuit 52 according to a modification of the fourth embodiment;

FIG. 11 is a circuit diagram representing an example configuration of an operational amplifier 12 according to a fifth embodiment of the present invention;

FIG. 12 is a circuit diagram representing a configuration of the prior art voltage-controlled oscillating circuit 70; and

FIG. 13 is a circuit diagram representing a configuration of a filter circuit provided correspondingly to a power source voltage of the voltage-controlled oscillating circuit 70.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed description will be given of embodiments of the present invention below with reference to the accompanying drawings. Note that the same symbols used in views of the drawings indicate the same or corresponding constituents.

##### First Embodiment

Referring to FIG. 1, a phase-locked loop circuit 1 according to the embodiment of the present invention controls an output clock CLKO supplied to an internal circuit 4 such that a feedback clock FBCLK feedback from the internal circuit 4 and an input clock CLKI are synchronized with each other. By doing so, a delay occurring in the internal circuit 4 is compensated and the internal circuit 4 can be operated in synchronism with the input clock CLKI.

The phase-locked loop circuit 1 includes: a phase comparator circuit 2 comparing the input clock CLKI and the feedback clock FBCLK; a control circuit 3 outputting a control voltage Vcn according to a phase comparison result of the phase comparator circuit 2; and a voltage-controlled oscillating circuit 10 generating an output clock CLKO

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having an oscillating frequency according to the control voltage Vcn. The voltage-controlled oscillating circuit 10 receives supply of a power source voltage Vdd from a power source line 5 to operate.

The output clock CLKO is supplied to the internal circuit 4 as an operating clock. The output clock CLKO is supplied to the phase comparator circuit 2 via one or more driver circuits 9 in the internal circuit 4 as a feedback clock FBCLK. Note that the output clock CLKO can also be used directly as the feedback clock FBCLK without passing through the driver circuit or circuits 9.

Referring to FIG. 2, the voltage-controlled oscillating circuit 10 includes: a bias voltage generating circuit 11 outputting a bias voltage Vos according to the control voltage Vcn; and a ring oscillator circuit 20 receiving supply of the bias voltage Vos to operate.

The ring oscillator circuit 20 has  $(2n+1)$  inverters 21 wherein  $n$  is a natural number, coupled in series. The inverters are interconnected in a closed ring and an output of an inverter at the final stage is feedback to the input node of an inverter at the first stage. The inverters 21 each receive the bias voltage Vos from a bias voltage line 6 and the ground voltage Vss from a ground line 7 and operate. The inverters 21 each have a pair of a P-channel transistor 22a and an N-channel transistor 22b, which complementarily turn on/off.

A frequency fosc of the output clock CLKO outputted by the ring oscillator circuit 20 is given by  $fosc = 1 / ((2n+1)(Th+Tl))$ , wherein Th indicates a rise time of the transistor 22a constituting each of the inverters and Tl a fall time of the transistor 22b constituting each of the inverters. The rise time Th and fall time Tl of the respective transistors 22a and 22b alter according to change in the bias voltage Vos. As a result, the oscillating frequency fosc is controlled according to a voltage level of the bias voltage Vos.

The bias voltage generating circuit 11 includes: an operational amplifier 12 receiving supply of the power source voltage Vdd to operate; a resistance element 14 coupled between an output terminal 13c and inverting input terminal 13b of the operational amplifier 12; and a resistance element 15 coupled between the inverting input terminal 13b and the ground line 7. Resistance values of the resistance elements 14 and 15 are indicated by Rf and Rs, respectively.

The control voltage Vcn from the control circuit 3 is inputted to a non-inverting terminal 13a of the operational amplifier 12. The output terminal 13c of the operational amplifier 12 is coupled with a bias voltage line 6 supplying the bias voltage Vos.

With such a configuration adopted, the bias voltage generating circuit 11 operates as a non-inverting amplifier circuit using an operational amplifier. Hence, the bias voltage Vos is given by a formula (1) shown below.

$$Vos = (1 + Rf/Rs) \cdot Vcn \quad (1)$$

Hence, the bias voltage generating circuit 11 amplifies the control voltage Vcn at an amplification factor equal to or more than 1, which is determined by a ratio in resistance value between the resistance elements 14 and 15, to generate the bias voltage Vos. Therefore, when the bias voltage Vos is altered from the ground voltage Vss to the power source voltage Vdd, a range of the oscillating frequencies fosc of the ring oscillator circuit 20 can be made wide. Thereby, a lock range of the phase-locked loop circuit 1 on which the voltage controlled oscillating circuit 10 is implemented becomes also wide.

Furthermore, the bias voltage  $V_{os}$  receives no direct influence of noise-caused fluctuations in voltage level of the power source voltage  $V_{dd}$  on the power source line 5. Accordingly, an influence of power source noise is suppressed and the output clock CLK0 with a low level variation in phase can be stably generated without providing a large scaled filter circuit.

An operational amplifier generally employed is of a multi-stage configuration in which an amplification factor is highly thought of, typically, a two-stage configuration. In contrast to this, the operational amplifier 12 used in the embodiment of the present invention is of a single-stage configuration having a lower gain, but being more excellent in frequency characteristics than that of the multi-stage configuration.

In FIG. 3, a conceptual diagram for representing frequency characteristics of operational amplifiers is shown. In a case where the operational amplifier 12 is not of a multi-stage configuration, but of a single-stage configuration, a range in which an amplifying operation can be stably performed in a practical sense is extended toward the high frequency side as indicated by  $f_0 \rightarrow f_1$  in FIG. 3. In such a way, with employment of an amplifier of a single-stage configuration excellent in frequency characteristics, a voltage-controlled oscillating circuit excellent in frequency characteristics can be designed.

Note that as shown in FIG. 1, the phase-locked loop circuit 1 on which the voltage-controlled oscillating circuit is implemented constitutes a feedback system; therefore, it is necessary to sufficiently take stability of the entire system into consideration. While the present invention has an object to improve characteristics of a voltage-controlled oscillating circuit using an operational amplifier, there will arise a risk of adversely affecting stability of the entire phase-locked loop circuit due to the configuration including an operational amplifier adopted when a frequency characteristic of a voltage-controlled oscillating circuit is deteriorated down to a level which cannot be neglected as compared with other circuits in the phase-locked loop circuit 1, especially with the control circuit 3, with the result that there arise a need of a margin for ensuring stability, leading to loss of feasibility in designing a PLL circuit.

Hence, in order to compatibly achieve both aspects of the object of the present invention: improved characteristics of a voltage-controlled oscillating circuit and ensured stability of the entire phase-locked loop circuit, it is desirable that an operating amplifier of a single-stage configuration is used in a voltage-controlled oscillating circuit and thereby, an influence of frequency characteristics of the voltage-controlled oscillating circuit exerting on stability of the phase-locked loop circuit can be neglected.

#### Second Embodiment

Referring to FIG. 4, a voltage-controlled oscillating circuit 30 according to the second embodiment of the present invention differs from the voltage-controlled oscillating circuit 10 shown in FIG. 2 in that the circuit 30 further includes: a filter circuit 31 coupled with the bias voltage line 6.

The filter circuit 31 has a resistance element 32 coupled in series with the bias voltage line 6; and a capacitor 33 coupled between the bias voltage line 6 and the ground line 7. If a resistance value of the resistance element 32 and a capacitance value of the capacitor 33 are  $R$  and  $C$ , respectively, by definition, a cut-off frequency of the filter circuit is given by  $f_c = 1/(2\pi \cdot R \cdot C)$ . The filter circuit 31 is provided in order to remove a high frequency component of

the bias voltage  $V_{os}$ , that is noise, and further stabilize an oscillating frequency  $f_{osc}$  of the ring oscillator circuit 20. A configuration and operation of the other constituents combined of the voltage-controlled oscillating circuit 30 are similar to the case of the voltage-controlled oscillating circuit 10 shown in FIG. 2; therefore, neither of detailed descriptions thereof is repeated.

Referring to FIG. 5, the filter circuit 31 can be constituted of the capacitor 33 coupled between the bias voltage line 6 and the ground line 7. By forming the filter circuit 31 with the capacitor 33 only, a drop in voltage level of the bias voltage  $V_{os}$  can be prevented to ensure a wider oscillating frequency range.

#### Third Embodiment

Referring to FIG. 6, a voltage-controlled oscillating circuit 40 according to the third embodiment of the present invention differs from the voltage-controlled oscillating circuit 10 shown in FIG. 2 in that the circuit 40 further includes: a filter circuit 35 coupled with the power source line 5 in addition to the configuration of the circuit 10.

The filter circuit 35 is a low pass filter including: a resistance element 36 coupled in series with the power source line 5; and a capacitor 37 coupled between the power source line 5 and the ground line 7. The filter circuit 35 is provided in order to remove noise in the power source voltage  $V_{dd}$  supplied to the operational amplifier 12. A configuration and operation of the other constituents combined of the voltage-controlled oscillating circuit 40 are similar to the voltage-controlled oscillating circuit 10; therefore, neither of detailed descriptions thereof is repeated.

Next, description will be given of an influence of power source noise in operation of the operational amplifier 12 using FIGS. 7A to 7D.

In FIG. 7A, shown is a frequency response amplified by a feedback operation of the operational amplifier. Referring to FIG. 7A, a high frequency component of  $f_1$  or higher is amplified by the feedback operation of the operational amplifier.

In FIG. 7B, shown is an attenuation characteristic of a high frequency component in the operational amplifier. Referring to FIG. 7B, a frequency component of  $f_h$  or higher is attenuated. Hence, in combination of the frequency characteristics shown in FIGS. 7A and 7B, a frequency characteristic of the bias voltage generating circuit 11 using the operational amplifier 12 is given as shown in FIG. 7C. In such a way, the frequency response of the bias voltage generating circuit 11 comes to have a peak frequency  $f_p$  due to a difference between the frequency response caused by a feedback operation of the operational amplifier and the attenuation characteristic of a high frequency component therein.

Accordingly, in order to make a frequency characteristic of the bias voltage generating circuit 11 smooth as shown in FIG. 7D, the bias voltage generating circuit 11 requires to be provided with a low pass filter having a cut-off frequency corresponding to the peak frequency  $f_p$  on the power source line 5.

That is, in the filter circuit 35 shown in FIG. 6, when a resistance value  $R$  of the resistance element 36 and a capacitance value  $C$  of the capacitor 37 are designed such that  $f_p = 1/(2\pi \cdot R \cdot C)$ , a frequency characteristic of the bias voltage generating circuit 11 can be made ideal as shown in FIG. 7D.

In this case, since the power source voltage  $V_{dd}$  is not supplied directly to the ring oscillator 20, a cut-off frequency

of the filter circuit 35 can be set high compared with the prior art filter circuit 71 shown in FIG. 12. As a result, the filter circuit 35 can be smaller in size than the prior art filter circuit 71.

Furthermore, as described above, by adopting the operational amplifier 12 of a single-stage configuration excellent in frequency characteristics, the peak frequency  $f_p$  can be set to the higher frequency side. By doing so, a capacitance value  $C$  of the capacitance 37 in the filter circuit 35 can be smaller, thereby enabling the capacitor 37 to be smaller in size.

In such a way, with a down-sized filter circuit adopted, an influence of power source noise can be further suppressed to generate the output clock CLK0 stably in frequency and phase.

Referring to FIG. 8, the filter circuit 35 according to another example configuration includes: a power supply transistor 38 coupled in series with the power source voltage 5; and a capacitor 37 coupled between the power source line 5 and the ground line 7. To the gate of the power supply transistor 38, inputted is a control signal PWC for instructing execution and cease of supply of the power source voltage Vdd to the operational amplifier 12. Thereby, in a period when operation of the operational amplifier 12 is unnecessary, the control signal PWC is inactivated to turn off the power supply transistor 38, thus enabling power consumption of the voltage-controlled oscillating circuit 40 to decrease.

On the other hand, in a period when the operational amplifier 12 operates, the control signal PWC is activated to turn on the power supply transistor 38 and supply the power source voltage Vdd to the operational amplifier 12. In this case, a low pass filter similar to FIG. 6 can be formed of an on-resistance of the power supply transistor 38 and a capacitor 37. As a result, in addition to suppression of power source noise, power consumption can be lowered by power supply control without scaling-up of the filter circuit 35.

#### Fourth Embodiment

In the fourth embodiment, description will be given of a variation of configuration of an operational amplifier circuit constituted by the operational amplifier 12 in the bias voltage generating circuit 11.

Referring to FIG. 9, a voltage-controlled oscillating circuit 50 according to the fourth embodiment of the present invention differs from the voltage-controlled oscillating circuit 10 shown in FIG. 2 comparing therewith in that a bias voltage generating circuit 51 is provided instead of the bias voltage generating circuit 11. A configuration and operation of the other constituents combined of the voltage-controlled oscillating circuit 50 are similar to the voltage-controlled oscillating circuit 10; therefore, neither of descriptions thereof is repeated.

The output terminal 13c of the operational amplifier 12 is coupled directly with the inverting input terminal 13b. On the other hand, to the input terminal 13a of the operational amplifier 12, the control voltage Vcn from the control circuit 3 is inputted. Hence, the bias voltage generating circuit 51 operates as a so-called voltage follower circuit.

In the bias voltage generating circuit 51, the bias voltage Vos corresponds to a state where  $R_s \rightarrow \infty$  in the formula (1); therefore,  $V_{os} = V_{cn}$ . In such a way, the bias voltage generating circuit 51 does not amplify a voltage level of the control voltage Vcn, while being able to stably set the bias voltage Vos to the same level as the control voltage Vcn.

In an ideal case, an input impedance of the operational amplifier 12 increases to infinity but an output impedance

becomes 0; therefore, the bias voltage generating circuit 51 can stably generate the bias voltage Vos of the same level as the control voltage Vcn without suffering from influences of a circuit group connected thereto at the previous and subsequent stages.

Hence, by stably controlling the oscillating frequency fosc of the output clock CLK0 according to the control voltage Vcn, the output clock CLK0 having a small variation in phase can be generated.

#### Modification of the Fourth Embodiment

Referring to FIG. 10, a voltage-controlled oscillating circuit 52 according to the modification of the fourth embodiment differs from the voltage-controlled oscillating circuit 10 shown in FIG. 2 in configuration comparing therewith in that a bias voltage generating circuit 53 is included instead of the bias voltage generating circuit 11. A configuration and operation of the other constituents combined of the voltage-controlled oscillating circuit 52 are similar to the voltage-controlled oscillating circuit 10, therefore, neither of detailed descriptions thereof is repeated.

The bias voltage generating circuit 53 has two inverting amplifier circuits 16 connected in series to each other. An inverting amplifier circuit 16 includes: the operational amplifier 12; a resistance element 17 coupled between the output terminal 13c of the operational amplifier 12 and the inverting input terminal 13b thereof; and a resistance element 18 connected to the inverting input terminal 13b. The non-inverting input terminal 13a of the operational amplifier 12 is coupled with the ground line 7. The control voltage Vcn from the control circuit 3 is inputted to the inverting input terminal 13b via the resistance element 18.

In the inverting amplifier circuit 16, if resistance values of the resistance elements 17 and 18 are  $R_f$  and  $R_s$ , respectively, by definition, a relationship between an input voltage Vi corresponding to the control voltage Vcn and an output voltage Vo at the output terminal 13c is given by a formula (2) as follows:

$$V_o = -(R_f/R_s) \cdot V_i \quad (2)$$

In such a way, in each of the inverting amplifier circuits 16, the output voltage Vo is inverted from the input voltage Vi in polarity. Moreover, in this embodiment, an amplification factor of each of the inverting amplifier circuits 16 is set 1 or less. That is, a relation  $R_f \leq R_s$  is set.

Accordingly, by coupling the two (or an even number of) inverting amplifier circuits 16 in series to each other in such a way, a voltage value according to and lower than the control voltage Vcn can be supplied to the ring oscillator 20 as the bias voltage Vos.

Such a configuration is suited for a case where a range of oscillating frequencies in the ring oscillator circuit 20 is unnecessary to be so much wide but requirement is imposed of strict suppression of a variation in phase caused by power source noise. That is, by setting an amplification factor to 1 or less, an effect of suppressing an influence of power source noise is further enhanced.

Furthermore, it is possible that this case is not adopted where an even number of inverting amplifier circuits 16 are coupled in series cascade, but a configuration is adopted where a ring oscillator circuit with converted polarity arrangement is driven by a single inverting amplifier circuit 16.

With such a configuration adopted, a case can be coped with where a range of oscillating frequencies is narrow and requirement is imposed of strict suppression of a variation in phase due to an influence of power source noise or the like.

## 11

## Fifth Embodiment

In the fifth embodiment, description will be given of a configuration of the operational amplifier 12 excellent in frequency characteristics employed in this embodiment of the present invention.

In FIG. 11, shown is an example configuration of an operational amplifier 12 according to this embodiment of the present invention.

In FIG. 11, shown is a configuration of an operational amplifier having a circuit configuration of a so-called folded cascode type.

Referring to FIG. 11, the operational amplifier 12 has a differential amplifier portion 41 differentially amplifying and converting a voltage difference between the non-inverting input terminal 13a and the inverting input terminal 13b into voltage levels at nodes N1 and N2; a first cascode amplifier portion 42 for forming a current path between the power source line 5 and the node N1; and a second cascode amplifier portion 43 for forming a current path between the power source line 5 and the node N2.

The differential amplifier portion 41 has: a P-channel transistor 44 electrically coupled between the power source line 5 and a node N0; a P-channel transistor 45a electrically coupled between the nodes N0 and N1 and having the gate coupled with the non-inverting input terminal 13a; and a P-channel transistor 45b electrically coupled between the nodes N0 and N2 and having the gate coupled with the inverting input terminal 13b.

The differential amplifier portion 41 further has: N-channel transistors 49a and 49b each electrically coupled between a corresponding one of the nodes N1 and N2, and the ground line 7. A common bias voltage V<sub>bd</sub> are inputted to the gates of the transistors 49a and 49b.

The first cascode amplifier portion 42 has: P-channel transistors 46a and 47a electrically coupled in series between the power source line 5 and a node N3; and an N-channel transistor 48a electrically coupled between the nodes N3 and N1.

The second cascode amplifier portion 43 has: P-channel transistors 46b and 47b electrically coupled in series between the power source line 5 and the output terminal 13c outputting the bias voltage V<sub>os</sub>; and an N-channel transistor 48b electrically coupled between the output terminal 13c and the node N2.

The gates of the transistors 46a and 46b are coupled with the node N3. A common bias voltage V<sub>bb</sub> is inputted to the gates of the transistors 47a and 47b. A common bias V<sub>bc</sub> is inputted to the gates of the transistors 48a and 48b. Hence, a current i<sub>2</sub> flowing through the transistors 46b, 47b and 48b in this order is proportional to a current i<sub>1</sub> flowing through the transistors 46a, 47a and 48a in this order. A proportion constant is determined according to a current drive ability ratio of the transistors.

The transistors 45a and 45b differentially operate according to voltage levels of the non-inverting input terminal 13a and the inverting input terminal 13b to alter voltage levels of the respective nodes N1 and N2. To be concrete, when a voltage level of the non-inverting input terminal 13a transitions to the relatively high side, then a voltage level of the node N1 goes low, while to the contrary, a voltage level of the node N2 goes high. To the contrary to this, when a voltage level of an input of the non-inverting input terminal 13a transitions to the relative low side, then voltage levels of the respective nodes N1 and N2 shift to the high side and the low side, respectively.

## 12

The current i<sub>1</sub> and i<sub>2</sub> alter according to a voltage level of the node N1. When a voltage level of the non-inverting input terminal 13a goes relatively high, the currents i<sub>1</sub> and i<sub>2</sub> increase to raise a voltage of the output terminal 13c, that is to raise the bias voltage V<sub>os</sub>. To the contrary, when a voltage level of the non-inverting input terminal 13a goes relatively low, the currents i<sub>1</sub> and i<sub>2</sub> decrease to lower the bias voltage V<sub>os</sub> as well.

In such a way, by adopting a circuit configuration of a folded cascode type, a gain (an amplification factor) can be attainable large in a single-stage operational amplifier low in possibility of oscillation.

Furthermore, current drive abilities of the transistors 45a, 46a, 47a, 48a and 49a for defining voltage levels of the nodes N1 and N3 can be set lower compared with the transistors 45b, 46b, 47b, 48b and 49b for defining voltage levels of the output terminal 13c generating the bias voltage V<sub>os</sub> and the associated node N2. Generally speaking, adjustment of a current drive ability can be realized by adjusting a design of a transistor size. Accordingly, by reducing transistor sizes of the transistors 45a to 49a, a layout area of the operational amplifier 12 can be decreased.

Note that in the circuit configuration shown in FIG. 11, a configuration can be adopted where each of the transistors is inverted in polarity and the power source line 5 and the ground line 7 are interchanged therebetween in role. To be concrete, N-channel transistors are adopted as the transistors 44, 45a, 45b, 46a, 46b, 47a and 47b, while P-channel transistors are adopted as the transistors 48a, 48b, 49a and 49b, and furthermore, not only is a line to which the transistors 44, 46a and 46b are connected altered from the power source line 5 to the ground line 7, but a line to which the transistors 49a and 49b are connected is also altered from the ground line 7 to the power source line 5. Even in such a configuration, a similar function of the operational amplifier 12 shown in FIG. 11 can be realized.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A voltage-controlled oscillating circuit receiving supply of a power source voltage to operate comprising:

a voltage generating circuit setting a voltage level of a bias voltage according to a control voltage being different from said power source voltage inputted from the outside,

said voltage generating circuit including an operational amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,

said operational amplifier having

first and second input terminals, wherein one of said first and second input terminals is electrically coupled with said control voltage, and

an output terminal outputting said bias voltage, and said voltage generating circuit further including a) a feedback portion coupled between said output terminal and another one of said first and second input terminals and b) a non-inverting amplifier circuit using said operational amplifier receiving supply of said power source voltage to operate; and

a ring oscillator circuit generating a clock having a frequency corresponding to said bias voltage, and having an odd-number of inverters, interconnected in



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- a closed ring, and each inverter receiving supply of said bias voltage to operate, wherein each of said inverters includes a p-channel MOS transistor receiving said bias voltage at its source electrode.
2. A voltage-controlled oscillating circuit receiving supply of a power source voltage to operate comprising:
- a voltage generating circuit setting a voltage level of a bias voltage according to a control voltage being different from said power source voltage inputted from the outside,
  - said voltage generating circuit including an operational amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,
  - said operational amplifier having
    - first and second input terminals, wherein one of said first and second input terminals is electrically coupled with said control voltage, and
    - an output terminal outputting said bias voltage, and
    - said voltage generating circuit further including a) a feedback portion coupled between said output terminal and another one of said first and second input terminals and b) an inverting amplifier circuit using said operational amplifier receiving supply of said power source voltage to operate; and
    - a ring oscillator circuit generating a clock having a frequency corresponding to said bias voltage, and having an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of said bias voltage to operate, wherein each of said inverters includes a p-channel MOS transistor receiving said bias voltage at its source electrode.
3. The voltage-controlled oscillating circuit according to claim 1 or 2, further comprising:
- a bias voltage line, provided between said voltage generating circuit and said ring oscillator circuit and transmitting said bias voltage; and
  - a low pass circuit, coupled with said bias voltage line, and for removing a high frequency component of said bias voltage.
4. The voltage-controlled oscillating circuit according to claim 1 or 2, further comprising:
- a low pass circuit, coupled between a node supplying said power source voltage and said voltage generating circuit, and for removing a high frequency component of said power source voltage.
5. The voltage-controlled oscillating circuit according to claim 4, wherein a cut-off frequency of said low pass circuit is set according to frequency characteristics of said operational amplifier.
6. The voltage controlled oscillating circuit according to claim 1 or 2, wherein said operational amplifier further includes:
- a differential amplifier portion, coupled between a first power source node supplying one of a ground voltage and said power source voltage and a second power source node supplying the other of said ground voltage and said power source voltage, and amplifying and converting a voltage difference between said first and second input terminals into a voltage difference between first and second nodes;
  - a first cascode amplifier portion forming a first current path between said first power source node and said first node; and
  - a second cascode amplifier portion forming a second current path between said first power source node and said second node, wherein

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- said output terminal is provided on said second current path,
- said first cascode amplifier portion alters a first current amount passing through said first current path according to a voltage level of said first node, and
- said second cascode amplifier portion alters a second current amount passing through said second current path in proportion to said first current amount.
7. The voltage-controlled oscillating circuit according to claim 6, wherein said first current amount is smaller than said second current amount.
8. The voltage-controlled oscillating circuit according to claim 6, wherein
- said differential amplifier portion has:
- a first transistor, electrically coupled between said first power source node and said first node, and having a control terminal coupled with said first input terminal;
  - a second transistor, electrically coupled between said first power source node and said second node, and having a control terminal coupled with said second input terminal;
  - a third transistor, electrically coupled between said first node and said second power source node, and receiving a first voltage at a control terminal thereof; and
  - a fourth transistor, electrically coupled between said second node and said second power source node, and receiving said first voltage at a control terminal thereof;
- wherein
- said first cascode amplifier portion has:
- a fifth transistor, electrically coupled between said first power source node and a third node, and having a control terminal coupled with said third node; and
  - a sixth transistor, electrically coupled between said first node and said third node, and receiving a second voltage at a control terminal thereof;
- and wherein
- said second cascode amplifier portion has:
- a seventh transistor, electrically coupled between said first power source node and said output terminal, and having a control terminal coupled with said third node; and
  - an eighth transistor, electrically coupled between said second node and said output terminal, and receiving said second bias voltage at a control terminal thereof.
9. The voltage-controlled oscillating circuit according to claim 8, wherein
- said first, third, fifth and sixth transistors have a first current drive ability and
  - said second, fourth, seventh and eighth transistors have a second current drive ability, said first current drive ability being smaller than said second current drive ability.
10. A voltage-controlled oscillating circuit receiving a power source voltage to operate, comprising:
- a voltage generating circuit receiving a control voltage and amplifying the control voltage at a prescribed amplification factor to generate a bias voltage of a voltage level different from that of said control voltage; and
  - a ring oscillator circuit generating a clock having a frequency according to that of said bias voltage, and having an odd number of inverters interconnected in a

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closed ring and receives supply of said bias voltage at each of said inverters to operate, wherein said amplification factor is larger than 1, and said voltage generating circuit includes a non-inverting amplifier circuit using an operational amplifier receiving supply of said power source voltage to operate.

11. A voltage-controlled oscillating circuit receiving a power source voltage to operate, comprising:

a voltage generating circuit receiving a control voltage and amplifying the control voltage at a prescribed amplification factor to generate a bias voltage of a voltage level different from that of said control voltage; and

a ring oscillator circuit generating a clock having a frequency according to that of said bias voltage, and having an odd number of inverters interconnected in a closed ring and receives supply of said bias voltage at each of said inverters to operate, wherein said amplification factor is small than 1, and said voltage generating circuit includes an inverting amplifier circuit using an operational amplifier receiving supply of said power source voltage to operate.

12. The voltage-controlled oscillating circuit according to claim 10 or 11, further comprising:

a bias voltage line, provided between said voltage generating circuit and said ring circuit, and transmitting said bias voltage; and

a low pass circuit, coupled with said bias voltage line, and for removing a high frequency component of said bias voltage.

13. The voltage-controlled oscillating circuit according to claim 10 or 11, further comprising:

a low pass circuit, coupled between a node supplying said power source voltage and said voltage generating circuit, and for removing a high frequency component of said power source voltage.

14. A phase-locked loop circuit generating an output clock for operating an internal circuit in synchronism with a reference clock, comprising:

a phase comparator circuit comparing said reference clock with a feedback clock from said internal clock;

a control circuit setting a voltage level of a control voltage based on a phase comparison result of said phase comparator circuit; and

a voltage-controlled oscillating circuit receiving supply of a power source voltage being different from said control voltage to operate and supply said output clock having a frequency according to said control voltage to said internal circuit,

said voltage-controlled oscillating circuit including a voltage generating circuit setting a voltage level of a bias voltage according to said control voltage,

said voltage generating circuit having an operational amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,

said operational amplifier having

first and second input terminals, wherein one of said first and second input terminals is electrically coupled with said control voltage, and

an output terminal outputting the bias voltage, and said voltage generating circuit further having

a feedback portion coupled between said output terminal and another one of said first and second input terminals, and

said voltage-controlled oscillating circuit further including a ring oscillator circuit generating a clock, as said output clock, having a frequency correspond-

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ing to that of said bias voltage, said ring oscillator circuit having an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of said bias voltage to operate.

15. The phase-locked loop circuit according to claim 14, wherein the one of said first and second input terminals is electrically coupled with said control voltage via a resistor.

16. The phase-locked loop circuit according to claim 14, wherein an other one of said first and second input terminals is electrically coupled with a reference voltage.

17. The phase-locked loop circuit according to claim 14, wherein each of said inverters includes a p-channel MOS transistor receiving said bias voltage at its source electrode.

18. A voltage-controlled oscillating circuit receiving supply of a power source voltage to operate comprising:

a voltage generating circuit setting a voltage level of a bias voltage according to a control voltage being different from said power source voltage inputted from the outside,

said voltage generating circuit including an operational amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,

said operational amplifier having

first and second input terminals, wherein one of said first and second input terminals is electrically coupled with said control voltage, and

an output terminal outputting said bias voltage, and said voltage generating circuit further including a feedback portion coupled between said output terminal and another one of said first and second input terminals; and

a ring oscillator circuit generating a clock having a frequency corresponding to said bias voltage, and having an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of said bias voltage to operate, wherein the one of said first and second input terminals is electrically coupled with said control voltage via a resistor.

19. A voltage-controlled oscillating circuit receiving supply of a power source voltage to operate comprising:

a voltage generating circuit setting a voltage level of a bias voltage according to a control voltage being different from said power source voltage inputted from the outside

said voltage generating circuit including an operational amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,

said operational amplifier having

first and second input terminals, wherein one of said first and second input terminals is electrically coupled with said control voltage, and

an output terminal outputting said bias voltage, and said voltage generating circuit further including a feedback portion coupled between said output terminal and another one of said first and second input terminals; and

a ring oscillator circuit generating a clock having a frequency corresponding to said bias voltage, and having an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of said bias voltage to operate, wherein an other one of said first and second input terminals is electrically coupled with a reference voltage.

20. A voltage-controlled oscillating circuit receiving supply of a power source voltage to operate comprising:

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voltage generating circuit setting a voltage level of a bias voltage according to a control voltage being different from said power source voltage inputted from the outside,

said voltage generating circuit including an operational 5 amplifier, which is an amplifier of a single stage configuration, and receiving supply of said power source voltage to operate,

said operational amplifier having

first and second input terminals, wherein one of said 10 first and second input terminals is electrically coupled with said control voltage, and

an output terminal outputting said bias voltage, and

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said voltage generating circuit further including a feedback portion coupled between said output terminal and another one of said first and second input terminals; and

a ring oscillator circuit generating a clock having a frequency corresponding to said bias voltage, and having an odd-number of inverters, interconnected in a closed ring, and each inverter receiving supply of said bias voltage to operate, wherein each of said inverters includes a p-channel MOS transistor receiving said bias voltage at its source electrode.

\* \* \* \* \*

**United States Patent** [19]  
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[54] **RECIRCULATING MOS CHARGE PUMP**

[75] **Inventors:** Herchel A. Vaughn; Joe W. Peterson,  
both of Austin, Tex.

[73] **Assignee:** Motorola, Inc., Schaumburg, Ill.

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[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,047,091 9/1977 Hutchines et al. .... 363/59  
4,053,821 10/1977 Hose et al. .... 363/60

**FOREIGN PATENT DOCUMENTS**

9571 1/1983 Japan ..... 363/60

*Primary Examiner*—William H. Beha, Jr.

*Attorney, Agent, or Firm*—Anthony J. Sarli, Jr.; Jeffrey  
Van Myers; Robert L. King

[57] **ABSTRACT**

A charge pump which can operate at low supply voltages is provided. The charge pump recirculates charge in response to an alternating clock signal which alternates the charge across a plurality of charge storage devices. Charge recirculation is used to compensate for threshold voltage drops associated with diodes or diode-configured transistors used to implement the charge pump. As a result, voltage amplification can occur in the charge pump even for small power supply values.

**12 Claims, 2 Drawing Figures**

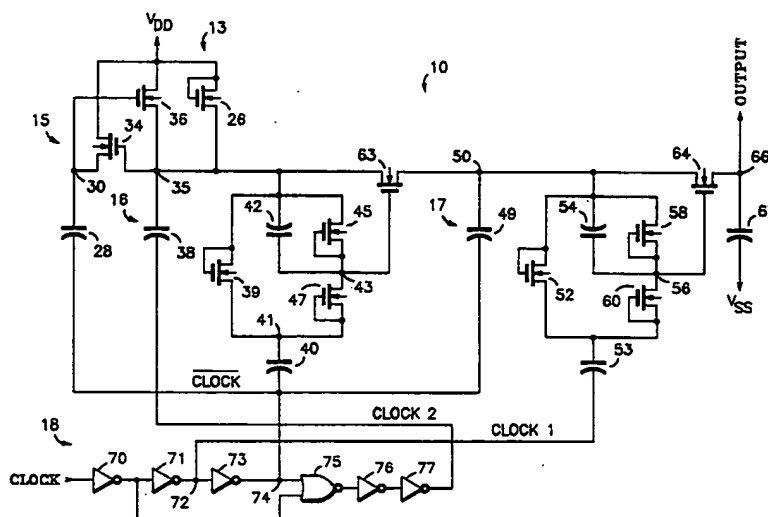
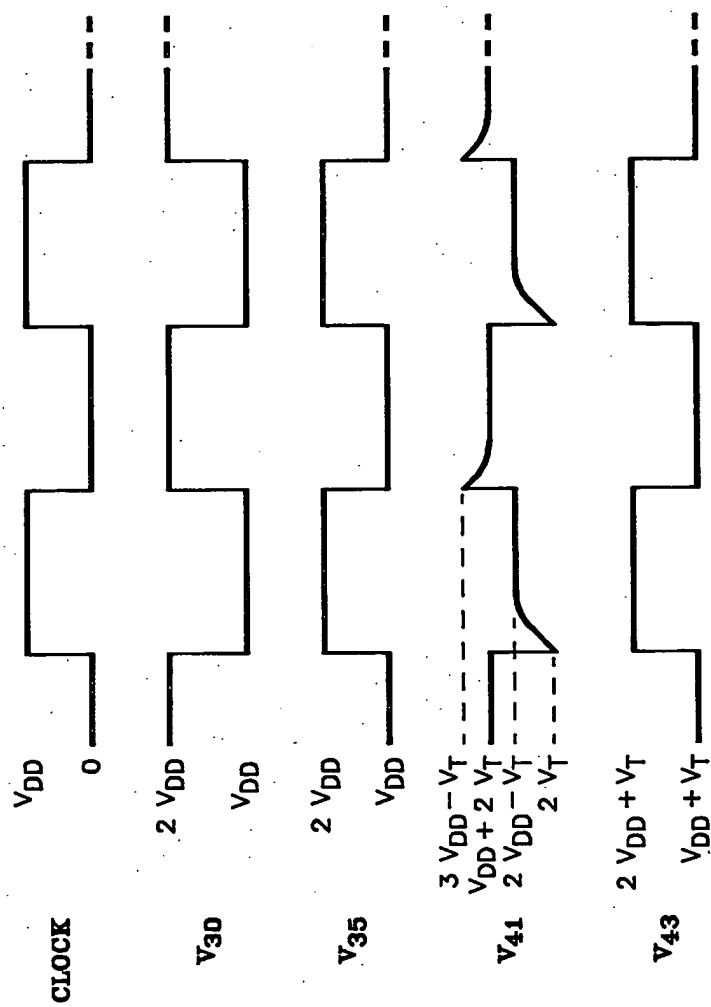




FIG. 2



## RECIRCULATING MOS CHARGE PUMP

### TECHNICAL FIELD

This invention relates generally to analog circuits requiring operating voltages greater than available power supply voltages, and more particularly, to charge pump circuits.

### BACKGROUND ART

Analog circuits are typically being designed to operate at low power supply voltages such as five volts. Although five volts is a commonly found power supply voltage level, power supply voltages of three volts and less are more desirable for battery operated circuits where power consumption is critical. Even in automotive applications where higher supply voltages are typically present, three volt power supply operation is desirable due to the wide variation of battery voltage which is possible. Typical analog circuits including analog switches however require a voltage greater than three volts to be operational. Therefore, a charge pump which functions to boost the level of the power supply for predetermined portions of a circuit must be utilized. Conventional charge pump circuits utilize diodes which are typically implemented by diode configured N-channel transistors in MOS circuits. A disadvantage with previous charge pump circuits results from a threshold voltage drop which is present across a diode or diode configured transistor. The threshold voltage drop decreases the output voltage of the charge pump by the threshold voltage value and may drastically reduce the efficiency of the charge pump. The reduced efficiency may be a critical factor when supply voltages of three volts or less are used because the threshold voltage of a diode becomes a significant portion of the power supply voltage. As a result, known charge pump circuits are not reliable for power supply potentials of three volts and less.

### BRIEF DESCRIPTION OF THE INVENTION

Accordingly, an object of the present invention is to provide an improved charge pump circuit.

Another object of the present invention is to provide an improved charge pump circuit for use with power supply voltages less than five volts.

Yet another object of the present invention is to provide an improved CMOS recirculating charge pump which substantially eliminates the effects of undesirable threshold voltage drops.

In carrying out the above and other objects of the present invention, there is provided, in one form, a circuit for increasing a power supply voltage from a power supply source and providing a boosted output voltage at an output terminal. A diode is coupled between a supply terminal for receiving the power supply voltage and the output terminal. The diode has a predetermined threshold voltage drop associated therewith and prevents current flow from the output terminal to the power supply source. Charge storage means are selectively coupled via a coupling device also having a threshold voltage drop to the output terminal. The charge storage means selectively store the power supply voltage and a boost voltage to provide the boosted output voltage. Compensation means are coupled to the diode, to the coupling device and to the charge storage means for providing compensation for the threshold

voltage drops. Therefore, the threshold voltage drops do not degrade the performance of the charge pump.

These and other objects, features and advantages will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates in partial schematic form a charge pump circuit in accordance with the present invention; and

FIG. 2 illustrates in schematic form voltage waveforms associated with the circuit of FIG. 1.

### DETAILED DESCRIPTION OF THE INVENTION

Shown in FIG. 1 is a charge pump 10 generally comprising diode portion 13, pump portions 15, 16 and 17 and clock portion 18. It should be understood that although specific N-channel and P-channel MOS devices are shown, charge pump 10 may be implemented by completely reversing the processing techniques (e.g. N-channel to P-channel) or by using other types of transistors.

Diode portion 13 generally comprises a diode configured N-channel transistor 26 having both a gate and a drain connected to power supply  $V_{DD}$ . It should also be apparent that other known semiconductor structures which function as a diode may be used in place of a diode configured MOS transistor.

Pump portion 15 generally comprises a capacitor 28 having a first electrode connected to a node 30. A second electrode of capacitor 28 is connected to a complement of a clock signal. An N-channel transistor 34 has a drain connected to power supply  $V_{DD}$ , a gate connected to a node 35, and a source connected to node 30. An N-channel transistor 36 has a drain connected to power supply  $V_{DD}$ , a gate connected to node 30, and a source connected to node 35.

Pump portion 16 generally comprises a capacitor 38 having a first electrode connected to node 35, and a second electrode connected to a clock signal labeled "CLOCK 2". An N-channel transistor 39 has a drain and a gate connected together to node 35. A source of transistor 39 is connected to a first electrode of a capacitor 40 at a node 41. A second electrode of capacitor 40 is connected to a complement of the clock signal. A first electrode of a capacitor 42 is connected to node 35, and a second electrode of capacitor 42 is connected to a node 43. An N-channel transistor 45 has a source connected to node 35, and both a gate and a drain connected together to node 43. A source of an N-channel transistor 47 is connected to node 43, and both a gate and a drain of transistor 47 are connected to the first electrode of capacitor 40 at node 41.

Pump portion 17 generally comprises a capacitor 49 having a first electrode connected to a node 50, and a second electrode connected to the complement of the clock signal. An N-channel transistor 52 has a drain and a gate connected together to node 50, and a source connected to a first electrode of a capacitor 53. A second electrode of capacitor 53 is connected to a clock signal labeled "CLOCK 1". A first electrode of a capacitor 54 is connected to node 50, and a second electrode of capacitor 54 is connected to a node 56. An N-channel transistor 58 has a source connected to node 50, and both a gate and a drain connected together to node 56. An N-channel transistor 60 has a source connected to

node 56, and both a drain and a gate connected together and coupled to the first electrode of capacitor 53.

An N-channel transistor 63 has a drain connected to node 35, a gate connected to node 43 and a source connected to node 50. An N-channel transistor 64 has a drain connected to node 50, a gate connected to node 56 and a source connected to an output terminal 66. A capacitor 67 has a first electrode connected to output terminal 66 and a second electrode connected to a second supply voltage, say  $V_{SS}$ . In the illustrated form, supply voltage  $V_{SS}$  is less positive than supply voltage  $V_{DD}$ .

Clock portion 18 generally comprises an inverter 70 having an input for receiving a clock signal labeled "CLOCK" and an output connected to an input of an inverter 71. An output of inverter 71 provides the "CLOCK 1" signal and is connected to the second electrode of capacitor 53 at a node 72 and is connected to an input of an inverter 73. An output of inverter 73 is connected to a first input of a NOR gate 75 at node 74. A second input of NOR gate 75 is connected to an output of inverter 70. An output of NOR gate 75 is connected to an input of an inverter 76 which has an output connected to an input of an inverter 77. An output of inverter 77 provides the "CLOCK 2" to the second electrode of capacitor 38.

Referring to associated waveforms in FIG. 2, the operation of charge pump 10 may be more readily understood. The waveforms of FIG. 2 represent steady state circuit conditions and do not illustrate initial start-up voltage conditions. Effects of parasitic capacitance are also not illustrated in the FIG. 2 waveforms but will be discussed below. A square wave clock signal which oscillates between zero volts or ground potential and the power supply voltage  $V_{DD}$  is coupled to the input of clock portion 18 at the input of inverter 70. For the purpose of explanation, assume that charge pump 10 is in a steady state of operation and that the clock signal is initially at a high logic level (i.e. the inverse clock is at zero volts) before transitioning to the zero volt potential. Since the inverse of the clock signal potential is coupled to capacitor 28, capacitor 28 charges to the supply voltage  $V_{DD}$  potential during this time period because node 30 is at the  $V_{DD}$  potential and the clock signal is at zero volts. Therefore, in addition to other circuit conditions to be explained below, the voltage at node 30 denoted as " $V_{30}$ " in FIG. 2 is initially at  $V_{DD}$ . However, the voltage at node 30 will be equal to  $2V_{DD}$  volts as shown in FIG. 2 during low cycles of the clock signal. The voltage  $2V_{DD}$  occurs at node 30 during low clock cycles in the following way. Simultaneous to the charging of capacitor 28 to  $V_{DD}$ , node 35 is being boosted above  $V_{DD}$  volts toward  $2V_{DD}$  by capacitor 38 and the CLOCK 2 signal. The threshold voltage drops associated with all of the diode configured transistors of charge pump 10 are each presumed substantially equal and each is designated by  $V_T$ . Therefore, node 35 is at a potential of approximately  $2V_{DD}$ . When the clock signal transitions to  $V_{DD}$ , the lower or second electrode of capacitor 28 is coupled to ground and node 30 initially transitions to  $V_{DD}$  volts. A very short delay period later, the CLOCK 2 signal is coupled as a high level signal to capacitor 38. In response, node 35 transitions from nearly  $V_{DD}$  to substantially  $2V_{DD}$ . The voltage potential at node 35 makes transistor 34 conductive which couples  $V_{DD}$  to node 30. Since node 35 is at a higher voltage than node 30, transistor 36 is nonconductive. When the clock signal transitions again to a low

level signal, the voltage at node 30 is increased by  $V_{DD}$  volts and returns to  $2V_{DD}$  volts. Simultaneously, node 35 drops  $V_{DD}$  volts to a potential of  $V_{DD}$ . Node 35 is pulled all the way to  $V_{DD}$  as a result of transistor 36 becoming conductive to directly couple the  $V_{DD}$  power supply terminal to node 35. The next half clock cycle when  $V_{DD}$  is coupled to the second electrode of capacitor 38, the node 35 potential approaches  $2V_{DD}$ . Therefore, capacitors 28 and 38 and transistors 34 and 36 function in combination to eliminate the effect of the threshold voltage drops between  $V_{DD}$  and node 35 and between  $V_{DD}$  and node 30. Transistor 26 functions to allow start-up of operation of transistors 34 and 36 and capacitors 28 and 38. The resulting voltage at node 35 varies between a full  $V_{DD}$  potential and a boosted  $2V_{DD}$  potential.

In operation, the boosted voltage of  $2V_{DD}$  at node 35 is selectively coupled to node 50 via coupling transistor 63 where the voltage is boosted another  $V_{DD}$  by capacitor 49. The voltage at node 50 is desired to vary between  $2V_{DD}$  and  $3V_{DD}$  and is selectively coupled to capacitor 67 when the voltage is  $3V_{DD}$ . Therefore, the output voltage is charged onto capacitor 67 and provided as a constant  $3V_{DD}$ . However, when the voltage at node 35 is coupled to node 50, the voltage at node 35 would be reduced by the threshold voltage drop of transistor 63 if transistor 63 were connected in a conventional diode configuration. Therefore, transistors 39, 45 and 47 and capacitors 40 and 42 function in combination to substantially eliminate the threshold voltage drop of transistor 63 so that the full potential of  $2V_{DD}$  is coupled to node 50.

In the illustrated form, the voltage at node 41 varies between four distinct voltage potentials as the complement clock signal varies between zero and  $V_{DD}$  volts. Assume that the CLOCK 2 signal is initially at  $V_{DD}$  and the complement clock signal at node 74 is at zero volts. The voltage potential of  $2V_{DD}$  at node 35 charges capacitor 40 via transistor 39 which is conductive. Therefore, the voltage at node 41 is  $(2V_{DD} - V_T)$ . When the CLOCK 2 signal transitions to zero volts and the complement clock signal is at  $V_{DD}$ , node 35 transitions to  $V_{DD}$  and node 41 is boosted to  $(3V_{DD} - V_T)$ . A voltage of substantially  $(2V_{DD})$  minus a threshold voltage drop ( $V_T$ ) exists across transistors 45 and 47. Capacitor 40 is therefore discharged via transistors 45 and 47 until node 41 reaches  $(V_{DD} + 2V_T)$  and node 43 reaches  $(V_{DD} + V_T)$ .

It should be readily apparent that a threshold voltage has been charged onto capacitor 42 when the clock signal is at zero volts. Since capacitor 42 is connected between the gate and drain of transistor 63, capacitor 42 pre-biases transistor 63 with a threshold voltage. Transistor 63 therefore functions as a diode configured transistor with no threshold voltage drop. If transistor 45 is fabricated with the same control electrode dimensions as transistor 63, transistors 45 and 63 have substantially the same threshold voltage. Therefore, the threshold voltage of transistor 45 which is stored onto capacitor 42 provides the correct bias across the gate and source of transistor 63 to cancel the threshold voltage drop of transistor 63. As a result, the voltage at node 50 will vary substantially between  $2V_{DD}$  and  $3V_{DD}$  as the lower or second electrode of capacitor 49 varies between zero and  $V_{DD}$  volts. Coupling transistor 64 has a threshold voltage drop associated therewith which is compensated in an analogous manner by transistors 52, 58 and 60 and capacitors 53 and 54. The transistor di-



mensions of transistors 45, 63 and 58, 64 may be adjusted for less drive voltage to reduce reverse leakage current through transistors 63 and 64. The present invention provides a significant advantage over previous charge pumps in that large output voltages may be provided from supply voltages of less than five volts. Knowing that the voltage differential between node 35 and node 41 must be equal to at least two threshold voltage drops, a theoretical minimum value of  $V_{DD}$  may be readily determined. Since

$$V_{41(max)} - V_{35(min)} \geq 2V_T$$

must be satisfied in order to charge a compensating threshold voltage onto capacitor 42, it follows that the minimum value for  $V_{DD}$  is:

$$V_{DD} \geq (3/2) V_T$$

For supply voltage values less than  $(3/2) V_T$ , the threshold voltage drop across transistor 63 cannot be cancelled completely and the output voltage of charge pump 10 will be reduced from the intended value. However, for MOS processes in which a transistor threshold voltage varies between one and two volts, charge pump 10 is fully functional for supply voltages as low as between two and three volts.

In one form, the output voltage may be limited by connecting node 50 to power supply voltage  $V_{DD}$  via a conventional diode clamp (not shown) such as two series connected diode configured N-channel MOS transistors. The purpose of such a diode clamp would be to limit the output voltage to a predetermined maximum value if the power supply value is subject to wide variation.

Clock portion 18 functions to coordinate the switching of the charge boosting of nodes 30, 35 and 50. A transition of a clock signal is initially reflected by CLOCK 1 which affects the charging and discharging of capacitor 53. When the complement clock signal transitions, the voltage at nodes 30, 41 and 50 changes in direct response. After the bias voltage of transistor 36 is established, the CLOCK 2 signal transitions to change the voltage at node 35. It should be apparent that many other types of clock logic circuits could be used to effect the required switching. A significant aspect of the clock timing provided by clock portion 18 is the fact that transistor 36 should be made nonconductive before capacitor 38 is charge boosted so that the charge on capacitor 38 does not leak back to the  $V_{DD}$  power supply. Additionally, the second electrodes of capacitors 40 and 53 should be clocked before nodes 35 and 50 are clocked, respectively. By first clocking capacitors 40 and 53, circulation of charge thru transistors 39, 45 and 47 and capacitor 42 begins immediately after a clock signal transition. Otherwise, the charging and discharging action of capacitors 38 and 49 by other coupled devices in charge pump 10 could inhibit charge circulation thru transistors 39, 45 and 47 and capacitor 42.

By now it should be apparent that a charge pump has been provided which operates at low supply voltages below five volts as well as at higher voltages. The present invention may be practised with one or more pump stages such as stage 16 depending upon an actual value of output voltage desired. Although the detailed description of the present invention does not acknowledge the effects of parasitics associated with the various nodes of pump 10, pump 10 remains effective in providing an accurate amplified output voltage at node 66

even when charge sharing of the nodal voltages occurs with parasitic capacitance.

While an embodiment has been disclosed using certain assumed parameters, it should be understood that certain obvious modifications to the circuit or the given parameters will become apparent to those skilled in the art, and the scope of the invention should be limited only by the scope of the claims appended hereto.

We claim:

1. A circuit for increasing a power supply voltage from a power supply source and providing a boosted output voltage at an output terminal, comprising:

diode means coupled between a first node and a supply terminal adapted to receive the power supply voltage, said diode means having a threshold voltage and preventing current flow from the first node to the supply terminal;

first charge storage means coupled to the output terminal for selectively storing the power supply voltage and a boost voltage to provide the boosted output voltage; and

transistor coupling means having a control electrode, a first current electrode coupled to the first node, and a second current electrode coupled to the output terminal, and a threshold voltage associated therewith;

wherein the improvement comprises:

compensation means coupled between the first node and the control electrode of the transistor coupling means, for providing a control voltage to the control electrode sufficiently above the threshold voltage of the transistor coupling means so as to reduce the effective threshold voltage drop between the first node and the output terminal to substantially zero volts.

2. The circuit of claim 1 wherein said compensation means further comprises:

second compensation means coupled between the supply terminal and the first node, for preventing the first node from dropping below the power supply voltage.

3. The circuit of claim 2 wherein said second compensation means further comprises:

a first transistor having its current conducting electrodes coupled between the supply terminal and the output terminal, and having a control electrode coupled to a first node;

a second transistor having its current conducting electrodes coupled between the supply terminal and the first node, and having a control electrode coupled to the output terminal; and

second charge storage means coupled to the first node for selectively storing the boost voltage.

4. The circuit of claim 1 wherein said compensation means further comprise means coupled between a predetermined one of the current electrodes of the transistor coupler and the control electrode of the transistor coupler, for cancelling the threshold voltage drop of the transistor coupler and making said threshold voltage drop substantially zero volts, comprising:

second charge storage means coupled between the output node and the control electrode of the transistor coupler;

a first diode configured transistor having both a first current electrode and a control electrode connected to the output terminal, and a second current electrode;

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a second diode configured transistor having a first current electrode coupled to the output terminal, and both a second current electrode and a control electrode connected to the control electrode of the transistor coupler;

a third diode configured transistor having a first current electrode coupled to the control electrode of the transistor coupler, and both a second current electrode and a control electrode connected together; and

third charge storage means coupled to the second current electrodes of the first and third diode configured transistors, for selectively storing the boost voltage.

5. The circuit of claim 1 further comprising:

clock means for receiving an input clock signal and providing therefrom a control signal and a complement thereof as the boost voltage to the charge storage means and to the compensation means, respectively.

6. A charge pump circuit for boosting a power supply voltage to provide a boosted output voltage, comprising:

a diode configured transistor having a first current electrode and a control electrode connected together and coupled to a terminal for receiving the power supply voltage, and a second current electrode connected to a first node for supplying a primary voltage at the first node, said diode configured transistor having a first threshold voltage drop associated therewith;

first capacitance means having a first electrode coupled to the first node and a second electrode for selectively receiving a clock signal voltage, said capacitance means boosting the primary voltage at the first node to a secondary voltage;

first compensation means coupled in parallel with the diode configured transistor for compensating for the first threshold voltage drop so that the primary voltage substantially equals the power supply voltage;

output capacitance means for selectively storing the secondary voltage to provide the boosted output voltage;

transistor coupler means having a second threshold voltage drop associated therewith, said transistor coupler means having a control electrode and current conducting electrodes which selectively couple the first node to the output capacitance means; and

second compensation means coupled between the control electrode and a predetermined one of the current conducting electrodes of the transistor coupler means for compensating for the second threshold voltage drop so that the boosted output voltage substantially equals the secondary voltage at the first node.

7. The charge pump of claim 6 wherein the first compensation means comprise:

a first transistor having a first current electrode coupled to the terminal for receiving the power supply voltage, a control electrode and a second current electrode coupled to the first node;

a second transistor having a first current electrode coupled to the terminal for receiving the power

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supply voltage, a control electrode coupled to the first node, and a second current electrode coupled to the control electrode of the first transistor; and

second capacitance means having a first electrode coupled to the second current electrode of the second transistor, and a second electrode for selectively receiving the clock signal voltage.

8. The charge pump of claim 6 wherein the second compensation means further comprise:

second capacitance means having a first electrode coupled to the first node and a second electrode coupled to the control electrode of the transistor coupler means;

a first diode configured transistor having a first current electrode coupled to the first node and both a control electrode and a second current electrode coupled to the control electrode of the transistor coupler means;

a second diode configured transistor having a first current electrode coupled to the control electrode of the transistor coupler means, and both a control electrode and a second current electrode connected together;

a third diode configured transistor having both a first current electrode and a control electrode coupled to the first node, and a second current electrode coupled to the second current electrode of the second diode configured transistor; and

third capacitance means having a first electrode coupled to the second current electrodes of the second and third diode configured transistors, and a second electrode for selectively receiving the clock signal voltage.

9. The charge pump of claim 7 wherein the second capacitance means selectively receives the clock signal voltage by receiving a delayed complement of the clock signal voltage.

10. The charge pump of claim 8 wherein the third capacitance means selectively receives the clock signal voltage by receiving a delayed complement of the clock signal voltage.

11. A method of providing a boosted output voltage from a power supply voltage, comprising the steps of:

coupling a power supply voltage terminal to a first node via a diode means having a first threshold voltage drop associated therewith;

coupling charge storage means to the first node for selectively boosting the first node's voltage potential to a predetermined voltage potential;

selectively coupling the first node to an output charge storage means via a coupling device having a second threshold voltage drop associated therewith; and

compensating for the second threshold voltage drop so that the voltage potential coupled to the output charge storage means substantially equals the voltage potential of the first node.

12. The method of claim 11 further comprising the step of:

compensating for the first threshold voltage drop of the diode means so that the first node has the same voltage potential as the power supply voltage terminal.

\* \* \* \* \*

# United States Patent [19]

Backes et al.

[11] Patent Number: 4,633,106

[45] Date of Patent: Dec. 30, 1986

[54] MOS BOOTSTRAP PUSH-PULL STAGE

[75] Inventors: Reiner Backes, Freiburg; Friedrich Schmidpott, Gundelfingen, both of Fed. Rep. of Germany

[73] Assignee: ITT Industries, Inc., New York, N.Y.

[21] Appl. No.: 614,295

[22] Filed: May 25, 1984

[30] Foreign Application Priority Data

May 27, 1983 [EP] European Pat. Off. .... 83105252.7

[51] Int. Cl.<sup>4</sup> ..... H03K 4/24; H03K 4/58; H03K 17/10; H03K 19/096

[52] U.S. Cl. .... 307/578; 307/482; 307/270

[58] Field of Search ..... 307/482, 578, 450, 453, 307/270

[56] References Cited

## U.S. PATENT DOCUMENTS

3,988,617 10/1976 Price ..... 307/453  
4,042,838 8/1977 Street et al. .... 307/482 X

4,284,905 8/1981 Rosenzweig ..... 307/482  
4,330,719 5/1982 Nagami ..... 307/578 X  
4,388,538 6/1983 Ikeda ..... 307/482  
4,390,803 6/1983 Koike ..... 307/270 X  
4,431,927 2/1984 Eaton, Jr. et al. .... 307/578 X  
4,500,799 2/1985 Sud et al. .... 307/482 X

## OTHER PUBLICATIONS

Fink et al, *Electronics Engineers' Handbook*, Second Edition, pp. 16-15 to 16-19, 1982.

Primary Examiner—Stanley D. Miller

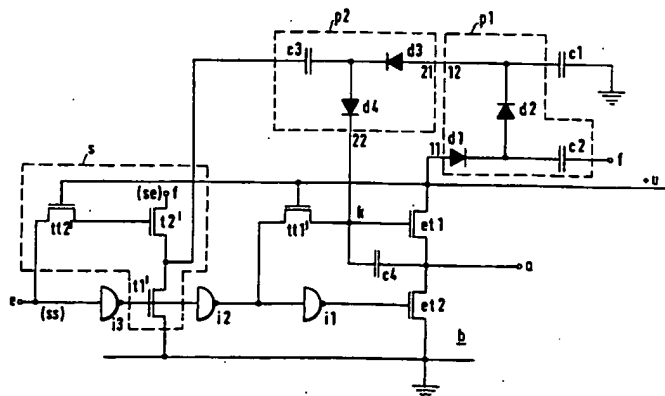
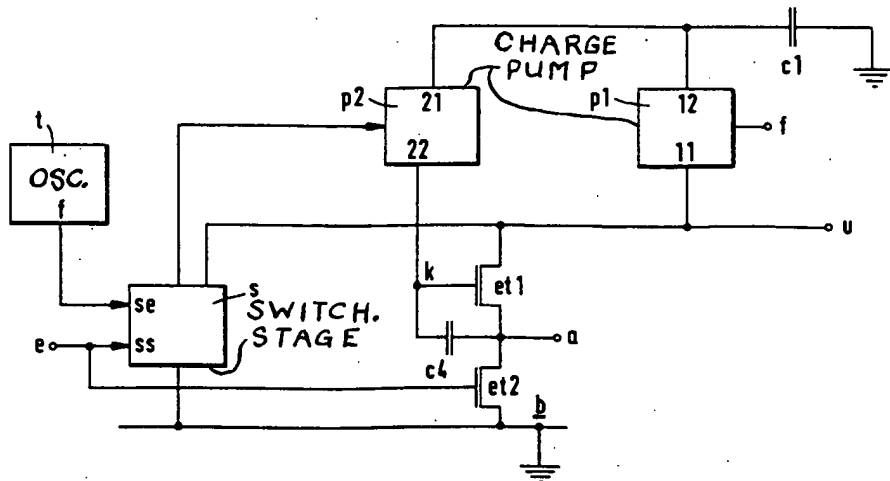
Assistant Examiner—David Bertelson

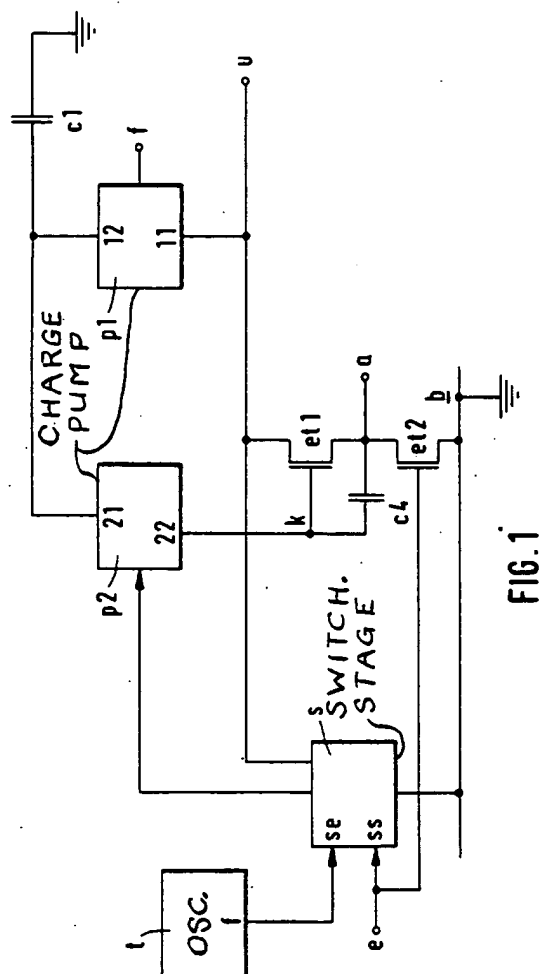
Attorney, Agent, or Firm—Donald J. Lenkszus

## [57] ABSTRACT

A circuit is described which holds the bootstrap node of a MOS push-pull end stage at a constant potential even if the end stage has to generate an output H-level. A diode/capacitor charge pump circuit supplies the required pulse current only fed to the node in case of the output H-level.

12 Claims, 3 Drawing Figures





**FIG. 1**

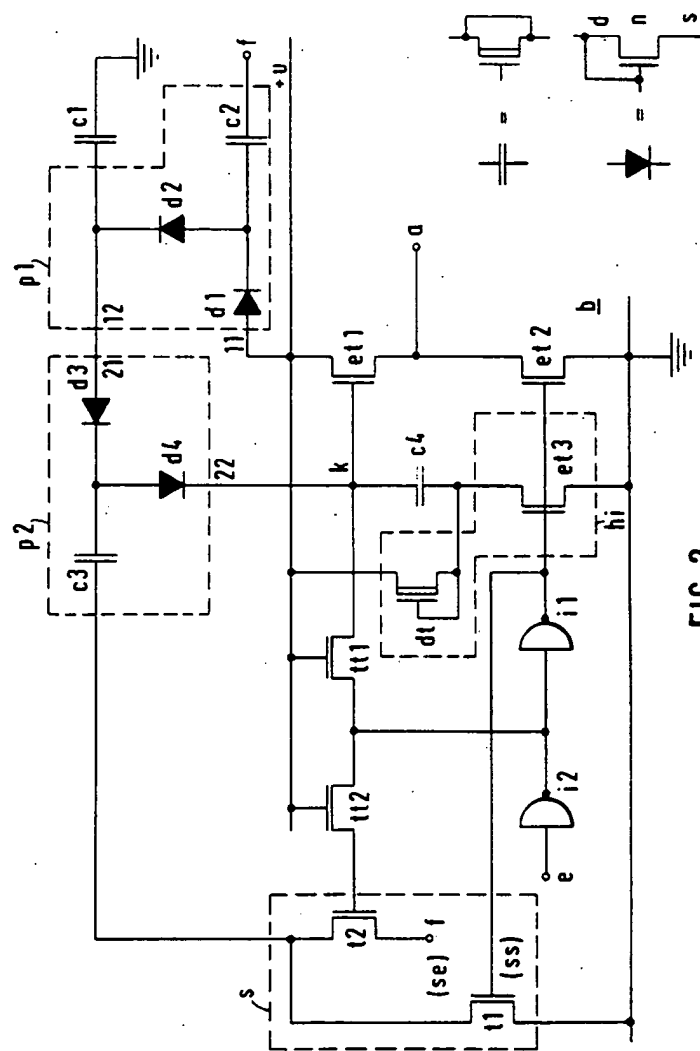


FIG. 2

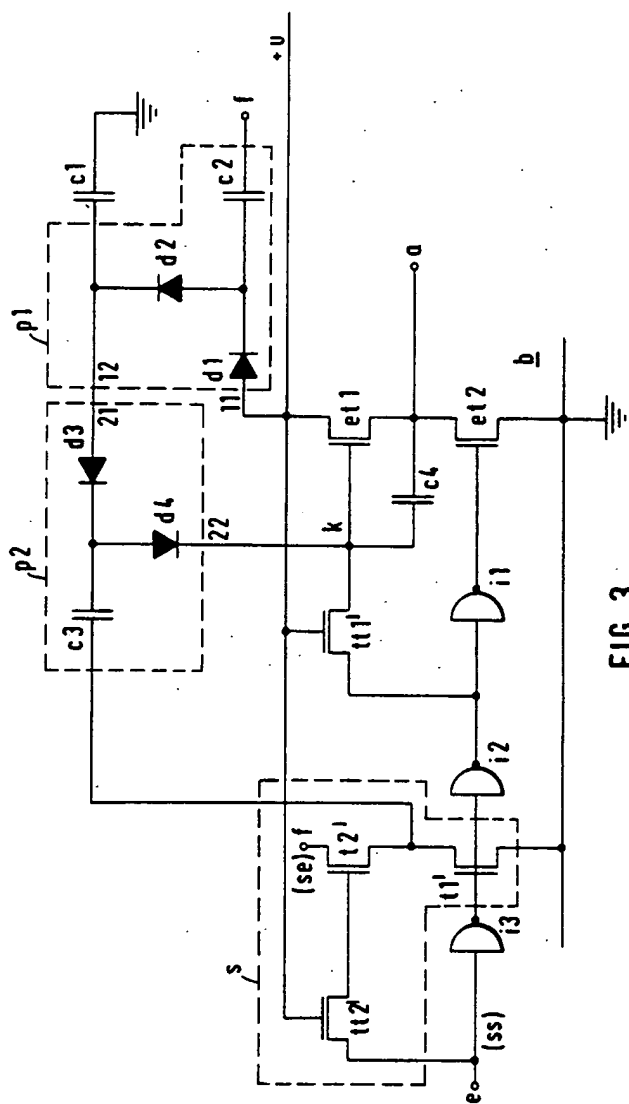


FIG. 3

## MOS BOOTSTRAP PUSH-PULL STAGE

## BACKGROUND OF THE INVENTION

This invention relates to a bootstrap push pull stage. More specifically, this invention relates to a digital monolithic integrated bootstrap push pull stage using insulated-gate field-effect transistor technology (MOS technology). Such a stage comprises two enhancement-mode output-stage transistors having their drain-source paths connected in series between the supply voltage and ground. A bootstrap capacitor has one of its terminals connected to the gate of the output-stage transistor coupled to the supply voltage, whereby the bootstrap node is formed, and has its other terminal connected to a point following the potential of the output of the bootstrap push-pull stage. The bootstrap push-pull stage further comprises a first charge pump circuit having its clock input connected directly to the output of a clock oscillator and having its first direct-voltage terminal, whose polarity is opposite to that of the supply voltage, connected to the supply voltage, and the inverters and capacitors.

A bootstrap push-pull stage of this kind is disclosed in Offenlegungsschrift DE No. 23 59 646. In that stage, manufacturing variations affecting the gate voltage are compensated for, so that operation within a linear range is ensured. The parameters of stages fabricated together with their load circuits on different semiconductor wafers vary if an externally generated gate voltage common to all push-pull stages is applied.

## SUMMARY OF THE INVENTION

The object of the invention is to improve the prior art circuit so that during the presence of an output level corresponding to the potential of the supply voltage, the voltage at the bootstrap node remains as constant as possible even over prolonged periods and the output level remains constant as well. The invention makes it possible to hold the output at a constant logic level over prolonged periods of time.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be explained in greater detail with reference to the accompanying drawings, in which:

FIG. 1 is a schematic circuit diagram of a bootstrap push-pull stage according to the invention; and

FIGS. 2 and 3 are circuit diagrams of different embodiments of such a bootstrap push-pull stage.

## DETAILED DESCRIPTION

The schematic circuit diagram of FIG. 1 shows the bootstrap push-pull stage b with the two enhancement-mode output-stage transistors, et1, et2, whose source-drain paths are connected in series between the supply voltage u and ground, the node of the source-drain paths being the output a of the bootstrap push-pull stage b. The bootstrap capacitor c4 is connected to the gate of the output-stage transistor et1, thereby forming the bootstrap node k, and to a point following the potential of the output a; in FIG. 1, this point is the output a itself. The drain of the output-stage transistor et1 is coupled to the supply voltage u. The first charge pump circuit p1 has its clock input connected to the output f of the clock oscillator t, and its first direct-voltage terminal 11,

whose polarity is opposite to that the supply voltage u, is connected to the supply voltage u.

The second direct-voltage terminal 12 of the first charge pump circuit p1 is connected to the first direct-voltage terminal 21 of the second charge pump circuit p2; the polarity of this terminal 21 is opposite to that of the supply voltage u. The second direct-voltage terminal 22 of the second charge pump circuit p2 is connected to the bootstrap node k. The second direct-voltage terminal 12 of the first charge pump circuit p1 and the first direct-voltage terminal 21 of the second charge pump circuit p2 are grounded through the first capacitor c1, which serves as a smoothing capacitor. The clock input of the second charge pump circuit p2 is connected to the output of the switching stage s, whose signal input se and control input ss are connected to the output f of the clock oscillator t and to the control input e of the bootstrap push-pull stage, respectively. The switching stage s passes on the clock signal when the input signal of the bootstrap push-pull stage b is at the logic level assigned to the supply voltage u. In the schematic circuit diagram of FIG. 1, the input e is shown connected to the gate of the grounded output-stage transistor et2 for simplicity.

FIGS. 2 and 3 are circuit diagrams of different embodiments of a bootstrap push-pull stage according to the invention. In both embodiments, the charge pump circuits p1, p2 are of the same design; the first, p1, consists of the first and second MOS diodes d1, d2 and the second capacitor c2, and the second, p2, consists of the third and fourth MOS diodes d3, d4 and the third capacitor c3, with the MOS diodes d1, d2 and d3, d4 connected in series in the same direction between the direct-voltage terminals 11, 12, and 21, 22, respectively, of the charge pump circuits.

In FIGS. 2 and 3, the supply-voltage u is assumed to be positive (+u), so the transistors are n-channel transistors. Then, the cathode, the first MOS diode d1 and the anode of the second MOS diode d2 are connected to the output f of the clock oscillator t through the second capacitor c2, and the cathode of the third MOS diode d3 and the anode of the fourth MOS diode d4 are connected to the output of the switching stage s through the third capacitor c3. The anode of the first MOS diode d1 is connected to the supply voltage +u, and the cathode of the fourth MOS diode d4 to the bootstrap node k.

In FIG. 2, that terminal of the bootstrap capacitor c4 which is not connected to the bootstrap node is tied to the output of the auxiliary inverter hi. The latter consists of the transistor et3, whose gate is connected to the gate of the output-stage transistor et2 and whose source is grounded, and the depletion-mode transistor dt, used as a load device and having its drain connected to the supply voltage +u. Associated with the output-stage transistors et1, et2 is the drive stage formed from the enhancement-mode transfer transistor tt1 and the two inverters i1, i2, with the gate of the grounded output-stage transistor et2 connected to the output of the first inverter i1, whose input is connected to the bootstrap node k via the source-drain path of the first transfer transistor tt1, whose gate is connected to the supply voltage +u, and to the input e of the bootstrap push-pull stage via the second inverter i2. The switching stage s of FIG. 2 consists of the first enhancement-mode transistor t1, whose source-drain path is located between the output of this stage and ground and whose gate, representing the control input ss, is connected to

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the output of the first inverter i1, and the second enhancement-mode transistor t2, whose source-drain path is located between the output of the signal input se of the switching stage ss, and whose gate is connected via the source-drain path of the second enhancement-mode transfer transistor tt2, which has its gate connected to the supply voltage, to the output of the second inverter i2 and via the source-drain path of the first transfer transistor tt1 to the bootstrap node k.

In FIG. 3, the terminal of the bootstrap capacitor c4 not connected to the bootstrap node is tied directly to the output a of the bootstrap push-pull stage. The gate of the output-stage transistor et2 is connected to the output of the first inverter i1 of the driver stage, and the input of this first inverter i1 is connected to the output of the second inverter i2 and, through the source-drain path of the transfer transistor tt1', whose gate is connected to the supply voltage +u, to the bootstrap node k. The input of the second inverter i2 is connected to the output of the third inverter i3, which has its input connected to the input e of the bootstrap push-pull stage b. The output of the third inverter i3 is also connected to the gate of the first enhancement-mode transistor t1' of the switching stage s. The source-drain path of this transistor is inserted between ground and the output of this stage. The second enhancement-mode transistor t2' has its source-drain path connected between the output and the signal input se of the switching stage s, and its gate is connected to the input e through the source-drain path of the transfer transistor tt2', whose gate is coupled to the supply voltage +u.

The MOS diodes d1 . . . d4 are n-channel enhancement-mode transistors with a gate-drain connection as the anode, and the capacitors c1, c2, c3 and the bootstrap capacitor c4 are MOS transistors of the same type with a drain-source connection.

To explain the operation of the circuit, reference will be made to FIG. 3.

It is assumed that the H level is the more positive of the two binary-system logic levels, and the L level the more negative one. Since the clock signal from the clock oscillator t is applied continuously to the pump circuit p1, the latter establishes at the ungrounded terminal of the first capacitor c1 a potential lying above the supply potential +u. This higher potential is further increased by the second pump circuit p2 with respect to the bootstrap node k depending on the logic signal at the input e. If the input e is at an H level, the gate of the transistor t2' is at an H level, too, while the gate of the transistor t1' is low. Both conditions together cause the clock signal to be transferred to the second pump circuit p2, which thus applies a correspondingly high voltage to the bootstrap node k. The H level at the input e causes an H level at the bootstrap k via the inverters i3, i2 and the transfer transistor tt1'. Since, on the other hand, the H level at the input e results in an L level at the gate of the output-stage transistor et2 because of the inverters i3, i2, i1, this transistor is cut off, so that the output a like the bootstrap node k, is at an H level. As long as the input e is high, i.e., as long as the output is to be high, too, this condition is maintained regardless of the leakage currents effective at the bootstrap node k, because the two pump circuits p1, p2 compensate for the leakage currents and, thus, maintain the high potential at the bootstrap node k that is required for the H level at the output a.

Viewed from an L state preceding the above-mentioned H state at the input e, the turnoff of the output-

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stage transistor et2 is delayed by the delay of the inverter i1 with respect to the generation of the H level at the bootstrap node k, so that the output a does not change from the L level caused by the L level at the input e to the H level until the H level is present at the bootstrap node k, i.e., the bootstrap action of the bootstrap capacitor c4 can take full effect.

If the input e is at an L level, the gate of the transistor t1' is at an H level, so that this transistor is conducting, and the gate of the transistor t2' is at an L level, so that this transistor is cut off. Thus, the capacitor c3 is practically at ground potential, and no clock signals are transferred to the second pump circuit p2. The bootstrap node k is at an L level, on which, however, the potential across the capacitor c1 is superimposed, which is applied therethrough the diodes d3, d4. The output-stage transistor et2 is constantly on because of the H level at its gate, so that the output a is at an L level.

During each L to H transition, the transfer transistors tt1' and tt2' cause a bootstrap effect at the gates of the output-stage transistor et1 and the transistor t2', respectively, which are connected to them. This has a favorable effect on the switching conditions and, thus, the slope of the transition edge.

What is claimed is:

1. A digital monolithic integrated bootstrap push-pull stage using insulated-gate field-effect transistor technology and comprising:

an input terminal;

first and second enhancement-mode output-stage transistors having their drain-source paths connected in series between a supply voltage terminal and a ground terminal, the drain source path of said first transistor connected to said supply voltage terminal said second transistor having its gate connected to said input terminal;

an output terminal coupled to the junction of said first and second transistors;

a bootstrap capacitor having a first terminal connected to the gate of said first transistor whereby a bootstrap node is formed, and having a second terminal connected to a circuit point which follows the potential at the output of the bootstrap push-pull stage;

a first charge pump circuit having a first clock input terminal for receiving clock signals, a first direct-voltage terminal connected to said supply voltage terminal, and a second direct-voltage terminal having a voltage polarity opposite to that of the supply voltage;

a second charge pump circuit having a first direct-voltage terminal having a voltage polarity opposite to that of the supply voltage and coupled to said first charge pump second direct voltage terminal, a second direct-voltage terminal connected to said bootstrap node, and a second clock input terminal for receiving clock signals; and

a switching stage having a third input terminal coupled to said input terminal and having a third clock input terminal for receiving said clock signals and having a clock output terminal for coupling said clock signals to said second clock input terminal via said clock output terminal if the input signal to said bootstrap push-pull stage at said input terminal is at a logic level assigned to the supply voltage at said supply voltage terminal.

2. A bootstrap push-pull stage in accordance with claim 1, wherein said second direct-voltage terminal of



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said first pump circuit and said first direct-voltage terminal of said second charge pump circuit are grounded through a first capacitor.

3. A bootstrap push-pull stage in accordance with claim 1, wherein:

said first charge pump circuit comprises first and second MOS diodes serially connected between said first and second direct-voltage terminals of said first charge pump circuit; and

said second charge pump circuit comprises third and fourth MOS diodes connected in series between said first and second direct-voltage terminals of said second charge pump circuit.

4. A bootstrap push-pull stage in accordance with claim 3 using n-channel transistors, wherein:

said first charge pump circuit includes a second capacitor, the cathode of said first MOS diode and the anode of said second MOS diode being connected to said first clock input terminal through said second capacitor;

said second charge pump circuit includes a third capacitor, the cathode of said third MOS diode and the anode of said fourth MOS diode are connected to said clock output terminal of said switching stage through said third capacitor; and

the anode of the first MOS diode and the cathode of the fourth MOS diode are connected respectively to said supply voltage terminal and said bootstrap node.

5. A bootstrap push-pull stage in accordance with claim 4, wherein said second terminal of said bootstrap capacitor is connected to the output of said bootstrap push-pull stage.

6. A bootstrap push-pull stage in accordance with claim 4 comprising:

an auxiliary inverter having an output coupled to said bootstrap capacitor second terminal and an input coupled to the gate of said second output stage transistor; and

a depletion mode transistor is used as a load in said auxiliary inverter.

7. A bootstrap push-pull stage in accordance with claim 6 using n-channel transistors, and wherein said depletion-mode transistor has its gate and source connected to said second terminal of said bootstrap capacitor.

8. A bootstrap push-pull stage in accordance with claim 4 wherein:

said first, second, third and fourth MOS diodes each comprise an enhancement-mode transistor with a gate-drain connection forming the anode; and said bootstrap capacitor and said second and third capacitors each comprise a transistor with a drain-source connection.

9. A bootstrap push-pull stage in accordance with claim 7 wherein:

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said first, second, third and fourth MOS diodes each comprise an enhancement-mode transistor with a gate-drain connection forming the anode; and said bootstrap capacitor and said second and third capacitors each comprise a transistor with a drain-source connection.

10. A bootstrap push-pull stage in accordance with claim 9 including: a driver stage having a first inverter, a second inverter and a first enhancement-mode transfer transistor; and wherein

the output of said first inverter is connected to the gate of said second output-stage transistor, the input of said first inverter is connected to said bootstrap node via the source-drain path of said first enhancement-mode transfer transistor, said transfer transistor having its gate connected to said supply terminal, and the input terminal of said bootstrap push-pull stage is connected to the input of said second inverter, and the output of said second inverter is connected to said input of said first inverter.

11. A bootstrap push-pull stage in accordance with claim 10, wherein said switching stage includes:

a third enhancement-mode transistor having a source-drain path connected between the clock output terminal of said switching stage and said ground terminal and a gate connected to the output of said first inverter;

a fourth enhancement-mode transistor having its source-drain path connected between said clock output terminal and said third clock input terminal of said switching stage; and

a second enhancement-mode transfer transistor having a source-drain path connected between the gate of said fourth enhancement-mode transistor and the output of said second inverter and a gate connected to said supply voltage terminal.

12. A bootstrap push-pull stage in accordance with claim 10, wherein:

said switching stage includes a third inverter, a fifth enhancement-mode transistor having its drain-source path connected between said switching stage clock output terminal and said ground terminal and having its gate connected to the output of said third inverter, a sixth enhancement-mode transistor having its source-drain path connected between said switching stage third clock input terminal and said clock output terminal and a third enhancement-mode transfer transistor having its source-drain path connected between the third input terminal and the gate of said sixth enhancement-mode transistor and having its gate connected to said supply voltage terminal; and the input of said second inverter is connected to the output of said third inverter.

\* \* \* \* \*

# United States Patent [19]

Cranford, Jr. et al.

[11] Patent Number: 4,752,699

[45] Date of Patent: Jun. 21, 1988

[54] ON CHIP MULTIPLE VOLTAGE GENERATION USING A CHARGE PUMP AND PLURAL FEEDBACK SENSE CIRCUITS

[75] Inventors: Hayden C. Cranford, Jr., Apex; Stacy J. Garvin, Durham; Wendy K. Hodgkin, Raleigh; John M. Mullen, Cary, all of N.C.

[73] Assignee: International Business Machines Corp., Armonk, N.Y.

[21] Appl. No.: 943,466

[22] Filed: Dec. 19, 1986

[51] Int. Cl.<sup>4</sup> ..... G05F 1/571

[52] U.S. Cl. .... 307/297; 307/200 B; 307/296 R; 307/494; 307/360; 363/60; 365/226

[58] Field of Search ..... 363/60; 365/184, 185, 365/226, 228; 361/90, 98; 307/200 B, 491, 494, 530, 351, 353, 354, 360, 246, 296 R, 297

[56] References Cited

## U.S. PATENT DOCUMENTS

4,405,868 9/1983 Lockwood ..... 363/60 X  
4,428,071 1/1984 Wilmsmeyer ..... 307/297 X  
4,439,692 3/1984 Beekmans et al. .... 307/297

4,460,835 7/1984 Masuoka ..... 307/296 R  
4,481,566 11/1984 Hoffman et al. .... 363/60  
4,506,350 3/1985 Asano et al. .... 365/191  
4,583,157 4/1986 Kirsch et al. .... 363/60  
4,601,020 7/1986 Arakawa et al. .... 365/226  
4,633,106 12/1986 Backes et al. .... 307/482 X  
4,638,464 1/1987 Cranford, Jr. et al. .... 365/226  
4,673,829 6/1987 Gupta ..... 365/226 X

Primary Examiner—Stanley D. Miller

Assistant Examiner—D. R. Hudspeth

Attorney, Agent, or Firm—Joscelyn G. Cockburn

## [57] ABSTRACT

A level selectable FET voltage generation system is described. The system includes a single charge pump controlled by multiple feedback paths and a power-down circuit. Each feedback path contains a capacitor divider network, a sense amplifier with a compensating voltage reference and a timer which periodically resets the capacitor divider network to insure sensing accuracy. The powerdown circuit and a selected feedback path provides a desired voltage level at the output of the charge pump.

8 Claims, 17 Drawing Sheets

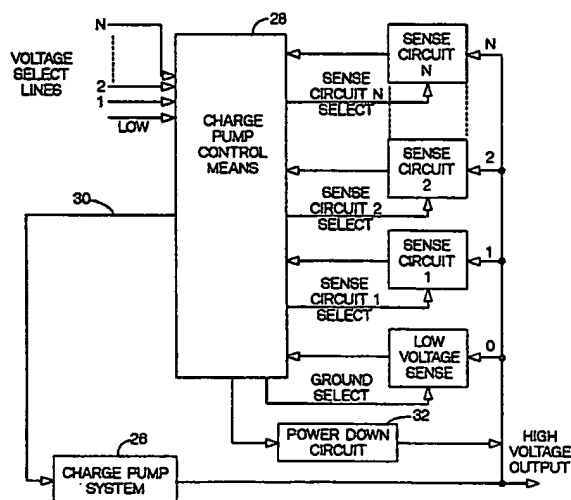


FIG. 1

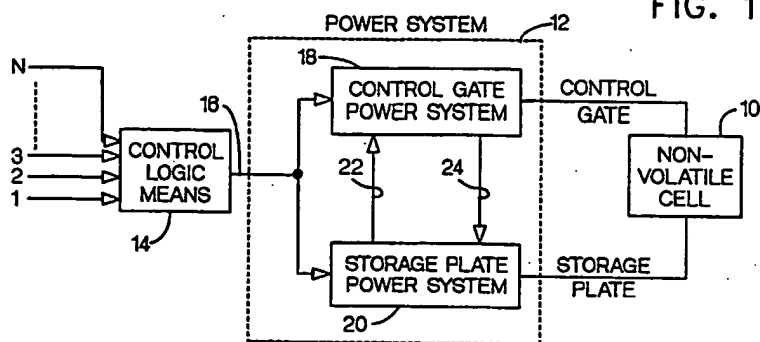
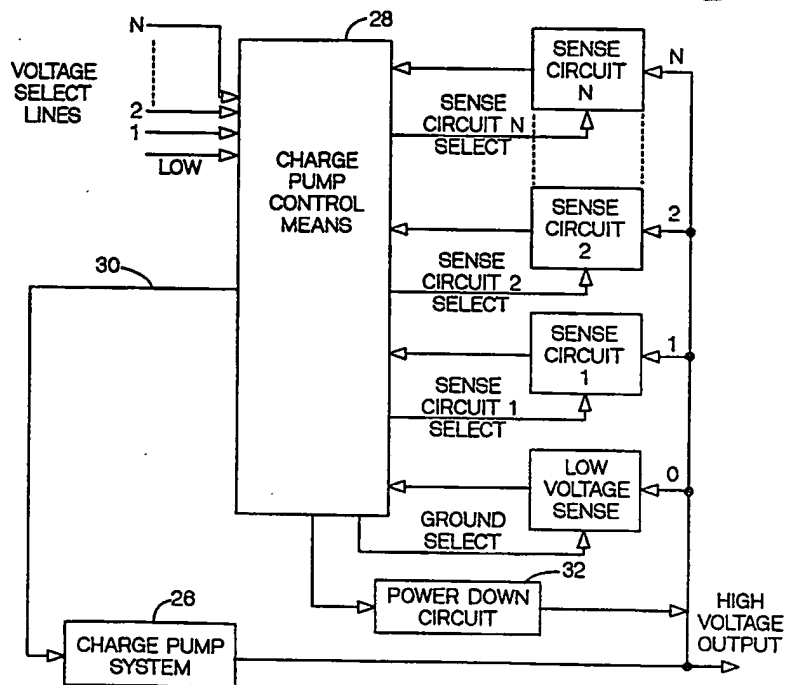


FIG. 2



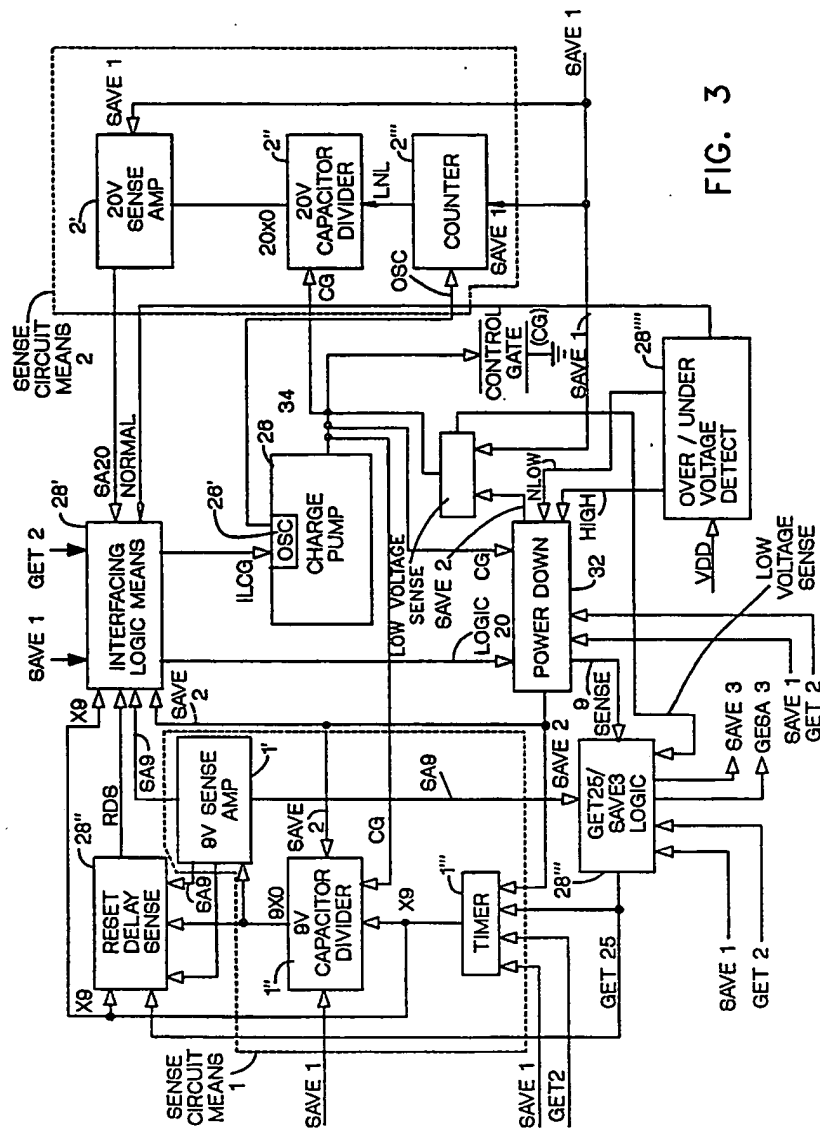


FIG. 3

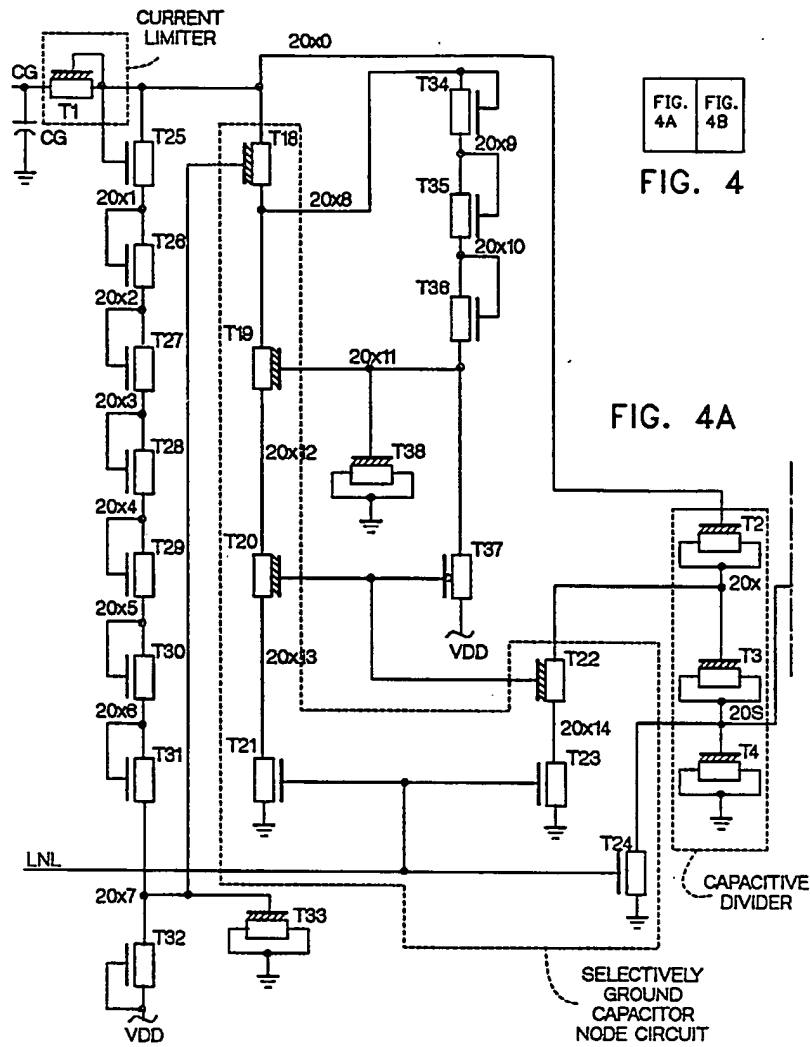
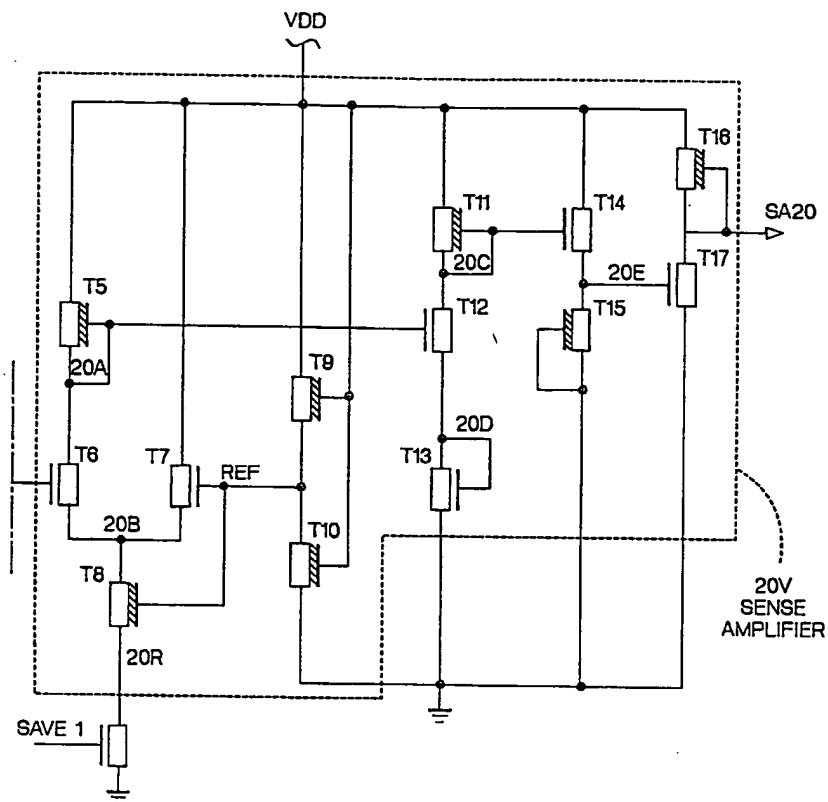
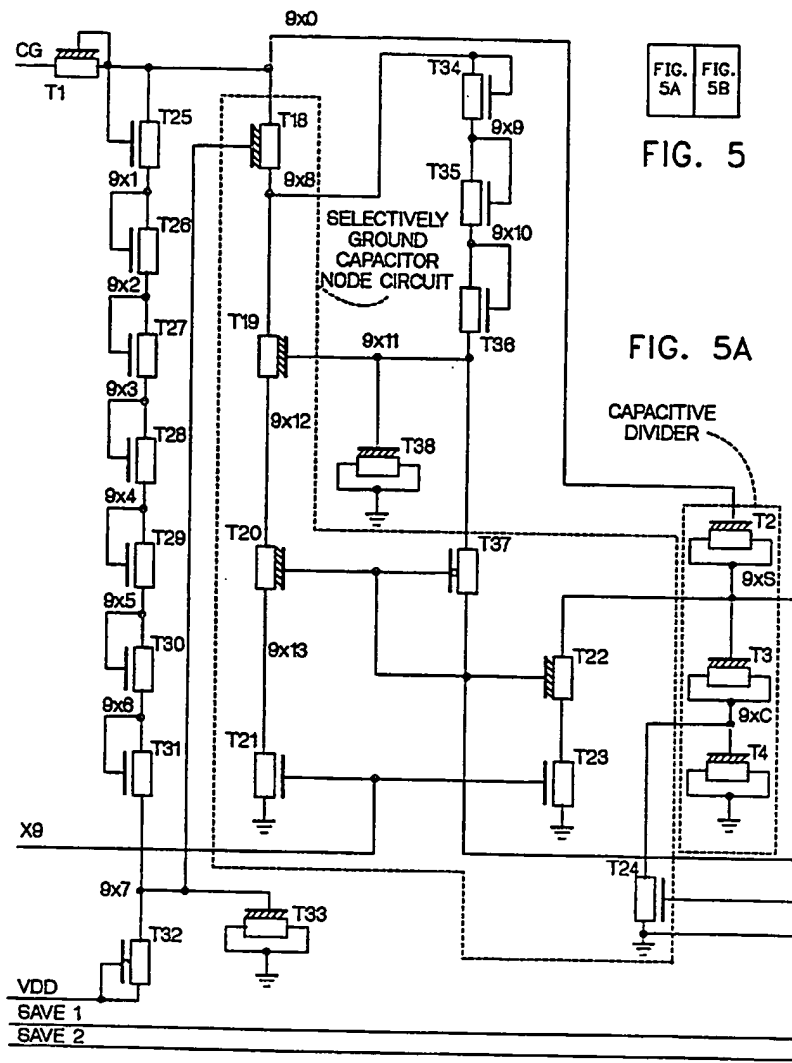
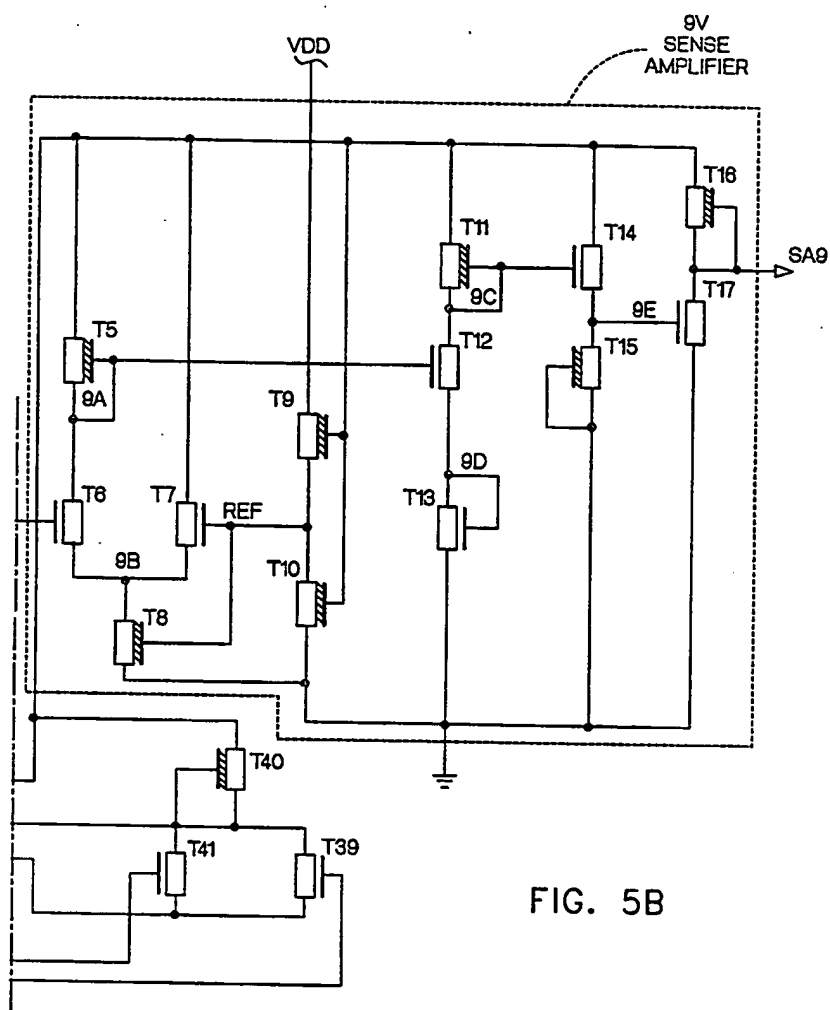


FIG. 4B









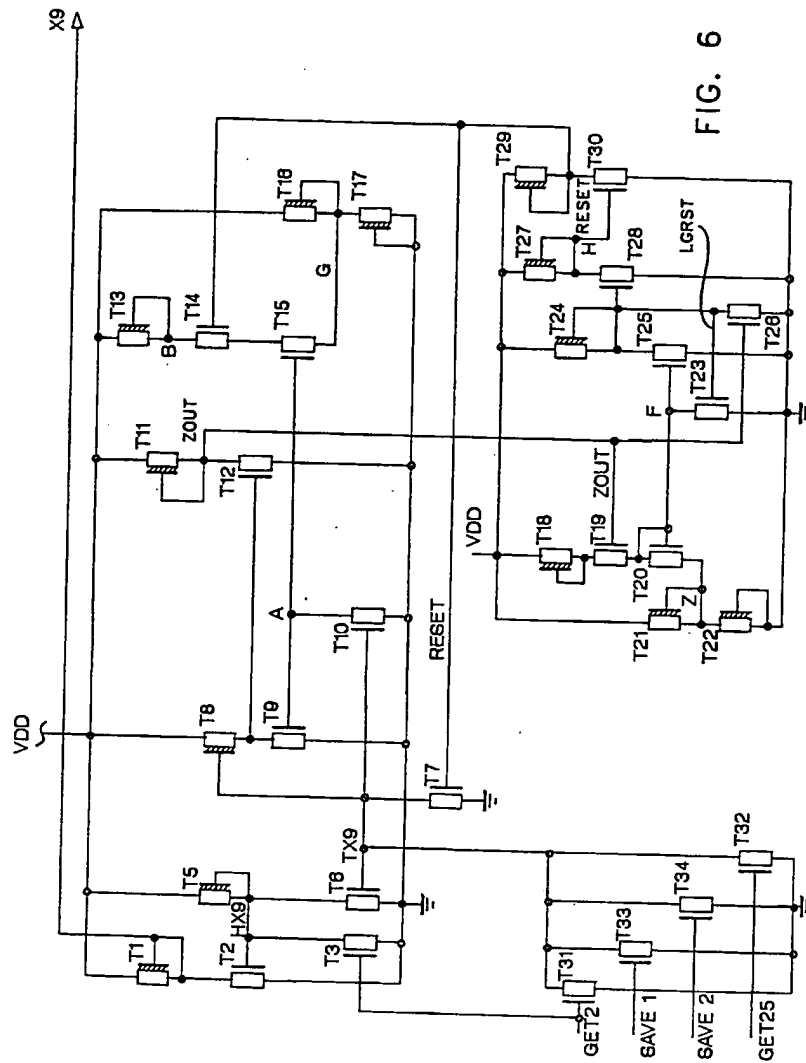
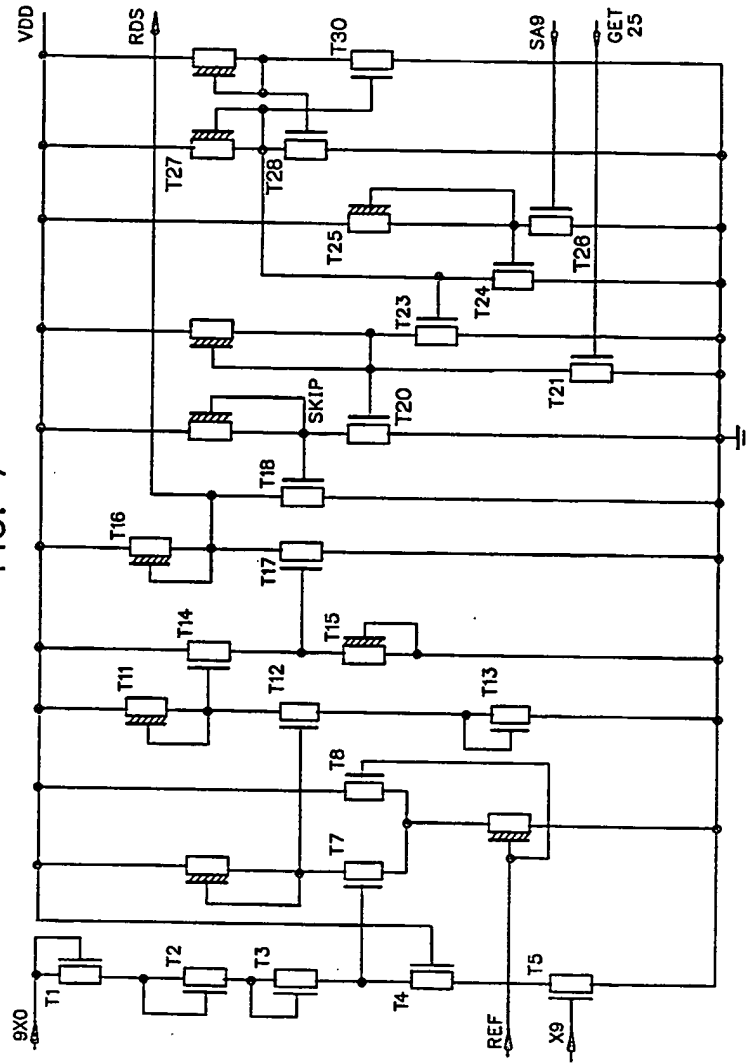


FIG. 6

FIG. 7



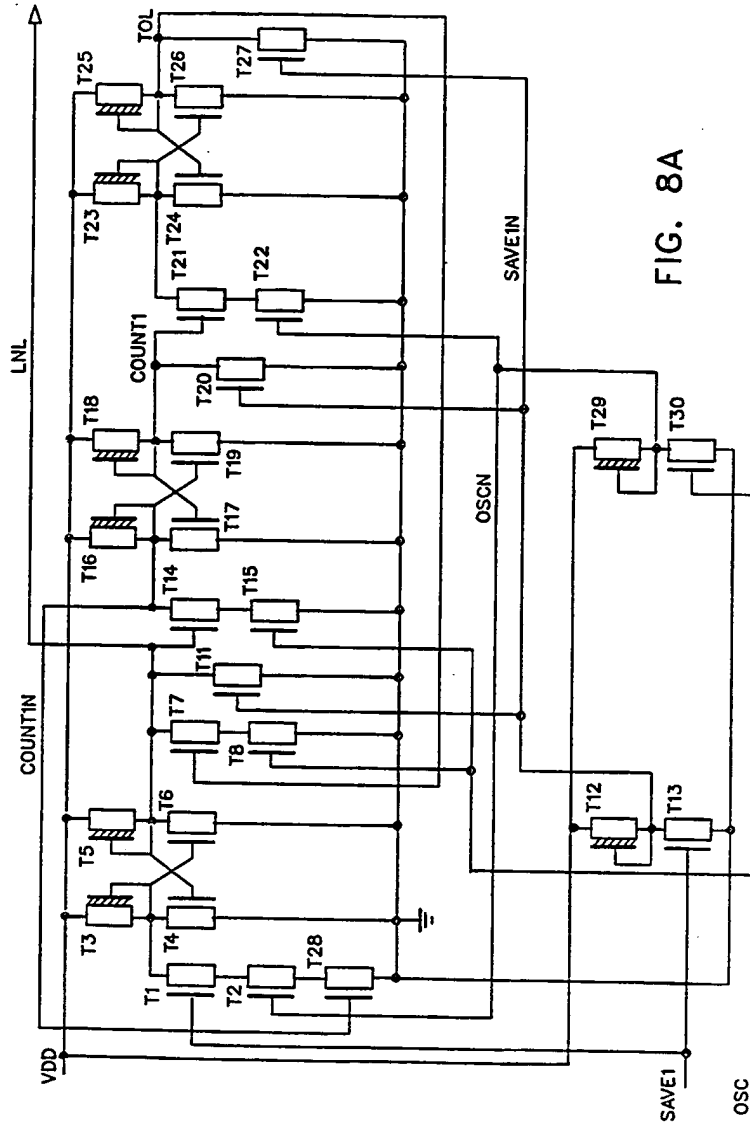


FIG. 8A

FIG. 8B

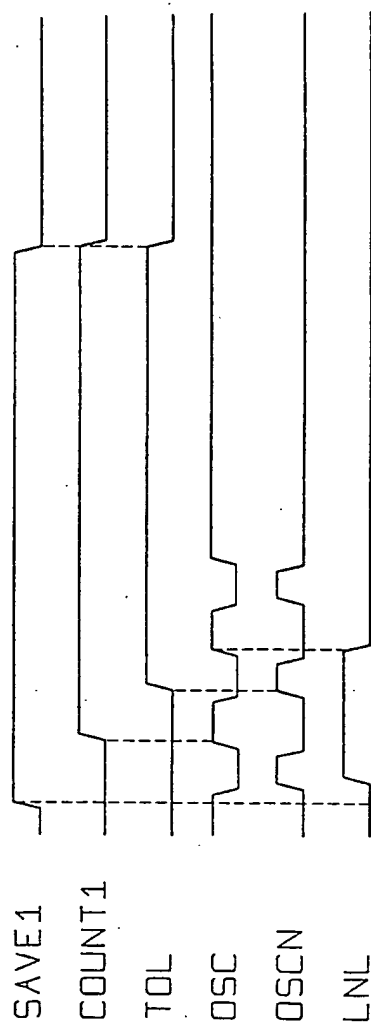


FIG. 9A

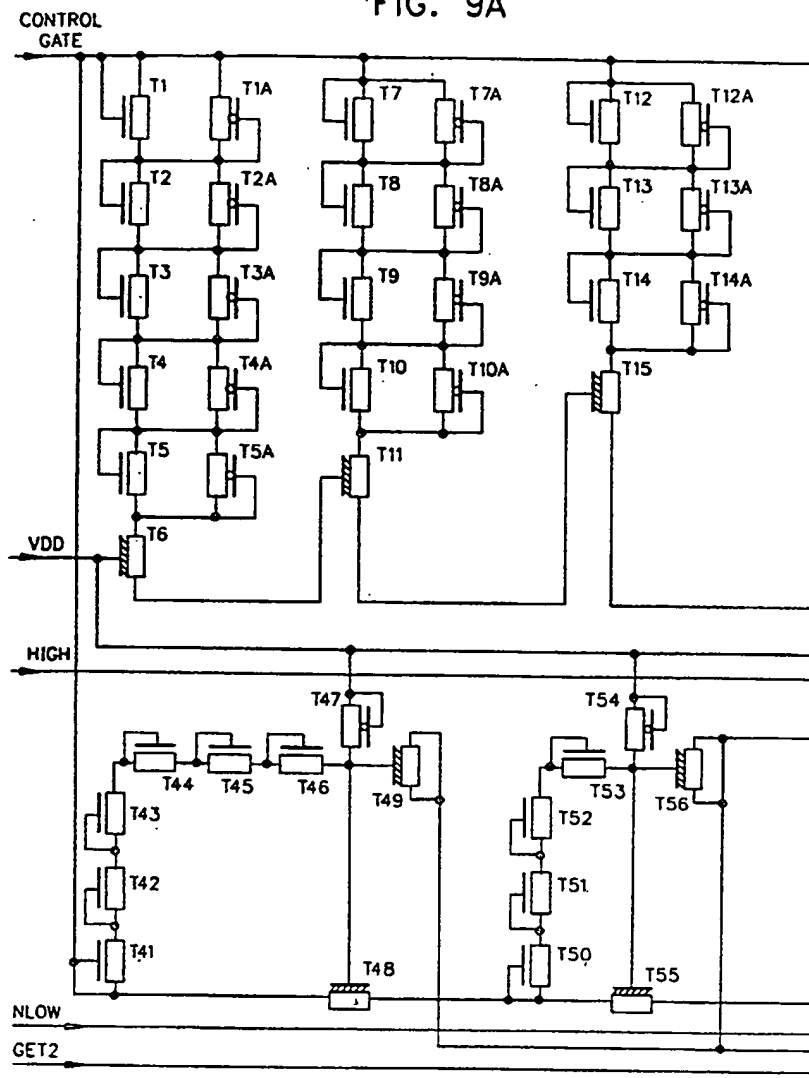
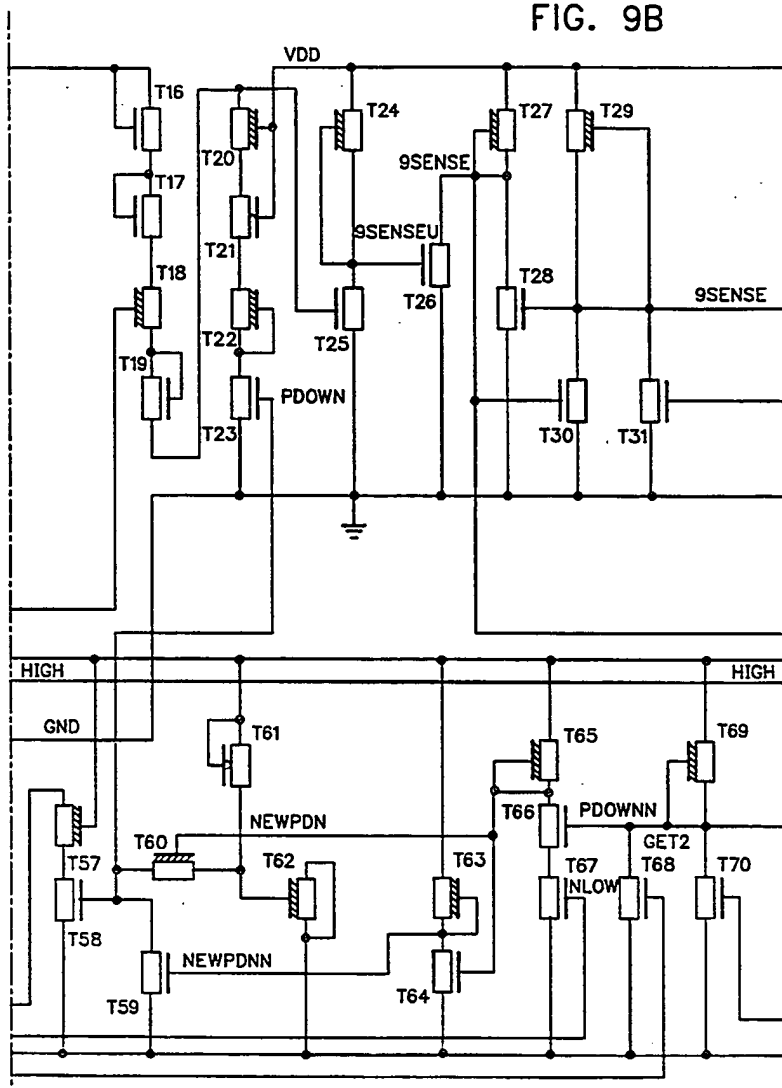


FIG. 9B



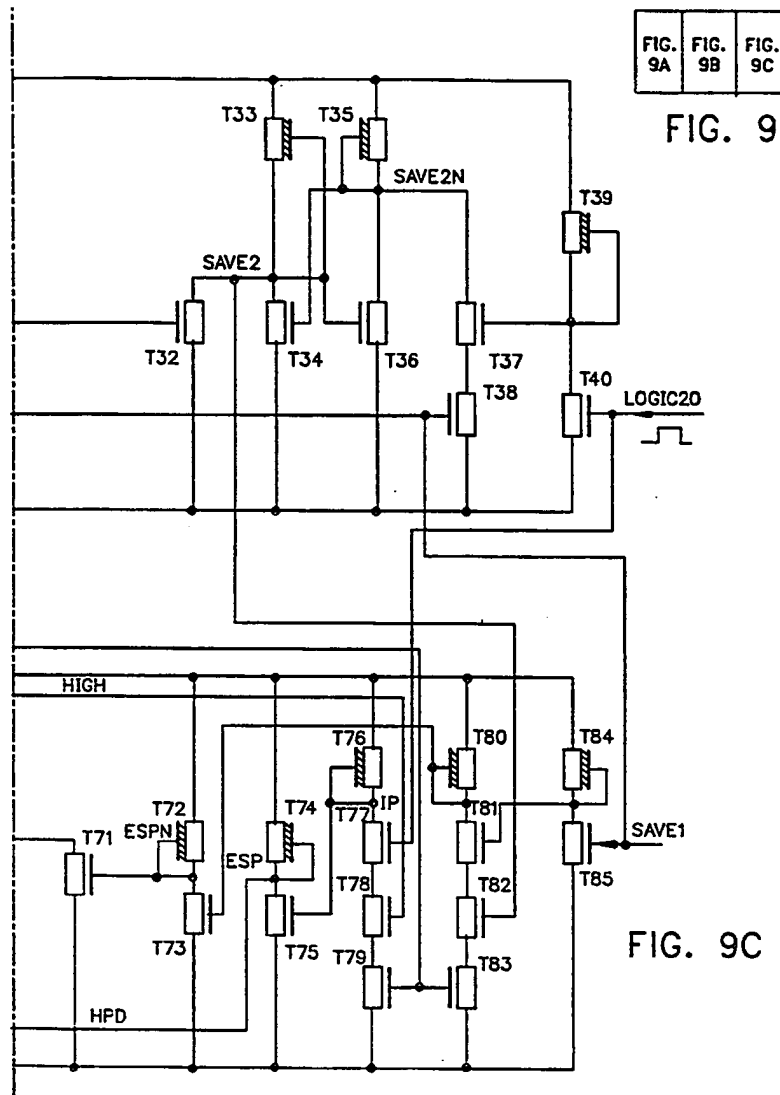


FIG. 10

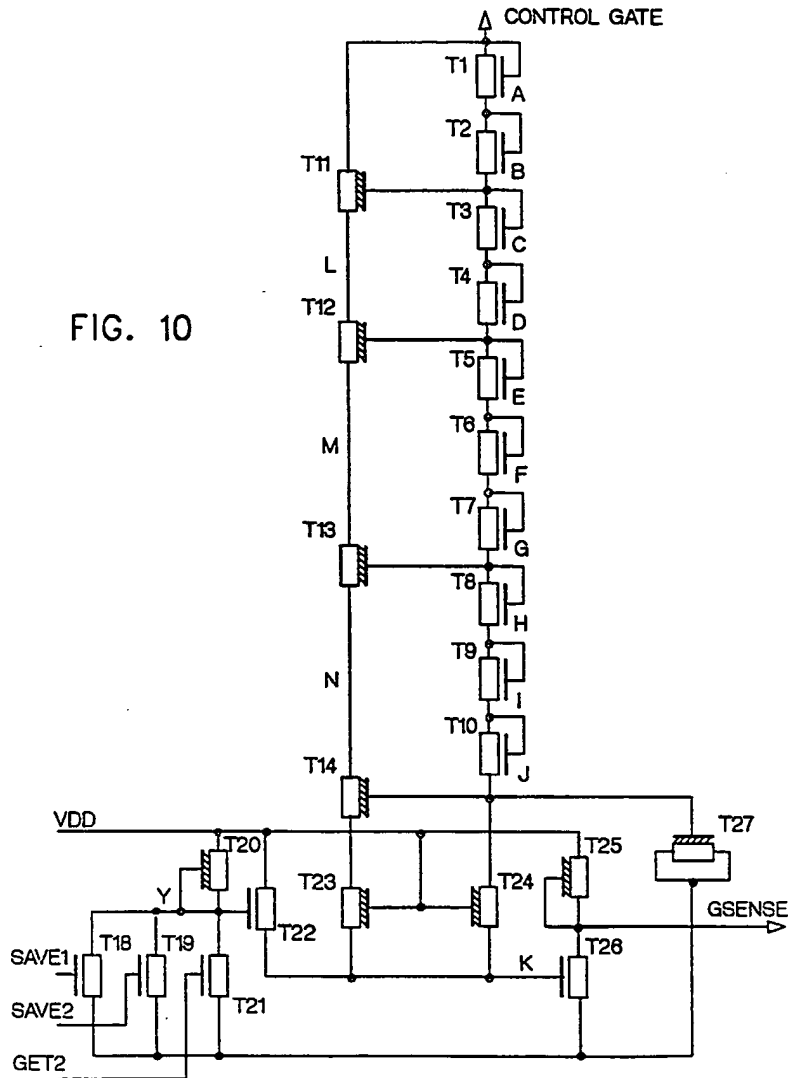




FIG. 11

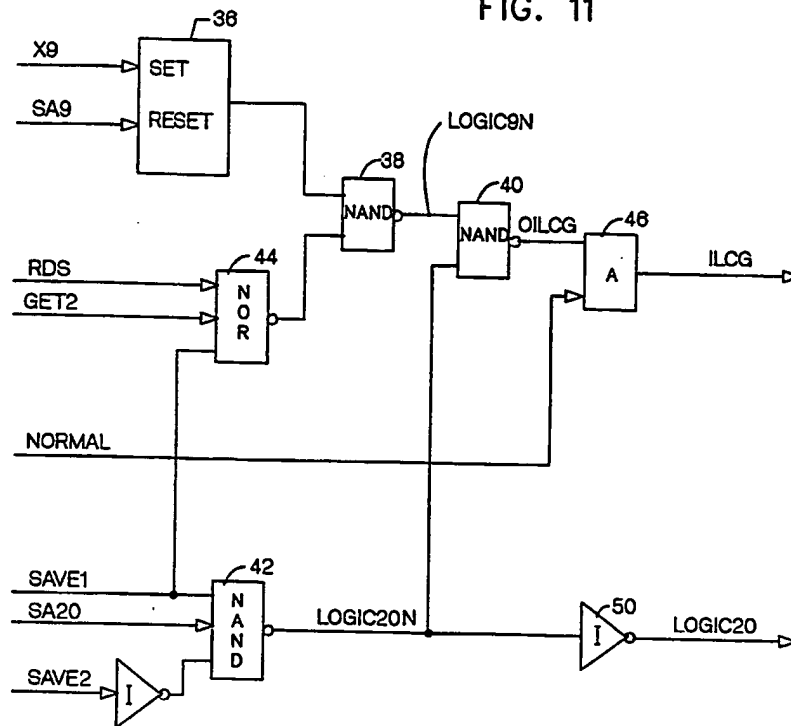
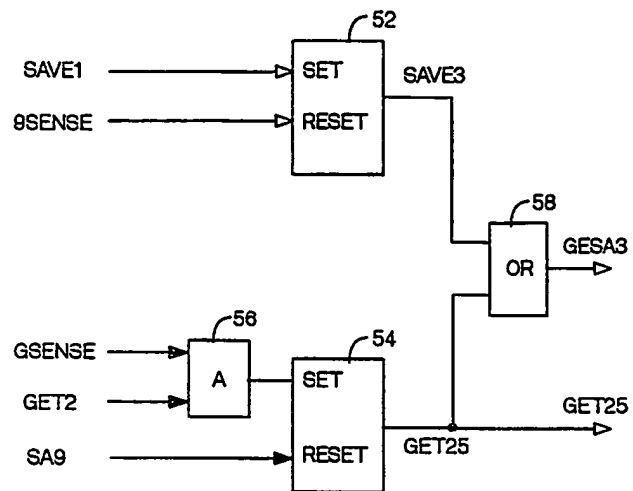


FIG. 12



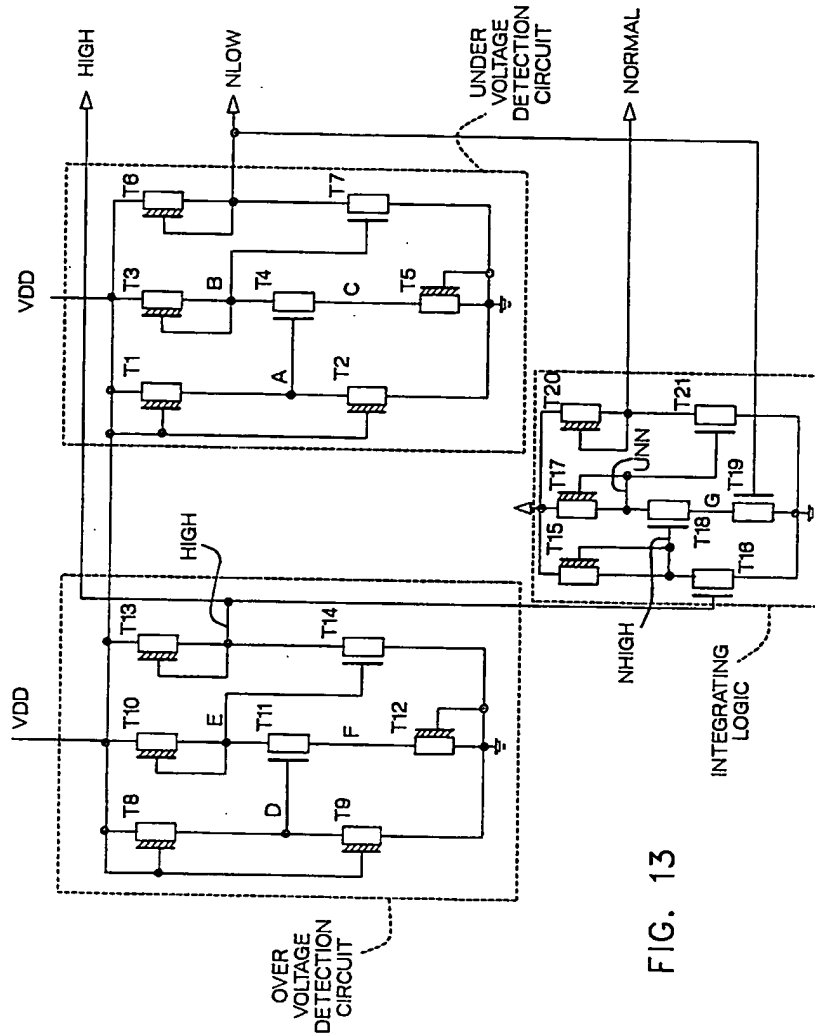


FIG. 13

Doluca et al.

[11] Patent Number: 4,769,784

[45] **Date of Patent:** Sep. 6, 1988

[54] CAPACITOR-PLATE BIAS GENERATOR FOR CMOS DRAM MEMORIES

[75] Inventors: Sinan Doluca, Santa Clara; Robert Yan, Cupertino, both of Calif.

[73] Assignee: Advanced Micro Devices, Inc.,  
Sunnyvale, Calif.

[21] Appl. No.: 897,893

[22] Filed: Aug. 19, 1986

[51] Int. Cl.<sup>4</sup> ..... G11C 11/24

[52] U.S. Cl. .... 365/149; 365/189;  
365/226; 307/297

[58] Field of Search ..... 365/149, 189, 226, 227;  
307/297, 296 R

## [56] References Cited

## U.S. PATENT DOCUMENTS

3,909,631	9/1975	Kitagawa .....	307/297
4,259,729	3/1981	Tokushige .....	365/149
4,375,596	3/1983	Hoshi .....	307/297

4,581,546	4/1986	Allan .....	307/297
4,593,382	6/1986	Fujishima et al. ....	365/149
4,670,861	6/1987	Shu et al. ....	365/226

*Primary Examiner*—Stuart N. Hecker

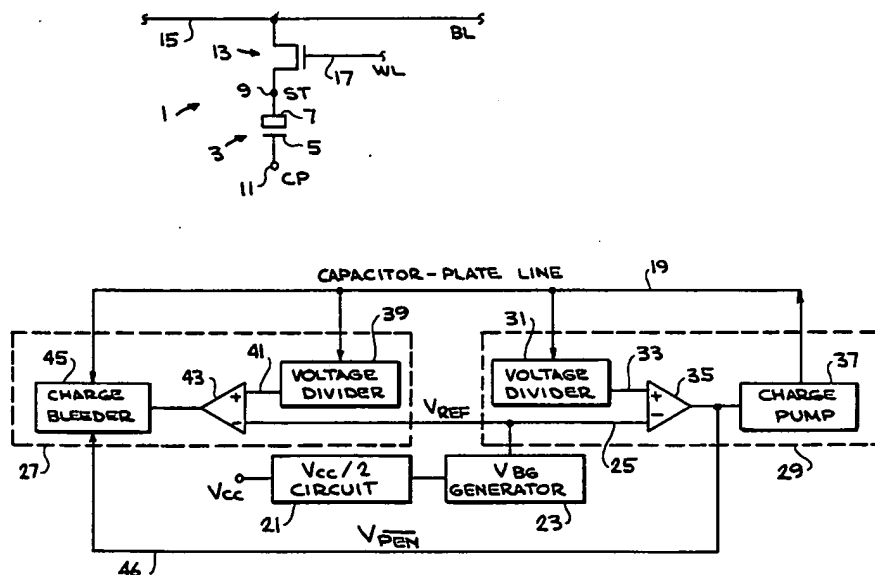
*Assistant Examiner—Glenn A. Gossage*

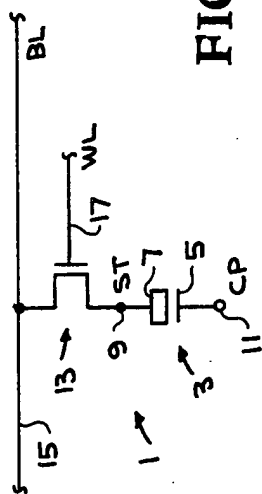
**Attorney, Agent, or Firm—Davis Chin; Eugene H. Valet**

[57]                      **ABSTRACT**

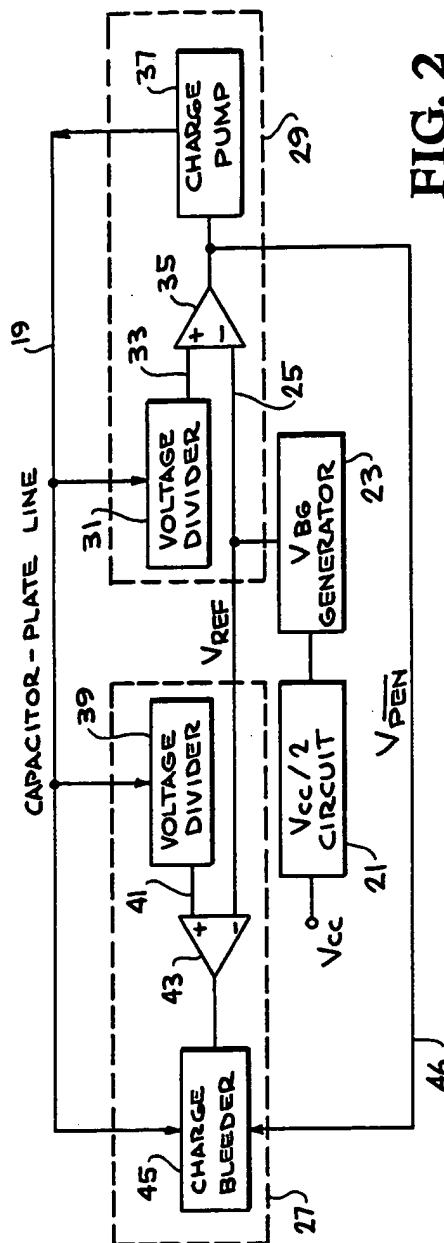
A capacitor-plate bias generator produces a voltage on the capacitor plate node which consists of a constant voltage plus the sense-level voltage. Consequently, the capacitor-plate node tracks any variations in the sense-level voltage. The constant voltage is  $3V_{BG}$ , or 3 times the bandgap voltage of silicon. The circuit includes a reference-voltage source which produces the sum of the sense-level voltage and  $V_{BG}$ , and a feedback control circuit for enabling either a charge pump or a charge bleeder to regulate the capacitor-plate voltage at a level above the circuit supply voltage.

**25 Claims, 3 Drawing Sheets**

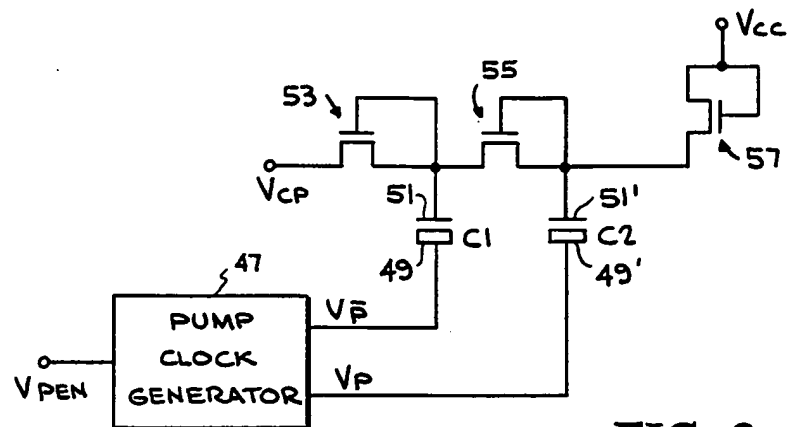




**FIG. 1**



**FIG. 2**



**FIG. 3**

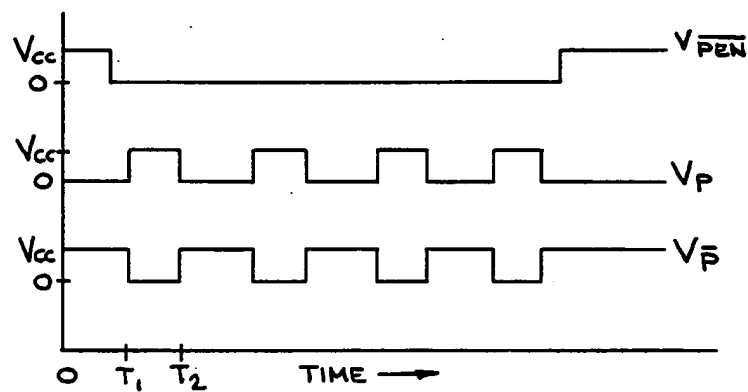


FIG. 4.

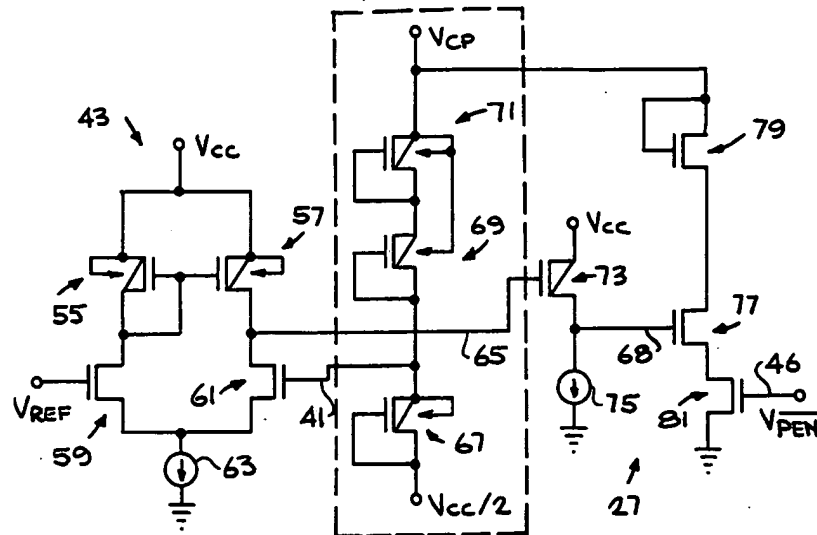


FIG. 5

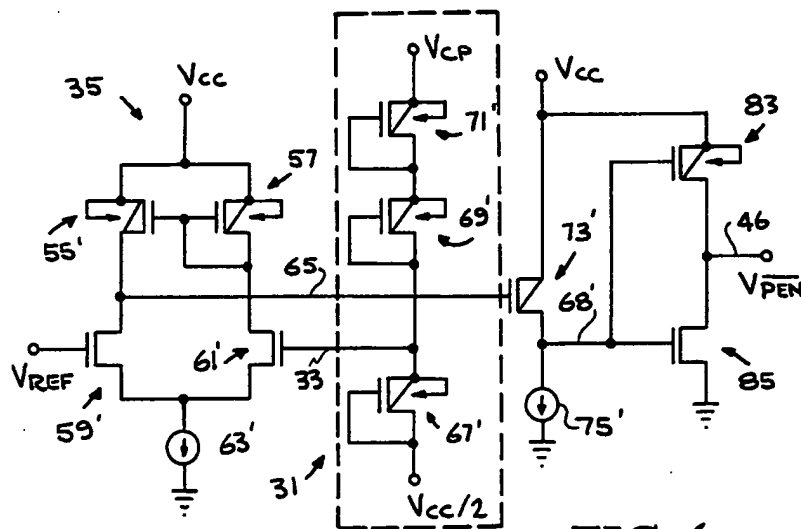


FIG. 6

## CAPACITOR-PLATE BIAS GENERATOR FOR CMOS DRAM MEMORIES

### BACKGROUND OF THE INVENTION

The present invention relates generally to dynamic read-write randomly accessible memory devices (DRAMs), more particularly to dynamic RAMs which use a grooved-surface structure to achieve a very high density of capacitive memory elements, and especially to a capacitor-plate bias generator circuit for such memory devices.

Digital information is stored in the form of capacitive charge in a matrix-array of many capacitive elements in the DRAM memory device. Recently, certain advances in the manner of forming the capacitive memory elements have increased the density of memory elements on each silicon wafer or chip.

One such advance has involved the provision of a grooved-surface microstructure on the silicon wafer, such that the surface area available for the formation of capacitive memory elements is increased substantially as compared to the planar structures formerly in use. However, the use of such a groove technology in forming the capacitive elements has resulted in changes in the capacitor structure which have set new requirements for the capacitor-plate bias voltage, as will appear from the detailed discussions later in this patent application.

In order that the newer groove technology results in reliable memory devices having the desired characteristics of high density and very low soft error rate, a new capacitor-plate bias generator circuit was needed. For reasons which will be discussed in the later portions of this application, the bias generator must generate a voltage which is higher than the  $V_{CC}$  voltage in use in the device, must be stable over a wide range of operating conditions, and must be insensitive to normal process and temperature variations.

### DESCRIPTION OF THE RELATED ART

A copending application, entitled *Midpoint Sense Amplification Scheme for a CMOS DRAM*, Ser. No. 06/740,356, filed June 3, 1985, now U.S. Pat. No. 4,694,205 and commonly assigned with the present invention, covers a novel system for controlling the sense amplification rate at the inputs of a CMOS sense amplifier. Like the present invention, the system is designed for use in a midpoint sensing scheme, i.e., one in which the 1 and 0 logic states of the memory cells are represented by  $V_{CC}$  volts and 0 volts, respectively, and the bit-lines are pre-charged at the beginning of each sense cycle to the midpoint of these two voltages, which is  $V_{CC}/2$ .

The above copending application also contains citations to other related art describing CMOS DRAMs using a similar sense cycle in which the bit-lines are pre-charged to a  $V_{CC}/2$  level. As will appear from the later descriptions of this application, such schemes ideally require that the voltages across the capacitive memory elements be referenced to a voltage which is dependent upon and tracks the  $V_{CC}/2$  voltage of the bit-lines.

### SUMMARY OF THE INVENTION

An object of the present invention is to produce a capacitor-plate bias voltage suitable for use in a CMOS DRAM using a  $V_{CC}/2$  sense scheme.

A second object of the present invention is to produce such a capacitor-plate bias voltage such that the

voltage depends upon and tracks the variations of the  $V_{CC}/2$  voltage.

A third object of the present invention is to produce such a capacitor-plate bias voltage having a magnitude of  $V_{CC}/2 + K$ , where  $K$  is a constant.

A fourth object of the present invention is to produce a capacitor-plate bias voltage having a magnitude greater than  $V_{CC}$ .

A fifth object of the present invention is to produce a capacitor-plate bias voltage having a magnitude greater than  $V_{CC}$  without requiring a source of voltage higher than  $V_{CC}$ .

To the above ends, a capacitor-plate bias generator according to the present invention includes a reference generator which produces a stable output voltage having a value of  $V_{CC}/2 + V_{BG}$ , where  $V_{BG}$  is the bandgap voltage of Silicon. The output voltage of this reference generator is coupled to one input of a charge-pump enable circuit, a second input of which is derived from the output or capacitor-plate voltage.

A charge pump under the control of the charge-pump enable circuit is used to pump sufficient charge into the capacitor-plate node to raise its voltage above the  $V_{CC}$  level. The charge pump may, for example, raise the voltage of this node to approximately  $V_{CC}/2 + 3V_{BG}$ .

The output voltage of the reference generator is also coupled to one input of a capacitor-plate bleeder circuit, a second input of which is derived from the output or capacitor-plate voltage. The capacitor-plate bleeder circuit establishes an upper voltage limit for the capacitor-plate node. When this limit is reached, a charge bleeder is activated to reduce the voltage slightly.

Together, the charge pump and charge bleeder are operated in such a way as to cause the capacitor-plate voltage to remain within a narrow range around a design voltage chosen large enough to permit the use of  $V_{CC}$  volts as the logic 1 voltage and 0 volts as the logic 0 voltage.

The above and other features, objects, and advantages of the present invention, together with the best mode contemplated by the inventors for carrying out their invention will become more apparent from reading the following detailed description of the invention and from studying the associated drawing, the various figures of which represent:

### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a simplified showing of a single capacitive memory cell according to the present invention;

FIG. 2 is a block-schematic representation of a capacitor-plate bias circuit according to the present invention;

FIG. 3 is a schematic representation of a charge pump according to the present invention;

FIG. 4 is a timing diagram of voltage waveforms in the circuit of FIG. 3.

FIG. 5 is a schematic diagram of the circuit within the left dotted rectangle in FIG. 2;

FIG. 6 is a schematic diagram of a portion of the circuit within the right dotted rectangle in FIG. 2.

### DETAILED DESCRIPTION OF THE PRESENT INVENTION

In FIG. 1, a single capacitive memory cell 1 has been illustrated in a much simplified and idealized form. A capacitive memory element 3 has an anode electrode 5 and a cathode electrode 7. Cathode 7 is connected to a



storage node 9, while anode electrode 5 is connected, in common with the anodes of the other capacitive memory elements in the matrix-array memory device (not shown) of which cell 1 is a part, to a capacitor-plate node 11.

A single data bit is stored in cell 1 and is represented by the voltage of storage node 9. Access to node 9 is controlled by a word-select gate transistor 13 which couples node 9 to a bit-line 15 whenever the potential on a word-line 17 goes high.

In one preferred scheme, logic 0 data is represented by 0 volts on node 9, logic 1 data is represented by a voltage of  $V_{CC}$  on node 9, and bit-line 15 is pre-charged to a voltage which is the midpoint of these values, or  $V_{CC}/2$  prior to connecting bit-line 15 to node 9 to read the data in cell 1.

Capacitor 3 is formed with a silicon cathode, a polysilicon anode, and with a relatively thin dielectric layer of, for example, 150 Angstroms of  $SiO_2$  separating its cathode and anode. Such a capacitive structure has a threshold voltage  $V_T$  of approximately 0.4 to 1.0 volts, depending on temperature. Consequently, the capacitor-plate node 11 must always be held at a voltage which is more positive than the voltage of the storage node 9 by  $V_T$  volts or more.

On the other hand, the relatively thin dielectric layer establishes an upper limit of about 10 volts that can safely be supported without fear of destruction of the dielectric. When the data in cell 1 is a 0, the voltage across capacitor 3 is  $V_{CP}$ , the voltage of capacitor-plate node 11.

Since the voltage level at which sensing occurs is the voltage of bit-line 15, an optimum voltage source for biasing the capacitor-plate node 9 should track this bit-line voltage. Finally, since the bit-line pre-charge voltage is  $V_{CC}/2$ , the voltage of the capacitor-plate bias source should be function of  $V_{CC}/2$  such that it follows any variations of bit-line voltage exactly.

Taking these requirements together, we can say that the ideal capacitor-plate bias source should produce a voltage:

$$V_{CP} = V_{CC}/2 + K, \text{ where } K \text{ is a constant having a value:}$$

$$K > V_{CC}/2 + V_T$$

If we consider that nominal values for  $V_{CC}$  and  $V_T$  might be on the order of 5 volts and 1 volt respectively, then the above relations suggest that  $K$  might be chosen to be 3.5 to 4, resulting in a value of  $V_{CP}$  of approximately 6 to 6.5 volts. The requirement that  $V_{CP}$  track  $V_{CC}/2$  results in that  $V_{CP}$  must increase or decrease by 0.5 volt in response to a 1.0 volt increase or decrease in  $V_{CC}$ , for example.

Turning now to FIG. 2, the circuit arrangement necessary to provide the capacitor-plate bias according to the present invention is shown in block-schematic form. A capacitor-plate line 19 at the top of the figure represents all the capacitor-plate nodes 11 of FIG. 1 whose voltage must be established and maintained in accordance with the foregoing criteria.

A  $V_{CC}/2$  circuit 21, which may be nothing more than a voltage divider, connects to a source of voltage  $V_{CC}$  at its input, and provides a voltage  $V_{CC}/2$  to a  $V_{BG}$  generator 23 at its output.  $V_{BG}$  generator 23 generates a voltage  $V_{BG}$  which is a stable facsimile of the bandgap voltage of silicon, or about 1.2 volts. Any of the known circuits for producing  $V_{BG}$ , such as the one discussed at

pp. 254-261 of *Analysis and Design of Analog Integrated Circuits* by Gray and Meyer, published by John Wiley, 1977, may be used as  $V_{BG}$  generator 23.

The output of generator 23, consisting of the sum of  $V_{CC}/2$  and  $V_{BG}$  is connected to a  $V_{REF}$  line 25, such that:

$$V_{REF} = V_{CC}/2 + V_{BG}$$

The function of the remainder of the circuitry of FIG. 2 can be summarized as the utilization of  $V_{REF}$  to establish and maintain a voltage on line 19 of  $V_{CC}/2 + K$ , in accordance with the discussion of FIG. 1 above. The method of doing this involves the periodic pumping of charge into line 19 to raise its potential and the periodic bleeding of charge from line 19 to lower its potential.

A bleeder control circuit 27, enclosed within the left dotted line produces and controls a bleeding of charge from the line 19, while a pump control circuit 29, enclosed within the right dotted line produces and controls the pumping of charge onto line 19.

As can be surmised from a brief study of FIG. 2, each of circuits 27 and 29 uses a scheme which may be summarized as follows: Derive a voltage which is a certain fraction of the voltage on line 19, compare this voltage with the  $V_{REF}$  voltage on line 25, and turn the charge pump or charge bleeder on or off in response to the difference between these two voltages.

Pump control circuit 29 thus includes a voltage divider 31 having an input connected to line 19 and having an output line 33 connected to one input of a comparator 35. As will be shown in the later detailed description of the circuitry used to realize the function of pump control circuit 29, the voltage produced on line 33 by divider 31 is:

$$V_{33} = (V_{CP} - V_{CC}/2)/3 + V_{CC}/2.$$

Comparator 35 compares  $V_{33}$  with  $V_{REF}$  and produces at its output a signal which turns on a charge pump 37 whenever

$$V_{33} \leq V_{REF}$$

Since  $V_{REF} = V_{CC}/2 + V_{BG}$ , this turn-on condition may be restated as:

$$[(V_{CP} - V_{CC}/2)/3] \leq V_{BG}, \text{ or}$$

$$[V_{CP} \leq 3V_{BG} + V_{CC}/2.]$$

Bleeder control circuit 27 includes a voltage divider 39 having an input connected to line 19 and having an output line 41 connected to one input of a comparator 43. The voltage produced on line 41 by divider 39 is:

$$V_{41} = (V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta.$$

Thus  $V_{41}$  differs from  $V_{33}$  above only by a small offset voltage  $\Delta$ . Comparator 43 compares the voltage on line 41 with  $V_{REF}$  and produces at its output a signal which turns on a charge bleeder 45 whenever

$$(V_{CP} - V_{CC}/2)/3 + V_{CC}/2 - \Delta \leq V_{REF}.$$

It can be shown that this bleeder turn-on condition ensures that:

$$V_{CP} \approx 3V_{BG} + V_{CC}/2 + 3\Delta.$$

Considering the pump and bleeder turn-on conditions together, it can be seen that the voltage on line 19 will be regulated between:

$$3V_{BG} + V_{CC}/2 \leq V_{CP} \leq 3V_{BG} + V_{CC}/2 + 3\Delta$$

In the interest of minimizing wasted power, the pump and bleeder should not operate simultaneously. The circuit of FIG. 2 provides two mechanism for avoiding such simultaneous operation: (1) the voltage  $V_{CP}$  at which the bleeder turns off is greater than the voltage  $V_{CP}$  at which the pump turns on by  $3\Delta$ ; (2) the  $V_{PEN}$  voltage produced by comparator 35 is fed back along line 46 to bleeder control circuit 27, where it disables charge bleeder 45 whenever charge pump 37 is in operation.

Turning now to FIGS. 3 and 4, a circuit realization of charge pump 37 is shown to include a pump clock generator 47, represented in schematic-block form. Clock generator 47 receives a negative-going pump-enabling input signal  $V_{PEN}$  and produces in response a biphasic pair of output signals  $V_P$  and  $V_P$ . These output signals are in turn connected to the cathode electrodes 49 and 49' of a pair of capacitors C1 and C2; the anode electrodes 51 and 51' of which connect to a pair of pass transistors 53 and 55. A charging transistor 57 supplies current from a source of voltage  $V_{CC}$ .

In the following discussion of the operation of this pump, it will be assumed that each of transistors 53, 55, and 57 has a threshold voltage of  $V_T$  volts, representing a loss or drop in voltage during conduction. However, capacitors C1 and C2 are assumed to have a negligible threshold voltage by being realized in a form, and with doping levels chosen, to eliminate their  $V_T$ .

Prior to the start of the operational cycle, i.e., at time 0 in FIG. 4, anode 51' will have been charged to a voltage of  $V_{CC} - V_T$  volts by transistor 57. Consequently, when signal  $V_P$  drives cathode 49' from 0 volts to  $V_{CC}$  volts at time  $T_1$ , anode 51' is also raised in potential, and would reach a voltage of  $2V_{CC} - V_T$  but for the fact that pass transistors 55 turns on, causing the charge on anode 51' to be shared with anode 51. During the next change of phase of the biphasic signals, some of this charge is transferred to the terminal  $V_{CP}$  through pass transistor 53.

Terminal  $V_{CP}$  is connected to capacitor plate line 19 in FIG. 2, such that this line is gradually pumped to a higher potential throughout the duration of the pump-enabling signal  $V_{PEN}$ . The limiting potential which can be reached using this pump design is  $3V_{CC} - 3V_T$ . Since  $V_T$  may be up to 1.5 volt, this pumping limit may be approximately 10 volts for a  $V_{CC}$  value of 5.

FIG. 5 shows, in schematic form, the details of a circuit which realizes the functions of bleeder control circuit 27 in FIG. 2. FIGS. 5 and 6 are illustrated as the corresponding circuits which would be if formed using an n-well process technology. That is, n-channel transistors are assumed to be formed directly in the p-substrate, while p-channel transistors, formed in an n-well in the p-substrate, are illustrated including an arrow symbolizing the n-well substrate.

In all except one of the p-channel transistors, the n-well substrate connects to the source electrode of the same transistor, as shown in FIGS. 5 and 6. It will be understood, however, that the present invention is equally applicable to devices utilizing p-well process

technology, such that n-channel transistors would be formed in a p-well.

Comparator 43 is shown to include a pair of p-channel transistors 55 and 57, each having its source connected to  $V_{CC}$ , and a pair of n-channel transistors 59 and 61, connected as a differential pair to a current source 63. The gate electrodes of transistors 55 and 57 are commonly connected to the drain electrode of transistor 59. An output driver transistor 73 receives the drain voltage of transistor 61 on line 65, connected to the gate of transistor 73. The source of transistor 73 is connected to  $V_{CC}$ , while its drain is connected to a current source 75.

The gate of transistors 59 receives the  $V_{REF}$  voltage from line 25 in FIG. 2, while the gate of transistor 61 is connected to line 41 to receive the output from voltage divider 39. Comparator 43 has very high gain, on the order to 10,000, and produces an output on line 68 which swings from 0 volts to  $V_{CC}$  volts when the voltage on line 41 exceeds  $V_{REF}$  by a few millivolts.

Voltage divider 39 consists of a series string of three p-channel transistors 67, 69, and 71, each with its gate and drain electrodes interconnected. The  $V_{CP}$  input from line 19 in FIG. 2 is connected to the source of transistor 71, while the drain of transistor 67 is connected to a voltage of  $V_{CC}/2$ . Thus, the voltage drop across the entire divider chain is  $V_{CP} - V_{CC}/2$ . Since line 41 connects to the source of transistor 67, the lowest in the chain of three, the voltage at this point would, if the three transistors were identically formed and connected, be:

$$[(V_{CP} - V_{CC}/2)/3] + V_{CC}/2.$$

However, the symmetry of divider 39 has been deliberately disturbed by connecting the substrate of transistor 69 to the source of transistor 71, while the substrates of each of transistors 71 and 67 is connected in the normal manner, each one to the source of its own transistor. The effect of this asymmetry is to cause the voltage drop across transistor 69 to be increased by a small amount while the voltage drop across each of the other transistors is decreased by a small amount.

If we arbitrarily call the increase in the voltage across transistor 69  $2\Delta$ , then the decrease in drop across each of the other transistors is one half of this amount, or  $\Delta$ . Consequently, the voltage output from divider 39 at line 41 is:

$$V_{41} = [(V_{CP} - V_{CC}/2)/3] + V_{CC}/2 - \Delta,$$

as was stated above in the description of FIG. 2.

The drain electrode of transistor 73 is connected to the gate of a transistor 77. The drain of transistor 77 is coupled, through a current-regulating transistor 79, to  $V_{CP}$  on line 19 of FIG. 2. Transistor 79 serves as a non-linear current regulator having a generally parabolic current-voltage characteristic.

A gate transistor 81 is connected with its drain to the source of transistor 77, and with its source to ground. The gate of transistor 81 receives the  $V_{PEN}$  voltage on the line 46 and disables the bleeder 27 whenever charge pump 37 is on.

In FIG. 6, the circuitry for realizing the pump control circuit 29 of FIG. 2 is shown. Primed reference numbers indicate parts of FIG. 6 which correspond with unprimed reference numbers in FIG. 5. The comparator 35 is very similar to the comparator 43 discussed above

with respect to FIG. 5, and differs only in the following respects: The common gate connection of p-channel transistors 55' and 57' is connected to the drain of transistor 61', and the comparator output line 65' connects to the drain of transistor 59'.

Similarly, voltage divider 31 functions exactly like voltage divider 39 except that it is entirely symmetrical, such that the output voltage produced by divider 31 on line 33 is  $\frac{1}{2}$  of the voltage difference across the entire divider string plus  $V_{CC}/2$ , or:

$$V_{33} = (V_{CP} - V_{CC}/2)/3 + V_{CC}/2,$$

which agrees with the expression for this voltage above in the discussion of FIG. 2.

The output of comparator 35 on line 65' goes low whenever  $V_{33}$  drops below  $V_{REF}$ , and this low output is coupled through a driver transistor 73' to the commonly connected gates of an inverting output pair of transistors 83 and 85. The high voltage on the common gate connection of these transistors turns transistor 83 off, and transistor 85 on. As a result, the output voltage on the line 46 drops, initiating the active low  $V_{PEN}$  output signal on line 46.

Although this invention has been described with some specificity in reference to embodiments thereof which represent the best mode known to the inventors for carrying out their invention, many changes could be made and many alternative embodiments could thus be derived without departing from the scope of the invention. Consequently, the scope of the invention is to be determined only from the following claims.

We claim:

1. In a dynamic, randomly-accessible memory (DRAM) of the type employing capacitive memory elements, each of said memory elements having an anode and a cathode, wherein a bit-line, pre-charged to a predetermined voltage prior to sensing data in a memory element, accesses the cathode of a memory element to sense the data therein, the anodes of all the capacitive memory elements being connected in common to a capacitor-plate node, a capacitor-plate bias generator for establishing and maintaining a voltage on said capacitor-plate node, comprising in combination;

charge pump means for pumping electrical charge into said capacitor-plate node, to thereby raise the potential of said node;

charge bleeder means for bleeding charge from said capacitor-plate node, to thereby lower the potential of said node;

a source of reference voltage;

feedback control means for comparing the voltage of said capacitor-plate node to said reference voltage and for initiating operation of a selected one of said charge pump means and said charge bleeder means to maintain said capacitor-plate voltage within a preselected range of voltages;

said feedback control means being formed of a pump control circuit and a bleeder control circuit;

said pump control circuit including first voltage divider means for deriving a first control voltage having a known relationship with the voltage of said capacitor-plate node, first comparator means for comparing said first control voltage with said reference voltage and for producing in response to the difference therebetween a first error voltage, and pump drivers means responsive to said first error voltage for producing a pump-enabling signal

when said first control voltage is less than said reference voltage; and

said bleeder control circuit including second voltage divider means for deriving a second control voltage having a known relationship with the voltage of said capacitor-plate node, second comparator means for comparing said second control voltage with said reference voltage and for producing in response to the difference therebetween a second error voltage, and bleeder means responsive to said second error voltage for producing a bleeding of charge from said capacitor-plate node when said second control voltage is greater than said reference voltage.

2. The apparatus of claim 1 wherein said bleeder control circuit further comprises bleeder gate means, connected to said pump control circuit to receive therefrom said pump enabling signal and responsive thereto to disable said bleeder means when said pump is enabled.

3. The apparatus of claim 1 wherein said charge pump means comprises:

a pump clock for receiving a pump-enabling input signal and for generating in response thereto a complementary pair of biphasic alternating output signals;

a first capacitor having an anode, and having a cathode connected to receive a first of said biphasic signals, and a second capacitor having an anode, and having a cathode connected to receive a second of said biphasic signals;

charging means to charge said capacitors and to produce thereacross a voltage at each capacitor anode which is higher than the voltage at the capacitor cathode;

coupling means to couple one of said capacitor anodes to said capacitor-plate node whenever said one capacitor anode is at a voltage exceeding the voltage of said capacitor-plate node by a certain threshold voltage  $V_T$ , and to decouple said one capacitor anode otherwise.

4. The apparatus of claim 3 wherein the one of said capacitor anodes coupled to said capacitor-plate node is said first capacitor anode, and wherein said coupling means further couples said second capacitor anode to said first capacitor anode whenever the voltage on said second capacitor anode exceeds the voltage of said first capacitor anode by  $V_T$ .

5. The apparatus of claim 1 wherein said first and second control voltages differ.

6. The apparatus of claim 5 wherein said second control voltage is less than said first control voltage by a fixed deviation voltage  $\Delta$ .

7. The apparatus of claim 5 wherein said first voltage divider means comprises a first series string of a plurality of  $n$  FET transistors, where  $n$  is an integer having a value of 2 or greater, each of said transistors in said first series string having a source, a drain, a gate, and a substrate connected to its source, and wherein said second voltage divider means comprises a second series string of a plurality of  $n$  FET transistors, where  $n$  is an integer having a value of 2 or greater, each of said transistors in said second series string having a source, a drain, a gate, and a substrate, one of said transistors in said second string having its substrate connected to a circuit node at a potential different from the potential of its source.

8. The apparatus of claim 1 wherein said reference voltage tracks variations in said predetermined voltage,

whereby said capacitor-plate bias generator maintains said capacitor-plate node at a voltage which also tracks variations in said predetermined voltage.

9. The apparatus of claim 8 wherein said capacitor-plate bias generator maintains said capacitor-plate node at a voltage which consists of a constant voltage and said predetermined voltage.

10. The apparatus of claim 9 wherein said constant voltage is  $3V_{BG}$ , where  $V_{BG}$  is the bandgap voltage of silicon.

11. The apparatus of claim 8 wherein said reference voltage consists of a constant voltage component and said predetermined voltage.

12. The apparatus of claim 11 wherein said constant voltage component is  $V_{BG}$ , the bandgap voltage of silicon.

13. The apparatus of claim 11 wherein said predetermined is  $V_{CC}/2$  volts, where  $V_{CC}$  is the common circuit supply voltage, and wherein said reference-voltage source comprises:

voltage means, connected to said common circuit supply voltage  $V_{CC}$ , for producing a voltage  $V_{CC}/2$  equivalent to said predetermined; voltage generator means for receiving said  $V_{CC}/2$  voltage from said voltage divider means, for generating a constant voltage component, and for combining said  $V_{CC}/2$  voltage and said constant voltage component to produce an output reference voltage.

14. The apparatus of claim 13 wherein said voltage generator means generates a constant voltage component  $V_{BG}$  which is the bandgap voltage of silicon, and combines said  $V_{CC}/2$  and  $V_{BG}$  voltages to produce an output reference voltage  $V_{REF}$  defined as:

$$V_{REF} = V_{CC}/2 + V_{BG}$$

15. The apparatus of claim 14 wherein said capacitor-plate bias generator maintains said capacitor-plate voltage  $V_{CP}$  at a value of

$$3V_{BG} + V_{CC}/2 \pm V_{CP}3V_{BG} + V_{CC}/2 + 3\Delta$$

where  $\Delta$  is a deviation from  $3V_{BG} + V_{CC}/2$ .

16. In a dynamic, randomly-accessibly memory (DRAM) of the type employing capacitive memory elements, each of said memory elements having an anode and a cathode, wherein a bit-line, pre-charged to a predetermined voltage prior to sensing of data in a memory element, accesses the cathode of a memory element to sense the data therein, the anodes of all the capacitive memory elements being connected in common to a capacitor-plate node, a capacitor-plate bias generator for establishing and maintaining a voltage on said capacitor-plate node, comprising in combination:

charge pump means for pumping electrical charge into said capacitor-plate node, to thereby raise the potential of said node;

charge bleeder means for bleeding charge from said capacitor-plate node, to thereby lower the potential of said node;

reference-voltage-generating means for generating a reference voltage consisting of a constant voltage component and said predetermined voltage;

feedback control means for comparing the voltage of said capacitor-plate node to said reference voltage and for initiating operation of a selected one of said charge pump means and said charge bleeder means

to maintain said capacitor-plate voltage within a preselected range of voltages;

said feedback control means being formed of a pump control circuit and a bleeder control circuit;

said pump control circuit including first voltage divider means for deriving a first control voltage having a known relationship with the voltage of said capacitor-plate node, first comparator means for comparing said first control voltage with said reference voltage and for producing in response to the difference therebetween a first error voltage, and pump driver means responsive to said first error voltage for producing a pump-enabling signal when said first control voltage is less than said reference voltage; and

said bleeder control circuit including second voltage divider means for deriving a second control voltage having a known relationship with the voltage of said capacitor-plate node, second comparator means for comparing said second control voltage with said reference voltage and for producing in response to the difference therebetween a second error voltage, and bleeder means responsive to said second error voltage for producing a bleeding of charge from said capacitor-plate node when said second control voltage is greater than said reference voltage.

17. The apparatus of claim 16 wherein said constant voltage component is  $V_{BG}$ , the bandgap voltage of silicon.

18. The apparatus of claim 16 wherein said bleeder control circuit further comprises bleeder gate means, connected to said pump control circuit to receive therefrom said pump enabling signal and responsive thereto to disable said bleeder means when said pump is enabled.

19. The apparatus of claim 16 wherein said capacitor-plate bias generator maintains said capacitor-plate node at a voltage which consists of a constant voltage and said predetermined voltage.

20. The apparatus of claim 19 wherein said constant voltage is  $3V_{BG}$ , where  $V_{BG}$  is the bandgap voltage of silicon.

21. The apparatus of claim 16 wherein said predetermined voltage is  $V_{CC}/2$  volts, where  $V_{CC}$  is the common circuit supply voltage, and wherein said reference-voltage source comprises:

voltage divider means, connected to said common circuit supply voltage  $V_{CC}$ , for producing a voltage  $V_{CC}/2$  equivalent to said predetermined voltage;

voltage generator means for receiving said  $V_{CC}/2$  voltage from said voltage divider means, for generating a constant voltage component, and for combining said  $V_{CC}/2$  voltage and said constant voltage component to produce an output reference voltage.

22. The apparatus of claim 21 wherein said voltage generator means generates a constant voltage component  $V_{BG}$  which is the bandgap voltage of silicon, and combines said  $V_{CC}/2$  and  $V_{BG}$  voltages to produce an output reference voltage  $V_{REF}$  defined as:

$$V_{REF} = V_{CC}/2 + V_{BG}$$

23. The apparatus of claim 16 wherein said charge pump means comprises:

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a pump clock for receiving a pump-enabling input signal and for generating in response thereto a complementary pair of biphasic alternating output signals;

a first capacitor having an anode, and having a cathode connected to receive a first of said biphasic signals, and a second capacitor having an anode, and having a cathode connected to receive a second of said biphasic signals;

charging means to charge said capacitors and to produce thereacross a voltage at each capacitor anode which is higher than the voltage at the capacitor cathode;

coupling means to couple the first capacitor anode to said capacitor-plate node whenever said first capacitor anode is at a voltage exceeding the voltage of said capacitor-plate node by a certain threshold voltage  $V_T$ , and to couple the second capacitor anode to said first capacitor anode whenever the voltage on said capacitor anode exceeds the voltage of said first capacitor anode by  $V_T$ .

24. The apparatus of claim 23 wherein said first voltage divider means comprises a first series string of a plurality of  $n$  FET transistors, where  $n$  is an integer having a value of 2 or greater, each of said transistors in said first series string having a source, a drain, a gate, and a substrate connected to its source, and wherein said second voltage divider means comprises a second series string of a plurality of  $n$  FET transistors, where  $n$  is an integer having a value of 2 or greater, each of said transistors in said second series string having a source, a drain, a gate, and a substrate, one of said transistors in said second string having its substrate connected to a circuit node at a potential different from the potential of its source.

25. In a dynamic, randomly-accessible memory (DRAM) of the type employing capacitive memory elements, each of said memory elements having an anode and a cathode, wherein a bit-line, pre-charged to a predetermined voltage prior to sensing data in a memory element of  $V_{CC}/2$  where  $V_{CC}$  is a common circuit supply voltage, accesses the cathode of a memory element to sense the data therein, the anodes of all the capacitive memory elements being connected in common to a capacitor-plate node, a capacitor-plate bias

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generator for establishing and maintaining a voltage on said capacitor-plate node, comprising in combination:

charge pump means for pumping electrical charge into said capacitor-plate node, to thereby raise the potential of said node;

charge bleeder means for bleeding charges from said capacitor-plate node, to thereby lower the potential of said node;

reference-voltage-generating means for generating a reference voltage consisting of a  $V_{BG}$  the bandgap voltage of silicon, and said predetermined voltage  $V_{CC}/2$ ; and,

feedback control means for comparing the voltage of said capacitor-plate node to said reference voltage and for initiating operation of a selected one of said charges pump means and said charge bleeder means to maintain said capacitor-plate voltage at a voltage of substantially  $V_{CC}/2$  and a constant voltage of  $3V_{BG}$ ;

said feedback control means including:

a pump control circuit comprising:

first voltage divider means for deriving a first control voltage having a known relationship with the voltage of said capacitor-plate node;

first comparator means for comparing said first control voltage with said reference voltage and for producing in response to the difference therebetween a first error voltage;

pump driver means responsive to said first error voltage to produce a pump-enabling signal when said first control voltage is less than said reference voltage;

a bleeder control circuit comprising:

second voltage divider means for deriving a second control voltage having a known relationship with the voltage of said capacitor-plate node;

second comparator means for comparing said second control voltage with said reference voltage and for producing in response to the difference therebetween a second error voltage;

bleeder means responsive to said second error voltage to produce a bleeding of charge from said capacitor-plate node when said second control voltage is greater than said reference voltage.

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**United States Patent** [19]  
**Bingham et al.**

[11] **Patent Number:** 4,777,577  
[45] **Date of Patent:** \* Oct. 11, 1988

[54] **INTEGRATED DUAL CHARGE PUMP  
POWER SUPPLY AND RS-232  
TRANSMITTER/RECEIVER**

[75] **Inventors:** David Bingham, San Jose; Charles M. Allen, Sunnyvale, both of Calif.

[73] **Assignee:** Maxim Integrated Products, Inc., Sunnyvale, Calif.

[\*] **Notice:** The portion of the term of this patent subsequent to Jan. 13, 2004 has been disclaimed.

[21] **Appl. No.:** 117,992

[22] **Filed:** Nov. 9, 1987

**Related U.S. Application Data**

[63] Continuation of Ser. No. 013,648, May 12, 1987, abandoned, which is a continuation of Ser. No. 782,953, Oct. 1, 1985, Pat. No. 4,636,930.

[51] **Int. Cl.<sup>4</sup>** ..... H02M 7/25

[52] **U.S. Cl.** ..... 363/60; 307/110

[58] **Field of Search** ..... 363/59, 60, 61; 307/109, 110, 284, 305, 567; 320/1

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,636,930 1/1987 Bingham et al. .... 363/60

*Primary Examiner*—Patrick R. Salce

*Assistant Examiner*—Judson H. Jones

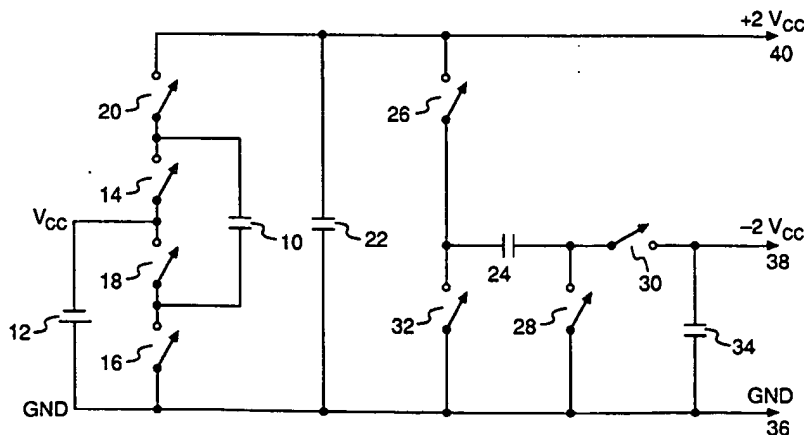
*Attorney, Agent, or Firm*—Lyon & Lyon

[57] **ABSTRACT**

A monolithic integrated circuit containing an inver-

ting/non-inverting voltage doubler charge pump circuit is disclosed for converting a unipolar supply voltage to a bipolar supply voltage of a greater magnitude. The unipolar input voltage is placed across a first external transfer capacitor by a first set of MOS switches during a first time period. The unipolar input voltage source is placed in series with the first transfer capacitor and this series combination of voltages is placed across a first external reservoir capacitor by a second set of MOS switches during a second time period. The voltage appearing across the first external reservoir capacitor is placed on a second transfer capacitor during the first time period by a third set of MOS switches. The voltage across the second transfer capacitor is placed into a second external reservoir capacitor with its polarity inverted by a fourth set of MOS switches during the second time period. A dual-collector lateral junction transistor, formed during the conventional CMOS processing steps used to fabricate the MOS switches, is connected as voltage clamp between a ground potential and the two bipolar DC output lines of the power supply circuit to assure correct start-up conditions for the conduit. Gain reduction devices are placed in the semiconductor substrate to collect minority carriers which would otherwise be injected into inherent parasitic four layer PNPJN junction devices created as a result of the architecture of the circuit, to prevent latch-up of the four layer devices. In a preferred embodiment, an RS-232 receiver and transmitter are contained on the same monolithic integrated circuit as the dual charge pump power supply.

33 Claims, 5 Drawing Sheets



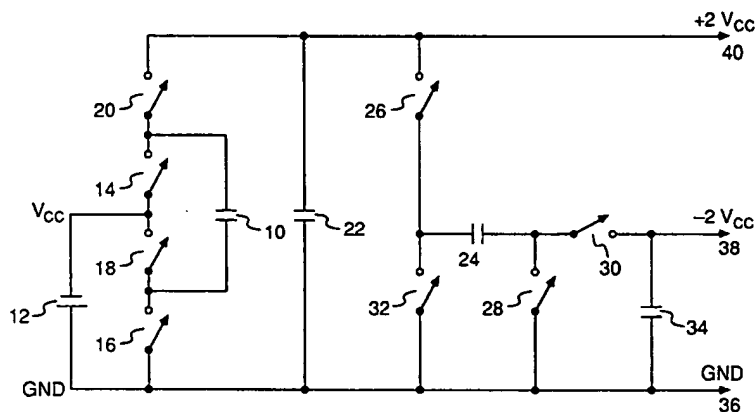


FIGURE 1A

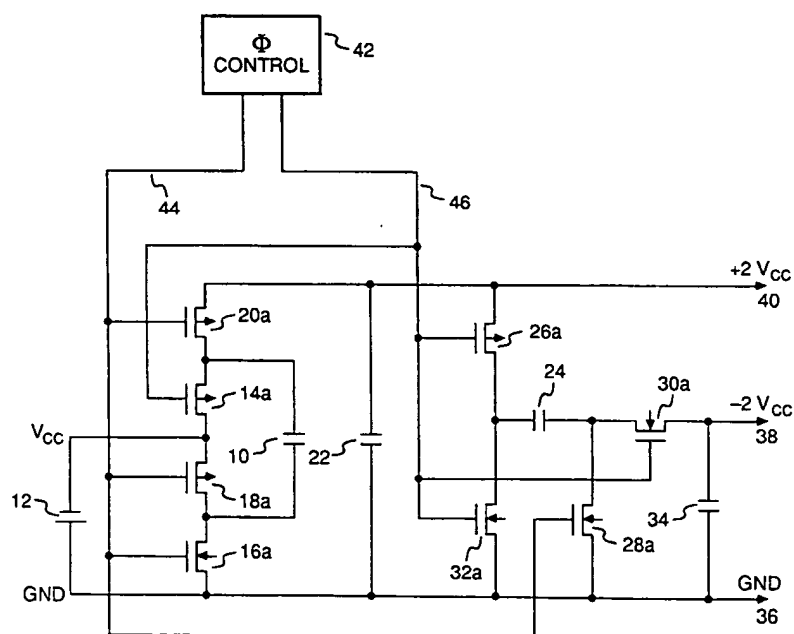


FIGURE 1B

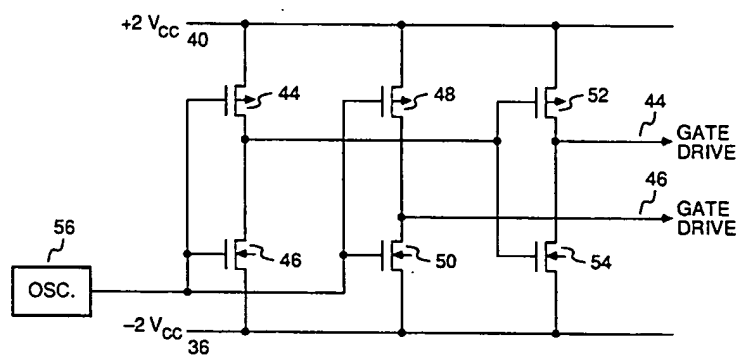


FIGURE 2

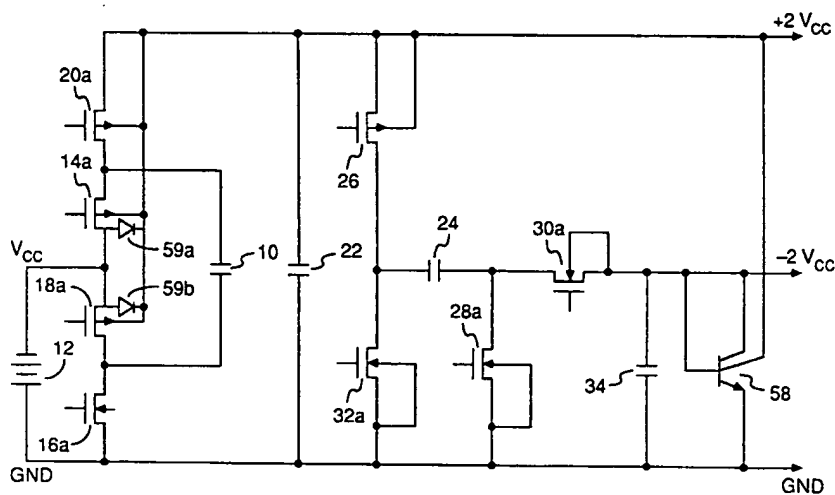


FIGURE 3



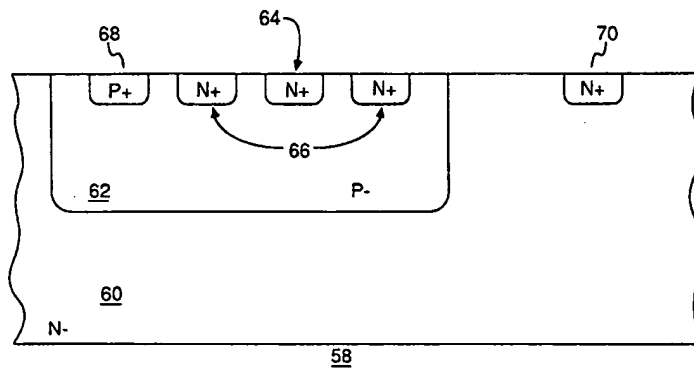


FIGURE 4

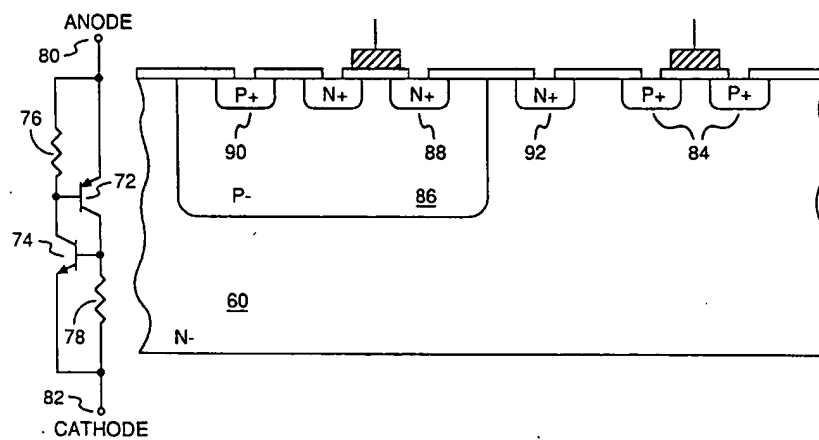


FIGURE 5A

FIGURE 5B

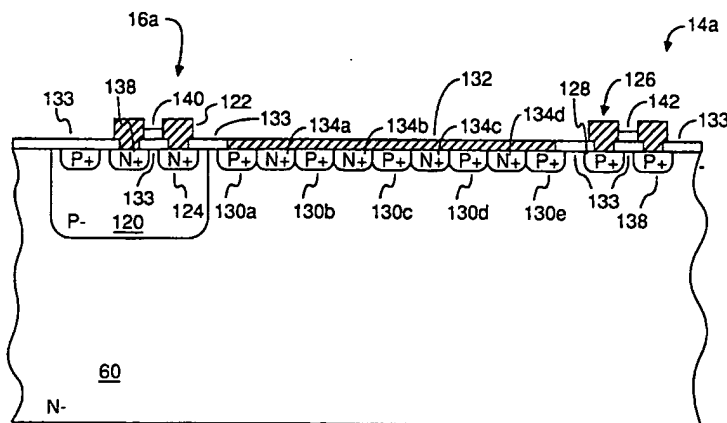


FIGURE 6B

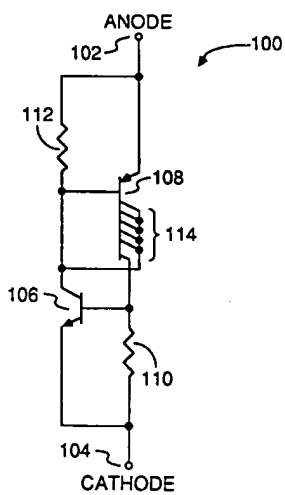


FIGURE 6A

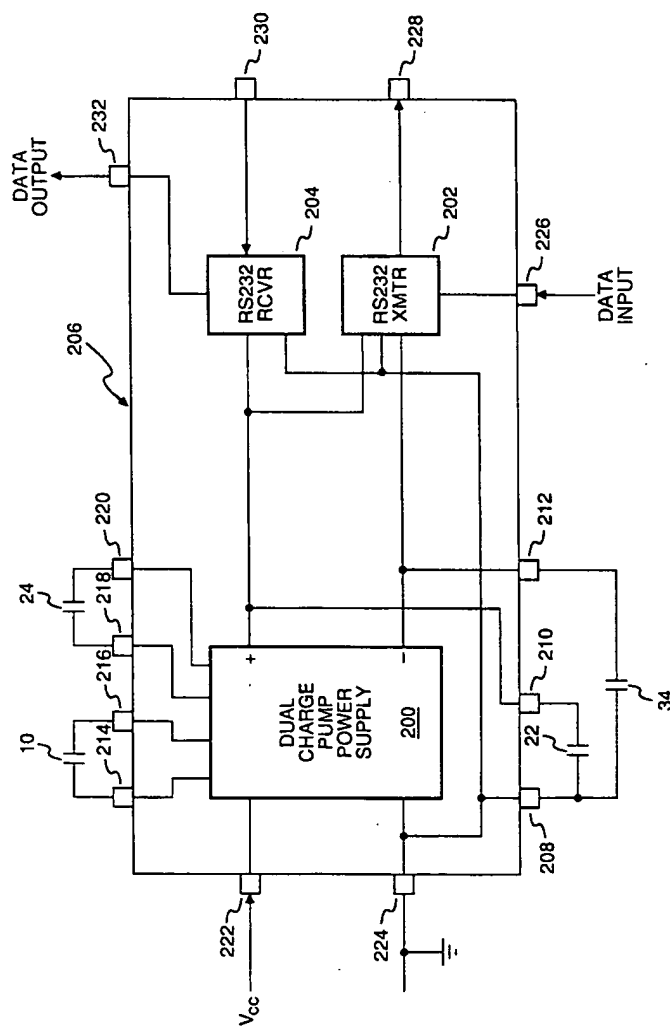


FIGURE 7

# INTEGRATED DUAL CHARGE PUMP POWER SUPPLY AND RS-232 TRANSMITTER/RECEIVER

This is a continuation of application Ser. No. 013,648, filed May 12, 1987, now abandoned, which was a continuation of application Ser. No. 782,953, filed Oct. 1, 1985, now U.S. Pat. No. 4,636,930.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention pertains to charge pump power supplies for generating bipolar output voltages greater in magnitude than a single unipolar input voltage. More particularly, the present invention pertains to the integration of such a circuit on a single piece of semiconductor substrate material. Further, the invention pertains to other circuitry integrable on a single piece of semiconductor substrate material along with such a power supply circuit.

### 2. Prior Art

Discrete component voltage doubler and voltage inverter circuits are well known in the art. Such circuits are used in many electronic systems which require a multiplicity of DC voltages for operation. More recently, in the context of digital circuits and systems, it has become common to employ a single five volt unipolar voltage supply to power digital circuitry in modern data processing systems. For example, semiconductor microprocessors, memories, and logic all commonly operate from a single five volt power supply. There are however, certain interface circuits and other special purpose circuits which require voltages other than five volts. More particularly, some circuits require voltages in the ranges of from five to fifteen volts. Additionally, requirements often exist for bipolar power supply voltages so that voltage power requirements of plus or minus 15 volts and plus or minus 12 volts are commonly encountered, for example in RS-232 communication loops.

For these communication circuits and other applications, bipolar DC power requirements are low when compared to the digital circuitry power requirements. In fact, it is common to encounter five volt unipolar power supplies for driving digital logic rated in tens or hundreds of watts whereas interface and other power requirements may be as low as tens or hundreds of milliwatts.

It is therefore often desirable to generate locally the various non-primary voltage sources, i.e., the bipolar voltage sources, if the power requirements are not high and if it can be done economically and with relatively high electrical power conversion efficiencies.

For an example, a minicomputer may have a 100 watt 5 volt power supply which supplies all of the requirements for a multiplicity of printed circuit boards holding logic integrated circuits. On one of those integrated circuit boards, there will often be an RS-232 digital interface circuit requiring a plus or minus 10 or plus or minus 15 volt power supply. This interface circuit may consume 50 milliwatts of power. Instead of generating the plus and minus 15 volt power supply from the main power supply and then bussing these voltages to the boards which require them, it is often more economical to generate these two voltages from the bussed five volt power supply locally on whatever board needs other voltages. However, generating such voltages by the use of discrete components is often disadvantageous be-

cause the additional components required to generate such voltages take up a relatively large amount of circuit board real estate, and often are power inefficient, i.e., heat producing.

The industry has recently turned its attention to attempts to furnish auxiliary power supplies of the nature herein described on a single semiconductor substrate. Such circuits have the obvious advantages of space saving, assembly labor savings, and relatively lower power dissipation. A form of such circuits known as charge pumps have been used in semiconductor memory chips to produce a crude back bias supply and for supplying the higher voltages needed to program such memory devices. Charge pump circuits have been used in the inverting mode to produce voltage polarities opposite to that of the supply voltage from which they are generated. An example of such a circuit is found in the product designated ICL 7660, a power supply circuit manufactured by the assignee of the present invention.

The efforts to design and implement a bipolar charge pump integrated circuit have met with several obstacles which result from the inherent nature of the integration process and the fabrication process which are used to manufacture these devices. It is well known to those in the art that when MOS or CMOS circuits are integrated onto a single semiconductor substrate, the chip layout geometry and architecture inherently produce parasitic junction devices. These devices include junction diodes, bipolar transistors, and PNP four layer diode devices, similar to silicon controlled rectifier (SCR) devices.

The existence of these parasitic devices has created difficulties in the design and fabrication of dual polarity charge pump power supply circuits. When forward biased, the aforementioned four layer diode device will cause a CMOS circuit to experience a phenomenon known as latch-up. Latch-up is a phenomenon common to CMOS circuits whereby the circuit can be triggered into a low impedance conducting state by forward biasing an inherent four layer diode device in the circuit. This four layer diode may be triggered by various means into a low voltage, low impedance state. When this occurs, operation of the circuit is inhibited and possible damage may occur to the circuit if there is no inherent current limiting designed into the circuit.

Another problem inherent in the design of dual polarity charge pump inverter circuits is the difficulty of assuring correct start-up of the circuit. The conditions existing in the semiconductor material at the time of start-up may randomly produce states which prevent such a circuit from ever starting up to produce the desired output voltages. In the past, elaborate systems and considerable extra circuitry has been designed into such circuits in an attempt to avoid this problem.

## BRIEF DESCRIPTION OF THE INVENTION

The present invention consists of a CMOS inverting and non-inverting charge pump power supply integrated into a single piece of semiconductor substrate material. An inherent lateral bipolar transistor formed during the CMOS fabrication process is utilized to always assure the correct operating conditions which will allow start-up of the circuit. In addition, the inherent four layer diode devices which are created during the fabrication of the circuit are identified during the geometry layout process which defines the locations on the semiconductor substrate where the various devices will be placed, and extra minority charge collector regions

are placed in the semiconductor substrate to collect injected minority charge carriers and prevent the possibility of triggering the inherent four layer PNPN junction into a low impedance conducting or latch-up mode.

Another aspect of the present invention is the integration, on a single piece of semiconductor substrate material, of an inverting charge pump power supply, a non-inverting charge pump power supply, and a combination of RS-232C receivers and transmitters. Combination of RS-232C transmitters and receivers may consist of at least one transmitter together with either zero or any number of receivers.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a simplified schematic diagram of the charge pump circuit of a preferred embodiment of the present invention.

FIG. 1(b) is a schematic diagram of the charge pump circuit of FIG. 1(a) wherein the switches are replaced by MOS transistors.

FIG. 2 is a gate drive circuit suitable for operating driving the gates of the charge pump circuit of FIG. 1(b).

FIG. 3 is a schematic diagram of a preferred embodiment of the present invention further showing the substrate connections of the MOS devices and a PNP lateral junction device for assuring the correct start-up conditions of the charge pump circuit.

FIG. 4 is a semiconductor substrate profile drawing of NPN lateral transistor suitable for use in the present invention.

FIGS. 5(a) and 5(b) are respectively a schematic representation of a four layer device and a semiconductor substrate profile drawing of such a device showing the MOS geometry which inherently creates such as device.

FIG. 6(a) is a schematic diagram of a four layer device having extra P region collectors, suitable for use in the present invention.

FIG. 6(b) is a substrate profile drawing of a four layer device suitable for use in the present invention having extra minority charge carrier collectors for preventing latch-up showing the relative placement of such charge collectors.

FIG. 7 is a block diagram of an embodiment of the present invention including a dual integrated charge pump power supply and a RS-232C receiver and transmitter.

#### DESCRIPTION OF A PREFERRED EMBODIMENT

Referring first to FIG. 1(a), simplified conceptual schematic drawing of the basic charge pump circuit of the present invention, the circuit of the present invention operates by placing an input voltage upon one of two transfer capacitors via a series of switches. The charge in that capacitor is then transferred to one of two reservoir capacitors. The polarity of the voltage is established via the switch interconnecting scheme.

More specifically, the operation of the circuit of FIG. 1(a) is time-divided into two segments, or phases. In a first phase, voltage from a voltage source is placed on transfer capacitors. During a second phase the voltage on the transfer capacitors is transferred to the reservoir capacitors.

Referring first to the positive voltage doubler portion of the circuit, transfer capacitor 10 is charged from voltage source 12 (having a value  $V_{cc}$ ) by closing

switches 14 and 16 while switches 18 and 20 remain open during a first phase. During a second phase switches 14 and 16 are open and switches 18 and 20 are closed.

As can be seen from FIG. 1(a), when switches 18 and 20 are closed during the second phase the voltage source 12 is effectively placed in series with the voltage stored across reservoir capacitor 10 and thus the sum of the voltage across voltage source 12 and capacitor 10 is placed across reservoir capacitor 22.

The inverting portion of the voltage doubler circuit operates as follows: transfer capacitor 24 is charged to the voltage across reservoir capacitor 22 via the switches 26 and 28 which are closed during the first phase of operation of the circuit while switches 30 and 32 remain open. During the second phase of circuit operation switches 26 and 28 are opened and the voltage across transfer capacitor 24 is placed on reservoir capacitor 34 via the closing of switches 30 and 32. Those of ordinary skill in the art will note that the circuit configuration is such that when the voltage across transfer capacitor 24 is placed across reservoir capacitor 34 the positive end of transfer capacitor 24 is connected to ground line 36 through switch 32 and the negative end of capacitor 24 is connected to the side of reservoir capacitor 34 connected to  $-2V_{cc}$  output line 38. The polarity of the voltage across reservoir capacitor 34 with respect to ground line 36 is thus such that the voltage across reservoir capacitor 34 is negative. The output of reservoir capacitor 22 is connected to  $+2V_{cc}$  output line 40.

The first and second phases of circuit operation described above are repeated at a frequency which may range from approximately 100 hertz to 100's of kilohertz or higher. It has been found that a frequency of approximately 15 KHz performs satisfactorily for the purposes of the present invention.

The foregoing represents an idealized characterization of the operation of the circuit of FIG. 1(a). Those of ordinary skill in the art will readily realize that it will take several first and second phase cycles before the resultant voltage between ground terminal 36 and  $+2V_{cc}$  output terminal 40 actually reaches a voltage value of  $+2V_{cc}$ . Likewise, it will be appreciated that several cycles are also needed for the voltage between ground terminal 36 and  $-2V_{cc}$  output terminal 38 arrives at a voltage of  $-2V_{cc}$ .

Those of ordinary skill in the art will also realize that the amount of current which may be drawn from the output of the circuit of FIG. 1(a) depends on the relative sizes of transfer capacitors 10 and 24 and reservoir capacitors 22 and 34, as well as the on impedance of switches 14, 16, 18, 20, 26, 28, 32 and 30.

It will also be apparent that the voltage appearing between output terminals 36 and 38 or 36 and 40 will be approximately twice the input voltage supplied by voltage source 12. Those of ordinary skill in the art will appreciate that other multiples of the input voltage  $V_{cc}$  at voltage source 12, are readily achievable using the concept of the present invention.

Turning now to FIG. 1(b), it is seen that in an actual embodiment of the present invention switches 14, 16, 18, 20, 26, 28, 30 and 32 have been replaced with MOS transistors. Thus, switch 14 is replaced by P-channel MOS transistor 14(a), switch 16 is replaced by N-channel MOS transistor 16(a), switch 18 is replaced by P-channel MOS transistor 18(a), switch 20 is replaced by P-channel MOS transistor 20(a), switch 26 is replaced

by P-channel MOS transistor 26(a), switch 28 is replaced by N-channel MOS transistor 28(a), switch 30 is replaced by N-channel MOS transistor 30(a), switch 32 is replaced by N-channel MOS transistor 32(a).

The time controlled operation of the circuit of FIG. 1(b) is implemented by phase control unit 42. Phase control unit 42 drives all of the gates of the MOS devices, 14(a), 16(a), 18(a), 20(a), 26(a), 28(a), 30(a), and 32(a) via gate control lines 44 and 46. Gate control lines 44 and 46 are connected to the gates of the P-channel MOS transistors and N-channel MOS transistors, used as MOS switches, such that the switches are turned on and off appropriately as described herein during the first and second phases of the circuit operation.

Those of ordinary skill in the art will readily appreciate that, in order to insure efficient power transfer, that switching of MOS switching devices should be accomplished on a break before make basis or, at worst case, on a simultaneous switching basis. Those of ordinary skill in the art will also realize that the order of phases could be reversed. Alternatively, a first clock could be used to control the sets of MOS switches controlling transfer capacitor 10 and reservoir capacitor 22, and a second clock could be used to control the sets of MOS switches controlling transfer capacitor 24 and reservoir capacitor 34.

It should be understood for purposes of this disclosure, that all of the capacitors shown in FIGS. 1(a) and 1(b) would be located outboard of the integrated circuit in an actual embodiment. That is, these capacitors are external components which connect to the integrated MOS switches on the semiconductor substrate via terminals provided on the semiconductor substrate for that purpose. For an operating frequency of 15 KHz, 20 microfarads is a sufficient size for all capacitors. Those of ordinary skill in the art will readily appreciate that as the switching frequency is increased the values of the capacitors will drop, but that switching losses will increase due to the changing to discharging at the clock rate of its parasitic nodal capacitances in the MOS devices. Conversely, as the switching frequency decreases, the size of the capacitors would increase, with the concomitant disadvantage that the increasing capacitor size is accompanied by increasing physical size of the capacitors.

For a current capacity of 10 milliampere at +10 volts and -10 volts, the MOS switching devices should have a channel width to channel length ratio of 5000 to 10,000, with channel lengths of approximately five microns. Those of ordinary skill in the art will recognize that the range of current output of the circuit described herein could be as large as approximately one ampere, however, the MOS devices would have to be scaled accordingly as is well known in the art.

Referring now to FIG. 2, an embodiment of the phase control unit 42 of the present invention, the operation of phase control unit 42 is disclosed. Those of ordinary skill in the art will recognize that phase control unit 42 may consist of three conventional CMOS inverter circuits each comprised of a P-channel and N-channel MOS transistor pair. The embodiment of FIG. 2 contains a first CMOS inverter comprised of P-channel MOS transistor 44 and N-channel MOS transistor 46, the inverter comprised of P-channel MOS transistor 48 and N-channel MOS transistor 50, and the inverter comprised of P-channel MOS transistor 52 and N-channel MOS transistor 54.

These three inverter pairs are driven by oscillator 56, which may be any conventional oscillator configured from CMOS elements as is well known to those skilled in the art.

The circuit of FIG. 2 is powered by +2Vcc and -2Vcc lines 36 and 40. This assures that the voltage swing on gate lines 44 and 46 will span approximately the entire power supply range, thus ensuring that all of the gates of the P-channel and N-channel devices which they drive will be as fully turned on as possible and can be turned off since all transistors and enhancement types. This will guarantee as low an on-state impedance of the MOS switches as possible thus maximizing the efficiency and current drive capabilities of the present invention.

In the illustration of a preferred embodiment of the present invention depicted in FIG. 1(a), the substrate connections of the MOS devices are shown uncommitted. Those of ordinary skill in the art will realize that junction isolated MOS transistors such as used in FIG. 1(b) are four-terminal devices and that both the gate terminal and the substrate terminal are control terminals. The turn-on voltage of the gate terminal is affected by the reverse bias on the substrate to source junction. As that reverse bias is increased, the turn on voltage of the device also increases. The affect is significantly greater for an N-channel transistor than a P-channel transistor.

As the substrate-to-source voltage increases the gate turn voltage of the device also increases, thus potentially increasing the on resistance of the device to a point where circuit operation could be seriously effected. Since, in a circuit of this nature, the drain-source resistance in the on state should be as low as possible, it is desirable to connect each N-channel MOS transistor substrate to its source.

With respect to P-channel transistors the effect of this reverse substrate source biasing is about half of that for N-channel MOS transistors due to lighter channel impurity doping densities. The most practical solution in the case of the P-channel MOS transistors is to connect all P-channel substrates to the most positive voltage in the circuit. That voltage is, as seen from FIG. 1(a) +2Vcc which appears on positive supply line 40. These connections are shown in respect to FIG. 3.

Prior to start-up, it is reasonable to assume that zero voltage exists on all capacitors. At start-up, reservoir capacitor 22 may be connected to ground line 36 or to -2Vcc line 38. Reservoir capacitor 22 will be immediately charged with the source substrate diodes of P-channel MOS transistors 14(a) and 18(a) to a voltage of approximately Vcc -0.6 of a volt. The voltage on reservoir capacitor 34 could lie somewhat between ground line 36 and the voltage on reservoir capacitor 22; depending which of transistors 26(a), 28(a), 30(a) or 32(a) were conducting (if any). This results in a voltage on the -2Vcc line that could be such that N-channel transistor 16(a) and other transistors being turned on. Under these conditions, a voltage between +2Vcc and -2Vcc drives the gates of all of the output transistors and is indeterminate. Thus both start-up and operation is not assured.

If the other possible start-up conditions of the capacitor and MOS device connections and off/on states are assumed, those of ordinary skill in the art will readily appreciate that the start-up and operation of the circuit of FIGS. 1 and 2 is not assured.

The solution to this dilemma is to place a clamp on the  $-2V_{cc}$  line 38 to clamp that voltage line to assure that it will never assume a voltage substantially more positive than that appearing on ground line 36. The  $+2V_{cc}$  line 40 is also clamped so that it will never assume a voltage substantially more negative than the voltage  $V_{cc}$  on approximately  $V_{cc} - 0.6$  volts.

While those of ordinary skill in the art will realize that, conceptually, a diode would be an ideal clamping means for the  $-2V_{cc}$  line 38, it is not possible to fabricate a simple PN junction diode in a MOS process. A junction transistor will always be created by an attempt to fabricate a diode. The presence of such a transistor in the circuit of FIG. 1(b) would cause excess wasted current to flow in the circuit, because of its beta or current gain.

In a preferred embodiment of the present invention, this clamp is comprised of a lateral NPN transistor. This lateral NPN transistor is shown in FIG. 3. The lateral collector and base of this device are both connected to  $-2V_{cc}$  line 38, its vertical collector connected to  $+2V_{cc}$ . The lateral collector serves to minimize the effective current gain of the unwanted but inherent vertical collector of NPN transistor 58, which would otherwise cause excess current flow from the  $+2V_{cc}$  line through ground. Unless the  $-2V_{cc}$  line 38 exceeds ground by approximately 0.6 of a volt in the positive direction, this device will not conduct current. If the  $-2V_{cc}$  line equal approximately 0.6 volts, the device turns on and current will flow in approximately equal portions through both collectors to maintain the  $-2V_{cc}$  line at no greater than zero plus approximately 0.6 volts.

With respect to the clamp for  $+2V_{cc}$  line 40, the action of the inherent junction diodes 59(a) and 59(b) present between the drain and substrate of devices 14(a) and 18(a) serve to clamp the  $+2V_{cc}$  line to a voltage no more negative than the input positive supply voltage  $V_{cc}$  minus approximately 0.6 volts.

Consequently the voltages on  $+2V_{cc}$  line and  $-2V_{cc}$  line are both well defined. Additionally the voltage difference between  $+2V_{cc}$  line 38 and  $-2V_{cc}$  line 40 at start-up is ( $V_{cc} - 1.2$ ) volts and is also well defined. This value of voltage is sufficiently large to guarantee operation of the drive circuitry for the gates of the output transistors until the charge pumps charge the lines  $+2V_{cc}$  (40) and  $-2V_{cc}$  (38) to those voltages.

The lateral NPN transistor used to clamp  $-2V_{cc}$  line 38 is fabricated using conventional CMOS fabrication techniques. For a current drain of plus and minus 10 mA at 10 volts, the periphery of the emitter for the lateral NPN transistor can typically be 100 microns. Those of ordinary skill in the art will appreciate that the size of this device may be scaled to accommodate larger current carrying requirements, and its periphery need not be larger than 1000 microns.

Referring now to FIG. 4, a substrate profile drawing of a dual collector lateral NPN transistor 58, that transistor 58 is fabricated on a portion of the lightly doped N type substrate material 60 in a P-well 62. P-well 62 is placed into substrate 60 using common CMOS processing techniques. N region 64 serves as the emitter of the lateral NPN transistor, and is surrounded by N region 66 which serves as the lateral collector. P region 68 in P-well 62 serves as the base contact, it being understood by those skilled in the art that P-well 62 itself serves as the base of lateral NPN transistor 58. N-region 70 located in a region of substrate 60 outside of P-well 62

serves as the unwanted, but inherent vertical collector of NPN lateral transistor 58.

When the base emitter junction of lateral NPN transistor 58 is forward biased, minority carriers injected by the emitter into the base are collected by both the vertical and lateral collectors in roughly equal amounts. Connecting the lateral collectors to the common base reduces the vertical collector current to approximately  $\frac{1}{2}$  of the clamp current. If a vertical NPN transistor had been used alone, the clamp current (base current) would be multiplied by the beta (approximately 500 of the device) thereby wasting large amounts of current.

Referring now to FIGS. 1(b) and 3, during start-up reservoir capacitor 22 is charged by the forward biased condition of the source-substrate diodes 59(a) and 59(b) of P-channel device 14(a) and the drain substrate diode of P-channel device 18(a). The initial current surge through these diodes can be hundreds of milliamperes and thus be well above the holding current of the inherent SCR type four layer diode device which exists in the circuit.

Such a four layer device is schematically represented in FIG. 5(a). Referring to FIG. 5(a), it is seen that the four layer device is made up of PNP transistor 72, NPN transistor 74, resistor 76, and resistor 78. Resistor 76 is connected across the base-emitter junction of PNP transistor 72 while resistor 78 is connected across the base-emitter junction of PNP transistor 74. The base of NPN transistor 74 is connected to the collector of PNP transistor 72 and the base of PNP transistor 72 is connected to the collector of NPN transistor 74. The connection of the emitter junction of PNP transistor 72 and resistor 76 form the anode connection 78 of the four layer device and the intersection of resistor 78 and the emitter of NPN transistor 74 form the cathode connection 80 of the four layer device.

As will be appreciated by those of ordinary skill in the art, the four layer device shown in FIG. 5(a) will enter a low impedance state between its anode 80 and cathode 82 after suitable triggering if the product of the betas of the two equivalent transistors is greater than one and the anode current into the four layer device is greater than the turn on voltage of either transistor divided by its equivalent base emitter shunting resistor, whichever is greatest.

Referring now to FIGS. 3, 5(a) and 5(b), it will be apparent to those of ordinary skill in the art that such a four layer device occurs in the circuit of FIG. 3. The sources of either of P-channel devices 14(a) and 18(a) (shown diagrammatically as P region 84 in FIG. 5(b)) represent the emitter of PNP transistor 72 of FIG. 5. The semiconductor substrate 60 forms the base of PNP transistor 72 as well as the collector of NPN transistor 74. P-well 86 forms the collector of PNP transistor 72 as well as the base of NPN transistor 74. The source of either of N-channel transistors 16(a) and 32(a), one of which is shown as N region 88 of FIG. 5(b), forms the emitter of NPN transistor 74. Resistor 76 is formed by the bulk resistance of the P-well 86. Likewise, the resistor 78 is formed by the bulk resistance of the substrate material. Those skilled in the art will note that regions such as P region 90 in P-well 86 and N region 92 in substrate 60 serve as low resistance surface planes commonly used in CMOS technology to buss supply voltages to the surfaces of substrate and P-wells.

In order to trigger the four layer device into its low impedance state, currents must be injected into the base of either of transistors 72 or 74, either the P-well 86 or

the substrate 60. These currents must be greater than the holding current required for the four layer device. This condition can occur by various means. For example, a very rapid rate of increase in the anode-cathode voltage will force current into the bases of transistors 72 and 74 due to the charging of the collector-base junction capacitors inherent in those devices. Alternatively, forward biasing of a region in the substrate junction adjacent to the P-well 86 and P-region 84 forming the emitter of transistor 72 could induce base currents to flow in transistor 72 and 74 sufficient to exceed holding current values. Either of these conditions could occur at start-up of the circuit of FIG. 3.

In order for the inverting doubler charge pump circuit of the present invention to reliably operate, it is necessary to assure that this possible latch-up condition can never occur. One method which is used in some CMOS circuits to inhibit the possibility of latch-up would be to insert high value resistors in series with either or both of the emitters of NPN transistor 74 or PNP transistor 72. This method, however, in the present invention would result in an unacceptably high value of on impedance for the MOS switches.

Another method of assuring that the latch-up condition never occurs is disclosed as an aspect of the present invention. The product of the betas of PNP transistor 72 and NPN transistor 74 is made less than unity. Thus, the current flowing between the anode terminal 80 and cathode terminal 82 of the four layer device will never reach a value great enough to equal the holding current necessary to sustain that device in its low impedance state.

Referring now to FIG. 6(a), another four layer device 100 composed of equivalent NPN and PNP transistors is shown. However, unlike the circuit of FIG. 5(a) the four layer device depicted in FIG. 6(a), having anode terminal 102 and cathode terminal 104, a single collector NPN transistor 106 and a multiple collector PNP transistor 108 as well as resistors 110 and 112. The multiple PNP collectors (shown at 114) are tied back to the base of the PNP transistor 108. Only a single multiple collector is connected to the base of NPN transistor 106. These collectors 114 are fabricated on substrate 60 in a region located between the emitter of NPN transistor 106 and the base of PNP transistor 108.

The function of the serial collectors 114 is to guard the forward biased PN junction formed between P regions 128 or 138 and substrate 60 by collecting the minority carriers which are injected into the substrate 60. These carriers are thus prevented from reaching the base of the PNP transistor 108 and assure that the beta product of these two transistors is less than unity. Most of the minority carriers injected into the substrate are collected by these serial collectors before they can diffuse and be collected by the P-well which is also the base of the NPN transistor. This may be designed to reduce the PNP beta to a value of less than the reciprocal of the NPN beta thereby preventing latch-up.

Referring now to FIG. 6(b), a semiconductor profile drawing of four layer device 100 of FIG. 6(a), NPN transistor 106 is formed in P-well 120. Contact 122, contacting N region 124 in P-well 120, constitutes cathode 104 of four layer device 100. This N region may be the source of either N-channel MOS transistor 16(a) or N-channel MOS transistor 32(a) from FIGS. 1 and 3. N region 124 forms the emitter of NPN transistor 106 and P-well 120 forms the base of NPN transistor 106. Sub-

strate 60 forms the collector of NPN transistor 106, as well as the base of PNP transistor 112.

Contact 126, contacting P region 128 is at  $V_{cc}$  potential. P region 128 may be either the source of P channel MOS transistor 14(a) or the drain of P-channel MOS transistor 18(a) from FIGS. 1 and 3. P region 128 forms the emitter of PNP transistor 108.

P regions 130(a) through 130(e), in substrate 60, form the multiple collectors of PNP transistor 108 (shown at 114 in FIG. 6(a)). Multiple collectors 130(a) through 130(e) are connected together at the surface of the semiconductor substrate 60 by layer 132 which may be made of aluminum and fabricated during the metalization step of a conventional CMOS fabrication process. N regions 134(a) through 134(d), disposed in between P regions 130(a) through 130(e) are used for the purpose of making a low impedance contact between the  $+2V_{cc}$  line and the substrate. P-well 120, the base of NPN transistor 106, also serves as the single collector of PNP transistor 108, as shown in FIG. 6(a). The regions 135, shown adjacent to layer 132, are the gate oxide layer of the MOS structures.

As is shown in FIG. 6(b) the multiple collectors of PNP transistor 114 are interposed in between the N-channel MOS transistor 16(a) in the P-well formed of N regions 124 and 136. This device, for illustration, shown as 16(a) on FIG. 6(b), has drain region 138 and gate 140. This device, for illustration, shown as 18(a) on FIG. 6(b), has drain region 138 and gate region 142. P-channel MOS transistor 14(a) formed of P region 128 and P region 138. In this manner these multiple collectors 130(a) through 130(e) are in a position to collect most of the minority carriers which are injected into the semiconductor substrate as a result of forward biasing at start-up of the parasitic PN junctions formed during the CMOS fabrication process.

Depending on the CMOS process used, the number of multiple collectors 114 may range from 1 to approximately 10. Furthermore, the spacing between the injecting PN junction and the nearest P-well should be typically anywhere from 25 to 500 microns. Spacing may be reduced if the lifetime of the substrate minority carriers is particularly low and or the substrate resistivity is very low (less than one ohm-centimeter). In the presently preferred embodiment the spacing between the injecting PN junctions and the nearest P-well is approximately 150 microns and four multiple collectors 114 are used. This is based upon a process using a substrate having a substrate resistivity of approximately 2.5 ohm-cm.

Although the presently preferred embodiment has been disclosed as a P-well CMOS embodiment, those of ordinary skill in the art will recognize that N-well CMOS technology could also be used without departing from the spirit and scope of the present invention. Those of ordinary skill in the art will readily understand from the disclosure herein how to fabricate such an N-well embodiment.

Referring now to FIG. 7, a block diagram of a preferred embodiment of the present invention including dual charge pump power supply 200, previously described, RS-232C transmitter circuit 202, and RS-232 receiver circuit 204. These elements are shown diagrammatically as fabricated on a single piece of semiconductor substrate material 206. Positive reservoir capacitor 22 is shown connected to the semiconductor substrate via terminal pads 208 and 210. Negative reservoir capacitor 34 is shown connected to the substrate via termi-



nal pads 208 and 212. Positive transfer capacitor 10 and negative transfer capacitor 24 are shown connected to the substrate via terminal pads 214, 216, 218 and 220 respectively. An input voltage is provided to the circuit at Vcc input terminal pad 222 and ground input terminal pad 224. Those of ordinary skill in the art will readily realize that ground input terminal 224 and terminal pad 208 may in some embodiments be the same connection terminal pad. The data input to RS-232 transmitter 202 is provided at terminal pad 226 and the output of RS-232 transmitter 202 is provided at terminal pad 228. The data input to RS-232 receiver 204 is provided at terminal pad 230 and the data output of RS-232 receiver 204 so provided at terminal pad 232.

A monolithic integrated circuit containing the dual charge pump power supply 20 and RS-232 transmitter 202 and receiver 204 may be fabricated as a monolithic integrated circuit. The only outboard components required for operation of the circuit are positive and negative reservoir capacitors 22 and 34 and the positive and negative transfer capacitors 10 and 24.

While the preferred embodiment of FIG. 7 shows a single RS-232 transmitter 202 and a single RS-232 transmitter 204, those of ordinary skill in the art will readily recognize that other combinations of receivers and transmitters could be added without departing from the spirit of the invention. It is noted, however, that an embodiment of the circuit of FIG. 7 which contains only one or more RS-232 receivers 204, and no RS-232 transmitters 202, does not require a negative power supply connection. This is because the negative swing of the RS-232 format signal is usually disregarded by the receiver circuitry.

The RS-232 transmitter circuit 202, as well as the RS-232 receiver circuit 204 may be conventionally configured out of CMOS elements as is well known in the art. For example, RS-232 transmitter circuit 202 may be a CMOS inverter with a level shifter to translate TTL logic levels to the RS-232 format, as is known in the art. Alternatively, it may be configured similarly to the MC 1488 circuit, manufactured by Motorola. RS-232 receiver circuits 204 may be a CMOS inverter with a level shifter to translate the incoming RS-232 format signal to TTL logic levels as is known in the art. Alternatively, it may be configured similarly to the MC 1489 circuit, manufactured by Motorola.

A preferred embodiment of the present invention has been disclosed. Those of ordinary skill in the art will readily recognize that other embodiments are possible which do not differ in material respects. It is the intention of the inventors to include such embodiment within the scope of the appended claims.

We claim:

1. A circuit, integratable on a single piece of semiconductor substrate material, for providing a bipolar voltage output at substantially double the voltage of a unipolar voltage input source, including:

first and second voltage input terminals,  
first and second positive transfer capacitor connection terminals,

first MOS semiconductor switch means for selectively connecting said first voltage input terminal to said first positive transfer capacitor connection terminal and said second voltage input terminal to said second positive transfer capacitor connection terminal,

first and second positive reservoir capacitor connection terminals, said first positive reservoir capacitor connection terminal connected to a fixed voltage, second MOS semiconductor switch means for selectively connecting said first voltage input terminal to said second positive transfer capacitor connection terminal and said first positive transfer capacitor connection terminal to said second positive reservoir capacitor connection terminal,

first and second negative transfer capacitor connection terminals,

third MOS semiconductor switch means for selectively connecting said second voltage input terminal to said first negative transfer capacitor connection terminal and said second positive reservoir capacitor connection terminal to said second negative transfer capacitor connection terminal,

first and second negative reservoir capacitor connection terminals, said first negative reservoir capacitor connection terminal connected to a fixed voltage,

fourth MOS semiconductor switch means for selectively connecting said first negative transfer capacitor connection terminal to said second negative reservoir capacitor connection terminal and said second negative transfer capacitor connection terminal to said second voltage input terminal, and selection means, coupled to said first, second, third and fourth semiconductor switch means, for selectively activating said first, second, third and fourth semiconductor switch means.

2. The circuit of claim 1 further including at least two RS-232 transmitter circuit, disposed in said semiconductor substrate material, having positive, negative and ground potential power conductors connected to said second positive reservoir capacitor terminal, said second negative reservoir capacitor connection terminal, and said second voltage input terminal, respectively, a data input connection terminal connected to said transmitter circuit for providing data to said transmitter circuit, and a data output terminal connection for providing an output from said transmitter circuit.

3. The circuit of claim 1 further including at least one RS-232 receiver circuit disposed on said semiconductor substrate material, including positive and ground power connection terminals connected to said first and second voltage input terminals and having a data input connection terminal and a data output connection terminal.

4. The circuit of claim 1 further including means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

5. The circuit of claim 4 wherein said means is an inherent NPN transistor having multiple collectors.

6. The circuit of claim 4 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

7. The circuit of claim 6 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

8. A circuit, integratable on a single piece of semiconductor substrate material, for providing a bipolar voltage output at substantially double the voltage of a unipolar voltage input source, including:

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first and second voltage input terminals,  
first and second positive transfer capacitor connection terminals,

a first set of MOS semiconductor switches, including a switch connected between said first voltage input terminal and said first positive transfer capacitor connection terminal and a switch connected between said second voltage input terminal and said second positive transfer capacitor connection terminal,

first and second positive reservoir capacitor connection terminals, said first positive reservoir capacitor connection terminal connected to a fixed voltage,

a second set of MOS semiconductor switches, including a switch connected between said first voltage input terminal and said second positive transfer capacitor connection terminal, and a switch connected between said first positive transfer capacitor connection terminal and said second positive reservoir capacitor connection terminal,

first and second negative transfer capacitor connection terminals,

a third set of MOS semiconductor switches, including a switch connected between said second voltage input terminal and said first negative transfer capacitor connection terminal and a switch connected between said second positive reservoir capacitor connection terminal and said second negative transfer capacitor connection terminal,

first and second negative reservoir capacitor connection terminals, said first negative reservoir capacitor connection terminal connected to a fixed voltage,

a fourth set of MOS semiconductor switches, including a switch connected between said first negative transfer capacitor connection terminal and said second negative reservoir capacitor connection terminal and a switch connected between said second negative transfer capacitor connection terminal and said second voltage input terminal,

selection means, coupled to said first, second, third and fourth set of semiconductor switches, for selectively activating said first, second, third and fourth sets of semiconductor switches.

9. The circuit of claim 8 further including at least one RS-232 transmitter circuit, disposed in said semiconductor substrate material, having positive, negative and ground potential power conductors connected to said second positive reservoir capacitor terminal, said second negative reservoir capacitor connection terminal, and said second voltage input terminal, respectively, a data input connection terminal connected to said transmitter circuit for providing data to said transmitter circuit, and a data output terminal connection for providing an output from said transmitter circuit.

10. The circuit of claim 8 further including at least one RS-232 receiver circuit disposed on said semiconductor substrate material, including positive and ground power connection terminals connected to said first and second voltage input terminals and having a data input connection terminal and a data output connection terminal.

11. The circuit of claim 8 further including means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

12. The circuit of claim 11 further including means for clamping said second negative reservoir capacitor

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connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

13. The circuit of claim 12 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

14. The circuit of claim 2 further including means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

15. The circuit of claim 9 wherein said means is an inherent NPN transistor having multiple collectors.

16. The circuit of claim 2 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

17. The circuit of claim 2 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

18. The circuit of claim 3 further including means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

19. The circuit of claim 18 wherein said means is an inherent NPN transistor having multiple collectors.

20. The circuit of claim 3 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

21. The circuit of claim 3 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

22. The circuit of claim 1 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

23. The circuit of claim 1 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

24. The circuit of claim 9 further including means for inhibiting latch-up of forward biased four layer devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

25. The circuit of claim 24 wherein said means is an inherent NPN transistor having multiple collectors.

26. The circuit of claim 9 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

27. The circuit of claim 9 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

28. The circuit of claim 10 further including means for inhibiting latch-up of forward biased four layer

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devices created as a result of layout of said circuit on a single piece of semiconductor substrate material.

29. The circuit of claim 28 wherein said means is an inherent NPN transistor having multiple collectors.

30. The circuit of claim 10 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

31. The circuit of claim 10 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage

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approximately equal to the voltage appearing on said first voltage input terminal.

32. The circuit of claim 8 further including means for clamping said second negative reservoir capacitor connection terminal to a voltage no more positive than a voltage approximately equal to the voltage appearing on said second voltage input terminal.

33. The circuit of claim 8 further including means for clamping said second positive reservoir capacitor terminal to a voltage no more negative than a voltage approximately equal to the voltage appearing on said first voltage input terminal.

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UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 4,777,577

DATED : October 11, 1988

INVENTOR(S) : Bingham, et. al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title page, item

[63] Related U. S. Application Data

Delete "Continuation of Ser. No. 013,648, May 12, 1987, abandoned, which is a continuation of Ser. No. 782,953, Oct. 1, 1985, Pat. No. 4,636,930."

Insert --Continuation of Ser. No. 013,648, May 12, 1987, Pat. No. 4,809,152, which is a continuation of Ser. No. 878,233, Jun. 25, 1986, Pat. No. 4,679,134, which is a continuation of Ser. No. 782,953, Oct. 1, 1985, Pat. No. 4,636,930.--

Signed and Sealed this

Twenty-sixth Day of April, 1994

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

[54] INTEGRATED DUAL CHARGE PUMP  
POWER SUPPLY AND RS-232  
TRANSMITTER/RECEIVER

- [75] Inventors: David Bingham, San Jose; Charles M. Allen, Sunnyvale, both of Calif.  
[73] Assignee: Maxim Integrated Products, Sunnyvale, Calif.  
[21] Appl. No.: 271,160  
[22] Filed: Nov. 14, 1988

Related U.S. Application Data

- [63] Continuation of Ser. No. 13,648, May 12, 1987, Pat. No. 4,809,152.  
[51] Int. Cl.<sup>4</sup> ..... 02M 7/25  
[52] U.S. Cl. .... 363/61; 307/110  
[58] Field of Search ..... 363/59, 60, 61;  
307/110; 320/1; 357/51

[56] References Cited

U.S. PATENT DOCUMENTS

3,470,443	9/1969	Berry et al. ....	363/62
3,731,112	5/1973	Smith .....	307/109
3,878,450	4/1975	Greatbatch .....	363/60
3,942,047	3/1976	Buchanan .....	307/296.6
3,943,428	3/1976	Whidden .....	363/60
3,955,353	5/1976	Astle .....	368/157
3,975,671	8/1976	Stoll .....	363/60
4,047,091	9/1977	Hutchines et al. ....	363/60
4,061,929	12/1977	Asano .....	307/246
4,068,295	1/1978	Portmann .....	363/60
4,106,086	8/1978	Holbrook et al. ....	363/60
4,186,436	1/1980	Ishiwatari .....	363/60
4,321,661	3/1982	Sano .....	363/60
4,460,952	7/1984	Risinger .....	363/61
4,485,433	11/1984	Topich .....	363/60

FOREIGN PATENT DOCUMENTS

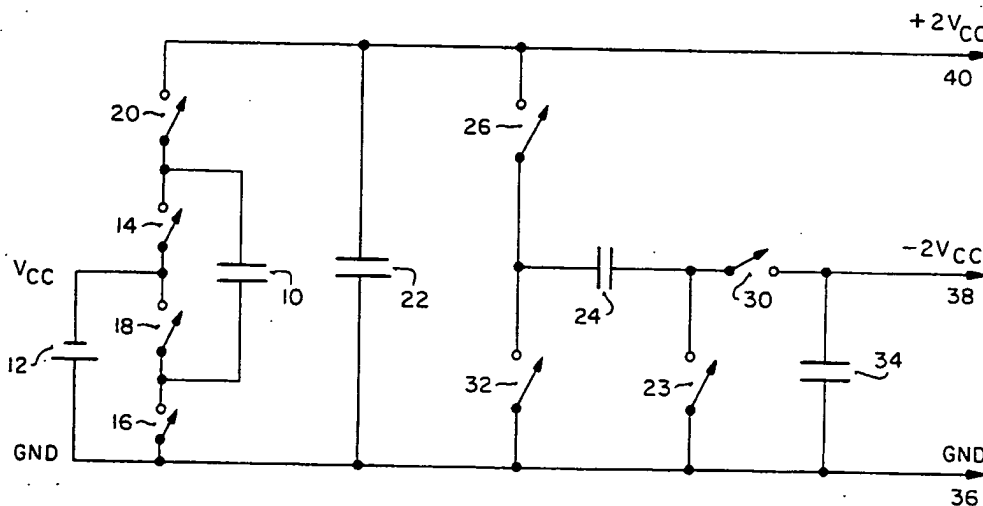
0080264	5/1982	Japan .....	363/60
0951602	8/1982	U.S.S.R. ....	363/60

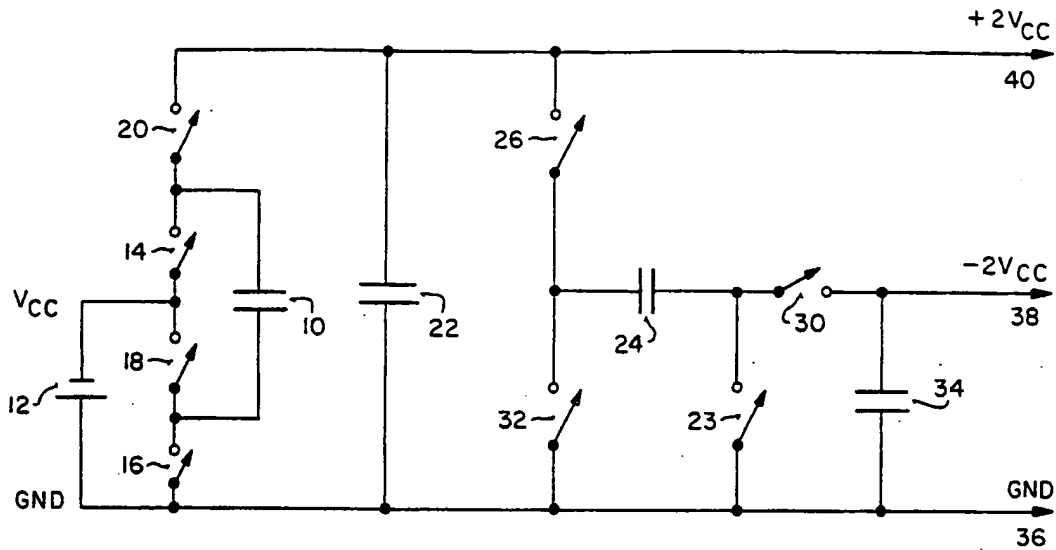
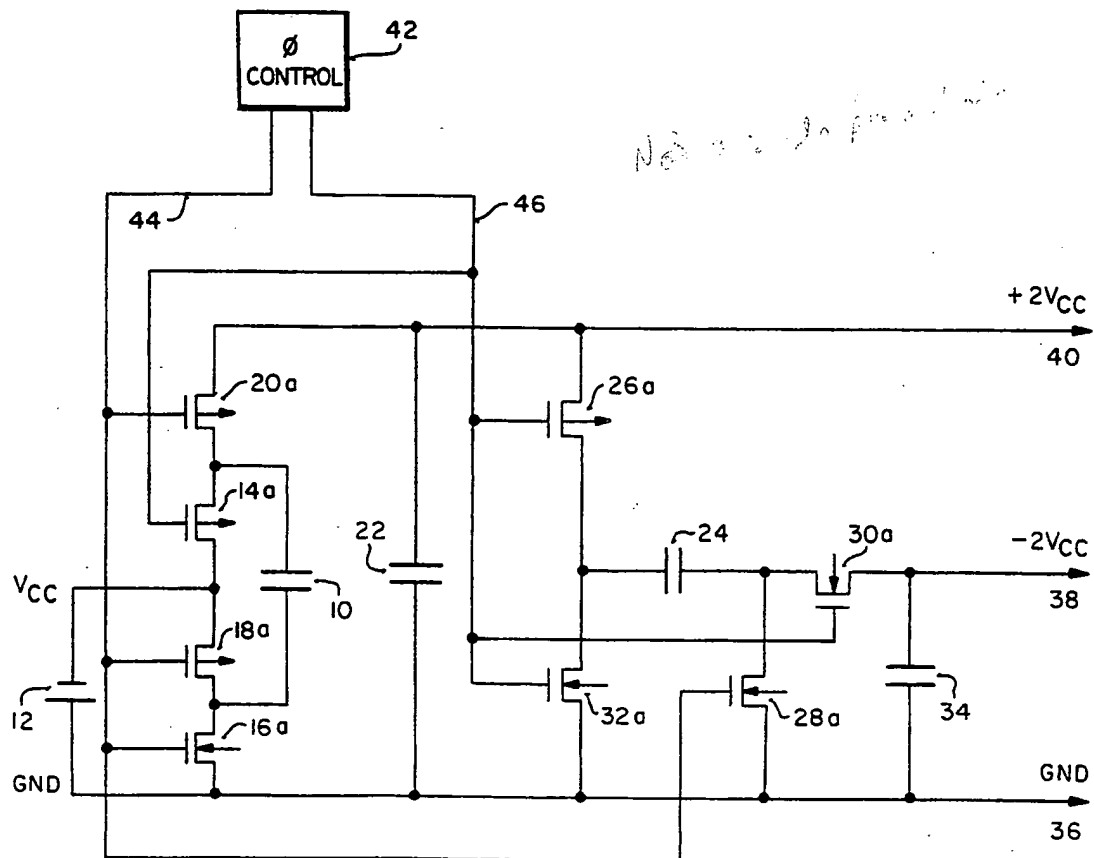
Primary Examiner—Patrick R. Salce  
Assistant Examiner—Judson H. Jones  
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

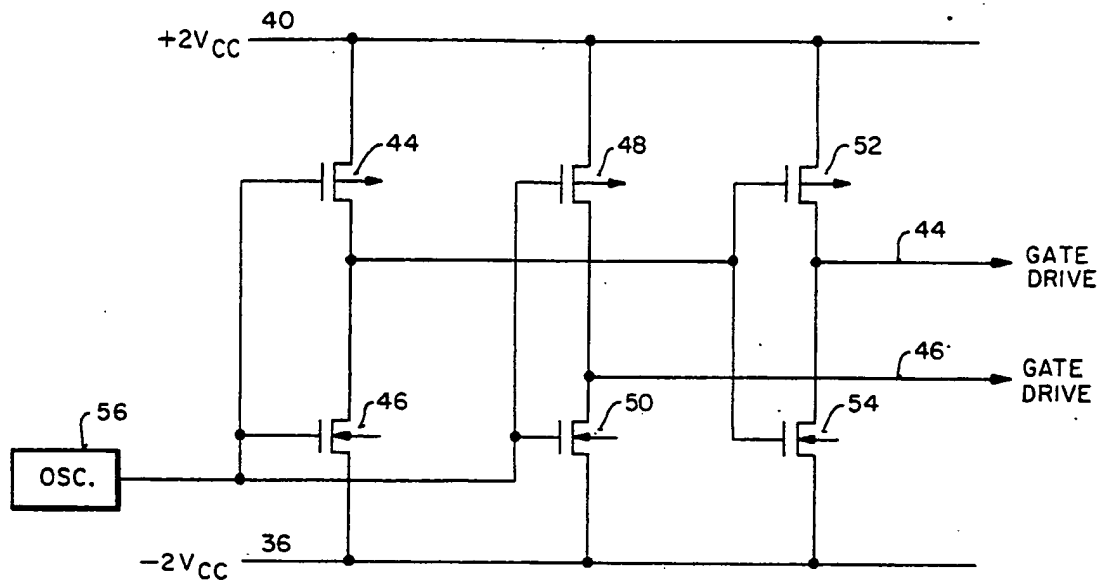
A monolithic integrated circuit containing an inverting/non-inverting voltage doubler charge pump circuit is disclosed for converting a unipolar supply voltage to a bipolar supply voltage of a greater magnitude. The unipolar input voltage is placed across a first external transfer capacitor by a first set of MOS switches during a first time period. The unipolar input voltage source is placed in series with the first transfer capacitor and this series combination of voltages is placed across a first external reservoir capacitor by a second set of MOS switches during a second time period. The voltage appearing across the first external reservoir capacitor is placed on a second transfer capacitor during the first time period by a third set of MOS switches. The voltage across the second transfer capacitor is placed into a second external reservoir capacitor with its polarity inverted by a fourth set of MOS switches during the second time period. A dual-collector lateral junction transistor, formed during the conventional CMOS processing steps used to fabricate the MOS switches, is connected as a voltage clamp between a ground potential and the two bipolar DC output lines of the power supply circuit to assure correct start-up conditions for the circuit. Gain reduction devices are placed in the semiconductor substrate to collect minority carriers which would otherwise be injected into inherent parasitic four layer PNP junction devices created as a result of the architecture of the circuit, to prevent latch-up of the four layer devices. In a preferred embodiment, an RS-232 receiver and transmitter are contained on the same monolithic integrated circuit as the dual charge pump power supply.

4 Claims, 5 Drawing Sheets

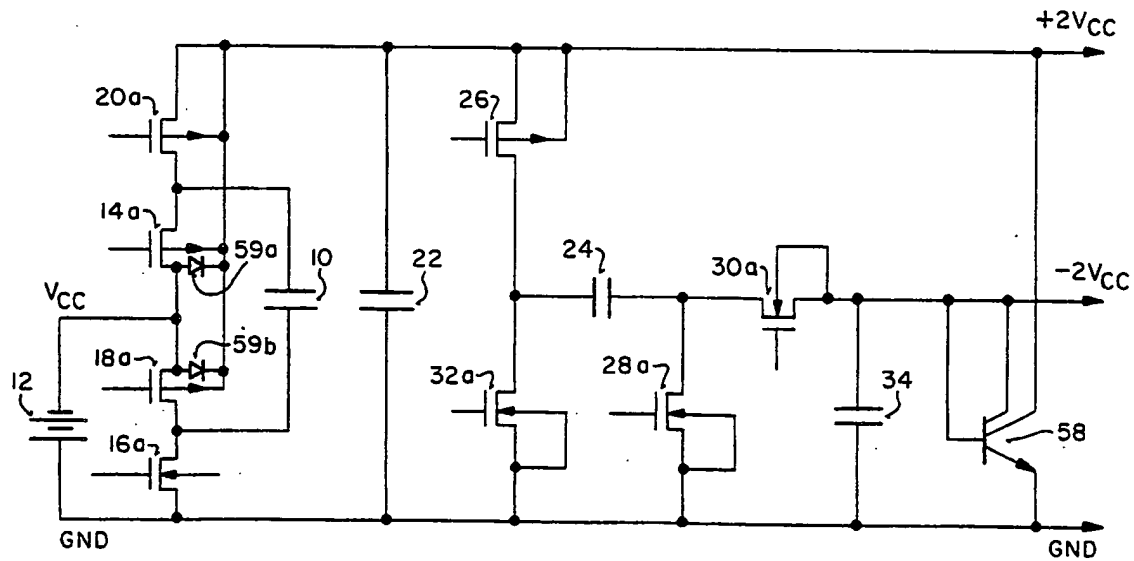


**FIG 1A****FIG 1B**

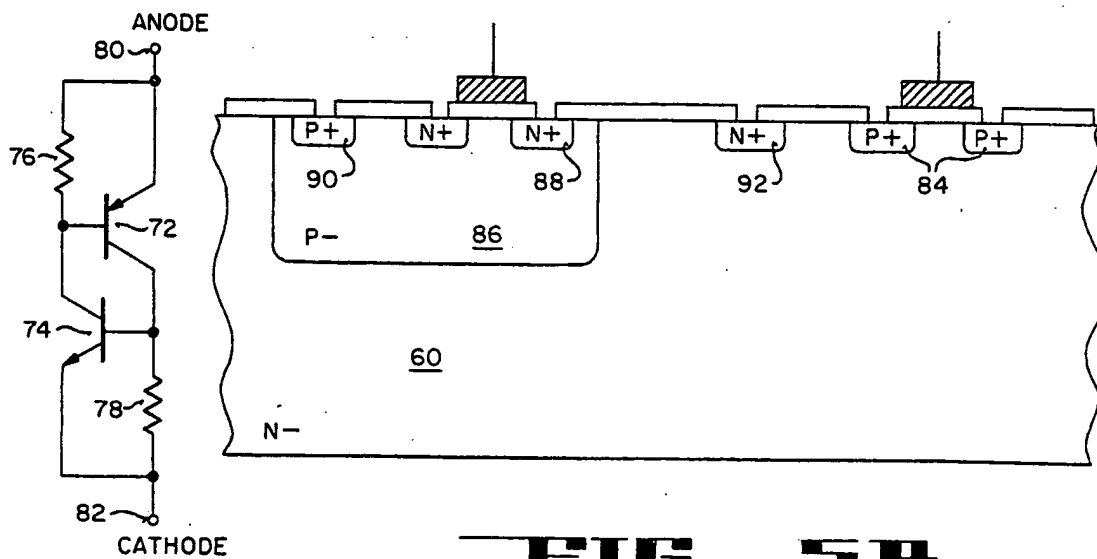
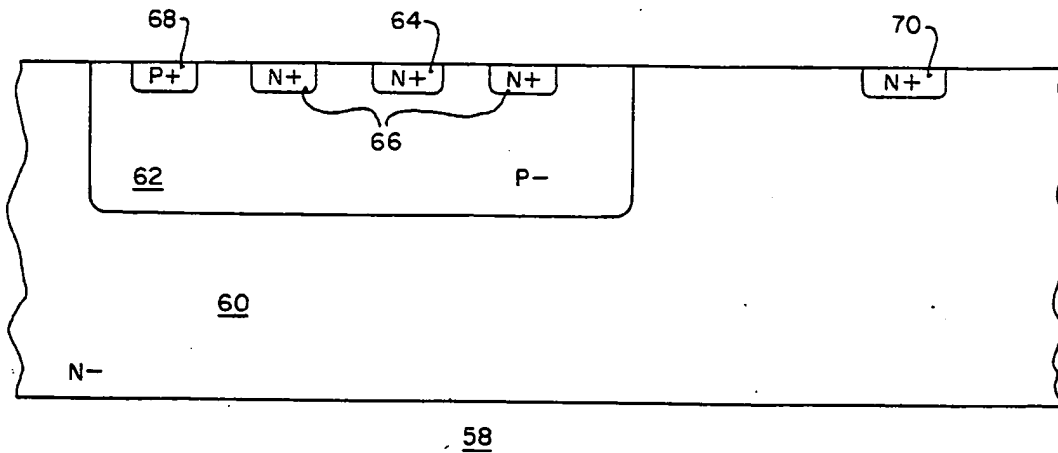
**FIG 2**



**FIG 3**



**FIG 4**

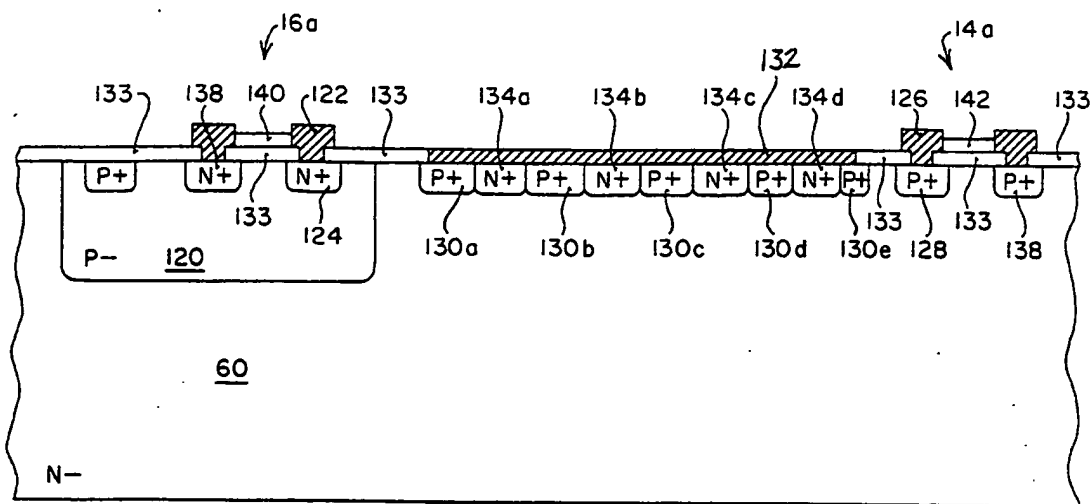


**FIG 5B**

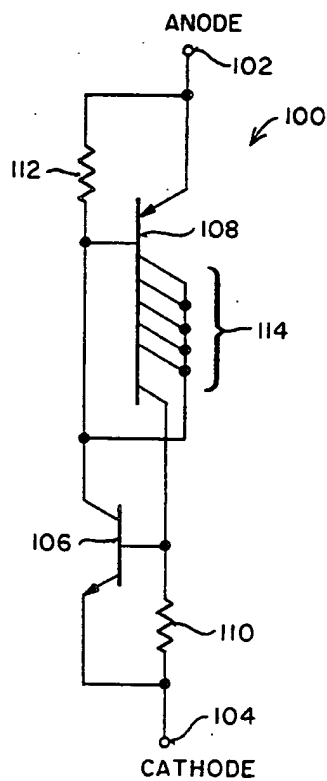
**FIG 5A**



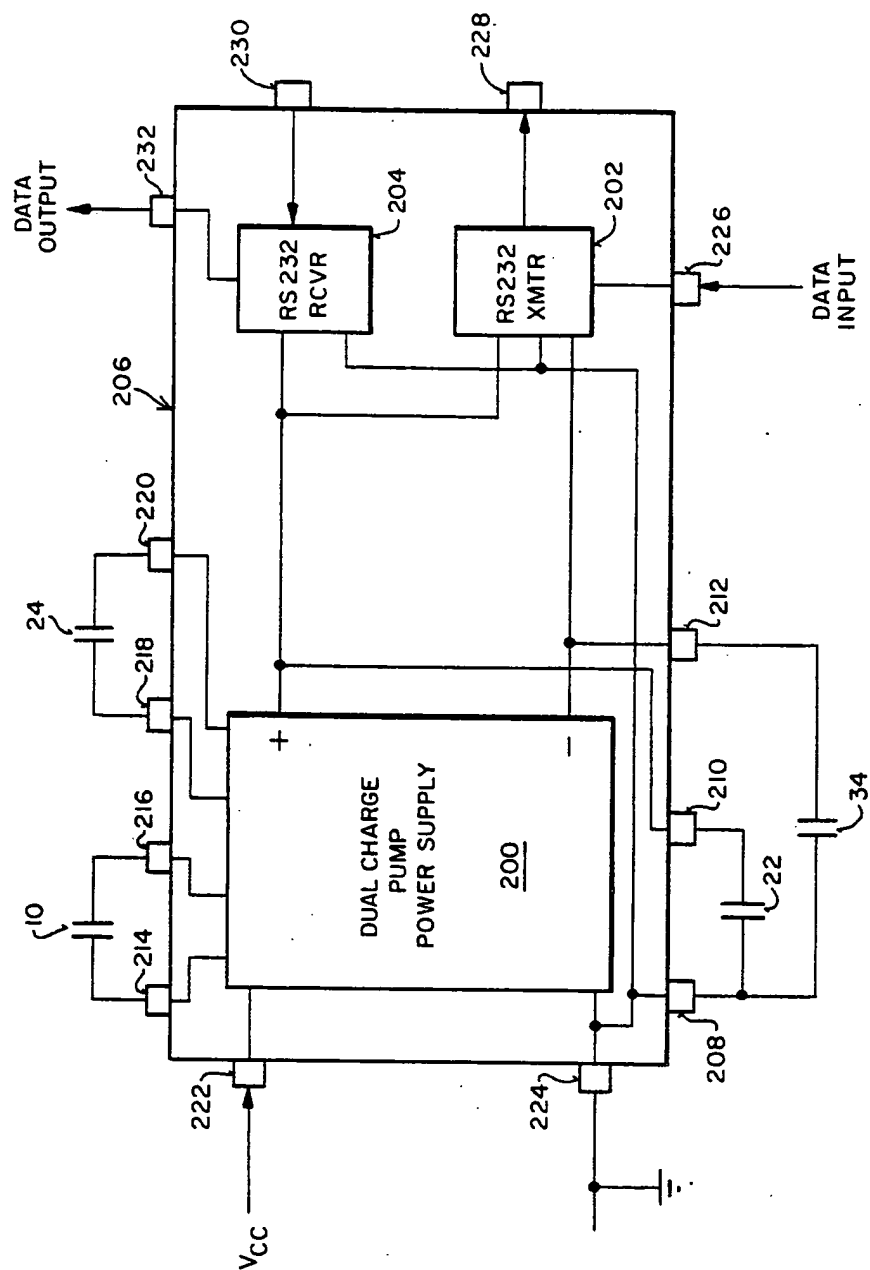
**FIG 6B**



**FIG 6A**



**FIG 7**



# INTEGRATED DUAL CHARGE PUMP POWER SUPPLY AND RS-232 TRANSMITTER/RECEIVER

This is a continuation of application Ser. No. 07/013,648, filed May 12, 1987, now U.S. Pat. No. 4,809,152.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention pertains to charge pump power supplies for generating bipolar output voltages greater in magnitude than a single unipolar input voltage. More particularly, the present invention pertains to the integration of such a circuit on a single piece of semiconductor substrate material. Further, the invention pertains to other circuitry integrable on a single piece of semiconductor substrate material along with such a power supply circuit.

### 2. Prior Art

Discrete component voltage doubler and voltage inverter circuits are well known in the art. Such circuits are used in many electronic systems which require a multiplicity of DC voltages for operation. More recently, in the context of digital circuits and systems, it has become common to employ a single five volt unipolar voltage supply to power digital circuitry in modern data processing systems. For example, semiconductor microprocessors, memories, and logic all commonly operate from a single five volt power supply. There are however, certain interface circuits and other special purpose circuits which require voltages other than five volts. More particularly, some circuits require voltages in the ranges of from five to fifteen volts. Additionally, requirements often exist for bipolar power supply voltages so that voltage power requirements of plus or minus 15 volts and plus or minus 12 volts are commonly encountered, for example in RS-232 communication loops.

For these communication circuits and other applications, bipolar DC power requirements are low when compared to the digital circuitry power requirements. In fact, it is common to encounter five volt unipolar power supplies for driving digital logic rated in tens or hundreds of watts whereas interface and other power requirements may be as low as tens or hundreds of milliwatts.

It is therefore often desirable to generate locally the various non-primary voltage sources, i.e., the bipolar voltage sources, if the power requirements are not high and if it can be done economically and with relatively high electrical power conversion efficiencies.

For an example, a minicomputer may have a 100 watt 5 volt power supply which supplies all of the requirements for a multiplicity of printed circuit boards holding logic integrated circuits. On one of those integrated circuit boards, there will often be an RS-232 digital interface circuit requiring a plus or minus 10 or plus or minus 15 volt power supply. This interface circuit may consume 50 milliwatts of power. Instead of generating the plus and minus 15 volt power supply from the main power supply and then bussing these voltages to the boards which require them, it is often more economical to generate these two voltages from the bussed five volt power supply locally on whatever board needs other voltages. However, generating such voltages by the use of discrete components is often disadvantageous because the additional components required to generate

such voltages take up a relatively large amount of circuit board real estate, and often are power inefficient, i.e., heat producing.

The industry has recently turned its attention to attempts to furnish auxiliary power supplies of the nature herein described on a single semiconductor substrate. Such circuits have the obvious advantages of space saving, assembly labor savings, and relatively lower power dissipation. A form of such circuits known as charge pumps have been used in semiconductor memory chips to produce a crude back bias supply and for supplying the higher voltages needed to program such memory devices. Charge pump circuits have been used in the inverting mode to produce voltage polarities opposite to that of the supply voltage from which they are generated. An example of such a circuit is found in the product designated ICL 7660, a power supply circuit manufactured by the assignee of the present invention.

The efforts to design and implement a bipolar charge pump integrated circuit have met with several obstacles which result from the inherent nature of the integration process and the fabrication process which are used to manufacture these devices. It is well known to those in the art that when MOS or CMOS circuits are integrated onto a single semiconductor substrate, the chip layout geometry and architecture inherently produce parasitic junction devices. These devices include junction biodes, bipolar transistors, and PNP four layer diode devices, similar to silicon controlled rectifier (SCR) devices.

The existence of these parasitic devices has created difficulties in the design and fabrication of dual polarity charge pump power supply circuits. When forward biased, the aforementioned four layer diode device will cause a CMOS circuit to experience a phenomenon known as latch-up. Latch-up is a phenomenon common to CMOS circuits whereby the circuit can be triggered into a low impedance conducting state by forward biasing an inherent four layer diode device in the circuit. This four layer diode may be triggered by various means into a low voltage, low impedance state. When this occurs, operation of the circuit is inhibited and possible damage may occur to the circuit if there is no inherent current limiting designed into the circuit.

Another problem inherent in the design of dual polarity charge pump inverter circuits is the difficulty of assuring correct start-up of the circuit. The conditions existing in the semiconductor material at the time of start-up may randomly produce states which prevent such a circuit from ever starting up to produce the desired output voltages. In the past, elaborate systems and considerable extra circuitry has been designed into such circuits in an attempt to avoid this problem.

## BRIEF DESCRIPTION OF THE INVENTION

The present invention consists of a CMOS inverting and non-inverting charge pump power supply integrated into a single piece of semiconductor substrate material. An inherent lateral bipolar transistor formed during the CMOS fabrication process is utilized to always assure the correct operating conditions which will allow start-up of the circuit. In addition, the inherent four layer diode devices which are created during the fabrication of the circuit are identified during the geometry layout process which defines the locations on the semiconductor substrate where the various devices will be placed, and extra minority charge collector regions are placed in the semiconductor substrate to collect

injected minority charge carriers and prevent the possibility of triggering the inherent four layer PNP junction into a low impedance conducting or latch-up mode.

Another aspect of the present invention is the integration, on a single piece of semiconductor substrate material, of an inverting charge pump power supply, a non-inverting charge pump power supply, and a combination of RS-232C receivers and transmitters. Combination of RS-232C transmitters and receivers may consist of at least one transmitter together with either zero or any number of receivers.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) is a simplified schematic diagram of the charge pump circuit of a preferred embodiment of the present invention.

FIG. 1(b) is a schematic diagram of the charge pump circuit of FIG. 1(a) wherein the switches are replaced by MOS transistors.

FIG. 2 is a gate drive circuit suitable for operating driving the gates of the charge pump circuit of FIG. 1(b).

FIG. 3 is a schematic diagram of a preferred embodiment of the present invention further showing the substrate connection of the MOS devices and a PNP lateral junction device for assuring the correct start-up conditions of the charge pump circuit.

FIG. 4 is a semiconductor substrate profile drawing of NPN lateral transistor suitable for use in the present invention.

FIGS. 5(a) and 5(b) are respectively a schematic representation of a four layer device and a semiconductor substrate profile drawing of such a device showing the MOS geometry which inherently creates such a device.

FIG. 6(a) is a schematic diagram of a four layer device having extra P region collectors, suitable for use in the present invention.

FIG. 6(b) is a substrate profile drawing of a four layer device suitable for use in the present invention having extra minority charge carrier collectors for preventing latch-up showing the relative placement of such charge collectors.

FIG. 7 is a block diagram of an embodiment of the present invention including a dual integrated charge pump power supply and a RS-232C receiver and transmitter.

#### DESCRIPTION OF A PREFERRED EMBODIMENT

Referring first to FIG. 1(a), simplified conceptual schematic drawing of the basic charge pump circuit of the present invention, the circuit of the present invention operates by placing an input voltage upon one of the two transfer capacitors via a series of switches. The charge in that capacitor is then transferred to one of two reservoir capacitors. The polarity of the voltage is established via the switch interconnecting scheme.

More specifically, the operation of the circuit of FIG. 1(a) is time-divided into two segments, or phases. In a first phase, voltage from a voltage source is placed on transfer capacitors. During a second phase the voltage on the transfer capacitors is transferred to the reservoir capacitors.

Referring first to the positive voltage doubler portion of the circuit, transfer capacitor 10 is charged from voltage source 12 (having a value  $V_{cc}$ ) by closing switches 14 and 16 while switches 18 and 20 remain

open during a first phase. During a second phase switches 14 and 16 are open and switches 18 and 20 are closed.

As can be seen from FIG. 1(a), when switches 18 and 20 are closed during the second phase the voltage source 12 is effectively placed in series with the voltage stored across reservoir capacitor 10 and thus the sum of the voltage across voltage source 12 and capacitor 10 is placed across reservoir capacitor 22.

The inverting portion of the voltage doubler circuit operates as follows: transfer capacitor 24 is charged to the voltage across reservoir capacitor 22 via the switches 26 and 23 which are closed during the first phase of operation of the circuit while switches 30 and 32 remain open. During the second phase of circuit operation switches 26 and 23 are opened and the voltage across transfer capacitor 24 is placed on reservoir capacitor 34 via the closing of switches 30 and 32. Those of ordinary skill in the art will note that the circuit configuration is such that when the voltage across transfer capacitor 24 is placed across reservoir capacitor 34 the positive end of transfer capacitor 24 is connected to ground line 36 through switch 32 and the negative end of capacitor 24 is connected to the side of reservoir capacitor 34 connected to  $-2 V_{cc}$  output line 38. The polarity of the voltage across reservoir capacitor 34 with respect to ground line 36 is thus such that the voltage across reservoir capacitor 34 is negative. The output of reservoir capacitor 22 is connected to  $+2 V_{cc}$  output line 40.

The first and second phases of circuit operation described above are repeated at a frequency which may range from approximately 100 hertz to 100's of kilohertz or higher. It has been found that a frequency of approximately 15 K Hz performs satisfactorily for the purposes of the present invention.

The foregoing represents an idealized characterization of the operation of the circuit of FIG. 1(a). Those of ordinary skill in the art will readily realize that it will take several first and second phase cycles before the resultant voltage between ground terminal 36 and  $+2 V_{cc}$  output terminal 40 actually reaches a voltage value of  $+2 V_{cc}$ . Likewise, it will be appreciated that several cycles are also needed for the voltage between ground terminal 36 and  $-2 V_{cc}$  output terminal 38 arrives at a voltage of  $-2 V_{cc}$ .

Those of ordinary skill in the art will also realize that the amount of current which may be drawn from the output of the circuit of FIG. 1(a) depends on the relative sizes of transfer capacitors 10 and 24 and reservoir capacitors 22 and 34, as well as the on impedance of switches 14, 16, 18, 20, 26, 28, 32 and 30.

It will also be apparent that the voltage appearing between output terminals 36 and 38 or 36 and 40 will be approximately twice the input voltage supplied by voltage source 12. Those of ordinary skill in the art will appreciate that other multiples of the input voltage  $V_{cc}$  at voltage source 12, are readily achievable using the concept of the present invention.

Turning now to FIG. 1(b), it is seen that in an actual embodiment of the present invention switches 14, 16, 18, 20, 26, 28, 30 and 32 have been replaced with MOS transistors. Thus, switch 14 is replaced by P-channel MOS transistor 14(a), switch 16 is replaced by N-channel MOS transistor 16(a), switch 18 is replaced by P-channel MOS transistor 18(a), switch 20 is replaced by P-channel MOS transistor 20(a), switch 26 is replaced by P-channel MOS transistor 26(a), switch 28 is re-

placed by N-channel MOS transistor 28(a), switch 30 is replaced by N-channel MOS transistor 30(a), switch 32 is replaced by N-channel MOS transistor 32(a).

The time controlled operation of the circuit of FIG. 1(b) is implemented by phase control unit 42. Phase control unit 42 drives all of the gates of the MOS devices, 14(a), 16(a), 18(a), 20(a), 26(a), 28(a), 30(a), and 32(a) via gate control lines 44 and 46. Gate control lines 44 and 46 are connected to the gates of the P-channel MOS transistors and N-channel MOS transistors, used as MOS switches, such that the switches are turned on and off appropriately as described herein during the first and second phases of the circuit operation.

Those of ordinary skill in the art will readily appreciate that, in order to insure efficient power transfer, that switching of MOS switching devices should be accomplished on a break before make basis or, at worst case, on a simultaneous switching basis. Those of ordinary skill in the art will also realize that the order of phases could be reversed. Alternatively, a first clock could be used to control the sets of MOS switches controlling transfer capacitor 10 and reservoir capacitor 22, and a second clock could be used to control the sets of MOS switches controlling transfer capacitor 24 and reservoir capacitor 34.

It should be understood for purposes of this disclosure, that all of the capacitors shown in FIGS. 1(a) and 1(b) would be located outboard of the integrated circuit in an actual embodiment. That is, these capacitors are external components which connect to the integrated MOS switches on the semiconductor substrate via terminals provided on the semiconductor substrate for that purpose. For an operating frequency of 15 KHz, 20 microfarads is a sufficient size for all capacitors. Those of ordinary skill in the art will readily appreciate that as the switching frequency is increased the values of the capacitors will drop, but that switching losses will increase due to the changing to discharging at the clock rate of its parasitic nodal capacitances in the MOS devices. Conversely, as the switching frequency decreases, the size of the capacitors would increase, with the concomitant disadvantage that the increasing capacitor size is accompanied by increasing physical size of the capacitors.

For a current capacity of 10 milliamperes at +10 volts and -10 volts, the MOS switching devices should have a channel width to channel length ratio of 5000 to 10,000, with channel lengths of approximately five microns. Those of ordinary skill in the art will recognize that the range of current output of the circuit described herein could be as large as approximately one ampere, however, the MOS devices would have to be scaled accordingly as is well known in the art.

Referring now to FIG. 2, an embodiment of the phase control unit 42 of the present invention, the operation of phase control unit 42 is disclosed. Those of ordinary skill in the art will recognize that phase control unit 42 may consist of three conventional CMOS inverter circuits each comprised of a P-channel and N-channel MOS transistor pair. The embodiment of FIG. 2 contains a first CMOS inverter comprised of P-channel MOS transistor 44 and N-channel MOS transistor 46, the inverter comprised of P-channel MOS transistor 48 and N-channel MOS transistor 50, and the inverter comprised of P-channel MOS transistor 52 and N-channel MOS transistor 54.

These three inverter pairs are driven by oscillator 56, which may be any conventional oscillator configured

from CMOS elements as is well known to those skilled in the art.

The circuit of FIG. 2 is powered by +2 Vcc and -2 Vcc lines 36 and 40. This assured that the voltage swing on gate lines 44 and 46 will span approximately the entire power supply range, thus ensuring that all of the gates of the P-channel and N-channel devices which they drive will be as fully turned on as possible and can be turned off since all transistors and enhancement types. This will guarantee as low an on-state impedance of the MOS switches as possible thus maximizing the efficiency and current drive capabilities of the present invention.

In the illustration of a preferred embodiment of the present invention depicted in FIG. 1(a), the substrate connections of the MOS devices are shown uncommitted. Those of ordinary skill in the art will realize that junction isolated MOS transistors such as used in FIG. 1(b) are four-terminal devices and that both the gate terminal and the substrate terminal are control terminals. The turn-on voltage of the gate terminal is affected by the reverse bias on the substrate to source junction. As that reverse bias is increased, the turn on voltage of the device also increases. The affect is significantly greater for an N-channel transistor than a P-channel transistor.

As the substrate-to-source voltage increases the gate turn voltage of the device also increases, thus potentially increasing the on resistance of the device to a point where circuit operation could be seriously effected. Since, in a circuit of this nature, the drain-source resistance in the on state should be as low as possible, it is desirable to connect each N-channel MOS transistor substrate to its source.

With respect to P-channel transistors the effect of this reverse substrate source biasing is about half of that for N-channel MOS transistors due to lighter channel impurity doping densities. The most practical solution in the case of the P-channel MOS transistors is to connect all P-channel substrates to the most positive voltage in the circuit. That voltage is, as seen from FIG. 1(a) +2 Vcc which appears on positive supply line 40. These connections are shown in respect to FIG. 3.

Prior to start-up, it is reasonable to assume that zero voltage exists on all capacitors. At start-up, reservoir capacitor 22 may be connected to ground line 36 or to -2 Vcc line 38. Reservoir capacitor 22 will be immediately charged with the source substrate diodes of P-channel MOS transistors 14(a) and 18(a) to a voltage of approximately Vcc -0.6 of a volt. The voltage on reservoir capacitor 34 could lie somewhere between ground line 36 and the voltage on reservoir capacitor 22; depending which of transistors 26(a), 28(a), 30(a) or 32(a) were conducting (if any). This results in a voltage on the -2 Vcc line that could be such that N-channel that transistor 16(a) and other transistors being turned on. Under these conditions, a voltage between +2 Vcc drives the gates of all of the output transistors and is indeterminate. Thus both start-up and operation is not assured.

If the other possible start-up conditions of the capacitor and MOS device connections and off/on states are assumed, those of ordinary skill in the art will readily appreciate that the start-up and operation of the circuit of FIGS. 1 and 2 is not assured.

The solution to this dilemma is to place a clamp on the -2 Vcc line 38 to clamp that voltage line to assure that it will never assume a voltage substantially more

positive than that appearing on ground line 36. The +2 Vcc line 40 is also clamped so that it will never assume a voltage substantially more negative than the voltage Vcc on approximately Vcc -0.6 volts.

While those of ordinary skill in the art will realize that, conceptually, a diode would be an ideal clamping means for the -2 Vcc line 38, it is not possible to fabricate a simple PN junction diode in a MOS process. A junction transistor will always be created by an attempt to fabricate a diode. The presence of such a transistor in the circuit of FIG. 1(b) would cause excess wasted current to flow in the circuit, because of its beta or current gain.

In a preferred embodiment of the present invention, this clamp is comprised of a lateral NPN transistor. This lateral NPN transistor is shown in FIG. 3. The lateral collector and base of this device are both connected to -2 Vcc line 38, its vertical collector connected to +2 Vcc. The lateral collector serves to minimize the effective current gain of the unwanted but inherent vertical collector of NPN transistor 58, which would otherwise cause excess current flow from the +2 Vcc line through ground. Unless the -2 Vcc line 38 exceeds ground by approximately 0.6 of a volt in the positive direction, this device will not conduct current. If the -2 Vcc line equals approximately 0.6 volts, the device turns on and current will flow in approximately equal portions through both collectors to maintain the -2 Vcc line at no greater than zero plus approximately 0.6 volts.

With respect to the clamp for +2 Vcc line 40, the action of the inherent junction diodes 59(a) and 59(b) present between the drain and substrate of devices 14(a) and 18(a) serve to clamp the +2 Vcc line to a voltage no more negative than the input positive supply voltage Vcc minus approximately 0.6 volts.

Consequently the voltages on +2 Vcc line and -2 Vcc line are both well defined. Additionally the voltage difference between +2 Vcc line 38 and -2 Vcc line 40 at start-up is (Vcc - 1.2) volts and is also well defined. This value of voltage is sufficiently large to guarantee operation of the drive circuitry for the gates of the output transistors until the charge pumps charge the lines +2 Vcc (40) and -2 Vcc (38) to those voltages.

The lateral NPN transistor used to clamp -2 Vcc line 38 is fabricated using conventional CMOS fabrication techniques. For a current drain of plus and minus 10 mA at 10 volts, the periphery of the emitter for the lateral NPN transistor can typically be 100 microns. Those of ordinary skill in the art will appreciate that the size of this device may be scaled to accommodate larger current carrying requirements, and its periphery need not be larger than 1000 microns.

Referring now to FIG. 4, a substrate profile drawing of a dual collector lateral NPN transistor 58, that transistor 58 is fabricated on a portion of the lightly doped N type substrate material 60 in a P-well 62. P-well 62 is placed into substrate 60 using common CMOS processing techniques. N region 64 serves as the emitter of the lateral NPN transistor, and is surrounded by N region 66 which serves as the lateral collector. P region 68 in P-well 62 serves as the base contact, it being understood by those skilled in the art that P-well 62 itself serves as the base of lateral NPN transistor 58. N-region 70 located in a region of substrate 60 outside of P-well 62 serves as the unwanted, but inherent vertical collector of NPN lateral transistor 58.

When the base emitter junction of lateral NPN transistor 58 is forward biased, minority carriers injected by the emitter into the base are collected by both the vertical and lateral collectors in roughly equal amounts.

Connecting the lateral collectors to the common base reduces the vertical collector current to approximately  $\frac{1}{2}$  of the clamp current. If a vertical NPN transistor had been used alone, the clamp current (base current) would be multiplied by the beta (approximately 500 of the device) thereby wasting large amounts of current.

Referring now to FIGS. 1(b) and 3, during start-up reservoir capacitor 22 is charged by the forward biased condition of the source-substrate diodes 59(a) and 59(b) of P-channel device 14(a) and the drain substrate diode of P-channel device 18(a). The initial current surge through these diodes can be hundreds of milliamperes and thus be well above the holding current of the inherent SCR type four layer diode device which exists in the circuit.

Such a four layer device is schematically represented in FIG. 5(a). Referring to FIG. 5(a), it is seen that the four layer device is made up of PNP transistor 72, NPN transistor 74, resistor 76, and resistor 78. Resistor 76 is connected across the base-emitter junction of PNP transistor 72 while resistor 78 is connected across the base-emitter junction of PNP transistor 74. The base of NPN transistor 74 is connected to the collector of PNP transistor 72 and the base of PNP transistor 72 is connected to the collector of NPN transistor 74. The connection of the emitter junction of PNP transistor 72 and resistor 76 form the anode connection 78 of the four layer device and the intersection of resistor 78 and the emitter of NPN transistor 74 form the cathode connection 80 of the four layer device.

As will be appreciated by those of ordinary skill in the art, the four layer device shown in FIG. 5(a) will enter a low impedance state between its anode 80 and cathode 82 after suitable triggering if the product of the betas of the two equivalent transistors is greater than one and the anode current into the four layer device is greater than the turn on voltage of either transistor divided by its equivalent base emitter shunting resistor, whichever is greatest.

Referring now to FIGS. 3, 5(a) and 5(b), it will be apparent to those of ordinary skill in the art that such a four layer device occurs in the circuit of FIG. 3. The sources of either of P-channel devices 14(a) and 18(a) (shown diagrammatically as P region 84 in FIG. 5(b)) represent the emitter of PNP transistor 72 of FIG. 5. The semiconductor substrate 60 forms the base of PNP transistor 72 as well as the collector of NPN transistor 74. P-well 86 forms the collector of PNP transistor 72 as well as the base of NPN transistor 74. The source of either of N-channel transistors 16(a) and 32(a), one of which is shown as N region 88 of FIG. 5(b) forms the emitter of NPN transistor 74. Resistor 76 is formed by the bulk resistance of the P-well 86. Likewise, the resistor 78 is formed by the bulk resistance of the substrate material. Those skilled in the art will note that regions such as P region 90 in P-well 86 and N region 92 in substrate 60 serve as low resistance surface planes commonly used in CMOS technology to buss supply voltages to the surfaces of substrate and P-wells.

In order to trigger the four layer device into its low impedance state, currents must be injected into the base of either of transistors 72 or 74, either the P-well 86 or the substrate 60. These currents must be greater than the holding current required for the four layer device.

This condition can occur by various means. For example, a very rapid rate of increase in the anode-cathode voltage will force current into the bases of transistors 72 and 74 due to the charging of the collector-base junction capacitors inherent in those devices. Alternatively, forward biasing of a region in the substrate junction adjacent to the P-well 86 and P-region 84 forming the emitter of transistor 72 could induce base currents to flow in transistor 72 and 74 sufficient to exceed holding current values. Either of these conditions could occur at start-up of the circuit of FIG. 3.

In order for the inverting doubler charge pump circuit of the present invention to reliably operate, it is necessary to assure that this possible latch-up condition can never occur. One method which is used in some CMOS circuits to inhibit the possibility of latch-up would be to insert high value resistors in series with either or both of the emitters of NPN transistor 74 or PNP transistor 72. This method, however, in the present invention would result in an unacceptably high value of on impedance for the MOS switches.

Another method of assuring that the latch-up condition never occurs is disclosed as an aspect of the present invention. The product of the betas of PNP transistor 72 and NPN transistor 74 is made less than unity. Thus, the current flowing between the anode terminal 80 and cathode terminal 82 of the four layer device will never reach a value great enough to equal the holding current necessary to sustain that device in its low impedance state.

Referring now to FIG. 6(a), another four layer device 100 composed of equivalent NPN and PNP transistors is shown. However, unlike the circuit of FIG. 5(a) the four layer device depicted in FIG. 6(a), having anode terminal 102 and cathode terminal 104, a single collector NPN transistor 106 and a multiple collector PNP transistor 108 as well as resistors 110 and 112. The multiple PNP collectors (shown at 114) are tied back to the base of the PNP transistor 108. Only a single multiple collector is connected to the base of NPN transistor 106. These collectors 114 are fabricated on substrate 60 in a region located between the emitter of NPN transistor 106 and the base of PNP transistor 108.

The function of the serial collectors 114 is to guard the forward biased PN junction formed between P regions 128 or 138 and substrate 60 by collecting the minority carriers which are injected into the substrate 60. These carriers are thus prevented from reaching the base of the PNP transistor 108 and assure that the beta product of these two transistors is less than unity. Most of the minority carriers injected into the substrate are collected by these serial collectors before they can diffuse and be collected by the P-well which is also the base of the NPN transistor. This may be designed to reduce the PNP beta to a value of less than the reciprocal of the NPN beta thereby preventing latch-up.

Referring now to FIG. 6(b), a semiconductor profile drawing of four layer device 100 of FIG. 6(a), NPN transistor 106 is formed in P-well 120. Contact 122, contacting N region 124 in P-well 120, constitutes cathode 104 of four layer device 100. This N region may be the source of either N-channel MOS transistor 16(a) or N-channel MOS transistor 32(a) from FIGS. 1 and 3. N region 124 forms the emitter of NPN transistor 106 and P-well 120 forms the base of NPN transistor 106. Substrate 60 forms the collector of NPN transistor 106, as well as the base of PNP transistor 112.

Contact 126, contacting P region 128 is at Vcc potential. P region 128 may be either the source of P channel MOS transistor 14(a) or the drain of P-channel MOS transistor 18(a) from FIGS. 1 and 3. P region 128 forms the emitter of PNP transistor 108.

P regions 130(a) through 130(e), in substrate 60, form the multiple collectors of PNP transistors 108 (shown at 114 in FIG. 6(a)). Multiple collectors 130(a) through 130(e) are connected together at the surface of the semiconductor substrate 60 by layer 132 which may be made of aluminum and fabricated during the metalization step of a conventional CMOS fabrication process. N regions 134(a) through 134(d), disposed in between P regions 130(a) through 130(e) are used for the purpose of making a low impedance contact between the +2 Vcc line and the substrate. P-well 120, the base of NPN transistor 106, also serves as the single collector of PNP transistor 108, as shown in FIG. 6(a). The regions 135, shown adjacent to layer 132, are the gate oxide layer of the MOS structures.

As is shown in FIG. 6(b) the multiple collectors of PNP transistor 114 are interposed in between the N-channel MOS transistor 16(a) in the P-well formed of N regions 124 and 136. This device, for illustration, shown as 16(a) on FIG. 6(b), has drain region 138 and gate 140. This device, for illustration, shown as 18(a) on FIG. 6(b), has drain region 138 and gate region 142. P-channel MOS transistor 14(a) formed of P region 128 and P region 138. In this manner these multiple collectors 130(a) through 130(e) are in a position to collect most of the minority carriers which are injected into the semiconductor substrate as a result of forward biasing at start-up of the parasitic PN junctions formed during the CMOS fabrication process.

Depending on the CMOS process used, the number of multiple collectors 114 may range from 1 to approximately 10. Furthermore, the spacing between the injecting PN junction and the nearest P-well should be typically anywhere from 25 to 500 microns. Spacing may be reduced if the lifetime of the substrate minority carriers is particularly low and or the substrate resistivity is very low (less than one ohm-centimeter). In the presently preferred embodiment the spacing between the injecting PN junctions and the nearest P-well is approximately 150 microns and four multiple collectors 114 are used. This is based upon a process using a substrate having a substrate resistivity of approximately 2.5 ohm-cm.

Although the presently preferred embodiment has been disclosed as a P-well CMOS embodiment, those of ordinary skill in the art will recognize that N-well CMOS technology could also be used without departing from the spirit and scope of the present invention. Those of ordinary skill in the art will readily understand from the disclosure herein how to fabricate such an N-well embodiment.

Referring now to FIG. 7, a block diagram of a preferred embodiment of the present invention including dual charge pump power supply 200, previously described, RS-232C transmitter circuit 202, and RS-232 receiver circuit 204. These elements are shown diagrammatically as fabricated on a single piece of semiconductor substrate material 206. Positive reservoir capacitor 22 is shown connected to the semiconductor substrate via terminal pads 208 and 210. Negative reservoir capacitor 34 is shown connected to the substrate via terminal pads 208 and 212. Positive transfer capacitor 10 and negative transfer capacitor 24 are shown connected to

the substrate via terminal pads 214, 216, 218 and 220 respectively. An input voltage is provided to the circuit at Vcc input terminal pad 222 and ground input terminal pad 224. Those of ordinary skill in the art will readily realize that ground input terminal 224 and terminal pad 208 may in some embodiments be the same connection terminal pad. The data input to RS-232 transmitter 202 is provided at terminal pad 226 and the output of RS-232 transmitter 202 is provided at terminal pad 228. The data input to RS-232 receiver 204 is provided at terminal pad 230 and the data output of RS-232 receiver 204 so provided at terminal pad 232.

A monolithic integrated circuit containing the dual charge pump power supply 200 and RS-232 transmitter 202 and receiver 204 may be fabricated as a monolithic integrated circuit. The only outboard components required for operation of the circuit are positive and negative reservoir capacitors 22 and 34 and the positive and negative transfer capacitors 10 and 24.

While the preferred embodiment of FIG. 7 shows a single RS-232 transmitter 202 and a single RS-232 receiver 204, those of ordinary skill in the art will readily recognize that other combinations of receivers and transmitters could be added without departing from the spirit of the invention. It is noted, however, that an embodiment of the circuit of FIG. 7 which contains only one or more RS-232 receivers 204, and no RS-232 transmitters 202, does not require a negative power supply connection. This is because the negative swing of the RS-232 format signal is usually disregarded by the receiver circuitry.

The RS-232 transmitter circuit 202, as well as the RS-232 receiver circuit 204 may be conventionally configured out of CMOS elements as is well known in the art. For example, RS-232 transmitter circuit 202 may be a CMOS inverter with a level shifter to translate TTL logic levels to the RS-232 format, as is known in the art. Alternatively, it may be configured similarly to the MC 1488 circuit, manufactured by Motorola. RS-232 receiver circuits 204 may be a CMOS inverter with a level shifter to translate the incoming RS-232 format signal to TTL logic levels as is known in the art. Alternatively, it may be configured similarly to the MC 1489 circuit manufactured by Motorola.

A preferred embodiment of the present invention has been disclosed. Those of ordinary skill in the art will readily recognize that other embodiments are possible which do not differ in material respects. It is the intention of the inventors to include such embodiment within the scope of the appended claims.

We claim:

1. An integrated single-chip voltage supply comprising:

a means adapted to be connected to a supply voltage for charging a capacitor approximately to a supply voltage;

a means for coupling said charged capacitor in series with said supply voltage to create a source of positive voltage approximately double the supply voltage; and

a means for inverting said doubled voltage and making it available on the same chip, thereby providing a source of two available supply voltages on the same chip, one being a positive voltage approximately two times said supply voltage, and the other being a negative voltage approximately two times said supply voltage.

2. The integrated single-chip voltage supply of claim 1 further characterized by said coupling means including a means for charging a second capacitor to approximately two times said supply voltage, and said inverting means including a means for inverting the positive doubled voltage on said second capacitor to provide an available negative voltage on the same chip in magnitude approximately twice said supply voltage.

3. An integrated voltage supply and RS-232 transmitter circuit or the same semiconductor chip, comprising: an RS-232 transmitter circuit;

a means adapted to be connected to a supply voltage for charging a capacitor approximately to a supply voltage;

a means for coupling said charged capacitor in series with said supply voltage to create a source of positive voltage approximately double the supply voltage;

a means for inverting said doubled voltage and making it available on the same chip, thereby providing a source of two available supply voltages on the same chip, one being a positive voltage approximately two times said supply voltage, and the other being a negative voltage approximately two times said supply voltage; and

means connecting said doubled voltage and said inverted doubled voltage to said RS-232 transmitter circuit for powering said RS-232 transmitter circuit.

4. The integrated single-chip voltage supply of claim 3 further characterized by said coupling means including a means for charging a second capacitor to approximately two times said supply voltage, and said inverting means including a means for inverting the positive doubled voltage on said second capacitor to provide an available negative voltage of magnitude approximately twice said supply voltage.

\* \* \* \* \*



# United States Patent [19]

Douglas et al.

[11] Patent Number: 5,038,325

[45] Date of Patent: Aug. 6, 1991

## [54] HIGH EFFICIENCY CHARGE PUMP CIRCUIT

[75] Inventors: Kurt P. Douglas; Wen-Foo Chern, both of Boise, Id.

[73] Assignee: Micron Technology Inc., Boise, Id.

[21] Appl. No.: 487,773

[22] Filed: Mar. 26, 1990

[51] Int. Cl.<sup>5</sup> ..... G11C 11/406; G11C 11/40

[52] U.S. Cl. .... 365/189.06; 365/189.09; 365/189.11; 365/203; 307/482; 307/578

[58] Field of Search ..... 365/189.06, 189.09, 365/189.11, 203, 204, 226; 307/578, 482

## [56] References Cited

### U.S. PATENT DOCUMENTS

4,404,661	9/1983	Nagayama	365/204 X
4,616,143	10/1986	Miyamoto	307/482 X
4,689,495	8/1987	Liu	307/482 X
4,769,784	9/1988	Doluca et al.	365/226 X
4,804,870	2/1989	Mahmud	307/482
4,896,297	1/1990	Miyatake	365/204 X
4,901,280	2/1990	Patel	365/203 X

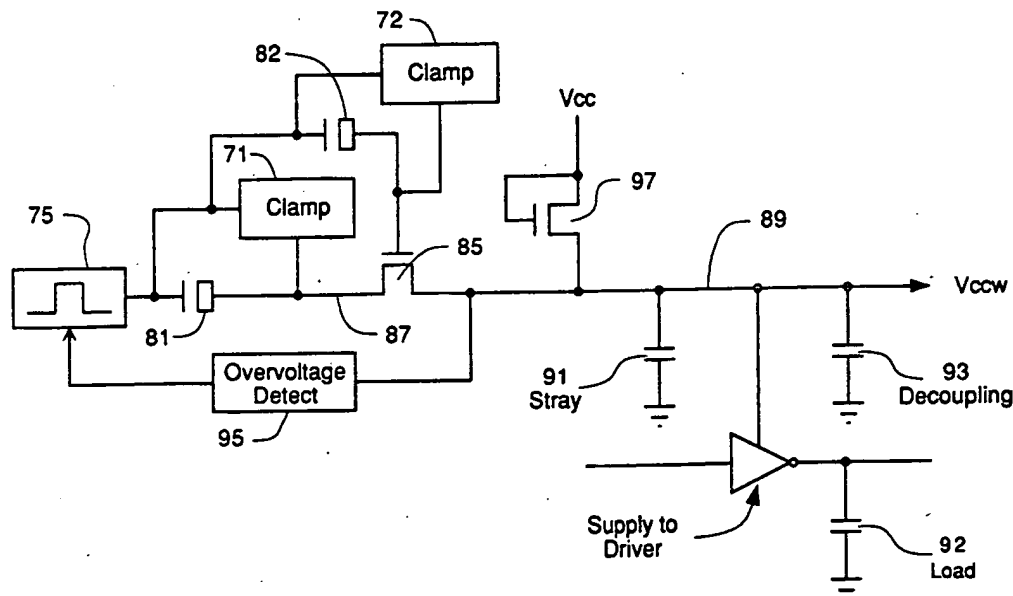
4,954,731 9/1990 Dhong et al. .... 307/482

Primary Examiner—Alyssa H. Bowler

## [57] ABSTRACT

An integrated circuit includes a charge pump to provide current at a potential which is greater than a supply potential. An oscillator provides an output to a pair of capacitors. Each capacitor is bypassed respectively by one of a pair of clamp circuits. An output transistor is gated by one of the clamp circuits to maintain a continuous output at an elevated potential, while reducing power loss caused by impedances within the charge pump circuit. By using the charge pump as a source of elevated potential, the circuit layout of the DRAM array is simplified and the potential boosting circuitry can be located outside of the array, on the periphery of the integrated circuit. When used with an integrated circuit device, such as a DRAM, the current from the charge pump may be supplied to nodes on isolation devices and nodes on word lines, thereby improving the performance of the DRAM without substantially changing the circuit configuration of the DRAM array.

13 Claims, 4 Drawing Sheets



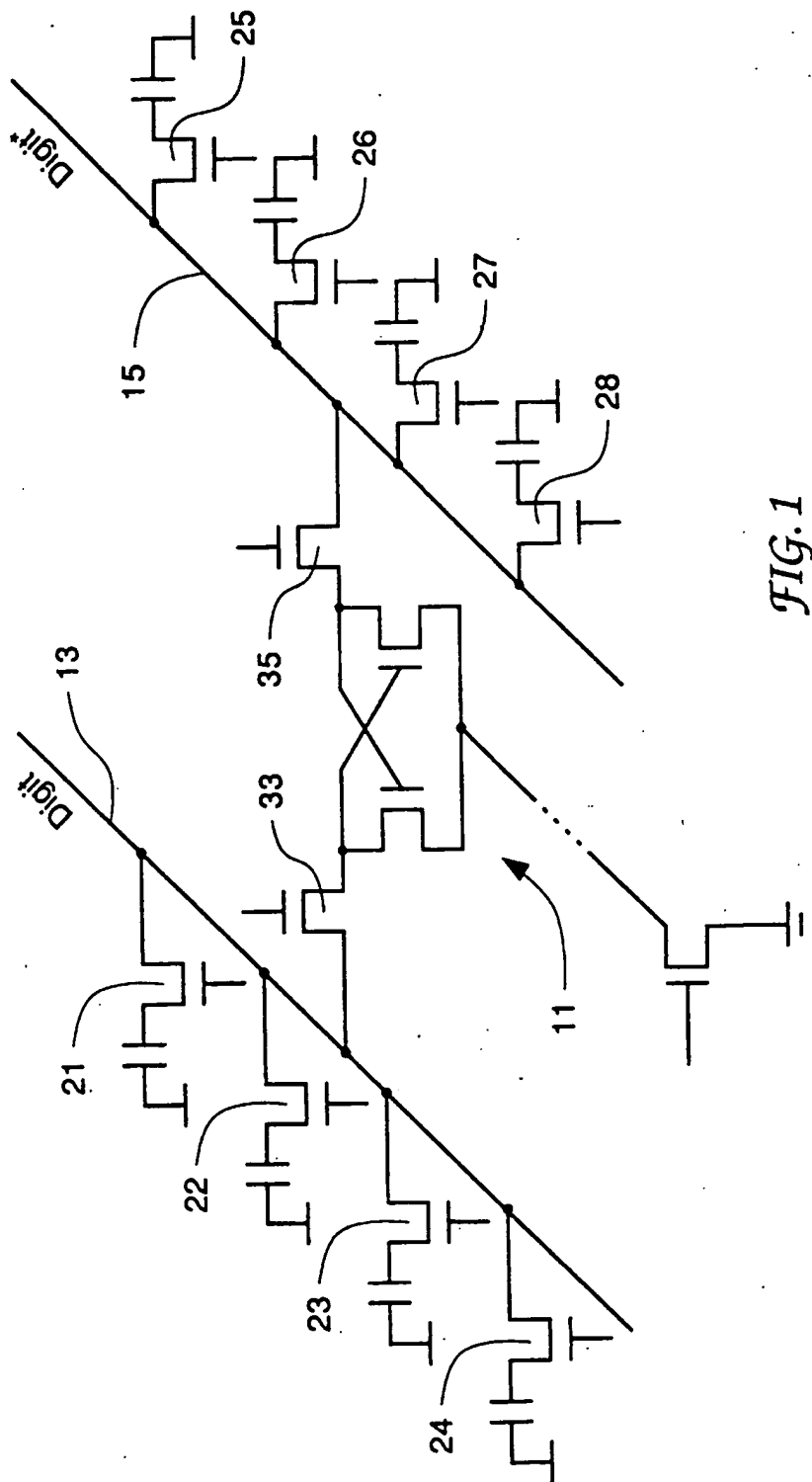
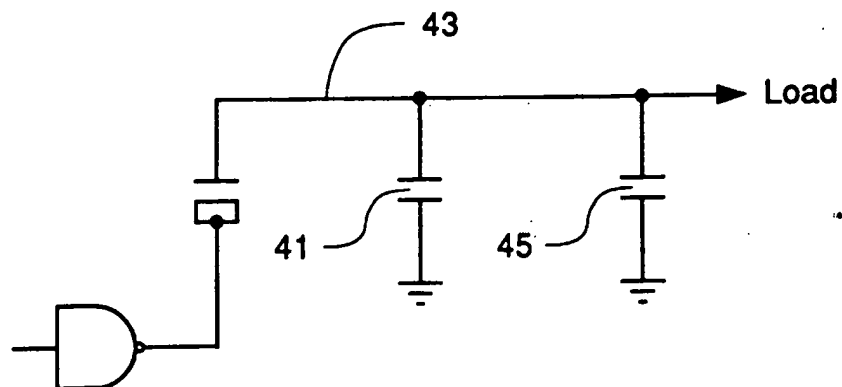
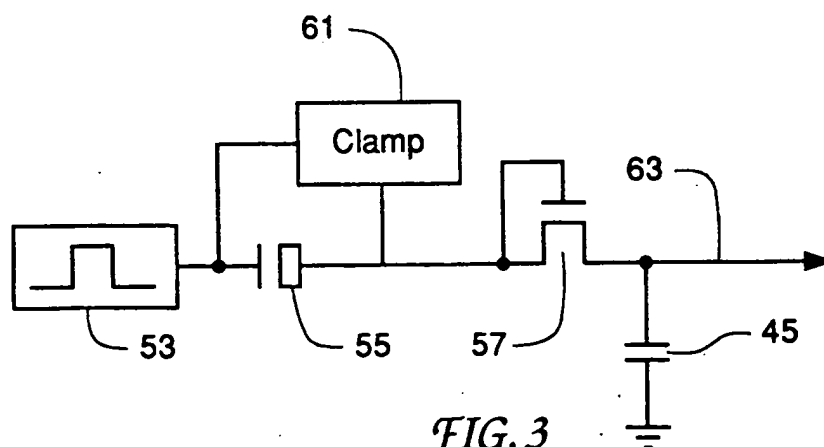


FIG. 1



*FIG. 2*  
(PRIOR ART)



*FIG. 3*  
(PRIOR ART)

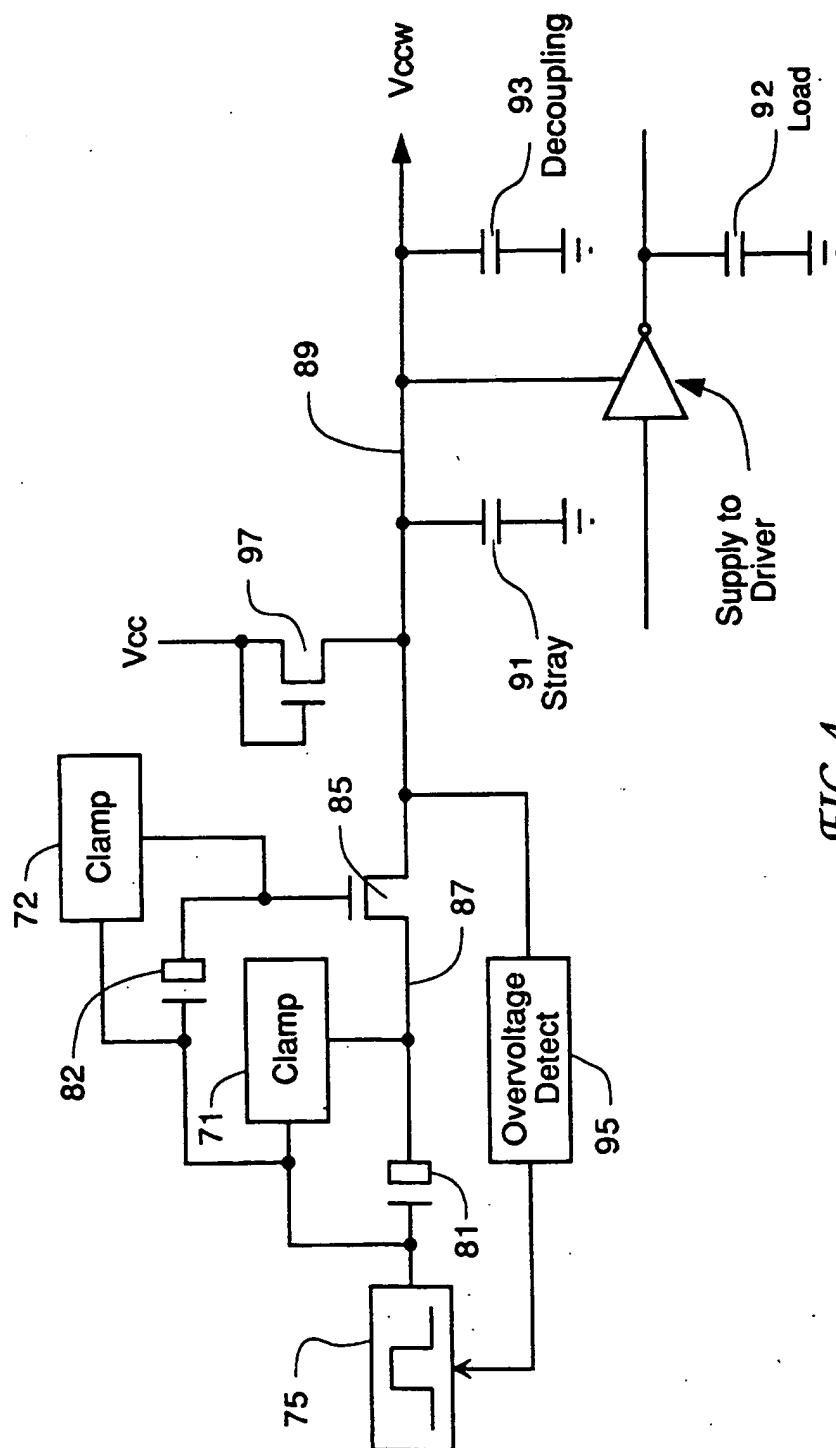


FIG. 4

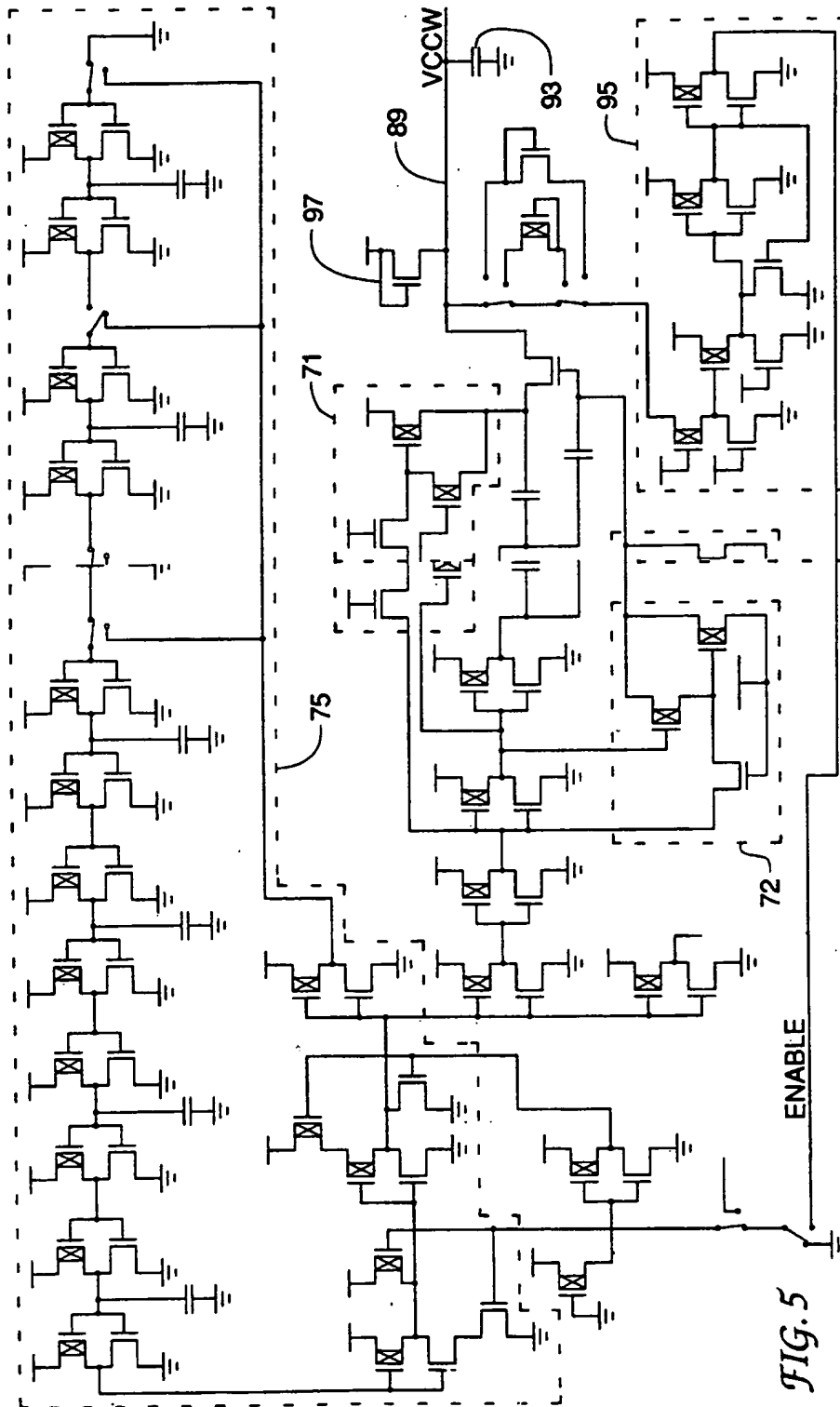


FIG. 5

## HIGH EFFICIENCY CHARGE PUMP CIRCUIT

## FIELD OF THE INVENTION

This invention relates to semiconductor circuit devices and more particularly to circuitry for providing current to sense amps on semiconductor integrated circuits. The invention is particularly applicable to dynamic random access memory devices (DRAMs).

## BACKGROUND OF THE INVENTION

The invention uses various materials which are electrically either conductive, insulating or semiconducting, although the completed semiconductor circuit device itself is usually referred to as a "semiconductor". One of the materials used is silicon, which is used as either single crystal silicon or as polycrystalline silicon material, referred to as polysilicon or "poly" in this disclosure.

In the operation of certain semiconductor circuit devices, it is necessary to draw up a node of the sense amp to a potential above  $V_{CC}$ . In the conception of the present invention, these nodes occur on iso (isolation) devices on an array of a memory device and on word lines. Memory devices which use such iso devices on an array include DRAMs (dynamic random access memories). A typical arrangement of DRAM memory cells with a sense amp is shown in FIG. 1. Other types of memory devices, such as static RAMs and video RAMs also may have similar circuit arrangements. An isolation device (iso device) is present in order to isolate a digit load from the sense amp, so that the sense amp can amplify the signal faster than if the digits were directly attached to the sense amp.

Gating an iso device with a higher potential speed read time reduces the required size of the iso device. These results are obtained because an increase in potential increases  $V_{GS}$ .

In a DRAM, the iso device is used with either multiplexed or non-multiplexed sense amps. In the case of multiplexed sense amps, reducing the size of the iso device allows configuring the circuit layout with the iso-devices "on pitch" (two pitch) rather than in a four pitch pattern. This simplifies layout design because the two pitch layout provides a configuration in which, for each sense amp, both iso devices are individually aligned with that sense amp. With four pitch layout patterns, more than one sense amp must be balanced as a unit.

The decrease in device width is obtained because increasing potential to gate gives the device a greater effective electrical transistor width.

In the prior art, bootstrapping had been used in order to charge nodes of a circuit to an increased potential. A typical bootstrap circuit is shown in FIG. 2. The bootstrap circuit provides an increased voltage level in response to a particular sequence, such as the receipt of a timing signal. The charge pump, on the other hand, provides a continuous output and an increased potential. The continuous high-potential output means that timing of the high-potential supply is not critical. This is particularly important when a high-potential node is used for the word line of a DRAM memory device, since the time required to select and address the word line is critical to the access speed of the DRAM.

Because the boot strap circuit is timed, individual boot strap circuits must be provided for each of several nodes, each of which receives current at the elevated

potentials at different times. The charge pump, with its continuous output, can be used for supplying current to each of these nodes.

Boot strap circuits were also located at the location of the device controlled by the boot strap circuit. This was because individual boot strap circuits were dedicated to particular driven circuits in which different sequences were timed. Because the boot strap circuits were dedicated to particular driven circuits and because the boot strap circuits were timed to coincide with operation of the particular driven circuit, the amount of circuit area utilized by all of the circuitry was increased. This increase could occur despite the possibility of having smaller individual transistors in the driven circuits.

The ability to write a continuous voltage supply is particularly important in the case of word lines on DRAM devices. This is because, in DRAMs, word line addressing is particularly critical with respect to the speed of the part. Therefore, while providing a charge pump rather than a boot-strap circuit, the timing of the elevated potential output is not a condition precedent to word line access, simply because the charge pump output is not timed.

Prior art charge pumps consisted of an oscillator and capacitor. In order to prevent latchup, a clamp circuit was used in order to control current from the oscillator to one side of the capacitor. The use of an oscillator and capacitor with a single clamp circuit provided a relatively constant elevated potential, but was somewhat inefficient when compared to a boot strap circuit. It would be desirable to provide a charge pump circuit which has the relative efficiencies of a boot strap circuit but yet provides a continuous output such as is associated with a charge pump.

Prior art charge pumps use an oscillator and capacitor, along with a clamp circuit. The oscillator provides current at a supply potential to one side of the capacitor and the clamp circuit is used to charge the other side. The current supplied to the capacitor by the oscillator generates an increased potential at an output node of the circuit. This prior art circuit is shown in FIG. 3.

It is desirable to design an auxiliary circuit, so that in the event that the auxiliary circuit does not function as anticipated, the auxiliary circuit can be bypassed. Specifically, during the design of an integrated circuit such as a DRAM, it is not known whether the electrical characteristics of the charge pump will exceed the limits of the circuit which receives the current from the charge pump. If the limits are exceeded, it is desirable to be able to make a small modification in the masks and thereby bypass the charge pump without sacrificing the remainder of the circuit design.

It is also likely that different product applications for integrated circuit parts may have different requirements of speed and supply voltage. If the auxiliary circuit provides a desirable function for one product application, but would make the part unsuitable for another product application, it would be desirable to be able to selectively bypass the auxiliary circuit. This would enable a single integrated circuit layout design to be used for both parts.

Ideally, an auxiliary circuit should automatically respond to circuit conditions which makes the auxiliary circuit unsuitable for its application. For example, a voltage boosting circuit would ideally attenuate its increased potential output or bypass itself as external

system voltage becomes sufficiently high to make the use of the boosting circuit undesirable.

### SUMMARY OF THE INVENTION

In accordance with the present invention, an integrated circuit device includes a charge pump to provide current at a potential which is greater than a supply potential. The current is supplied to certain nodes on the integrated circuit device in order to enhance the performance of the integrated circuit device.

When used with an integrated circuit device, such as a DRAM, the current from the charge pump may be supplied to nodes on isolation devices and nodes on word lines. This allows the nodes to be operated at an elevated potential, thereby improving the performance of the DRAM. This enhanced performance is achieved without substantially changing the circuit configuration of the DRAM array, so that, in the event that the use of the charge pump proves to be inopportune, the charge pump can be bypassed by minor changes in the masks used to produce the integrated circuit device. This configuration allows the same basic mask layout to be used in different DRAMs designed to operate under different parameters.

It is further possible to alter the inventive integrated circuit to function without its charge pump by fuse repair techniques. Fuse repair techniques permit a circuit on a device to be deliberately "damaged" by either direct application of energy, such as laser cutting, or by application of an excess amount of electrical energy through connection points (pinout connections) on an integrated circuit. This removes the functionality of a part of the circuit, and bypasses that circuit. In the case of a charge pump, the fuse repair would either permit the charge pump circuitry to directly conduct supply current to the output node of the charge pump, or would permit a separate circuit to conduct to the output node in lieu of the charge pump.

Likewise, it is possible to provide the charge pump with an overvoltage shutoff circuit. The overvoltage shutoff circuit would permit the charge pump to operate under conditions of low supply voltage, but allows the charge pump to be effectively bypassed when supply voltage is sufficiently high to make bypass desirable.

In accordance with the further aspect of the invention, the charge pump is designed to operate at a higher efficiency by the use of a pair of clamp circuits. An oscillator provides an output to a pair of capacitors. Each capacitor is bypassed respectively by one of the clamp circuits, and the clamp circuits are separately timed. The output of the first capacitor is also connected to an output transistor which is gated by the second clamp circuit connected in parallel to the second capacitor. The controlled gating of the output transistor permits the clamp circuit to maintain a continuous output at an elevated potential, while reducing power loss caused by impedances within the charge pump circuit.

By using the charge pump as a source of elevated potential, the circuit layout of the DRAM array is simplified and the potential boosting circuitry can be located outside of the array, on the periphery of the integrated circuit.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a configuration of sense amps in a DRAM array;

FIG. 2 (prior art) shows an equivalent circuit of the output of a bootstrap circuit;

FIG. 3 (prior art) schematically shows a prior art configuration of a charge pump;

FIG. 4 schematic block diagram of a charge pump constructed in accordance with the present invention; and

FIG. 5 schematically shows the charge pump of FIG. 4.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a sense amp 11 is connected between digit and digit\* lines 13, 15 on a memory array. The digit and digit\* lines 13, 15 are connected to an array of memory cells, such as cells 21-28 shown.

The memory cells 28-28 are connected to the digit and digit\* lines through word lines, such as word line 31. Iso devices 33, 35 are used to gate the current between the sense amp 11 and either of the digit and digit\* lines 13, 15 in order to permit the differential amp 11 to sense the relative levels of the digit and digit\* lines 13, 15. By selectively gating one of the memory cells 21-28 to either the digit or the digit\* lines, it is possible to detect the memory storage level in the memory cell. The memory storage level is either higher or lower than that of the unconnected digit and digit\* lines, according to whether the bit represented by that level is a logical low (zero) or high (one). Hence, the sense amp is a differential amplifier which senses the difference between one of the digit and digit\* lines connected to a selected memory cell and the other one of the digit and digit\* lines, which is not connected to a cell.

In order to increase the sensitivity of the differential amp 11 and to permit the differential amp 11 to more rapidly respond to the differential potential in the digit and digit\* lines 13, 15 of the iso devices 33, 35 must have a relatively large effective transistor width. One way to accomplish this without increasing the physical size of the iso devices 33, 35 is to gate the iso devices 33, 35 at a slightly elevated potential. In other words, it is advantageous to have  $V_{GS}$  greater than  $V_{CC}$ . Having  $V_{GS}$  greater than  $V_{CC}$  reduces resistance between gate and source, thereby increasing effective transistor width.

This is a trade off because smaller iso devices make sensing faster but slows down the time to fully discharge the DIGIT and DIGIT\* lines to ground. Bigger iso devices allow DIGIT or DIGIT\* to be written to opposite states faster. For a given desired drive ability, the iso device can be smaller if  $V_{GS}$  is elevated. Furthermore, a smaller iso device is easier to design into high density circuitry.

If a bootstrap circuit is used to provide an elevated voltage, the equivalent circuit appears as shown in FIG. 2. The bootstrap circuit includes a boost capacitor 41 which provides current at an elevated potential at node 43. The node 43 has a strong capacitance, indicated at 45. This strong capacitance 45 may be unpredictable until the circuit is constructed, but is believed to stabilize the potential from the charge pump and, in effect, function as an integral part of the charge pump circuit.

FIG. 3 shows a prior art charge pump 51. As can be seen, the charge pump consists of an oscillator 53, which provides its output to a capacitor 55 and to a diode 57. The output of the oscillator is also connected to a clamp circuit 61, which functions to provide current to an output node 63.

The inventive circuit, shown at FIGS. 4 and 5, uses two clamp circuits 71, 72. This increases the efficiency of the charge pump and thereby provides a higher po-

tential with less power consumption. An oscillator 75 provides its output to first and second capacitors 81, 82. The clamp circuits 71, 72 are connected across the capacitors 81, 82.

The oscillator 75 is a ring oscillator which can be metal mask adjusted to increase or decrease frequency.

Instead of diode 57 (FIG. 3), an output transistor 85 is connected between node 87 of capacitors 81 and a circuit output 89 node. The circuit output is an elevated potential current source, and is identified as  $V_{CCW}$ . The combination of clamp circuit 72 and capacitor 82 is used to control the output of the charge pump.

Both clamp circuits 71, 72 turn on and off at the same time, but the connection of clamp circuit 72 across capacitor 82 and in series with the output transistor has the result that the operation of the second clamp circuit 72 causes the output transistor 85 to conduct when potential at the node 87 is at a high potential. The rising edge of the oscillator 75 couples a high voltage through the capacitors 81, 82 which shuts the clamps 71, 72 off and allows the nodes 87, 89 to go high. The falling edge of the output of the oscillator 75 couples a drop in potential through the capacitors 81, 82, at which point, the clamps 71, 72 turn on, preventing the nodes 87, 89 from going low.

The line capacitance at the output and the capacitance of the load, represented as 91, 92 cooperate with the switched output of capacitor 81 in order to provide a boosted potential output to the load (at 92). A decoupling capacitor 93 further cooperates with the charge pump in order to provide a steady boosted output.

An overvoltage shutoff circuit 95 is provided in order to prevent the potential at the load from exceeding a predetermined value. The overvoltage shutoff circuit 95 senses a high voltage on the output node 89. When that level goes above a certain threshold, the shutoff circuit causes the oscillator 75 to stop oscillating. After enough charge has leaked off, the pumped potential at node 89 will eventually drop after supplying the row lines and/or iso devices with charge. The overvoltage shutoff circuit 95 will then turn on the oscillator 75 and allow the oscillator 75 to run again.

In the preferred embodiment, the overvoltage shutoff circuit 95 provides an ENABLE output to the oscillator 75. The connection of the overvoltage shutoff circuit 95 to the oscillator 75 is configured as a NAND gate, thereby disabling the oscillator when the ENABLE output goes low.

On the other hand, if the potential provided by the charge pump is inadequate, a diode connected transistor 97 is used to effectively bypass the charge pump. This transistor 97 is an n channel device connected to a supply voltage node  $V_{CC}$ . The transistor 97 will conduct from  $V_{CC}$  to node 89 as long as  $V_{CCW} < (V_{CC} - V_T)$ . It is off whenever  $V_{CCW} > (V_{CC} - V_T)$ . This portion of the circuit also helps charge up  $V_{CCW}$  on power up.

We claim:

1. In a semiconductor circuit device having a signal generating source, at least one signal line which is precharged to operating levels, a signal level voltage source providing current at a signal level potential, a circuit connected to the signal line which accepts an elevated potential above a potential of the signal level voltage source, and a precharge circuit which precharges the signal line, the precharge circuit comprising:

(a) an oscillator receiving current from the signal level voltage source and providing an oscillating output;

(b) a capacitor connected between the oscillator and a first node;

(c) a first switching circuit connected in parallel with the capacitor and providing a timed output in response to the oscillating output;

(d) a second switching circuit connected in series with said capacitor, between said capacitor at the first node and an output node;

(e) a third switching circuit controlling the second switching circuit in a timed sequence with respect to said timed output; and

a decoupling capacitor connected to the output node, the decoupling capacitor providing a storage capacity sufficient to maintain said elevated potential at a potential above the signal level potential during a substantial portion of an operating cycle of the semiconductor circuit device.

2. The semiconductor device as described in claim 1, further comprising:

(a) the first switching circuit including an output transistor having a source and drain connection in said series connection between the first node and the output node; and

(b) a third switching circuit, the third switching circuit controlling the second switching circuit by gating the output transistor.

3. The semiconductor device as described in claim 1, further comprising:

a second capacitor connected in parallel with the third switching circuit.

4. The semiconductor device as described in claim 1, further comprising:

a potential maintenance transistor connected to conduct from the signal level voltage source at times when potential at the output node falls below a predetermined potential with respect to the potential of the output node and to present an open circuit when potential at the output node is greater than the potential of the signal level voltage source.

5. The semiconductor device as described in claim 4, further comprising:

the potential maintenance transistor having a source and drain connection in a series connection between the signal level voltage source and the output node, and the potential maintenance transistor being connected with its gate to the signal level voltage source

6. The semiconductor device as described in claim 1, further comprising:

(a) means to maintain the output node at a predetermined minimum potential by conducting current from the signal level voltage source; and

(b) a potential limiting circuit responsive to potential at the output node, the potential limiting circuit attenuating the output of the precharge circuit to limit the potential at the output node.

7. In a semiconductor circuit device having a signal generating source, at least one signal line which is precharged to operating levels, a signal level voltage source providing current at a signal level potential, a circuit connected to the signal line which accepts an elevated potential above a potential of the signal level voltage source, and a precharge circuit which precharges the signal line, the precharge circuit comprising:



- (a) an oscillator receiving current from the signal level voltage source and providing an oscillating output;
  - (b) a first capacitor connected between the oscillator and a first node;
  - (c) an output switching circuit connected in series with the first capacitor, between the first capacitor at the first node and an output node, the output switching circuit including an output transistor having a source and drain connection in said series connection between the first node and the output node;
  - (d) a first clamp circuit connected in parallel with the first capacitor and providing a timed output in response to the oscillating output; and
  - (e) a second clamp circuit controlling the output switching circuit in a timed sequence with respect to said timed output, the second clamp circuit controlling the output switching circuit by gating the output transistor.
8. The semiconductor device as described in claim 7, further comprising:
- a second capacitor connected in parallel with the second clamp circuit.
9. In a dynamic random access memory array, which includes an array of capacitor cells corresponding to memory address locations, at least one signal line which is precharged to signal sensing levels, a circuit for providing signals corresponding to signal levels in the capacitor cells to the signal line, a precharge circuit which precharges the signal line, an equalization transistor for equalization of the precharge signal levels across the signal line, a signal level voltage source, the circuit device comprising:
- (a) an oscillator receiving current from the signal level voltage source and providing an oscillating output;
  - (b) a capacitor connected between the oscillator and a first node;
  - (c) an output switching circuit connected in series with said capacitor, between said capacitor at the first node and an output node, the output switching circuit including an output transistor having a source and drain connection in said series connection between the first node and the output node;
  - (d) a first clamp circuit connected in parallel with said capacitor and providing a timed output in response to the oscillating output; and
  - (e) a second clamp circuit controlling the output switching circuit in a timed sequence with respect to said timed output, the second clamp circuit con-

trolling the output switching circuit by gating the output transistor.

10. The dynamic random access memory array described in claim 9, further comprising:

- a second capacitor connected in parallel with the second clamp circuit.

11. In a random access memory array, which includes an array of capacitor cells corresponding to memory address locations, at least one signal line which is precharged to signal sensing levels, a circuit for providing signals corresponding to signal levels in the capacitor cells to the signal line, a precharge circuit which precharges the signal line, an equalization transistor for equalization of the precharge signal levels across the signal lines, a signal level voltage source, the circuit device comprising:

- (a) the precharge circuit including a ring oscillator providing an elevated potential output at an output node, whereby isolation devices on the memory array and word lines are supplied with current by the precharge circuit; and

means to maintain the output node at a predetermined minimum potential by conducting current from the signal level voltage source, said means including a potential maintenance transistor connected to conduct from the signal level voltage source at times when potential at the output node falls below a predetermined potential with respect to the potential of the output node and to present an open circuit when potential at the output node is greater than the potential of the signal level voltage source, the potential maintenance transistor having a source and drain connection in a series connection between the signal level voltage source and the output node, and the potential maintenance transistor being connected with its gate to the signal level voltage source.

12. The random access memory array described in claim 11, further comprising:

- a potential limiting circuit responsive to potential at an output node, the potential limiting circuit attenuating the output of the precharge circuit to limit the potential at the output node.

13. The random access memory array described in claim 11, further comprising:

- a potential limiting circuit responsive to potential at an output node, the potential limiting circuit attenuating the output of the precharge circuit to limit the potential at the output node.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. 5,038,325  
DATED August 6, 1991  
INVENTOR(S) Douglas et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On title page, item [21] "487,773" should read --498,773--  
column 4, line 15, "28-28" should read --21-28--

Signed and Sealed this

Twenty-second Day of March, 1994

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

**United States Patent** [19]  
**Takagi et al.**

[11] **Patent Number:** 5,068,626  
[45] **Date of Patent:** Nov. 26, 1991

[54] **CHARGE PUMP CIRCUIT**

[75] **Inventors:** Kotaro Takagi, Tokyo; Satoshi Yokoya, Kanagawa, both of Japan

[73] **Assignee:** Sony Corporation, Tokyo, Japan

[21] **Appl. No.:** 538,187

[22] **Filed:** Jun. 13, 1990

[30] **Foreign Application Priority Data**

Jun. 27, 1989 [JP] Japan ..... 1-165113

[51] **Int. Cl.:** ..... H03L 7/00

[52] **U.S. Cl.:** ..... 331/17; 331/25

[58] **Field of Search** ..... 331/17, 25; 328/151, 328/155, 133; 307/511

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,636,748 1/1987 Latham, II ..... 331/17

4,668,918 5/1987 Adams ..... 331/17 X

**Primary Examiner**—Robert J. Pascal

**Attorney, Agent, or Firm**—Alvin Sinderbrand; William S. Frommer

[57] **ABSTRACT**

A charge pump circuit for charging a capacitor in response to a phase difference between first and second input signals comprises a constant current source for providing a first constant current; a constant current sink for absorbing a second constant current; a circuit for substantially equalizing the magnitudes of the first and second constant currents; and a switching circuit for providing the first constant current and the second constant current flowing in opposed directions to the capacitor through an output terminal of the charge pump circuit in response to the phase difference between the first and second input signals to produce a voltage level across the capacitor corresponding to the phase difference. In a phase locked loop system employing such a charge pump circuit, a phase comparator produces a phase difference signal for controlling the provision of the first and second constant currents by the switching circuit to the capacitor. The capacitor acts as a loop filter supplying the voltage thereacross as a control voltage to a voltage controlled oscillator of the phase locked loop system.

11 Claims, 5 Drawing Sheets

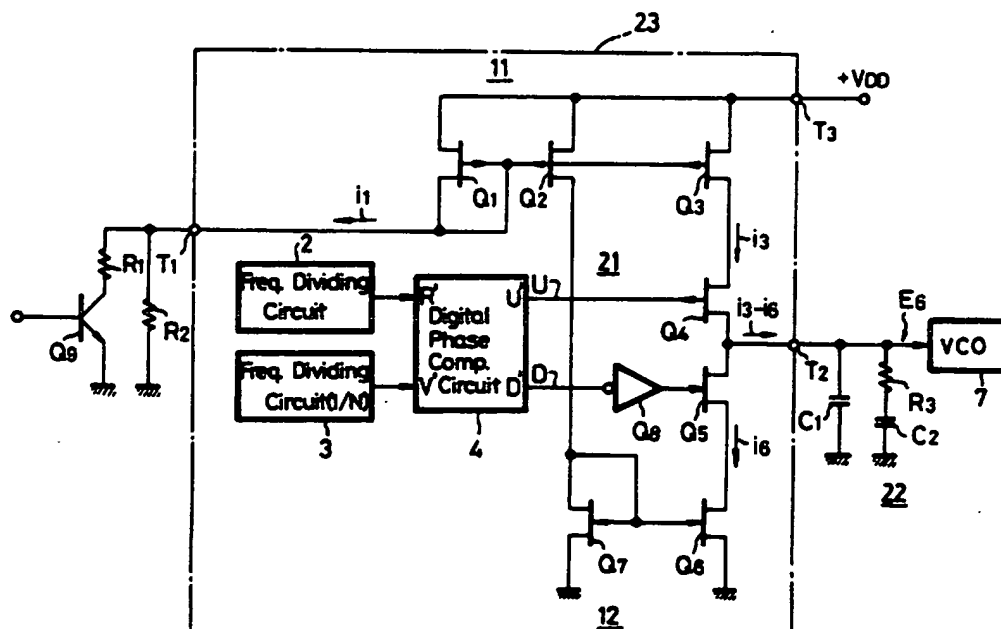


FIG. 1 (PRIOR ART)

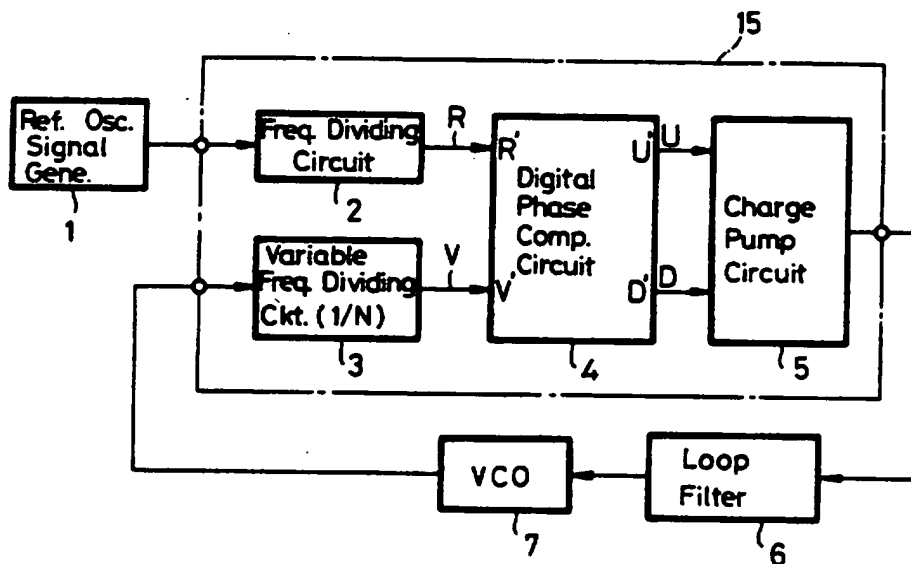


FIG. 2 (PRIOR ART)

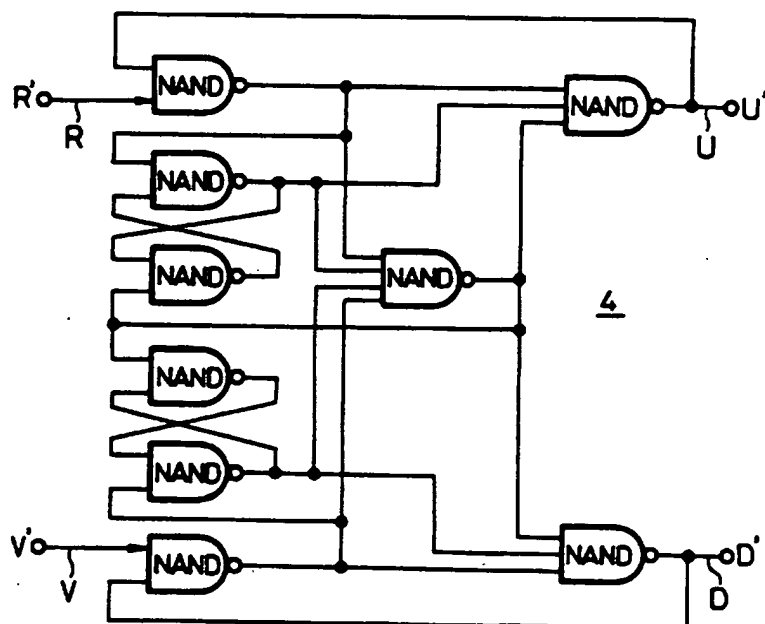


FIG. 3 (PRIOR ART)

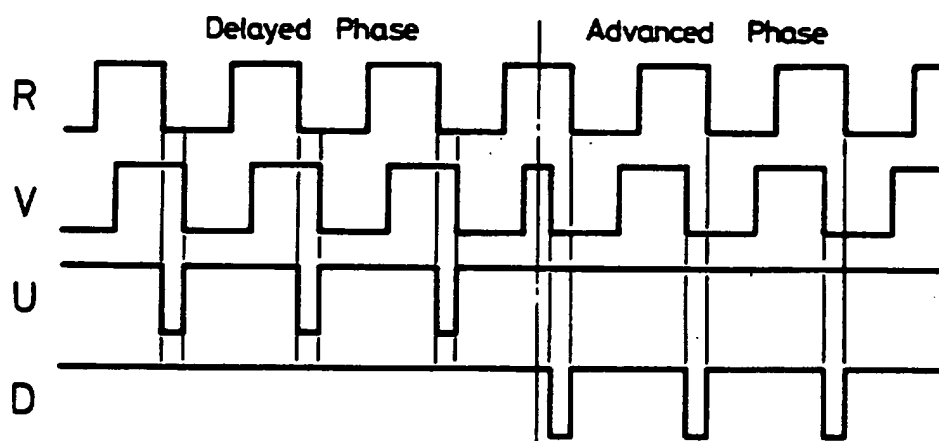
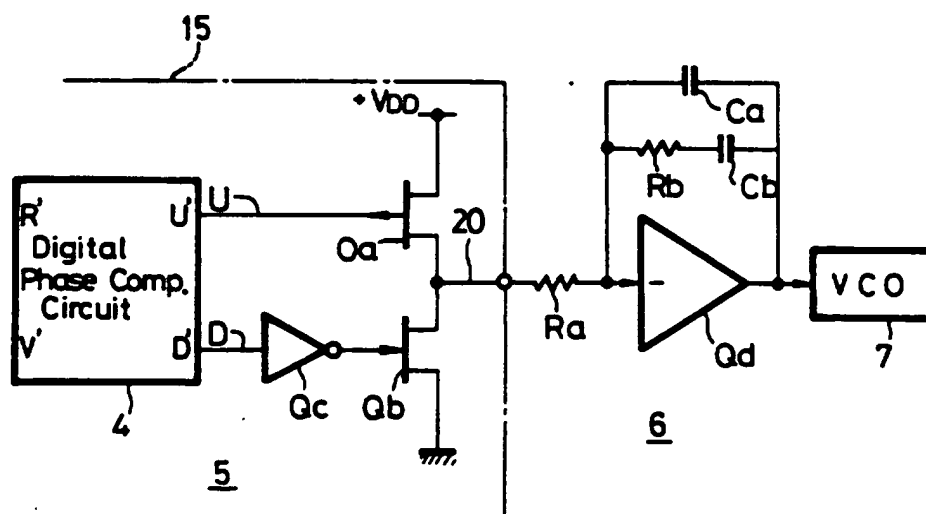
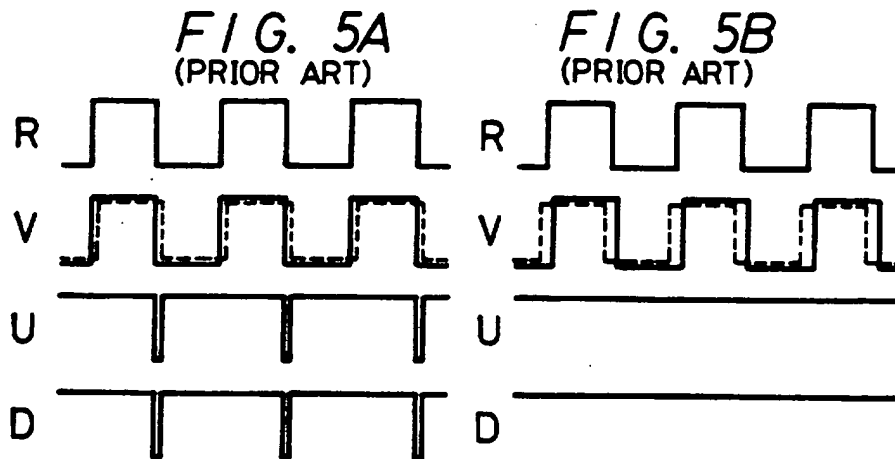


FIG. 4 (PRIOR ART)





**FIG. 6**

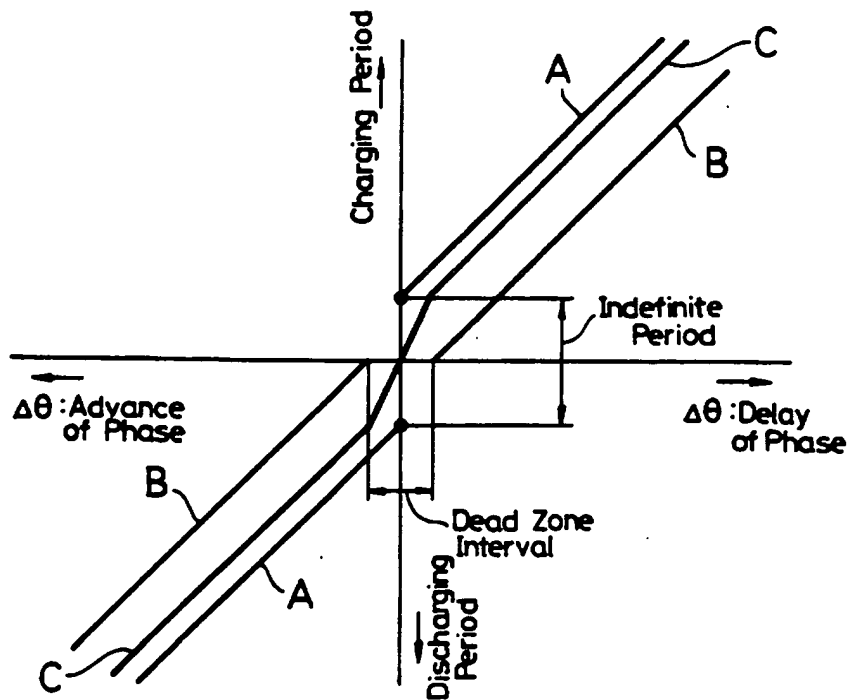


FIG. 7

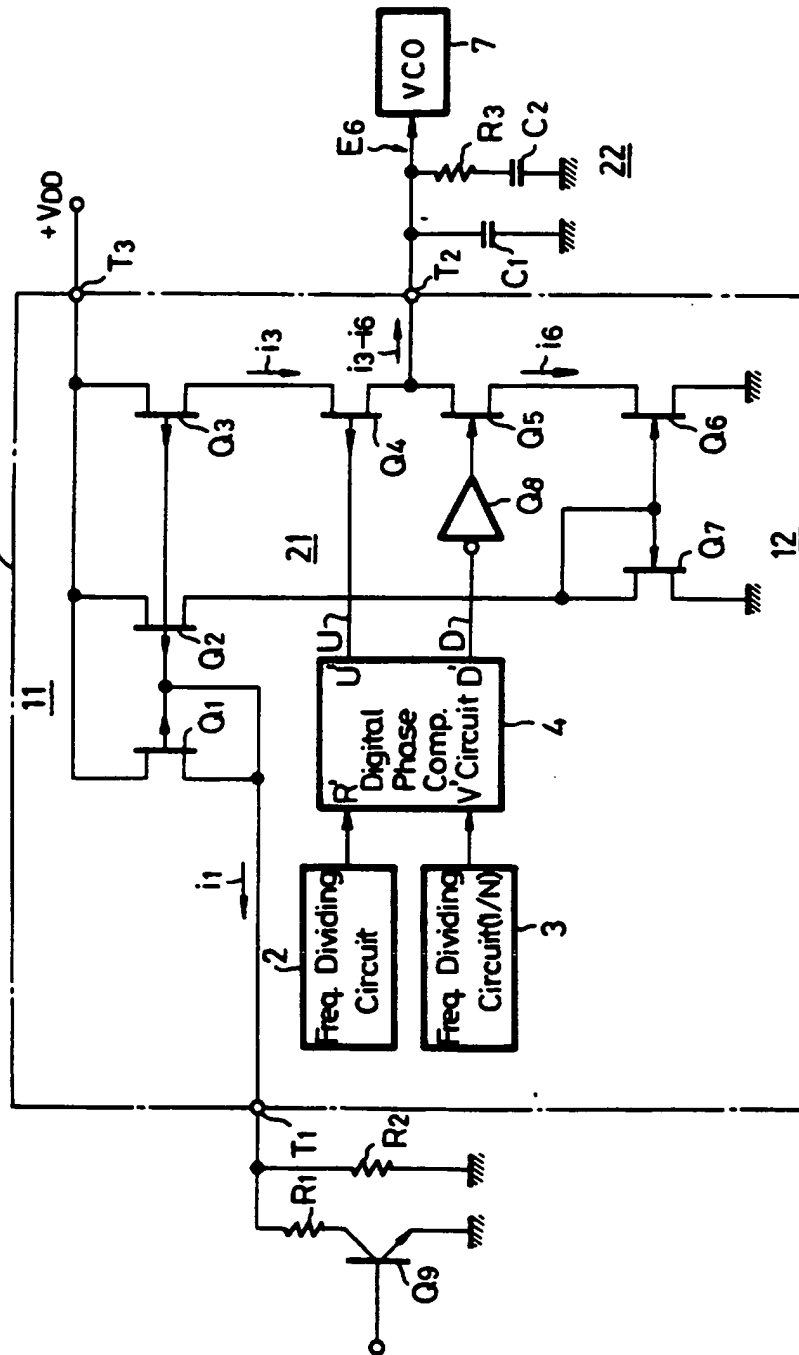
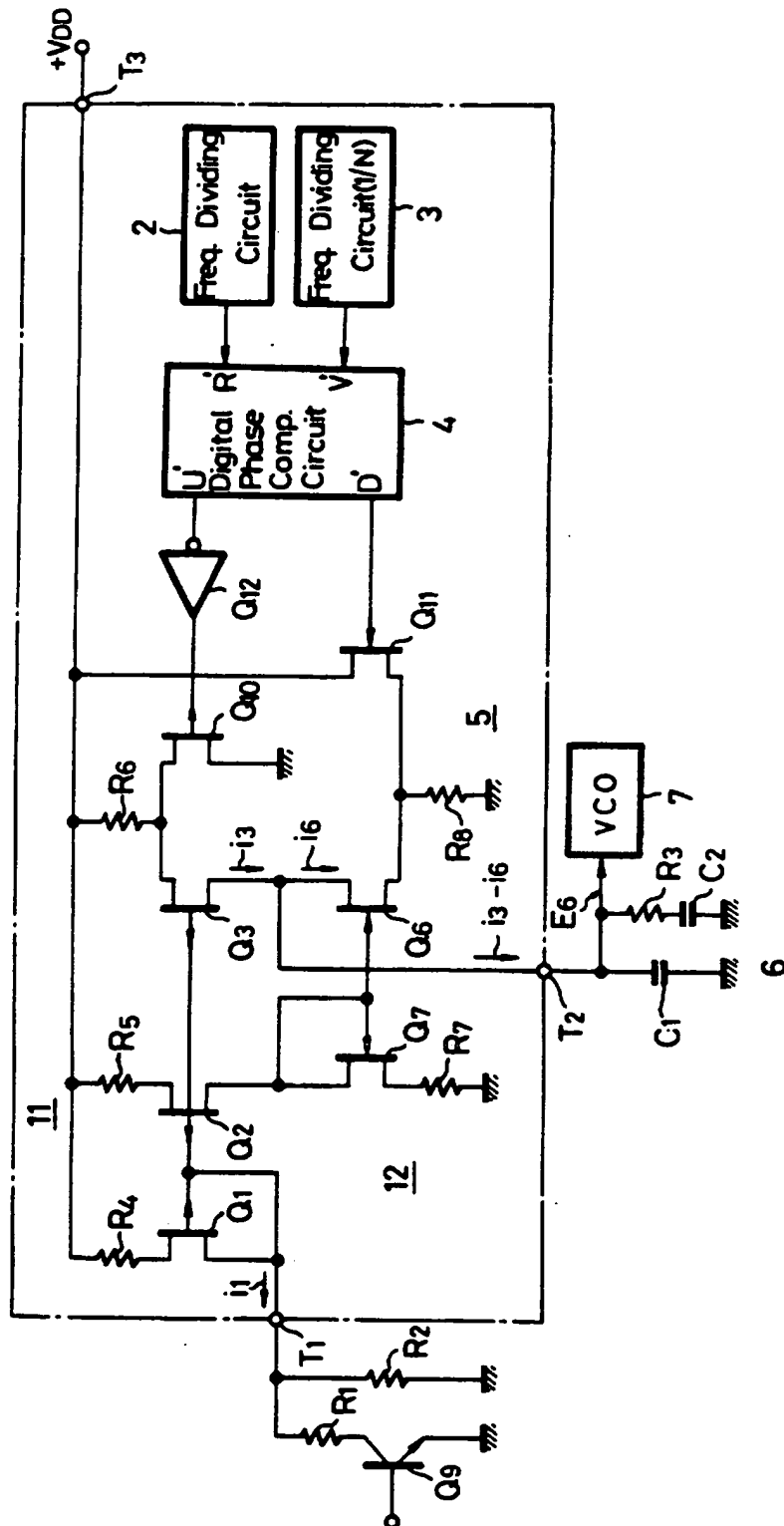


FIG. 8





## CHARGE PUMP CIRCUIT

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present invention generally relates to charge pump circuits, for example, for use in a phase locked loop (PLL) system.

## 2. Description of The Prior Art

FIG. 1 illustrates a conventional PLL utilizing a digital phase comparison circuit 4. A reference oscillation signal is produced by a reference oscillation signal generating circuit 1 and is provided to a frequency-dividing circuit 2, in which it is frequency-divided to provide a frequency-divided signal R at an output terminal of the circuit 2. The frequency-divided signal R has a reference frequency, for example, of 25 kHz. The output terminal of the frequency-dividing circuit 2 is coupled with an input terminal R' of the digital phase comparison circuit 4 to provide the frequency-divided signal R thereto as a first phase comparison signal.

A voltage controlled oscillator (VCO) 7 produces an oscillation signal which it supplies to the input of a variable frequency-dividing circuit 3 simultaneously with the provision of the reference oscillation signal to the frequency-dividing circuit 2. The variable frequency-dividing circuit 3 divides the frequency of the oscillation signal from the VCO 7 by a divisor N to provide a frequency-divided signal V which it supplies to a second input terminal V' of the digital phase comparison circuit 4 as a second phase comparison signal.

With reference to FIG. 2, the digital phase comparison circuit 4 includes nine NAND gates connected as shown therein. With reference also to FIG. 3, the digital phase comparison circuit 4 is operative to provide a first phase difference signal U at a first output terminal U' thereof and a second phase comparison signal D at a second output terminal D' thereof in response to a phase difference between the first and second phase comparison signals R and V received at the input terminals R' and V', respectively. More specifically, when the first phase comparison signal V is delayed in phase with respect to the second phase comparison signal R, as shown in the left side of FIG. 3, the first phase difference signal U changes from a logic "1" state (a high voltage level) to a logic "0" state (a low voltage level) upon a transition of the phase comparison signal R from a logic "1" state to a logic "0" state. The first phase difference signal U thereafter remains in the logic "0" state until the phase comparison signal V subsequently falls from a logic "1" state to a logic "0" state, whereupon the first phase difference signal U rises to a logic "1" state. The second phase difference signal D remains in a logic "1" state so long as the phase of the first phase comparison signal R leads that of the second phase comparison signal V.

However, at such times that the phase of the second phase comparison signal V leads that of the first phase comparison signal R, as shown in the right hand side of FIG. 3, the first phase difference signal U remains in a logic "1" state, while the second phase difference signal D changes from a logic "1" state to a logic "0" state when the second phase comparison signal V falls from a logic "1" state to a logic "0" state and thereafter remains in a logic "0" state until the first comparison signal R also falls from a logic "1" state to a logic "0"

state, whereupon the second phase difference signal D is raised to a logic "1" state.

With reference again to FIG. 1, the first and second phase difference signals U and D are supplied to respective inputs of a charge pump circuit 5. With reference also to FIG. 4, it will be seen that the charge pump circuit 5 includes a p-channel field effect transistor (FET) Qa whose gate is connected to output U' of the digital phase comparison circuit 4 to receive the first phase difference signal U therefrom and whose drain-source circuit is coupled between a source of positive power voltage +H<sub>DD</sub> and an output terminal 20 of the charge pump circuit 5. The charge pump circuit 5 also includes an n-channel FET Qb whose gate electrode is coupled through an inverter Qc with output D of the digital phase comparison circuit 4 to receive the second phase difference signal D therefrom. The source-drain path of the FET Qb is coupled between the output terminal 20 of the charge pump circuit 5 and a circuit ground.

A loop filter 6 includes an operational amplifier Qd having an inverting input terminal coupled through an input resistor Ra with the output terminal 20 of the charge pump circuit 5. An output terminal of the operational amplifier Qd is coupled with a control voltage terminal of the VCO 7. A first feedback capacitor Ca is coupled between the output terminal of the operational amplifier Qd and its inverting input terminal. A second feedback capacitor Cb has a first terminal connected with the output terminal of the operational amplifier Qd and a second terminal connected with a first terminal of a feedback resistor Rb having a second terminal connected with the inverting input terminal of the operational amplifier Qd. In this manner, the loop filter 6 takes the form of a mirror integrating circuit.

At such times that the phase of the first phase comparison signal R leads the phase of the second phase comparison signal V, the voltage applied to the gate of the FET Qa is periodically brought low by the first phase difference signal U to turn ON the FET Qa. Since the second phase difference signal D remains at a logic "1" state (high voltage) the gate of the FET Qb remains essentially at ground potential, so that the FET Qb is OFF. Accordingly, while the phase of the first phase comparison signal R leads that of the second phase comparison signal V, the loop filter 6 is charged by the power source voltage +H<sub>DD</sub> whenever the first phase difference signal U goes low in a logic "0" state. Conversely, at such times that the phase of the second phase comparison signal V leads that of the first phase comparison signal R, the FET Qa is maintained in an OFF state by the high voltage level of the first phase difference signal U in the logic "1" state, while the FET Qb is turned ON periodically by the high voltage level at the output of the inverter Qc produced at such times that the second phase difference signal D is in a logic "0" state so that the loop filter 6 is then discharged through the FET Qb. However, when both of the first and second phase difference signals U and D are in a logic "1" state, FETs Qa and Qb are both turned OFF so that the loop filter 6 is neither charged nor discharged. Accordingly, the loop filter 6 produces a dc voltage level at the output terminal thereof corresponding with the phase difference between the first and second phase difference signals U and D.

As noted above, the dc voltage level produced at the output of the loop filter 6 is applied to the control voltage terminal of the VCO 7 so that, in a stationary state,

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the VCO 7 produces an oscillation signal whose frequency is N times the frequency of the phase comparison signal R. The frequency dividing circuit 2, the variable frequency-dividing circuit 3, the digital phase comparison circuit 4 and the charge pump circuit 5 may be fabricated as a single chip integrated circuit 15 (see "Practical Use Guide to PLL", pages 125-127, dated Aug. 30, 1974, by Seibundoshinkosha and Japanese Laid-Open Patent No. 51-139758 published Dec. 2, 1976).

With reference again to FIG. 2, the phase comparison circuit 4 ideally provides the first and second phase difference signals U and D in a logic "1" state whenever the phase comparison signals R and V are in phase. However, due to the inherent propagation delays of the circuit elements comprising the phase comparison circuit 4, upon the simultaneous high to low logic state transitions of the in-phase first and second phase comparison signals R and V (as shown by the solid line waveforms in FIG. 5A) both the first and second phase difference signals U and D are then brought to a logic "0" state for a brief but significant period of time. When the second phase comparison signal V becomes delayed in phase with respect to the first phase comparison signal R by a very small amount as shown by the dashed line in FIG. 5A, the first and second phase difference signals U and D are suddenly placed in logic states similar to those illustrated in the left-hand side of FIG. 3, although a brief interval may exist during which both signals are simultaneously in a logic "0" state. Alternatively, where the second phase comparison signal V becomes advanced in phase by a very small amount with respect to the first phase comparison signal R the first and second phase difference signals U and D are suddenly placed in states similar to those illustrated in the right-hand side of FIG. 3. The resulting relationship between the phase difference  $\Delta\theta$ , (that is, the phase difference of the second phase comparison signal V with respect to the first phase comparison signal R) and the charging and discharging periods controlled by the first and second phase difference signals U and D, is illustrated by the line A in FIG. 6. In FIG. 6, the axis of ordinates represents the relative charging and discharging periods of the loop filter 6, while the axis of abscissas represents the relative phase delay or advance of the second phase comparison signal V with respect to the first phase comparison signal R. It will be seen from FIG. 6 that an indefinite charging period exists where the signals R and V are either in phase or only slightly out of phase so that the operation of the PLL is unstable under such conditions.

In order to overcome the foregoing problem, it has been proposed that a dead zone interval be introduced for phase differences  $\Delta\theta$  which do not exceed a predetermined magnitude, so that, when the first and second phase comparison signals R and V are in phase, the first and second phase difference signals U and D are reliably maintained in a logic "1" state. Accordingly, the combination of the operational delay times of the NAND gates and other circuit elements forming the phase comparison circuit 4 are changed so that the relationship of the charging and discharging periods to the phase difference  $\Delta\theta$  is instead expressed by the broken line b of FIG. 6. That is, even when the second phase comparison signal V is phase delayed with respect to the first phase comparison signal R by a relatively small amount (for example, as shown by the solid line waveform illustrated in FIG. 5B) or when the sec-

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ond phase comparison signal V is advanced in phase with respect to the first phase comparison signal R (for example, as shown by the dashed line waveform in FIG. 5B), the first and second phase difference signals U and D are maintained in a logic "1" state. Accordingly, unless the phase difference  $\Delta\theta$  exceeds a minimum predetermined magnitude defining the extremes of the dead zone interval, the charge pump circuit 5 will neither charge nor discharge the loop filter 6.

Where the phase comparison circuit 4 and the charge pump circuit 5 are constructed as above so that an indefinite charging period exists (as represented by the discontinuous line A in FIG. 6) or where a dead zone interval is provided (as shown by the broken line B of FIG. 6), the phase locked loop exhibits a different natural frequency  $\omega_n$  and damping coefficient  $\xi$  when operating in a phase locked condition than while operating in an unlocked condition. Accordingly, the natural frequency and damping coefficient of the phase-locked loop cannot be optimized and, consequently, the purity of the oscillation frequency of the VCO 7 deteriorates. The foregoing results in the deterioration of the carrier-to-noise ratio where, for example, the output of the VCO 7 is utilized to provide a local oscillation signal for a radio receiver. Moreover, where the conventional phase locked loop as described above, is utilized for FM modulation, the modulated output signal exhibits distortion as a consequence of deterioration in the purity of the oscillation frequency.

A further disadvantage inherent in the conventional phase locked loop described above is an unavoidable dependency between the loop gain and the cut-off frequency of the loop filter 6. That is, although the loop gain can be adjusted by selecting the ratio between the resistance values of the resistors  $R_a$  and  $R_b$ , this likewise changes the cut-off frequency of the loop filter 6. The design of the conventional phase locked loop, therefore, is inherently inflexible. In addition, the conventional phase locked loop requires the use of the operational amplifier  $Q_d$  for constructing the loop filter 6, resulting in a poor space factor and increased cost.

#### OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide an improved charge pump circuit and an improved phase locked loop system which avoid the above mentioned disadvantages and problems associated with the prior art.

More specifically, it is an object of the present invention to provide a charge pump circuit for a phase locked loop which is capable of more reliably charging and discharging a loop filter thereof in proportion to a phase difference which is arbitrarily small.

Another object of the present invention is to provide a charge pump circuit capable of reducing the lock-up time of a phase locked loop system to thereby provide stable operation.

Still another object of the present invention is to provide a phase locked loop system employing a charge pump circuit for charging a loop filter wherein the cut-off frequency of the loop filter is independent of the loop gain of the phase locked loop system, and vice versa.

Yet another object of the present invention is to provide a phase locked loop system which has an advantageous space factor and which can be made inexpensively.

In accordance with an aspect of the present invention, a charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals comprises constant current source means for providing a first constant current; constant current sinking means for absorbing a second constant current; means for substantially equalizing the magnitudes of the first constant current provided by the constant current source means and the second constant current absorbed by the constant current sinking means; and switching means for providing the first constant current and the second constant current flowing in opposed directions to said capacitive means through an output terminal of the charge pump circuit in response to the phase difference between the first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to the phase difference.

In accordance with another aspect of this invention, a phase locked loop system comprises means for receiving a reference signal; voltage controlled oscillator means for providing a phase adjustable output signal controllable by a control voltage applied at a control terminal thereof; means for producing a phase difference signal representative of a phase difference between the reference signal and the phase adjustable output signal of the voltage controlled oscillator means; means for producing the control voltage including constant current source means for providing a first constant current, constant current sinking means for absorbing a second constant current, means for substantially equalizing the magnitudes of the first current provided by the constant current source means and the second constant current absorbed by the constant current sinking means, capacitive means for producing the control voltage, and switching means for providing the first constant current and the second constant current flowing in opposed directions to the capacitive means in response to the phase difference signal for selectively charging and discharging the capacitive means to produce the control voltage corresponding to the phase difference signal; and means for applying the control voltage produced by the capacitive means to the control terminal of the voltage control oscillator means.

These, and other objects, features and advantages of the invention, will be apparent in the following detailed description of certain illustrative embodiments thereof which is to be read in conjunction with the accompanying drawings forming a part hereof, and wherein corresponding parts and components are identified by the same reference numerals in the several views of drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an exemplary prior art phase locked loop circuit utilizing a digital phase comparison circuit;

FIG. 2 is a schematic diagram of a digital phase comparison circuit incorporated in the phase locked loop circuit of FIG. 1;

FIG. 3 is a waveform diagram of frequency-divided, phase comparison signals input to the phase comparison circuit of FIG. 2 and phase difference signals output thereby to which reference is made in explaining the operation thereof;

FIG. 4 is a partially schematic and partially block diagram illustrating a charge pump circuit and a loop

filter incorporated in the phase locked loop circuit of FIG. 1;

FIGS. 5A and 5B are waveform diagrams of frequency-divided, phase comparison signals input, respectively, to the phase comparison circuit of FIG. 2 and to a modified form thereof, and output phase difference signals therefrom, to which further reference is made in explaining the operation thereof;

FIG. 6 is a graph of certain operational characteristics of prior art phase locked loop circuits, including the phase locked loop circuit of FIG. 1, and of the phase locked loop system of the present invention;

FIG. 7 is a partially block and partially schematic circuit diagram illustrating a first embodiment of a charge pump circuit and phase locked loop system in accordance with the present invention; and

FIG. 8 is a partially schematic and partially block diagram illustrating a second embodiment of a charge pump circuit and phase locked loop system in accordance with the present invention.

#### DETAILED DESCRIPTION OF THE CERTAIN PREFERRED EMBODIMENTS

With reference to FIG. 7, a phase locked loop system in accordance with a first embodiment of the present invention is illustrated therein. Elements of the FIG. 7 embodiment corresponding to elements shown in FIG. 1 bear the same reference numerals.

In a charge pump circuit 21 of the FIG. 7 embodiment, the source-drain paths of p-channel FETs  $Q_3$  and  $Q_4$  are connected in series between a positive voltage power source terminal  $T_3$  and an output terminal  $T_2$  of the charge pump circuit 21. Charge pump circuit 21 also includes n-channel FETs  $Q_5$  and  $Q_6$  whose drain-source paths are connected in series between the output terminal  $T_2$  and circuit ground. The FET  $Q_3$  is a current source transistor which supplies a charging current  $i_3$  of constant magnitude in a first direction toward the output terminal  $T_2$  for charging a loop filter 22 described in greater detail hereinbelow. The FET  $Q_6$  is a current sink transistor which draws a discharging current  $i_6$  of constant magnitude in a second direction from the output terminal  $T_2$  to circuit ground for discharging the loop filter 22. The FET  $Q_4$  acts as a first switching transistor for controlling the application of the charging current  $i_3$  supplied by the current source transistor  $Q_3$ , while the FET  $Q_5$  serves as a second switching transistor for controlling the flow of the discharging current  $i_6$  from the output terminal  $T_2$  to ground through the current sink transistor  $Q_6$ .

A current mirror circuit 11 includes a p-channel FET  $Q_1$  at an input side thereof, the FET  $Q_1$  having a source electrode connected with terminal  $T_3$  and drain and gate electrodes both connected to a control terminal  $T_1$  of the charge pump circuit 21. The FET  $Q_3$  is arranged at an output side of the current mirror circuit 11 such that its gate electrode is coupled with that of the FET  $Q_1$ . A further p-channel FET  $Q_2$  is also connected at the output side of the current mirror circuit 11 such that its gate electrode is coupled with that of the FET  $Q_1$  and its source electrode is connected with that of FET  $Q_1$  to the terminal  $T_3$ .

A second current mirror circuit 12 includes an n-channel FET  $Q_7$  whose source electrode is connected to circuit ground and whose drain and gate electrodes are connected with the drain electrode of the FET  $Q_2$ . The current sink transistor  $Q_6$  forms the output side of the

current mirror circuit 12 such that its gate electrode is connected with that of the FET  $Q_7$ .

The output terminal  $U'$  of the digital phase comparison circuit 4 is connected to the gate electrode of the first switching transistor  $Q_4$  and the output terminal  $D'$  of the digital phase comparison circuit 4 is coupled through an inverter  $Q_5$  to the gate electrode of the second switching transistor  $Q_5$ . The digital phase comparison circuit 4 and the charge pump circuit 21 together with the frequency-dividing circuits 2 and 3, are fabricated as an integrated circuit 23, as indicated in FIG. 7.

A resistor  $R_2$  is connected between the control terminal  $T_1$  and circuit ground. A resistor  $R_1$  has a first terminal connected to the control terminal  $T_1$  and a second terminal connected with the collector of a non transistor  $Q_9$  whose emitter is connected to circuit ground.

The loop filter 22 includes a capacitor  $C_1$  connected between the output terminal  $T_2$  and circuit ground. The loop filter 22 further includes a resistor  $R_3$  having a first terminal connected with the output terminal  $T_2$  of the charge pump circuit 21, and a capacitor  $C_2$  having a first terminal connected with a second terminal of the resistor  $R_3$  and a second terminal connected with the circuit ground. The loop filter 22 produces a voltage  $E_6$  at the terminal  $T_2$  which the loop filter 22 supplies to the control terminal of the VCO 7.

The digital phase comparison circuit 4 receives the first and second phase comparison signals  $R$  and  $V$  as inputs and produces the first and second phase difference signals  $U$  and  $D$  as outputs, as discussed above in connection with FIGS. 3 and 5A. Accordingly, the relationship of the first and second phase difference signals  $U$  and  $D$  produced by the phase comparison circuit 4 to the phase difference between the first and second phase comparison signals  $R$  and  $V$  provided as inputs thereto is expressed essentially by the discontinuous line A of FIG. 6.

In operation, the current  $i_1$  flowing in the FET  $Q_1$  has a constant magnitude depending on a signal level applied to the base of the transistor  $Q_9$ , as discussed more fully hereinbelow. Since the FETs  $Q_1$  and  $Q_3$  form respective input and output portions of the current mirror circuit 11, the magnitude of the current  $i_3$  flowing in the source-drain path of the FET  $Q_3$  will be equal to that of the current  $i_1$  of the FET  $Q_1$ . Since the FETs  $Q_1$  and  $Q_2$  likewise form respective input and output portions of the current mirror circuit 11, the current flowing in the source-drain path of the FET  $Q_2$  is also equal in magnitude to that of the current  $i_1$  and, therefore, to that of the current  $i_3$ . Since the FETs  $Q_7$  and  $Q_6$  constitute input and output portions, respectively, of the current mirror circuit 12, the current  $i_6$  flowing in the source-drain path of the FET  $Q_6$  is equal to the current flowing in the source-drain path of the FET  $Q_7$ . Since the current flowing in the source-drain path of the FET  $Q_7$  is equal to that flowing in the source-drain path of the FET  $Q_2$  and, therefore, is also equal to that of  $i_3$ , it is apparent that the magnitudes of the currents  $i_3$  and  $i_6$ , when permitted to flow through the switching transistors  $Q_4$  and  $Q_5$ , respectively, will have the same magnitude. Accordingly, the charge pump circuit 21 forces the magnitudes of the currents  $i_3$  and  $i_6$  to be equal that of the reference current  $i_1$  whenever the respective switching transistors  $Q_4$  and  $Q_5$  are turned ON.

In operation, where the phase comparison signal  $V$  is phase delayed with respect to the phase comparison signal  $R$  such that the phase difference signal  $U$  is in a

logic "0" state and the phase difference signal  $D$  is in a logic "1" state, the switching transistor  $Q_4$  is turned ON and the switching transistor  $Q_5$  is turned OFF. Accordingly, the constant current  $i_3$  is then provided to the loop filter 22 to charge the capacitors  $C_1$  and  $C_2$  to increase the level of the output voltage  $E_6$  of the loop filter 22. Consequently, the phase (that is, the oscillation frequency) of the oscillation signal produced by the VCO 7 is advanced. Since the capacitors  $C_1$  and  $C_2$  are charged by a current  $i_3$  having a constant magnitude, the voltage level  $E_6$  is linearly increased thereby.

When the second phase comparison signal  $V$  is phase advanced with respect to the first phase comparison signal  $R$  so that the first phase difference signal  $U$  is in a logic "1" state while the second phase difference signal  $D$  is in a logic "0" state, the first switching transistor  $Q_4$  is then turned OFF while the second switching transistor  $Q_5$  is turned ON such that the capacitors  $C_1$  and  $C_2$  are thereby discharged by the constant current  $i_6$ . Consequently, this simultaneously decreases the level of the output voltage  $E_6$  of the loop filter 22 in a linear fashion, such that the phase of the oscillation signal produced by the VCO 7 is delayed.

Furthermore, at such times that the first and second phase comparison signals  $R$  and  $V$  are in phase such that the first  $U$  and second phase difference signals  $U$  and  $D$  are in a logic "1" state, the first and second switching transistors  $Q_4$  and  $Q_5$  are both turned OFF, so that neither the current  $i_3$  nor the current  $i_6$  is permitted to flow to the output terminal  $T_2$ . Consequently, the capacitors  $C_1$  and  $C_2$  are neither charged or discharged and the output voltage level  $E_6$  is maintained at a constant value such that the phase of the oscillation signal produced by the VCO 7 is likewise unchanged.

As noted above, where the phase comparison signals  $R$  and  $V$  are in phase, during a short period of time commencing from the trailing edges of the phase comparison signals  $R$  and  $V$ , both of the first and second phase difference signals  $U$  and  $D$  switch to a logic "0" state before returning to a logic "1" state at the end of the short time period. Since, however, the magnitudes of the charging and discharging currents  $i_3$  and  $i_6$ , respectively, are equal, they add to zero when both of the first and second switching transistors  $Q_4$  and  $Q_5$  are turned ON by the logic "0" levels of the first and second phase difference signals  $U$  and  $D$ . Accordingly, the capacitors  $C_1$  and  $C_2$  of the loop filter 22 are neither charged nor discharged at such time and the level of the output voltage  $E_6$  is maintained at a constant value so that the phase of the oscillation signal produced by the VCO 7 is unchanged.

With reference again to FIG. 6, the continuous line C indicates the relationship of the phase difference  $\Delta\theta$  between the phase comparison signals  $V$  and  $R$  input to the phase comparison circuit 4 and the charging and discharging periods produced in response thereto by the charge pump circuit 21. It will be seen therefrom that a linear relationship exists between the phase difference  $\Delta\theta$  and the resulting charging and discharging periods. Since the charge pump circuit 21 supplies charging and discharging currents  $i_3$  and  $i_6$ , respectively, which have a constant magnitude, it will be appreciated that the FIG. 7 embodiment provides a linear relationship between the phase difference  $\Delta\theta$  and the control voltage  $E_6$  even at arbitrarily small phase differences. Accordingly, the phase of the oscillation signal produced by the VCO 7 varies linearly with the

phase difference  $\Delta\theta$  between the first and second phase comparison signals R and V.

When the transistor  $Q_9$  is turned OFF, the reference current  $i_1$  flows through the resistor  $R_2$  only, such that the reference current  $i_1$  is maintained at a relatively low value by the relatively high impedance presented by the resistor  $R_2$  alone. When however, the transistor  $Q_9$  is turned ON, the current  $i_1$  is able to flow through the parallel combination of resistors  $R_1$  and  $R_2$ , such that the magnitude of the current  $i_1$  flowing through the FET  $Q_1$  is increased. Since the currents  $i_3$  and  $i_6$  are equal in magnitude to the reference current  $i_1$ , it will be seen that a means is provided for adjusting the magnitudes of the constant currents  $i_3$  and  $i_6$  by controlling the ON-OFF states of the transistor  $Q_9$ . Since the output voltage  $E_6$  of the loop filter 22 varies linearly with the magnitudes of the currents  $i_3$  and  $i_6$ , it will be seen that, by adjusting the magnitudes of the constant currents  $i_3$  and  $i_6$  by selecting the ON-OFF states of the transistor  $Q_9$ , the loop gain of the phase locked loop is thereby adjusted. It will also be appreciated that the lock-up time of the phase locked loop can be selectively reduced by increasing the loop gain in the foregoing manner. Since the cut-off frequency of the loop filter 22 is determined only by the capacitors  $C_1$  and  $C_2$  and the resistor  $R_3$ , whose values are unaffected by the magnitudes of the charging and the discharging currents  $i_3$  and  $i_6$ , the cut-off frequency of the loop filter 22 is unaffected by adjusting the loop gain in the foregoing manner. It will also be apparent that the loop gain can be made independent of the cut-off frequency.

With reference now to FIG. 8, a second embodiment of a phase locked loop system in accordance with the present invention is illustrated therein. Elements of the FIG. 8 embodiment corresponding to elements shown in the foregoing figures bear the same reference numerals.

In the FIG. 8 embodiment, the first and second current source transistors  $Q_3$  and  $Q_6$  are coupled directly to the output terminal  $T_2$ , while the source-drain path of the current source transistor  $Q_3$  is coupled to the positive voltage power source terminal  $T_3$  through a resistor  $R_4$ , while the source-drain path of the current sink transistor  $Q_6$  is coupled to circuit ground through a resistor  $R_5$ . The source of the FET  $Q_1$  is coupled to the positive voltage power supply terminal  $T_3$  through a resistor  $R_4$ , while the source of the FET  $Q_2$  is coupled to the positive voltage power source  $T_3$  through a resistor  $R_5$ . The source of the FET  $Q_7$  is coupled to circuit ground through a resistor  $R_7$ . A p-channel bypass switching FET  $Q_{10}$  has its source-drain path coupled in series with the resistor  $R_6$  between the terminal  $T_3$  and circuit ground and has its gate electrode coupled with the output terminal  $U'$  of the phase comparison circuit 4 through an inverter  $Q_{12}$ . Accordingly, the bypass switching transistor  $Q_{10}$  is operative to control the flow of the constant current  $i_3$  supplied by the current source transistor  $Q_3$  by bypassing the current  $i_3$  whenever the first phase difference signal  $U$  is high.

An n-channel bypass switching FET  $Q_{11}$  has its source-drain path connected in series through the resistor  $R_8$  between the terminal  $T_3$  and circuit ground and its gate electrode connected with the output terminal  $D'$  of the phase comparison circuit 4. Accordingly, the FET  $Q_{11}$  acts as a second bypass switching transistor for controlling the flow of the constant current  $i_6$  supplied by the current sink transistor  $Q_6$  such that whenever the second phase difference signal supplied at the output

terminal  $D'$  of the phase comparison circuit 4 is in a logic "1" state, the second bypass switching transistor  $Q_{11}$  is turned ON to bypass the current  $i_6$  which otherwise would flow through the current sink transistor  $Q_6$ . In all other respects, the operation of the FIG. 8 embodiment is identical to that of the FIG. 7 embodiment.

It will be readily appreciated by those skilled in the art that the embodiments of FIGS. 7 and 8 may be similarly constructed with the use of bipolar transistors in place of the field effect transistors (FETs) specifically disclosed herein.

Although specific embodiments of the invention have been described in detail herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one skilled in the art without departing from the scope or spirit of the invention as defined in the appended claims.

What is claimed is:

1. A charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals, comprising:

constant current source means for providing a first constant current;

constant current sinking means for absorbing a second constant current;

an output terminal adapted to be connected to a capacitive means;

switching means for providing said first constant current and said second constant current flowing in opposed directions through said output terminal to the capacitive means in response to said phase difference between said first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to said phase difference; and

means for substantially equalizing the magnitudes of the first constant current provided by said constant current source means and the second constant current absorbed by said constant current sinking means so that a linear relationship exists between said phase difference between said first and second input signals and the resulting charging and discharging periods of the capacitive means.

2. A charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals, comprising:

constant current source means including current source transistor means for providing a first constant current;

constant current sinking means for absorbing a second constant current;

means for substantially equalizing the magnitudes of the first constant current provided by said constant current source means and the second constant current absorbed by said constant current sinking means;

an output terminal adapted to be connected to a capacitive means; and

switching means for providing said first constant current and said second constant current flowing in opposed directions through said output terminal to the capacitive means in response to said phase difference between said first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to said phase difference, said switching

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means including transistor means for providing the capacitive means with said first constant current flowing through said output terminal in a first direction, and said current source transistor means and said first switching transistor means being coupled in series between a power source terminal of said charge pump circuit and said output terminal of said charge pump circuit.

3. The charge pump circuit according to claim 2, wherein said constant current sinking means comprises current sinking transistor means for absorbing said second constant current, and

said switching means further comprises second switching transistor means for providing the capacitive means with said second constant current flowing through said output terminal in a second direction;

said current sinking transistor means and said second switching transistor means being coupled in series between said output terminal of said charge pump circuit and a ground of said charge pump circuit.

4. A charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals, comprising:

constant current source means including current source transistor means for providing a first constant current;

constant current sinking means for absorbing a second constant current;

means for substantially equalizing the magnitudes of the first constant current provided by said constant current source means and the second constant current absorbed by said constant current sinking means;

an output terminal adapted to be connected to a capacitive means; and

switching means including first switching transistor means for bypassing current of said current source transistor means and thereby providing said first constant current and said second constant current flowing in opposed directions through said output terminal to the capacitive means in response to said phase difference between said first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to said phase difference.

5. The charge pump circuit according to claim 4, wherein said constant current sinking means comprises current sinking transistor means for providing said second constant current; and

said switching means comprises second switching transistor means for bypassing current of said current sinking transistor means.

6. A charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals, comprising:

constant current source means for providing a first constant current;

constant current sinking means for absorbing a second constant current;

means for substantially equalizing the magnitudes of the first and second constant currents including means for producing a third constant current substantially equal in magnitude to one of said first and

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second constant currents, and means for setting the other of said first and second constant currents substantially equal to said third constant current; an output terminal adapted to be connected to a capacitive means; and

switching means for providing said first constant current and said second constant current flowing in opposed directions through said output terminal to the capacitive means in response to said phase difference between said first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to said phase difference.

7. The charge pump circuit according to claim 6, wherein said means for producing a third constant current comprises:

first current mirroring means for producing said third constant current such that said third constant current is substantially equal in magnitude to a predetermined reference current; and

second current mirroring means for substantially equalizing the magnitude of said one of said first and second constant currents and said reference current.

8. The charge pump circuit according to claim 7, wherein said means for setting the other of said first and second constant currents substantially equal to said third constant current includes third current mirroring means for substantially equalizing the magnitude of said other of said first and second constant currents with the magnitude of said third constant current.

9. A charge pump circuit for charging capacitive means in response to a phase difference between first and second input signals, comprising:

constant current source means for providing a first constant current;

constant current sinking means for absorbing a second constant current;

means for substantially equalizing the magnitudes of the first and second constant current including means for maintaining said first constant current and said second constant current equal in magnitude to a reference current;

an output terminal adapted to be connected to a capacitive means; and

switching means for providing said first constant current and said second constant current flowing in opposed directions through said output terminal to the capacitive means in response to said phase difference between said first and second input signals for selectively charging and discharging the capacitive means to produce a voltage level thereof corresponding to said phase difference.

10. The charge pump circuit according to claim 9, further comprising means for adjusting the magnitude of the reference current to thereby adjust the magnitude of said first constant current and said second constant current.

11. The charge pump circuit according to claim 1, further comprising means for adjusting the magnitudes of said first constant current and said second constant current.

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Wong

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**[54] INTEGRATED CHARGE PUMP CIRCUIT  
WITH BACK BIAS VOLTAGE REDUCTION**

[75] Inventor: Stephen L. Wong, Scarsdale, N.Y.  
[73] Assignee: U.S. Philips Corp., New York, N.Y.  
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[52] U.S. Cl. .... 307/296.2; 323/314;  
363/60  
[58] Field of Search ..... 307/296.2; 363/60;  
323/313.4

**[56] References Cited****U.S. PATENT DOCUMENTS**

4,513,212	4/1985	Money	307/296.2
4,559,548	12/1985	Iizuka et al.	307/296.2
4,647,956	3/1987	Shrivastava et al.	307/296.2
4,675,557	7/1987	Huntington	323/314
4,825,142	4/1989	Wang	307/296.2
4,839,787	6/1989	Kojima et al.	363/60

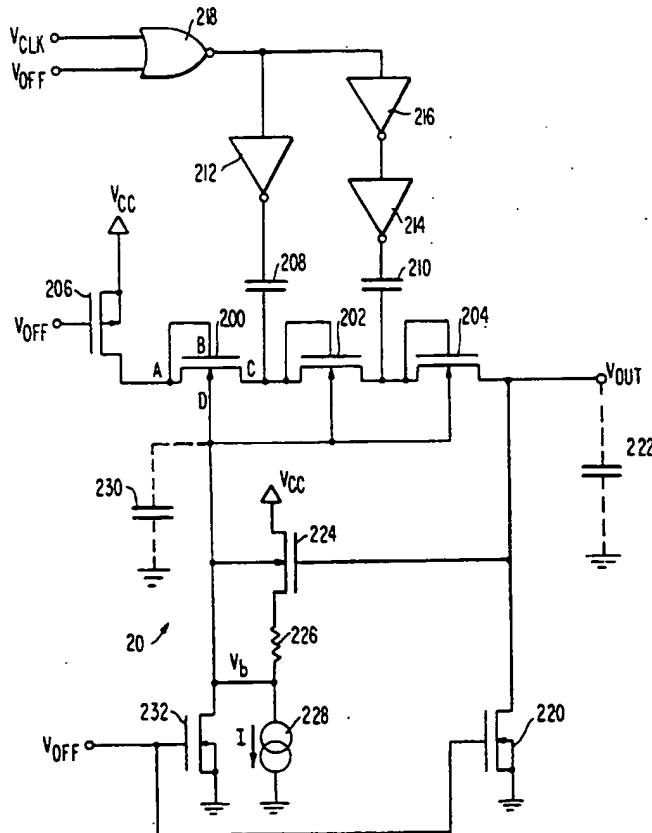
Primary Examiner—Stanley D. Miller

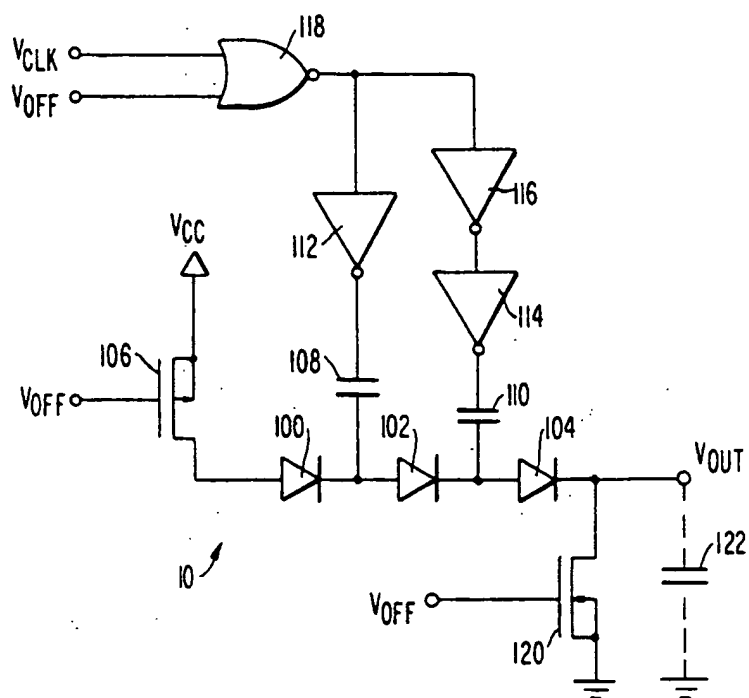
Assistant Examiner—Andrew Sanders  
Attorney, Agent, or Firm—Steven R. Biren

**[57] ABSTRACT**

An integrated charge pump circuit with back bias voltage reduction includes one or more diode type voltage-multiplier stages, with each stage having a diode-connected NMOS transistor in place of the conventionally-used p-n junction diode. The transistors are formed within a P-type well, which forms the back gate of each transistor within the well, and the transistor threshold voltages are dependent on the potential of the P-type well. Performance of the charge pump circuit using NMOS transistors is enhanced by the use of a bias circuit which generates a bias voltage as a function of the output voltage generated by the charge pump circuit, and applies this bias voltage to the P-type well to minimize the back-body effects of the NMOS transistors. The bias circuit thus permits the construction of an integrated charge pump circuit with significantly lower MOS diode voltage drops than would otherwise be possible.

4 Claims, 3 Drawing Sheets





**FIG. 1**  
PRIOR ART



FIG. 2

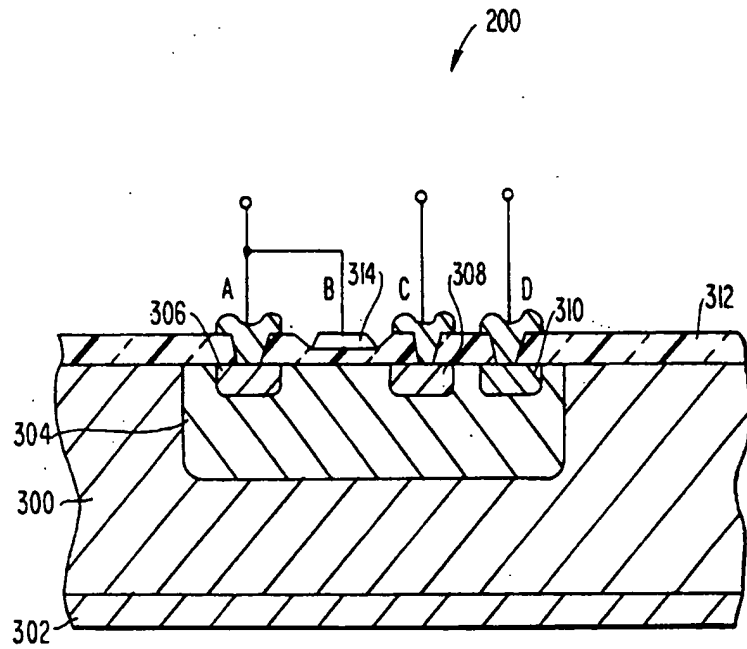


FIG. 3

# INTEGRATED CHARGE PUMP CIRCUIT WITH BACK BIAS VOLTAGE REDUCTION

## BACKGROUND OF THE INVENTION

The invention relates generally to voltage multiplier circuits, and relates more specifically to an integrated charge pump circuit with back bias voltage reduction.

Conventional charge pump circuits, such as those shown, for example, in FIG. 1 of this application or in FIG. 1 of U.S. Pat. No. 4,439,692, typically employ a plurality of series-connected diodes having an input terminal, an output terminal and one or more intermediate terminals, with each intermediate terminal being fed by a capacitively-coupled driver. Since the purpose of this circuit is to provide a voltage multiplication, the series-connected diodes in the charge-pump circuit must withstand voltages which exceed the normal power supply voltage range. When a charge pump circuit is required in MOS devices fabricated using standard MOS process technology, it becomes difficult to isolate the relatively high-voltage p-n junctions of these diodes, and additional process steps are usually necessary.

One possible solution to this problem, as shown in U.S. Pat. No. 4,439,692, is to use MOS-configured diodes (MOS transistors connected as diodes) for the conventional diodes of the prior art charge pump circuit. However, because these MOS-configured diodes typically have a larger diode drop (several volts as compared with the 0.7 volt of a conventional p-n junction), the voltage-multiplying capability of the charge pump is substantially degraded. In other words, to achieve a given output voltage level from the charge pump, the number of cascaded stages in an all-MOS charge pump would be greater than the number of stages in the conventional p-n junction diode circuit. This results in a slower, more complex circuit which occupies additional silicon area. Thus, using prior-art technology, there are substantial drawbacks connected with the otherwise-desirable use of MOS technology in fabricating charge pump circuits.

There are two basic reasons for the relatively large diode drops in MOS-configured diodes. First, in MOS process technology, it is conventional to use a threshold-implant step to force the threshold voltage to between about 1 and 2 volts. Thus, for example, in U.S. Pat. No. 4,439,692, all of the transistors in the charge pump circuit 18 in FIG. 3 are designated as "H" (hard) transistors. In this context, a "hard" transistor is deemed to be one which has a substantially larger positive or negative threshold voltage than that of a so-called "soft" transistor. Thus, as shown in FIG. 4 of U.S. Pat. No. 4,439,692, so-called "hard" transistors may have a threshold voltage of about +1 volt for enhancement mode FET's and a threshold voltage of about -3 volts for depletion-mode FET's. In no case will these "hard" transistors have a relatively low threshold voltage, as the "hard" transistors are by definition those which have a more negative or more positive threshold voltage value.

Secondly, the threshold voltage is further increased by a large body effect caused by large source-to-substrate voltages in integrated circuits employing MOS transistors in the charge pump circuit. This effect occurs because the sources of the MOS transistors cannot be tied to the P-well substrate in which the transistors (typically NMOS devices) are fabricated because the

sources must be allowed to rise above the supply voltage to permit the device to function as intended.

In order to create a relatively simple, efficient, fast and compact all-MOS charge pump circuit in an integrated circuit, these problem inherent in the prior-art structures must be overcome.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an integrated charge pump circuit which improves efficiency, speed, simplicity and compactness as compared to existing circuits.

In accordance with the invention, this object is achieved by a new integrated charge pump circuit having at least one diode type voltage-multiplier stage incorporating a diode-configured NMOS transistor fabricated in a P-type well which surrounds the NMOS transistor and forms its back gate. The improved physical and operational characteristics of the invention are achieved by making the NMOS transistor a relatively low-threshold transistor, and by using a bias circuit to generate a bias voltage which is less than the back bias voltage generated by the charge pump circuit. This bias circuit is advantageous in that it allows the P-type well to be biased at its highest possible potential without forward biasing any P-type well to bulk or P-type well to source junction. In this manner, the voltage difference between the source of the NMOS transistors and the P-type well can be minimized. This reduces the back bias voltage which further reduces the threshold of the NMOS transistors to result in a structure which offers performance in an all-MOS charge pump which approaches that of prior-art p-n junction diode circuits.

In a preferred embodiment of the invention, the threshold of the diode-configured transistors is selected to be relatively low (less than one voltage at zero back-body bias).

The bias circuit used to generate the bias voltage in the charge pump circuit may advantageously be composed of a further NMOS transistor connected as a source follower, with its gate being connected to an output terminal of the charge pump circuit and its source being coupled, through a resistor, to the P-type well in which the back gates of the diode-connected MOS transistors are formed. This configuration allows the P-well to always be biased one gate-to-source voltage plus one resistor drop below the output terminal voltage of the charge pump when the output is less than the supply voltage, and biased just one resistor drop below the supply voltage when the output is above the supply voltage. The value of the resistor drop can be selected to secure the desired output voltage value. This bias circuit serves to minimize the back bias when the charge pump is ON, and prevents forward conduction from the P-well to the bulk junction when the charge pump is OFF. The invention may be more completely understood with reference to the following detailed description, to be read in conjunction with the accompanying drawing.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows a schematic circuit diagram of a prior art charge pump circuit;

FIG. 2 shows a schematic circuit diagram of an all-MOS charge pump circuit in accordance with the invention; and

FIG. 3 shows a simplified cross section of a semiconductor device that is used in the integrated charge pump circuit in accordance with the invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a conventional prior-art charge pump circuit 10 employing series-connected p-n junction diodes 100, 102 and 104. Power supply voltage  $V_{cc}$  is fed to the anode of diode 100 through switching transistor 106 and the output voltage of the charge pump is generated at the cathode of diode 104, as shown by the symbol  $V_{out}$ . The intermediate points in the diode string are connected to capacitors 108 and 110, which are in turn driven by inverters 112, 114 and 116, and NOR gate 118 having inputs  $V_{off}$  and  $V_{clk}$ . The circuit is turned ON and OFF by MOS transistors 106 and 120, which serve respectively to connect the anode of diode 100 to the power supply and disconnect the output terminal  $V_{out}$  when the circuit is OFF, with the switching being accomplished as a function of the signal  $V_{off}$  applied to the gates of transistors 106 and 120. The capacitance of the load connected to the terminal  $V_{out}$  is shown schematically by a capacitor 122 connected between the output terminal and ground by a dotted line.

The prior-art circuit of FIG. 1 operates in a conventional manner similar to that of charge pump 18 in FIG. 1 of U.S. Pat. No. 4,439,692, and accordingly will not be described in detail. Briefly, however, the circuit operates as follows.

$V_{clk}$  is a high frequency clock signal (about 1 MHz) that feeds the input of inverters 112 and 116.  $V_{off}$  is a control signal which, when high, disables the charge pump by blocking the  $V_{clk}$  signal and by discharging the load capacitor 122. When  $V_{off}$  is low, the  $V_{clk}$  signal is allowed to pass through gate 118; transistor 106 turns on, and 120 turns off. In this state, the charge pump is on; node  $V_{out}$  is first pulled to a value 3 diode drops below  $V_{cc}$ ; alternating pulses that drive capacitors 108 and 110 at the  $V_{clk}$  frequency effectively deliver charge packets that further drive up the voltage  $V_{out}$  across capacitor 122. The unidirectional connection of the diodes (100, 102, 104) forms a voltage multiplying circuit that forces charged to flow only in the direction of the output.

With this scheme, it can be shown that the achievable steady state value of  $V_{out}$  is

$$V_{out} = V_{cc} + 2V_p - 3V_d$$

where  $V_p$  is the output swing of inverting drivers 112 and 114, and  $V_d$  is the diode drop across diode 100, 102, or 104. Thus it can be seen that  $V_{out}$  is maximized if the diode drops are minimized.

In conventional charge pump circuits such as the one shown in FIG. 1, the node voltages at p-n junction diodes 100, 102 and 104 will exceed the supply voltage  $V_{cc}$ . When this type of circuit is implemented in an MOS structure, using standard MOS processed technology, it becomes difficult to isolate these high-voltage p-n junctions and additional process steps are usually required. One way to overcome these problems is to substitute MOS-configured diodes for the p-n junction diodes in the charge pump circuit, as shown for example in U.S. Pat. No. 4,439,692. However, because MOS transistors typically have larger diode drops (several volts as compared to 0.7 volts for a typical p-n junction), the voltage-multiplying capability of the charge pump circuit is substantially degraded. To achieve a

given output voltage from the charge pump, the number of cascaded stages would have to be increased when using MOS transistors instead of p-n junction diodes. This has a very adverse affect on the speed of operation of the circuit, and requires additional silicon area as well.

The main reason for this relatively large MOS diode drop, and the resulting degradation in performance, is that the source of the MOS devices in the charge pump cannot be tied to the P-well substrate because the source must be allowed to rise above the supply voltage during operation. This problem, present in prior-art MOS charge pump circuits such as those disclosed in U.S. Pat. No. 4,439,692, results in larger, slower and less efficient implementation of charge pump circuitry.

FIG. 2 shows an improved charge pump circuit 20 in accordance with the invention, in which the aforementioned problem is largely eliminated, thus resulting in a faster, smaller and thus more efficient all-MOS charge pump circuit implementation. It should be noted that while a two-stage charge pump circuit is shown in FIG. 2, charge pump circuits in accordance with the invention can also be fabricated with only one stage, or with more than two stages. Also, for clarity, components in FIG. 2 having counterparts in FIG. 1 are provided with reference numerals having the last two digits the same as those of the corresponding components in FIG. 1.

In FIG. 2, the basic charge-pump circuit with its capacitively-coupled drivers (shown in the top portion of the figure) is the same as that of FIG. 1, except that the p-n junction diodes 100, 102 and 104 have been replaced by diode-connected MOS transistors 200, 202 and 204, respectively. In accordance with the invention, and contrary to the teaching of the prior art, these transistors can advantageously be low threshold unimplanted NMOS transistors, with a threshold voltage of less than one volt. Such transistors can be easily fabricated without using additional masks, in a double-poly process, by forming the gates of the transistors with a poly-layer that is provided before the threshold implant, thereby effectively shielding the implant from the channel.

Additionally, a new bias circuit, shown in the lower portion of FIG. 2, provides a reduced back-bias voltage for the P-well in which the diode-connected MOS transistors 200, 202 and 204 are fabricated, when the charge pump is ON. Additionally, this bias circuit prevents forward conduction in the P-well to bulk junction when the charge pump is OFF. Physically, the back gate terminals of the diodes can be either the individual p-wells of the diodes, as shown in FIG. 3, electrically tied together, or they can be one common p-well surrounding all three diodes. By way of example, FIG. 3 shows a simplified cross-section of a representative diode-connected transistor, here transistor 200 of FIG. 2. In transistor 200, a substrate 300, here of n-type conductivity, is provided with a highly-doped n type contact layer 302 and a p type well 304. Drain and source regions 306 and 308 of n type conductivity are provided in the well 304, along with a p type back-gate contact 310. An insulating layer 312, typically of silicon dioxide, is provided over the top surface of the device, and is provided with apertures for contacting the drain, source and back gate contact. A gate electrode 314 is provided over a portion of the insulating layer 312 having reduced thickness, and the gate electrode is connected to drain region 306. For clarity, corresponding

terminals A, B, C and D of transistor 200 are shown in both FIG. 2 and FIG. 3. Alternatively, as noted above, all of the diode-connected transistors can be fabricated in a single p type well.

In the circuit of FIG. 2, the output voltage  $V_{out}$  is taken from the output region of the device and is provided to the gate of an additional MOS transistor 224 which is connected in a source follower configuration with its channel connected between the supply voltage  $V_{cc}$  and one end of a resistor 226. The other end of resistor 226 is connected to one terminal of a current source 228, the other terminal of which is connected to ground. The output of the bias circuit is taken at the junction between the resistor 226 and the current source 228, and the bias voltage developed at this point is designated as  $V_b$ . The bias voltage  $V_b$  is then applied to the back gates of transistors 200, 202, 204, and 224 within the P-well, with capacitor 230, shown in dotted lines in FIG. 2, representing the capacitance of the P-well. Finally, an additional transistor 232 is provided to discharge the bias voltage to ground when the charge pump is turned OFF, while the charge pump output voltage  $V_{out}$  is discharged to ground by transistor 220.

In each phase of operation, it is important that the p-well potential of the MOS diodes remain below the  $V_{cc}$  potential, and always be lower than the lowest source of drain node potential of these transistors, because otherwise parasitic p-n junctions can be activated that can result in destructive latch-up of the circuit. At the same time, it is important that the p-well potential be as high as possible in order to minimize the back body effect, and thus the threshold voltages, of these diodes. The bias circuit shown in FIG. 2 allows the p-well potential to be biased at least one gate-to-source voltage below the lowest source potential of the diodes when  $V_{out}$  is still below  $V_{cc}$  (during the transient charging phase of the output), and be biased at about  $V_{cc}$  when  $V_{out}$  is above  $V_{cc}$  (during steady state).

The bias voltages can be further reduced by adding an optional resistive drop via resistor 22 so that the amount of body effect, and thus the threshold voltage, of the MOS diode can be tailored to realize an exact value of the output at steady state.

The bias circuit receives a voltage  $V_{out}$  at the gate of source-follower transistor 224, and generates a bias voltage  $V_b$  which is roughly equal to  $V_{cc} - I_{228} \times R_{226}$ . Thus, the bias voltage can be precisely controlled in order to optimize the diode drops across the MOS-connected transistors 200, 202 and 204. When the charge pump is turned OFF, transistors 220 and 232 are activated by the voltage  $V_{off}$ , thereby discharging both  $V_{out}$  and  $V_b$  to ground. It should be noted that if the

particular circuit application does not require the bias voltage to be well controlled, then the value of resistor 226 can be set to zero without sacrificing the benefit to be derived from the invention.

In order to insure that  $V_{out}$  will not discharge faster than  $V_b$ , which might forward bias the P-well to the output region junction of transistor 204, the width-to-length ratio W/L of transistors 220 and 232 can be proportioned in accordance with the ratio of the load capacitance 222 to the P-well capacitance 230.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail, such as using a charge pump with a different number of stages, or using different polarity devices may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An integrated charge pump circuit comprising an output terminal for outputting a back bias voltage and at least one diode-type voltage-multiplier stage having a diode-configured NMOS transistor, a P-type well surrounding said NMOS transistor and forming the back gate thereof, said NMOS transistor being a low-threshold transistor, and a bias circuit for continuously generating a bias voltage as a function of and less than said back bias voltage to be applied to said P-type well and having an input connected to and having an input signal derived continuously from said output terminal and an output connected to and providing an output signal continuously to said P-type well.

2. An integrated charge pump circuit as claimed in claim 1, wherein the threshold voltage of said diode-configured transistor is less than about one volt at zero back gate bias.

3. An integrated charge pump circuit as claimed in claim 1, wherein said bias circuit comprises a further NMOS transistor connected as a source-follower, the input of said source follower being connected to said output terminal and the output of said source follower being coupled to said P-type well.

4. An integrated charge pump circuit as claimed in claim 3, further comprising a resistor and a current source connected in series, a first terminal of said resistor being connected to the source of said further NMOS transistor, a second terminal of said resistor being connected to a first terminal of said current source and forming the output of said source follower, a second terminal of said current source being connected to ground, and the drain of said further NMOS transistor being connected in operation to a source of voltage.

\* \* \* \* \*



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**United States Patent** [19]  
**Marshall**

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[45] **Date of Patent:** **May 5, 1992**

[54] **CHARGE PUMP**

[75] **Inventor:** Andrew Marshall, Dallas, Tex.

[73] **Assignee:** Texas Instruments Incorporated,  
Dallas, Tex.

[21] **Appl. No.:** 630,703

[22] **Filed:** Dec. 20, 1990

[51] **Int. Cl.<sup>5</sup>** ..... H02M 7/00

[52] **U.S. Cl.** ..... 363/60; 363/59

[58] **Field of Search** ..... 363/59, 60, 61

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,186,436 1/1980 Ishiwatari ..... 363/60  
4,926,354 5/1990 Pattantyus ..... 363/60 X

**FOREIGN PATENT DOCUMENTS**

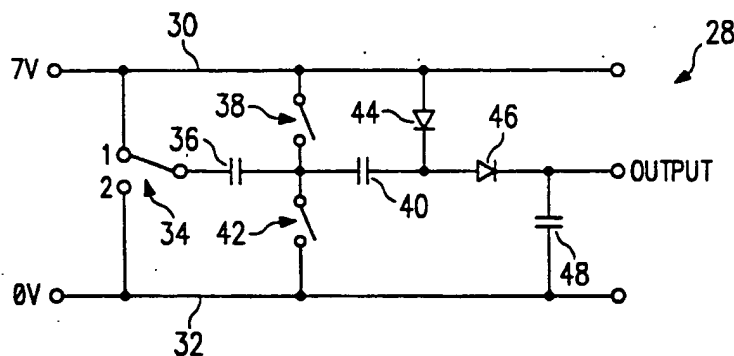
0010166 1/1984 Japan ..... 363/60 X  
0026466 2/1986 Japan .

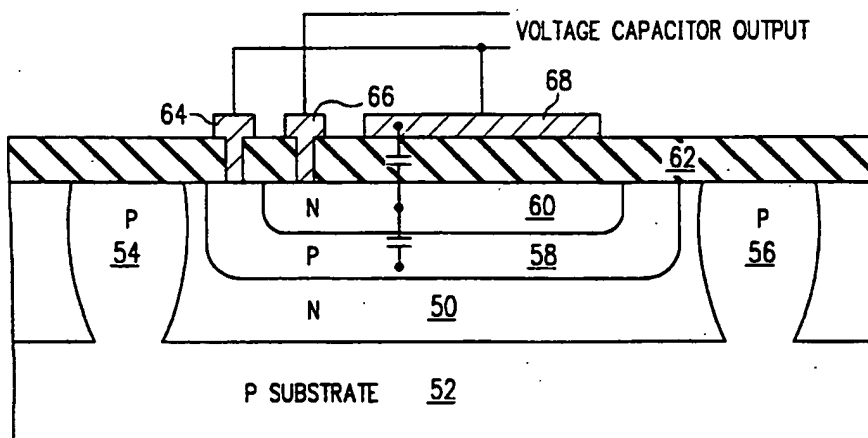
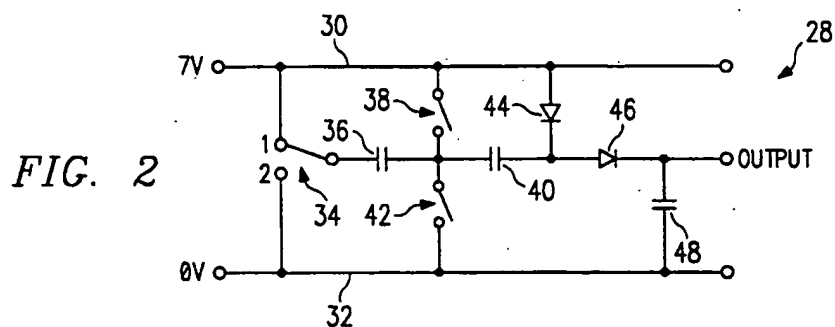
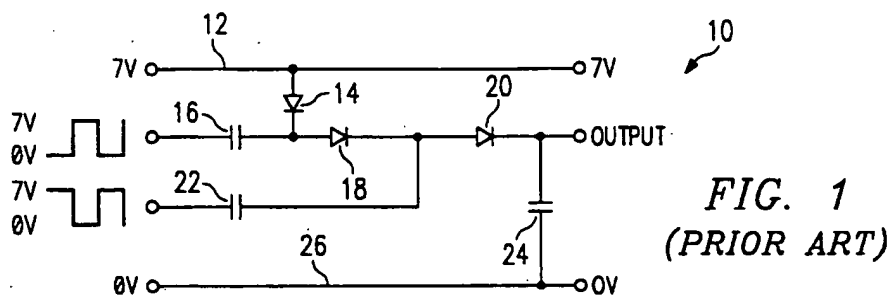
*Primary Examiner*—Steven L. Stephan  
*Assistant Examiner*—Emanuel Todd Voeltz  
*Attorney, Agent, or Firm*—B. Peter Barndt; Richard  
Donaldson; William E. Hiller

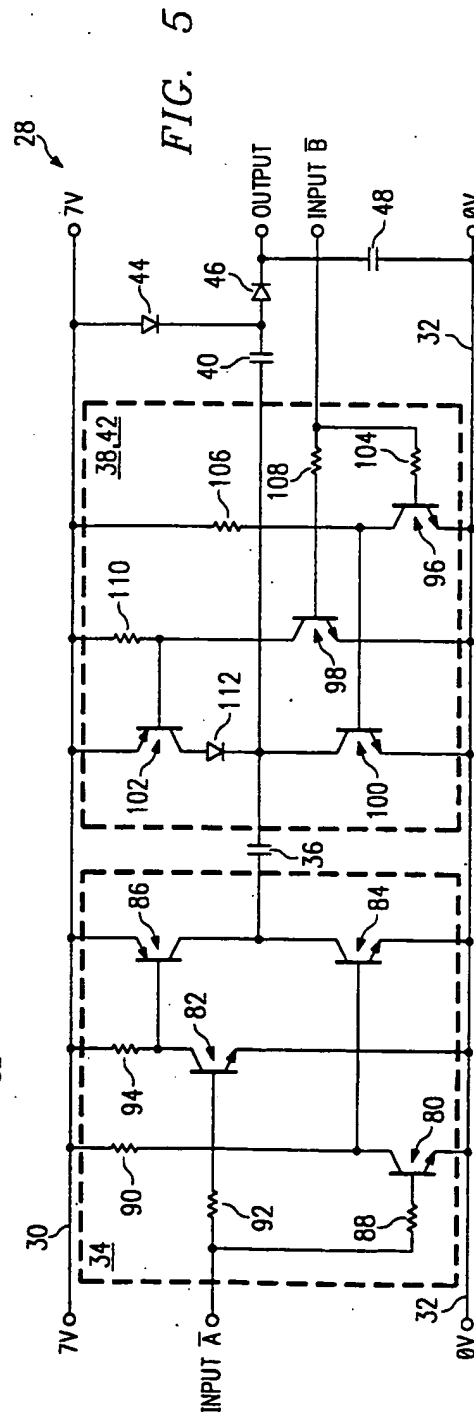
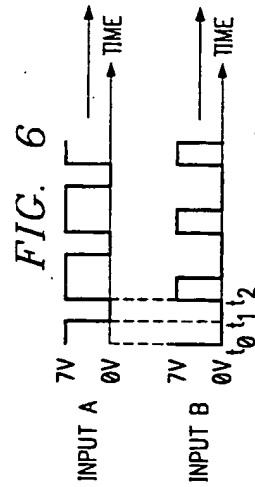
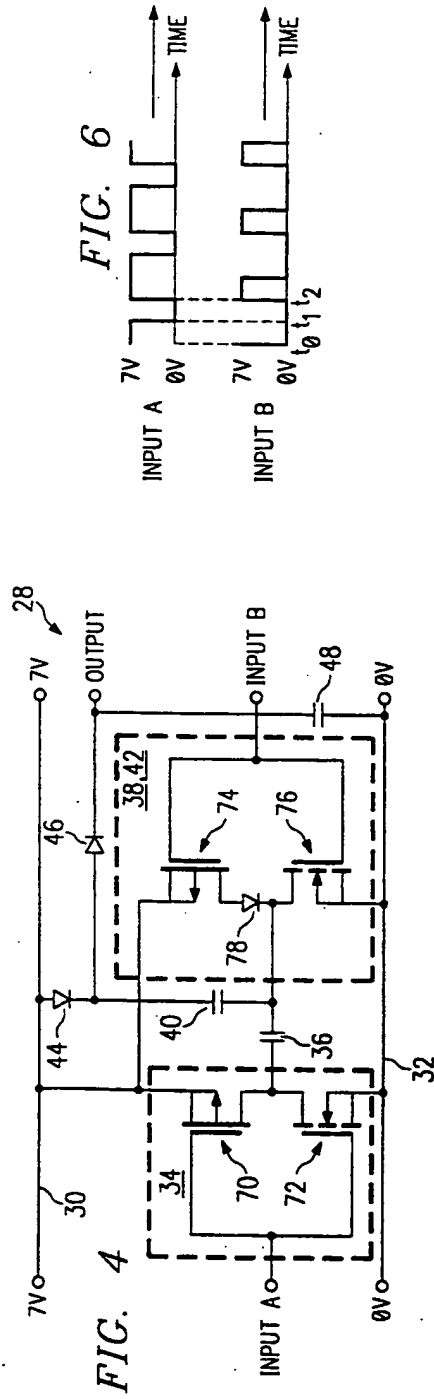
[57] **ABSTRACT**

A charge pump comprises high voltage and low voltage supply rails coupled to first and second capacitors via switching circuitry. The switching circuitry is operable to charge the first and second capacitors to desired voltages to generate a desired output voltage of increased magnitude.

20 Claims, 2 Drawing Sheets









## CHARGE PUMP

## BACKGROUND OF THE INVENTION

In many circuits, it is necessary to generate a voltage which is greater in magnitude than the supply voltage. For example, in order to efficiently drive DMOS output structures of MOS based power IC's, it is necessary to supply a gate-to-source voltage of typically 10-15 volts. In many high-side drive and low-side drive intelligent power switches, a voltage tripler is normally required, as the bulk of intelligent power switch designs are for the automotive market, where operating voltage may be as low as 4.5 volts. At this voltage, most DMOS structures are not functional, or have a very high on resistance. A voltage doubler would normally provide about 7 volts, with a supply voltage of 4.5 volts, when diode and saturation losses are taken into account. This is normally insufficient to fully turn on a DMOS output, so a tripler is required. Other circuits, such as EPROMS and EEPROMS, require a programming voltage ( $V_{pp}$ ) of 12-17 volts to be generated from a five volt supply.

Typically, charge pumps (also referred to as "voltage multipliers") are used to generate a voltage of increased magnitude. Present day charge pumps comprise a series of stages, each stage including a capacitor and a MOS or junction diode. Each stage of the charge pump boosts the magnitude of the voltage signal by a voltage equal approximately to the voltage swing of a clock signal applied to the capacitor less the threshold voltage of the diode. At each stage, the capacitor will see an increased maximum voltage difference across its plates. For example, using a seven volt supply, the first capacitor will see a difference of seven volts across its plates and the capacitor of the second stage will see a maximum voltage difference of fourteen volts across its plates. Subsequent stages would result in additional increased voltage across the capacitors. The magnitude of voltage across the capacitor will determine its structure and size. Consequently, by limiting the voltage across the capacitors, the density of the circuit can be increased and the complexity of the fabrication may be decreased.

Therefore, a need has arisen in the industry for a charge pump using low voltage capacitors.

## SUMMARY OF THE INVENTION

In accordance with the present invention, a charge pump is provided which substantially eliminates the problems associated with prior such devices.

The charge pump of the present invention provides high and low voltage supply rails having a predetermined voltage differential. First and second capacitors are coupled in series. Switching circuitry is coupled to the high voltage and low voltage supply rails and to the first and second capacitors, and is operable to selectively charge the first and second capacitors to desired voltages to generate a desired output voltage.

The present invention provides significant advantages over the prior art. By selectively charging the series capacitors, the increased voltage can be obtained by using low voltage capacitors, thereby decreasing the complexity of the circuit design and increasing the density of the device.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now

made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a schematic representation of a prior art charge pump;

FIG. 2 illustrates a schematic representation of a preferred embodiment of the charge pump of the present invention;

FIG. 3 illustrates a cross-sectional side view of a base-emitter capacitor which may be used in the present invention;

FIG. 4 illustrates a schematic representation of a MOS implementation of the charge pump of FIG. 2;

FIG. 5 illustrates a schematic representation of a bipolar implementation of the charge pump of FIG. 2; and

FIG. 6 illustrates the timing diagrams for the input waveforms for the charge pump of FIGS. 4 and 5.

## DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiment of the present invention and its advantages are best understood by referring to FIGS. 1-6 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIG. 1 illustrates a schematic representation of the prior art charge pump circuit 10. The high voltage supply rail 12 (shown at seven volts) is coupled to the anode of diode 14. The cathode of diode 14 is coupled to the first plate of capacitor 16 and to the anode of diode 18. The second plate of capacitor 16 is coupled to a clock signal. The cathode of diode 18 is coupled to the anode of diode 20 and to the first plate of capacitor 22. The second plate of capacitor 22 is coupled to a clock signal (typically a square wave) which is 180° out of phase with the clock signal coupled to capacitor 16. The cathode of diode 20 is coupled to the first plate of a capacitor 24 having a second plate coupled to the low voltage supply rail 26 (shown at zero volts) for a low side driver case. The output voltage is taken across capacitor 24. The capacitor may also be coupled between the cathode of diode 20 and the high voltage rail, or between the cathode of diode 20 and another voltage node.

For simplicity of explanation, the operation of the charge pump will be described without taking into account the voltage drops across the diodes 14, 18 and 20. Typically, however, the diodes will each account for a voltage drop of approximately 0.7 volts for a junction diode and a voltage drop which is significantly higher for a MOS diode. Initially, it is assumed that the voltage at the cathodes of diodes 14, 18 and 20 is seven volts, generated by the high voltage supply rail 12. The clock signal coupled to capacitor 16 is initially at zero volts and the clock signal coupled to capacitor 22 is initially at seven volts. As the clock coupled to capacitor 16 transitions from zero volts to seven volts, the voltage at the cathode of diode 14 is boosted from seven volts to fourteen volts. Consequently, the voltages at the cathodes of diodes 18 and 20 are also boosted to fourteen volts. When the clock coupled to capacitor 16 transitions from zero volts to seven volts, the clock coupled to capacitor 22 transitions from seven volts to zero volts. As the clock transitions from zero volts to seven volts, the voltage at the cathode of diode 18, and consequently the voltage at the cathode of diode 20, is boosted to twenty-one volts. Hence, the voltage supplied by the voltage rails 12 and 26 is essentially tripled.

As can be seen, the voltage across capacitor 22 may be as great as fourteen volts. If additional stages were used, each capacitor would have an increased voltage across it. Hence, high voltage capacitors must be used.

FIG. 2 illustrates a schematic representation of the preferred embodiment of the charge pump of the present invention. The charge pump 28 has high voltage and low voltage supply rails 30 and 32, shown at seven volts and zero volts, respectively. A first switch 34 selectively couples a first plate of capacitor 36 to one of the supply rails 30 or 32. Switch 38 selectively couples the high voltage supply rail 30 to the second plate of capacitor 36 and to the first plate of capacitor 40. Similarly, switch 42 selectively couples the low voltage supply rail to the second plate of capacitor 36 and the first plate of capacitor 40. Diode 44 has an anode connected to the high voltage supply rail 30 and a cathode coupled to the second plate of capacitor 40. Diode 46 has an anode coupled to the cathode of diode 44 and a cathode coupled to the first plate of capacitor 48. The second plate of capacitor 48 is coupled to the low voltage supply rail 32 (or to the high voltage rail, if desired, or to another voltage node). If the charge pump 28 is coupled to a DMOS transistor, the gate/source and gate/drain capacitances can be used as capacitor 48 by coupling the cathode of diode 46 to the gate of the DMOS transistor. The operation of the charge pump 28 will be discussed in connection with TABLE 1.

TABLE 1

STEP	Switch 34	Switch 38	Switch 42
1	2	CLOSED	OPEN
2	1	OPEN	OPEN
3	2	OPEN	CLOSED
4	2	CLOSED	OPEN
5	1	OPEN	OPEN
6	2	OPEN	CLOSED

Initially, it is presumed that capacitors 36, 40 and 48 are discharged to zero volts. In step 1, switch 34 couples the low voltage supply rail to the first plate of capacitor 36, switch 38 is closed, and switch 42 is open. Hence, capacitor 36 is charged to seven volts. In step 2, the high voltage supply rail 30 is coupled to the first plate of capacitor 36, switch 38 is open and switch 42 is open. Hence, the first plate of capacitor 36 is at seven volts, the second plate of capacitor 36 is boosted to fourteen volts. The first and second plates of capacitor 40 are likewise boosted to fourteen volts. In step 3, switch 34 couples the low voltage supply rail 32 to the first plate of capacitor 36, switch 38 is open and switch 42 is closed. Hence, capacitor 36 is discharged to zero volts, and capacitor 40 is charged to seven volts. The sequence of the first three steps puts the charge pump 28 in the desired initial condition.

The three-step cycle described above is repeated in steps 4-6. In step 4, the first capacitor is charged to seven volts, generating a fourteen volt potential across the two capacitors 36 and 40. In step 5, the high voltage supply rail 30 is coupled to the first plate of capacitor 36, thereby boosting the voltage on the second plate of capacitor 36 to fourteen voltages and boosting the voltage on the second plate of capacitor 40 to twenty-one volts. Hence, capacitor 48 is charged to twenty-one volts. In step 6, capacitor 36 is discharged, preparing the charge pump for the next cycle. The three-step cycle may be repeated as often as necessary to maintain the desired voltage across capacitor 48.

As can be seen, no more than seven volts is placed across either capacitor 36 or 40. Additional capacitors could be provided in series along with respective switches to the high and low rails 30 and 32 in order to further increase the generated output voltage. Even with additional capacitors, no capacitor in the series would need to handle more than seven volts. Hence, only one capacitor, capacitor 48, needs to be a high voltage capacitor.

Consequently, a low voltage capacitor structure, such as that shown in FIG. 3, may be used to implement the series capacitors 36 and 40. FIG. 3 illustrates a cross-sectional side view of structure readily available in bipolar, biCMOS, and similar integrated circuit processes. An n tank region 50 is formed in a substrate 52. The n tank region is isolated by p regions 54 and 56. A p type diffused region 58 is formed in the n tank 50 and an n type diffused region 60 is formed in the p type diffused region 58. The p type and n type diffused regions 58 and 60 may be formed in conjunction with the base and emitter diffusions of an npn transistor. An oxide layer 62 overlies the structure with contacts 64 and 66 providing an electrical coupling to the p type diffused region 58 and the n type diffused region 60, respectively. The base/emitter capacitor formed by the n type diffused region 60 and p type diffused region 58 is well suited for implementing the seven-volt capacitors 36 and 40. An emitter/metal capacitor can also be implemented by forming a metal layer 68 on the emitter 60.

FIG. 4 illustrates a MOS implementation of the charge pump 28 of FIG. 2. In this embodiment, switch 34 is implemented by PMOS transistor 70 and NMOS transistor 72. The gates of transistors 70 and 72 are coupled to an input A (shown in FIG. 6). The source of PMOS transistor 70 is connected to the high voltage supply rail 30 and the source of NMOS transistor 72 is connected to the low voltage supply rail 32. The drains of the transistors 70 and 72 are coupled to the first plate of capacitor 36.

Switches 38 and 42 are implemented by PMOS transistor 74, NMOS transistor 76 and diode 78. The gates of transistors 74 and 76 are connected an input B (shown in FIG. 6). The sources of transistors 74 and 76 are coupled to the high voltage rail 30 and the low voltage rail 32, respectively. The drain of transistor 74 is coupled to the anode of diode 78. The cathode of diode 78 is coupled to the drain of transistor 76.

The operation of the charge pump 28 shown in FIG. 4 will be discussed in connection with the timing diagram shown in FIG. 6. At  $t_0$ , input A is high and input B is low. With input A high, the NMOS transistor 72 is enabled and the PMOS transistor 70 is disabled, thereby coupling the low voltage supply rail 32 to the first plate of capacitor 36. With input B low, PMOS transistor 74 is enabled and the NMOS transistor 76 is disabled, thereby coupling the high voltage supply rail 30 to the second plate of capacitor 36 and the first plate of capacitor 40. At  $t_1$ , input A transitions low while input B remains low. A low voltage on input A enables PMOS transistor 70 and disables NMOS transistor 72, thereby coupling the high voltage supply line 30 to the first plate of capacitor 36. Consequently, the voltage on the second plate of capacitor 36 is boosted to fourteen volts, causing diode 78 to decouple the high voltage supply line 30 from the second plate of capacitor 36 and the first plate of capacitor 40, even though transistor 74 is still enabled.

At  $t_2$ , inputs A and B both transition high, enabling NMOS transistors 72 and 76 and disabling PMOS transistors 70 and 74. Hence, the first plate of capacitor 36 is coupled to zero volts and the second plate of capacitor 36 and the first plate of capacitor 40 are coupled to zero volts. As can be seen from FIG. 6, inputs A and B repeat the three-stage cycle continuously.

FIG. 5 illustrates an embodiment of the charge pump 28 which is implemented using bipolar technology. In this implementation, switch 34 is implemented using npn transistors 80, 82, and 84, and pnp transistor 86. The base of transistor 80 is coupled to input A (the inversion of clock signal A illustrated in FIG. 6) via resistor 88. The collector of transistor 80 is coupled to the high supply line 30 via resistor 90, and to the base of transistor 84. The emitter of transistor 80 is coupled to the low voltage supply rail 32. The base of transistor 82 is coupled to input A via resistor 92. The collector of transistor 82 is coupled to the high voltage supply rail 30 via resistor 94 and to the base of transistor 86. The emitter of transistor 82 is coupled to the low voltage supply rail 32. The collector of transistor 84 is connected to the collector of transistor 86. The emitter of transistor 84 is coupled to the low voltage supply rail 32 and the emitter of transistor 86 is coupled to the high voltage supply rail 30.

Switches 38 and 42 are implemented using npn transistors 96, 98 and 100 and pnp transistor 102. The base of npn transistor 96 is coupled to input B (the inversion of clock signal B of FIG. 6) via resistor 104. The collector of transistor 96 is coupled to the high voltage supply rail 30 via resistor 106 and to the base of transistor 100. The emitter of transistor 96 is coupled to the low voltage supply rail 32. The base of transistor 98 is coupled to input B via resistor 108. The collector of transistor 98 is coupled to the high voltage supply rail 30 via resistor 100 and to the base of transistor 102. The emitter of transistor 98 is coupled to the low voltage supply rail 32. The collector of transistor 100 is connected to the cathode of diode 112. The anode of diode 112 is connected to the collector of transistor 102. The emitter of transistor 102 is coupled to the high voltage supply rail 30 and the emitter of transistor 100 is connected to the low voltage supply rail 32.

The operation of the charge pump 28 of FIG. 5 is similar to the operation of the charge pump of FIG. 4. When input A is low, the first plate of capacitor 36 is coupled to the low voltage supply rail 32 and when input A is high, the high voltage supply rail 30 is coupled to the first plate of capacitor 36. Similarly, when input B is low, the low voltage supply rail 32 is coupled to the second plate of capacitor 36 and to the first plate of capacitor 40. When input B is high, the high voltage supply rail 30 is coupled to the second plate of capacitor 36 and the first plate of capacitor 40, unless the voltage at the cathode of diode 112 is greater than seven volts, in which case neither supply rail is coupled to the capacitors 36 and 40.

In the preferred embodiment, the seven-volt rail is internally generated; for example, using a Zener regulator. Further, a switch may be included in series with diode 44, 46 or with the output node. This switch would be used for the purpose of switching off the device coupled to the output of the charge pump 28.

The present invention allows a charge pump to be implemented using low voltage capacitors, fabricated using standard processes. The use of low voltage capac-

itors decreases the size of the devices and the complexity of fabricating the capacitors.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A charge pump comprising:
  - high voltage and low voltage supply rails having a predetermined voltage differential;
  - first and second capacitors coupled in series;
  - first switching circuitry coupled to said high voltage and low voltage supply rails and said first and second capacitors, said first switching circuitry operable to selectively charge said first and second capacitors to desired voltages; and
  - second switching circuitry coupled to said high voltage and low voltage supply rails and to said first capacitor, said second switching circuitry operable to selectively couple said first capacitor to said high and low voltage supply rails to said first capacitor so as to generate a desired output voltage.
2. The charge pump of claim 1 and further comprising a third capacitor operatively coupled between the second capacitor and one of said supply rails.
3. The charge pump of claim 1 and further comprising a third capacitor operatively coupled between the second capacitor and a voltage node.
4. The charge pump of claim 3 wherein said third capacitor comprises the gate of a DMOS transistor.
5. The charge pump of claim 2 and further comprising a diode coupled between said second and third capacitors to prevent a charge transfer from said third capacitor to said second capacitor.
6. The charge pump of claim 1 wherein said switching circuitry further comprises a first switch selectively coupling a first plate of said first capacitor to said high voltage and low voltage supply rails.
7. The charge pump of claim 6 wherein said switching circuitry further comprises a second switch for selectively coupling a second plate of said first capacitor and a first plate of said second capacitor to the high voltage supply rail or to the low voltage supply rail.
8. The charge pump of claim 7 wherein said second switch is operable to decouple said second plate of the first capacitor and the first plate of the second capacitor from both the high and low voltage supply rails.
9. The charge pump of claim 6 wherein said first switch comprises a PMOS transistor and an NMOS transistor having gates coupled to a clock signal, sources coupled to the high voltage and low voltage supply rails, respectively, and drains coupled to the first plate of said first capacitor.
10. The charge pump of claim 7 wherein said second switch comprises a PMOS transistor and an NMOS transistor having gates coupled to a second clock signal, sources coupled to the high voltage and low voltage supply rails, respectively, and drains coupled to the second plate of said first capacitor and to the first plate of said second capacitor.
11. The charge pump of claim 10 and further comprising a diode coupled between the drains of the PMOS and NMOS transistors.
12. The charge pump of claim 6 wherein said first switch comprises a pnp and a npn transistor having bases driven responsive to a clock signal, emitters cou-

pled to said high and low voltage rails, respectively, and collectors coupled to the first plate of said first capacitor.

13. The charge pump of claim 7 wherein said second switch comprises a pnp and a npn transistor having bases driven responsive to a clock signal, emitters coupled to said high and low voltage rails, respectively, and collectors coupled to the second plate of said first capacitor and the first plate of said second capacitor.

14. The charge pump of claim 13 and further comprising a diode coupled between the collectors of said pnp and npn transistors.

15. A method of multiplying a supplied voltage comprising the steps of:

providing first and second capacitors, said first and second capacitors each comprising first and second plates, said first plate of said second capacitor coupled to the second plate of said first capacitor;

providing first switching circuitry operable to selectively couple said first plate of said second capacitor and said second plate of said first capacitor to a high voltage supply rail and alternatively to a low voltage supply rail;

providing second switching circuitry operable to selectively couple said first plate of said first capacitor to said high voltage supply rail and alternatively to said low voltage supply rail;

charging said second capacitor to a first predetermined voltage;

charging said first capacitor to a second predetermined voltage, such that said voltage across said first and second capacitors is substantially equal to the sum of said first and second predetermined voltages; and

increasing the voltage at said first plate of said first capacitor, thereby increasing the voltage output from the second plate of said second capacitor.

16. The method of claim 15 and further comprising the step of charging a third capacitor responsive to the voltage on the second plate of said second capacitor.

17. The method of claim 15 wherein said first predetermined voltage equals said second predetermined voltage.

18. The method of claim 15 wherein said step of charging said second capacitor comprises the step of selectively coupling said second capacitor between high and low voltage rails.

19. The method of claim 18 wherein said step of charging said first capacitor comprises the step of selectively coupling the first capacitor between said high and low supply rails.

20. The method of claim 19 wherein said step of increasing the voltage at said first plate of said first capacitor comprises the step of switching the first plate of said first capacitor from said low voltage supply rail to said high voltage supply rail.

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## United States Patent [19]

Chern

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[45] Date of Patent: Jun. 30, 1992

## [54] HIGH EFFICIENCY CHARGE PUMP

[75] Inventor: Wen-Foo Chern, Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[21] Appl. No.: 716,697

[22] Filed: Jun. 17, 1991

[51] Int. Cl.<sup>5</sup> ..... G05F 3/08

[52] U.S. Cl. .... 307/296.2; 307/296.1;

307/296.8; 307/304

[58] Field of Search ..... 307/296.2, 296.1, 296.8,  
307/304

## [56] References Cited

## U.S. PATENT DOCUMENTS

4,307,333	12/1981	Hargrove	307/296.2
4,740,715	4/1988	Okada	307/296.2
4,935,644	6/1990	Tsujimoto	307/296.2
4,961,007	10/1990	Kumanaya et al.	307/296.2
5,029,282	7/1991	Ito	307/296.8

## OTHER PUBLICATIONS

Y. Nakagome, et al., A 1.5V Circuit Technology for 64Mb DRAMs, *IEEE* 1990 Symposium on VLSI Circuits, Feb., 1990, pp. 17-18.

Y. Nakagome, et al., An Experimental 1.5-V 64-Mb

DRAM, *IEEE Journal of Solid State Circuits*, vol. 26, No. 4, Apr., 1991, pp. 465-472.

Primary Examiner—John S. Heyman

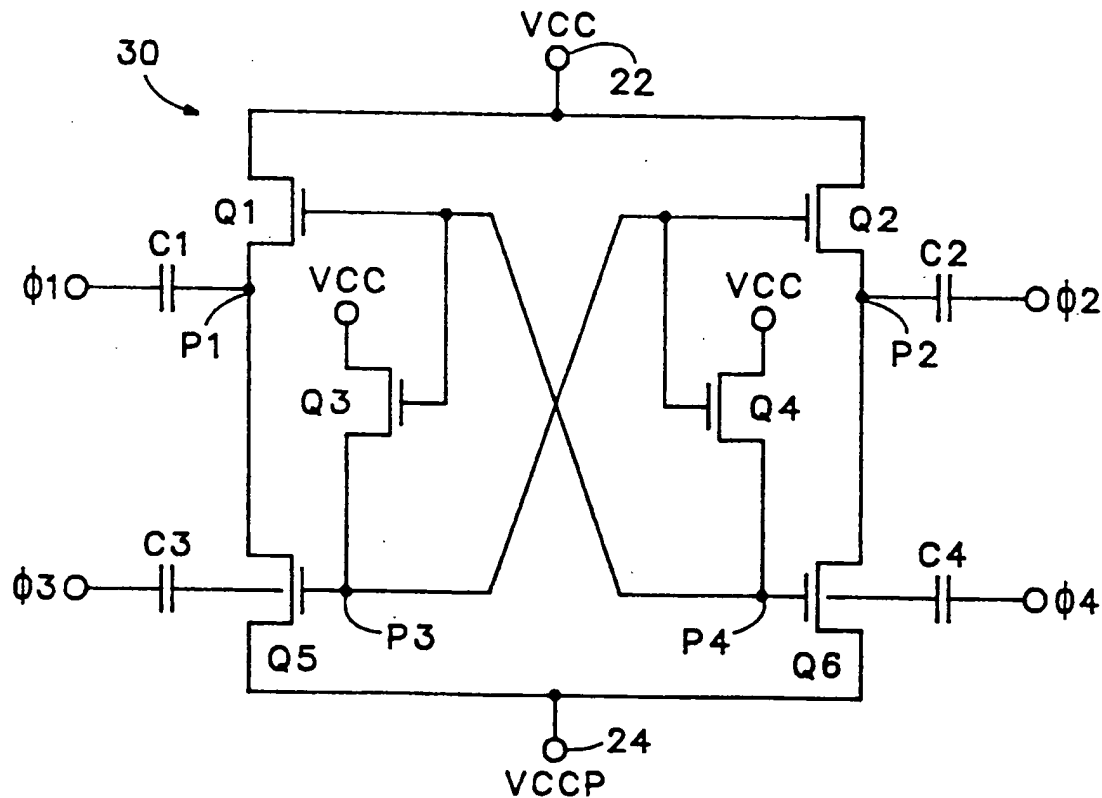
Assistant Examiner—Scott A. Ouellette

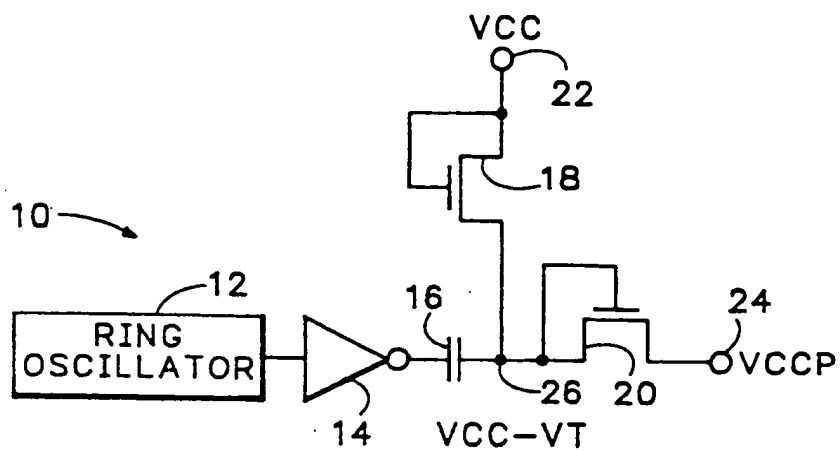
Attorney, Agent, or Firm—Marger, Johnson, McCollom & Stolowitz

## [57] ABSTRACT

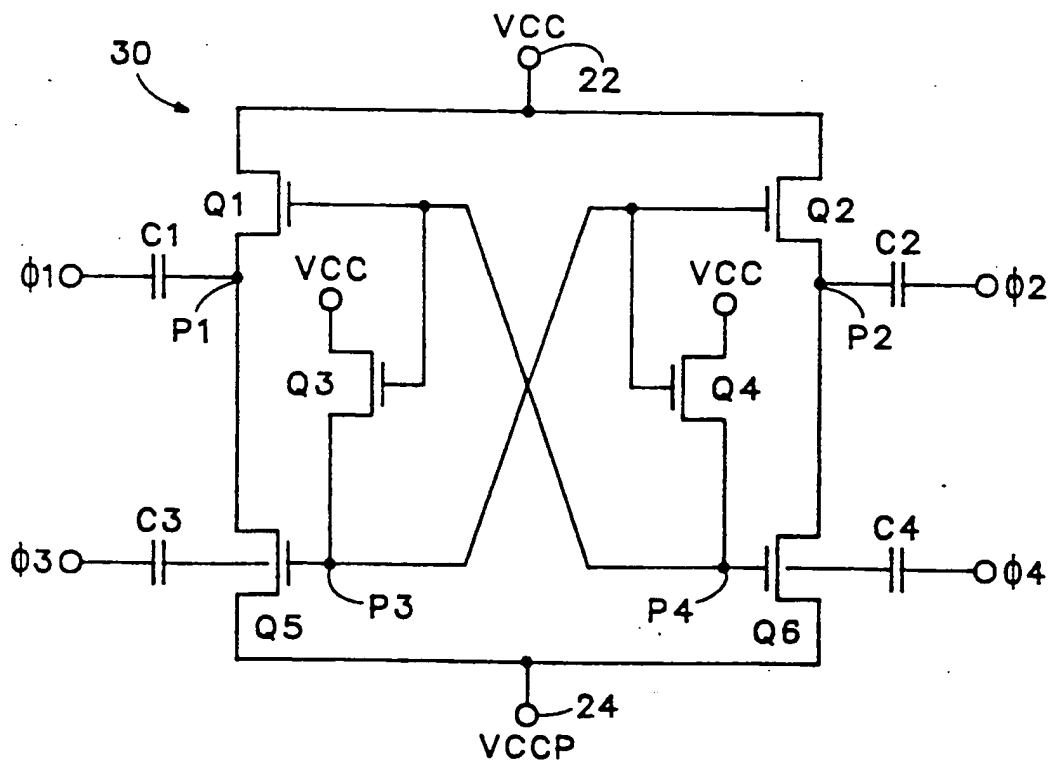
A high efficiency charge pump includes first and second charging transistors for delivering current to a substrate or well and first and second capacitors respectively coupled to the first and second charging transistors. A control circuit coupled to the first and second charging transistors discharges the first capacitor through the first charging transistor and precharges the second capacitor during a first half-cycle of a ring oscillator output signal. The control circuit discharges the second capacitor through the second charging transistor and precharges the first capacitor during a second half-cycle of the ring oscillator output signal. The control circuit also includes first and second symmetrical halves respectively coupled to third and fourth capacitors. The first, second, third, and fourth capacitors are energized by a four-phase clock signal.

23 Claims, 6 Drawing Sheets

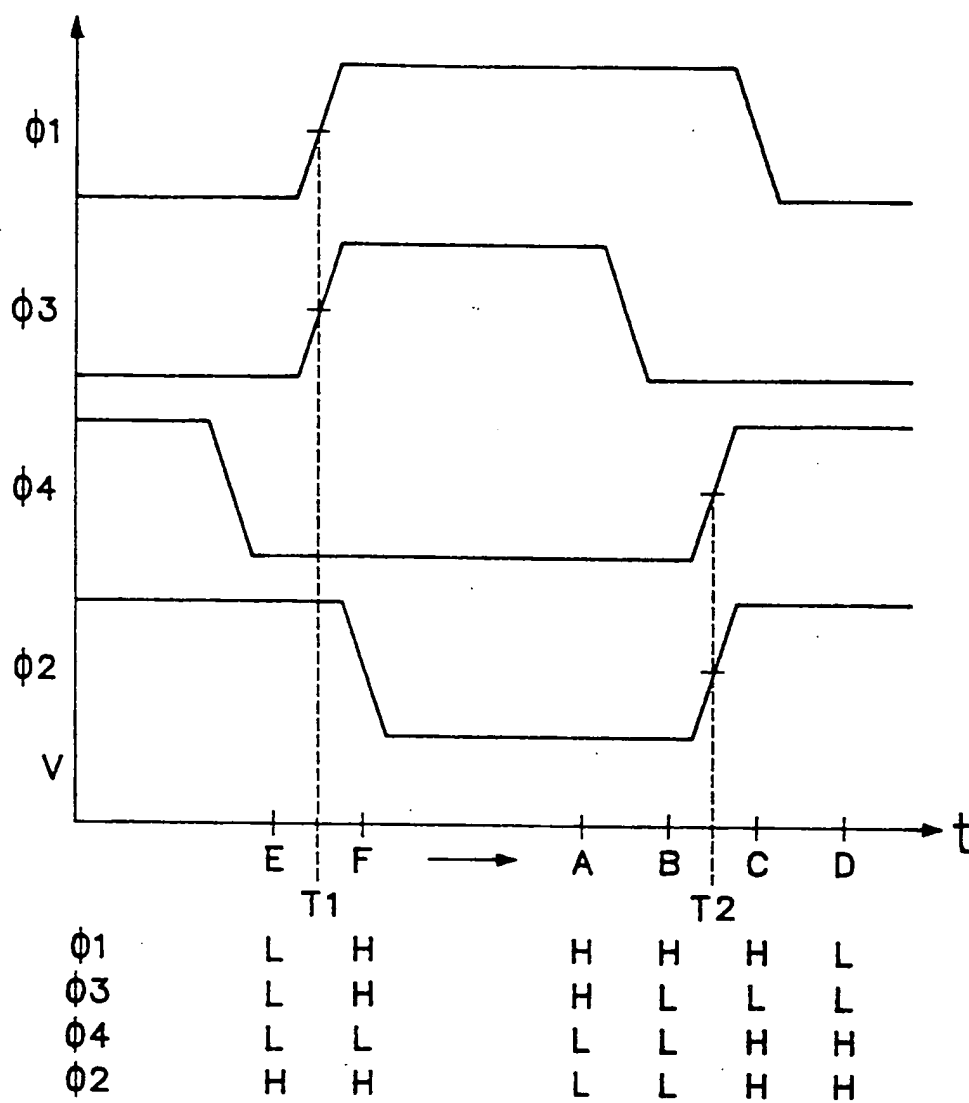




*FIG. 1*  
PRIOR ART



*FIG. 2*

*FIG. 3*

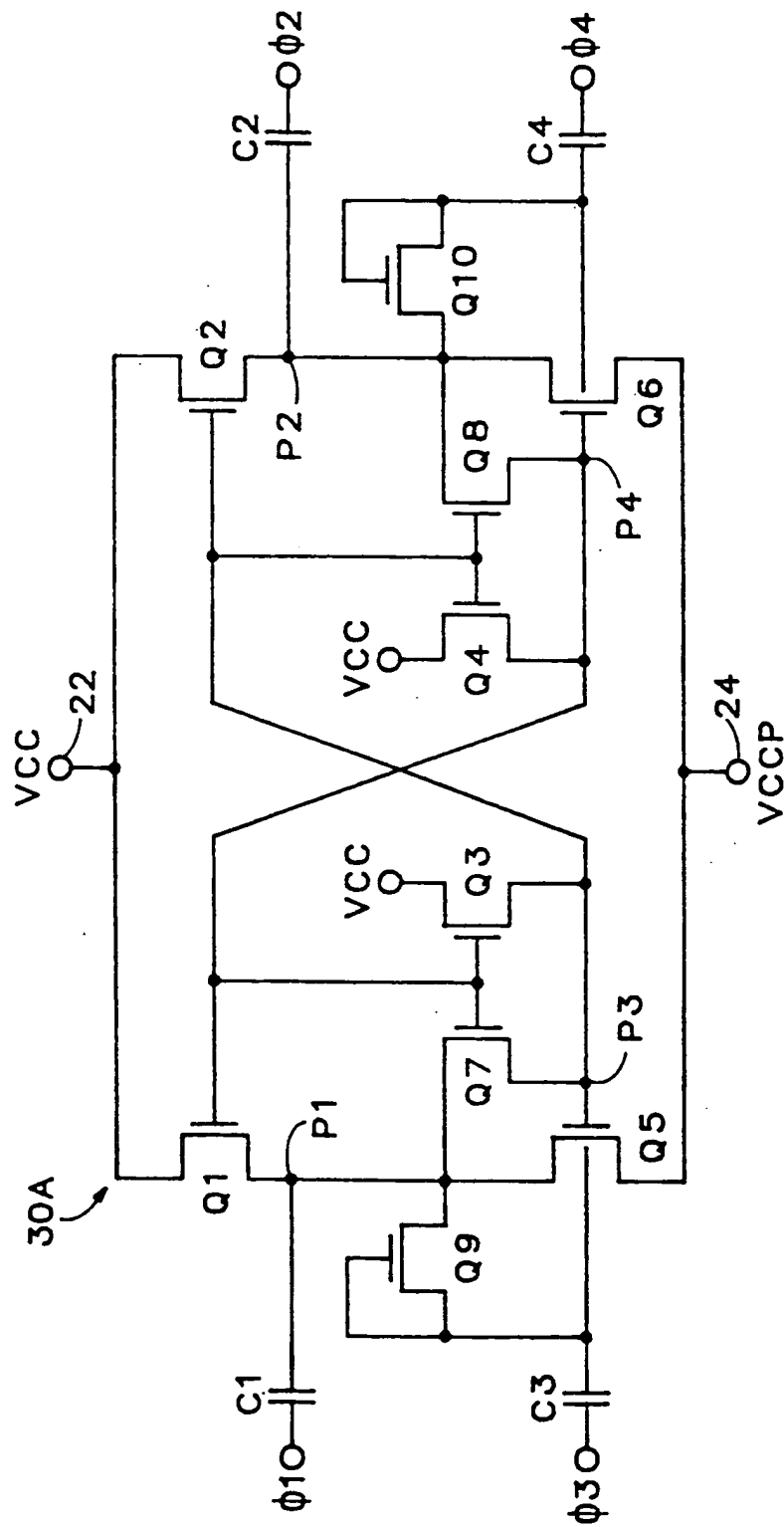


FIG. 4



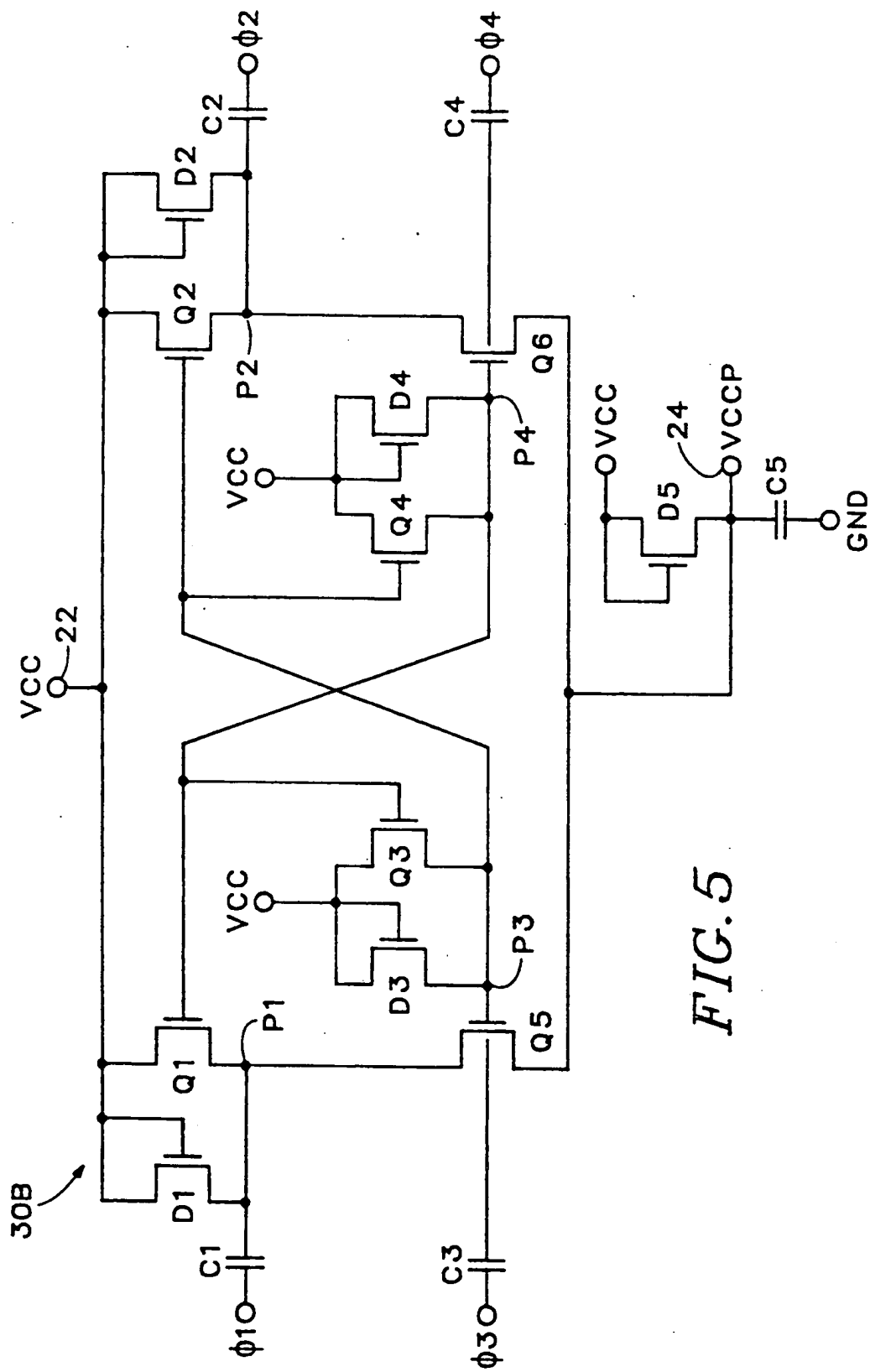


FIG. 5

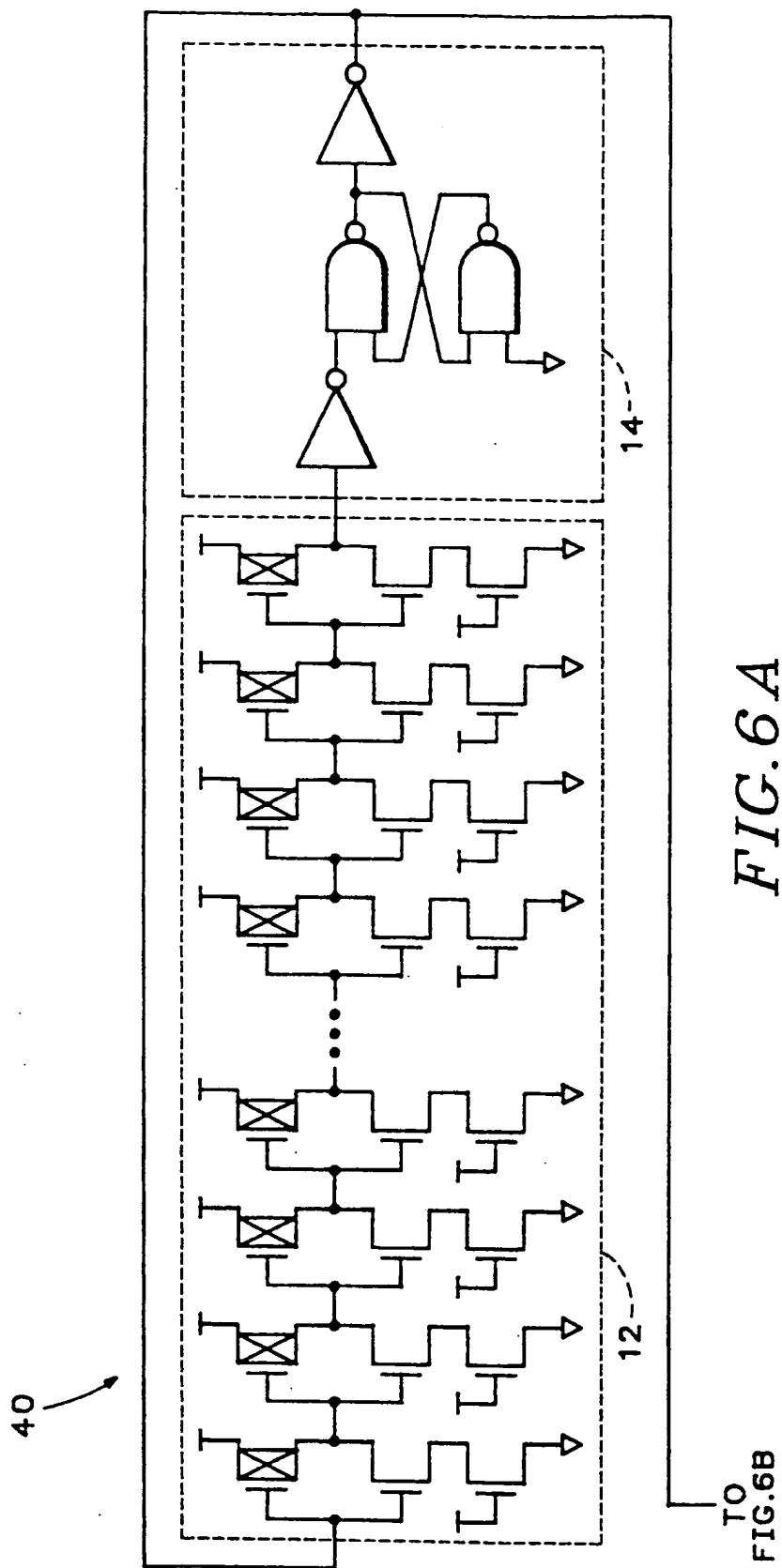
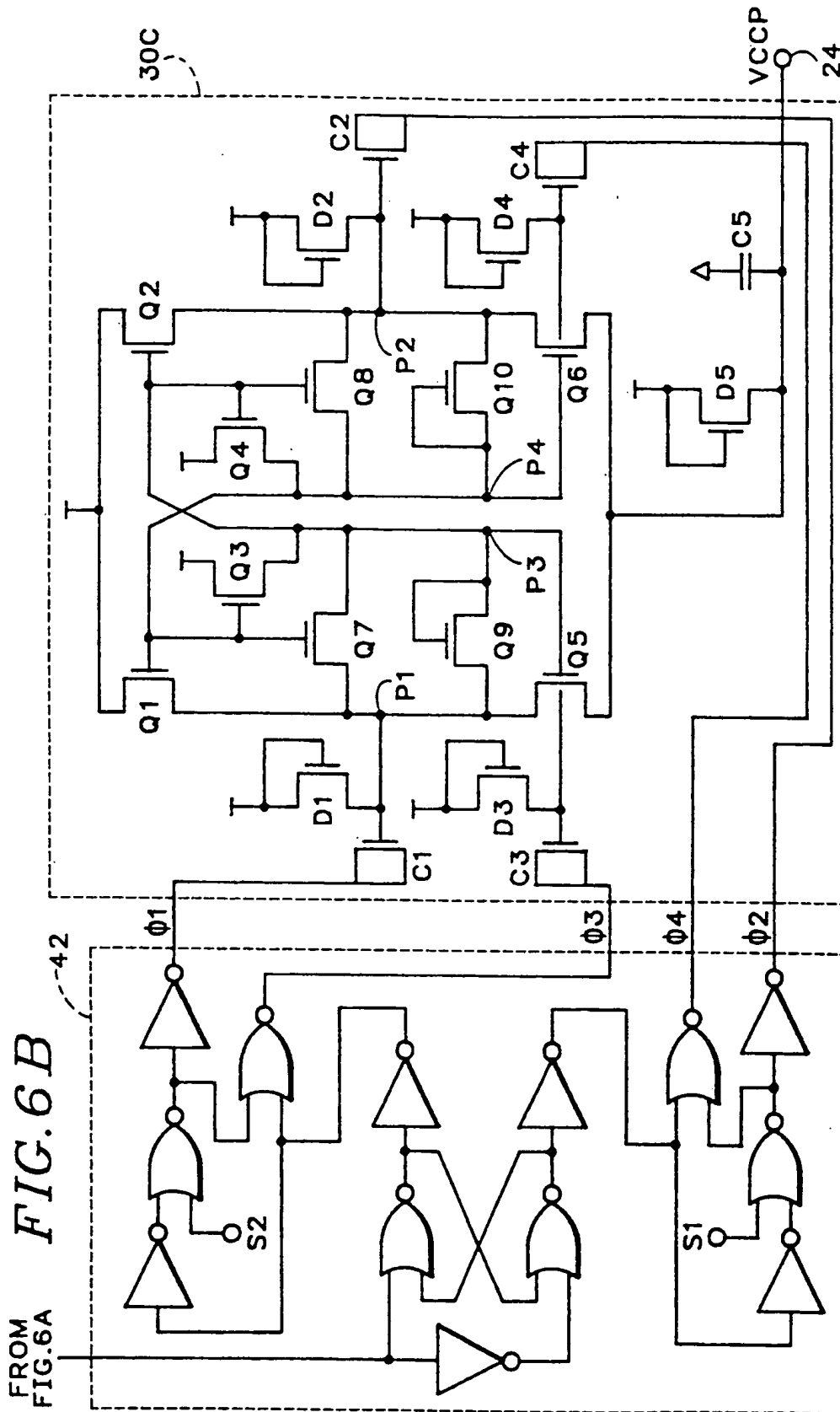


FIG. 6A



## HIGH EFFICIENCY CHARGE PUMP

### BACKGROUND OF THE INVENTION

This invention pertains to charge pumps for biasing a semiconductor substrate, well, or the like, and more particularly, to a method and apparatus for efficiently, and therefore more quickly, biasing the substrate or well to a final desired voltage.

Charge pumps are well known in the art as an on-chip voltage generator capable of providing a voltage more positive than the most positive external supply voltage and/or negative voltage in the absence of a negative external supply voltage. The advantages of charge pumps are also well known in the art such as providing a bias voltage for the substrate of an integrated circuit or N-type and P-type wells, or for providing greater output voltage swings, among other advantages.

Most charge pumps comprise some variation of the basic charge pump 10 shown in the schematic diagram of FIG. 1. The basic charge pump 10 configuration includes a ring oscillator 12 that provides a square wave or pulse train having voltage swings typically between ground and the most positive external power supply voltage, VCC. An inverter 14, buffer amplifier, or Schmitt trigger circuit may be used to sharpen the edges of the oscillating output signal of the ring oscillator 12. A capacitor 16 is discharged into the substrate 24 through diode-connected transistors 18 and 20. (Typically the drain and gate of a diode-connected transistor are coupled together to form the anode of a diode and the source forms the cathode of the diode.) Transistor 18 is coupled to the external power supply voltage, VCC, at terminal 22. When the ring oscillator 12 produces a voltage close to ground, circuit node 26 is approximately at the voltage of the power supply minus a transistor threshold voltage,  $VCC - VT$ . When the ring oscillator 12 produces a voltage close to VCC, the incremental charge on the capacitor 16 is delivered to the substrate 24. Capacitor 16 is prevented from discharging to any other circuit node by the reverse bias on diode-connected transistors 18 and 20.

In the charge pump 10, one pulse of current is delivered to the substrate 24 for every clock cycle of the ring oscillator. Therefore, charge pump 10 has an active half-cycle in which current is delivered to the substrate 24, and the charge asymptotically reaches the final desired voltage. However, charge pump 10 also has an inactive half-cycle in which capacitor 16 is precharged for the next active half-cycle. Although this inactive half-cycle is necessary to precharge the capacitor 16, no current is delivered to the substrate or well 24, which delays the attainment of the final desired voltage. In addition, the voltage across capacitor 16 is limited to  $VCC - VT$  due to the voltage drop across transistor 18.

In most integrated electronic circuits, such as a memory chip, it is desirable that the final voltage at the substrate or well be reached as quickly as possible. Proper device functions and attributes, such as the integrity of stored data, cannot be guaranteed until the substrate or well has reached the final value. Therefore, what is desired is a charge pump that more efficiently delivers current to a substrate or well in order to more quickly achieve a desired level of voltage bias.

### SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method and apparatus that can be fabricated

on a semiconductor integrated circuit for efficiently delivering charge to a semiconductor substrate, well, or the like.

It is another object of the present invention to quickly bias the semiconductor substrate or well of an integrated circuit such that the guaranteed circuit performance can be more quickly achieved.

It is still another object of the present invention to inject two current pulses into the substrate or well for each cycle of the ring oscillator output signal.

It is still another object of the present invention to increase the voltage across the charging capacitors of the charge pump, and thus the available charge that is delivered to the substrate or well.

It is an advantage of the present invention that a circuit embodying the principles of the invention is easily fabricated in an integrated circuit without occupying excessive die area.

It is another advantage of the present invention that the size of the charging transistors necessary to bias a given substrate or well can be reduced.

According to the present invention, a high efficiency charge pump includes first and second charging transistors for delivering current to a substrate or well and first and second capacitors respectively coupled to the first and second charging transistors. A control circuit coupled to the first and second charging transistors discharges the first capacitor through the first charging transistor and precharges the second capacitor during a first half-cycle of a ring oscillator output signal. The control circuit discharges the second capacitor through the second charging transistor and precharges the first capacitor during a second half-cycle of the ring oscillator output signal. In a preferred embodiment, the control circuit includes first and second symmetrical halves respectively coupled to third and fourth capacitors. To realize the control function, the first, second, third, and fourth capacitors are energized by a four-phase clock signal.

The foregoing and other objects, features and advantages of the present invention are more readily apparent from the following detailed description of a preferred embodiment that proceeds with reference to the drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a combined block/schematic diagram of a prior art charge pump;

FIG. 2 is a schematic diagram of the charge pump according to the present invention;

FIG. 3 is a combined timing diagram and table illustrating the phase relationship of a four-phase clock coupled to the charge pump of FIG. 2;

FIG. 4 is a schematic diagram of the charge pump of FIG. 2 further including a pair of level maintenance transistors and a pair of incremental charging diodes;

FIG. 5 is a schematic diagram of the charge pump of FIG. 2 further including five diode voltage clamps; and

FIGS. 6A-6B form a detailed schematic diagram of a complete charge pump system according to the present invention including a ring oscillator and a four-phase clock generator.

### DETAILED DESCRIPTION

The following detailed description describes an N-channel charge pump for generating a positive voltage greater than the voltage of an external positive power

supply, VCC. A positive voltage is desirable for biasing an N-type substrate or well. It is apparent to those skilled in the art that a P-channel version of the charge pump can be constructed to generate a negative voltage for biasing a P-type substrate or well to a negative voltage in the absence of an external negative supply voltage. After the N-channel charge pump is described, the desirable changes to the circuit configuration for the P-channel charge pump are described.

Referring now to FIG. 2, the basic circuit configuration of a high efficiency charge pump 30 includes transistors Q1-Q6. Each transistor is desirably an N-channel field-effect transistor ("FET") having a gate, a first current node (drain), and a second current node (source). Since an FET is typically a symmetrical device, the designation of "source" and "drain" is only possible once a voltage is impressed on the terminals. Charge pump 30 further includes capacitors C1-C4 and an output terminal 24 for biasing a semiconductor substrate or well. The drains of transistors Q1-Q4 are coupled together and to a source of positive supply voltage, VCC, at terminal 22. The value of VCC is typically five volts, or about three volts for highly integrated, sub-micron circuits and systems. In charge pump 30, the source of transistor Q1 and the drain of transistor Q5 are coupled together and to one end of capacitor C1 at circuit node P1. The other end of capacitor C1 receives a first clock signal, designated  $\phi 1$ . The source of transistor Q2 and the drain of transistor Q6 are coupled together and to one end of capacitor C2 at circuit node P2. The other end of capacitor C2 receives a second clock signal, designated  $\phi 2$ . The source of transistor Q3 and the gates of transistors Q2, Q4, and Q5 are coupled together and to one end of capacitor C3 at circuit node P3. The other end of capacitor C3 receives a third clock signal, designated  $\phi 3$ . The source of transistor Q4 and the gates of transistors Q1, Q3, and Q6 are coupled together and to one end of capacitor C4 at circuit node P4. The other end of capacitor C4 receives a fourth clock signal, designated  $\phi 4$ . The sources of transistors Q5 and Q6 are coupled together and to output terminal 24 that is coupled to the substrate or well. Transistors Q5 and Q6 are charging transistors that deliver current to the substrate or well. The substrate or well is ultimately biased to a voltage, VCCP, that is more positive than the external power supply voltage VCC. The final value of the boosted voltage VCCP is theoretically equal to  $2 VCC - VT$ .

The timing relationships of the individual clock signals  $\phi 1$ - $\phi 4$  that comprise a four-phase clock signal are shown in FIG. 3. Only one cycle of the waveform is shown. Clock signals  $\phi 1$  and  $\phi 3$  each have a rising edge that occurs simultaneously at time instant T1. Clock signal  $\phi 2$  has a falling edge that occurs after time instant T1, and clock signal  $\phi 4$  has a falling edge that occurs before time instant T1. Clock signals  $\phi 2$  and  $\phi 4$  each have a rising edge that occurs simultaneously at time instant T2. Clock signal  $\phi 1$  has a falling edge that occurs after time instant T2, and clock signal  $\phi 3$  has a falling edge that occurs before time instant T2. The designations A, B, C, D, E, and F in FIG. 3 refer generally to time intervals wherein the clock signals are in one of six possible logic states. This is also illustrated by the table below the time designations. For example, during time interval A, clocks signals  $\phi 1$  and  $\phi 3$  are in a logic high state (H), and clock signals  $\phi 2$  and  $\phi 4$  are in a logic low state (L).

The operation of charge pump 30 is discussed below with reference to FIGS. 2-3. To understand the operation of the charge pump 30 of FIG. 2, assume as an initial condition that circuit nodes P1-P4 and the output terminal 24 are clamped to the external positive power supply voltage minus a transistor threshold voltage ( $VCC - VT$ ). (The clamping function provided by diodes D1-D5 is discussed in greater detail below with reference to FIG. 5.) Further assume that the four-phase clock signal is in the logic state associated with time interval A. In the transition between time intervals A and B, clock signal  $\phi 3$  changes state from a logic high to a logic low. The voltage on circuit node P3 changes from  $VCC - VT$  to a voltage below  $VCC - VT$ . Transistor Q5 turns off, isolating circuit node P1 from the output terminal 24. Transistors Q2 and Q4 also turn off, isolating circuit nodes P2 and P4 from VCC.

In the transition between time intervals B and C, clock signals  $\phi 2$  and  $\phi 4$  each change state from a logic low to a logic high. The voltage on circuit nodes P2 and P4 increases to a voltage slightly less than  $2 VCC - VT$ . The voltage is slightly less due to charge sharing with parasitic capacitances associated with each circuit node. Transistor Q6 turns on, discharging capacitor C2 and injecting current into the substrate or well through output terminal 24. Consequently, the voltage on circuit node P2 leaks down to the voltage on the output terminal 24, initially  $VCC - VT$ . Transistors Q1 and Q3 also turn on, precharging circuit nodes P1 and P3 to VCC. Transistor Q5 is off since the voltage on circuit nodes P1 and P3 is equal to VCC, and the output terminal 24 is at about  $VCC - VT$ . Neither of the current nodes of transistor Q5 are less than the gate by an amount more than the transistor threshold voltage, VT, a necessary condition for current conduction.

In the transition between time intervals C and D, clock signal  $\phi 1$  changes state from a logic high to a logic low, which establishes a potential across capacitor C1 of approximately equal to VCC. Circuit node P1 stays high at a value also equal to VCC, since the first and second current nodes are at a voltage of about VCC, while the gate is at a voltage slightly less than  $2 VCC - VT$ .

In the transition between time intervals D and E, clock signal  $\phi 4$  changes state from a logic high to a logic low, and the voltage on circuit node P4 changes from about  $2 VCC - VT$  to  $VCC - VT$ . Transistor Q6 turns off, isolating circuit node P2 from the output terminal 24. Transistors Q1 and Q3 also turn off, isolating circuit nodes P1 and P3 from VCC.

In the transition between time intervals E and F, clock signals  $\phi 1$  and  $\phi 3$  each change state from a logic low to a logic high. The voltage on circuit nodes P1 and P3 increases to a voltage slightly less than  $2 VCC$ . Transistor Q5 turns on, discharging capacitor C1 and injecting current into the substrate or well through output terminal 24. Consequently, the voltage on circuit node P1 leaks down to the voltage on the output terminal. Transistors Q2 and Q4 also turn on, precharging circuit nodes P2 and P4 to VCC. Transistor Q6 is off since the voltage on circuit nodes P2 and P4 is equal to VCC, and the output terminal is at about  $VCC - VT$ .

In the final transition between time interval F and the original time interval A, clock signal  $\phi 2$  changes state from a logic high to a logic low, which establishes a potential across capacitor C2 of approximately equal to VCC. Circuit node P2 stays high at a value also equal to

VCC, since the first and second current nodes are at a voltage of about VCC, while the gate is at a voltage slightly less than 2 VCC. The process is repeated in sequence until the final voltage is reached, approximately equal to  $2 VCC - VT$ .

Thus, the basic operation of the charge pump 30 begins by providing first and second charging transistors Q5 and Q6 and first and second capacitors C1 and C2. The sources of the charging transistors Q5 and Q6 are coupled to the substrate or well. Transistors Q5 and Q6 alternatively deliver current pulses to the substrate or well through output terminal 24. First and second capacitors C1 and C2 are respectively coupled to the charging transistors. Capacitors C1 and C2 provide the charge storage that is converted to a charge pulse when the capacitors are discharged. Thus, during the first half-cycle of the four-phase clock signal, the first capacitor C1 is discharged through the first charging transistor Q5 and the second capacitor C2 is precharged for the next half-cycle. Consequently, during the second half-cycle of the four-phase clock signal, the second capacitor C2 is discharged through the second charging transistor Q6 and the first capacitor C1 is precharged. As the alternative current pulses are delivered to the substrate or well, two for each clock cycle, the voltage on the substrate or well moves from the initial voltage of  $VCC - VT$  to the final desired voltage of  $2 VCC - VT$ . Charge pump 30 is more efficient than charge pump 10 shown in FIG. 1. In charge pump 10, node 26 can attain a maximum voltage of  $VCC - VT$ , whereas in charge pump 30, nodes P1 and P2 can attain a maximum voltage of VCC. Therefore, an incremental charging voltage of VT delivers an incremental charge to the substrate or well that is not available in the prior art. Thus, the substrate or well reaches the final voltage bias level more quickly.

Referring now to FIG. 4, charge pump 30A includes a pair of level maintenance transistors Q7 and Q8 and a pair of incremental charging transistors Q9 and Q10 not shown in the basic charge pump 30. The gate of the first level maintenance transistor Q7 is coupled to the gate of the transistor Q1, the drain of the first level maintenance transistor Q7 is coupled to the drain of transistor Q5, and the source of the first level maintenance transistor Q7 is coupled to the gate of transistor Q5. The gate of the second level maintenance transistor Q8 is coupled to the gate of the transistor Q2, the drain of the first level maintenance transistor Q8 is coupled to the drain of transistor Q6, and the source of the first level maintenance transistor Q8 is coupled to the gate of transistor Q6. Charge pump 30A also includes a first incremental charging diode-connected transistor Q9 coupled between the gate and the drain of transistor Q5 and a second incremental charging diode-connected transistor coupled between the gate and the drain of transistor Q6.

Transistor Q7 turns on whenever transistors Q1, Q3, and Q6 turn on. Similarly, transistor Q8 turns on whenever transistors Q2, Q4, and Q5 turn on. Transistor Q7 maintains the gate and the source of transistor Q5 at the same potential such that the gate-to-source voltage is zero, and the transistor is off. The source of transistor Q5, which is also the output terminal 24, is typically more positive than the gate or drain as the substrate or well becomes more positively biased. Since transistor Q5 is off when transistor Q6 is on during one half-cycle, charge is delivered only to the substrate or well, and is not discharged from the substrate or well through tran-

sistor Q5. Likewise, transistor Q8 maintains the gate and source of transistor Q6 at the same potential such that the gate-to-source voltage is zero, and the transistor is off. The source of transistor Q6 is also typically more positive than the gate or drain as the substrate or well becomes more positively biased. Since transistor Q6 is off when transistor Q5 is on during the other half-cycle, charge is delivered only to the substrate or well, and is not discharged from the substrate or well through transistor Q6.

Transistors Q7 and Q8 further guarantee that transistors Q5 and Q6 remain off during the precharge cycle. The voltage between nodes P1 and P3, and the voltage between nodes P2 and P4 are clamped to a voltage less than VT by the action of transistors Q7 and Q8. This assures that transistors Q5 and Q6 do not turn on and rob charge from the substrate or well.

Diode-connected transistors Q9 and Q10 contribute incrementally to the charge delivered to the substrate or well by about 1% to 5%. Diode-connected transistor Q9 leaks the charge off of circuit node P3 onto the drain of charging transistor Q5. Circuit node P3 typically charges to a voltage of about 2 VCC during one half-cycle. This voltage is necessary to turn on transistor Q5 and discharge capacitor C1 to the substrate or well. However, the discharge through transistor Q5 typically takes less than a full half-cycle. The remaining charge on circuit node P3 is no longer needed for any circuit function and can itself be discharged to the substrate or well through transistors Q9 and Q7. Similarly, transistor Q10 provides the same discharge function for the excess charge stored on circuit node P4 when transistor Q6 is on and transistor Q5 is off. Capacitor C5 is coupled from the output terminal 24 to ground to help regulate and smooth out the voltage on the substrate or well once the final desired voltage is achieved.

Referring now to FIG. 5, charge pump 30B includes five diode clamps D1-D5 not shown in the basic charge pump 30 for voltage clamping appropriate circuit nodes. Each diode clamp is a diode-connected FET. Voltage clamps D1-D4 each have a power node (anode) coupled to the positive supply voltage VCC and a clamping node (cathode) respectively coupled to the end of capacitors C1-C4 not coupled to the four-phase clock. A fifth voltage clamp D5 has a power node coupled to VCC and a clamping node coupled to the output terminal 24.

To improve the efficiency of the basic charge pump 30 it is desirable that circuit nodes be initially clamped to voltages that are as close to the final voltage on that circuit node as possible. Initially, the most positive voltage available in the circuit is VCC. Therefore circuit nodes P1-P4 and VCCP are all clamped to a voltage equal to (i.e. not more negative than)  $VCC - VT$ . Starting at this positive voltage eliminates at least one clock cycle delay in obtaining the final desired output voltage at terminal 24. After one clock cycle is passed, the diode clamps D1-D5 turn off, since all circuit nodes have reached at least a voltage equal to VCC. Thus, diode clamps D1-D4 ensure that circuit nodes P1-P4 are precharged properly to  $VCC - VT$ , and the output is also precharged to  $VCC - VT$ . The charge pump 30 only has increase the output voltage from the initial value of  $VCC - VT$  to VCCP. Without the diode clamps D1-D5, the output voltage is initially at ground. Thus, the diode clamps D1-D5 provide a "head start" on charging the substrate or well, which minimizes charging time to the final desired voltage.

Referring now to FIGS. 6A and 6B, a complete charge pump system 40 is shown including a ring oscillator 12, conditioning circuit 14, four-phase clock generator 42, and a charge pump circuit 30C, including the combination of all clamps and additional transistors of charge pumps 30, 30A, and 30B. For simplicity, the positive voltage VCC in FIGS. 6A and 6B is depicted in the conventional manner as a short horizontal solid line. The ring oscillator 12 conventionally includes a number of serially-connected inverter stages. Each inverter stage includes a P-channel FET and two N-channel FETs. Alternatively, each inverter stage can have two serially-connected P-channel FETs and one N-channel FET, or simply one N-channel FET and one P-channel FET. The exact circuit design for the inverter stage depends upon the delay desired for each stage, and consequently, the final operating frequency of the ring oscillator 12. Conditioning circuit 14 includes two inverters and two cross-coupled NAND gates for providing an output signal with sharp-edge transitions between the logic low and high states. The output of the conditioning circuit 14 is fed back to the input of the ring oscillator 12 to start and maintain the oscillation. Conditioning circuit 14 serves to buffer the drive of the ring oscillator 12. The conditioning circuit 14 can be completely eliminated if ring oscillator 12 has sufficient drive capability. The four-phase clock generator 42 receives a one-phase clock signal from the ring oscillator 12 and conditioning circuit 14, and generates the four-phase clock signal including component clock signals  $\phi 1$ - $\phi 4$  having the timing characteristics shown in FIG. 3. The four-phase clock generator 42 creates clock signals  $\phi 1$ - $\phi 4$  by providing delay paths of unequal for the rising edge and the falling edge of the basic one-phase clock signal. The unequal delay paths are provided for an inverted and non-inverted half to create a total of four clock signals. It can be shown by those skilled in the art that clock generator 42 creates the clock signals shown in FIG. 3. It is also appreciated by those skilled in the art that many other such circuits for generating a four-phase clock signal with the characteristics shown in FIG. 3 are possible by an appropriate combination of logic elements.

Charge pump 30C is essentially the combination of all circuit elements contained in the previously discussed charge pumps 30, 30A, and 30B. The notable difference is that capacitors C1-C4 are shown as capacitor-connected transistors. A capacitor-connected transistor is a transistor wherein the gate forms one plate of a capacitor, and the drain and source are shorted together to form the other plate of the capacitor. The following values and W/L ratios are desirable for charge pump 30: (Note: W/L ratios are expressed in terms of the minimum feature size of the photolithographic process that is used. For example, in a 1 micron process, a designation of 15/1 refers to 15 microns by 1 micron. It should also be noted that the following W/L ratios are desirable for a particular application. These values can change for other applications and are dependent upon the operating frequency of the ring oscillator 12, the amount of charging current desired, as well as other factors.)

Circuit element	W/L ratio or value
Q1	90/1
Q2	90/1
Q3	15/1

-continued

Circuit element	W/L ratio or value
Q4	15/1
Q5	340/1
Q6	340/1
Q7	20/1
Q8	20/1
Q9	10/1
Q10	10/1
D1	12/1
D2	12/1
D3	6/1
D4	6/1
D5	200/1
C1	120/200
C2	120/200
C3	120/25
C4	120/25
C5	300 pF

In the above table, it is apparent that the charging transistors Q5 and Q6, capacitors C1, C2, C5, and diode clamp D5 are desirably made large in comparison to other circuit elements. The reason for the large size of these circuit elements is that they are involved in transferring large current pulses to the substrate or well. The next-largest circuit elements are transistors Q1 and Q2, and capacitors C3 and C4. The reason for the comparatively large size of these circuit elements is that capacitors C3 and C4 must have sufficient capacitance to precharge circuit nodes P1 and P2, but these circuit nodes must be quickly precharged (within one half-cycle of the clock signal).

It has been shown that the charge pump of the present invention is capable of quickly biasing the semiconductor substrate or well of an integrated circuit such that the guaranteed circuit performance can be more quickly achieved. The increase in efficiency is due, in part, to charging circuit nodes P1 and P2 fully to VCC, which increases the total amount of charge delivered to the substrate or well. The basic circuit configuration of the charge pump 30 includes only six transistors and four capacitors and therefore can be easily fabricated in an integrated circuit without occupying excessive die area. The charging transistors necessary to bias a given substrate or well can be reduced by a factor of at least two over the prior art because of the two charging pulses per clock cycle.

An all N-channel substrate pump, wherein all transistors, capacitors, and diodes are formed of N-channel transistors, has been described above for generating a positive voltage more positive than the most positive external power supply voltage. The following changes are desirable to create an all P-channel substrate pump for generating a negative voltage at the output terminal 24 suitable for biasing a P-type substrate, well, or the like. Each transistor Q1-Q10 is ideally replaced with a P-channel FET. Referring to FIGS. 2, 4, or 5, circuit node 22 is coupled to ground instead of VCC. Thus, transistors Q1-Q4, and diode clamps D1-D5 are each coupled at one end to ground instead of VCC. Each of the clock signals retains the relative timing relationships shown in FIG. 3, however in the P-channel version, however each clock signal  $\phi 1$ - $\phi 4$  is inverted in polarity. The final voltage at the output terminal 24 is equal to  $V_T - 2 V_{CC}$ , and is sometimes designated VBB.

Having illustrated and described the principles of my invention in a preferred embodiment thereof, it is apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing

from such principles. I claim all modifications coming within the spirit and scope of the accompanying claims. I claim:

1. A high efficiency charge pump comprising:
  - first and second charging transistors for delivering 5 current to a substrate or well;
  - first and second capacitors having a first node respectively coupled to the first and second charging transistors and a second node for respectively receiving first and second clock signals; 10
  - a control circuit including first and second symmetrical halves coupled to the first and second charging transistors for discharging the first capacitor through the first charging transistor and precharging the second capacitor during a first time interval 15 and for discharging the second capacitor through the second charging transistor and precharging the first capacitor during a second time interval;
  - a third capacitor having a first node coupled to the first symmetrical control circuit half and a second 20 node for receiving a third clock signal; and
  - a fourth capacitor having a first node coupled to the second symmetrical control circuit half and a second node for receiving a fourth clock signal.
2. A high efficiency charge pump as in claim 1 in 25 which
  - the first and third clock signals each have a transition from a first logic state to a second logic state that occurs simultaneously at a first time instant, the 30 second clock signal has a transition from the second logic state to the first logic state that occurs after the first time instant, and the fourth clock signal has a transition from the second logic state to the first logic state that occurs before the first time instant, and 35
  - the second and fourth clock signals each have a transition from the first logic state to the second logic state that occurs simultaneously at a second time instant, the first clock signal has a transition from the second logic state to the first logic state that occurs after the second time instant, and the third 40 clock signal has a transition from the second logic state to the first logic state that occurs before the second time instant.
3. A method for efficiently charging a substrate or 45 well, the method comprising the steps of:
  - providing first and second charging transistors;
  - coupling the first and second charging transistors to the substrate or well for delivering current thereto;
  - coupling first and second capacitors respectively to 50 the first and second charging transistors;
  - discharging the first capacitor through the first charging transistor and precharging the second capacitor during a first time interval;
  - discharging the second capacitor through the second 55 charging transistor and precharging the first capacitor during a second time interval;
  - coupling a third capacitor to a control node of the first charging transistor; and
  - coupling a fourth capacitor to a control node of the 60 second charging transistor.
4. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of: 65
  - providing first, second, third, and fourth clock signals; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.

5. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of:
  - providing first, second, third, and fourth clock signals,
  - the first and third clock signals each having a transition from a first logic state to a second logic state that occurs simultaneously at a first time instant and the second and fourth clock signals each having a transition from the first logic state to the second logic state that occurs simultaneously at a second time instant; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.
6. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of:
  - providing first, second, third, and fourth clock signals,
  - the second clock signal having a transition from a first logic state to a second logic state that occurs after a first time instant, and the fourth clock signal having a transition from the first logic state to the second logic state that occurs before a first time instant,
  - the first clock signal having a transition from the first logic state to the second logic state, that occurs after a second time instant, and the third clock signal having a transition from the first logic state to the second logic state that occurs before a second time instant; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.
7. A high efficiency charge pump comprising:
  - first, second, third, fourth, fifth, and sixth transistors each having a gate, a first current node, and a second current node;
  - first, second, third, and fourth capacitors each having a first node and a second node; and
  - an output terminal for biasing a substrate or well, wherein
  - the first current nodes of the first, second, third, and fourth transistors are coupled together and to a source of supply voltage,
  - the second current node of the first transistor and the first current node of the fifth transistor are coupled together and to the first node of the first capacitor, the second node of the first capacitor receiving a first clock signal,
  - the second current node of the second transistor and the first current node of the sixth transistor are coupled together and to the first node of the second capacitor, the second node of the second capacitor receiving a second clock signal,
  - the second current node of the third transistor and the gates of the second, fourth, and fifth transistors are coupled together and to the first node of the third capacitor, the second node of the third capacitor receiving a third clock signal,
  - the second current node of the fourth transistor and the gates of the first, third, and sixth transistors are coupled together and to the first node of the fourth capacitor, the second node of the fourth capacitor receiving a fourth clock signal, and
  - the second current nodes of the fifth and sixth transistors are coupled together and to the output terminal.



from such principles. I claim all modifications coming within the spirit and scope of the accompanying claims. I claim:

1. A high efficiency charge pump comprising:
  - first and second charging transistors for delivering 5 current to a substrate or well;
  - first and second capacitors having a first node respectively coupled to the first and second charging transistors and a second node for respectively receiving first and second clock signals; 10
  - a control circuit including first and second symmetrical halves coupled to the first and second charging transistors for discharging the first capacitor through the first charging transistor and precharging the second capacitor during a first time interval 15 and for discharging the second capacitor through the second charging transistor and precharging the first capacitor during a second time interval;
  - a third capacitor having a first node coupled to the first symmetrical control circuit half and a second 20 node for receiving a third clock signal; and
  - a fourth capacitor having a first node coupled to the second symmetrical control circuit half and a second node for receiving a fourth clock signal.
2. A high efficiency charge pump as in claim 1 in 25 which
  - the first and third clock signals each have a transition from a first logic state to a second logic state that occurs simultaneously at a first time instant, the 30 second clock signal has a transition from the second logic state to the first logic state that occurs after the first time instant, and the fourth clock signal has a transition from the second logic state to the first logic state that occurs before the first time 35 instant, and
  - the second and fourth clock signals each have a transition from the first logic state to the second logic state that occurs simultaneously at a second time instant, the first clock signal has a transition from the second logic state to the first logic state that 40 occurs after the second time instant, and the third clock signal has a transition from the second logic state to the first logic state that occurs before the second time instant.
3. A method for efficiently charging a substrate or 45 well, the method comprising the steps of:
  - providing first and second charging transistors;
  - coupling the first and second charging transistors to the substrate or well for delivering current thereto;
  - coupling first and second capacitors respectively to 50 the first and second charging transistors;
  - discharging the first capacitor through the first charging transistor and precharging the second capacitor during a first time interval;
  - discharging the second capacitor through the second 55 charging transistor and precharging the first capacitor during a second time interval;
  - coupling a third capacitor to a control node of the first charging transistor; and
  - coupling a fourth capacitor to a control node of the 60 second charging transistor.
4. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of:
  - providing first, second, third, and fourth clock 65 signals; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.

5. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of:
  - providing first, second, third, and fourth clock signals,
  - the first and third clock signals each having a transition from a first logic state to a second logic state that occurs simultaneously at a first time instant and the second and fourth clock signals each having a transition from the first logic state to the second logic state that occurs simultaneously at a second time instant; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.
6. A method for efficiently charging a substrate or well as in claim 3 further comprising the steps of:
  - providing first, second, third, and fourth clock signals,
  - the second clock signal having a transition from a first logic state to a second logic state that occurs after a first time instant, and the fourth clock signal having a transition from the first logic state to the second logic state that occurs before a first time instant,
  - the first clock signal having a transition from the first logic state to the second logic state, that occurs after a second time instant, and the third clock signal having a transition from the first logic state to the second logic state that occurs before a second time instant; and
  - energizing the first, second, third, and fourth capacitors with the respective first, second, third, and fourth clock signals.
7. A high efficiency charge pump comprising:
  - first, second, third, fourth, fifth, and sixth transistors each having a gate, a first current node, and a second current node;
  - first, second, third, and fourth capacitors each having a first node and a second node; and
  - an output terminal for biasing a substrate or well, wherein
    - the first current nodes of the first, second, third, and fourth transistors are coupled together and to a source of supply voltage,
    - the second current node of the first transistor and the first current node of the fifth transistor are coupled together and to the first node of the first capacitor, the second node of the first capacitor receiving a first clock signal,
    - the second current node of the second transistor and the first current node of the sixth transistor are coupled together and to the first node of the second capacitor, the second node of the second capacitor receiving a second clock signal,
    - the second current node of the third transistor and the gates of the second, fourth, and fifth transistors are coupled together and to the first node of the third capacitor, the second node of the third capacitor receiving a third clock signal,
    - the second current node of the fourth transistor and the gates of the first, third, and sixth transistors are coupled together and to the first node of the fourth capacitor, the second node of the fourth capacitor receiving a fourth clock signal, and
    - the second current nodes of the fifth and sixth transistors are coupled together and to the output terminal.

8. A high efficiency charge pump as in claim 7 in which the first, second, third, fourth, fifth, and sixth transistors each comprise an N-channel field-effect transistor.

9. A high efficiency charge pump as in claim 7 in which the first, second, third, fourth, fifth, and sixth transistors each comprise a P-channel field-effect transistor.

10. A high efficiency charge pump as in claim 7 in which the first, second, third, and fourth capacitors each comprise an N-channel, capacitor-connected field-effect transistor.

11. A high efficiency charge pump as in claim 7 in which the first, second, third, and fourth capacitors each comprise a P-channel, capacitor-connected field-effect transistor.

12. A high efficiency charge pump as in claim 7 further comprising:

first, second, third, and fourth voltage clamps each having a power node coupled to the source of supply voltage and a clamping node respectively coupled to the second node of first, second, third, and fourth capacitors; and

a fifth voltage clamp having a power node coupled to the source of supply voltage and a clamping node coupled to the output terminal.

13. A high efficiency charge pump as in claim 7 further comprising first and second level maintenance transistor each having a gate, a first current node, and a second current node, wherein

the gate of the first level maintenance transistor is coupled to the gate of the first transistor, the first current node of the first level maintenance transistor is coupled to the first current node of the fifth transistor, and the second current node of the first level maintenance transistor is coupled to the gate of the fifth transistor, and

the gate of the second level maintenance transistor is coupled to the gate of the second transistor, the first current node of the second level maintenance transistor is coupled to the first current node of the sixth transistor, and the second current node of the second level maintenance transistor is coupled to the gate of the sixth transistor.

14. A high efficiency charge pump as in claim 7 further comprising:

a first incremental charging diode coupled between the gate and the first current node of the fifth transistor; and

a second incremental charging diode coupled between the gate and the first current node of the sixth transistor.

15. A high efficiency charge pump as in claim 7 further comprising a capacitor coupled between the output terminal and ground.

16. A high efficiency charge pump as in claim 7 in which

the first and third clock signals each have a transition from a first logic state to a second logic state that occurs simultaneously at a first time instant, the second clock signal has a transition from the second logic state to the first logic state that occurs after the first instant, and the fourth clock signal has a transition from the second logic state to the first logic state that occurs before the first time instant, and

the second and fourth clock signals each have a transition from the first logic state to the second logic state that occurs simultaneously at a second time instant, the first clock signal has a transition from the second logic state to the first logic state that occurs after the second time instant, and the third clock signal has a transition from the second logic state to the first logic state that occurs before the second time instant.

17. A high efficiency charge pump as in claim 12 in which the first, second, third, fourth, and fifth voltage clamps each comprise an N-channel, diode-connected field-effect transistor.

18. A high efficiency charge pump as in claim 12 in which the first, second, third, fourth, and fifth voltage clamps each comprise a P-channel, diode-connected field-effect transistor.

19. A high efficiency charge pump as in claim 13 in which the first and second level maintenance transistors each comprise an N-channel field-effect transistor.

20. A high efficiency charge pump as in claim 13 in which the first and second level maintenance transistors each comprise a P-channel field-effect transistor.

21. A high efficiency charge pump as in claim 14 in which the first and second incremental charging diodes each comprise an N-channel, diode-connected field-effect transistor.

22. A high efficiency charge pump as in claim 14 in which the first and second incremental charging diodes each comprise a P-channel, diode-connected field-effect transistor.

23. A high efficiency charge pump as in claim 15 in which the value of the capacitor is about 300 picofarads.

\* \* \* \* \*



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## United States Patent [19]

Yamazaki et al.

[11] Patent Number: 5,138,190

[45] Date of Patent: Aug. 11, 1992

## [54] CHARGE PUMP CIRCUIT

[75] Inventors: Akihiro Yamazaki, Sagami-hara;  
Tomotaka Saito, Yokohama, both of  
Japan[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki,  
Japan

[21] Appl. No.: 406,092

[22] Filed: Sep. 12, 1989

## [30] Foreign Application Priority Data

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[51] Int. Cl.<sup>3</sup> ..... H03K 3/01; H03K 19/01[52] U.S. Cl. .... 307/296.5; 307/296.2;  
307/264; 307/482; 365/189.11; 365/226[58] Field of Search ..... 307/296.1, 296.2, 296.5,  
307/264, 304, 482, 578; 365/226, 227, 189.11,  
189.09; 363/60

## [56] References Cited

## U.S. PATENT DOCUMENTS

4,374,357 2/1983 Olesin et al. .... 307/304  
4,631,421 12/1986 Inoue et al. .... 307/296.2  
4,638,182 1/1987 McAdams ..... 307/578  
4,689,495 8/1987 Liu ..... 307/264  
4,916,334 4/1990 Minagawa et al. .... 307/296.5

## OTHER PUBLICATIONS

Fink et al., *Electronics Engineers' Handbook*,  
McGraw-Hill Book Company, pp. 16-16, 1982.J. F. Dickson, "On-Chip High-Voltage Generation in  
MNOS Integrated Circuits Using an Improved VoltageMultiplier Technique", IEEE Journal of Solid-State  
Circuits, vol. SC-11, No. 3, Jun. 1976, pp. 374-378.

Primary Examiner—Edward P. Westin

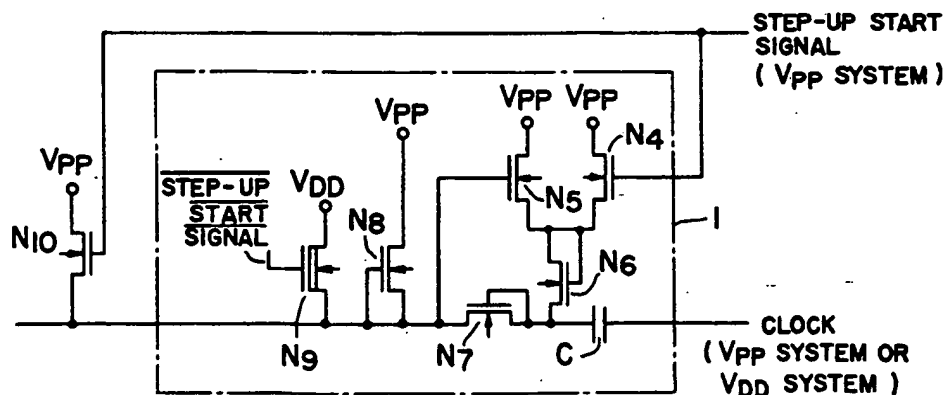
Assistant Examiner—Richard Roseen

Attorney, Agent, or Firm—Foley &amp; Lardner

## [57] ABSTRACT

A charge pump circuit including a step-up section (1) having an output point to which a load is connected, the step-up section (1) having a function to step up an output potential from a predetermined potential lower than a potential ( $V_{PP}$ ) of a power supply to a desired potential higher than the power supply potential ( $V_{PP}$ ), wherein the charge pump circuit comprises initial potential setting switch ( $N_{10}$ ) connected between the power supply and the output point of the step-up section (1), and operative so that it is turned on with the beginning of the step-up operation of the step-up section (1) to propagate the power supply potential ( $V_{PP}$ ) to the output point of the step-up section (1), and that it is turned off in a suitable time. With the beginning of the step-up operation of the step-up section (1), the initial potential setting switch ( $N_{10}$ ) is turned on. As a result, a power supply potential ( $V_{PP}$ ) is propagated to the output point of the step-up section (1). Thus, the output potential is initially set to a relatively high potential obtained by subtracting a voltage drop of the initial potential setting switch ( $N_{10}$ ) from the power supply potential ( $V_{PP}$ ). When the output of the step-up section (1) rises to some extent in a suitable time, the initial potential setting switch ( $N_{10}$ ) is turned off. After that, the step-up section (1) delivers a voltage to the load.

5 Claims, 4 Drawing Sheets



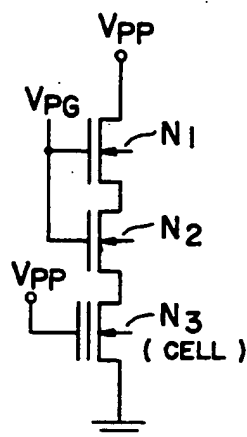


FIG. 1  
PRIOR ART

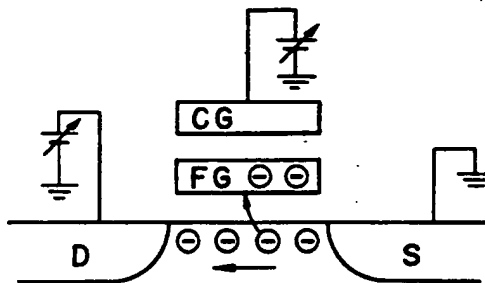


FIG. 2 PRIOR ART

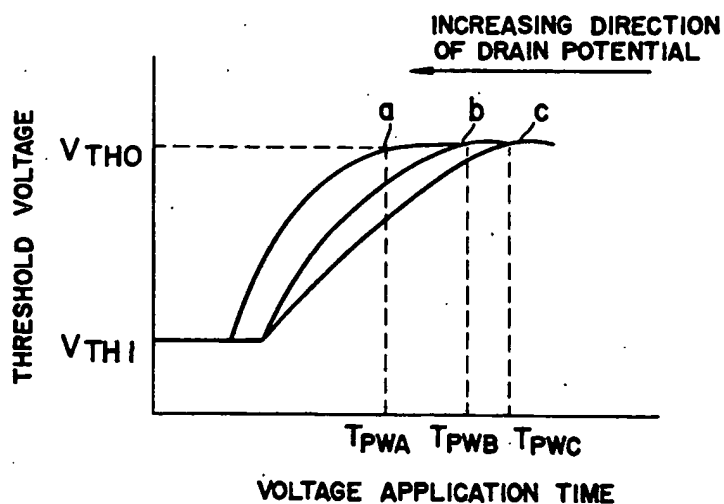


FIG. 3 PRIOR ART

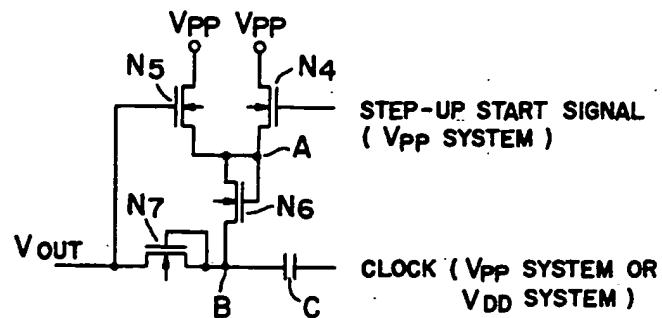


FIG. 4 PRIOR ART

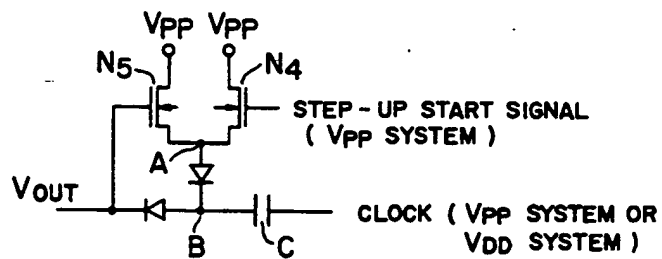


FIG. 5 PRIOR ART

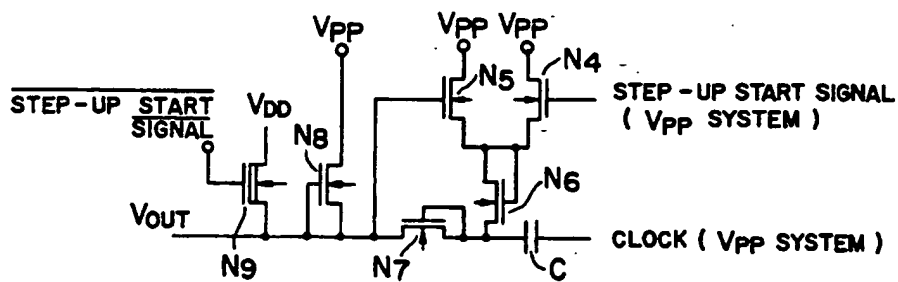


FIG. 6 PRIOR ART

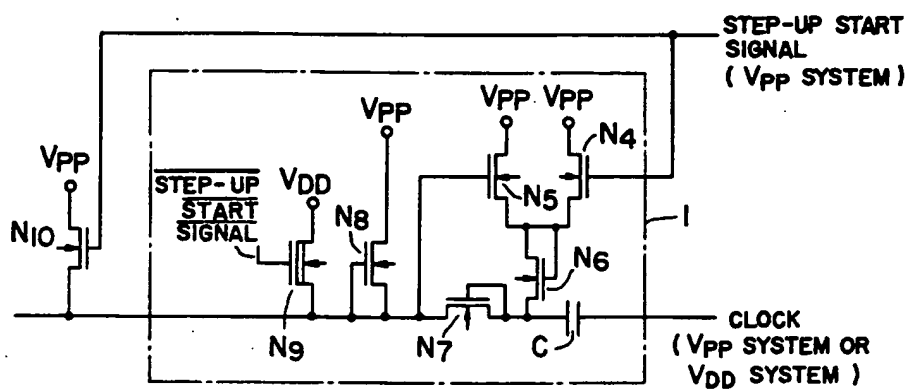


FIG. 7

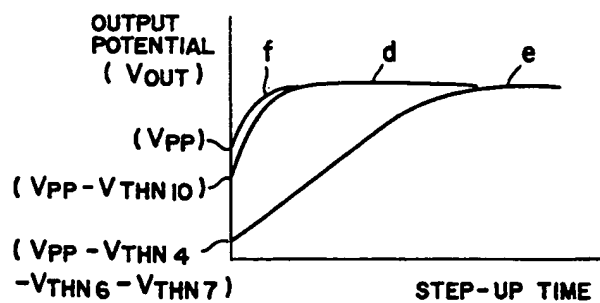


FIG. 8

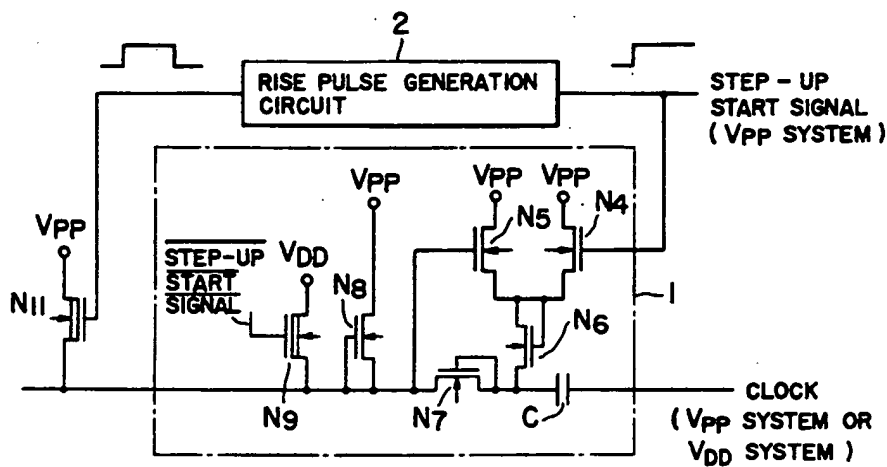


FIG. 9

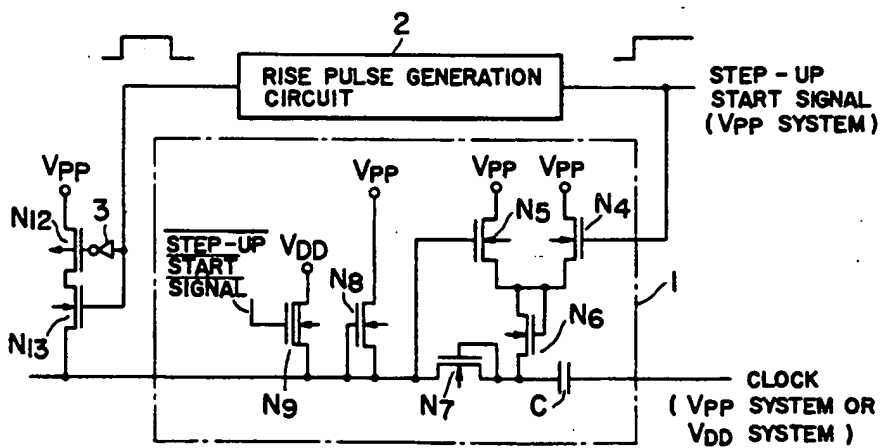


FIG. 10

## CHARGE PUMP CIRCUIT

## BACKGROUND OF THE INVENTION

This invention relates to a charge pump circuit, and more particularly to a charge pump circuit used for driving a semiconductor non-volatile memory having FAMOS (Floating gate avalanche injection MOS) transistors as respective cells.

In an EPROM or a flash EEPROM, etc., having FAMOS transistors as their cells, a high potential called a program potential,  $V_{PP}$ , is externally applied thereto in order to effect a write operation, i.e., to inject electrons into the floating gate of the cell.

An equivalent circuit at the time of write operation of a typical EPROM is shown in FIG. 1. A program potential  $V_{PP}$  is applied to the drain of a cell transistor  $N_3$  through N-channel transistors  $N_1$  and  $N_2$  as shown. In this example, the transistors  $N_1$  and  $N_2$  are called a "write transistor" and a "select transistor", respectively.

When a high potential is applied to the drain D of the cell transistor  $N_3$  and a program potential  $V_{PP}$  is applied to the control gate CG as shown in FIG. 2, electrons are injected into the floating gate FG by the avalanche injection. Cells to which electrons have been injected undergo an increase in the threshold voltage  $V_{TH}$ . Writing into these cells is, thus, performed. On the other hand, cells to which no electrons are injected undergo no change in the threshold voltage  $V_{TH}$ . Thus, the programming of "0" and "1" is carried out in dependency upon difference of the threshold voltage.

Referring to FIG. 3, there is shown a rise characteristic of the threshold voltage  $V_{TH}$  vs. the program voltage application time to the gate of each cell. This figure shows that, when a potential on the drain is taken as a parameter, the rise characteristic of the threshold voltage varies as indicated by the curves c, b and a in order recited according as the potential on the drain is increased. Accordingly, it is considered that the potential on the drain and the write time  $T_{PW}$  (time until the threshold voltage reaches a predetermined threshold voltage  $V_{TH0}$ ) are correlative with each other. Namely, it is preferable that the potential on the drain is high if the write time  $T_{PW}$  is desired to be shortened.

To realize this, the following measure is taken: Since the write operation is conducted through the N-channel transistors  $N_1$  and  $N_2$  as previously shown in FIG. 1, gate control potentials  $V_{PG}$  of these transistors  $N_1$  and  $N_2$  as previously shown in FIG. 1, a gate control potential  $V_{PG}$  for these transistors  $N_1$  and  $N_2$  is set to a value higher than the program potential  $V_{PP}$ , thus preventing voltage drops on these N-channel transistors  $N_1$  and  $N_2$ . To obtain a high potential of the gate control potential  $V_{PG}$ , a charge pump circuit is used. Such a technology is disclosed in, e.g., J. PATHAK et al., "A 19-ns 250 mW CMOS Erasable Programmable Logic Device", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, No. 5, OCTOBER, 1986.

A conventional circuit and its equivalent are shown in FIGS. 4 and 5, respectively. In this example, N-channel MOS transistors  $N_6$  and  $N_7$  equivalently serve as diodes as shown in FIG. 5, respectively. These transistors serve to block a reverse-current and hold a stepped-up voltage.

As seen from FIG. 4, an output potential (initial potential)  $V_{OUT}(0)$  at the time of beginning of the step-up

operation in this charge pump circuit is expressed as follows:

$$V_{OUT}(0) = V_{PP} - V_{THN4} - V_{THN6} - V_{THN7} \quad (1)$$

where  $V_{THN4}$ ,  $V_{THN6}$  and  $V_{THN7}$  represent threshold voltages of the transistors  $N_4$ ,  $N_6$  and  $N_7$ , respectively. This output potential is considerably lower than the applied program potential  $V_{PP}$ . For example, when it is assumed that  $V_{PP} = 12.5$  V and  $V_{THN1} = V_{THN3} = V_{THN} = 2.5$  V, the output potential will become equal to a value expressed below:

$$V_{OUT}(0) = 12.5 - 2.5 \times 3 = 5 \text{ V.}$$

Further, an initial potential  $V_B(0)$  on the point B will become equal to a value expressed below:

$$V_B(0) = V_{PP} - V_{THN4} - V_{THN6} \quad (2)$$

Thereafter, when a clock is delivered to a step-up capacitor C, a potential on the point B is stepped up by to a potential of the clock (e.g., a value corresponding to  $V_{PP}$  where the clock is of the  $V_{PP}$  system). As a result, this potential is passed through the transistor  $N_7$  (subjected to a voltage drop corresponding to  $V_{THN7}$ ) and appears on the output  $V_{OUT}$ . This results in no voltage drop in the transistor  $N_5$ . Thus the program potential appears on the point A as it is and a potential on the point B is expressed as follows

$$V_B = V_{PP} - V_{THN6} \quad (3)$$

This potential is further stepped up by a potential of the clock (e.g., a value corresponding to  $V_{PP}$ ) and is subjected to voltage drop corresponding to the threshold voltage  $V_{THN7}$  of the transistor  $N_7$ , with the result that it appears on the output  $V_{OUT}$ . Accordingly, the output potential  $V_{OUT}$  finally obtained is expressed at the maximum as follows:

$$V_{OUT} = V_{PP} - V_{THN6} + V_{CLOCK} - V_{THN7} \quad (4)$$

wherein  $V_{CLOCK}$  is a potential of the clock (e.g.  $V_{PP}$ ).

It is to be noted that a scheme is practically employed to further provide a transistor  $N_8$  for limiter on the output point, thus limiting the output potential  $V_{OUT}$  to about  $V_{PP} + \alpha$  ( $\alpha$  is a desired step-up value). In addition, a scheme is also employed to deliver an ordinary potential  $V_{DD}$  for read operation through a D (depletion) type transistor  $N_9$  at the time of nonprogramming, thus to stand by readout operation.

The problem with such a conventional charge pump circuit is that the initial value  $V_{OUT}$  of the output potential is lower than the program potential  $V_{PP}$  as given by the equation (1). Inconvenience due to this fact occurs mainly when the load of the step up circuit is large. Namely, since the step up efficiency is poor in the case of a large load, it will take much time for rising of the output as described above. For this reason, write time  $T_{PW}$  may be rather prolonged.

## SUMMARY OF THE INVENTION

An object of this invention is to provide a step up circuit such that an initial value of the output potential is relatively high, and that the rise characteristic is excellent, resulting in no possibility that write time is prolonged even in the case of a large load.



A charge pump circuit according to this invention includes a step-up section having an output point to which a load is connected, the step up section having a function to step up an output potential from a first predetermined potential lower than a potential of a power supply to a desired potential higher than the power supply potential, characterized in that the charge pump circuit includes an initial potential setting switch means connected between the power supply and the output point of the step-up section, and operative so that it is turned on with the beginning of the step-up operation of the step up section to transmit the power supply potential to the output point of the step up section, and operative so that it is turned on with the beginning of the stepping up operation of the step up section to propagate the power supply potential to the output point of the step up section, and is turned off in a suitable time.

In this step up circuit, the initial potential setting switching means is turned on with the beginning of the step up operation, whereby the power supply potential is propagated to the output point of the step-up section. Thus, the output potential is initially set to a relatively high potential obtained by subtracting a voltage drop of the initial potential setting switch means from the power supply potential. By the time an output potential of the step-up section itself rises up to such a relatively high initial set potential, an output from the power supply is delivered to the load through the initial potential setting switch means. For this reason, a load applied to the step-up section is lessened. Thus, the step-up section can rapidly raise the output. When the output of the step-up section rises to some extent in a suitable time, the initial potential setting switch means is turned off. After that, the step up circuit delivers an output to the load. After the output of the step up section rises to a value close to the power supply potential by this turn-off operation, a reverse-current from the charge pump circuit to the power supply is blocked, thus preventing the step-up characteristic from being deteriorated. Accordingly, the step-up characteristic is drastically improved. In addition, since the number of elements added in order to obtain such a conspicuous effect is small, there is no possibility that such elements occupy a broad pattern area, giving hindrance to miniaturization.

#### BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is an equivalent circuit at the time of write operation of a typical EPROM,

FIG. 2 is a view showing the writing principle of a typical EPROM cell,

FIG. 3 is a write characteristic diagram of the typical EPROM cell,

FIG. 4 is a circuit diagram showing an example of a conventional step up circuit,

FIG. 5 is an equivalent circuit of FIG. 4,

FIG. 6 is a circuit diagram showing the conventional circuit of FIG. 4 together with a circuit associated therewith,

FIG. 7 is a circuit diagram showing an embodiment of this invention,

FIG. 8 is a view showing the step up characteristic of the embodiment according to this invention in comparison with that of the conventional example,

FIG. 9 is a circuit diagram showing another embodiment according to this invention, and

FIG. 10 is a circuit diagram showing a further embodiment according to this invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments according to this invention will now be described with reference to the attached drawings.

Initially referring to FIG. 7, there is shown an embodiment of a charge pump circuit according to this invention. The charge pump circuit of this embodiment includes a step-up section 1 of the same configuration as that of the conventional step-up section shown in FIG. 6, and an E (enhancement) type N-channel MOS transistor  $N_{10}$  having a source and a drain connected to the output point of the step-up section 1 and a power source of the program potential  $V_{PP}$  system, respectively. This transistor  $N_{10}$  functions as follows. When an initial step-up start signal ( $V_{PP}$  system) is delivered to its gate, the transistor  $N_{10}$  is turned on, thus setting the output potential  $V_{OUT}$  of the step-up section 1 to an initial potential.

The step-up section 1 includes an N-channel transistor  $N_4$  as a step-up operation start switch, which is turned on in response to an input of the step-up start signal to the gate thereof to output, to the source side, a program potential  $V_{PP}$  applied to the drain thereof; an N-channel transistor  $N_6$  as a first diode having an anode connected to the source of the transistor  $N_4$ ; a step-up capacitor  $C$  having one end connected to the cathode of the first diode  $N_6$ , thus to add a potential of a clock ( $V_{PP}$  system or  $V_{DD}$  system) applied to the other end thereof to a cathode potential of the first diode  $N_6$ ; and an N-channel transistor  $N_7$  as a second diode having an anode connected to the cathode of the first diode  $N_6$ , and a cathode serving as the output point of the step-up section 1.

In this embodiment, the first diode  $N_6$  serves to prevent a current from reversely flowing from the stepped up cathode side to the anode side of a low potential, thus to hold a stepped up cathode potential. Further, the second diode  $N_7$  serves to prevent a current from reversely flowing from the cathode side to the anode side when the clock falls, thus to hold a stepped up output potential  $V_{OUT}$ . The step-up section 1 further includes an N-channel transistor  $N_5$  provided in parallel with the first switch  $N_4$  and having a gate to which the output potential  $V_{OUT}$  is delivered.

This transistor  $N_5$  functions as follows. When an output potential  $V_{OUT}$  stepped up so that it is higher than the program potential  $V_{PP}$  is applied to its gate, the transistor  $N_5$  outputs the program potential  $V_{PP}$  on the drain side to the source side as it is without a voltage drop to allow the first switch  $N_4$  to undergo no voltage drop, thus to provide a further improved step-up characteristic of the step-up section 1. Moreover, the step-up section 1 further comprises an N-channel transistor  $N_8$  as a limiter to limit a stepped up output potential  $V_{OUT}$  to a desired potential  $V_{PP} + \alpha$  to finally output the limited potential. It is to be noted that whether or not the transistors  $N_5$  and/or  $N_8$  are provided, and whether a clock of the  $V_{PP}$  system is used or a clock of the  $V_{DD}$  system is used are determined to what degree the step-up value  $\alpha$  of a final output potential  $V_{PP} + \alpha$  is set. In addition, the step-up section 1 further comprises a D type N-channel transistor  $N_9$  for delivering a drain potential  $V_D$  for readout. This transistor  $N_9$  is turned on at the time of non-programming in response to an inverted signal of the step-up signal applied to its gate.

In the configuration stated above, when an input of a step-up start signal is provided, the initial potential setting transistor  $N_{10}$  is turned on. As a result, the output potential  $V_{OUT}$  is immediately set to an initial potential  $V_{OUT}(0)$  expressed as follows:

$$V_{OUT}(0) = V_{PP} - V_{THN10} \quad (5)$$

where  $V_{THN10}$  is a threshold potential of the transistor  $N_{10}$ . For this reason, as indicated by the curve d in FIG. 8, the output potential  $V_{OUT}$  can rise from the potential  $V_{PP} - V_{THN10}$ . This rising process is substantially the same as that of the conventional circuit which has been previously described. However, rising is started from the initial potential  $V_{PP} - V_{THN4} - V_{THN6} - V_{THN7}$  as previously explained in the case of the rising characteristic of the conventional circuit indicated by the curve e. On the contrary, the circuit of this embodiment can start rising from an initial potential which is high by a multiple of threshold value  $V_{TH}$  corresponding to two stages of the transistors as compared to the conventional circuit. For example, when it is assumed that the program voltage  $V_{PP}$  is equal to 12.5 volts and the threshold voltage  $V_{TH}$  of each transistor is nearly equal to 2.5 volts in the same manner as in the case of the study on the prior art, an initial potential  $V_{OUT}(0)$  according to this embodiment is expressed as follows:

$$V_{OUT}(0) = 12.5 \text{ V} - 2.5 \text{ V} = 10 \text{ V}.$$

It is seen from this that a considerably higher initial potential can be provided as compared to  $V_{OUT}(0) = 5 \text{ V}$  of the prior art.

Further, since the step-up section 1 must drive a load of the output from the beginning, as described above in the prior art, the step-up efficiency is poor, so the rise characteristic is gentle as indicated by the curve e. On the contrary, in the case of this embodiment, since the load is driven by the initial potential setting transistor  $N_{10}$  for a time period during which the transistor  $N_{10}$  is turned on, the step-up section 1 has no need to drive a load. Accordingly, the step-up efficiency is good and the rising is sharp or steep.

It is seen from the above that this embodiment can step up the output potential  $V_{OUT}$  to a desired potential in an extremely short time as compared to that of the prior art.

It is to be noted that since when the output potential  $V_{OUT}$  is raised to the initial potential  $V_{PP} - V_{THN10}$  in this embodiment, the gate-source voltage of the initial potential setting transistor  $N_{10}$  is lowered to reach the threshold voltage  $V_{THN10}$ , it is automatically turned off, and, after that, an output potential is delivered by the step-up section 1, thus to perform a step-up operation. This turn off operation prevents that a current inversely flows from the output point stepped up above the power supply voltage  $V_{PP}$  to the power source through the transistor  $N_{10}$ , so that an excessive load is applied to the step-up section 1, resulting in a deteriorated step-up characteristic.

Turning now to FIG. 9, there is shown another embodiment of this invention. This embodiment differs from the embodiment shown in FIG. 7 in that a D type N-channel transistor  $N_{11}$  is used as the initial potential setting transistor, thus to apply, to the gate thereof, an output pulse ( $V_{PP}$  system) from a rise pulse generation circuit 2 for generating a pulse having a fixed time width in response to the rise of the step-up start signal.

The merit of this embodiment is that the initial value  $V_{OUT}(0)$  of an output potential can be set to a value higher than that in the embodiment shown in FIG. 7. Namely, since D type transistor is used as the initial potential setting transistor  $N_{11}$ , there is no voltage drop on the transistor  $N_{11}$ . Accordingly, a power supply potential  $V_{PP}$  on the drain side is propagated to the output point on the source side, and then appears as the initial potential  $V_{OUT}(0)$ . Thus, sharper rise characteristic of the output potential  $V_{OUT}$  can be provided, as indicated by the curve f.

In this case, even when the output potential  $V_{OUT}$  reaches the power supply potential  $V_{PP}$ , the transistor  $N_{11}$  is not automatically turned off because it is a D type. In view of this, an approach is employed to limit the pulse width of the rise pulse generation circuit 2 to a fixed value, thus to forcibly turn the transistor  $N_{11}$  off when the output potential  $V_{OUT}$  has reached the power supply potential  $V_{PP}$ .

In the embodiment shown in FIG. 9, when the potential  $V_{PP}$  becomes equal to zero volts at the time of non step-up operation i.e., in the state where the output potential  $V_{OUT}$  is equal to the potential  $V_{DD}$ , since the transistor  $N_{11}$  is not turned off as described above, an inconvenience might occur such that a direct current flows out from the potential  $V_{DD}$  side through the transistor  $N_{11}$ .

An embodiment improved to prevent this is shown in FIG. 10. In this embodiment, a series circuit consisting of an E type P-channel transistor  $N_{12}$  and an E type N-channel transistor  $N_{13}$  is used in place of the transistor  $N_{11}$  of FIG. 9. It is to be noted that while the transistor  $N_{13}$  is of the E type, its threshold voltage is substantially equal to zero volts (i.e., zero volts, or a value close to zero volts). Further, since these two transistors  $N_{12}$  and  $N_{13}$  are turned on only for a predetermined time period from the beginning of the step-up operation, an output signal from the rise pulse generation circuit 2 is applied to the gate of the N-channel type transistor  $N_{13}$ , and such an output signal is also inverted through an inverter 3 and is then applied to the gate of the P-channel transistor  $N_{12}$ .

In this embodiment, since the transistors  $N_{12}$  and  $N_{13}$  are in an off state even when the potential  $V_{PP}$  becomes equal to zero volts at the time of non step-up operation, no direct current path is formed. On the other hand, since voltage drops on those transistors  $N_{12}$  and  $N_{13}$  at the time of step-up operation are substantially equal to zero volts, an initial potential  $V_{OUT}(0)$  nearly equal to the potential  $V_{PP}$  is provided.

What is claimed is:

1. A charge pump circuit including a step-up section having an output point to which a load is connected, said step-up section being responsive to a step-up start signal to start a step-up operation in which a potential of said output point is stepped up from a predetermined potential lower than a potential of a power supply to a desired potential higher than said power supply potential,

said charge pump circuit comprising:

an initial potential setting switch means connected between said power supply and said output point of said step-up section, and responsive to the step-up start signal to be turned on at the beginning of the step-up operation of said step up section to propagate said power supply potential to said output point of said step-up section, and to be turned off at a suitable time.

2. A charge pump circuit as set forth in claim 1, wherein said step-up section includes step-up start switch means operative in response to the step-up start signal and having one end connected to said power supply, first diode means having an anode connected to the the end of said switch means, a step-up capacitor having one end connected to the cathode of said first diode means, thus to add a potential applied to the other end thereof to a potential on the cathode of said first diode means, and second diode means having an anode connected to the cathode of said first diode means and a cathode serving as said output point of said step-up section.

3. A charge pump circuit as set forth in claim 1, wherein said initial potential setting switch means comprises an enhancement type N-channel MOS transistor having a source and a drain connected to said power supply and said output point, respectively, said enhancement type N-channel MOS transistor being controlled by the set-up start signal to be turned on at the beginning of the step-up operation.

4. A charge pump circuit as set forth in claim 1, wherein said initial potential setting switch means comprises a depletion type N-channel MOS transistor having a source and a drain connected to said power supply and said output point, respectively, said depletion type N-channel MOS transistor being controlled by the step-up start signal to be in an ON state only for a predeter-

mined time period from the beginning of the step-up operation in said step-up section.

5. A charge pump circuit including a step-up section having an output point to which a load is connected, said step-up section being responsive to a step-up start signal to step up a potential of said output point from a predetermined potential lower than a potential of a power supply to a desired potential higher than said power supply potential,

said charge pump circuit comprising:

initial potential setting switch means connected between said power supply and said output point of said step-up section, and responsive to the step-up start signal to be turned on at the beginning of the step-up operation of said step up section to propagate said power supply potential to said output point of said step-up section, and to turned off at a suitable time;

wherein said initial potential setting switch means is comprised of a series circuit consisting of an enhancement type P-channel MOS transistors and an enhancement type N-channel MOS transistor, said N-channel MOS transistor having a threshold voltage substantially equal to zero volts, a control signal being applied to respective gates of said two transistors so that they are in an ON state only for a predetermined time period from the beginning of the step-up operation in said step-up section.

\* \* \* \* \*



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# United States Patent [19]

Ghilardelli et al.

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[45] Date of Patent: Oct. 10, 2000

## [54] NMOS NEGATIVE CHARGE PUMP

[75] Inventors: Andrea Ghilardelli, Cinisello Balsamo;  
Jacopo Mulatti, Latisana; Maurizio  
Branchetti, San Polo D'Enza, all of  
Italy

[73] Assignee: STMicroelectronics S.r.l., Agrate  
Brianza, Italy

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## [30] Foreign Application Priority Data

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[51] Int. Cl.<sup>7</sup> ..... G05F 3/02

[52] U.S. Cl. .... 327/536; 327/534

[58] Field of Search ..... 327/534, 536,  
327/537, 589; 363/59, 60

## [56] References Cited

## U.S. PATENT DOCUMENTS

4,922,402 5/1990 Olivo et al. .... 363/60  
5,489,870 2/1996 Arakawa ..... 327/536  
5,612,921 3/1997 Chang et al. .... 365/226

## FOREIGN PATENT DOCUMENTS

0 570 597 A1 11/1993 European Pat. Off. .  
0 616 329 A2 9/1994 European Pat. Off. .  
0 638 984 A1 2/1995 European Pat. Off. .  
0 678 970 A2 10/1995 European Pat. Off. .

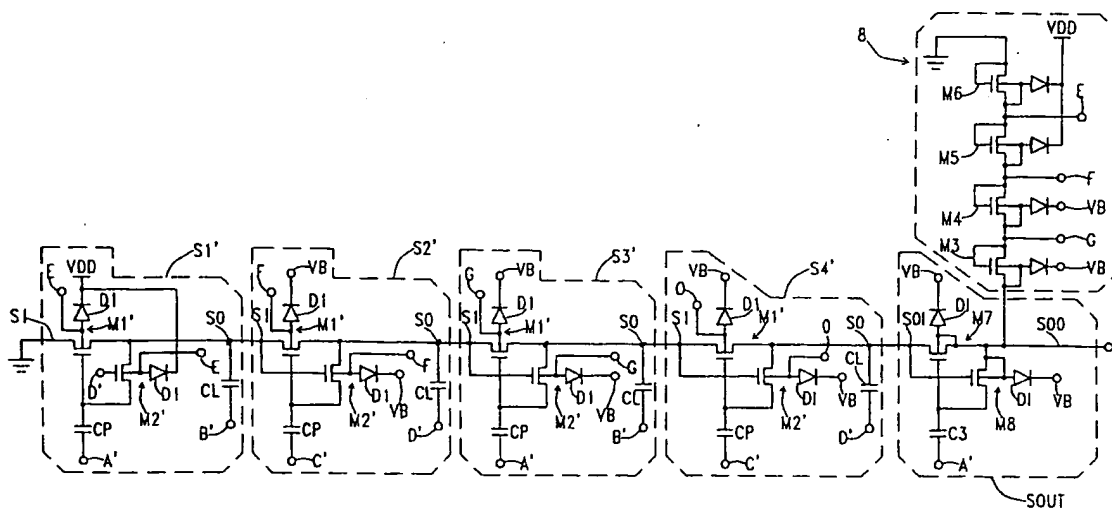
Primary Examiner—Jung Ho Kim

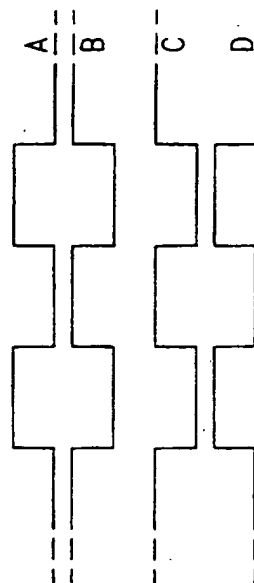
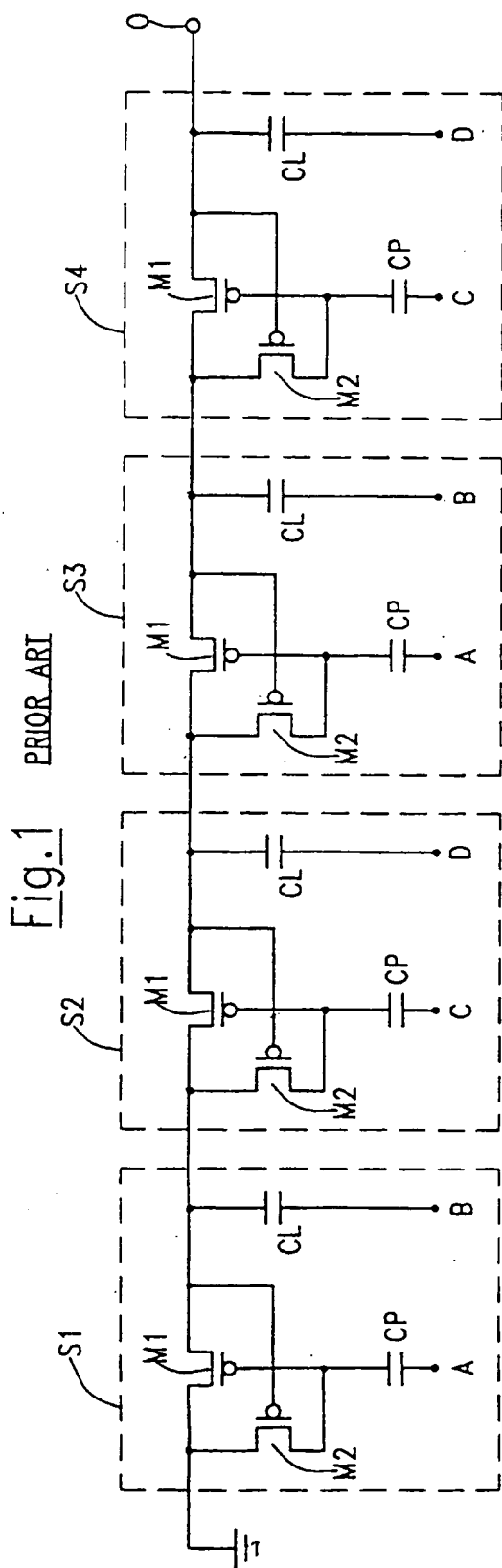
Attorney, Agent, or Firm—Theodore E. Galanthay; David V.  
Carlson; Seed IP Law Group PLLC

## [57] ABSTRACT

A negative charge pump circuit comprises a plurality of charge pump stages connected in series to each other. Each stage has a stage input terminal and a stage output terminal. A first stage has the stage input terminal connected to a reference voltage, a final stage has the stage output terminal operatively connected to an output terminal of the charge pump at which a negative voltage is developed; intermediate stages have the respective stage input terminal connected to the stage output terminal of a preceding stage and the respective stage output terminal connected to the stage input terminal of a following stage. Each stage comprises a first N-channel MOSFET with a first electrode connected to the stage input terminal and a second electrode connected to the stage output terminal, a second N-channel MOSFET with a first electrode connected to the stage output terminal and a second electrode connected to a gate electrode of the first N-channel MOSFET, a boost capacitor with one terminal connected to the gate electrode of the first N-channel MOSFET and a second terminal driven by a respective first digital signal switching between the reference voltage and a positive voltage supply, and a second capacitor with one terminal connected to the charge pump stage output terminal and a second terminal connected to a respective second digital signal switching between the reference voltage and the voltage supply. A gate electrode of the second N-channel MOSFET is connected, in the first stage, to a third digital signal switching between the reference voltage and the voltage supply, while in the remaining stage the gate electrode of the second N-channel MOSFET is connected to the stage input terminal.

31 Claims, 3 Drawing Sheets





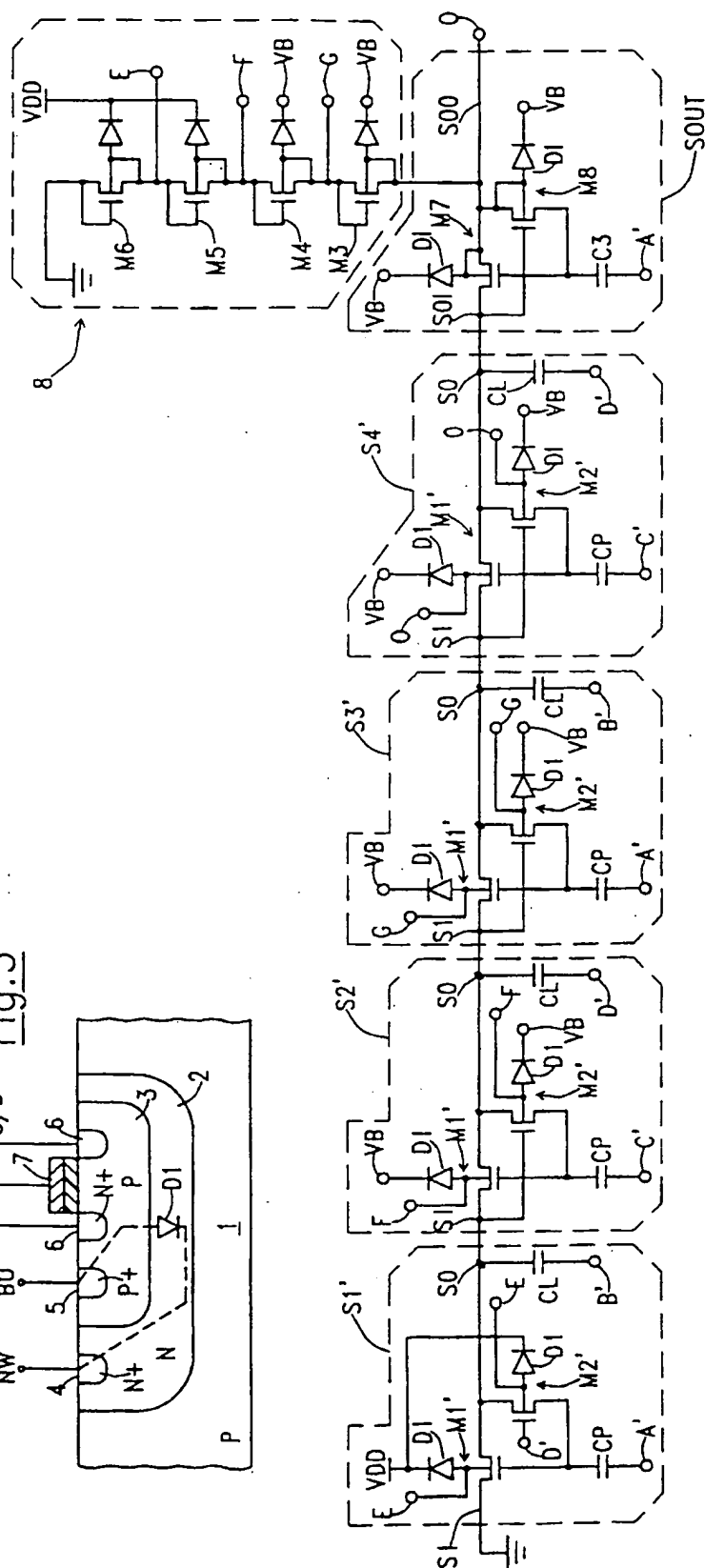
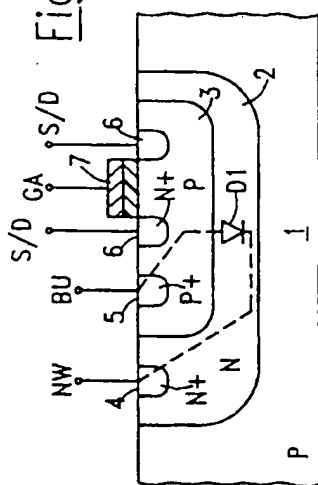


Fig. 4

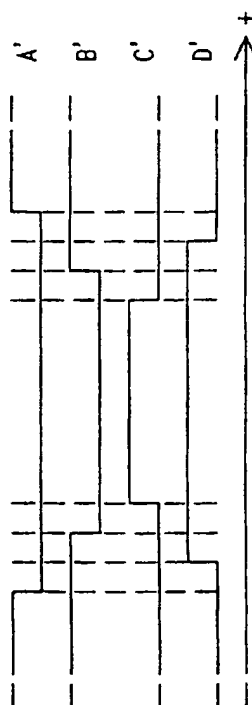


Fig. 5

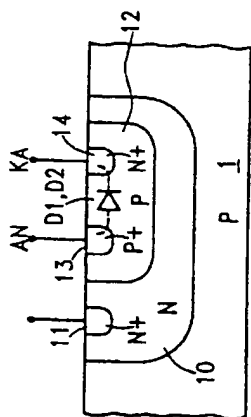


Fig. 7

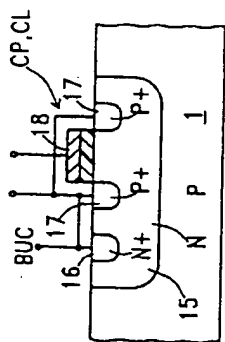
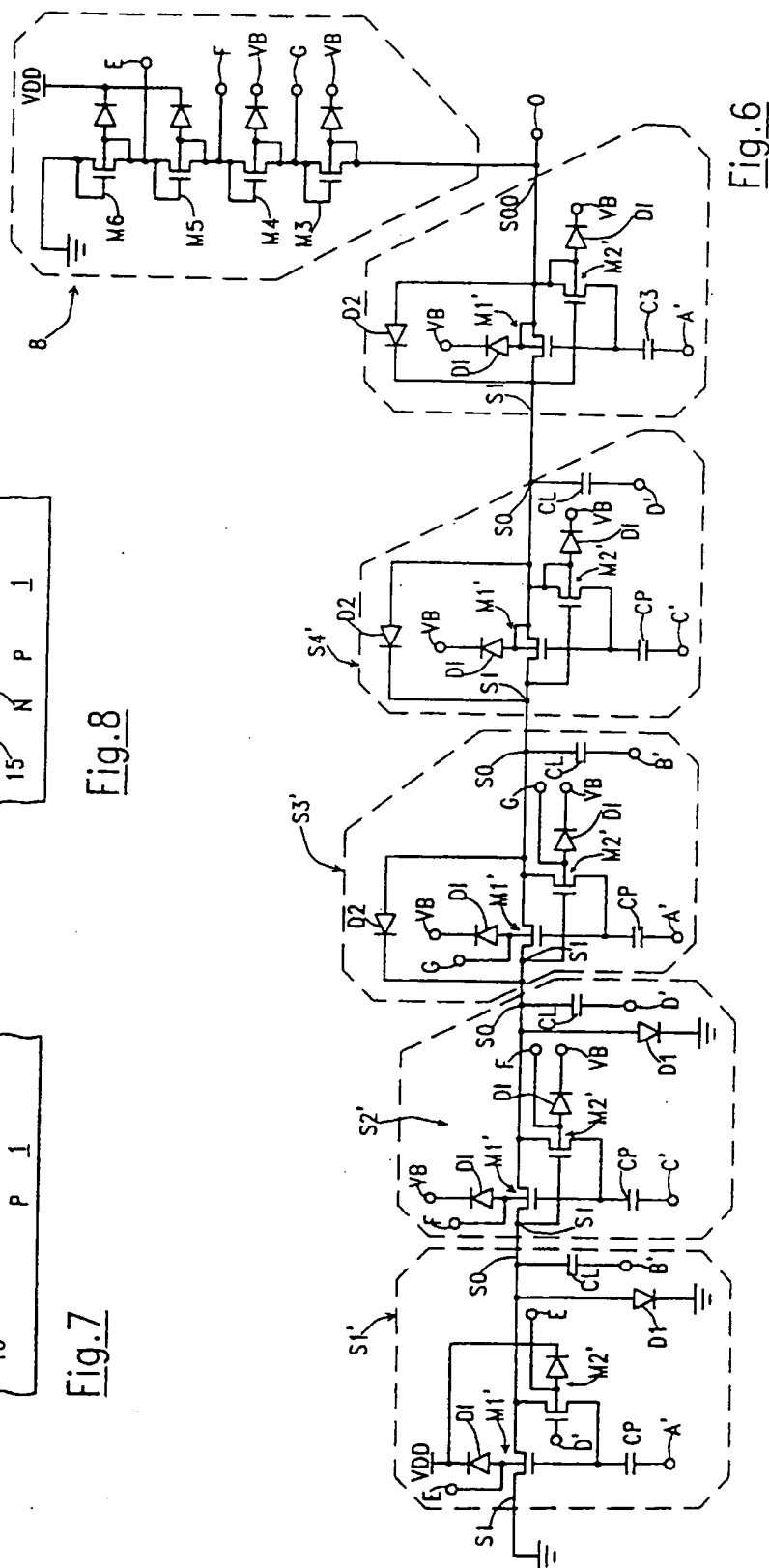


Fig. 8



## NMOS NEGATIVE CHARGE PUMP

## TECHNICAL FIELD

The present invention relates to an NMOS negative charge pump, particularly for the integration in CMOS non-volatile memory devices.

## BACKGROUND OF THE INVENTION

In the field of integrated circuits, particularly in non-volatile memory devices, it is often necessary to generate on-chip negative voltages starting from the positive voltage supply (VDD) which supplies the integrated circuit. This is for example the case of EEPROMs and Flash EEPROMs, wherein a negative voltage is necessary for the erase operation of the memory cells.

Conventionally, negative voltages are generated on-chip by means of negative charge pumps using P-channel MOSFETs, of the type shown in FIG. 1. With reference to this figure, it is possible to see that the negative charge pump is composed of several stages S1-S4 (four in this example), connected in series between ground and an output terminal O of the charge pump at which a negative voltage is provided. Each stage S1-S4 comprises a P-channel pass transistor M1, a P-channel pre-charge transistor M2, a charge storage capacitor CL driven by a respective first digital signal B or D periodically switching between ground and the voltage supply VDD, and a boost capacitor CP driven by a respective second digital signal A or C substantially in phase opposition with respect to signal B or D; the simplified timing of signals A, B, C and D is depicted in FIG. 2.

In operation, a positive charge flow takes place from the storage capacitor CL of a given stage to the storage capacitor CL of the adjacent, left-hand stage in FIG. 1, through the pass transistors M1, so that the output terminal O acquires a negative potential. The pre-charge transistor M2 pre-charges the boost capacitor CP, which in turn boosts the gate voltage of M1 so as to allow a most efficient charge transfer to take place.

When the negative charge pump is integrated in a CMOS integrated circuit, the P-channel MOSFETs are conventionally formed inside respective N-type wells which are in turn formed inside a common P-type semiconductor substrate.

The main drawbacks of the circuit described above will be now discussed.

First, due to the body effect affecting MOS transistors, a progressive increase in the threshold voltage of the P-channel MOSFETs takes place moving from the stages near to the terminal of the charge pump connected to ground to the stages proximate to the output terminal O. In fact, the N-type wells wherein the P-channel MOSFETs are formed cannot be biased at negative voltages (otherwise the N-type well/P-type substrate junction becomes forward biased), while the source and drain electrodes of the P-channel MOSFETs are biased at more and more negative potentials. This reduces efficiency of the charge pump, because the voltage gain of each stage decreases; this reflects on a higher number of stages being necessary for generating a given negative voltage. Furthermore, the body effect limits the negative voltage value that can be generated, because when the body effect is so high that the threshold voltage of the P-channel MOSFETs reaches the value of the voltage supply VDD, even if more stages are added to the charge pump the negative output voltage cannot increase further (in absolute value).

Second, P-channel MOSFETs are intrinsically slower than N-channel MOSFETs, so that the maximum operating frequency of the charge pump is limited; this has a negative impact on the output current capability of the charge pump.

Third, the charge pump structure shown in FIG. 1 has a poor reliability; in fact, when the pass transistors M1 are off, the voltage applied to their gate oxide is equal to the difference between their gate voltage and the bias voltage of the N-type wells inside which the transistors are formed; the gate voltage can go strongly negative (especially in the final stages of the charge pump), but the bias voltage of the N-type wells cannot be lower than 0 V (to prevent forward biasing of the N-type wells/P-type substrate junctions).

Fourth, conventional CMOS manufacturing process could easily provide N-channel MOSFETs which are more resistant to junction breakdown than their P-channel counterparts; in this case, the reliability of the charge pump is lower relative to using N-channel MOSFETs.

## SUMMARY OF THE INVENTION

In view of the state of the art described, it is an object of the present invention to provide a negative charge pump which is not affected by the above mentioned problems.

According to the present invention, such object is attained by means of negative charge pump circuit comprising a plurality of charge pump stages connected in series to each other, each stage having a stage input terminal and a stage output terminal, said plurality of stages comprising a first stage having the respective stage input terminal connected to a reference voltage, a final stage having the respective stage output terminal operatively connected to an output terminal of the charge pump at which a negative voltage is developed, and a plurality of intermediate stages each having the respective stage input terminal connected to the stage output terminal of a preceding stage and the respective stage output terminal connected to the stage input terminal of a following stage, characterized in that each charge pump stage comprises a first N-channel MOSFET with a first electrode connected to the stage input terminal and a second electrode connected to the stage output terminal, a second N-channel MOSFET with a first electrode connected to the stage output terminal and a second electrode connected to a gate electrode of the first N-channel MOSFET, a boost capacitor with one terminal connected to the gate electrode of the first N-channel MOSFET and a second terminal driven by a respective first digital signal switching between the reference voltage and a positive voltage supply, and a second capacitor with one terminal connected to the stage output terminal and a second terminal connected to a respective second digital signal switching between the reference voltage and the voltage supply and substantially in phase opposition to the first digital signal, a gate electrode of the second N-channel MOSFET being connected, in the first stage, to a third digital signal switching between the reference voltage and the voltage supply, a gate electrode of the second N-channel MOSFET in all the stages other than said first stage being connected to the stage input terminal.

## BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be made apparent by the following detailed description of two particular embodiments thereof, illustrated as non-limiting examples in the annexed drawings, wherein:

FIG. 1 is a circuit diagram of a negative charge pump according to the prior art;

FIG. 2 is a simplified time diagram of drive signals for the charge pump of FIG. 1;



FIG. 3 shows in cross-sectional view the structure of an N-channel MOSFET for use in a negative charge pump according to the present invention;

FIG. 4 is a circuit diagram of a first embodiment of a negative charge pump according to the present invention, which makes use of N-channel MOSFETs with the structure shown in FIG. 3;

FIG. 5 is a time diagram of drive signals for the charge pump of FIG. 4;

FIG. 6 is a circuit diagram of a negative charge pump according to a second embodiment of the present invention;

FIG. 7 shows in cross-sectional view the structure of a junction diode for use in the charge pump of FIG. 6; and

FIG. 8 shows in cross-sectional view the structure of a capacitor for use in the charge pump of FIG. 6.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows the circuit structure of a negative charge pump according to the prior art, using P-channel MOSFETs; FIG. 2 shows the simplified time evolution of the drive signals of the charge pump of FIG. 1. This conventional kind of negative charge pump has already been discussed in the foregoing, and the drawbacks thereof have been described.

FIG. 3 is a cross-sectional view of an N-channel MOSFET which is used in the negative charge pump according to the present invention. Inside a P type substrate 1 (which forms the common substrate of the integrated circuit wherein the negative charge pump is integrated), an N type well 2 is formed; inside the N type well 2, an N+ contact region 4 for biasing the N type well 2 and a P type well 3 are formed; inside the P type well 3, a P+ contact region 5 for biasing the P type well 3 and N+ source/drain regions 6 of the N-channel MOSFET are formed; over the P type well 3, between the source/drain regions 6, an insulated gate 7 is formed. The device has five terminals: two source/drain terminals S/D, a gate terminal GA, a bulk terminal BU and an N well bias terminal NW. The device is functionally equivalent to an N-channel MOSFET with a diode DI inserted between terminals BU and NW. This structure makes up one embodiment of a biasing subcircuit. Thanks to this structure, which can be realized using a triple-well CMOS manufacturing process, it is possible to bias the P type well 3 wherein the N-channel MOSFET is formed at a potential different from that of the P type substrate 1, which is normally kept grounded.

In FIG. 4 a circuit diagram of a first embodiment of the present invention is shown. The negative charge pump comprises a plurality of stages (S1'-S4', totaling four in the shown example) connected in series between ground and a decoupling stage SOUT, the output thereof being an output terminal O of the charge pump at which a negative voltage is provided. Each stage has a stage input terminal SI (SOI) and a stage output terminal SO (SOO); the stage input terminal of the first stage S1' is connected to ground; the stage output terminal of the last stage S4' is connected to the input terminal SOI of the decoupling stage SOUT; the stage output terminal SOO of the latter is connected to the output terminal O; in the intermediate stages, the stage input terminal SI is connected to the stage output terminal of the preceding stage.

Each stage S1'-S4' comprises an N-channel pass transistor M1' and an N-channel pre-charge transistor M2', both having the structure shown in FIG. 3, a storage capacitor CL and a boost capacitor CP. The pre-charge transistor M2' has

source/drain terminals connected to the control gate of the pass transistor M1' and to a stage output terminal SO; in the first stage S1', the control gate of the pre-charge transistor M2' is driven by a digital signal D' (to be described hereinafter), while in all the other stages the control gate of M2' is connected to the stage input terminal SI. In each stage the boost capacitor CP has one plate driven by a respective digital signal A' or C', and the storage capacitor CL has one plate driven by another respective digital signal B' or D'. The timing of signals A', B', C' and D' is shown in FIG. 5; all these four signals are digital signals periodically switching between ground and a positive voltage supply VDD, which is the supply voltage of the integrated circuit wherein the charge pump is integrated.

The charge pump also comprises a bias voltage generator 8 which generates three bias voltages E, F and G; bias voltage E is used for biasing the bulk terminal BU of transistors M1' and M2' in the first stage S1'; bias voltage F is used for biasing the bulk terminal BU of transistors M1' and M2' in the second stage S2'; and bias voltage G is used for biasing the bulk terminal BU of transistors M1' and M2' in the third stage S3'. The bulk terminal BU of transistors M1' and M2' in the last stage S4' is instead connected directly to the output terminal O of the charge pump.

The decoupling stage SOUT is similar to the other stages S1'-S4', comprising N-channel MOSFETs M7 and M8 and a boost capacitor C3 driven by signal A'. The bulk terminal BU of MOSFETs M7 and M8 is connected to the output terminal O of the charge pump.

The bias voltage generator 8 comprises a voltage divider formed by four diode-connected N-channel MOSFETs M3-M6, having the structure shown in FIG. 3, connected in series between the output terminal O of the charge pump and ground. Bias voltages E, F and G are derived from intermediate nodes between MOSFETs M3 and M4, M4 and M5 and M5 and M6; thus, voltages E, F and G are progressively more negative. The bulk terminals BU of MOSFETs M3-M6 are short-circuited to the respective source terminals of the transistors.

The N-well terminals NW of MOSFETs M1' and M2' of the stages of the charge pump, as well as the N-well terminals of the MOSFETs M3-M6 of the bias voltage generator 8, could be directly connected to the positive voltage supply VDD. In this way, it would be assured that the junctions between the N type wells 2 and the P type substrate 1 are reverse biased and that the P type wells 3 wherein the MOSFETs are formed are electrically isolated from the substrate. However, it is preferable that the N-type well terminals NW of the MOSFETs whose P-type well is biased at negative voltages which are rather high in absolute value are biased at ground, to reduce electrical stresses. To this purpose, the N-type well terminals NW of MOSFETs M1' and M2' in stages S2' to S4', and M7 and M8 in SOUT, and the N-type well terminals NW of MOSFETs M4 and M3 in the bias voltage generator 8 are connected to a voltage VB which is switchable between the voltage supply VDD and ground. In operation, voltage VB will be kept at VDD as long as the output voltage O is low in absolute value, and is then switched to ground when the negative voltage O becomes high (in absolute value).

The operation of the circuit is the following.

When signal D' switches from "0" to "1" (i.e., from ground to VDD), the potential of the output terminal SO of stage S4' raises. Since signal B' is still at VDD, the potential of the output node SO of stage S3' is high, so that M2' in stage S4' is on; CP can thus charge (signal C' is still at

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ground). When signal B' switches from VDD to ground, M2' in stage S4' turns off; when signal C' switches to VDD, the gate voltage of M1' in stage S4' is boosted to a high value, and the potentials of the stage output terminal SO of stage S4' and of the stage output terminal SO of stage S3' are equalized by means of charge transfer from capacitor CL in stage S4' to capacitor CL in stage S3'. Then, M1' in stage S4' is turned off by switching of signal C' from VDD to ground. In this way, a positive charge has been transferred from capacitor CL in stage S4' to capacitor CL in stage S3'. In a similar way, a transfer of positive charge takes place from capacitor CL in one stage to capacitor CL in the left-hand adjacent stage, and finally to ground, so that the stage output terminal SO of the stage S4' acquires a negative potential. Stage SOUT decouples the output terminal O from the stage output terminal SO of stage S4'; the potential of node O will be approximately constant not affected by ripples present at the output SO of stage S4'.

It is to be observed that signals A', B', C' and D' are properly disoverlapped. In fact, signal C' cannot switch from ground to VDD before signal B' has switched from VDD to ground and signal D' has switched from ground to VDD; this is necessary to prevent a positive charge flow taking place from the left-hand to the right-hand stages of the charge pump; for similar reasons, signal C' must switch to ground before signal B' has switched to VDD and signal D' has switched to ground.

The arrangement shown in FIG. 4 minimizes the influence of body effect on the threshold voltages of the N-channel MOSFETs; thanks to the particular biasing scheme of the P-type wells 3 of the N-channel MOSFETs, it is assured that the P-type well of a given MOSFET is biased at the minimum among the source and drain voltages of the MOSFET; this is the best biasing condition, because the body effect is thus minimized. The number of elements of the voltage divider of the bias voltage generator 8 must be equal to the number of stages of the charge pump.

FIG. 6 is a circuit diagram of a second embodiment of the present invention. The differences from the structure shown in FIG. 4 are the following:

In each of the first two stages S1' and S2' of the charge pump, a respective junction diode D1 is provided having an anode connected to the output terminal SO of the respective stage and a cathode connected to ground. In the last two stages S3' and S4' and in the decoupling stage SOUT, a respective diode D2 is provided having an anode connected to the output terminals SO, SOO respectively of the stage, and a cathode connected to the input terminals SI, SOI respectively of the stage. This structure makes up one embodiment of a speed-up circuit.

The provision of diodes D1 and D2 has the advantage that the internal nodes of the charge pump start from an initial potential equal to the threshold voltage of a PN junction, instead of from a higher voltage. In this way, the charge pump can reach the steady-state quicker.

Preferably, diodes D1 and D2 have the structure shown in FIG. 7, comprising an N-type well 10 formed inside the P-type substrate 1, wherein an N+ contact region 11 and a P-type well 12 are formed. Inside the P-type well 12, a P+ region 13 and an N+ region 14 are formed. Region 11 provides a bias terminal for the N-type well 10; regions 13 and 14 respectively form the anode AN and cathode KA electrodes of the diode.

Junction diodes are preferred over P-channel MOSFETs because they are more reliable because junction diodes are not subject to oxide damages, and have a higher breakdown

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voltage. For these reasons, junction diodes can be directly connected between the internal nodes of the charge pump and ground (at least in the first stages of the pump), instead of between one stage and the following (as for example D2 in S4' and SOUT); thanks to this, the stages of the charge pump start from a voltage VT (threshold voltage of a PN junction) instead of higher voltages, and the charge pump reaches steady-state conditions faster.

FIG. 8 shows the structure of a PMOS-type capacitor used for the practical realization of capacitors CP and CL of the stages of the charge pump. In the P-type substrate 1, an N-type well 15 is formed; inside the N-type well 15, an N+ contact region 16 is formed for providing a bulk biasing terminal BUC, and two P+ regions 17 are also formed; over the surface of the N-type well 15 an insulated gate 18 is formed. The insulated gate forms one terminal of the capacitor, while the other terminal is formed by regions 17 and 16.

By connecting the terminals BUC and 17 of the capacitors to the respective digital signal A', B', C' or D' which drives one of the terminals of the capacitors, the capacitor can work also in the accumulation region. This kind of connection of the capacitors has two advantages: first, non diodes or start-up circuits are necessary for turning the capacitors on; second, and related to the first, the pump startup is faster, because it is not necessary to wait for turning of the capacitors on.

What is claimed is:

1. Negative charge pump circuit comprising:

- a plurality of charge pump stages connected in series to each other, each stage having a stage input terminal and a stage output terminal, said plurality of stages comprising a first stage having the respective stage input terminal connected to a reference voltage, a final stage having the respective stage output terminal operatively connected to an output terminal of the charge pump at which a negative voltage is developed, and a plurality of intermediate stages each having the respective stage input terminal connected to the stage output terminal of a preceding stage and the respective stage output terminal connected to the stage input terminal of a following stage, wherein each charge pump stage includes:
  - a first N-channel MOSFET with a first electrode connected to the stage input terminal and a second electrode connected to the stage output terminal;
  - a second N-channel MOSFET with a first electrode connected to the stage output terminal and a second electrode connected to a gate electrode of the first N-channel MOSFET;
  - a boost capacitor with one terminal connected to the gate electrode of the first N-channel MOSFET and a second terminal driven by a respective first digital signal switching between the reference voltage and a positive voltage supply;
  - a second capacitor with one terminal connected to the charge pump stage output terminal and a second terminal connected to a respective second digital signal switching between the reference voltage and the voltage supply and substantially in phase opposition to the first digital signal;
  - a gate electrode of the second N-channel MOSFET being connected, in the first stage, to a third digital signal switching between the reference voltage and the voltage supply; and
  - a gate electrode of the second N-channel MOSFET in all the stages other than said first stage being connected to the stage input terminal.

2. The negative charge pump according to claim 1 wherein said third digital signal coincides with the second digital signal of a second stage having the stage input terminal connected to the stage output terminal of said first stage.

3. The negative charge pump according to claim 2, further comprising:

a decoupling stage having an input terminal connected to the stage output terminal of said final stage; and  
an output terminal connected to the output terminal of the charge pump.

4. The negative charge pump according to claim 3 wherein said decoupling stage comprises:

a third N-channel MOSFET with a first and a second electrodes respectively connected to the input and output terminals of the decoupling stage;

a fourth N-channel MOSFET with a first and a second electrodes respectively connected to a gate electrode of the third N-channel MOSFET and to the output terminal of the decoupling stage; and

a third capacitor with one terminal connected to the gate electrode of the third N-channel MOSFET and a second terminal driven by a respective digital signal switching periodically between the reference voltage and the voltage supply.

5. The negative charge pump according to claim 4 wherein each of said first, second, third and fourth N-channel MOSFETs has a respective bulk electrode, the bulk electrodes of the first and second N-channel MOSFETs in each charge pump stage being biased by a respective bias voltage for that stage which becomes progressively more negative in going from the first stage towards the final stage, the bulk electrodes of the third and fourth N-channel MOSFETs in the decoupling stage being connected to the output terminal of the charge pump.

6. The negative charge pump according to claim 5, further comprising a bias voltage generator generating said bias voltages starting from the voltage of the output terminal of the charge pump.

7. The negative charge pump according to claim 6 wherein said bias voltage generator comprises a voltage divider connected between the output terminal of the charge pump and the reference voltage, the voltage divider having a number of intermediate nodes directly proportional to the number of stages of the charge pump.

8. The negative voltage pump according to claim 7 wherein said voltage divider comprises a series connection of diode-connected N-channel MOSFETs, said intermediate nodes being common nodes of adjacent diode-connected MOSFETs.

9. The negative charge pump according to claim 8 wherein each of said first, second, third and fourth N-channel MOSFETs comprises:

an N-type well formed in a P-type substrate;

a P-type well formed inside the N-type well; and

an N-type source/drain regions formed inside the P-type well.

10. The negative charge pump according to claim 9 wherein the first stage and each stage of a first sub-plurality of stages proximate to the first stage comprise a respective junction diode having an anode connected to the stage output terminal and a cathode connected to the reference voltage.

11. The negative charge pump according to claim 10 wherein in each of said N-type wells an N-type well contact region is formed.

12. The negative charge pump according to claim 11 wherein the well contact regions of the first and second MOSFETs of the first stage are electrically connected to the voltage supply, while the well contact regions of the first and second MOSFETs of the remaining stages and of the third and fourth MOSFETs of the decoupling stage are connected to a switchable potential which is switchable between the voltage supply and the reference voltage.

13. The negative charge pump according to claim 12 wherein each stage of a second sub-plurality of stages proximate to the output terminal and the decoupling stage comprise a respective junction diode with an anode connected to the stage output terminal and a cathode connected to the stage input terminal.

14. The negative charge pump according to claim 13 wherein the first and second digital signals supplying a given stage are substantially in phase opposition respectively to the first and second digital signals supplying the adjacent stages.

15. The negative charge pump according to claim 14 wherein the first and second digital signals supplying each stage are disoverlapped, so that the second terminal of the second capacitor is driven to the reference voltage after the second terminal of the boost capacitor has been driven to the reference voltage, and the second terminal of the second capacitor is driven back to the supply voltage before the second terminal of the boost capacitor is driven back to the supply voltage.

16. The negative charge pump according to claim 15 wherein the first digital signals supplying two adjacent stages are disoverlapped, so that the second terminal of the boost capacitor in each stage is driven to the supply voltage after the second terminal of the boost capacitors in the adjacent stages has been driven to the reference voltage, and after the second terminal of the second capacitor in the adjacent stages has been driven to the reference voltage, and the second terminal of the boost capacitor in each stage is driven back to the reference voltage before the second terminal of the boost capacitors in the adjacent stages is driven back to the supply voltage and before the second terminal of the second capacitor in the adjacent stages is driven back to the supply voltage.

17. The negative charge pump according to claim 16 wherein in each stage the second digital signal switches from the supply voltage to the reference voltage after the second digital signal in the adjacent stages has switched from the reference voltage to the supply voltage and before the first digital signal in the adjacent stages switches from the reference voltage to the supply voltage, and said second digital signal in each stage switches from the reference voltage to the supply voltage after the first digital signal in the adjacent stages has switched from the supply voltage to the reference voltage and before the second digital signal in the adjacent stages switches from the supply voltage to the reference voltage.

18. The negative charge pump according to claim 17 wherein each one of said boost capacitor, second capacitor and third capacitor is formed by an N-type well formed in said P-type substrate and by at least one P-type region formed in said N-type well, a first terminal of the capacitor being formed by said P-type region short-circuited to said N-type well, and a second terminal of the capacitor being formed by a conductive gate insulatively disposed over said N-type well.

19. A negative charge pump, comprising:

a plurality of stage circuits coupled to each other in stages, including at least a first stage and a second stage;

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at least one NMOS transistor formed within an N-type well, coupled between a first voltage and an output terminal within each stage; and

a biasing sub-circuit coupled to the NMOS transistor in each stage;

wherein an input of the second stage circuit is coupled to the output terminal of the previous stage, wherein the second stage circuit produces a voltage reduction at its output from the voltage appearing at its input; and

a bias voltage generator circuit producing a plurality of biasing voltages, one biasing voltage per stage, wherein the biasing voltage for each stage is coupled to the biasing sub-circuit to increase the voltage reduction from the input terminal to the output terminal of that stage.

20. The device according to claim 19, wherein the biasing sub-circuit is formed in a P-type substrate and comprises a diode having an anode and a cathode, the anode coupled to the body of the NMOS transistor and the bias voltage generator circuit, and the cathode coupled to a second voltage, wherein the P-N junction between the N-type well within which the NMOS transistor is formed and the P-type substrate is reverse biased.

21. The device according to claim 19, wherein the biasing voltages are increasingly negative from the first stage to the second stage.

22. The device according to claim 19, further comprising a plurality of speed up circuits coupled respectively to each of the plurality of stage circuits wherein the speed up circuit causes the output of each stage circuit to reach steady state in a decreased time period than without the speed up circuit present.

23. The device according to claim 22, wherein each respective speed up circuit comprises a diode.

24. The device according to claim 14, wherein the stage circuit further comprises a capacitor coupled to the output terminal.

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25. The device according to claim 19, wherein each stage includes a capacitor and the capacitor comprises:

a first capacitor terminal; and an n-type well having a bulk biasing terminal coupled to the first capacitor terminal.

26. A charge pump circuit comprising;

a plurality of charge pump stages including a first stage and a second stage;

a decoupling stage between the second stage of the charge pump and a final output terminal of the charge pump circuit; and

a bias voltage generator generating a plurality of bias voltages from the voltage of the final output terminal of the charge pump.

27. The circuit according to claim 26 wherein each stage has an input terminal and an output terminal and the output terminal of the first stage is coupled to the input terminal of the second stage.

28. The circuit according to claim 27 further including a third charge pump circuit having an input terminal coupled to the output terminal of the second charge pump stage.

29. The circuit according to claim 27 in which each stage further includes:

at least one MOS transistor formed with an N-well, coupled between a first voltage and an output terminal for that particular stage;

a biasing sub-circuit coupled to the N-MOS transistor in each stage; and

a bias voltage generator circuit producing a plurality of biasing voltages, one biasing voltage per stage wherein the biasing voltage for each stage is respectively coupled to the biasing sub-circuit for each stage.

30. The circuit according to claim 27 further including a plurality of speed up circuits within each respective stage.

31. The device according to claim 30 wherein the speed up circuit comprises a diode.

\* \* \* \* \*



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**Miyamitsu**

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(45) **Date of Patent:** **Nov. 9, 2004**

(54) **BOOSTER CIRCUIT**

(75) Inventor: **Fumiaki Miyamitsu, Kunisaki-machi (JP)**

(73) Assignee: **Texas Instruments Incorporated, Dallas, TX (US)**

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) Int. Cl.<sup>7</sup> ..... **G05F 1/10; G05F 3/02**

(52) U.S. Cl. .... **327/536**

(58) Field of Search ..... **327/536, 589; 363/59-60**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,191,232 A \* 3/1993 Wang ..... 327/306  
5,276,646 A 1/1994 Kim et al. .... 365/189.09  
5,420,505 A 5/1995 Kondo ..... 324/158.1  
5,999,425 A \* 12/1999 Lacey et al. .... 363/60  
6,091,282 A 7/2000 Kim ..... 327/536  
6,100,752 A \* 8/2000 Lee et al. .... 327/536

6,278,316 B1 8/2001 Tanzawa et al. .... 327/536  
6,297,687 B1 10/2001 Sugimura ..... 327/536

**FOREIGN PATENT DOCUMENTS**

JP 02062796 A \* 3/1990 ..... G11C/16/06  
JP 11146634 A \* 5/1999 ..... H02M/3/07  
JP 11308856 A \* 11/1999 ..... H02M/3/07

\* cited by examiner

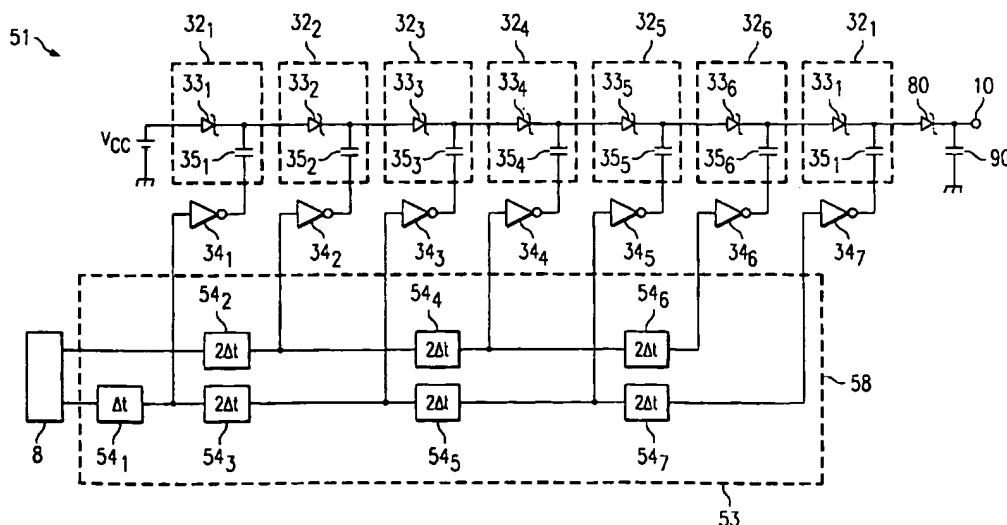
*Primary Examiner*—Quan Tra

(74) *Attorney, Agent, or Firm*—William B. Kempler; W. James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

The objective of the invention is to provide a booster circuit with reduced power consumption and switching noise. Booster circuit 1 of the present invention has gate circuits 4<sub>1</sub>–4<sub>7</sub>, an auxiliary control circuit 9. Each of gate circuits 4<sub>1</sub>–4<sub>7</sub> has charging/discharging circuit 11 and auxiliary charging/discharging circuit 12 used for charging/discharging capacitors 5<sub>1</sub>–5<sub>7</sub>. Under the control of auxiliary control circuit 9, said charging/discharging circuit 11 can operate independently or operate together with auxiliary charging/discharging circuit 12. When the booster circuit is started, charging/discharging circuit 11 and auxiliary charging/discharging circuit 12 are operated together to increase the drivability of gate circuits 4. As a result, the charging time of capacitors 5<sub>1</sub>–5<sub>7</sub> in charge-pump circuits 2<sub>1</sub>–2<sub>7</sub> can be shortened. On the other hand, at steady state, charging/discharging circuit 11 operates independently. As a result, the drivability of the gate circuits is reduced compared with that at the time when the booster circuit is started. Consequently, the loss in power consumption and noise can be reduced.

**2 Claims, 6 Drawing Sheets**



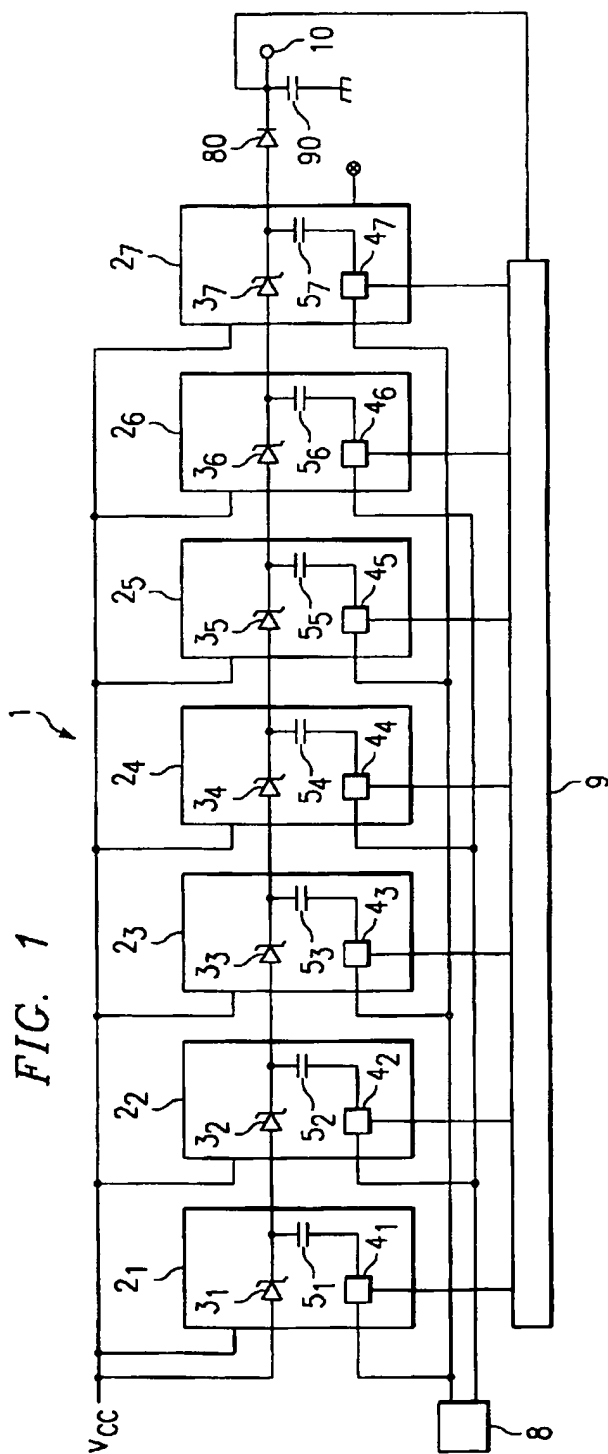


FIG. 2

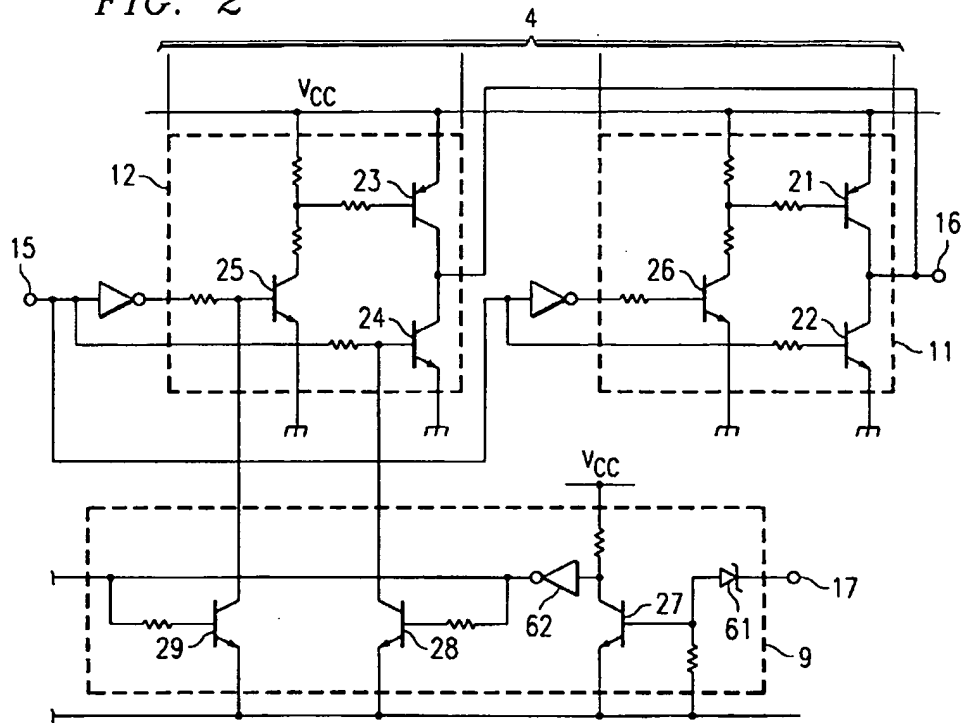


FIG. 3

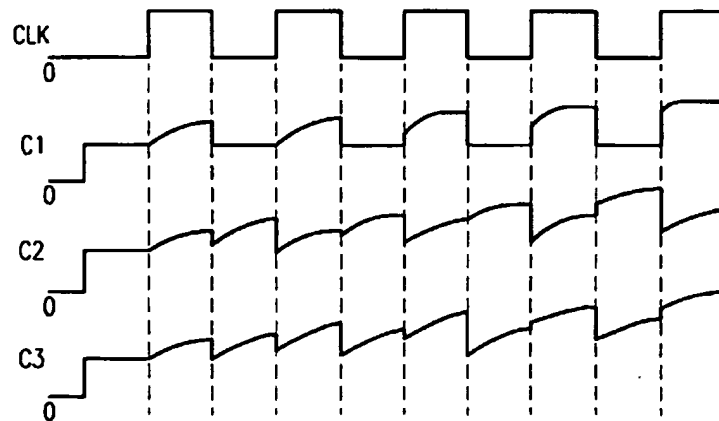


FIG. 4

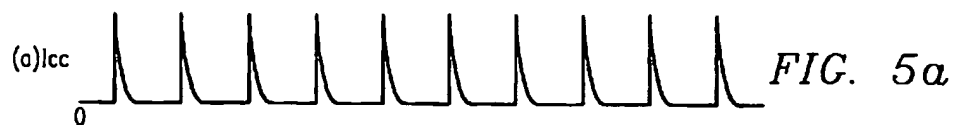
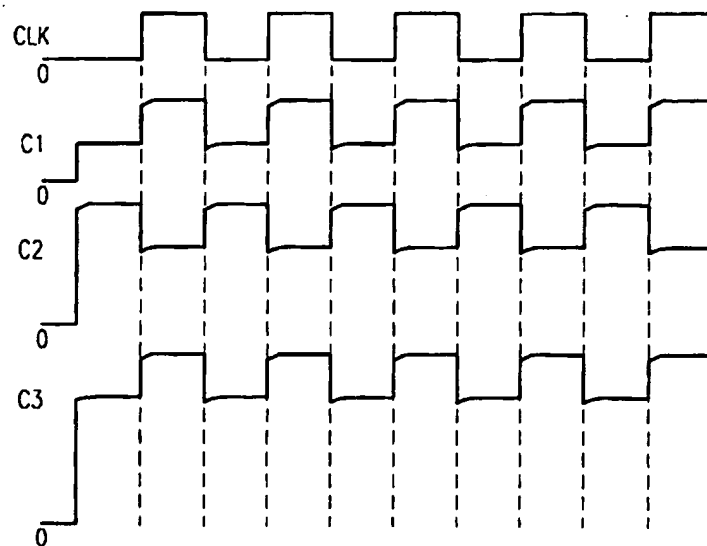


FIG. 5a



FIG. 5b

FIG. 6

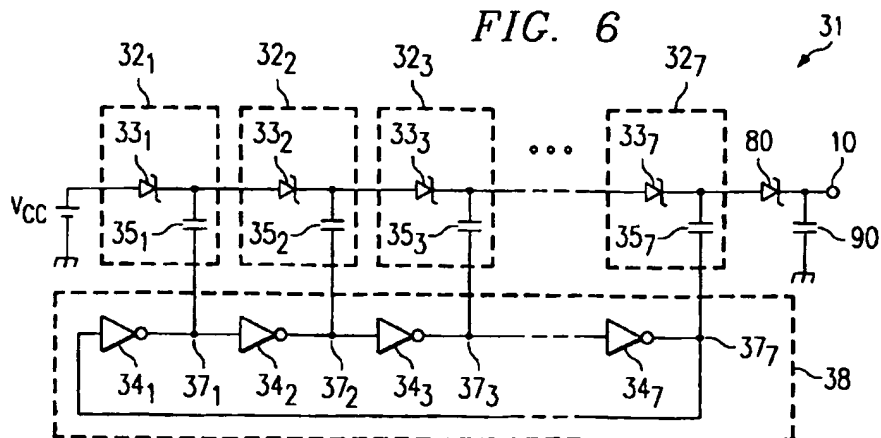




FIG. 7

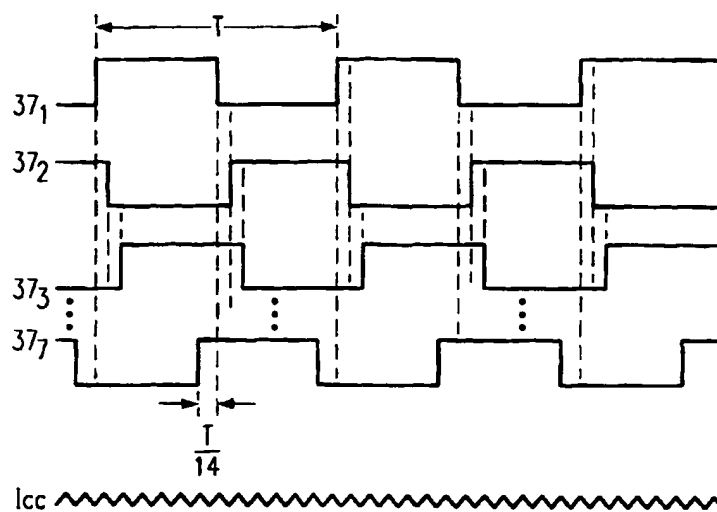
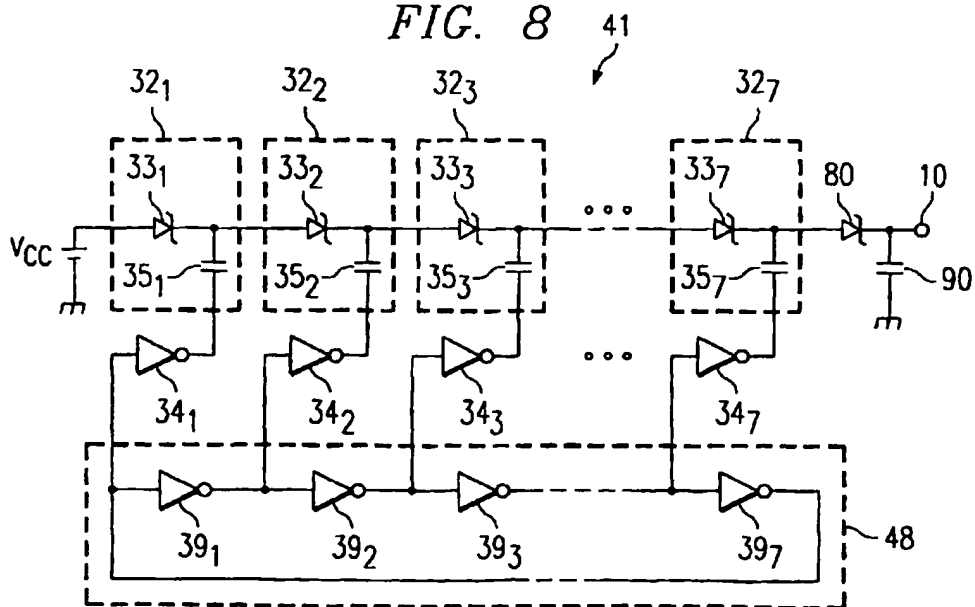
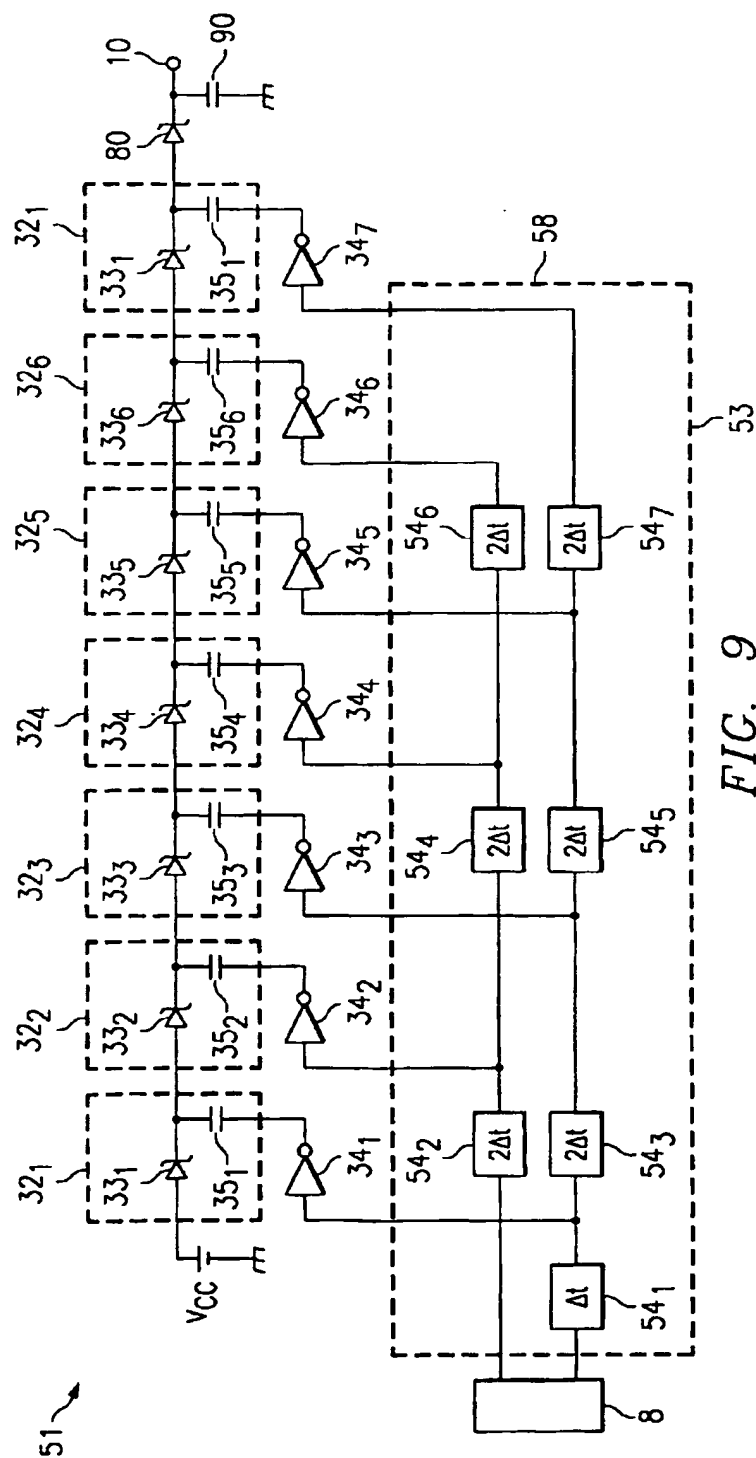
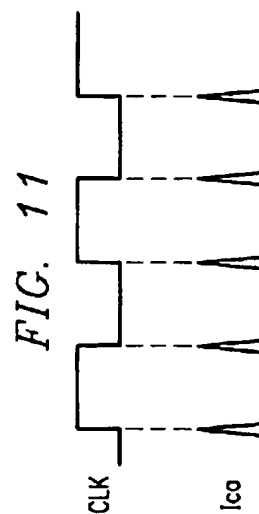
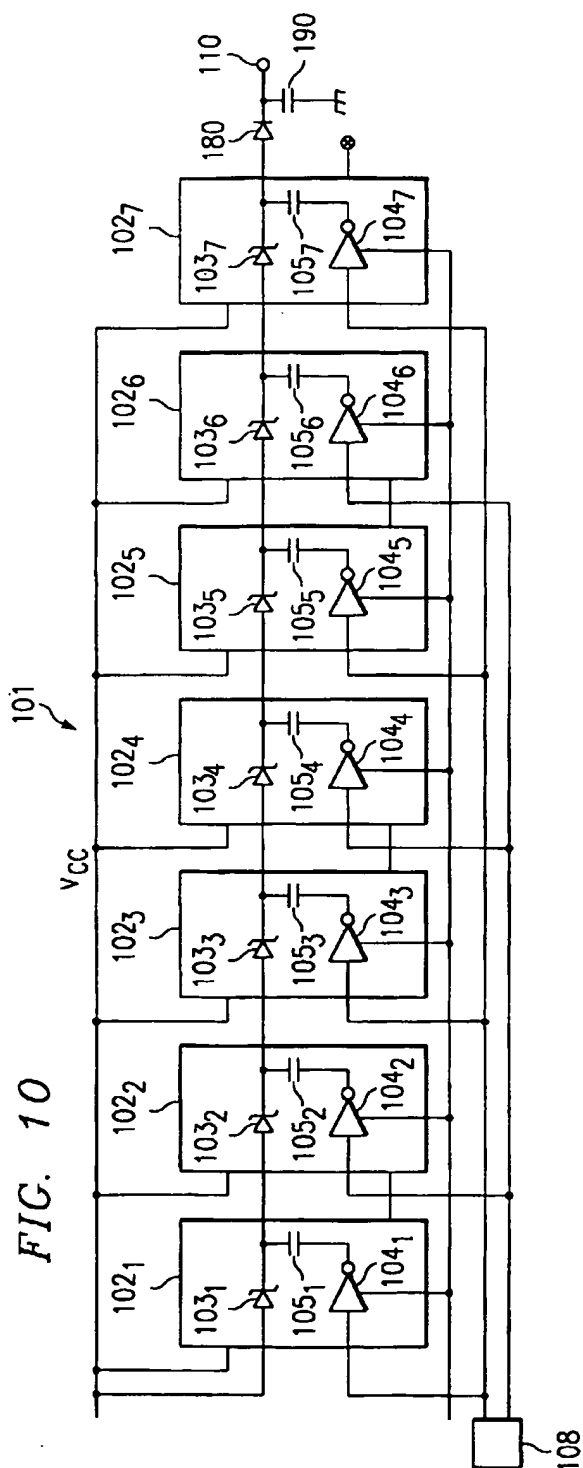


FIG. 8







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**BOOSTER CIRCUIT**

This application is a division of application No. 09/642, 280 filed Aug. 18, 2000, now U.S. Pat. No. 6,469,569.

**FIELD OF THE INVENTION**

The present invention pertains to a booster circuit. In particular, the present invention pertains to a charge-pump-type booster circuit used in power supply circuits, etc.

**BACKGROUND OF THE INVENTION**

Reference numeral 101 in FIG. 10 represents an example of a conventional booster circuit.

Said booster circuit 101 has multiple charge-pump circuits and is formed by connecting the charge-pump circuits in series. In this case, the booster circuit has 7 charge-pump circuits 102<sub>1</sub>–102<sub>7</sub>.

The input terminal of charge-pump circuit 102<sub>1</sub> of the first stage is connected to power supply voltage Vcc, and its output terminal is connected to charge-pump circuit 102<sub>2</sub> of the second stage.

The input terminals of the charge-pump circuits of the stages subsequent to the first stage are connected to the output terminals of the charge-pump circuits of the previous stages up to the last stage, that is, the input terminals of the charge-pump circuits 102<sub>2</sub>–102<sub>6</sub> of the second through sixth stages are connected to the output terminals of the charge-pump circuits of the respectively previous stage.

The input terminal of charge-pump circuit 102<sub>7</sub> of the last stage is connected to the output terminal of charge-pump circuit 102<sub>6</sub> of the previous stage, and its output terminal is connected to output terminal 110 via a diode 180 for preventing reverse current. The boosted voltage can be output from said output terminal 110 to the load circuit (not shown in the figure). Also, an output capacitor 190 is connected between output terminal 110 and ground.

The internal configuration of each charge-pump circuit 102 is the same. Each charge-pump circuit is comprised of diode 103, gate circuit 104, and capacitor 105.

The anode terminal of each diode 103 is used as the input terminal of each charge-pump circuit 102. The anode terminal of diode 103<sub>1</sub> of charge-pump circuit 102<sub>1</sub> of the first stage is connected to power supply voltage Vcc. The anode terminals of diodes 103<sub>2</sub>–103<sub>7</sub> of charge-pump circuits 102<sub>2</sub>–102<sub>7</sub> from the second stage on are connected to the cathode terminals of diodes 103<sub>1</sub>–103<sub>6</sub> of charge-pump circuits 102<sub>1</sub>–102<sub>6</sub> of the previous stage. The cathode terminal in charge-pump circuit 102<sub>7</sub> of the last stage is connected to output terminal 110 via diode 180 for preventing the flow of reverse current.

One terminal of each capacitor 105 is connected to the cathode terminal of one of diodes 103<sub>1</sub>–103<sub>7</sub>, and the other terminal of capacitor 105 is connected to the output terminal of gate circuit 104 to be described below.

Gate circuit 104 is an inverter circuit. The input terminal of the gate circuit is used as the control terminal of the charge-pump circuit where the control signal is input. When a high-level control signal is input, the terminal of capacitor 105 on the low-potential side is connected to ground GND. When a low-level control signal is input, the terminal of capacitor 105 on the low-potential side is connected to power supply voltage Vcc.

When a high-level control signal is input to gate circuit 104<sub>1</sub> of the first stage, gate circuit 104<sub>1</sub> of the first stage connects the terminal of capacitor 105<sub>1</sub> on the low-potential

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side of charge-pump circuit 102<sub>1</sub> of the first stage to ground GND. At that time, since the power supply voltage Vcc is applied to the anode terminal of diode 103<sub>1</sub> of charge-pump circuit 102<sub>1</sub> of the first stage, diode 103<sub>1</sub> is forward-biased, and capacitor 105<sub>1</sub> is charged to the power supply voltage Vcc.

Next, when a low-level control signal is input to gate circuit 104<sub>1</sub> of charge-pump circuit 102<sub>1</sub> in the first stage, the terminal of capacitor 105<sub>1</sub> on the low-potential side is connected to power supply voltage Vcc, and the voltage at the terminal of capacitor 105<sub>1</sub> on the high-potential side is boosted by as much as the power supply voltage Vcc from the charged voltage (Vcc) on capacitor 105<sub>1</sub> to become 2Vcc. Since the potential at the anode terminal of diode 103<sub>1</sub> in charge-pump circuit 102<sub>1</sub> of the first stage is the power supply voltage Vcc, which is less than the potential at the cathode terminal, diode 103<sub>1</sub> is reverse-biased.

In that state, gate circuit 104<sub>2</sub> of charge-pump circuit 102<sub>2</sub> of the second stage connects the terminal of capacitor 105<sub>2</sub> on the low-potential side to ground GND. Since 2Vcc is applied to the anode terminal of diode 103<sub>2</sub> of charge-pump circuit 102<sub>2</sub> of the second stage, diode 103<sub>2</sub> is forward-biased, and capacitor 105<sub>2</sub> of charge-pump circuit 102<sub>2</sub> of the second stage is charged by the boosted voltage 2Vcc.

Next, when gate circuit 104<sub>2</sub> of charge-pump circuit 102<sub>2</sub> of the second stage connects the terminal of capacitor 105<sub>2</sub> on the low-potential side to power supply voltage Vcc, the voltage at the terminal of capacitor 105<sub>2</sub> on the high-potential side is boosted by as much as the power supply voltage Vcc from the charged voltage (2Vcc) on capacitor 105<sub>2</sub> to become 3Vcc. Since the output voltage 2Vcc of charge-pump circuit 102<sub>1</sub> of the first stage is applied to the anode terminal of diode 103<sub>2</sub> of the second stage, diode 103<sub>2</sub> of the second stage is reverse-biased by the boosted voltage 3Vcc.

At that time, when a high level control signal is input to gate circuit 104<sub>3</sub> of charge-pump circuit 102<sub>3</sub> of the third stage, gate circuit 104<sub>3</sub> of charge-pump circuit 102<sub>3</sub> of the third stage connects the terminal of capacitor 105<sub>3</sub> on the low-potential side of the third stage to ground GND, and said capacitor 105<sub>3</sub> is charged by the boosted voltage 3Vcc on charge-pump circuit 102<sub>2</sub> of the second stage.

In said booster circuit 101, the voltage input to each of charge-pump circuits 102<sub>1</sub>–102<sub>6</sub> is boosted by as much as the power supply voltage Vcc as described above. As a result, a voltage equal to (number of charge-pump circuit stages+1)×Vcc, that is, 8Vcc is output from charge-pump circuit 102<sub>7</sub> of the last stage to a load circuit (not shown in the figure) via diode 180 which is used to prevent the flow of reverse current, at output terminal 110.

In the steady state, each capacitor 105 of said charge-pump circuit 102 is initially charged to a voltage corresponding to the number of stages of charge-pump circuits 102. On the other hand, since the voltage across the two terminals of each capacitor 105 is 0 V before the booster circuit is started, the amount of the electric charge on each capacitor 105 at steady state is greater than that when the booster circuit is started.

Conventionally, the time needed for each capacitor to be charged to a prescribed level when the booster circuit is started can be shortened by increasing the drivability of gate circuit 105 in advance. In this case, since each gate circuit 105 has a drivability higher than the essential level in the steady state, power consumption and noise also become higher than the essential level in the steady state.

In said booster circuit 101, when a high-level control signal is input to gate circuit 104<sub>n</sub> of charge-pump circuit

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102<sub>n</sub> of a given stage to boost the voltage by as much as the power supply voltage V<sub>cc</sub>, low level signals must be input to gate circuits 104<sub>n-1</sub> and 104<sub>n+1</sub> of the charge-pump circuits of the previous and subsequent stages. Therefore, it is preferred to input control signals of opposite phase to the gate circuits of neighboring stages.

Consequently, said conventional booster circuit 101 has a signal-generating circuit 108 used for generating control signals. The same first control signal is input to gate circuits 104<sub>1</sub>, 104<sub>3</sub>, 104<sub>5</sub>, and 104<sub>7</sub> of the charge-pump circuits of the odd-numbered stages, while a second control signal of different phase than the first control signal is input to gate circuits 104<sub>2</sub>, 104<sub>4</sub>, and 104<sub>6</sub> of the charge-pump circuits of the even-numbered charge-pump circuits. In this case, the first and second control signals have opposite phase.

In this case, since the same first control signal is input to gate circuits 104<sub>1</sub>, 104<sub>3</sub>, 104<sub>5</sub>, and 104<sub>7</sub> in the charge-pump circuits of the odd-numbered stages, when the logic level of the first control signal is switched, the logic level of the output signals of gate circuits 104<sub>1</sub>, 104<sub>3</sub>, 104<sub>5</sub>, and 104<sub>7</sub> are switched at the same time.

On the other hand, since the same second control signal is input to gate circuits 104<sub>2</sub>, 104<sub>4</sub>, and 104<sub>6</sub> of the charge-pump circuits of the even-numbered stages, when the logic level of the second control signal is switched, the logic levels of the output signals of said gate circuits 104<sub>2</sub>, 104<sub>4</sub>, and 104<sub>6</sub> are switched at the same time.

When the logic level of the output signal of each gate circuit 104 is switched, charging/discharging of capacitor 105 is switched, and current flows to each gate circuit 104. FIG. 11 shows the relationship between the output signal of the gate circuits and the sum I<sub>ca</sub> of the currents flowing to all of gate circuits 104<sub>1</sub>-104<sub>7</sub>.

When the logic level of the output signal is switched, the current flowing to each gate circuit 104 is very small. In the conventional booster circuit, however, since the logic levels of the output signals of gate circuits 104<sub>1</sub>, 104<sub>3</sub>, 104<sub>5</sub>, and 104<sub>7</sub> of the odd-numbered stages as well as gate circuits 104<sub>2</sub>, 104<sub>4</sub>, and 104<sub>6</sub> of the even-numbered stages are switched at the same time and capacitors connected to the various gate circuits are charged/discharged at the same time, the currents are concentrated to result in a large current when the logic level is switched. As a result, the switching noise level becomes high.

The purpose of the present invention is to solve the aforementioned problem of the conventional technology by providing a booster circuit which can reduce the power consumption and the switching noise level.

#### SUMMARY OF THE INVENTION

In order to realize the aforementioned purpose, claim 1 of the present invention provides a booster circuit characterized by the following facts: the booster circuit has N rectifying elements which are electrically connected in series between a voltage input terminal and a voltage output terminal with the terminal on the anode side taken as the aforementioned voltage input terminal side; N capacitors, each of which has one of the terminals electrically connected to the terminal on the cathode side of one of the aforementioned rectifying elements; N drive circuits, each of which has its output terminal electrically connected to the other terminal of the aforementioned capacitor and is able to drive the other terminal of the aforementioned capacitor to a first voltage or a second voltage as a function of a control signal; a signal supply circuit which supplies a first control signal to the aforementioned drive circuits of the odd-numbered stages

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and supplies a second control signal whose phase is opposite to that of the first control signal to the drive circuits of the even-numbered stages; and an output circuit which monitors the output voltage at the aforementioned voltage output terminal and outputs a disable signal to each of the aforementioned drive circuits when the aforementioned output voltage is above a prescribed level; wherein each of the aforementioned drive circuits has first and second drive units which can drive the other terminal of the aforementioned capacitor to the first or second voltage; and wherein the aforementioned second drive unit is able to suspend driving of the other terminal of the aforementioned capacitor as a function of the aforementioned disable signal.

According to claim 2 of the present invention, the booster circuit described in claim 1 has a diode for preventing reverse current that is electrically connected between the terminal on the cathode side of the rectifying element of the Nth stage and the aforementioned voltage output terminal, and an output capacitor which is connected between the aforementioned voltage output terminal and reference potential where the aforementioned rectifying elements are diodes.

Claim 3 of the present invention provides a booster circuit characterized by the following facts: the booster circuit has N rectifying elements that are electrically connected in series between a voltage input terminal and a voltage output terminal with the terminal on the anode side taken as the aforementioned voltage input terminal side; N capacitors, each of which has one of the terminals electrically connected to the terminal on the cathode side of one of the aforementioned rectifying elements; and a signal supply circuit which supplies a first control signal to the aforementioned capacitors of the odd-numbered stages and supplies a second control signal whose phase is opposite to that of the first control signal to the capacitors of the even-numbered stages; a first time delay is applied sequentially to the first control signal supplied to the other terminal of each capacitor of the odd-numbered stages, and a second time delay is applied sequentially to the second control signal supplied to the other terminal of each capacitor of the even-numbered stages.

According to claim 4 of the present invention, the booster circuit described in claim 3 has a diode for preventing reverse current, which is electrically connected between the terminal on the cathode side of the rectifying element of the Nth stage and the aforementioned voltage output terminal, and an output capacitor which is connected between the aforementioned voltage output terminal and reference potential where the aforementioned rectifying elements are diodes, and the aforementioned signal supply circuit is composed of a ring oscillator.

The booster circuit of the present invention has a first drive unit (charging/discharging circuit) and a second drive unit (auxiliary charging/discharging circuit). The charging/discharging circuit can operate independently or together with the auxiliary charging/discharging circuit.

When the booster circuit is started, both the charging/discharging circuit and the auxiliary charging/discharging circuit are operated together to increase the drivability of the drive circuits (gate circuits) to shorten the capacitor charging time. On the other hand, when the charging/discharging circuit is operated independently in the steady state, which does not require a high drivability, the drivability becomes lower than that at the time when the booster circuit is started. Consequently, the power consumption and noise can be reduced compared with the conventional booster circuit which uses gate circuits with high drivability.

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The output voltage (boosted voltage) is at a high level in the steady state but at a low level when the booster circuit is started. Therefore, it is possible to detect whether the booster circuit is in steady state or has just been started by detecting the output of the booster circuit.

Consequently, when the booster circuit is started with the output of the booster circuit at a low level, the charging/discharging circuit is operated together with the auxiliary charging/discharging circuit. When the booster circuit is steady state with the output at a high level, the charging/discharging circuit is operated independently. In this way, the drivability can be increased only when the booster circuit is started.

In another booster circuit of the present invention, the first and second control signals generated in the signal supply circuit (timing control circuit) are applied to the charge-pump circuits comprised of rectifying elements and capacitors in each stage after the control signals are delayed by different periods of time for each charge-pump circuit, respectively. Since each charge-pump circuit is synchronized with the input control signal to perform switching between charging and discharging of a capacitor, the charging/discharging states of the capacitors arranged in the various charge-pump circuits are switched at completely different times, and it is possible to avoid the situation that the charging/discharging states of two or more capacitors are switched at the same time.

In another booster circuit of the present invention, the timing control circuit is made of a ring oscillator comprised of multiple inverters. The output signals of the inverters are input to the charge-pump circuits.

In particular, when the number of inverter stages is equal to the number of charge-pump stages and the output signal of each inverter is input to a charge-pump circuit, in a ring oscillator comprised of N inverters and having a period of T, the signal input to each inverter is delayed by  $(T/(2 \times N))$ . Consequently, the output signals of the inverters are always switched one at a time.

Since each charge-pump circuit switches the charging/discharging state of the capacitor of each charge-pump circuit as a result of switching of the output signal of the inverter, the charging/discharging states of the capacitors can always be switched one at a time.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating the booster circuit disclosed in an embodiment of the present invention.

FIG. 2 is a circuit diagram illustrating the relationship between the gate circuits and the auxiliary control circuit of the booster circuit disclosed in an embodiment of the present invention.

FIG. 3 is a diagram illustrating the waveform of the output voltage of each charge-pump circuit when the booster circuit of the present invention is started.

FIG. 4 is a diagram illustrating the steady-state output voltage waveform of each charge-pump circuit of the booster circuit disclosed in the present invention.

FIG. 5(a) is a diagram illustrating the waveform of the current flowing in a gate circuit with a high drivability.

FIG. 5(b) is a diagram illustrating the waveform of the current flowing in a gate circuit with a low drivability.

FIG. 6 is a circuit diagram illustrating the booster circuit disclosed in another embodiment of the present invention.

FIG. 7 is a waveform diagram explaining the operation of the ring oscillator in the booster circuit disclosed in another embodiment of the present invention.

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FIG. 8 is a diagram explaining a variant of the booster circuit disclosed in another embodiment of the present invention.

FIG. 9 is a circuit diagram illustrating the booster circuit disclosed in yet another embodiment of the present invention.

FIG. 10 is a circuit diagram illustrating an example of the conventional booster circuit.

FIG. 11 is a waveform diagram explaining the operation of the conventional booster circuit.

#### REFERENCE NUMBERS AND SYMBOLS AS SEEN IN THE DRAWINGS

1, 31, 41, 51, Booster circuits, 2<sub>1</sub>-7, 3<sub>1</sub>-31, charge-pump circuits, 3<sub>1</sub>-37, 33<sub>1</sub>-337, diodes, 4<sub>1</sub>-47, 34<sub>1</sub>-347, gate circuits, 5<sub>1</sub>-57, 35<sub>1</sub>-357, capacitors, 38, 48 ring oscillator auxiliary, control circuit 58 timing control circuit.

#### DESCRIPTION OF EMBODIMENTS

In the following, an embodiment of the present invention will be explained with reference to figures. Reference numeral 1 in FIG. 1 represents the booster circuit in an embodiment of the present invention.

Said booster circuit 1 has seven charge-pump circuits 2<sub>1</sub>-2<sub>7</sub>, a signal-generating circuit 8, an auxiliary control circuit 9, a diode 80 for preventing reverse current, an output capacitor 90 and an output terminal 10.

Said charge-pump circuits 2<sub>1</sub>-2<sub>7</sub> are connected to each other in series. The input terminal of charge-pump circuit 2<sub>1</sub> of the first stage is connected to the power supply voltage Vcc, and the output terminal is connected to the input terminal of charge-pump circuit 2<sub>2</sub> of the second stage.

The input terminals of the charge-pump circuits of the stages subsequent to the first stage are connected to the output terminals of the charge-pump circuit in the previous stages up to the last stage, that is, the input terminals of the second through sixth charge-pump circuits 2<sub>2</sub>-2<sub>6</sub> are connected to the output terminals of the charge-pump circuits 2<sub>1</sub>-2<sub>5</sub> of the respectively previous stage. The output terminals are connected to the input terminals of the charge-pump circuits 2<sub>3</sub>-2<sub>7</sub> of the respectively following stage.

The input terminal of charge-pump circuit 2<sub>7</sub> of the last stage is connected to the output terminal of charge-pump circuit 2<sub>6</sub> of the previous stage, and the output terminal is connected to output terminal 10 of booster circuit 1 via diode 80 used for preventing reverse current. Also, output terminal 10 is connected to a load circuit (not shown in the figure).

The input terminal of auxiliary control circuit 9 is connected to output terminal 10 to detect the magnitude of the output voltage and output an auxiliary control signal. Each charge-pump circuit 2 has a gate circuit 4. The aforementioned auxiliary control signal is output to each gate circuit 4.

In addition to said gate circuit 4 each charge-pump circuit 2 has a diode 3 and a capacitor 5.

The anode terminal of diode 3 is used as the input terminal of each charge-pump circuit 2. The anode terminal of diode 3<sub>1</sub> of charge-pump circuit 2<sub>1</sub> of the first stage is connected to power supply voltage Vcc. The anode terminals of diodes 3<sub>2</sub>-3<sub>7</sub> of charge-pump circuits 2<sub>2</sub>-2<sub>7</sub> from the second stage on are connected to the cathode terminals of diodes 3<sub>1</sub>-3<sub>6</sub> of charge-pump circuits 2<sub>1</sub>-2<sub>6</sub> of the respectively previous stages. The cathode terminal of diode 3<sub>7</sub> of charge-pump circuit 2<sub>7</sub> of the last stage is connected to output terminal 10 via diode 80 used for preventing the flow of reverse current.

One terminal of each of capacitors  $5_1$ - $5_7$  is connected to the cathode terminal of one of diodes  $3_1$ - $3_7$ , while the other terminal is connected to the output terminal of one of gate circuits  $4_1$ - $4_7$ .

When a high-level control signal is input from signal-generating circuit 8 to gate circuit  $4_1$  of the first stage, the output voltage of gate circuit  $4_1$  of the first stage goes to ground potential GND, and the terminal of capacitor  $5_1$  on the low-potential side of charge-pump circuit  $2_1$  of the first stage is connected to ground potential GND. At that time, diode  $3_1$  is forward-biased by the power supply voltage Vcc applied to the anode terminal of diode  $3_1$  of the first stage, and capacitor  $5_1$  of the first stage is charged by the power supply voltage Vcc.

Next, when a low level control signal is input from signal-generating circuit 8 to gate circuit  $4_1$  in the first stage, the terminal of capacitor  $5_1$  on the low-potential side is connected to the power supply voltage Vcc, and the potential at the terminal of capacitor  $5_1$  on the high-potential side is boosted by as much as the power supply voltage Vcc from the charged voltage on capacitor  $5_1$ . Diode  $3_1$  of charge-pump circuit  $2_1$  of the first stage is reverse-biased by the boosted voltage.

When a high level control signal is input to gate circuit  $4_2$  of charge-pump circuit  $2_2$  of the second stage in that state, the terminal of capacitor  $5_2$  on the low-potential side in charge-pump circuit  $2_2$  of the second stage is connected to ground GND. Diode  $3_2$  of charge-pump circuit  $2_2$  of the second stage is forward-biased by the output voltage of charge-pump circuit  $2_1$  of the first stage. When capacitor  $5_2$  of charge-pump circuit  $2_2$  of the second stage is charged, charge is sent from capacitor  $5_1$  of the first stage to capacitor  $5_2$  of the second stage.

Next, when a low-level control signal is input to gate circuit  $4_2$  of charge-pump circuit  $2_2$  of the second stage, the terminal of capacitor  $5_2$  on the low-potential side of the second stage is connected to the power supply voltage Vcc. The potential at the terminal of capacitor  $5_2$  on the high-potential side of the second stage is boosted by as much as the power supply voltage Vcc from the charged voltage of capacitor  $5_2$  of the second stage, and diode  $3_2$  is reverse-biased by the boosted voltage.

At that time, when a high level control signal is input to gate circuit  $4_3$  of charge-pump circuit  $2_3$  of the third stage, gate circuit  $4_3$  in charge-pump circuit  $2_3$  of the third stage connects the terminal of capacitor  $5_3$  of charge-pump circuit  $2_3$  of the third stage to ground GND. Capacitor  $5_3$  of the third stage is charged by the output voltage of charge-pump circuit  $2_2$  of the second stage, and charge is sent from capacitor  $5_2$  of the second stage to capacitor  $5_3$  in the third stage.

When capacitors  $5_1$ - $5_7$  are respectively charged by charge-pump circuits  $2_1$ - $2_7$ , charge is sent sequentially to capacitor  $5_7$  of charge-pump circuit  $2_7$  of the last stage, and the voltage input to each of charge-pump circuits  $2_1$ - $2_7$  can be boosted. From the high-voltage side terminal of capacitor  $5_7$  of charge-pump circuit  $2_7$  of the last stage, the boosted voltage can be supplied from the output terminal to a load circuit via diode 80 for preventing the flow of reverse current.

As shown in FIG. 2, each of said gate circuits 4 has input terminal 15, output terminal 16, charging/discharging circuit 11, auxiliary charging/discharging circuit 12.

Input terminal 15 is connected to the output terminal of said signal-generating circuit 8, while output terminal 16 is connected to the terminal of capacitor 5 on the low voltage side.

Charging/discharging circuit 11 has push-pull connected pnp and npn output transistors 21 and 22 as well as npn drive transistor 26.

The emitter terminal of drive transistor 26 is grounded, and the collector terminal is connected to the power supply voltage and the base terminal of pnp output transistor 21 via a resistor.

The collector terminal of pnp output transistor 21 is connected to the collector terminal of npn output transistor 22, and the emitter terminal is connected to the power supply voltage Vcc. The emitter terminal of npn output transistor 22 is grounded.

In charging/discharging circuit 11, when a control signal is input to input terminal 15 of the gate circuit, the control signal is input to the base terminal of npn output transistor 22 and also input to the base terminal of drive transistor 26 after being inverted by an inverter. The two collector terminals of output transistors 21 and 22 are both connected to output terminal 16 of the gate circuit.

When a low-level control signal is input to input terminal 15 of gate circuit 4, driving transistor 26 conducts since an inverted high level signal is input at its base terminal. As a result, the base potential of pnp output transistor 21 drops to reach a conductive state. At that time, since npn output transistor 22 is off since a low-level signal is input at its base terminal, output terminal 16 of the gate circuit is connected to the power supply voltage Vcc via pnp transistor 21, and the terminal of capacitor 5 on the low voltage side is connected to the power supply voltage Vcc.

On the other hand, when a high level control signal is input to input terminal 15, the aforementioned operation is reversed. Since pnp transistor 21 and npn transistor 22 become nonconducting and conducting, respectively, output terminal 16 of the gate circuit is connected to the ground potential via npn transistor 22, and the terminal of capacitor 5 on the low-voltage side is grounded.

Said auxiliary charging/discharging circuit 12 has npn drive transistor 25 as well as pnp and npn output transistors 23 and 24. These transistors respectively correspond to drive transistor 26 and output transistors 21 and 22 of said charging/discharging circuit 11. Since the internal configuration of auxiliary charging/discharging circuit 12 is identical to that of charging/discharging circuit 11, its detailed explanation has been omitted.

Said auxiliary charging/discharging circuit 12 is connected in parallel with charging/discharging circuit 11 between input and output terminals 15, 16 of gate circuit 4 and can operate together with charging/discharging circuit 11. Said auxiliary charging/discharging circuit 12 is operated under the control of auxiliary control circuit 9 and is able to operate together with charging/discharging circuit 11.

Said auxiliary control circuit 9 has Zener diode 61, inverter 62, npn detecting transistor 27, npn control transistors 28 and 29.

The cathode terminal of Zener diode 61 is connected to output terminal 10 of the booster circuit via an auxiliary control terminal 17, and its anode terminal is connected to the base terminal of detecting transistor 27. The diode conducts when the potential at output terminal 10 of the booster circuit goes high. As a result, the potential at the base terminal of detecting transistor 27 goes high. Also, the base terminal of detecting transistor 27 is connected to ground via a resistor.

The emitter terminal of detecting transistor 27 is connected to ground potential. Its collector terminal is con-

connected to the power supply voltage  $V_{cc}$  via a resistor and is also connected to the input terminal of inverter 62. The transistor conducts when the potential at the base terminal goes high. The input terminal of the inverter is connected to ground potential. The potential at the input terminal of inverter 62 is kept at the low level.

The output terminal of inverter 62 is connected to the base terminals of control transistors 28 and 29 via a resistor. When the potential at the input terminal is at the low level, a high-level signal is output to the base terminals of control transistors 28 and 29.

The collector terminals of control transistors 28 and 29 are connected to the base terminals of npn transistor 24 of auxiliary charging/discharging circuit 12 and drive transistor 25, respectively. The emitter terminals are connected to ground potential. The transistors conduct when the potential at the base terminal is at the high level.

When control transistors 28 and 29 conduct, the base terminals of drive transistor 25 and npn output transistor 24 of auxiliary charging/discharging circuit 12 are connected to ground potential via control transistors 28 and 29, respectively. As a result, the operations of driving transistor 25 and npn output transistor 24 of auxiliary charging/discharging circuit 12 are stopped, and the operation of auxiliary charging/discharging circuit 12 is disabled.

FIG. 3 shows the waveform of the output voltage of each charge-pump circuit 2 when booster circuit 1 is started. In FIG. 3, C1, C2, and C3 respectively represent the output voltage waveforms of charge-pump circuits 2<sub>1</sub>, 2<sub>2</sub>, and 2<sub>3</sub> of the corresponding first, second, and third stages.

When booster circuit 1 is started, a low voltage appears at output terminal 10 of booster circuit 1. Therefore, Zener diode 61 of auxiliary control circuit 9 is non-conducting, as is detection transistor 27. As a result, the input voltage of inverter 62 is on the high level. Consequently, the output voltage of inverter 62 is low and low voltage is applied to the base terminals of control transistors 28 and 29. As a result, both control transistors 28 and 29 are nonconducting.

Since the base terminals of drive transistor 25 and npn output transistor 24 in auxiliary charging/discharging circuit 12 are not connected to the ground potential via control transistors 28 and 29, drive transistor 25 and output transistor 24 operate corresponding to the potential at input terminal 15 of the gate circuit, and auxiliary charging/discharging circuit 12 operates together with charging/discharging circuit 11. When charging/discharging circuit 11 operates together with auxiliary charging/discharging circuit 12, the drivability of gate circuit 4 is increased.

When each capacitor 5 is charged/discharged by a gate circuit 4 with a high drivability and charge is transferred sequentially from charge-pump circuit 2<sub>1</sub> of the first stage to charge-pump circuit 2<sub>7</sub> of the last stage, the voltage at output terminal 10 of booster circuit 1 is able to rise and soon reach the steady state. FIG. 4 shows the output voltage of each charge-pump circuit at steady state. In FIG. 4, CLK represents the waveform of the control signal input to charge-pump circuit 22 of the second stage. C1, C2, and C3 respectively represent the waveforms of the output voltages of charge-pump circuits 2<sub>1</sub>, 2<sub>2</sub>, and 2<sub>3</sub> of the corresponding first, second, and third stages.

At steady state, charge-pump circuit 21 of the first stage boosts the input power supply voltage  $V_{cc}$  by  $V_{cc}$  and outputs the boosted voltage  $2V_{cc}$  to charge-pump circuit 22 of the second stage. Charge-pump circuit 2<sub>2</sub> of the second stage boosts the boosted voltage  $2V_{cc}$  from charge-pump circuit 2<sub>1</sub> of the first stage by  $V_{cc}$  and outputs this boosted

voltage to charge-pump circuit 2<sub>3</sub> of the third stage. Each of charge-pump circuits 2<sub>1</sub>-2<sub>7</sub> boosts the input voltage by  $V_{cc}$ . Consequently, a voltage equal to the (number of charge-pump circuit stages+1)× $V_{cc}$ , that is,  $8V_{cc}$  is output from charge-pump circuit 2<sub>7</sub> of the last stage. The output voltage is output to a load circuit (not shown in the figure) via diode 80 which prevents the flow of reverse current, and output terminal 10.

At steady state, since the voltage at output terminal 10 of the booster circuit is at the high level, Zener diode 61 of auxiliary control circuit 9 conducts. Detection transistor 27 also conducts. As a result, the input terminal of inverter 62 is connected to ground via detection transistor 27. Consequently, the output voltage of inverter 62 reaches the high level, and both control transistors 28 and 29 conduct.

Since the base terminals of drive transistor 25 and output transistor 24 of auxiliary charging/discharging circuit 12 are connected to ground via control transistors 29 and 28, respectively, drive transistor 25 and output transistor 24 are off, and the operation of auxiliary charging/discharging circuit 12 is disabled. When the operation of auxiliary charging/discharging circuit 12 is disabled, charging/discharging circuit 11 operates independently in the steady state. When the charging/discharging circuit operates independently, the drivability of gate circuit 4 is less than that when the charging/discharging circuit operates together with the auxiliary charging/discharging circuit.

Next, when current flows to the load circuit, the charge on capacitor 5<sub>7</sub> of the last stage is reduced, and the charge deficit can be restored by transferring charge from the previous stage to the next stage. In this case, however, charging/discharging circuit 11 also operates independently, and the drivability of each gate circuit 4 is kept low.

As explained above, when booster circuit 1 is started, charging/discharging circuit 11 operates together with auxiliary charging/discharging circuit 12 to increase the drivability of gate circuit 4. At steady state, charging/discharging circuit 11 operates independently. As a result, the drivability of gate circuit 4 is reduced.

FIGS. 5(a) and 5(b) show the waveforms of the currents flowing from the side of power supply voltage  $V_{cc}$  to each gate circuit for the case when gate circuits with high drivability are used and for the case when gate circuits with low drivability are used, respectively. As shown in FIGS. 5(a) and 5(b), when gate circuits with high drivability are used, the inrush current that flows at the time of switching is high. When gate circuits with low drivability are used, the current that flows at the time of switching is low.

In the conventional booster circuit which uses gate circuits with constantly high drivability, since a large inrush current as shown in FIG. 5(a) flows at steady state, the loss in the power consumption, and the noise level are high. In the present embodiment, however, since high drivability is required when the booster circuit is started, the drivability of each gate circuit 4 is increased by operating charging/discharging circuit 11 together with auxiliary charging/discharging circuit 12. On the other hand, at steady state when high drivability is unnecessary, charging/discharging circuit 11 is operated independently to reduce the drivability of gate circuit 4. As a result, the current is reduced as shown in FIG. 5(b). Consequently, compared with the conventional case, the loss in power consumption and noise can be reduced at steady state.

Another embodiment of the present invention will be explained below. In FIG. 6, 31 represents the booster circuit disclosed in another embodiment of the present invention.



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Like booster circuit 1 shown in FIG. 1, said booster circuit 31 is constituted by connecting multiple charge-pump circuits in series. In this case, seven charge-pump circuits 32<sub>1</sub>-32<sub>7</sub> are interconnected to each other in series.

Like charge-pump circuits 2<sub>1</sub>-2<sub>7</sub> shown in FIG. 1, said charge-pump circuits 32<sub>1</sub>-32<sub>7</sub> also have diodes 33<sub>1</sub>-33<sub>7</sub> and capacitors 35<sub>1</sub>-35<sub>7</sub>, respectively. However, gate circuits 34<sub>1</sub>-34<sub>7</sub> used for controlling charging/discharging of capacitors 35<sub>1</sub>-35<sub>7</sub> comprise inverters and are arranged outside charge-pump circuits 32<sub>1</sub>-32<sub>7</sub>. This is different from charge-pump circuits 2<sub>1</sub>-2<sub>7</sub> shown in FIG. 1.

Said gate circuits 34<sub>1</sub>-34<sub>7</sub> are interconnected in series. The output of gate circuit 34<sub>7</sub> of the last stage is input to gate circuit 34<sub>1</sub> of the first stage. A ring oscillator 38 comprises said gate circuits 34<sub>1</sub>-34<sub>7</sub>.

The output terminals of gate circuits 34<sub>1</sub>-34<sub>7</sub> are connected to the terminals of capacitors 35<sub>1</sub>-35<sub>7</sub> on the low-potential side of charge-pump circuits 32<sub>1</sub>-32<sub>7</sub>, respectively. When the output signal is on the low level or high level, said gate circuits 34<sub>1</sub>-34<sub>7</sub> can connect the terminals of capacitors 35<sub>1</sub>-35<sub>7</sub> on the low-potential side to ground or the power supply voltage to charge/discharge capacitors 35<sub>1</sub>-35<sub>7</sub>.

The operation of ring oscillator 38 will be explained below. FIG. 7 shows the waveforms of output voltages 37<sub>1</sub>-37<sub>7</sub> of gate circuits 34<sub>1</sub>-34<sub>7</sub>.

Gate circuits 34<sub>1</sub>-34<sub>7</sub> of ring oscillator 38 invert the input signal and output it to the gate circuit of the next stage after delaying the input signal by a time period  $\tau$ .

When the output signal of gate circuit 34<sub>1</sub> of the first stage is at the high level, a high level signal is input to gate circuit 34<sub>2</sub> of the second stage, inverted to the low level, delayed by  $\tau$ , and then output to gate circuit 34<sub>3</sub> of the third stage. The low-level signal input to gate circuit 34<sub>3</sub> of the third stage is inverted to the high level in gate circuit 34<sub>3</sub> of the third stage, delayed by  $\tau$ , and then output to gate circuit 34<sub>4</sub> of the fourth stage. The output signal of gate circuit 34<sub>4</sub> of the first stage is sequentially reversed and delayed by  $\tau$  in gate circuits 34 and is ultimately output to gate circuit 34<sub>7</sub> of the last stage.

The output signal of gate circuit 34<sub>7</sub> of the last stage is inverted a total of 6 times by gate circuits 34<sub>2</sub>-34<sub>7</sub> from the second stage to the last stage. Then, the output signal of the final gate circuit which is at the high level is output to the input terminal of gate circuit 34<sub>1</sub> in the first stage. After that, a low-level signal is output from gate circuit 34<sub>1</sub> of the first stage, successively inverted by each of the gate circuits 34<sub>2</sub>-34<sub>7</sub>, and output to the gate circuit of the next stage.

When signals are inverted and transferred by gate circuits 34<sub>1</sub>-34<sub>7</sub> as described above, the signals from two neighboring gate circuits will be output out of phase. The power supply voltage  $V_{cc}$  input to charge-pump circuit 32<sub>1</sub> of the first stage is sequentially boosted by as much as the power supply voltage  $V_{cc}$  by each of the charge-pump circuits 32<sub>1</sub>-32<sub>7</sub>. As a result, a boosted voltage equal to (the number of stages of the charge-pump circuits+1) $\times V_{cc}$  is output from charge-pump circuit 32<sub>7</sub> of the last stage to a load circuit (not shown in the figure) via diode (80), which prevents the flow of reverse current, and output terminal 10.

The number of stages of gate circuits 34<sub>1</sub>-34<sub>7</sub> is 7. The signal delayed by a time period  $\tau$  of each of the gate circuits 34<sub>1</sub>-34<sub>7</sub> will return to the original phase when delayed  $7 \times 2$  times. Therefore, if the oscillation period of the ring oscillator is  $T$ , the relationship  $7 \times 2\tau = T$  can be obtained, and the time delay  $\tau$  of each gate circuit will be  $T/14$ .

Consequently, when the logic level of the output signal of one of gate circuits 34<sub>1</sub>-34<sub>7</sub> is switched, the logic level of

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the output signal of gate circuits 34<sub>2</sub>-34<sub>7</sub> of the next stage will be switched after a period of  $\tau = T/14$  since the point in time that the logic level of the output signal of said one of gate circuits 34<sub>1</sub>-34<sub>7</sub> is switched.

In said gate circuits 34<sub>1</sub>-34<sub>7</sub>, since the logic level of each output signal is sequentially delayed by  $T/14$  before it is switched, the logic levels of the output signals will not be switched simultaneously in two or more gate circuits.

Current will flow to each of gate circuits 34<sub>1</sub>-34<sub>7</sub> when the logic level of the output signal is switched. However, as described above, the logic levels of the output signals are not switched simultaneously for two or more gate circuits, unlike the case of the conventional technology, where a large current flows because the logic levels of the output signals of all of the gate circuits are switched at the same time. As shown in FIG. 7, the sum of the currents  $I_{ca}$  flowing to various gate circuits 34 is reduced. Therefore, the noise can also be reduced.

In the circuit shown in FIG. 6, ring oscillator 38 comprises gate circuits 34<sub>1</sub>-34<sub>7</sub> which charge/discharge capacitors 35<sub>1</sub>-35<sub>7</sub>, respectively. However, the present invention is not limited to this constitution. For example, as shown by symbol 41 in FIG. 8, seven inverters 39<sub>1</sub>-39<sub>7</sub> are used in addition to gate circuits 34<sub>1</sub>-34<sub>7</sub>. A ring oscillator 48 comprises said inverters 39<sub>1</sub>-39<sub>7</sub>. The outputs of said inverters 39<sub>1</sub>-39<sub>7</sub> are input to gate circuits 34<sub>1</sub>-34<sub>7</sub> for charging/discharging, respectively.

When gate circuits 34<sub>1</sub>-34<sub>7</sub> for charging/discharging are separated from ring oscillator 48, the influence of the change in the load can be eliminated.

Also, as shown in FIG. 9, instead of ring oscillator 48 used in booster circuit 41 shown in FIG. 8, it is also possible to use a signal-generating circuit 8 and a timing control circuit 58.

Timing control circuit 58 has first through seventh delay circuits 54<sub>1</sub>-54<sub>7</sub>.

Among the first through seventh delay circuits 54<sub>1</sub>-54<sub>7</sub>, the first, third, fifth, and seventh delay circuits 54<sub>1</sub>, 54<sub>3</sub>, 54<sub>5</sub>, and 54<sub>7</sub> are connected to each other in series, while the second, fourth, and sixth delay circuits 54<sub>2</sub>, 54<sub>4</sub>, and 54<sub>6</sub> are also connected to each other in series. The input terminals of the first and second delay circuits 54<sub>1</sub> and 54<sub>2</sub> are connected to the output terminal of signal-generating circuit 8. The time delay of the first delay circuit 54<sub>1</sub> is taken as  $\Delta t$ , while the time delays of the second through seventh delay circuits 54<sub>2</sub>-54<sub>7</sub> are taken as  $2\Delta t$ .

When a control signal is output from signal-generating circuit 8 to the first delay circuit 54<sub>1</sub>, the control signal is delayed by a period of  $\Delta t$  by the first delay circuit 54<sub>1</sub> and output to the third delay circuit 54<sub>3</sub>. Then, the control signal is delayed by  $2\Delta t$  by each of the third, fifth, and seventh delay circuits 54<sub>3</sub>, 54<sub>5</sub>, and 54<sub>7</sub>.

Consequently, in the third delay circuit 54<sub>3</sub>, the control signal is delayed by  $(\Delta t + 2\Delta t) = 3\Delta t$ , that is, the sum of the time delay  $\Delta t$  of the first delay circuit 54<sub>1</sub> and the time delay  $2\Delta t$  of the third delay circuit 54<sub>3</sub> before it is output. Similarly, in the fifth delay circuit 54<sub>5</sub>, the control signal is delayed by  $(\Delta t + 2\Delta t + 2\Delta t) = 5\Delta t$  before it is output. In the seventh delay circuit 54<sub>7</sub>, the control signal is delayed by  $(\Delta t + 2\Delta t + 2\Delta t + 2\Delta t) = 7\Delta t$  before it is output.

On the other hand, when a control signal with a phase opposite to that of the control signal input to the first delay circuit 54<sub>1</sub> is input to the second delay circuit 54<sub>2</sub>, the control signal is delayed by  $2\Delta t$  by each of the second, fourth, and sixth delay circuits 54<sub>2</sub>, 54<sub>4</sub>, and 54<sub>6</sub>. Therefore,

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the control signal is delayed by  $2\Delta t$ ,  $4\Delta t$ , and  $6\Delta t$ , respectively, when it is output from the second, fourth, and sixth delay circuits  $54_2$ ,  $54_4$ , and  $54_6$ .

When the logic level of the control signal input to the first delay circuit  $54_1$  is switched, the logic level of the output signal of the first delay circuit  $54_1$  is switched after a period of  $\Delta t$  since the point in time that the logic level of the control signal is switched. Similarly, the logic levels of the output signals of the third, fifth, and seventh delay circuits  $54_3$ ,  $54_5$ , and  $54_7$  are switched after  $3\Delta t$ ,  $5\Delta t$ , and  $7\Delta t$  since the point in time that the logic level of the input control signal is switched, respectively. On the other hand, when the logic level of the control signal input to the second delay circuit  $54_2$  is switched, the logic level of the output of the second delay circuit  $54_2$  is switched after a period of  $2\Delta t$  since the point in time that the logic level of the control signal is switched. Similarly, the logic levels of the output signals of the fourth and sixth delay circuits  $54_4$  and  $54_6$  are switched after  $4\Delta t$  and  $6\Delta t$  since the point in time that the logic level of the control signal is switched, respectively.

Since the control signals input to the first and second delay circuits  $54_1$  and  $54_2$  are out of phase, the logic levels are switched almost simultaneously between the control signals. However, as described above, in the first to the seventh delay circuits  $54_1$ – $54_7$ , the logic level of each output signal is switched after a different time delay in the range of  $\Delta t$ – $7\Delta t$  from the point in time that the logic level of each control signal is switched. Consequently, the logic levels of the output signals of two or more delay circuits will not be switched at the same time.

Gate circuits  $34_1$ – $34_7$  are synchronized with the switching of the logic levels of the output signals of delay circuits  $54_1$ – $54_7$ , to switch the charging/discharging state of capacitors  $35_1$ – $35_7$  of the various charge-pump circuits. Consequently, similarly to booster circuits 31 and 41 shown in FIGS. 6 and 8 that use ring oscillators, in this case, the charging/discharging states of two or more capacitors will also not be switched at the same time. Therefore, a large flow of current can be avoided at the time that the charging/discharging state is switched.

Said booster circuits 1, 31, 41, and 51 are all composed of seven charge-pump circuit stages. However, the present invention is not limited to this number of charge-pump circuit stages.

Also, in booster circuit 51 shown in FIG. 9, the configuration of timing control circuit 58 is not limited to that

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shown in FIG. 9. It is also possible to output the control signal to each charge-pump circuit after it is delayed by a different period of time for each charge-pump circuit.

The power consumption and noise of a booster circuit using charge-pump circuits can be reduced.

What is claimed is:

1. A booster circuit comprising N rectifying elements that are electrically connected in series between a voltage input terminal and a voltage output terminal with the terminal on an anode side taken as the voltage input terminal side,

N capacitors, each of which has one terminal electrically connected to the terminal on the cathode side of one of the rectifying elements, and

a first signal supply circuit which supplies a first control signal to the capacitors of the odd-numbered stages and a second signal supply circuit which supplies a second control signal whose phase is opposite to that of the first control signal to the capacitors of the even-numbered stages; wherein a first time delay is applied sequentially to the first control signal supplied to the other terminal of each capacitor of the odd-numbered stages, and a second time delay is applied sequentially to the second control signal supplied to the other terminal of each capacitor of the even-numbered stages, wherein the first control signal is delayed by a time interval  $\Delta t$  before being applied to the first stage, and delayed sequentially by a time interval  $2\Delta t$  between each odd-numbered stage, the second control signal is delayed by a time interval of  $2\Delta t$  before being applied to the second stage and by a time interval of  $2\Delta t$  between each even-numbered stage.

2. The booster circuit described in claim 1 further comprising a diode for preventing reverse current, which is electrically connected between the terminal on the cathode side of the rectifying element of the Nth stage and the voltage output terminal, and an output capacitor which is connected between the voltage output terminal and a reference potential where the rectifying elements are made of diodes, and an inverter is coupled between the first and second control signals supplied to the odd-numbered and even-numbered stages, respectively and the other terminal of each respective capacitor.

\* \* \* \* \*



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(54) **LOW POWER CHARGE PUMP CIRCUIT**

(75) **Inventors:** **Osama Khouri, Milan (IT); Andrea Plerin, Graffignana (IT); Dario Soltész, Gioia Del Colle (IT); Guido Torelli, Sant'Alessio con Vialone (IT)**

(73) **Assignee:** **STMicroelectronics S.r.l., Agrate Brianza (IT)**

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(52) **U.S. Cl.** **327/536; 363/60; 365/227**

(58) **Field of Search** **327/535, 536; 363/59, 60; 365/189.09, 227**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,301,097 A 4/1994 McDaniel ..... 363/60

5,969,565 A \* 10/1999 Naganawa ..... 327/536  
6,278,317 B1 \* 8/2001 Hsu et al. .... 327/536  
6,486,728 B2 \* 11/2002 Cleveland ..... 327/536  
2002/0175745 A1 \* 11/2002 Kim ..... 327/536  
2003/0058029 A1 \* 3/2003 Matsui ..... 327/536

**FOREIGN PATENT DOCUMENTS**

EP 0 716 368 A1 6/1996  
EP 1 111 763 A2 6/2001

\* cited by examiner

*Primary Examiner*—Timothy P. Callahan

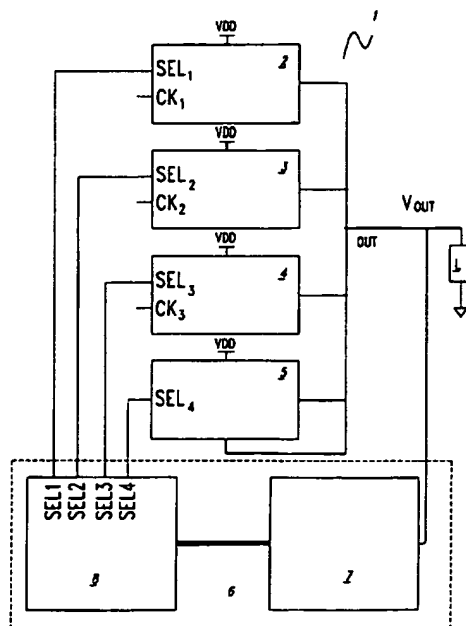
*Assistant Examiner*—Terry L. Englund

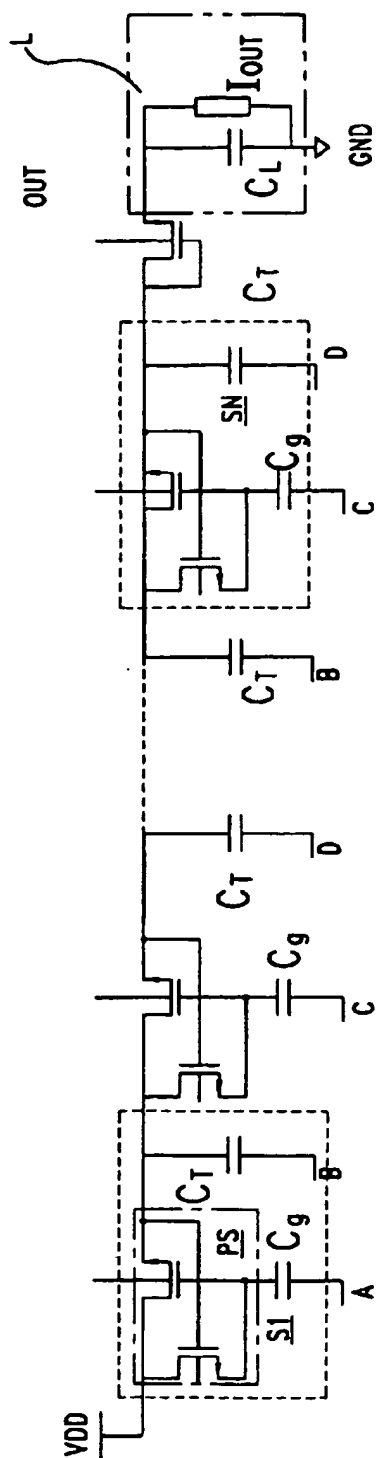
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; Dennis M. de Guzman; Seed IP Law Group PLLC

(57) **ABSTRACT**

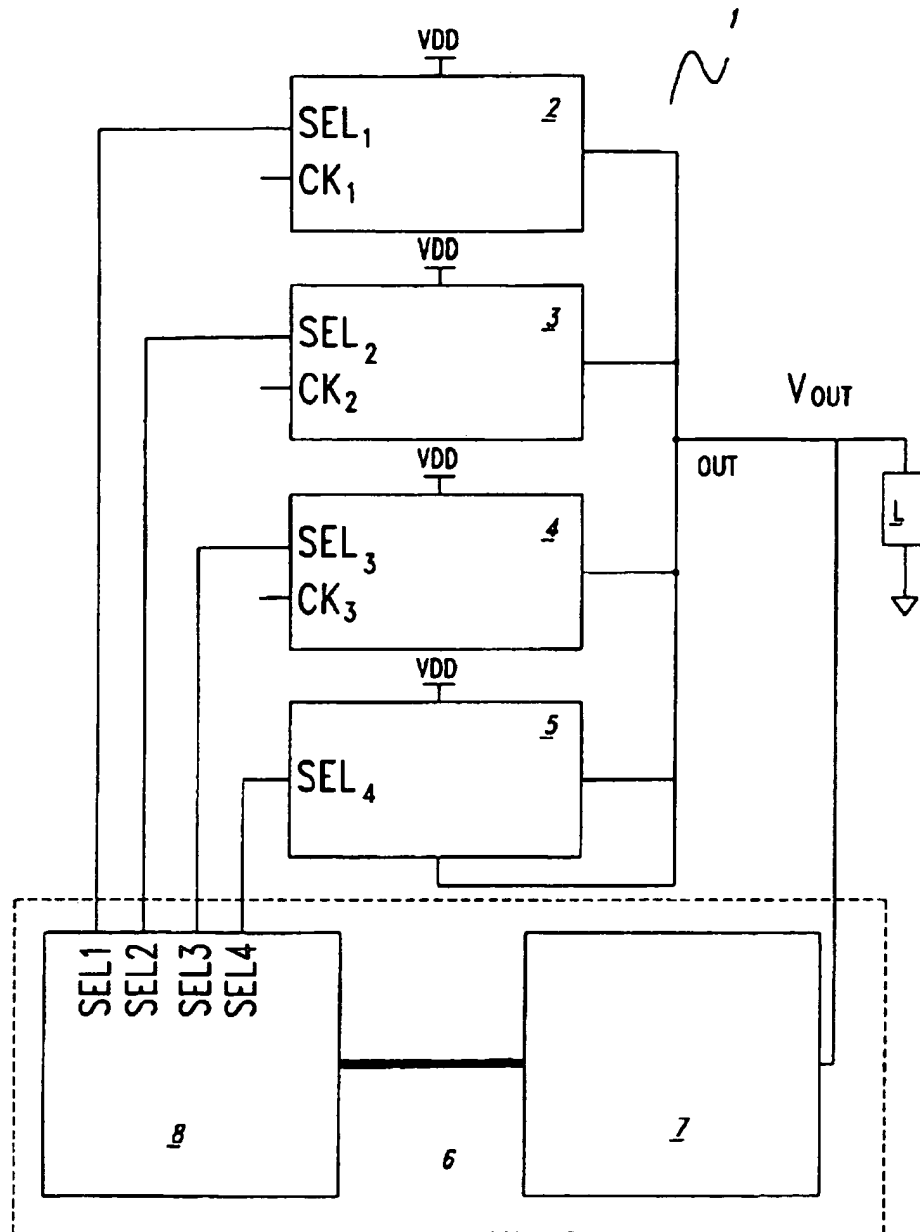
A charge pump circuit, connected between a first voltage reference and an output terminal, comprises at least two parallel-coupled stages having an elementary charge pump circuit connected between said first voltage reference and said output terminal, and adjustment circuitry connected between said output terminal and respective control terminals of said at least two stages. This adjustment circuitry is arranged to select for actuation an appropriate combination of these elementary stages according to the current absorbed from a load connected to the output terminal.

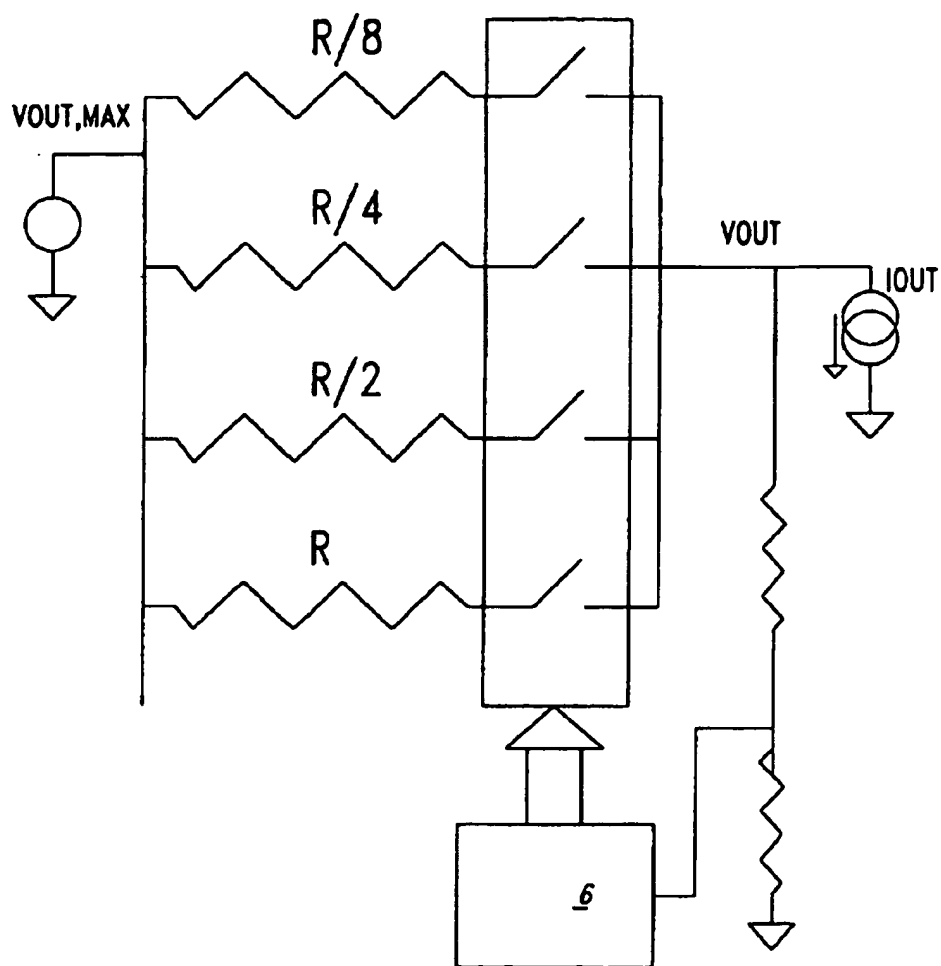
**21 Claims, 7 Drawing Sheets**





**FIG. 1**  
**(Prior Art)**

*FIG. 2*

*FIG. 3*

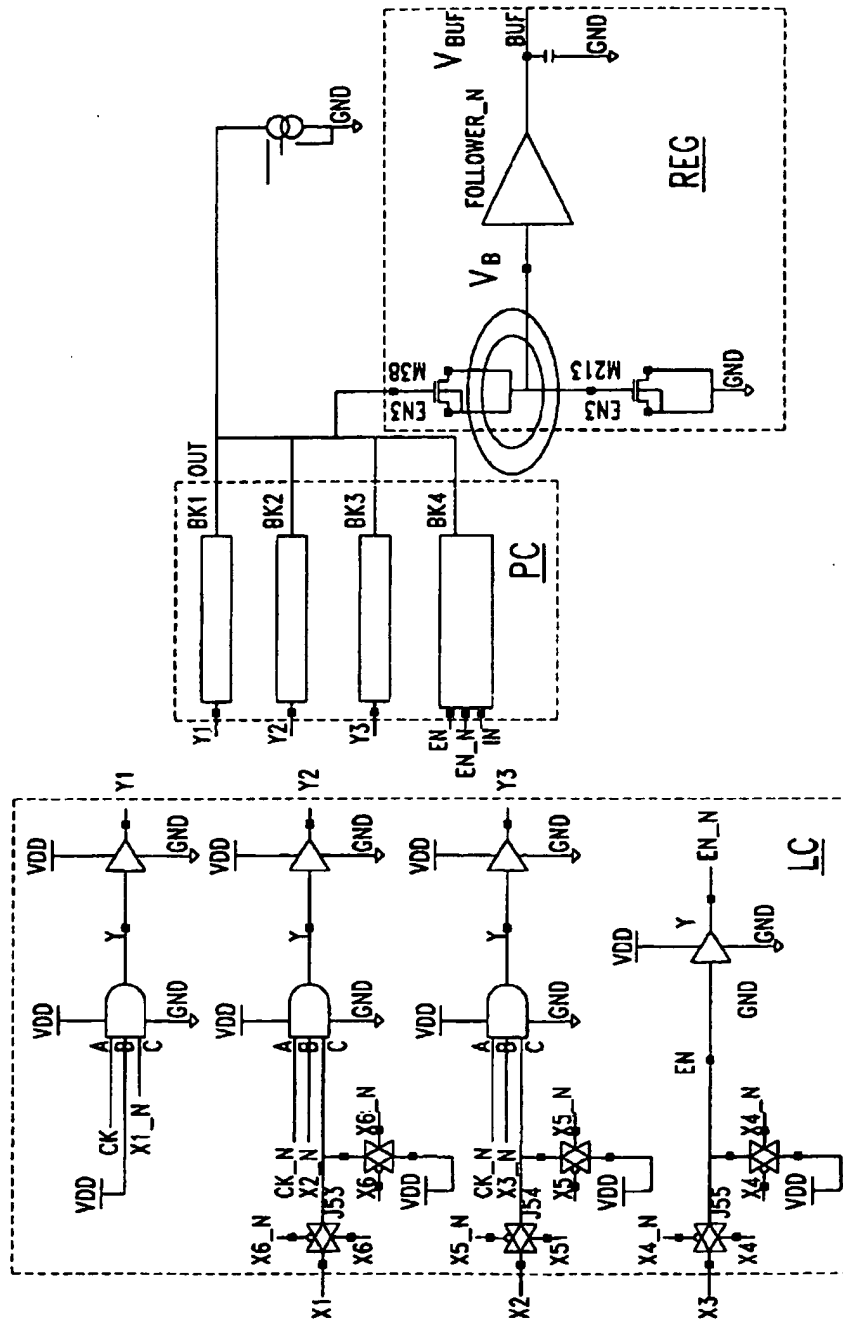
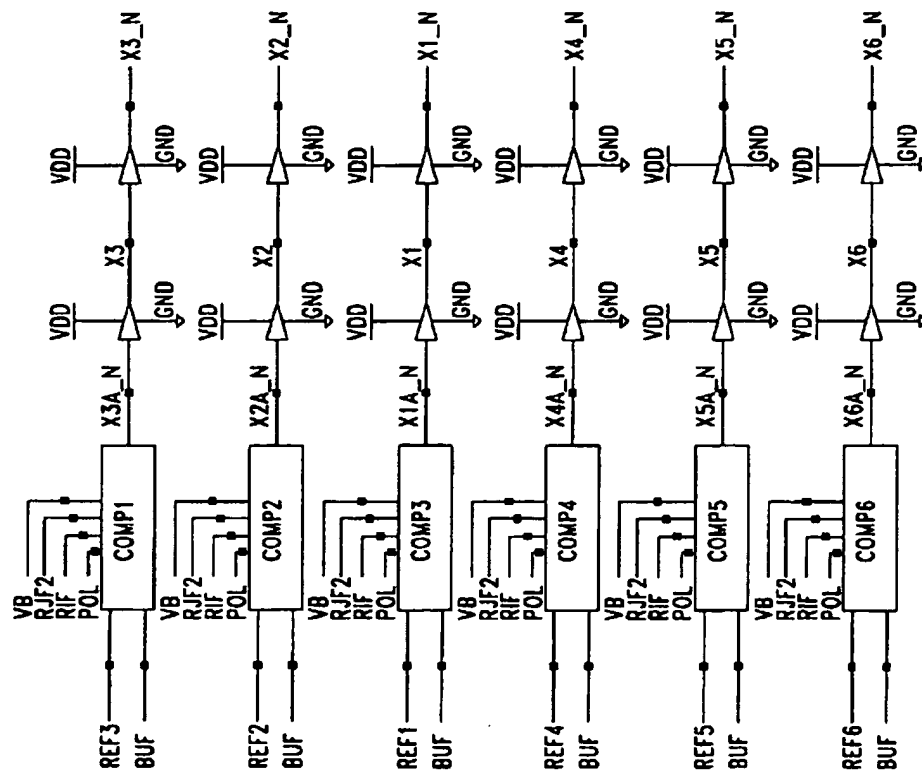
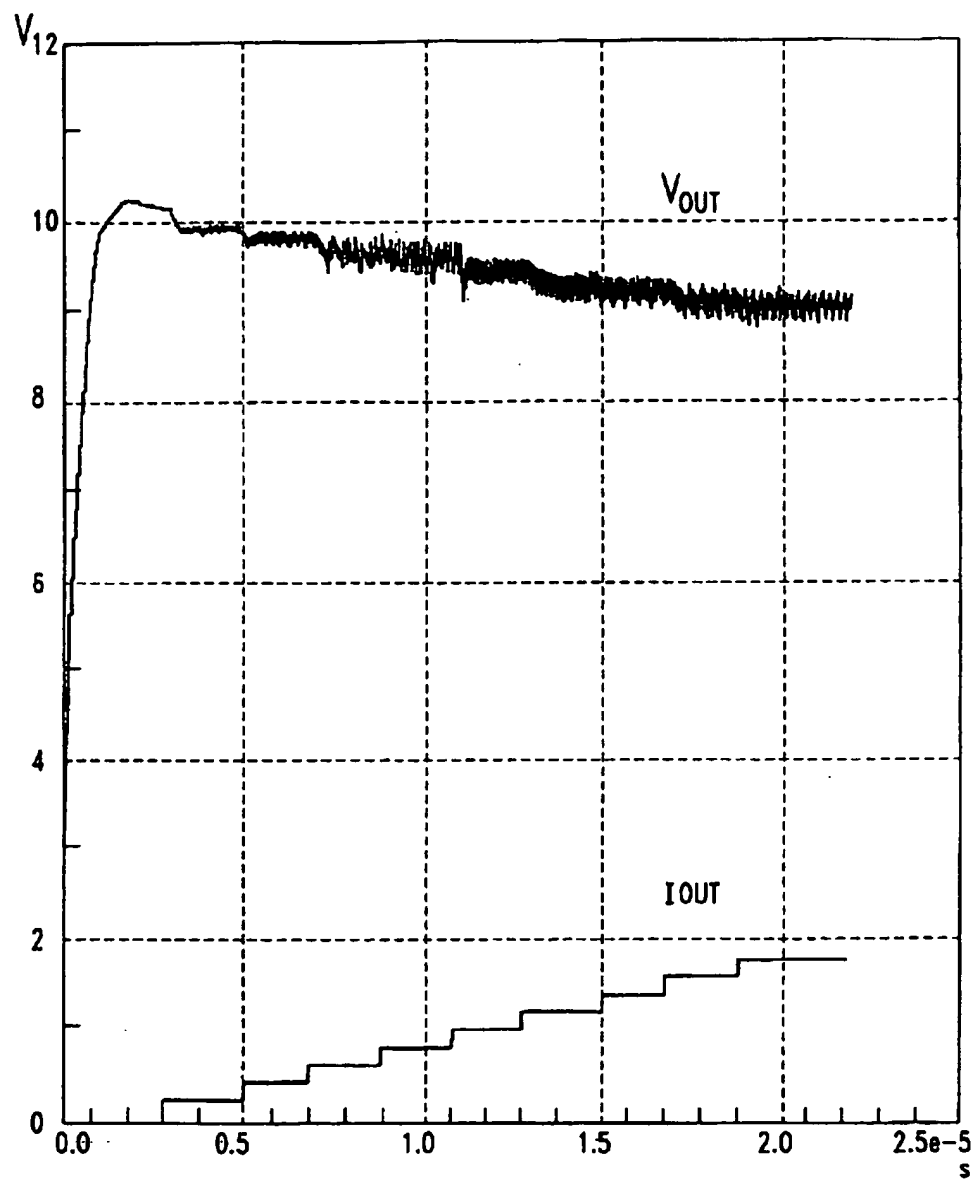


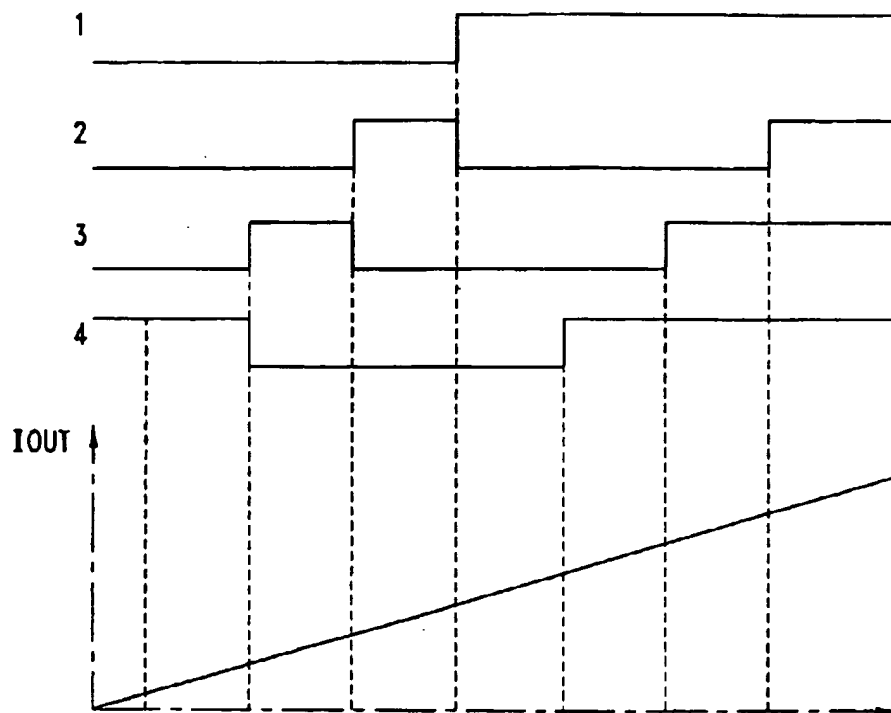
FIG. 4



**FIG. 5**



*FIG. 6*

*FIG. 7*

## LOW POWER CHARGE PUMP CIRCUIT

## FIELD OF THE INVENTION

The present invention relates to a low power consumption charge pump circuit.

Specifically, the invention relates to a charge pump circuit that is connected between a first voltage reference and an output terminal.

The invention further relates to a method of generating a substantially constant voltage signal whose value exceeds a supply voltage reference.

The invention relates, particularly but not exclusively, to a charge pump circuit for low power applications, this description covering that field for convenience of illustration only.

## DESCRIPTION OF THE RELATED ART

As is well known, extensive use is made nowadays of nonvolatile digital data memory devices. Consumer products, such as still and TV cameras, "walkmen," cellular phones, and electronic notebooks, require this kind of memory devices for storing information in a compact support of large capacity.

A shortcoming of nonvolatile memory devices is the high power consumption that associates with their operation. This is obviously of major consequence to portable products like those listed above, which have to be battery powered.

Most of the power expended to operate such memories goes to charge pump circuits, which are arranged to raise the voltage value above the supply (usually, battery) level for further supplying a part of the circuitry integrated in the memory device. This is because the voltages needed to perform such basic operations as program and erase operations in nonvolatile memory devices, and in low voltage supply circuits read operations as well, are higher than the supply voltage.

Thus, providing charge pump circuits that would absorb as little as possible on the power supply for their operation is quite important, and the present trend toward ever lower supply voltages for integrated circuits can only emphasize this importance.

A standard charge pump circuit for nonvolatile memory chips is shown in FIG. 1, that illustrates a known charge pump of the Dickson type.

This charge pump comprises a plurality of stages S1-SN, which are connected in cascade between an input node that is connected to a voltage supply line VDD, and an output node. The output node is connected to a load L represented by a capacitor having a capacitance  $C_L$  and being connected in parallel with a current-absorbing element  $I_{OUT}$  connected between said output node and a reference GND. Each stage comprises a charge transfer element PS comprising of a pass transistor that has its gate terminal driven by appropriate drive signals, and a transfer capacitor of capacitance  $C_T$  having one plate connected to the transfer element PS and the other plate connected to a drive signal A, B, C, D.

Two equations are related with the circuit of FIG. 1 which link the circuit output voltage  $V_{OUT}$  and the current  $I_{IN}$  absorbed from the supply reference to variation of the current  $I_{OUT}$  that the circuit is to supply to the load:

$$V_{OUT} = (n+1)V_{DD} - n \frac{I_{OUT}}{fC_T} = V_{OUT,MAX} - R_{OUT}I_{OUT} \quad (1)$$

$$I_{IN} = (n+1)I_{OUT} + n f C_{PAR} V_{DD} \quad (2)$$

where:

$n$  is the number of stages used in the charge pump;

$I_{OUT}$  is the output current, i.e., the current absorbed from the load;

$V_{DD}$  is the supply voltage;

$C_T$  is the capacitance of the transfer capacitors;

$C_{PAR}$  is the capacitance of a parasitic capacitor of the bottom plate of each transfer capacitor; and

$f$  is the frequency of the clock signal (i.e., the switching frequency of the drive signals A, B, C, D to the charge pump).

The single parasitic effect considered in equation (2) is that due to the parasitic capacitance that exists between the bottom plates of the transfer capacitors of capacitance  $C_T$  and the ground reference GND. This, of course, is inclusive of the parasitic capacitance of the lines connected to this plate, which capacitance is usually much lower than the parasitic capacitance of the plate itself. In particular, the parasitic capacitances associated with the internal nodes of the charge pump, such as the capacitance of the top plates of the capacitors and the parasitic capacitances associated with the capacitors  $C_g$  and the other charging elements PS, are neglected in Equations (1) and (2).

In particular, it is evinced from Equation (1) that the loadless output voltage  $V_{OUT,MAX}$ , i.e., the current absorbed from the load  $L$  is zero, of the charge pump is  $V_{OUT,MAX} = (n+1)V_{DD}$ , and the loadless output resistance  $R_{OUT}$  is  $n/fC_T$ .

Equation (1) shows that, if a current  $I_{OUT}$  is to be delivered with the output voltage  $V_{OUT}$  held at or above a predetermined value, a minimum of stages must be used. Also, to minimize the voltage drop due to the charge pump circuit delivering the current  $I_{OUT}$ , a high frequency and large transfer capacitors must be used.

However, the last-mentioned requirement collides with the provisions of Equation (2) because, as the capacitance  $C_T$  of the transfer capacitors increases, the value  $C_{PAR}$  of the parasitic capacitances also increases, and with it the current  $I_{IN}$  absorbed from the power supply. The same consideration applies to the frequency  $f$ .

Accordingly, the charge pump circuits are at once required to deliver the necessary current to the load, to hold the output voltage at an adequate level, and to absorb the lowest possible amount of current  $I_{IN}$  from the power supply.

This is particularly true when the charge pump is used for driving a load whose absorption of the current  $I_{OUT}$  varies conspicuously with time. To provide a desired value of the output voltage  $V_{OUT}$  at a large value of the current  $I_{OUT}$ , the product  $fC_T$  has to be sufficiently high. With such a pump, when the current  $I_{OUT}$  absorbed from the load is small, the output voltage  $V_{OUT}$  approaches its maximum  $V_{OUT,MAX}$  (corresponding to the loadless voltage value). The drop due to the term  $I_{OUT}/fC_T$  is thus minimized.

Under these conditions, the voltage value  $V_{OUT}$  is high, although a lower output voltage value  $V_{OUT}$  would be sufficient to ensure proper performance of the whole circuit. Thus, it makes no sense to keep the charge pump at the top of its capacity under such conditions, while it could be operated at lower levels and reduced power absorbed from the power supply, i.e., at a lower value of  $fC_T$ .

A first prior approach to reach this requirement provides for on/off control of the output voltage  $V_{OUT}$ , i.e., the charge

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pump turns off as soon as the output voltage reaches a higher preset threshold value, and turns on again as the output voltage falls below this value.

Despite its simple design, this approach has a drawback in that, at each working cycle of the drive signals, a predetermined charge amount  $\Delta Q$  is output. As said before, if the charge pump circuit is sized to provide a desired output voltage level  $V_{OUT}$  when there is a high output current  $I_{OUT}$ , the charge amount  $\Delta Q$  will be adequately large, because the charge amount  $\Delta Q$  equals the amount of charge absorbed by the load  $L$  during one cycle of the drive signals A-D. Thus, as the control loop by which the charge pump is turned on/off operates the charge pump, the output voltage  $V_{OUT}$  will experience a manifest increase. This increase is then cancelled, in time interval, by the absorption from the load  $L$ . This produces substantial rippling of the output voltage  $V_{OUT}$ .

The ripple is the more manifest when some delay occurs in the control loop. In this case, the charge pump may stay 'on' for some time even if the output voltage  $V_{OUT}$  exceeds the preset threshold level, so that the ripple amplitude is increased.

A prior embodiment based on the on/off control technique provides for the capacitance  $C_T$  of the transfer capacitors to vary with the current  $I_{OUT}$  absorbed from the load. This requires the availability of a DPCA (Digital Programmable Capacitor Array), i.e., sets of cascaded capacitors adapted for independent activation. However, where high operating voltages are involved, high-voltage capacitors must be used, i.e., capacitors that can withstand large electric fields between their plates. By reason of their construction, such capacitors exhibit large parasitic capacitances between their bottom plates and ground. With the bottom plates of the capacitors connected to the drive signals, this leads to a large dissipation of power according to Equation (2). Also, the connection of the bottom plate to the internal node of the charge pump causes the capacitive partition ratio of the individual stages to be exceedingly low, thus draining a significant portion of the charge on the internal nodes of the charge pump to ground and reducing the maximum attainable value  $V_{OUT,MAX}$  of the output voltage.

Furthermore, high-voltage switches must be provided for selecting the DPCA capacitors, these switches taking up a large amount of silicon area and having large parasitic capacitances.

A second prior approach to the problem of controlling power consumption of the charge pump provides for the output voltage to be controlled by adjusting the frequency of the clock signal.

However, not even this approach is devoid of shortcomings, although it does provide a smoother output voltage. Since the capacitance  $C_T$  of the transfer capacitor must be large when the current absorption from the load  $L$  is small, the output voltage  $V_{OUT}$  is once again rippled (due to that the charge amount  $\Delta Q$  may be too large during a single cycle of the drive signals).

The underlying technical problem of this invention is to provide a charge pump circuit with appropriate structural and functional features to lower power consumption both in operation and standby, i.e., when no current is absorbed by the charge pump output (standby), thereby overcoming the drawbacks that beset prior art circuits.

#### BRIEF SUMMARY OF THE INVENTION

The resolute idea which is at the basis of this invention is that of providing a charge pump that comprises a parallel of at least two elementary charge pump circuits, wherein the

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charge pump is able to sense the current  $I_{OUT}$  absorbed from the load connected thereto, and accordingly select the best combination of elementary charge pump circuits for each absorbed current  $I_{OUT}$ .

Based on this principle, the technical problem is solved by a circuit as indicated, and as defined in claim 1.

The problem is further solved by a method as previously indicated, and as defined in claim 10.

The features and advantages of the device according to the invention will be apparent from the following detailed description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

In the drawings:

FIG. 1 shows a charge pump circuit according to the prior art;

FIG. 2 shows a block diagram of the charge pump circuit according to an embodiment of the invention;

FIG. 3 shows a schematic equivalent circuit diagram of the charge pump circuit according to an embodiment of the invention;

FIGS. 4 and 5 show a possible embodiment of the charge pump circuit shown in FIG. 2;

FIG. 6 shows a time graph of the output voltage from the circuit of this invention, plotted against the current absorbed from a load connected to the circuit; and

FIG. 7 shows a qualitative time graph of the activating signals to four stages of the charge pump circuit embodiment of this invention, plotted against the current absorbed from the load connected to the circuit.

#### DETAILED DESCRIPTION OF THE INVENTION

Embodiments of a low power charge pump circuit are described herein. In the following description, numerous specific details are given to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

With reference to the drawings, in particular to the example of FIG. 2, a charge pump circuit realized according to an embodiment of this invention is generally shown at 1 in schematic form. The charge pump circuit can be used, i.e., in integrated memory device.

The circuit 1 of this invention comprises a plurality  $n$  of stages connected together in parallel between a supply voltage reference  $V_{DD}$  and an output terminal OUT.

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A control circuit 6 is connected between the output terminal OUT of the circuit 1 and the input of each stage, to provide respective select/enable signals SEL1, SEL2, . . . , SEL4 to the stages. According to the invention, the control circuit 6 is adapted to select for activation a suitable combination of these elementary stages according to a current absorbed by a load connected to the output terminal OUT.

In one embodiment, herein described and illustrated by way of non-limitative example, the circuit 1 comprises four stages 2, 3, 4, 5, each incorporating a conventional elementary charge pump circuit. However, nothing prevents providing only two such stages.

Each stage of the first three 2, 3, 4 has a terminal to which synchronization (clock) signals CK1, . . . , CK3 are connected. Advantageously, these clock signals CK1, . . . , CK3 are connected to a common signal. In particular, according to an embodiment of the invention, these stages 2, 3, 4 are driven by clock signals CK1, . . . , CK3 that have all the same frequency and are derived from one signal, referred to as the master clock signal, through a conventional enable/disable network. However, nothing prevents these clock signals CK1, . . . , CK3 from all being different.

According to an embodiment of the invention, the stages 2, 3, 4, 5 comprise charge pumps having the same loadless output voltage ( $V_{OUT,MAX}$ ) and different output resistances, as schematically illustrated by the equivalent circuit of FIG. 3.

In one embodiment of the circuit 1 according to the invention, the stages 2, 3, 4, 5 comprise each at least one conventional charge pump circuit of the pass transistor type, with each of these circuits including transfer capacitors of a different size from those of the other blocks.

In particular, the first stage 2 comprises a charge pump circuit having transfer capacitors of a capacitance CT, the second stage 3 a charge pump circuit having transfer capacitors of a capacitance CT/2, the third stage 4 a charge pump circuit having transfer capacitors of a capacitance CT/4, and the fourth stage 5 a charge pump circuit having transfer capacitors of a capacitance CT/8. The four stages 2, 3, 4, 5 deliver their charge to the single output terminal OUT, and may be operated in parallel.

Advantageously, the stage 5 comprises a pass-transistor elementary charge pump circuit, wherein the clock signal is provided by a voltage-controlled oscillator (VCO). In this stage 5, the control signals (and, hence, the frequency of the output signal) are dependent on the pump output voltage. However, nothing prevents the other stages 2, 3, 4 could also be provided with a voltage-controlled oscillator VCO, instead of being connected to the same clock signal, with the clock signal CK1, . . . , CK3 being fixed.

A possible embodiment of such stages is shown in FIG. 4 as a block PC that contains the four charge pump circuits of the stages 2, 3, 4, 5.

The control circuit 6 of FIG. 2 may comprise an analog-to-digital converter 7 and selection logic 8, for example.

In particular, the converter 7 will produce logic control signals for controlling the output voltage  $V_{OUT}$ , as this voltage varies at the output terminal OUT.

Referring to FIGS. 4 and 5, in a non-limitative example, the converter 7 comprises a first section REG and a second section COMP. The first section REG comprises a voltage divider arranged to reduce the output voltage  $V_{OUT}$  to a value  $V_B$  within a reference range, for instance between ground voltage GND and supply voltage  $V_{DD}$ . This voltage  $V_B$  is input to the second section COMP of FIG. 5 through

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a voltage repeater. The second section COMP comprises a plurality of comparators. These comparators are to compare the output voltage  $V_{BUF}$  from the voltage repeater with predetermined reference voltages  $V_{REF1}$ , . . . ,  $V_{REF6}$  and output an appropriate logic signal. In the embodiment of FIG. 5, these logic signals are designated X1, X2, X3, X4, X5, X6.

The selection logic 8 will select one or more of the charge pump circuits in the stages 2, 3, 4, 5 for activation, according to the logic signals that are generated by the converter 7. In a typical configuration, a pump would be activated by enabling its drive signals, and deactivated by disabling its drive signals, i.e., holding them at a fixed level. A possible embodiment of this activation logic is illustrated by block LC in FIG. 4.

As to the operation of this circuit 1, when the current  $I_{OUT}$  absorbed by a load on the output terminal OUT is small, only stage 5, i.e., the stage with lowest transfer capacitance is enabled. The dynamic power consumption of the circuit 1 is, therefore, very low. The output voltage  $V_{OUT}$  is held at a value preset by this stage 5.

Advantageously, when the clock signal to the stage 5 is provided by a VCO, with no absorption of output current  $I_{OUT}$ , the charge pump of the stage 5 is operated at the lowest available frequency and consumes lowest power.

With the circuit 1 loadless, the voltage at the output terminal OUT is the highest available from the circuit 1. When the current  $I_{OUT}$  absorbed from the load is other than zero, the stage 5, which is the only active one, senses a variation in the load that produces a decrease in the output voltage, and through the clock signal controlled by the VCO, raises its frequency to compensate for the current change.

In practice, this single charge pump of the stage 5 operates in the example illustrated on the charge pump adjustment principle using the drive signal frequency.

As the current  $I_{OUT}$  increases again, the control circuit enables one or more of the stages 2, 3, 4 according to the magnitude of the current  $I_{OUT}$ .

Of course, each module that is activated involves some loss, so that the smaller the number of modules that are turned on, the less the power used up in the circuit 1.

As is evinced from Equation (1) when applied to each elementary charge pump stage, once  $n$ ,  $f$  and  $V_{DD}$  are set, for each value of the output current  $I_{OUT}$  there will be a transfer capacitance value  $C_T$  at which the output voltage  $V_{OUT}$  reached by the charge pump equals the voltage  $V_{REG}$  to which the output terminal OUT need to be raised. More precisely, when the current  $I_{OUT}$  is small, a small capacitance value  $C_T$  of the transfer capacitor will suffice (for the same  $f$ ), i.e., a small transfer capacitor will suffice having a small parasitic capacitance  $C_{PAR}$  associated therewith. Consequently, the current absorbed by the supply reference will be reduced.

According to one embodiment of the invention, only such stages as are necessary for the circuit 1 to perform correctly may be actuated.

In summary, according to an embodiment of the invention a plurality of stages may be connected in parallel, with each stage including at least one charge pump with transfer capacitors of different sizes. According to the current  $I_{OUT}$  being delivered to the load, the stage in the circuit 1 is activated whose charge pump has the most appropriate transfer capacitance. Also, when  $m$  is the number of stages employed in the circuit 1, by activating  $j$  (where  $j$  varies between 1 and  $m$ ) stages simultaneously instead of one at a

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time, the output voltage can be a finely adjusted value. In other words, the control circuit 6 operates activating, according to the value of the current  $I_{OUT}$ , the connection of a charge pump combination to the output.

The activation of one or more charge pumps implies the overall output resistance of the circuit 1 varying as shown in FIG. 3. Thus, by programming the elementary charge pumps in the stages 2, 3, 4 and, hence, the overall output resistance, the number of charge pumps kept working at any one time, and the dynamic power dissipated through the whole circuit; can be minimized.

In the example shown in FIGS. 4 and 5, there are only seven elementary charge pump combinations possible, requiring six comparators in the analog/digital converter 7.

FIG. 7 illustrates a possible actuation sequence for the four stages 2, 3, 4, 5 of the circuit 1 in the embodiment of FIGS. 4 and 5, against the current absorbed from the load connected to the circuit 1 of this invention.

Nothing prevents any of the combinations of elementary charge pumps possible in the stages 2, 3, 4, 5 can be activated. For example, to best utilize the binary weighing strategy adopted for the four stages with charge pumps, there may be provided no more than fifteen comparators in the analog-to-digital converter 7.

FIG. 6 is a simulation graph of the circuit output voltage  $V_{OUT}$  against the current  $I_{OUT}$  absorbed from the load. In the simulation, the load was an ideal voltage-driven current generator. As can be seen, in going from an output current  $I_{OUT}$  equal 0 to an output current  $I_{OUT}$  equal 1.8 mA; the output voltage  $V_{OUT}$  of the circuit 1 varies by the range of 1 Volt.

In particular, when the current  $I_{OUT}$  equals 0 mA, only stage 5 is enabled in the circuit 1 of this invention, with the loadless voltage of the circuit 1 at the maximum loadless voltage value  $V_{OUT,MAX}$ . As the current  $I_{OUT}$  begins to rise, i.e., the current demand from the load increases, one or more of the stages 2, 3, 4 are actuated in the circuit 1 to keep the output voltage  $V_{OUT}$  substantially constant. A small voltage drop can be observed in the output voltage  $V_{OUT}$  where the current  $I_{OUT}$  rises.

To summarize, the device of one embodiment of this invention affords:

a large reduction in the current absorbed from the system under a condition of a small or no load current being delivered, meaning less power used up by the power supply; quick response to manifest variations of considerable magnitude in the current absorbed from the load, since in this invention, one or more charge pumps are always kept operating to maintain the charge on the internal nodes of the circuit;

a smaller number of charge pump circuit switchings, making for improved efficiency of the circuit;

freedom to choose from different types of charge pumps, e.g., Dickson-type charge pumps, for use in the system.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are pos-

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sible within the scope of the invention and can be made without deviating from the spirit and scope of the invention.

These and other modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

What is claimed is:

1. A charge pump circuit connected between a first voltage reference and an output terminal, the charge pump circuit comprising:

at least two stages, each stage including an elementary charge pump circuit and being connected between said first voltage reference and said output terminal, each stage further including a control terminal to respectively select each stage; and

adjustment circuitry connected between said output terminal and respective control terminals of said at least two stages, including a converter circuit to generate logic signals based on a current at the output terminal, wherein the elementary charge pump circuit of each stage has transfer capacitors with different capacitances from the other stages.

2. A charge pump circuit according to claim 1 wherein one of said at least two stages is activated or deactivated during circuit operation by said adjustment circuitry as a value of the current on said output terminal varies under application of an external load.

3. A charge pump circuit according to claim 1 wherein a combination of said at least two stages is activated or deactivated during circuit operation by said adjustment circuitry as a value of the current absorbed by an external load varies on said output terminal.

4. A charge pump circuit according to claim 1 wherein the elementary charge pump circuit of each stage has transfer capacitors whose capacitance values are multiples of a smallest capacitance value found within any of the stages.

5. A charge pump circuit according to claim 1 wherein at least one of the stages comprises a charge pump with a variable clock signal.

6. A charge pump circuit according to claim 5 wherein said variable clock signal is generated by a voltage-controlled oscillator driven by said charge pump.

7. A charge pump circuit according to claim 5 wherein said charge pump with the variable clock signal comprises transfer capacitors of least capacitance compared to capacitances of transfer capacitors in another of said at least two stages.

8. A charge pump circuit according to claim 3 wherein said adjustment circuitry comprises selection logic and an analog-to-digital converter, connected in cascade together between said output terminal and said plurality of stages.

9. A method of generating a substantially constant voltage signal of a higher value than a supply voltage reference, the method comprising:

generating said voltage signal to an output terminal using a charge pump circuit, said charge pump circuit comprising a plurality of stages, with each stage including an elementary charge pump circuit, said stages being connected parallelly with each other;

determining a value of a current absorbed from a load connected to said output terminal;

generating logic signals based on the determined value of the absorbed current; and

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selectively actuating said stages in response to the generated logic signals and according to the determined value of said absorbed current, wherein only one of said stages is actuated when said determined current value is zero, and that a combination of said stages is actuated when said determined current value is other than zero.

10. A method of generating a voltage signal according to claim 9 wherein said stages are actuated selectively by adjustment circuitry connected between said output terminal and respective control terminals of said stages.

11. A method of generating a voltage signal according to claim 10 wherein each stage is driven by a respective clock signal from plural clock signals, each of the plural clock signals being different from the other clock signals by at least frequency.

12. A method of generating a substantially constant voltage signal of a higher value than a supply voltage reference, the method comprising:

generating said voltage signal to an output terminal using a charge pump circuit, said charge pump circuit comprising a plurality of stages, with each stage including an elementary charge pump circuit, said stages being connected parallelly with each other;

determining a value of a current absorbed from a load connected to said output terminal;

generating logic signals based on the determined value of the absorbed current; and

selectively actuating said stages in response to the generated logic signals and according to the determined value of said absorbed current, wherein the elementary charge pump circuit of each stage has transfer capacitors of different capacitances from the other stages.

13. An apparatus, comprising:

a plurality of stages coupled in parallel between a voltage reference and an output terminal, at least some of the stages including a charge pump circuit; and

a control circuit coupled between the output terminal and an input terminal of each stage to control activation of the at least some of the stages, the control circuit including selection logic to selectively activate or deactivate at least one of these stages according to a current that varies at the output terminal under different load conditions, the control circuit further including a converter to cooperate with the selection logic to generate logic signals based on the current at the output terminal, wherein the charge pump circuit of the at least some of the stages includes a capacitor having a different capacitance than capacitors of other stages.

14. An apparatus, comprising:

a plurality of stages coupled in parallel between a voltage reference and an output terminal, at least some of the stages including a charge pump circuit; and

a control circuit coupled between the output terminal and an input terminal of each stage to control activation of the at least some of the stages, the control circuit including selection logic to selectively activate or deactivate at least one of these stages according to a current that varies at the output terminal under different load conditions, the control circuit further including a converter to cooperate with the selection logic to generate logic signals based on the current at the output terminal, wherein at least one stage having the charge pump circuit includes a charge pump circuit with a variable clock signal generated by a voltage-controlled oscillator.

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15. A method, comprising:

determining a value of a current absorbed by a load at an output terminal;

generating logic signals to selectively activate at least one of parallel stages of a charge pump circuit based on the determined value of the current;

generating a substantially constant output voltage, of a higher value than a supply voltage, based on the selectively activated at least one stage;

providing the generated output voltage to the load; and driving the stages by a respective one of plural clock signals, each clock signal different from each other by at least frequency.

16. The method of claim 15, further comprising:

activating only one of the stages if the determined value of the current is substantially zero; and

activating a combination of the stages if the detected value of the current is other than substantially zero.

17. A charge pump circuit connected between a first voltage reference and an output terminal, the charge pump circuit comprising:

at least two stages, each stage including an elementary charge pump circuit and being connected between said first voltage reference and said output terminal, the elementary charge pump circuit of each stage having at least one transfer capacitor with a different capacitance from a capacitor of another stage; and

adjustment circuitry connected between said output terminal and respective control terminals of said at least two stages, wherein the at least one capacitor has a capacitance that is a multiple of a smallest capacitance value found within any of the stages.

18. A charge pump circuit connected between a first voltage reference and an output terminal, the charge pump circuit comprising:

at least two stages, each stage including an elementary charge pump circuit and being connected between said first voltage reference and said output terminal, at least one of the stages having a charge pump circuit with a variable clock signal and having transfer capacitors of least capacitance compared to capacitances of transfer capacitors in another stage; and

adjustment circuitry connected between said output terminal and respective control terminals of said at least two stages.

19. A method of generating a substantially constant voltage signal of a higher value than a supply voltage reference, the method comprising:

generating said voltage signal to an output terminal using a charge pump circuit, said charge pump circuit having a plurality of parallel stages, with each stage including an elementary charge pump circuit, the elementary charge pump circuit of each stage having transfer capacitors of different capacitances from other stages;

determining a value of a current absorbed from a load connected to said output terminal; and

selectively actuating said stages according to the determined value of said absorbed current.

20. A apparatus for generating a substantially constant voltage signal of a higher value than a supply voltage reference, the apparatus comprising:

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a means for generating said voltage signal to an output terminal using a charge pump circuit, said charge pump circuit having a plurality of parallel stages, with at least one stage including an elementary charge pump circuit, the elementary charge pump circuit of that stage having a transfer capacitor of different capacitance from capacitors of other stages; 5

a means for determining a value of a current absorbed from a load connected to said output terminal;

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a means for selectively actuating said stages according to the determined value of said absorbed current; and

a means for using a binary-weighting strategy to determine capacitances for each of the stages.

**21.** The apparatus of claim 20 wherein each of the stages includes an elementary charge pump circuit.

\* \* \* \* \*





US005392186A

**United States Patent** [19][11] **Patent Number:** **5,392,186****Alexander et al.**[45] **Date of Patent:** **Feb. 21, 1995**

[54] **PROVIDING VARIOUS ELECTRICAL PROTECTIONS TO A CMOS INTEGRATED CIRCUIT**

[75] **Inventors:** James W. Alexander, Hillsboro;  
Louis Johnson, Beaverton, both of  
Oreg.

[73] **Assignee:** Intel Corporation, Santa Clara, Calif.

[21] **Appl. No.:** 962,886

[22] **Filed:** Oct. 19, 1992

[51] **Int. Cl.<sup>6</sup>** ..... H02H 3/24

[52] **U.S. Cl.** ..... 361/92; 361/88;  
361/118

[58] **Field of Search** ..... 361/92, 91, 118, 88;  
320/8, 15; 307/272, 443, 451, 592

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

5,140,177 8/1992 Suda et al. .... 307/272  
5,204,610 4/1993 Pierson et al. .... 320/15

*Primary Examiner*—Marc S. Hoff

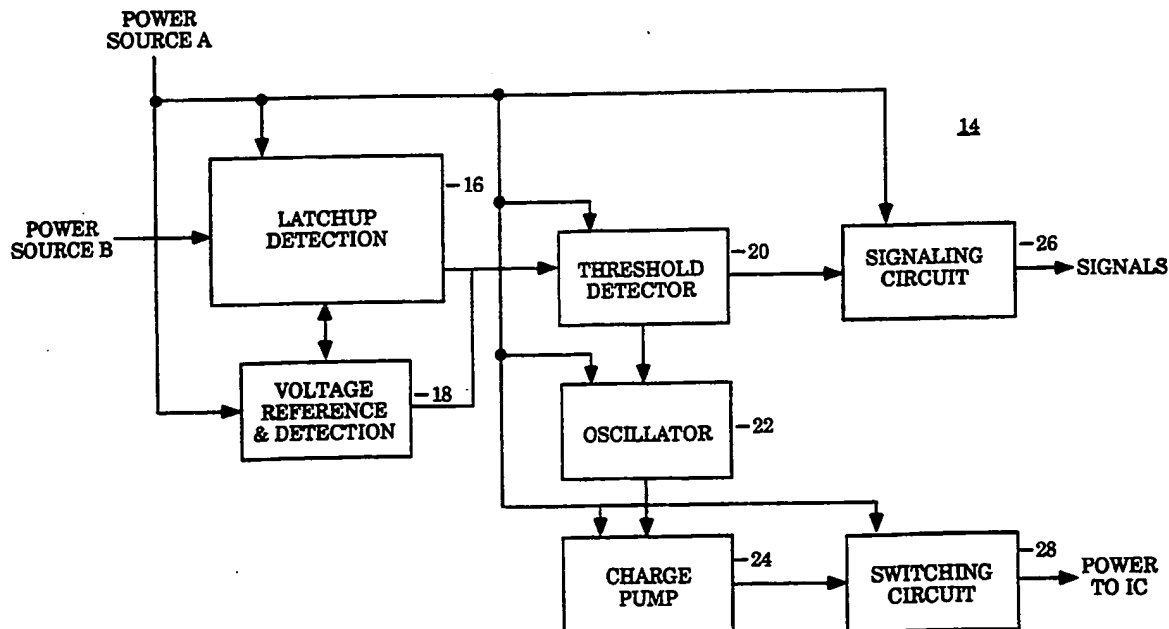
*Assistant Examiner*—S. Jackson

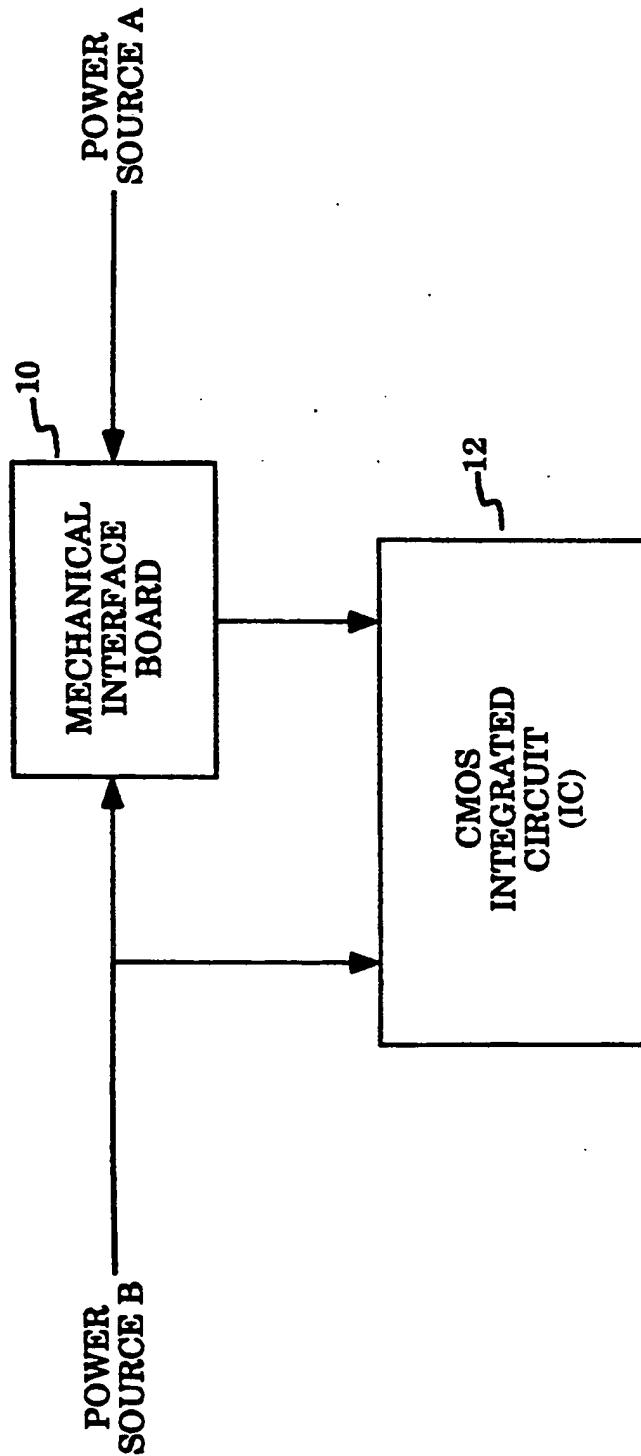
*Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman

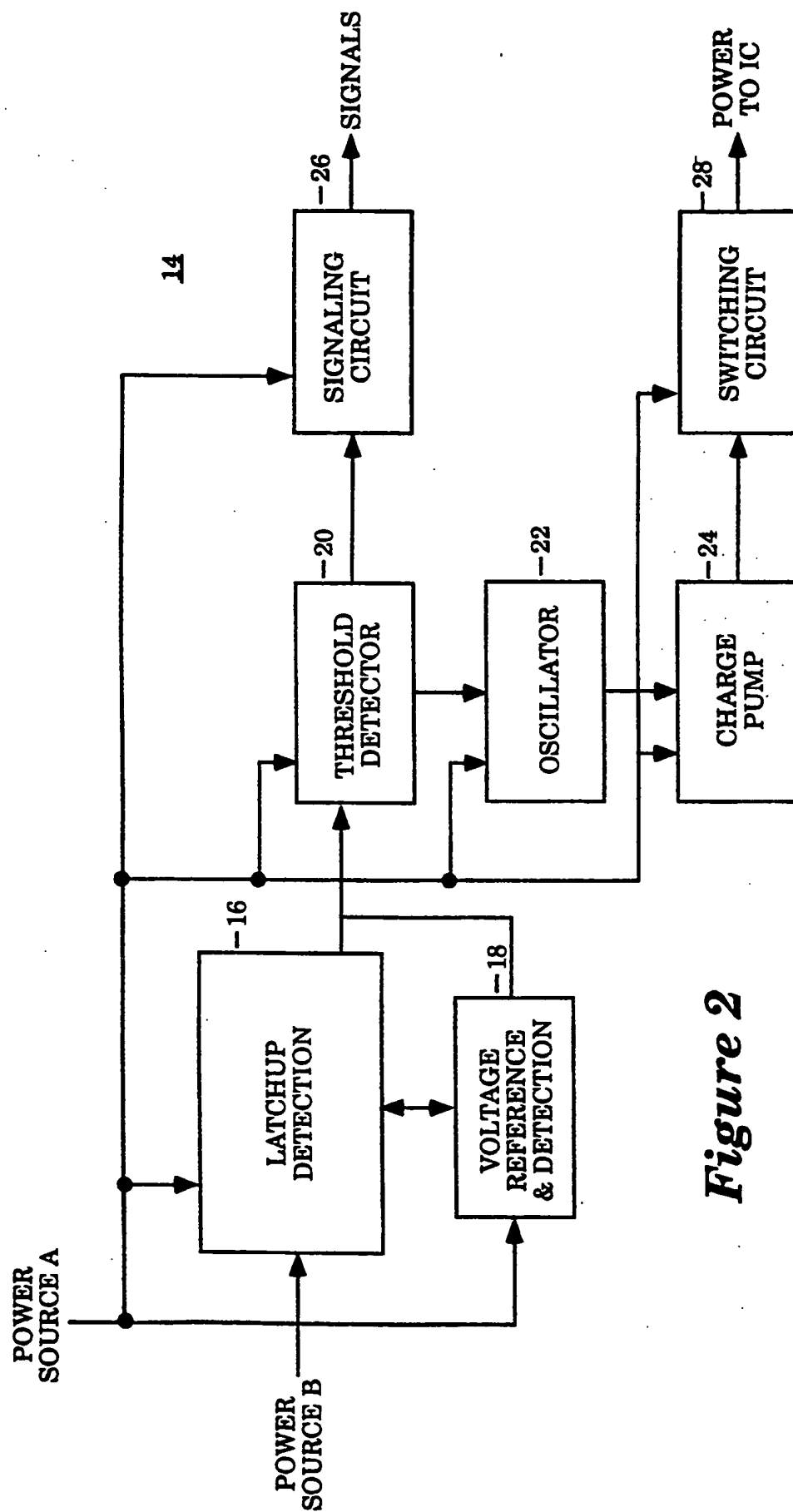
[57] **ABSTRACT**

The electrical protection circuit disclosed comprises a latchup detection circuit, a threshold detector, an oscillator, a charge pump, a switching circuit, a voltage reference and detection circuit, and a signaling circuit. The latchup detection circuit, the threshold detector, the oscillator, the charge pump, and the switching circuit cooperate to provide latchup protection for the CMOS integrated circuit. The switching circuit provides integrated reverse current protection to the CMOS integrated circuit. The voltage reference and detection circuit, the threshold detector, and the signaling circuit provides low voltage protection for the SRAM-based software-downloaded Field Programmable Gate Array of the CMOS integrated circuit.

**12 Claims, 9 Drawing Sheets**



*Figure 1*

*Figure 2*

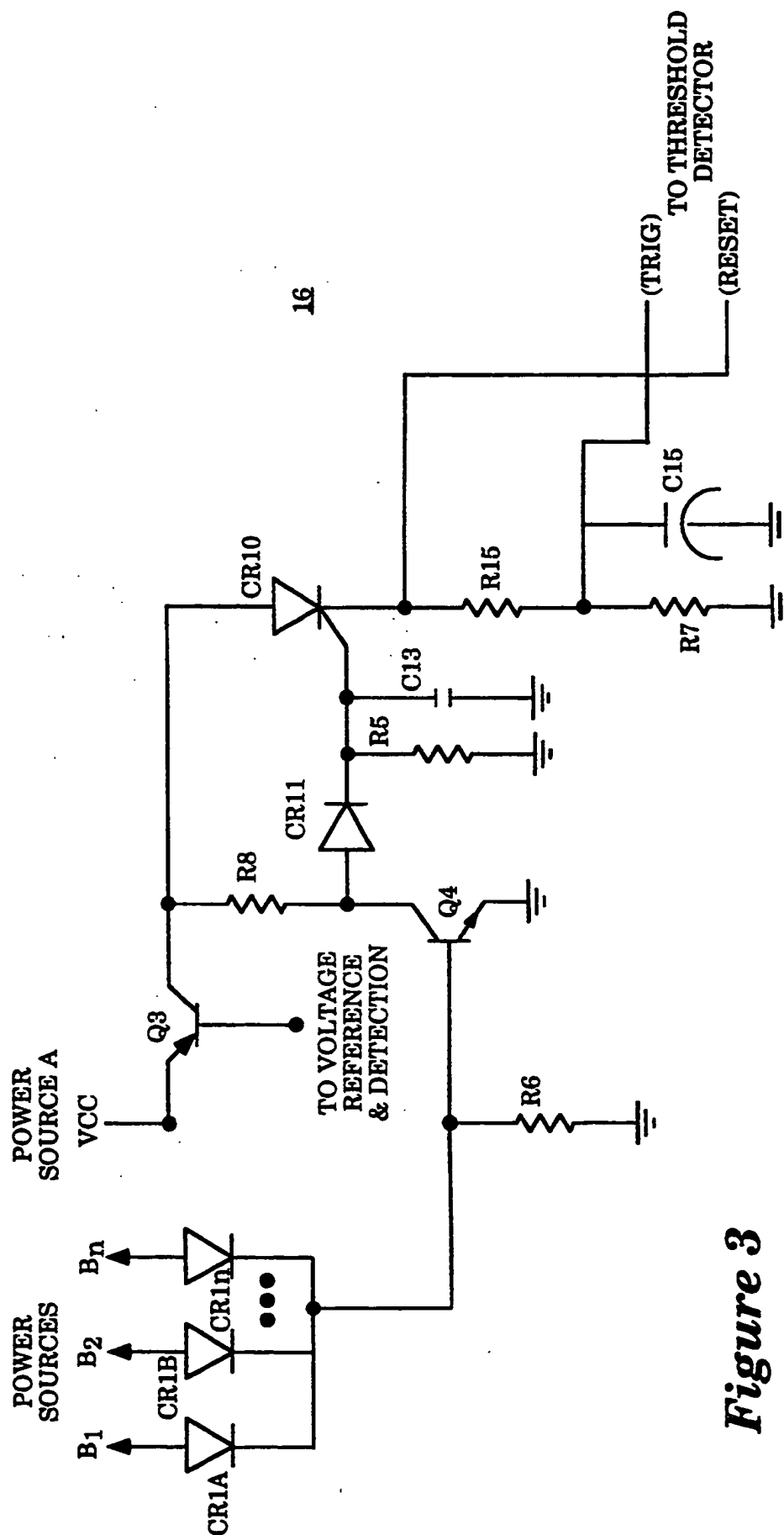


Figure 3

TRUTH TABLE

$\overline{R_1}$	R	S	OUT	DISCH
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	As Previously Established	
1	0	1	1	Z
1	1	0	0	0
1	1	1	1	Z

Z = Open Circuit

R1 =  $\emptyset$  When RESET =  $\emptyset$

R = 1 When THRES is higher than a minimum voltage

S = 1 When TRIG is lower than a minimum voltage

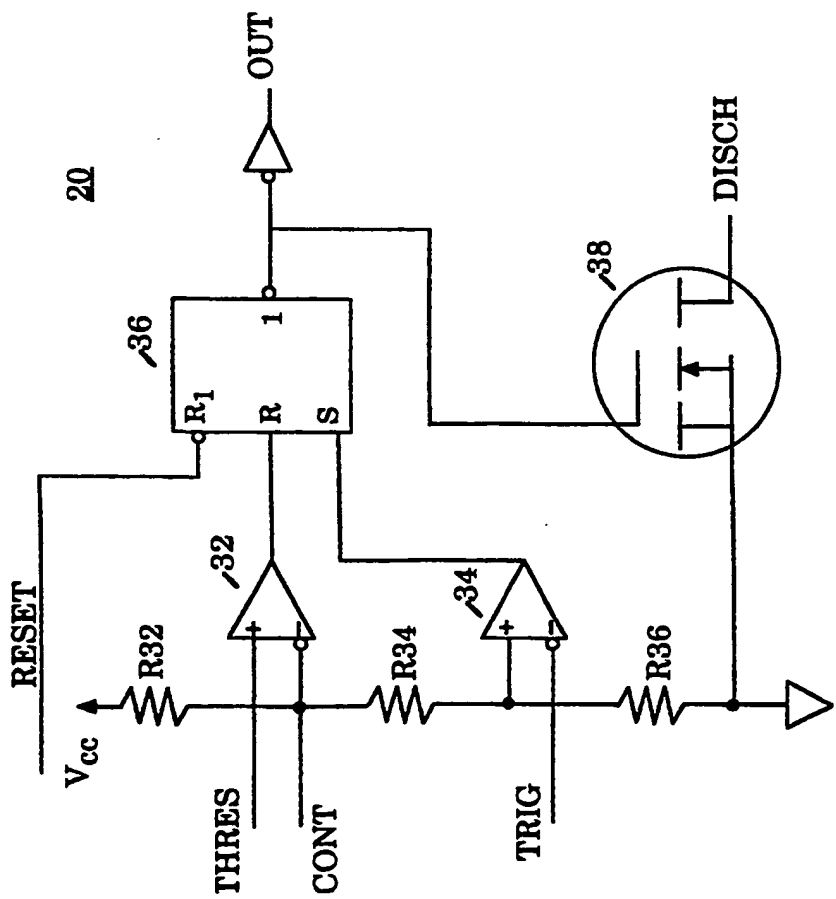


Figure 4

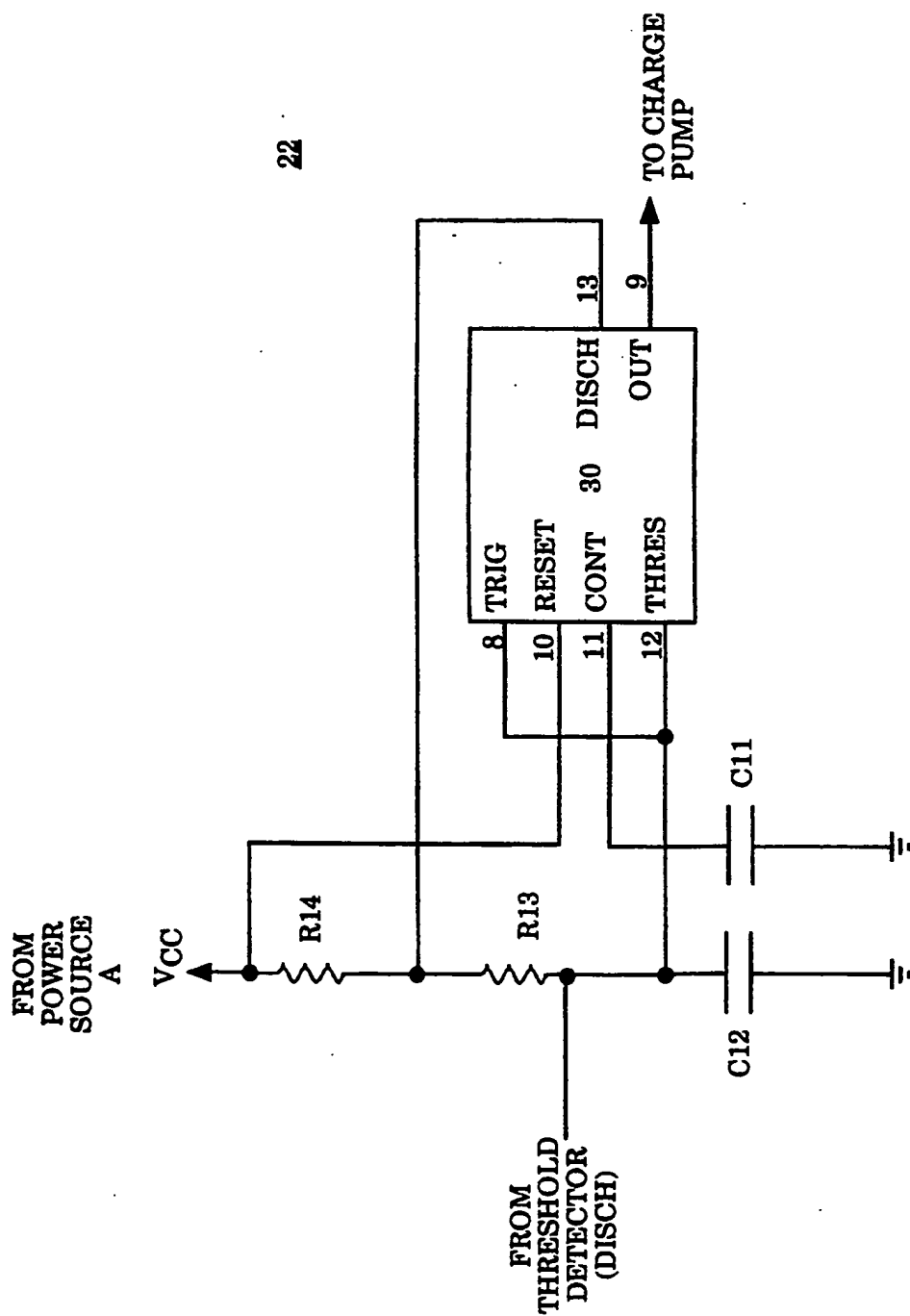


Figure 5

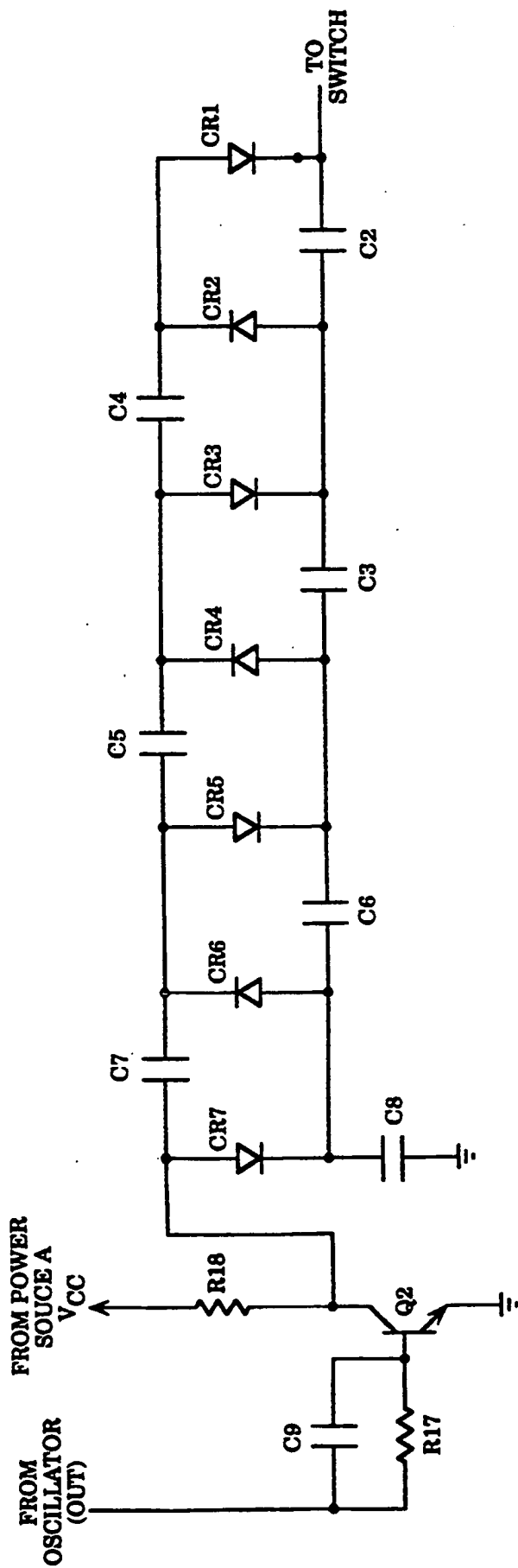


Figure 6

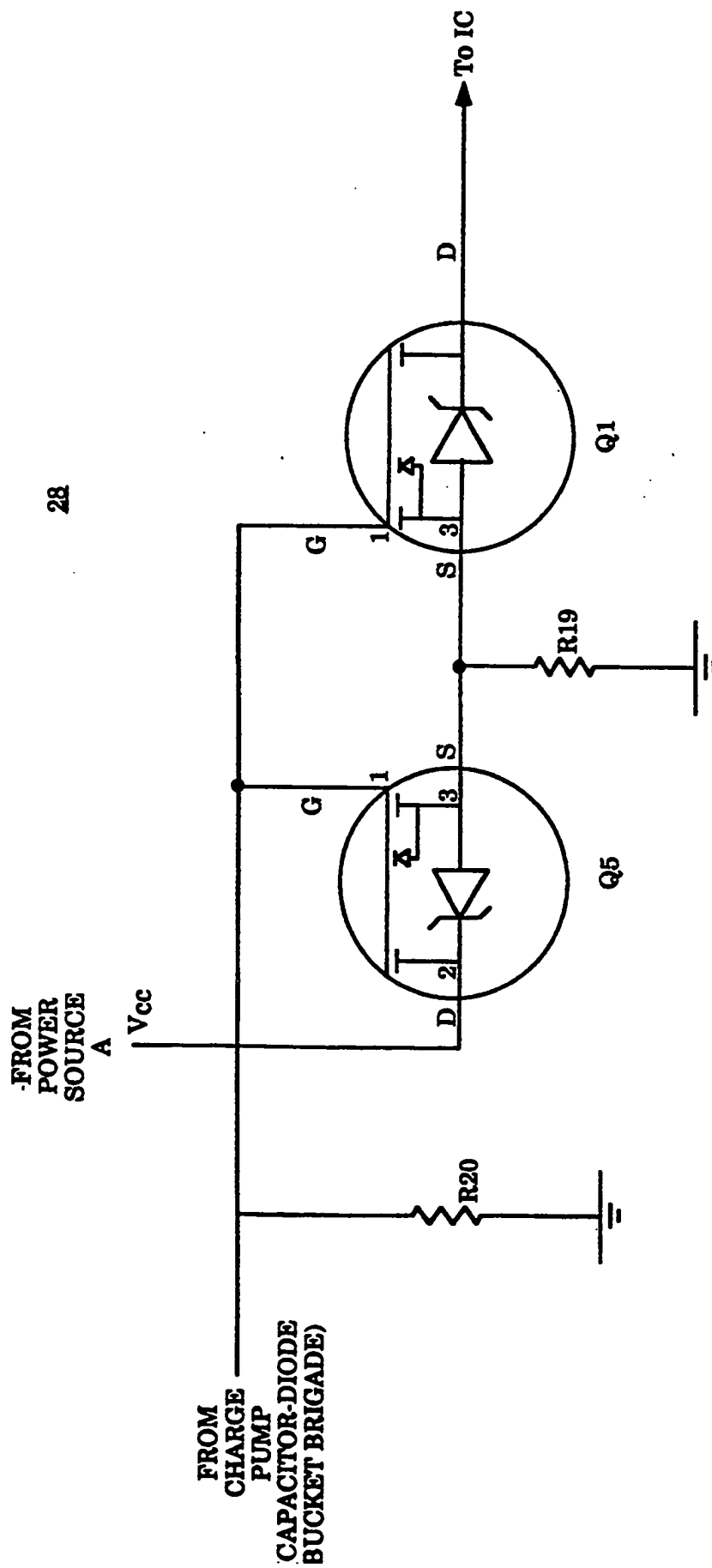


Figure 7



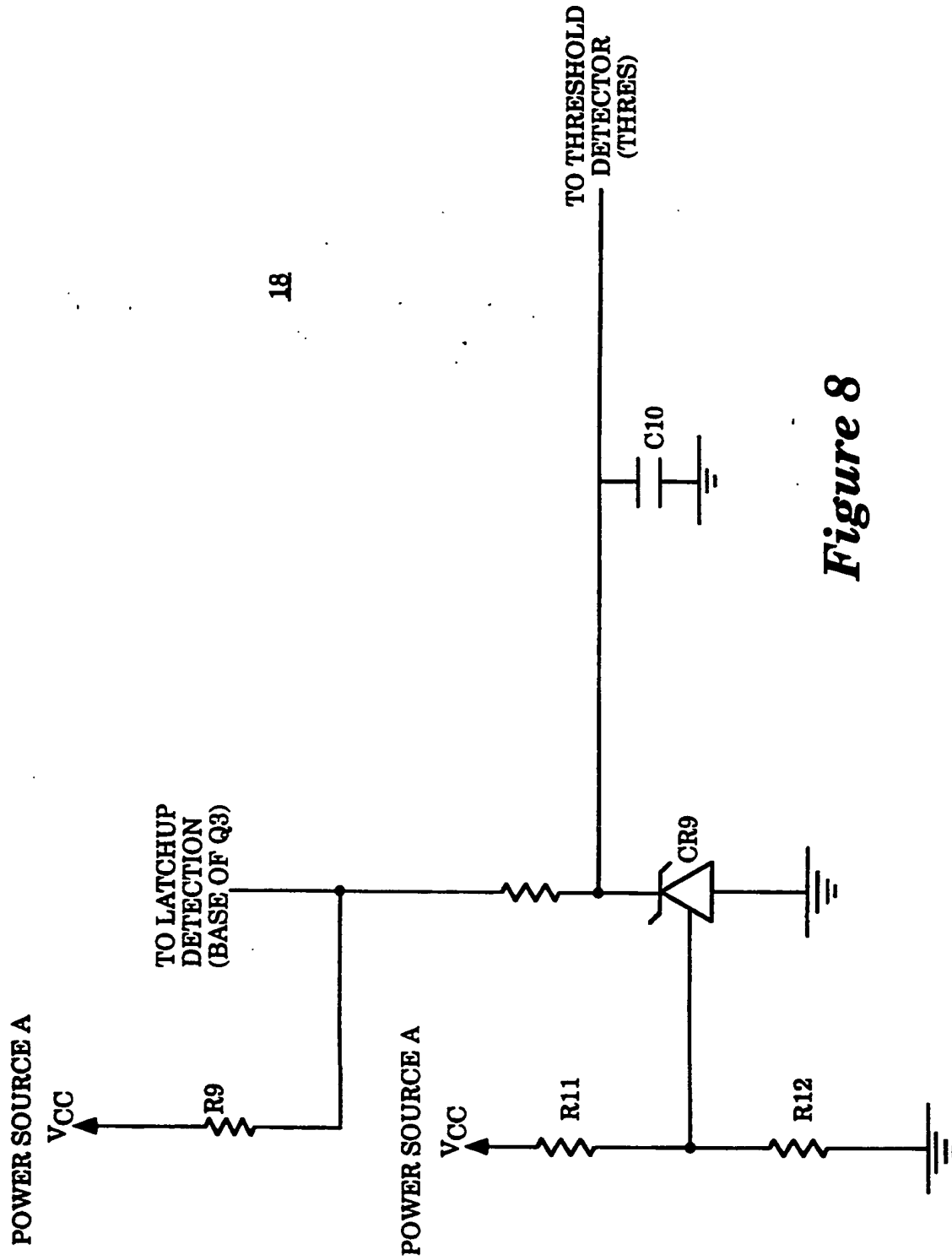


Figure 8

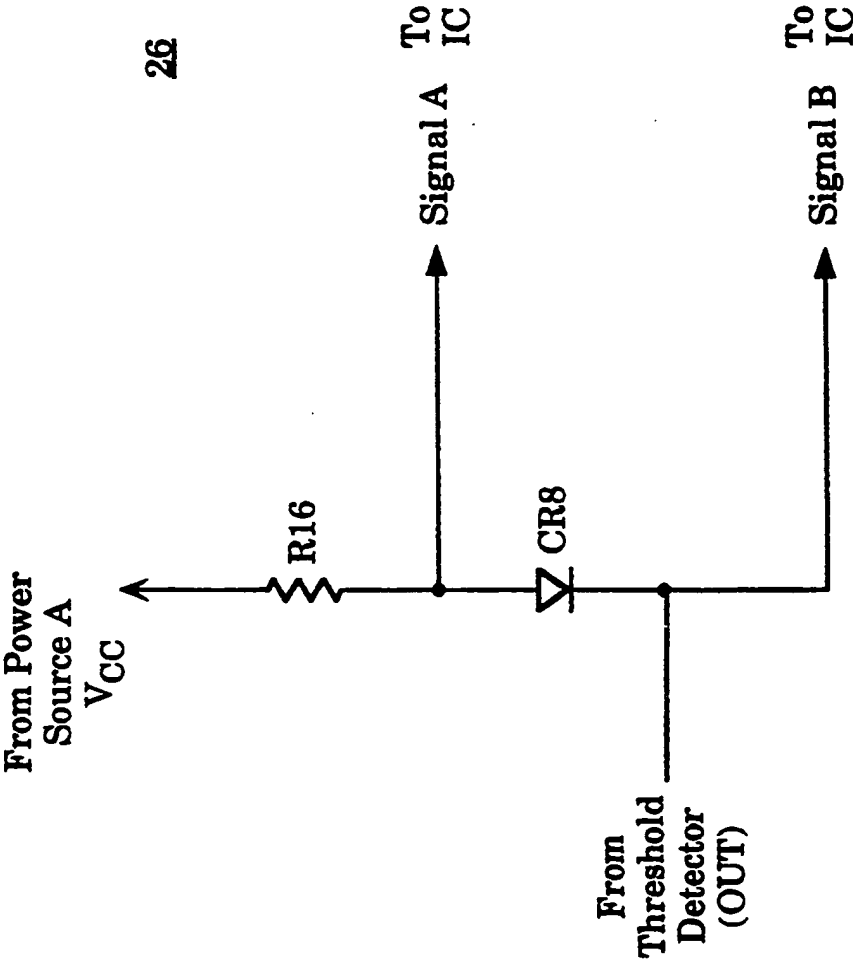


Figure 9

## PROVIDING VARIOUS ELECTRICAL PROTECTIONS TO A CMOS INTEGRATED CIRCUIT

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to the field of integrated circuit, more specifically, CMOS based integrated circuits. The present invention relates to providing various electrical protections to a CMOS integrated circuit.

#### 2. Art Background

It is a well known fact that, under certain conditions, a parasitic pnpn junction would be created in a CMOS integrated circuit, resulting in the latchup and possibly destruction of the CMOS integrated circuit. For certain CMOS integrated circuits receiving power supply from more than one source, i.e. power being supplied through the inputs as well as from the  $V_{cc}$  pins, one of such conditions is the power being supplied in an improper sequence. Particular examples of such CMOS integrated circuits are CMOS integrated circuits in a processor module with their  $V_{cc}$  pins coupled to an in-circuit emulator (ICE), and their inputs coupled to an ISA bus having a number of drivers with large current delivery capacity.

Traditionally, integrated circuit designers have often relied on the fact that typically the operating characteristics of a CMOS integrated circuit are insufficient to surpass the high current threshold for triggering a latchup. The potential problem is simply ignored. Other times when the operating characteristics of a CMOS integrated circuit are sufficient to surpass even the high current threshold and trigger a latchup, it is often left up to the user to ensure that the power is applied in proper sequence.

Alternatively, a fuse or a polyfuse may be employed to protect the CMOS integrated circuit. A polyfuse is a self-closing circuit breaker. The use of a low cost one time fuse has the disadvantage of having to have the fuse replaced, each time it is blown. Such a requirement is often unacceptable, particularly in situations where the CMOS integrated circuits are used in a novice end user application, such as personal computer or consumer electronics. On the other hand, the use of a polyfuse has the disadvantages of being more costly, and having to wait for it to reclose.

As a further alternative, an intervening protection circuitry may be provided to enforce the sequence in which the power is to be applied. However, a practical intervening protection circuitry for a VLSI environment must be low in economic cost as well as hardware real estate cost.

On the other hand, it will be desirable if a low cost intervening protection circuitry could nevertheless provide protection against potential damages resulted from reverse current being sourced from one of the power supply to another power supply being deenergized unexpectedly. An intervening protection circuit between the deenergized power supply and the CMOS integrated circuits, in conjunction with the CMOS integrated circuits, may behave in such a manner, that allows current to be sourced from the drivers of the still energized power supply to the deenergized power supply. Since a deenergized power supply looks like a low impedance to ground, the drivers of the still energized power supply, the CMOS integrated circuits, as well as

the intervening protection circuit itself could be strained beyond their maximum current ratings.

Furthermore, for CMOS integrated circuits comprising volatile SRAM-based software-downloaded Field Programmable Gate Array (FPGA), it will also be desirable if the low cost intervening protection circuit could also protect these SRAM-based FPGA from destructive reconfiguration as a result of low voltage.

As will be disclosed, the present invention provides a method and apparatus for providing various electrical protections to a CMOS integrated circuit that achieves the above described desired results.

### SUMMARY OF THE INVENTION

A electrical protection circuit providing latchup, reverse current and low voltage protection to a CMOS integrated circuit is disclosed. The electrical protection circuit has particular application to protecting CMOS integrated circuits receiving power supplies from a power source A, and a power source B comprising a number of drivers with high current delivery capacity. The electrical protection circuit comprises a latchup detection circuit, a threshold detector, an oscillator, a charge pump, a switching circuit, a voltage reference and detection circuit, and a signaling circuit. The latchup detection circuit, the threshold detector, the oscillator, the charge pump, and the switching circuit cooperate to provide latchup protection for the CMOS integrated circuit. The switching circuit provides integrated reverse current protection to the CMOS integrated circuit. The voltage reference and detection circuit, the threshold detector and the signaling circuit provides low voltage protection for the SRAM-based FPGA of the CMOS integrated circuit.

The latchup detection circuit drives a RESET input of the threshold detector high in the absence of a latchup condition, and pulls the RESET input low in the presence of a latchup condition. A latchup condition exists, whenever any of the power supplies from power source B rises above a predetermined voltage ( $V_B$ ), before the power supply from power source A rises above a predetermined voltage ( $V_A$ ). The RESET input resets the threshold detector when it is driven low. The threshold detector gates the oscillator; it releases the oscillator's feedback path, allowing oscillation, when the RESET input is driven high, and grounds the oscillator's feedback path, preventing oscillation, when the RESET input is driven low. The oscillator, when allowed to oscillate, generates current pulses for the charge pump. The charge pump boosts the voltage, supplying the boosted voltage to the switching circuit, thereby closing the switching circuit. The switching circuit is designed to quickly open, whenever the boosted voltage is withdrawn. As a result, power from source A is provided to the CMOS integrated circuit whenever the power supply from power source A rises above  $V_A$ , before any of the power supplies from power source B rises above the predetermined voltage  $V_B$ , and deprived from the CMOS integrated circuit, whenever the converse is true.

The switching circuit comprises FET transistor switches. The FET transistor switches are connected in series at their sources, causing their parasitic zener diodes to be connected in opposing fashion. Thus, at any particular point in time, one of the parasitic zener diodes will be reversed biased. As a result, current will be shut off, whenever the FET transistor switches' gates are

grounded, regardless whether their drains are energized, thereby preventing current to be sourced from power source B to power source A if power source A is deenergized unexpected while power source B is still energized.

The voltage reference and detection circuit provides voltage to pull the THRES input of the threshold detector above its trigger range upon detecting a low voltage condition, and allow the THRES input to fall below the trigger range in the absence of the low voltage condition. A low voltage condition exists when the voltage of power source A falls below  $V_A$ . Concurrently, the voltage reference and detection circuit causes the base-emitter junction of a transistor in the latchup detection circuit to be reverse biased upon detecting the low voltage condition. The latchup detection circuit grounds the TRIG and RESET inputs of the threshold detector, whenever the base-emitter junction of the particular transistor is reverse biased. The threshold detector, as a result of its RESET input being grounded, grounds the feedback path of the oscillator, preventing oscillation, thereby shutting off the charge pump, opening up the switching circuit, and depriving the CMOS integrated circuit of power from power source A. Additionally, the threshold detector, as a result of its THRES input being pulled above its trigger range, drives its OUT output low. In response to the OUT output of the threshold detector going low, the signaling circuit generates a number of signals indicating a low voltage condition.

In one embodiment, the signaling circuit generates two low voltage indicator signals, one for a configuration engine coupled to the SRAM-based FPGA of the CMOS integrated circuit, another one for an isolation gate coupled to the CMOS integrated circuit. Having been informed of the low voltage condition, the configuration engine reloads the SRAM-based FPGA when the fault is subsequently cleared. Upon notified of the low voltage condition, the isolation gate isolates the CMOS integrated circuit from other CMOS integrated circuits receiving power supply from power source B.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention will be apparent from the following detailed description of the presently preferred and alternate embodiments of the invention with references to the drawings in which:

FIG. 1 illustrates one embodiment of the present invention for providing various electrical protections to a CMOS integrated circuit having more than one power supply.

FIG. 2 illustrates a component view of the present invention.

FIG. 3 illustrates the latch up protection circuit of the present invention.

FIG. 4 illustrates the threshold detector of FIG. 2.

FIG. 5 illustrates the oscillator of FIG. 2.

FIG. 6 illustrates the charge pump of FIG. 2.

FIG. 7 illustrates the switching circuit of FIG. 2.

FIG. 8 illustrates the voltage reference and detection circuit of FIG. 2.

FIG. 9 illustrates the signaling circuit of FIG. 2.

#### DETAILED DESCRIPTION PRESENTLY PREFERRED AND ALTERNATE EMBODIMENTS

A electrical protection circuit providing latchup, reverse current and low voltage protection to a CMOS integrated circuit is disclosed. The electrical protection circuit has particular application to CMOS integrated circuits receiving power supplies from a power source A, and a power source B comprising a number of drivers with high current delivery capacity. In the following description for purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well known systems are shown in diagrammatical or block diagram form in order not to obscure the present invention unnecessarily.

Referring now to FIG. 1, a block diagram illustrating an embodiment of the present invention. Shown is a mechanical interface board 10 comprising the electrical protection circuit of the present invention coupled to a CMOS integrated circuit. The electrical protection circuit in the mechanical interface board 10 receives power supplies from both sources of the CMOS integrated circuit 12. The CMOS integrated circuit 12 receives one of its power supply from one of the sources (source A) indirectly through the electrical protection circuit in the mechanical interface board 10, and from the other source (source B) directly.

Power source A is intended to represent a broad category of main power supply to the CMOS integrated circuit, such as the ICE power supply to CMOS integrated circuits of a processor module described in the earlier example. Power source B is intended to represent a broad category of multiple secondary power supplies, such as the various power being supplied from the drivers of an ISA bus coupled to the processor module having large current delivery capacity as described in the earlier example.

While the present invention is being illustrated with the electrical protection circuit disposed in the mechanical interface board 10 of the CMOS integrated circuit 12, based on the descriptions to follow, it will be appreciated that the present invention may be practiced with the electrical protection circuit disposed on other media.

Referring now to FIG. 2, a block diagram illustrating a component view of the electrical protection circuit of the present invention. The 1.5 electrical protection circuit 14 comprises a latchup detection circuit 16, a voltage reference and detection circuit 18, and a switching circuit 28. Additionally, the electrical protection circuit 14 comprises a threshold detector 20, an oscillator 22, a charge pump 24, and a signaling circuit 26. The latchup detection circuit 16, the threshold detector 20, the oscillator 22, the charge pump 24, and the switching circuit 28 cooperate to provide latch up protection for the CMOS integrated circuit. The switching circuit 28 provides integrated reverse current protection to the CMOS integrated circuit. The voltage reference and detection circuit 18, the threshold detector 20 and the signaling circuit 26 provides low voltage protection for the SRAM-based FPGA of the CMOS integrated circuit. The manner in which each of these electrical protections is effectuated through these components will be

described in turn, with additional periodic references to the remaining figures, which illustrate these components in further detail.

Still referring to FIG. 2, latch up protection will first be described. The latchup detection circuit 16 is used to driver a RESET input of the threshold detector 20 high in the absence of a latchup condition, and drives the RESET input low in the presence of a latchup condition. A latchup condition exists, whenever any of the power supplies from power source B rises above a predetermined voltage ( $V_B$ ), before the power supply from power source A rises above a predetermined voltage ( $V_A$ ). The RESET input is used to reset the threshold detector 20, when it is driven low. The threshold detector 20 is used to gate the oscillator 22; it releases the feedback path of the oscillator 22, allowing oscillation, when its RESET input is driven high, and grounding the feedback path of the oscillator 22, preventing oscillation, when its RESET input is driven low. The oscillator 22, when allowed to oscillate, is used to generate current pulses for the charge pump 24. The charge pump 24 is used to boost voltage, and supply the boosted voltage to the switching circuit 28, thereby closing the switching circuit 28. The switching circuit 28 is designed to open quickly, when it is deprived of the boosted voltage. Thus, power from source A is provided to the CMOS integrated circuit whenever the power supply from power source A rises above  $V_A$ , before any of the power supplies from power source B rises above the predetermined voltage  $V_B$ , and deprived from the CMOS integrated circuit, whenever the converse is true.

Referring now FIG. 3, a circuit diagram illustrating the elements of the latchup detection circuit in further detail is shown. The latchup detection circuit 16 comprises a silicon controlled rectifier CR10, a diode CR11, a pnp transistor Q3, and a npn transistor Q4. The cathode of CR10 is coupled to a RESET pin of the threshold detector and a TRIG pin of the threshold detector through a resistor R15, the gate of CR10 is coupled to the cathode of CR11, and the anode of CR10 is coupled to the collector of Q3. The emitter of Q3 is coupled to power source A of the CMOS integrated circuit, and the base of Q3 is coupled to the voltage reference. The collector of Q4 is coupled to the connection of CR10 and Q3 through a resistor R8, the emitter of Q4 is coupled to ground, and the base of Q4 is coupled to the power sources of power source B of the CMOS integrated circuit. The anode of CR11 is coupled to the connection between the collector of Q4 and the resistor R8.

Additionally, the latchup detection circuit 16 comprises a resistor R6 which connects the connection between the power source B and the base of Q4 to ground, a resistor R5 and a capacitor C13 which parallelingly connects the connection between the cathode of CR11 and the gate of CR10 to ground, a resistor R7 and a capacitor C15 which parallelingly connects the connection between the resistor R15 and the TRIG pin to ground.

The physical characteristics of R6, R8 and Q4 are designed to complement the characteristics of power sources A and B, such that together they ground the collector of Q4 before Q3 can be turned on, if any power supplied from power source B is above  $V_B$  before power source A rises above  $V_A$ . For example, R6, R8, and Q4 may be designed to ground the collector of Q4 before Q3 can be turned on, if any power supplied

from power source B is above 1.0 volt before power source A rises above 4.5 volts.

Similarly, the characteristics of CR10 and CR11 are designed to be such that when the collector of Q4 is grounded, the anode of CR11 will be below a predetermined voltage ( $V_{CR11-A}$ ), thereby causing the cathode to be below another predetermined voltage ( $V_{CR11-C}$ ), the minimum trigger voltage necessary to close CR10 ( $V_{CR10-G}$ ). For example, CR11 may be designed such that when the collector of Q4 is grounded, the anode of CR11 is below 0.5 volt, thereby causing the cathode of CR11 to be below 0.1 volt, the minimum trigger voltage necessary to close CR10.

When CR10 is open, its cathode is effectively grounded through R15 and R7, thereby causing the RESET pin of the threshold detector to be grounded, driving the RESET input low. Even if Q3 is subsequently turned on, CR10 will remain open. Thus, the RESET pin of the threshold detector remains grounded, and the RESET input remains low.

On the other hand, if all the power supplies from power source B are below  $V_B$ , then the collector of Q4 is open, allowing the anode of CR11 to be electrically connected to power source A through R8 and Q3. Thus, when Q3 is turn on, the cathode of CR11 will exceed  $V_{CR11-C}$ , the minimum voltage necessary to trigger and turn on CR10  $V_{CR10-G}$ . Once CR10 is turn on, the RESET pin is set, driving the RESET input to high.

Additionally, R6 is also used to pull down on the base of Q4 preventing the self-biasing of Q4 when there is no other current path from power source B to ground. R5 is used to provide a path to ground when no current is sourced through CR11, preventing CR10 from triggering, since a voltage sufficiently high to trigger CR10 is easily developed across R5 when sufficient current is present at the cathode of CR11. C13 is used as a noise suppressor which keeps electrostatic discharge events from triggering CR10. C15 serves as a time delay, ensuring that after the RESET input of the threshold detector goes high (inactive), the TRIG input of the threshold detector stays low (active). The function and usage of the TRIG input of the threshold detector will be described later, when low voltage protection is described.

Referring now to FIG. 4, a circuit diagram illustrating one embodiment of the threshold detector is shown. In this embodiment, the threshold detector 20 comprises two comparators, 32 and 34, a sequential logic 36, a FET transistor switch 38, and a number of resistors, R32-R34. The threshold detector 20 receives a first and a second input, RESET and TRIG, from the latchup detection circuit, a third input THRES from the voltage reference and detection circuit, and power supply from power source A. In response, the threshold detector 20 outputs a first and a second output, OUT and DISCH.

The RESET input drives the R1 input of the sequential logic 36 directly. R1 is low when RESET is low. The THRES input and the voltage level of power source A drives the R input of the sequential logic 36 through the first comparator 32. R is high when THRES is higher than a predetermined minimum voltage. Similarly, the TRIG input and the voltage level of power source A drives the S input of the sequential logic 36 through the second comparator 34. S is high when TRIG is lower than a predetermined minimum voltage. The output of the sequential logic 36 drives the OUT output directly, and the DISCH output through

the FET transistor switch 38 in conjunction with the power supply from power source A. The various output states of the OUT and DISCH output are given in the truth table in FIG. 4.

Referring now to FIG. 5, a circuit diagram illustrating one embodiment of the oscillator is shown. In this embodiment, the oscillator 22 comprises an internal timer 30, two capacitors C11 and C12, and two resistors R13 and R14. The oscillator 22 receives the DISCH output from the threshold detector as input and power supply from power source A. In response, the oscillator 22 conditionally outputs current pulses to the charge pump.

The internal timer 30 comprises six pins, pin 8 TRIG, pin 10 RESET, pin 11 CONT, pin 12 THRES, Pin 9 OUT, and pin 13 DISCH. Pin 10 RESET is coupled to power source A and to ground through R14, R13, and C12. Pin 8 TRIG and pin 12 THRES are coupled to power source A through R13 and R14, to pin 13 DISCH through R 13, and to ground through C12. The manner in which these elements cooperate to function as an oscillator and generate current pulses is well known and will not be further described here.

The oscillator 22 is allowed to oscillate, thereby sourcing current pulses to the charge pump, when the DISCH output of the threshold detector is high, releasing the feedback path of the oscillator 22. The oscillator 22 is prevented from oscillating, thereby depriving current pulses to the charge pump, when the DISCH output of the threshold detector is low, grounding the feedback path of the oscillator 22.

The physical characteristics of these elements are designed to achieve an oscillating frequency that complements the load to be placed on the charge pump. The internal timer 30 may be implemented with circuitry similar to the threshold detector described earlier or its equivalent. Additionally, even though the oscillator 22 is described as a "timer-based" oscillator, it will be appreciated that the present invention may be practiced with "non-timer based" oscillators.

Referring now to FIG. 6, a circuit diagram illustrating one embodiment of the charge pump is shown. In this embodiment, the charge pump 24 comprises a npn transistor Q2 and a brigade of capacitor-diode buckets CR1-CR7 and C2-C8. Additionally, the charge pump 24 comprises a speedup capacitor C9 and two resistors R17 and R18. The charge pump receives current pulses as input through the OUT output of the oscillator and power supply from power source A. In response, the charge pump boost the voltage and output the boosted voltage to the switching circuit.

The base of Q2 is coupled to the oscillator output through the speedup capacitor C9 or the resistor R 17, the emitter of Q2 is coupled to ground, and the collector of Q2 is coupled to power source A through the resistor R18 and the capacitor-diode bucket brigade, CR1-CR7 and C2-C8. The resistor R17 serves as a current limiter to the base of Q2, and the speedup capacitor C9 is used to improve the efficiency of the charge pump 24. In order for the charge pump to operate efficiently, the waveform entering it must transition all the way from  $V_{cc}$  to ground. One way to ensure that is to get the fastest possible edges out of the collector of Q2. To do so, the charges in the saturated base-collector junction of Q2 must be swept out quickly, preventing a large delay between grounding the base and floating the collector of Q2. The speedup capacitor C9 provides an additional path from the base of Q2 to ground when the

input to R17 drops from some voltage to ground. Since C9 is discharged, this additional path initially looks like a short to ground. This low resistance path is only temporary, until C9 is charged up with the charge in the collector-base junction of Q2, thereby sweeping the charges out of the base-collector junction of Q2 quickly.

The diode-capacitor matrix, CR1-CR7 and C2-C8, cooperate to produce a steady state voltage  $4 \times V_{cc}$  for the switching circuit. The manner in which the diode-capacitor matrix cooperate to achieve the desired boosted voltage is well known and will not be further described here. While the charge pump has been illustrated with an embodiment that yield  $4 \times V_{cc}$ , it will be appreciated that the present invention may be practiced with a charge pump having pump capacity that is greater or smaller than the embodiment illustrated, depending on the characteristics of the switching circuit. The boosted voltage must be high enough to close the switching circuit, and the charge pump current capacity must be high enough to provide the voltage required by the switching circuit.

Referring now to FIG. 7, a circuit diagram illustrating one embodiment of the switching circuit is shown. In this embodiment, the switching circuit 28 comprises two resistors, R19 and R20, and two FET transistor switches, Q1 and Q5. The switching circuit receives the boosted voltage from the capacitor-diode bucket brigade of the charge pump as input, and power supply from power source A. In response, the switching circuit 28 closes, allowing the power supply from power source A to be provided to the CMOS integrated circuit.

Q1 and Q5, are connected in series at their sources, thereby causing their zener diodes to be connected in opposing fashion. The drain of Q5 is coupled to power source A, whereas the drain of Q1 is coupled to the CMOS integrated circuit. The gates of Q1 and Q5 are coupled to last capacitor-diode bucket of the capacitor-diode bucket brigade of the charge pump. Additionally, the connection between the sources of Q1 and Q5, and the connection between the gates of Q1 and Q5 and the capacitor-diode bucket brigade, are grounded through R19 and R20 respectively.

Thus, when the pumped up voltage is applied to the gates of Q1 and Q5 by the charge pump, Q1 and Q5 close, thereby allowing power to be supplied from power source A to the CMOS integrated circuit. R 19 serves as a source reference for the gates of Q1 and Q5, to guard against the unlikely event that the switch is prevented from closing by a high voltage at the drain of Q1. On the other hand, when the pumped up voltage is withdrawn from the gates of Q1 and Q5 after the charge pump is shut off, Q 1 and Q5 open, thereby depriving the CMOS integrated circuit of power supplied from power source A. R20 serves at a gate leakage resistor, allowing the gates of Q1 and Q5 to discharge quickly after the charge pump has shut off, thereby quickly opening the switching circuit 28 and quickly depriving power supply from power source A from the CMOS integrated circuit.

The current capacity of the switching circuit 28 is designed to complement the load presented by the CMOS integrated circuit to be protected. The gate bleeder resistor R20 is designed to be large enough to prevent dropping the pumped up voltage, and yet small enough to give a satisfactory quick turn-off time for the switching circuit. Additionally, it will be appreciated

that the zener diodes of the Q 1 and Q5 are not "enabling" elements of the present invention, they are more like "constraints" imposed by the present FET technology, that the present invention has to contend with.

Still referring to FIG. 7, reverse current protection will next be described. Since Q1 and Q5 are connected in series at their sources, causing their zener diodes to be connected in opposing fashion. At any particular point in time, one of the zener diodes will be reversed biased. Thus, current will be shut off, whenever the gates of Q 1 and Q5 are grounded, regardless whether the drain of Q5 or Q1 is energized. Thus, if power source A is deenergized unexpectedly, causing the gates of Q1 and Q5 to be grounded, the switching circuit will quickly open, preventing current to be sourced from power source B, through the CMOS integrated circuit and the electrical protection circuit of the present invention to power supply A.

Referring back to FIG. 2, low voltage protection will next be described. The voltage reference and detection circuit 18 is used to provide voltage to pull the THRES input of the threshold detector 20 above its trigger range upon detecting a low voltage condition, and allow the THRES input to fall below the trigger range in the absence of the low voltage condition. A low voltage condition exists when the voltage of power source A falls below  $V_A$ . Concurrently, the voltage reference and detection circuit 18 is also used to reverse biased the base-emitter junction of Q3 in the latchup detection circuit 18 upon detecting the low voltage condition. The latchup detection circuit 16 is also used to ground the TRIG and RESET inputs of the threshold detector 20, whenever the base-emitter junction of Q3 is reverse biased. The threshold detector 20 is used to shutoff the oscillator 22 as a result of its TRIG and RESET inputs being grounded, thereby shutting off the charge pump 24, opening up the switching circuit 28, and depriving the CMOS integrated circuit of power from power source A. The threshold detector 20 is also used to allow current to be sourced to the signaling circuit 26 as a result of its THRES input being pulled above the trigger range. The signaling circuit 26 is used to generate a number of signals indicating a low voltage condition, thereby preventing erroneous reconfiguration of SRAM-based FPGA on the CMOS integrated circuit.

Referring now to FIG. 8, a circuit diagram illustrating the voltage reference and detection circuit in further detail is shown. The voltage reference and detection circuit 18 comprises a zener diode CR9, two pairs of resistors, R9 and R10, and, R11 and R12, and a capacitor C10. The voltage reference and detection circuit 18 receives power supply from power source A. In response, the voltage reference and detection circuit 18 allows power from power source A to be sourced to the base of Q3 of the latchup detection circuit, and the THRES input of the threshold detector.

The cathode of CR9 is coupled to power source A through the resistor pair R9 and R10, to the base of Q3 in the latchup detection circuit through R10, and to the THRES input of the threshold detector. The anode of CR9 is coupled to ground, and the gate is coupled also to power source A through R11. Additionally, the connection between the cathode of CR9 and the THRES input is coupled to ground through C10, and the connection between the gate of CR9 and R11 is coupled to ground through R 12.

When the voltage of power source A goes below  $V_A$ , CR9 becomes an open circuit. The cathode of CR9 goes to  $V_{cc}$  through R9 and R10. The THRES input of the threshold detector is also pulled to  $V_{cc}$  through the same resistors, thereby pulling it above its trigger range. Concurrently, when CR9 becomes open, the base-emitter junction of Q3 in the latchup detection circuit becomes reverse biased. C10 keeps the THRES pin below the trigger range (inactive) while  $V_{cc}$  is ramping up. When  $V_{cc}$  settles below the trigger range of CR9 indicating a lower power source A voltage condition, then CR9 will remain open, allowing C10 to charge up to the trigger range, resetting the threshold detector, keeping the switching circuit open. When  $V_{cc}$  settles above the trigger range of CR9 indicating a satisfactory power source A voltage condition, then CR9 will close, preventing CR10 from changing up to the trigger voltage of the THRES input allowing TRIG to control the state of OUT and DISCH outputs. Since power source A supplies  $V_{cc}$  to charge C10 as well as  $V_{cc}$  to the threshold detector, and since the trigger range of the THRES input is a function of  $V_{CC}$ , then the delay induced by C10 between the ramp-up of the THRES input versus the ramp-up of  $V_{cc}$  is sufficient to hold the THRES input below its trigger range until CR9 closes.

Referring back to FIGS. 3-4, when the opening of CR9 in the voltage reference and detection circuit causes the base-emitter junction of Q3 of the latchup detection circuit to be reverse biased, the collector of Q3 is grounded through CR10, R 15 and R7 of the latchup detection circuit 16. Thus, the RESET as well as the TRIG inputs of the threshold detector 20 also get grounded. As described earlier, the opening of CR9 in the voltage reference and detection circuit also causes the THRES input to be pulled above its trigger range. As a result, as illustrated by the truth table in FIG. 4, both the OUT and DISCH outputs of the threshold detector 20 are grounded.

Referring now to FIG. 9, a circuit diagram illustrating one embodiment of the signal generator is shown. In this embodiment, the signaling circuit 26 comprises a diode CR8 and a resistor R16. The signal generating circuit receives the OUT output of the threshold detector as input, and power supply from power source A. In response, the signaling circuit 26 generates two signals, A and B. Signal A is provided to a configuration engine coupled to the CMOS integrated circuit for configuring the SRAM-based FPGA of the CMOS integrated circuit. Having been notified of the low voltage condition, the configuration engine reloads the SRAM-based FPGA when the fault condition is cleared. Signal B is provided to an isolation gate coupled to the CMOS integrated circuit for isolating the CMOS integrated circuit from other CMOS integrated circuits receiving power supply from power source B only. Upon receipt of the notification, the isolation gate isolates the CMOS integrated circuit.

The anode of CR8 is coupled to power source A through R16, and the cathode is coupled to OUT of the threshold detector. Additionally, the connection between the anode of CR8 and R16, and the connection between the cathode of CR8 and the OUT output of the threshold detector, are coupled to the configuration engine and the isolation gate respectively. When the OUT output of the threshold detector is clamped to ground, it is driven low and causes the signals A and B to be provided to the configuration engine and the isolation gate respectively.

While the signaling circuit is being described with an embodiment that generates two signals, it will be appreciated that the present invention may be practiced alternative embodiments that generate more or less signals used for similar or different purposes.

While the present invention has been described in terms of presently preferred and alternate embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. The method and apparatus of the present invention can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting on the present invention.

What is claimed is:

1. A circuit for protecting a CMOS integrated circuit from latching up as a result of improper application of power to said CMOS integrated circuit, said CMOS integrated circuit receiving power supplies from more than one power source, said circuit comprising:

- a) a latchup detection circuit coupled to said power sources of said CMOS integrated circuit for detecting certain predetermined power differential pattern between a first and the remainder of said power sources and sourcing a first output current in response;
- b) a threshold detector coupled to said latchup detection circuit and said first power source for receiving said first output current from said latchup detection circuit and power from said first power source, and sourcing a second output current in response;
- c) an oscillator coupled to said threshold detector and said first power source for receiving said second output current from said threshold detector and power from said first power source, and alternately sourcing a third and a fourth output current in response;
- d) a charge pump coupled to said oscillator and said first power source for receiving said third and fourth output current alternately from said oscillator and power from said first power source, and providing a steady output voltage larger than said first power source' voltage; and
- e) a switching circuit coupled to said charge pump, said first power source, and said CMOS integrated circuit for receiving said steady output voltage from said charge pump and power from said first power source, and closing itself in response, allowing said power from said first power source to be provided to said CMOS integrated circuit.

2. The circuit as set forth in claim 1, wherein, said predetermined power differential pattern is a pattern under which one of said remainder power sources rises above a first predetermined voltage before said first power source rises above a second predetermined voltage.

3. The circuit as set forth in claim 2, wherein, said latchup detection circuit comprises:

- a.1) a pnp transistor coupled to said first power source and ground;
- a.2) a npn transistor coupled to said pnp transistor, the remainder power sources, and ground;
- a.3) a diode coupled to said pnp and npn transistors; and
- a.4) a silicon controlled rectifier coupled to said pnp transistor, said diode, said threshold detector, and ground.

4. The circuit as set forth in claim 1, wherein, said threshold detector comprises:

- b.1) first comparator means coupled to a voltage detection and reference circuit and said first power source for comparing a THRES input from said voltage detection and reference circuit to said first power source' voltage, and outputting a first comparison output;
- b.2) second comparator means coupled to said latchup detection circuit and said first power source for comparing a TRIG input from said latchup detection and reference circuit to said first power source' voltage, and outputting a second comparison output;
- b.3) combinatorial logic means coupled to said latchup detection circuit, said first and second comparator means for receiving a RESET input from said latchup detection circuit, and said first and second comparison outputs from said first and second comparator means respectively, and outputting a first threshold detector output; and
- b.4) transistor switch means coupled to said combinatorial logic means and said first power source for receiving said first threshold detector output from said combinatorial logic means and said power from said first power source, and outputting a second threshold detector output.

5. The circuit as set forth in claim 1, wherein, said oscillator comprises

- c.1) a first capacitor coupled to said first power source, said threshold detector and ground;
- c.2) a second capacitor coupled to ground; and
- c.3) an internal timer coupled to said first power source, said threshold detector, said first and second capacitors, and said charge pump.

6. The circuit as set forth in claim 1, wherein, said charge pump comprises:

- d.1) a capacitor-resistor combination coupled to said oscillator;
- d.2) a npn transistor coupled to said capacitor-resistor combination, said first power source and ground; and
- d.3) a capacitor-diode bucket brigade comprising a plurality of capacitor-diode buckets coupled to said npn transistor, said first power source, and said switching circuit.

7. The circuit as set forth in claim 1, wherein, said switching circuit comprises:

- e.1) a first transistor switch comprising a first zener diode coupled to said power source, said charge pump; and
- e.2) a second transistor switch comprising a second zener diode coupled to said first transistor switch, said first power source and said CMOS integrated circuit.

8. The circuit as set forth in claim 7, wherein, said circuit further provides reverse current protection for said CMOS integrated circuit;

said first and second transistor switches are coupled to each other serially at their sources with their zener diodes opposing each other, and coupled to said charge pump at their gates.

9. The circuit as set forth in claim 1, wherein, said circuit further provides low voltage protection to said CMOS integrated circuit's SRAM-based FPGA;

said circuit further comprises a voltage reference and detection circuit coupled to said first power source,



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said latchup detection circuit, and said threshold detector, for detecting a predetermined voltage drop pattern of said first power source, and sourcing a fifth output current to said threshold detector in response, said voltage reference and detection circuit also opening said latchup detection circuit in response;

said latchup detection circuit cuts off said first output current and a seventh output current to said threshold detector in response;

said threshold detector cuts off said second output current to said oscillator and drives low an output signal in response;

said oscillator cuts off said third and fourth output current to said charge pump in response;

said charge pump cuts off said steady output voltage to said switching circuit in response;

said switching circuit opens itself in response, depriving said CMOS integrated circuit of said power from said first power source;

said circuit further comprises a signaling circuit coupled to said threshold detector and said CMOS integrated circuit for receiving said low output signal and outputting a plurality of low voltage indicator signals.

10. The circuit as set forth in claim 9, wherein, said voltage reference and detection circuit comprises a zener diode coupled to said first power source, said threshold detector, and ground.

11. The circuit as set forth in claim 9, wherein, said low voltage indicator signals comprise a first and a second signal, said first signal being provided to a configuration engine coupled to said CMOS integrated circuit for configuring SRAM-based software-downloaded Field Programmable Gate Array (FPGA) of said CMOS integrated circuit,

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said second signal being provided to an isolation gate coupled to said CMOS integrated circuit for isolating said CMOS integrated circuit from other CMOS integrated circuits receiving power supply from the remaining power sources;

said signaling circuit comprises a diode coupled to said first power source, said threshold detector, said configuration engine and said isolation gate.

12. A circuit comprising:

a) state indicating means coupled to a first and a second power source comprising a silicon controlled rectifier for indicating one of two states, said state indicating means having the following state transition rules:

a.1) if said state indicating means is in a first state and said second power source is on, said state indicating means stays in said first state;

a.2) if said state indicating means is in said first state, said second power source is off, and said first power source is on, said state indicating means goes into a second state;

a.3) if said state indicating means is in said second state and said first power source is on, said state indicating means stays in said second state;

a.4) if said state indicating means is in said second state and said first power source is off, said state indicating means goes into said first state; and

b) enabling means coupled to said state indicating means, said first power source, and a CMOS integrated circuit for sourcing power from said first power source to said CMOS integrated circuit when said state indicating means is in said second state, and depriving power from said first power source to said CMOS integrated circuit when said state indicating means is in said first state.

\* \* \* \* \*

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UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. : 5,392,186  
DATED : February 21, 1995  
INVENTOR(S) : Alexander et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, at line 52, delete "The 1.5 electrical" and  
substitute --The electrical--.

Signed and Sealed this  
Twenty-ninth Day of October 1996

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks



## Javanifard et al.

[45] **Date of Patent:** **Oct. 3, 1995**

- [22] Filed: Mar. 14, 1995

### Related U.S. Application Data

- [62] Division of Ser. No. 119,425, Sep. 10, 1993.
- [51] Int. Cl.<sup>6</sup> ..... G11C 16/06  
[52] U.S. Cl. .... 365/185.18; 365/226; 365/230.06  
[58] Field of Search ..... 365/185, 226,  
  365/230.06, 218

- |           |         |                        |         |
|-----------|---------|------------------------|---------|
| 5,313,429 | 5/1994  | Chevallier et al. .... | 365/226 |
| 5,315,547 | 5/1994  | Shoji et al. ....      | 365/185 |
| 5,317,535 | 5/1994  | Talreja et al. ....    | 365/185 |
| 5,327,384 | 6/1994  | Ninomiya ....          | 365/185 |
| 5,329,488 | 7/1994  | Hashimoto ....         | 365/200 |
| 5,337,281 | 8/1994  | Kobayashi et al. ....  | 365/185 |
| 5,339,297 | 8/1994  | Toms et al. ....       | 365/185 |
| 5,375,094 | 12/1994 | Naruke ....            | 365/185 |

## OTHER PUBLICATIONS

**"TP9.3: A 5V-Only 0.6  $\mu$ m Flash EEPROM with Row Decoder Scheme in Triple-Well Structure", pp. 152-153 and 170, by Masao Kuriyama, Shigeru Alsumi, Axira Umezawa, Hironori Banba, Ken-ichi Imamiya, Kiyomi Naruke, Seiji Yamada, Etsushi Ohi.**

Masamitsu Oshikiri, Tomoko Suzuki, Mashashi Wada, Sumio Tanaka, 1992 IEEE International Solid-State Circuits Conference, ISSCC92 Session 9/Non-Volatile and Dynamic RAMS/Paper 9.3.

*Primary Examiner*—Joseph E. Clawson, Jr.

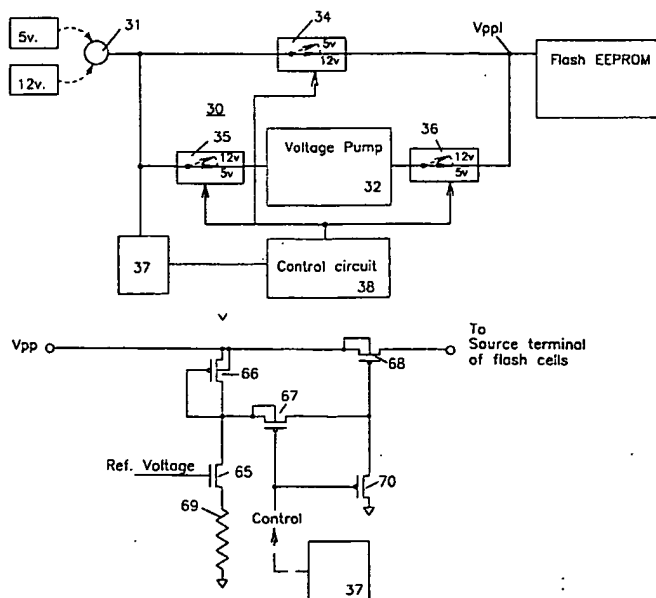
**Attorney, Agent, or Firm—**Blakely, Sokoloff, Taylor & Zafman

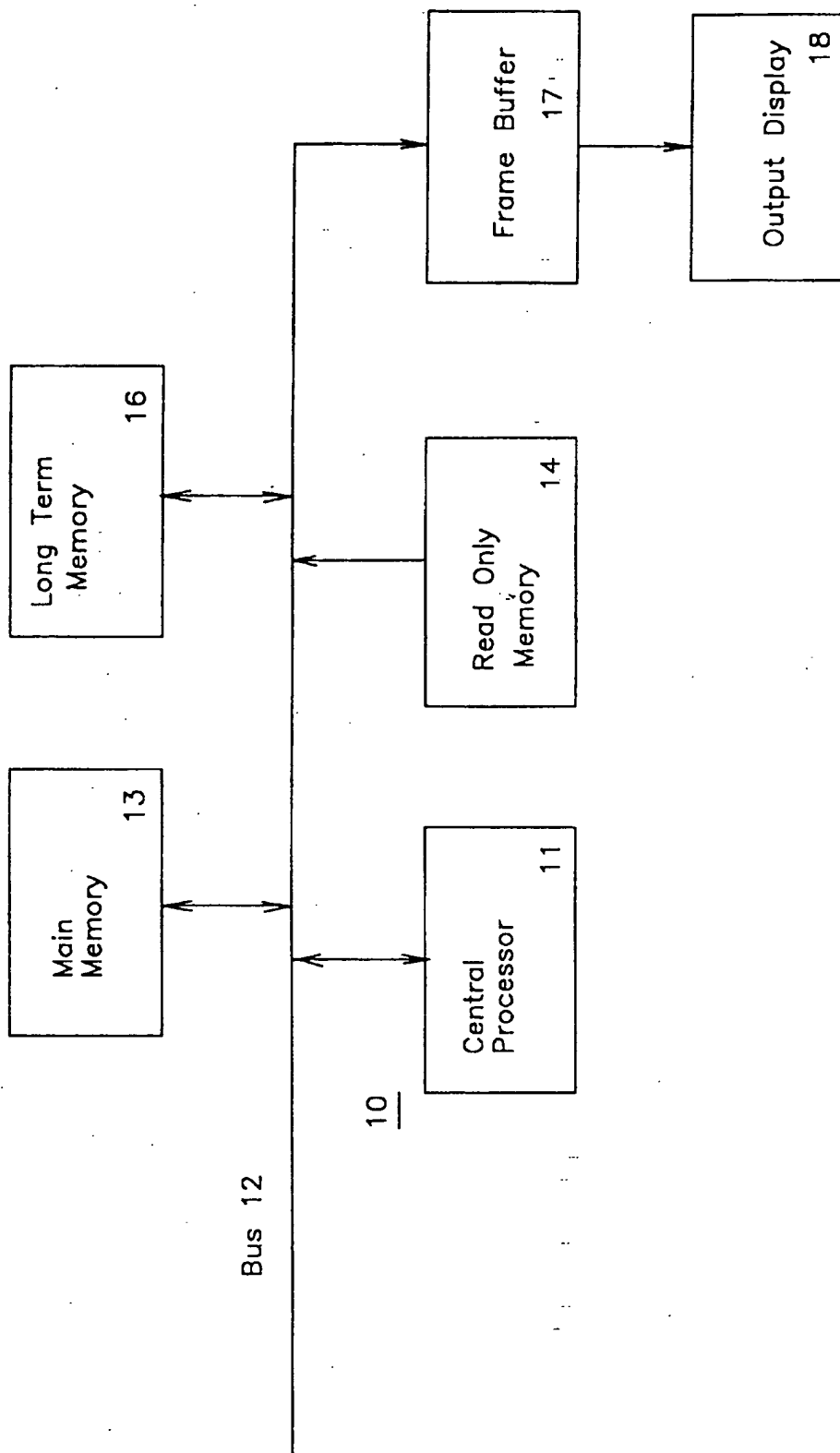
## ABSTRACT

- [57]

An integrated circuit which provides an arrangement by which the source of voltage for erasing the flash EEPROM memory array is detected and, if the source is a charge pump, the current provided is held to a constant lower value while, if the source is an external high voltage source, then the current is allowed to flow freely without regulation except by the size of a field effect transistor device in the path from the source of voltage to the memory array. In this manner, the circuitry is adapted to function with either internal or external power sources without paying a performance penalty for either type of operation.

**4 Claims, 6 Drawing Sheets**



Figure 1

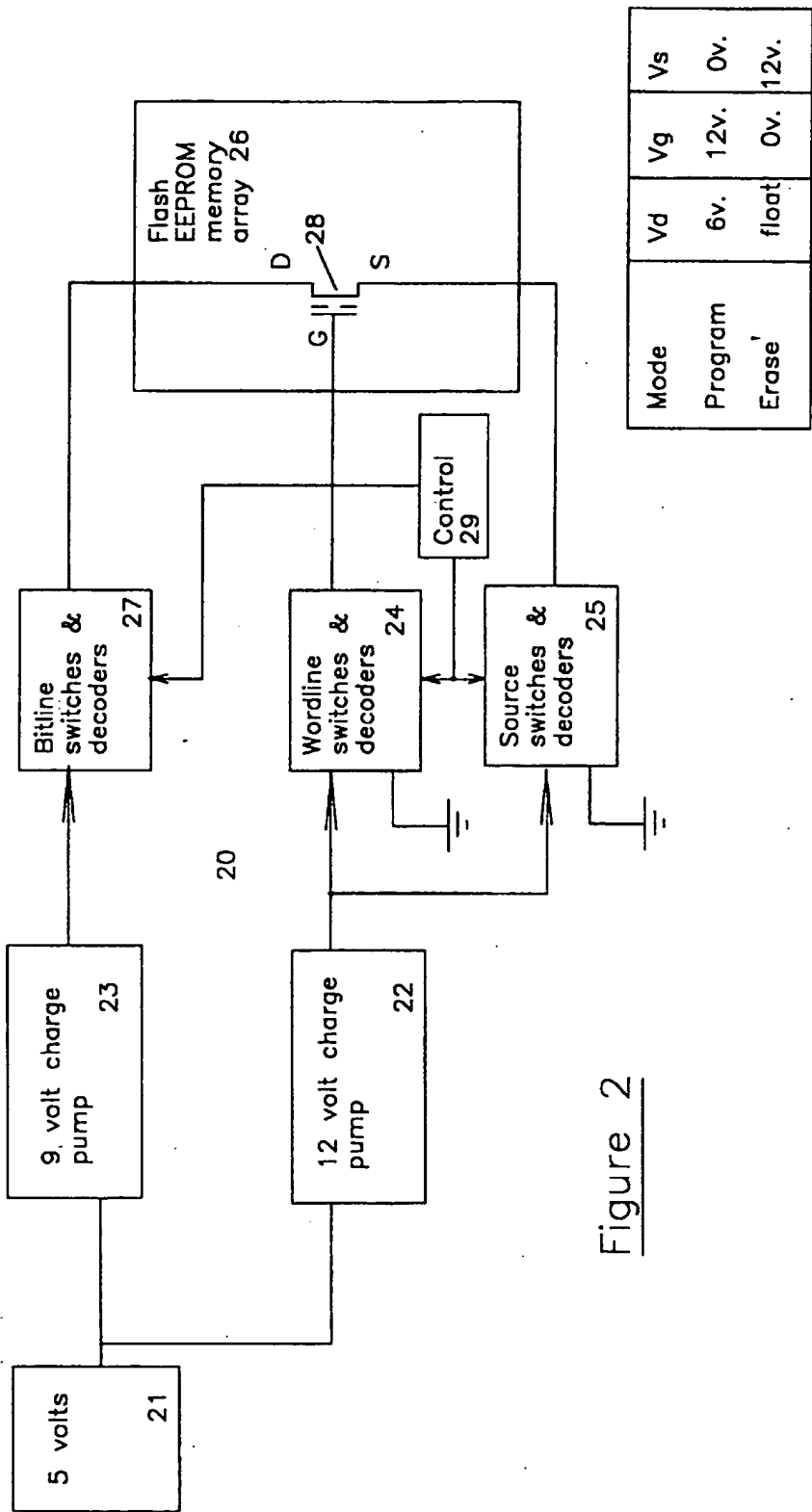


Figure 2

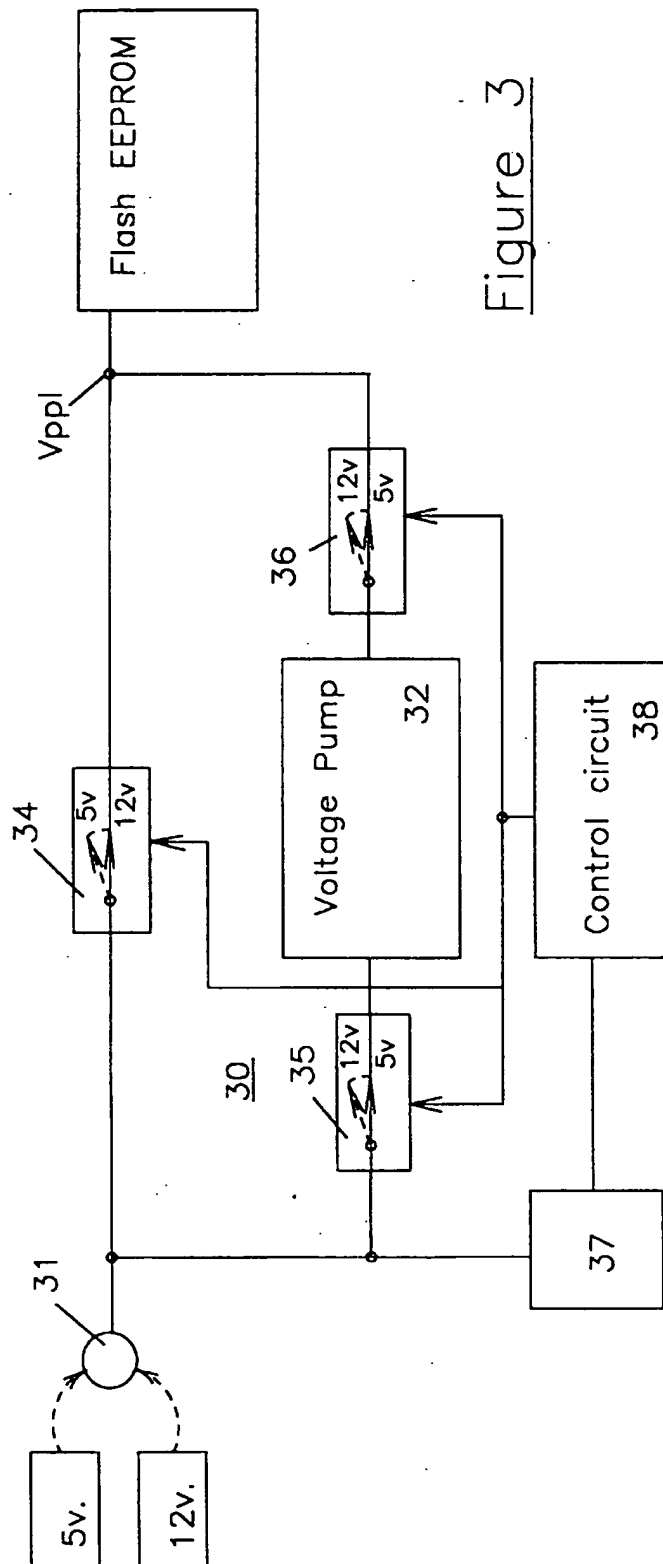


Figure 3

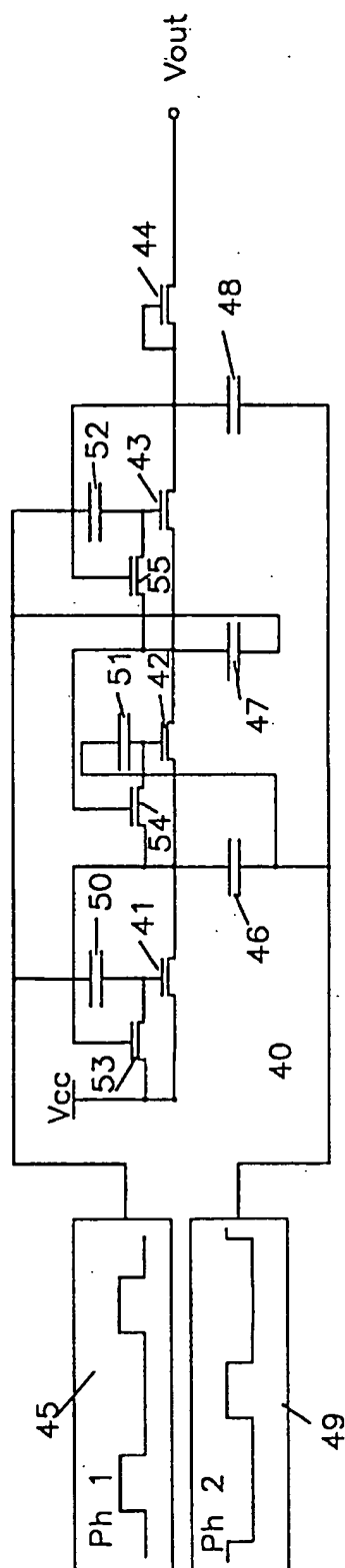


Figure 4

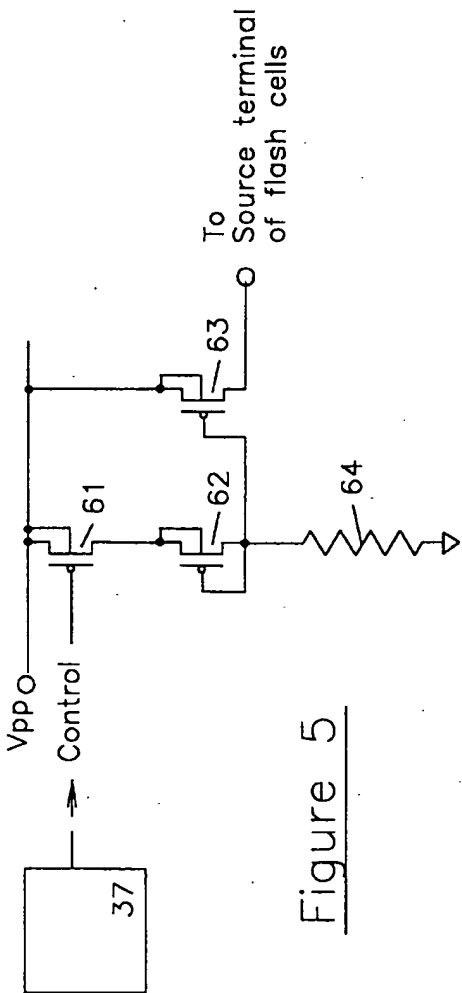


Figure 5

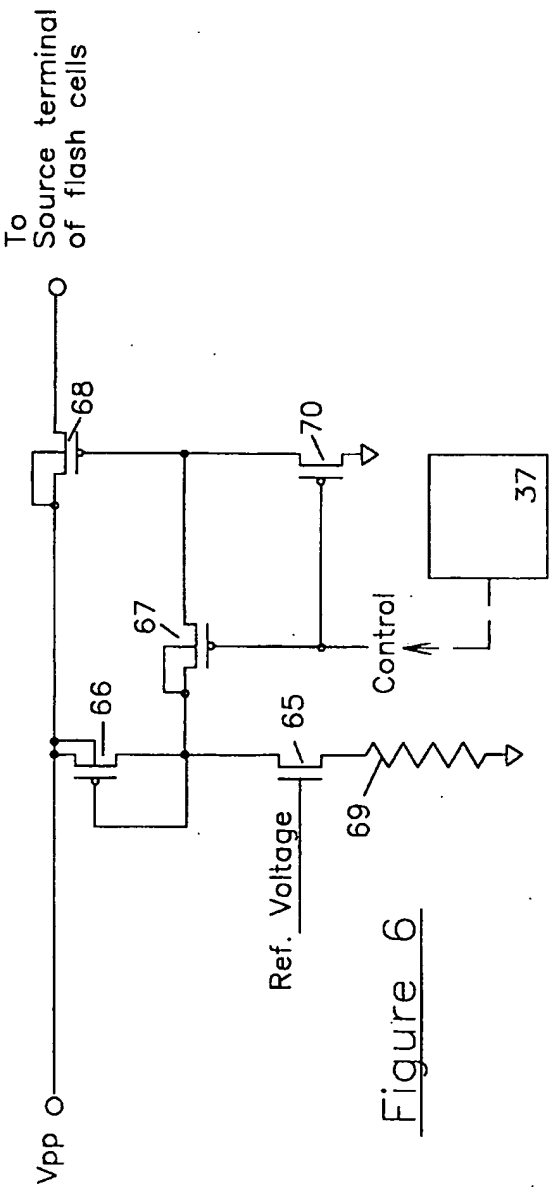
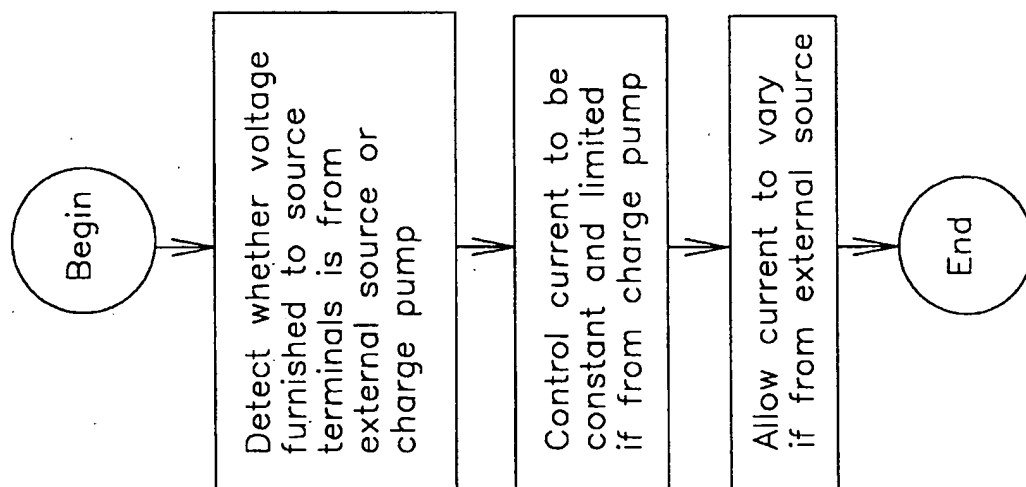


Figure 6



Figure 7

# METHOD AND APPARATUS FOR CONTROLLING THE OUTPUT CURRENT PROVIDED BY A CHARGE PUMP CIRCUIT

This is a divisional of application Ser. No. 08/119,425, filed Sep. 10, 1993.

## BACKGROUND OF THE INVENTION

### 1. Field Of The Invention

This invention relates to computer systems and, more particularly, to methods and apparatus for controlling the output current produced by charge pumps used for erasing flash electrically-erasable programmable read only memory (flash EEPROM) arrays.

### 2. History Of The Prior Art

There has been a recent trend toward lowering the power requirements of portable computers. In order to reduce power consumption, much of the integrated circuitry used in personal computers is being redesigned to run at lower voltage levels. The circuitry and components used in portable computers are being designed to operate at voltage levels such as five volts and 3.3 volts. This helps a great deal to reduce the power needs of such computers.

Unfortunately, some features desired in portable computers require higher voltages. Recently, flash electrically-erasable programmable read only memory (flash EEPROM memory) has been used to store basic input/output startup (BIOS) processes for personal computers. This flash EEPROM memory may be erased and reprogrammed without being removed from the computer by running a small update program when the BIOS processes are changed. However, erasing and reprogramming flash EEPROM memory requires approximately twelve volts to accomplish effectively, a voltage not available from the lower voltage batteries provided in personal computers.

In other electronic arrangements, charge pump circuits have been used to provide a high voltage from a lower voltage source. However, even though charge pumps have long been available which are capable of providing the voltages necessary for programming and erasing flash EEPROM memory arrays, no arrangement had been devised until recently for utilizing charge pumps integrated with flash EEPROM memory arrays to provide the voltages needed to accomplish erasing and programming of the flash EEPROM memory arrays using those positive source erase techniques which are used when twelve volts is available from an external source.

The primary reason for the failure is the universal perception that insufficient current can be generated using charge pumps to accomplish the erase process. The positive source method of erasing flash EEPROM memories draws a very substantial amount of current. However, recently it was discovered that using specially designed charge pumps sufficient current could be generated to accomplish positive source erase of flash EEPROM memory arrays. A charge pump arrangement for accomplishing positive source erase is disclosed in detail in U.S. patent application Ser. No. 08/119,719, now U.S. Pat. No. 5,414,669 entitled *Method And Apparatus For Programming And Erasing Flash EEPROM Memory Arrays Utilizing A Charge Pump Circuit*, K. Tedrow et al, filed on even date herewith, and assigned to the assignee of the present invention.

One of the problems encountered in providing charge pumps for generating source voltages for flash EEPROM memory arrays occurs because some manufactures desire to

utilize the flash EEPROM arrays in circuitry for which an external power supply is available. This means that the memory array circuitry for providing the source voltage must be capable of utilizing power provided either by its internal charge pumps or by an external source. Typically the current available from an external power source is more than sufficient to erase the memory cells of the array during an erase operation. When provided by an external power source, the amount of current actually available is such that the memory cells are typically moved into a soft breakdown region in which current is dissipated through the source-substrate diode. The current transferred through the source-substrate diode junction is wasted.

However, the current available from the charge pumps is less abundant. There is insufficient current available from charge pumps to erase the memory cells in a time period which is competitive with other forms of memory. For this reason, in order to assure that sufficient current to erase and program the array, it is necessary to assure that current is appropriately utilized so that the dissipation of large amounts of current through the source/substrate diode junction does not occur.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an arrangement for controlling the current provided by a charge pump to a flash EEPROM memory array during erasing of the memory cells without loss of erase performance.

It is another object of the present invention to provide an arrangement for providing current limiting of the current when provided by a charge pump and for eliminating current limiting of the current when provided by an external source of high voltage for erasing flash EEPROM memory arrays.

These and other objects of the present invention are realized in an integrated circuit arrangement which provides an arrangement by which the source of voltage for erasing the flash EEPROM memory array is detected and, if the source is a charge pump, the current provided is held to a constant lower value while, if the source is an external high voltage source, then the current is allowed to flow freely without regulation. In this manner, the circuitry is adapted to function with either internal or external power sources without paying a performance penalty for either type of operation.

These and other objects and features of the invention will be better understood by reference to the detailed description which follows taken together with the drawings in which like elements are referred to by like designations throughout the several views.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a computer system which may utilize the present invention.

FIG. 2 is a block diagram of a circuit for providing programming and erase voltages for flash EEPROM memory arrays from charge pumps.

FIG. 3 is a block diagram of a multiplexing arrangement for utilizing both pump current and external current for erasing flash EEPROM memory arrays.

FIG. 4 is a block diagram of a charge pump which may be used in the circuit of FIG. 2 to provide voltages and currents sufficient for positive source erase techniques.

FIG. 5 is a diagram of a first circuit in accordance with the

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present invention for controlling the output current of a charge pump such as that illustrated in FIG. 4.

FIG. 6 is a block diagram of a second circuit in accordance with the present invention for controlling the output current of a charge pump such as that illustrated in FIG. 4.

FIG. 7 is a flow chart illustrating a method of practicing the present invention.

#### NOTATION AND NOMENCLATURE

Some portions of the detailed descriptions which follow are presented in terms of symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. The operations are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Further, the manipulations performed are often referred to in terms, such as adding or comparing, which are commonly associated with mental operations performed by a human operator. No such capability of a human operator is necessary or desirable in most cases in any of the operations described herein which form part of the present invention; the operations are machine operations. Useful machines for performing the operations of the present invention include general purpose digital computers or other similar devices. In all cases the distinction between the method operations in operating a computer and the method of computation itself should be borne in mind. The present invention relates to apparatus and to a method for operating a computer in processing electrical or other (e.g. mechanical, chemical) physical signals to generate other desired physical signals.

#### DETAILED DESCRIPTION

Referring now to FIG. 1, there is illustrated a computer system 10. The system 10 includes a central processor 11 which carries out the various instructions provided to the computer 10 for its operations. The central processor 11 is joined to a bus 12 adapted to carry information to various components of the system 10. Joined to the bus 12 is main memory 13 which is typically constructed of dynamic random access memory arranged in a manner well known to those skilled in the prior art to store information during a period in which power is provided to the system 10. Also joined to the bus 12 is read only memory 14 which may include various memory devices well known to those skilled in the art each of which is adapted to retain a particular memory condition in the absence of power to the system 10. The read only memory 14 typically stores various basic functions used by the processor 11 such as basic input/output processes and startup processes typically referred to as BIOS processes. Such memory 14 may be constructed of flash EEPROM memory cells adapted to be modified as various ones of the BIOS processes used by a particular computer are changed. If the memory 14 is constructed of flash EEPROM memory cells, it may be modified by running an

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update process on the computer itself to reprogram the values stored in the memory 14. Typically, such flash EEPROM memory will include circuitry for programming and erasing the memory array.

Also connected to the bus 12 are various peripheral components such as long term memory 16 and circuitry such as a frame buffer 17 to which data may be written which is to be transferred to an output device such as a monitor 18 for display. The construction and operation of long term memory 16 (typically electro-mechanical hard disk drives) is well known to those skilled in the art. However, rather than the typical electromechanical hard disk drive, a flash EEPROM memory array may be used as the long term memory 16. Such flash EEPROM memory arrays are programmed and erased through techniques which utilize voltages greater than those typically available to the integrated circuits of more advanced portable computers. Such flash EEPROM memory arrays typically include circuitry for programming and erasing the memory array. Consequently, in accordance with the present invention, such long term memory arrays as well as memory 14 may provide circuitry for generating high voltages from the lower voltages available from the batteries typically utilized with such computers.

A flash EEPROM memory array is made up of memory cells which include floating gate field effect transistor devices. Such memory transistors may be programmed to change the charge stored on the floating gate, and the condition of the transistors (programmed or erased) may be detected by interrogating the cells. The conventional method of erasing an array of flash EEPROM memory cells (called positive source erase) erases all of the cells together (or at least some large block thereof). Typically, this requires the application of twelve volts to the source terminals of all of the memory cells, the grounding of the gate terminals, and the floating of the drain terminals. The programming of memory cells is typically accomplished a word at a time but conventionally requires that the drain of selected cells be placed at six or seven volts, the gate at eleven or twelve volts, and that the source be grounded.

Although it has been typical to provide charge pumps to generate higher voltages when only lower voltages are available, charge pumps which are associated internally with flash EEPROM memory arrays have not been used for erasing and programming flash EEPROM memory arrays using conventional positive source erase techniques. Although such charge pumps are able to raise the voltage to an appropriate level, prior art charge pumps were not felt to provide sufficient current to effectively erase and program flash EEPROM memory when erased in the conventional positive source manner.

An N type flash EEPROM memory cell has a source region which is an N doped region surrounded by a P doped substrate. The P doped substrate is grounded so that a diode junction is formed between the source and the substrate. When twelve volts is placed at the source terminal in the normal positive source erase process where current is furnished from an external source, the diode junction between the source and substrate is biased into the soft breakdown region so that substantial source current flows. Initially this breakdown current is very large, and it may in fact be destructive. Because of this substantial source current when the erase process is conducted using positive source erase with an external power source, the source of the erase voltage must be able to furnish a substantial amount of current when erase was accomplished in this conventional manner. It was not believed by those skilled in the art that

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a sufficient amount of current could be furnished by a charge pump.

FIG. 2 is a block diagram which illustrates an integrated circuit 20 including a flash EEPROM memory array 26 and circuitry for programming and erasing the flash EEPROM memory array 26 utilizing positive source erase techniques and charge pump circuitry. This circuit 20 includes a source of voltage 21 such as a low powered battery capable of furnishing five volts. Voltage from the source 21 is provided to a pair of charge pump circuits 22 and 23. The charge pump circuit 22 is devised to provide a pumped output voltage of approximately twelve volts while the charge pump circuit 23 is devised to produce a pumped output voltage of approximately nine volts.

Voltage from the charge pump 22 is furnished to a set of wordline switches and decoders 24 which, in a manner well known to those skilled in the art, provide voltages at the gate terminals of flash EEPROM memory transistor devices 28 (only one transistor device 28 is illustrated in FIG. 2). Voltage from the pump 22 is also furnished to a set of source switches and decoders 25 which, in a manner well known to those skilled in the art, provide voltages at the source terminals of flash EEPROM memory transistor devices 28. The voltage furnished by the pump 23 is furnished to a set of bitline switches and decoders 27 which, in a manner well known to those skilled in the art, provide voltages at the drain terminals of flash EEPROM memory transistor devices 28. Each of the sets of switches and decoders 24, 25, and 27 is controlled by signals from a control circuit 29 to provide appropriate voltages at erase and programming to accomplish those results. In one embodiment, the control circuit 29 is a microprocessor designed to provide control of all of the operations of the memory array 26 including reading, programming, and erasing among other things. The use of such a control circuit is described in U.S. patent application Ser. No. 08/086,186, entitled *Flash Memory Array System and Method*, M. Fandrich et al, filed Jun. 30, 1993, and assigned to the assignee of the present invention.

At the lower right corner of FIG. 2 is shown a table which includes the voltages which are typically applied to the various terminals of the memory cells during the program and erase operations using positive source erase techniques. As may be seen, the erasing of the memory device 28 requires that a positive twelve volts be applied to the source terminal of the device 28, ground be applied to the gate terminal, and the drain be floated.

A new voltage pump circuit has been devised which is capable of providing the high voltages and currents which are required to program and erase flash EEPROM memory arrays. U.S. patent application Ser. No. 08/119,427, entitled *Method and Apparatus for A Bootstrap Voltage Pump*, K. Tedrow et al, filed on even date herewith, and assigned to the assignee of the present invention. Such a voltage pump circuit is described in detail hereinafter.

Although the circuit of FIG. 2 allows the use of internal charge pumps to generate voltages for programming and erasing a flash EEPROM memory array, it does not allow the use of an external source of power. FIG. 3 is a block diagram illustrating a circuit arrangement 30 designed in accordance with the present invention which allows switching between an external source and internal charge pumps in order to provide source voltage to operate a flash EEPROM memory array. The arrangement 30 includes a terminal 31 which receives voltage from a source of external voltage. The source of voltage connected to the terminal 31 may be either a twelve volt source capable of furnishing whatever current

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is necessary for programming and erasing a flash EEPROM memory array. Alternatively, the source of voltage connected to the terminal 31 may be a source of a lower voltage such as five volts which must be used to generate a higher voltage within the circuit arrangement 30. The arrangement 30 also includes a voltage pump circuit 32 designed in accordance with the principles described in the copending patent application to generate from an external voltage of five volts an internal voltage of approximately twelve volts with a current sufficient to erase and program flash EEPROM memory arrays.

Either of the voltages available at the terminal 31 or the voltage pump circuit 32 may be provided to an output terminal designated Vppl (internal high voltage) in the figure depending on the availability of the external high voltage source at the terminal 31. If the high voltage external source is available to the computer (or other) system at the terminal 31, then a first switch 34 is closed to connect the source at the terminal 31 to the output terminal Vppl. Simultaneously, a pair of switches 35 and 36 are each opened to disconnect the voltage pump circuit 32 from the output terminal Vppl. If the source of high voltage is not available, then the switch 34 is opened while the switches 35 and 36 are closed to connect the voltage pump circuit 32 to the output terminal Vppl and to the input terminal 31 at which the lower voltage is available.

In order to test the presence of the high voltage at the terminal 31, a test circuit 37 is provided. The circuit 37 is a voltage level detector which monitors the value of the voltage available at the terminal 31 and controls the closure of the switches 34, 35 and 36 which connect the different sources to the output terminal Vppl. The circuit 37 may be designed in a manner well known to those skilled in the art to produce a voltage level detector. For example, one circuit which may be utilized for this purpose is described in detail in U.S. patent application Ser. No. 08/003,618, entitled *Circuitry For Power Supply Voltage Detection and System Lockout For a Nonvolatile Memory*, M. Landgraf, filed Jan. 13, 1993, and assigned to the assignee of the present invention. If the voltage is at the high level, then the circuit 37 causes a controller circuit 38 to operate the switches in the manner discussed in order to provide the correct voltage from the terminal 31 at the output terminal Vppl. If on the other hand, the voltage at the terminal 31 is the lower level (e.g., five volts), then the circuit 37 provides signals to cause the controller 38 to operate the switches 34, 35, and 36 to connect the output of the voltage pump source 32 to the output terminal Vppl.

If the controller circuit 38 is an integrated microprocessor as described in the copending application *Flash Memory Array And Method*, it may be programmed to respond to particular control signals to provide signals to close particular switching devices such as the switches 34, 35, and 36 used in the circuit arrangement 31. It should be noted that it is not necessary to include a device as powerful as the microprocessor of the preferred embodiment in order to response to a signal from the circuit 37 and operate the switches 34, 35, and 36 in the manner described above; any number of other controlling circuits will occur to those skilled in the art to accomplish this purpose.

FIG. 4 illustrates a bootstrap pump arrangement 40 as described in the aforementioned copending patent application which may be utilized to provide the high voltages and currents required for erasing and programming flash EEPROM memory arrays in accordance with this invention. As is shown in FIG. 4, the pump 40 includes a number of stages of N type field effect transistor devices 41, 42, 43, and

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44 each having drain and source terminals connected in series between a source of voltage  $V_{cc}$  and an output terminal  $V_{out}$ . Input clock signals are furnished to the circuit 40 from a source of clock signals 49 via capacitors 46, 51, and 48. A second set of input clock signals are furnished from a source of clock signals 45 by capacitors 50, 47, and 52. Each stage of the circuit 40 includes an N channel field effect transistor device 53, 54, or 55 providing a path between source and drain terminals to the gate terminal of the associated device 41, 42, or 43 of that stage.

The two phases of input clock pulses (phase 1 and phase 2) produced by the sources 45 and 49 are applied in a unique manner in order to allow the operation of the circuit 40 to produce the desired output voltages and currents.

The details of the construction and operation of the charge pump circuit illustrated in FIG. 4 are provided in the copending patent application referred to above entitled *Method and Apparatus for A Bootstrap Voltage Pump*. The essence of the operation of the charge pump is as follows. When the phase 1 clock goes high, the device 41 turns on; and current provided by the source  $V_{cc}$  charges the capacitor 46. When the phase 1 pulse goes low the device 41 switches off. Then the phase 2 clock pulse turns on the device 42; and the capacitor 46 provides stored charge and charge due to the phase 2 pulse to the capacitor 47. The device 42 switches off when the phase 2 pulse goes low. When the phase 1 pulse again goes high, the source  $V_{cc}$  again charges the capacitor 46. Simultaneously, the device 43 goes on and the capacitor 47 provides stored charge as well as the pulse from the phase 1 clock to charge a capacitor 48. When the phase 1 clock goes low, the device 43 turns off.

Ultimately, the charging of the capacitor 48 and the positive swing of the phase 2 clock pulse raise the voltage level on the capacitor 48 sufficiently above the level  $V_{out}$  to cause the conduction of the switching device 44. When the phase 2 clock goes high, the output device 44 turns on and furnishes a pumped voltage at  $V_{out}$ . A major advantage of the charge pump circuit illustrated is that in operation none of the stages except the last stage operates in a range in which it exhibits a  $V_t$  drop. Thus, the charge pump provides almost twice the current to the output terminal as do prior art charge pump circuits.

Thus, the charge pump provides the desired output voltage while furnishing a high level of current necessary to erase and program flash EEPROM memory arrays. The three stage pump circuit 40 illustrated in FIG. 4 furnishes approximately N (where N is the number of stages) plus one times the voltage of the source  $V_{cc}$  at the output terminal less the  $V_t$  drop of the device 44. For example, with  $V_{cc}$  equal to 4.4 volts, an output voltage of 17.1 volts is furnished at the output of the pump circuit 40. Thus, as may be seen, the arrangement of FIG. 4 provides a reliable charge pump circuit capable of producing high levels of current.

It should be noted that the smaller charge pump 23 of FIG. 2 required to furnish the voltage used at the drain terminals of the flash EEPROM memory cells during programming of the array may be provided by charge pumps similar to the pump described in FIG. 4 with the exception that fewer stages are used. For example, a charge pump having only two stages is capable of providing a 9.5 volt output which may be used at the drain terminals of the memory cells during programming. Because the charge pump circuits described do not provide an overabundance of current for programming and erasing the memory array, an arrangement has been devised in accordance with the present invention. FIG. 5 illustrates a first circuit by which current provided by

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a charge pump such as that illustrated in FIG. 4 may be limited to a constant lower value while current provided by an external source which may furnish essentially unlimited amounts of current is not limited. By this arrangement the peak current transferred by the source/substrate diode is kept to a much lower value when current is furnished by a charge pump than when current is furnished by an external power source. The circuit of FIG. 5 includes a first P type field effect transistor device 61 having its source terminal connected to the source of the voltage  $V_{pp}$  to be applied to the source terminals of the memory cells of the array. The gate of the device 61 is connected to receive an input control signal which may be furnished by the voltage detector circuit 37 illustrated in FIG. 3 which detects whether the array is receiving voltage from an external source or pumping voltage for erasing the array. The drain terminal of the device 61 is joined to the source terminal of a second P type field effect transistor device 62. The device 62 has its gate and drain terminals connected together and to a large (e.g., one-half megohms) resistor 64. The resistor 64 is in turn connected to ground. The gate terminal of a third P type field effect transistor device 63 is joined to the gate and drain of the device 62 while the source terminal of the device 63 is connected to the source which supplies the erase voltage  $V_{pp}$  to the source terminals of the flash EEPROM memory cells. The drain of the device 63 is then joined to the array to allow the voltage  $V_{pp}$  to be applied to the source terminals of the flash EEPROM memory cells during erase.

FIG. 7 is a flow chart which describes a method of operation of the invention shown in FIG. 5. In the circuit of FIG. 5, when ground (a zero valued signal) is furnished from the detector circuit 37 to signify that an external power supply of five volts is being furnished and is pumped to provide the voltage  $V_{pp}$ , the device 61 switches on and applies a voltage of  $V_{pp}$  at the source terminal of the device 62. The device 62 has its drain and gate terminals connected to ground through the resistor 64. Consequently, the device 62 turns on and operates in its saturation region causing current to flow from the source  $V_{pp}$  through the device 61, the device 62, and the resistor 64 to ground. Since the resistor 64 is a large value, it controls the current through the device 62 to be a constant limited value. The voltage at the gate and drain of the P device 62 is applied at the gate of the P device 63 turning on the device 63 and mirroring the current through the device 62. This current is furnished to the source terminals of the flash cells being erased. This current is limited by choice of device size and the resistance value to a value such that the flash cells receive sufficient current to erase without receiving a peak current capable of pushing the cells so far into the soft breakdown region that there is insufficient switching current to accomplish the positive source erase.

When a one valued signal is furnished from the detector circuit 37 to signify that an external power supply of twelve volts is being furnished to provide the voltage  $V_{pp}$ , the device 61 turns off. Consequently, no current flows through the device 62, and the gate terminal of the device 63 is held at ground through the resistor 64. This places the device 63 in an operating region in which all of the current available from the external source of the voltage  $V_{pp}$  may be furnished to the flash EEPROM memory cells and they may be erased in the conventional manner by transition into the soft breakdown region. In this case, the amount of current which may be transferred is limited by the sizing of the P device 63.

FIG. 6 illustrates a second circuit which performs the same function of allowing all of the current provided by an external source to be transferred to the source terminals of

a flash EEPROM memory array while limiting the current available from an internal charge pump like that described above to a lesser and constant value. The circuit of FIG. 6 includes a first P type field effect transistor device 66 having its source terminal connected to the source of the voltage  $V_{pp}$  to be applied to the source terminals of the memory cells of the array. The device 66 has its gate and drain terminals connected to the source terminal of a second P type field effect transistor device 67 and to the drain of an N type field effect transistor device 65. The N device 65 has its source terminal connected to ground through a large resistor 69. The gate of the N device 65 is connected to receive a reference voltage which remains constant throughout operation of the circuit of FIG. 6. The gate of the device 67 is connected to receive the input control signal which may be at a zero or a twelve volt level and may be furnished by the voltage detector circuit 37 illustrated in FIG. 3 which detects whether the array is receiving voltage from an external source or pumping voltage for erasing the array. The drain terminal of the device 67 is joined to the gate terminal of a third P type field effect transistor device 68. The device 68 has its source and drain terminals connected in series in a path between the source of the voltage  $V_{pp}$  and the source terminals of the array.

Also connected to receive the control signals provided by the voltage detector circuit 37 which detects whether the array is receiving voltage from an external source or pumping voltage for erasing the array is a N type field effect transistor device 70. The device 70 receives the control signals at its gate terminal while its source terminal is connected to ground and its drain terminal to the gate terminal of the device 68.

In operation (which is illustrated in the flow chart of FIG. 7), the detector provides a zero valued signal when the source voltage  $V_{pp}$  is provided by the internal charge pumps. This value is applied to the gate of the N device 70 and the gate of the P device 67. The zero value disables the N device 70. The device 66 is so biased that it turns on and conducts in the saturated range. This provides a voltage value at the drain of the device 67 which is somewhat less than the voltage  $V_{pp}$ . Since the N device 65 has a constant reference voltage at its gate terminal, it is on constantly and transfers a current controlled by the resistor 69. The large value of the resistor 69 controls the current through the device 66 to remain constant.

The voltage  $V_{pp}$  at the source of the device 66 less the  $V_t$  drop across the device 66 is also applied at the source of the device 67. The voltages at the source and gate of the device 67 turn it on in a region of operation in which it exhibits essentially no  $V_t$  drop causing the voltage  $V_{pp}$  less the  $V_t$  drop of the device 66 to be applied at the gate of the device 68. With the gate and source terminals of each of the devices 66 and 68 being at the same values, the device 68 conducts mirroring the constant current through the device 66. In one embodiment, the device 68 has a channel width which is twenty-five times that of the device 66 so that it transfers twenty-five times the constant current transferred by the device 66, a current which remains constant no matter what current is furnished at the source of the voltage  $V_{pp}$ . Thus, when the detector 37 signals that the charge pump is providing the source voltage, the current provided is limited to a constant value. This value is selected to be such that the peak current applied to the memory devices of the flash EEPROM array moves those devices into a portion the soft breakdown region so that too much current is not dissipated by transfer through the diode action of the source to substrate junction.

On the other hand, when the detector determines that the external source is providing voltage for erasing the array, a one valued or high signal of twelve volts is provided at the control terminal. This signal disables the device 67 and enables the N type device 70. The device 70 conducts and ground is applied at the gate terminal of the device 68. Ground at the gate of the device 68 causes the device 68 to operate in the region in which it transfers current limited only by the size of the device 68 to the source terminals of the memory cells of the flash EEPROM array.

Although the present invention has been described in terms of a preferred embodiment, it will be appreciated that various modifications and alterations might be made by those skilled in the art without departing from the spirit and scope of the invention. The invention should therefore be measured in terms of the claims which follow.

What is claimed is:

1. A method for controlling the current furnished to source terminals of floating gate field effect transistors of a flash EEPROM memory array comprising the steps of:

detecting whether a voltage furnished to source terminals of floating gate field effect transistors is derived from an external voltage source or from a charge pump,

controlling the current furnished to the source terminals of floating gate field effect transistors to be a constant current of a limited value if the voltage furnished to source terminals of floating gate field effect transistors is derived from a charge pump, and

allowing the current furnished to source terminals of floating gate field effect transistors to vary if the voltage furnished to source terminals of floating gate field effect transistors is derived from an external source.

2. A method for controlling the current furnished to source terminals of floating gate field effect transistors of a flash EEPROM memory array as claimed in claim 1 in which the step of controlling the current furnished to the source terminals of floating gate field effect transistors to be a constant current of a limited value if the voltage furnished to source terminals of floating gate field effect transistors is derived from a charge pump comprising the steps of: providing a constant current, and

mirroring the constant current to source terminals of floating gate field effect transistors if the voltage furnished to source terminals of floating gate field effect transistors is derived from a charge pump.

3. A method for providing power to a plurality of floating gate field effect transistor devices during an erase operation, said floating gate field effect transistor devices having a gate terminal, a drain terminal and a source terminal, said method comprising the steps of:

providing a charge pump circuit;

generating, from said charge pump circuit, a positive voltage for source terminals of said floating gate field effect transistor devices during an erase operation;

receiving power at a first terminal from an external source; supplying power for said erase operation from either said first terminal or said charge pump circuit to a second terminal; and

regulating, at said second terminal, said power to a first constant current when said power is supplied from said charge pump circuit, and not regulating current when said power is supplied from said external source, said first constant current being insufficient to bias a floating gate field effect transistor devices in a soft breakdown region during an erase operation.

## 11

4. The method as set forth in claim 3, wherein the step of regulating said power to a first constant current when said power is supplied from said charge pump circuit, and not regulating current when said power is supplied from said external source comprises the steps of:

coupling a constant current source, including a first transistor, to said second terminal;

biasing said first transistor to activate said constant current source when said power is selectively supplied from said charge pump circuit;

biasing said first transistor to inactivate said constant

## 12

current source when said power is selectively supplied from said external source; and

coupling a second transistor between said second terminal and said selective source terminals of said floating gate field effect transistor devices during an erase operation; and

biasing said second transistor with said constant current source so as to regulate current to generate said first constant current.

\* \* \* \* \*

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UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,455,794  
DATED : October 3, 1995  
INVENTOR(S) : Javanifard et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4 at line 13 delete "mcmo.ny" and insert --memory--

In column 4 at line 37 delete "ceils" and insert --cells--

In column 5 at line 8 delete "batten" and insert --battery--

In column 5 at line 51 delete "08/119,427," and insert --08/119,423,--

In column 6 at line 37 delete "System" and insert --System--

In column 8 at line 59 delete "carrent" and insert --current--

In column 8 at line 67 delete "externai" and insert --external--

In column 10 at line 58 delete "siad" and insert --said--

In column 10 at line 61 delete "powere" and insert --power--

Signed and Sealed this

Twenty-fifth Day of February, 1997

Attest:



BRUCE LEBMAN

Attesting Officer

Commissioner of Patents and Trademarks





US005519360A

**United States Patent** [19]

Keeth

[11] **Patent Number:** **5,519,360**[45] **Date of Patent:** **May 21, 1996**[54] **RING OSCILLATOR ENABLE CIRCUIT WITH IMMEDIATE SHUTDOWN**[75] **Inventor:** Brent Keeth, Boise, Id.[73] **Assignee:** Micron Technology, Inc., Boise, Id.[21] **Appl. No.:** 506,216[22] **Filed:** Jul. 24, 1995[51] **Int. Cl.<sup>6</sup>** ..... H03B 5/24; H03L 3/00[52] **U.S. Cl.** ..... 331/57; 331/173; 327/534[58] **Field of Search** ..... 331/45, 57, 111; 331/143, 172, 173; 327/534-537[56] **References Cited****U.S. PATENT DOCUMENTS**

3,319,078	5/1967	Dunnet et al.	331/173 X
4,344,003	8/1982	Harmon et al.	331/57 X
4,471,290	9/1984	Yamaguchi	331/57 X
5,023,465	6/1991	Douglas et al.	365/203
5,038,325	8/1991	Douglas et al.	365/189.06
5,039,877	8/1991	Chern	307/296.2
5,126,590	6/1992	Chern	307/296.2
5,182,529	1/1993	Chern	331/57
5,311,476	5/1994	Kajimoto et al.	331/57 X
5,345,186	9/1994	Lesmeister	331/57 X

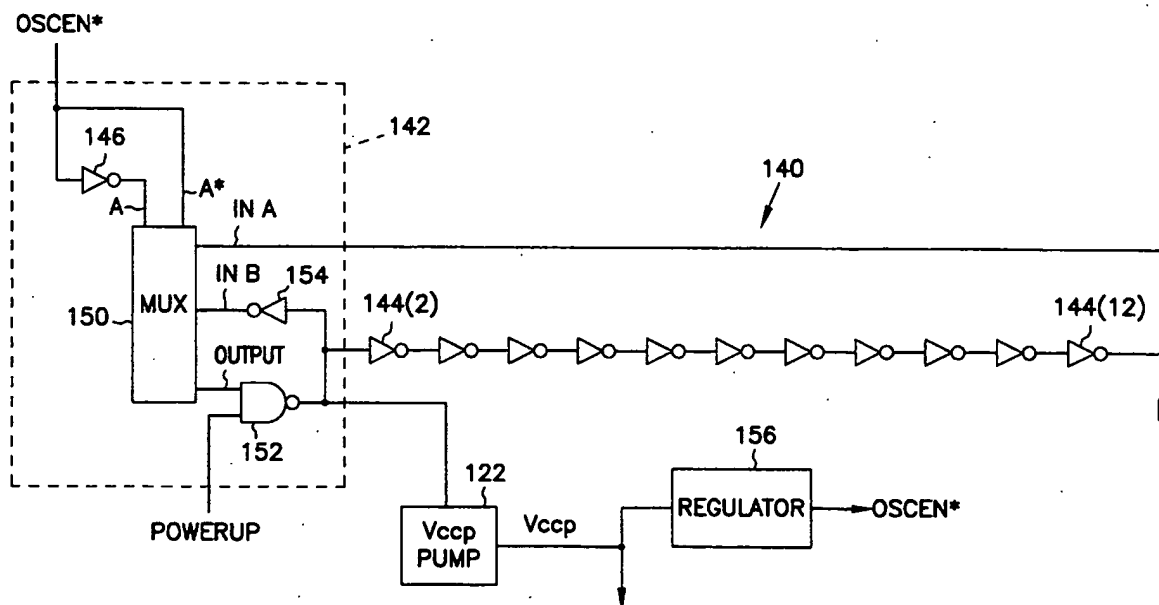
5,355,097	10/1994	Scott et al.	331/173 X
5,396,114	3/1995	Lee et al.	327/535

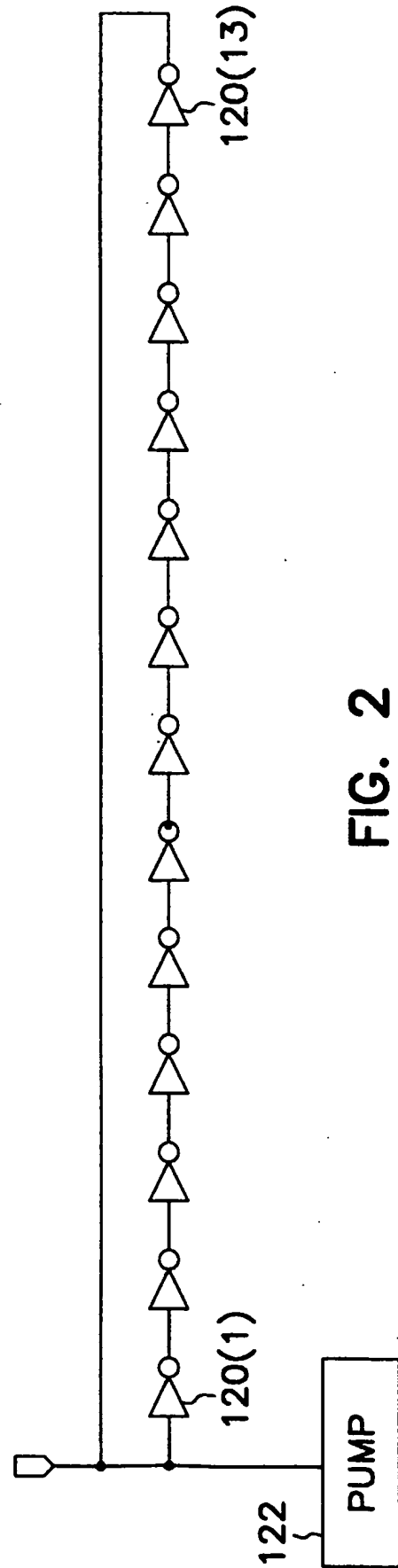
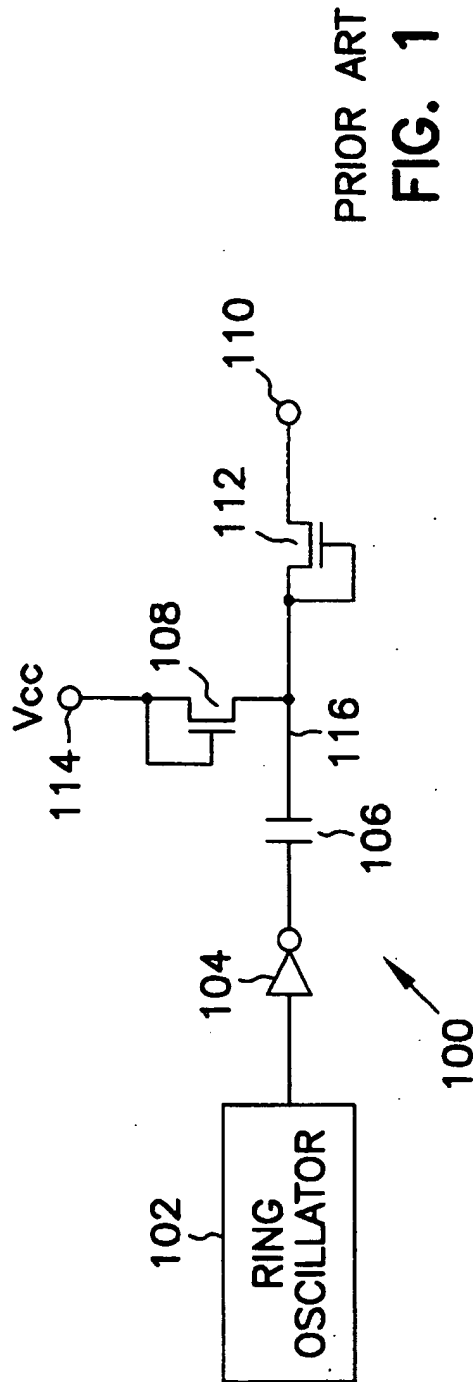
**FOREIGN PATENT DOCUMENTS**

1033013 2/1986 Japan ..... 331/57

*Primary Examiner*—David Mis*Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth[57] **ABSTRACT**

An integrated memory circuit is described which includes a charge pump for producing a pumped voltage and a ring oscillator coupled to the charge pump. The ring oscillator is used to operate the charge pump, such that pump cycles are activated on the edges of the oscillator output. The ring oscillator includes an oscillator enable circuit which is controlled by a regulator to maintain a controlled pump voltage. The oscillator enable circuit immediately shuts the ring oscillator off when the pump voltage reaches a predetermined upper voltage limit so that additional oscillator cycles are eliminated, thereby, reducing the chance of an overshoot in the pump voltage. The oscillator enable circuit turns the oscillator on when the pump voltage decreases to a predetermined lower level.

**11 Claims, 4 Drawing Sheets**



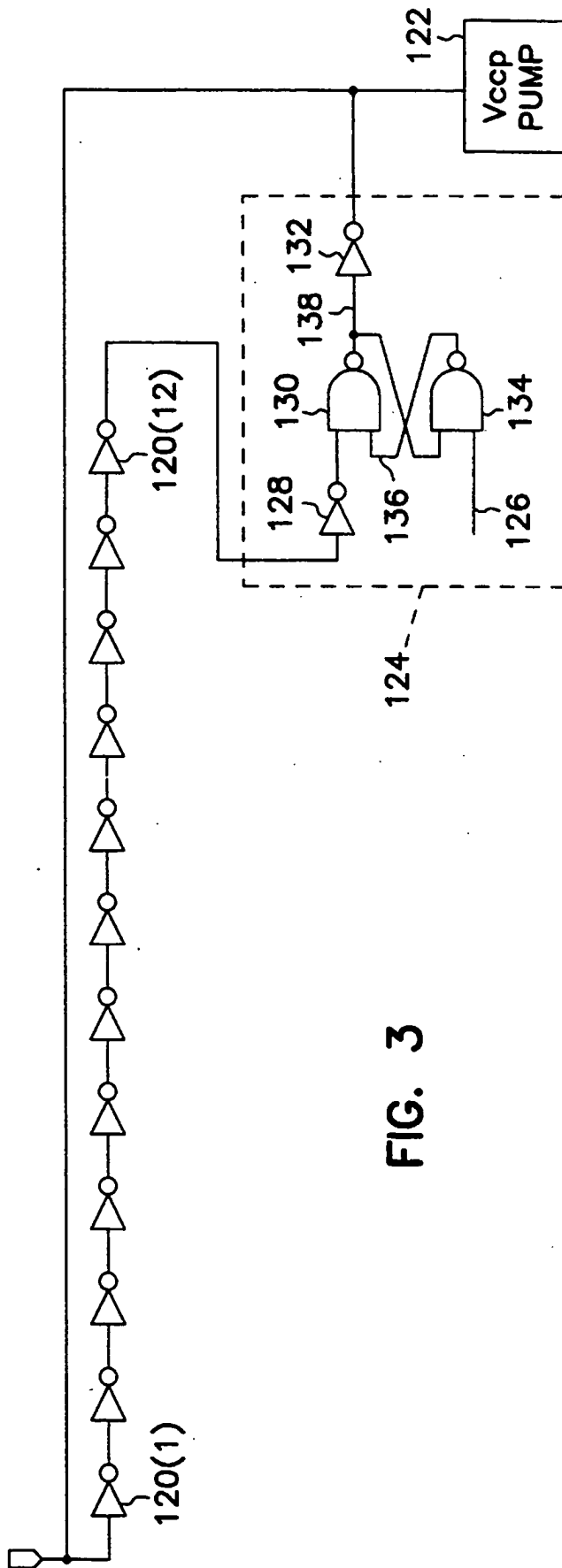


FIG. 3

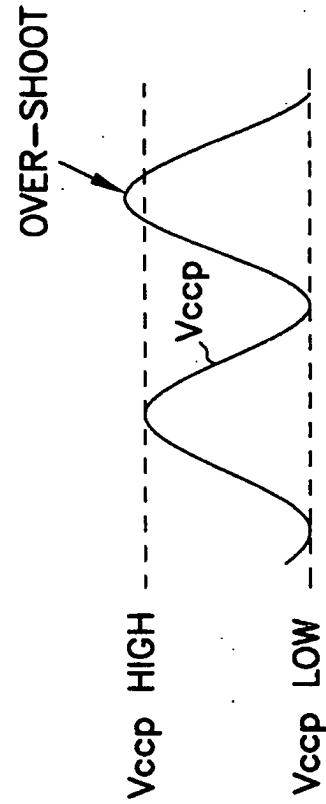


FIG. 4

FIG. 5

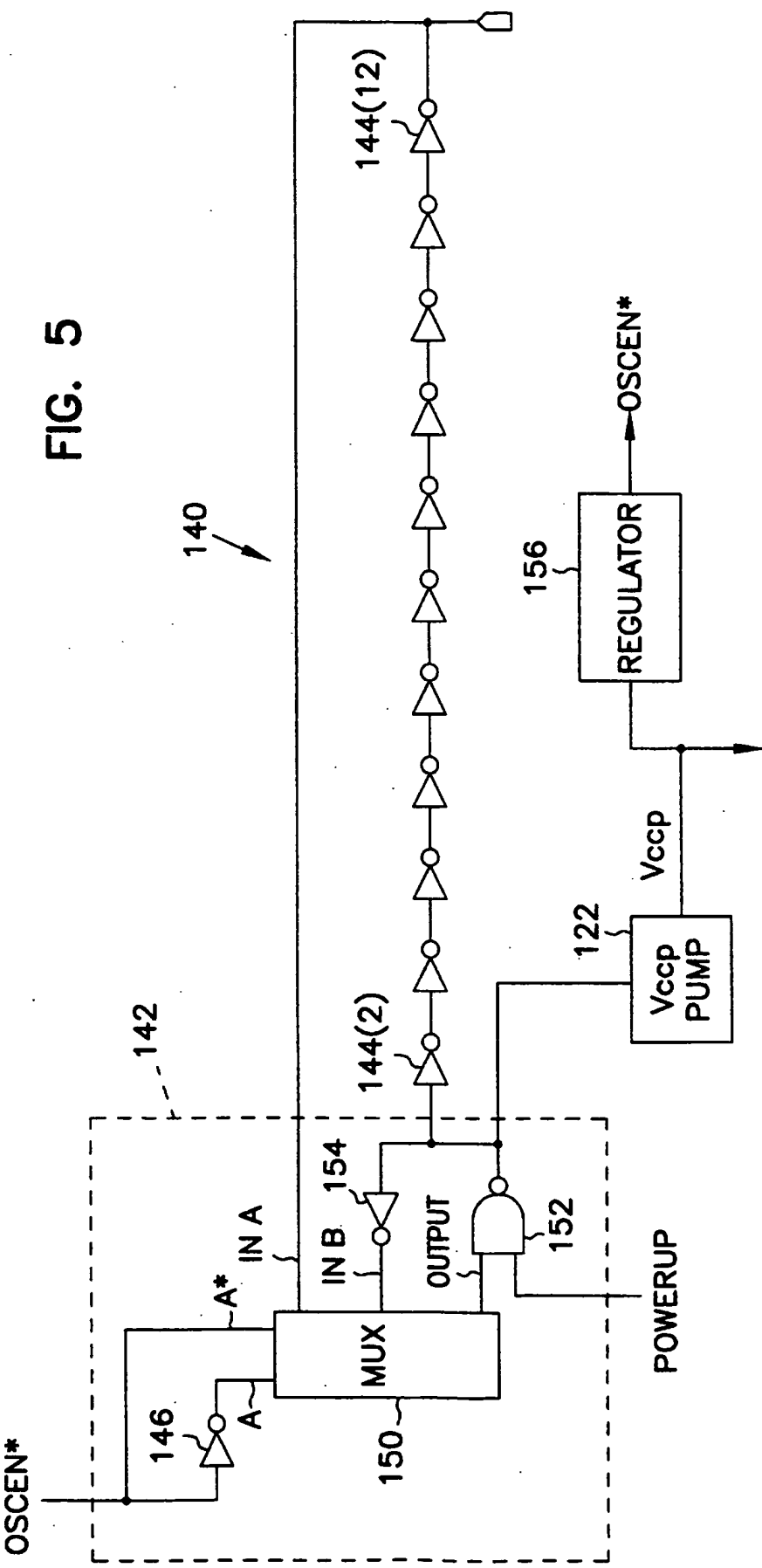
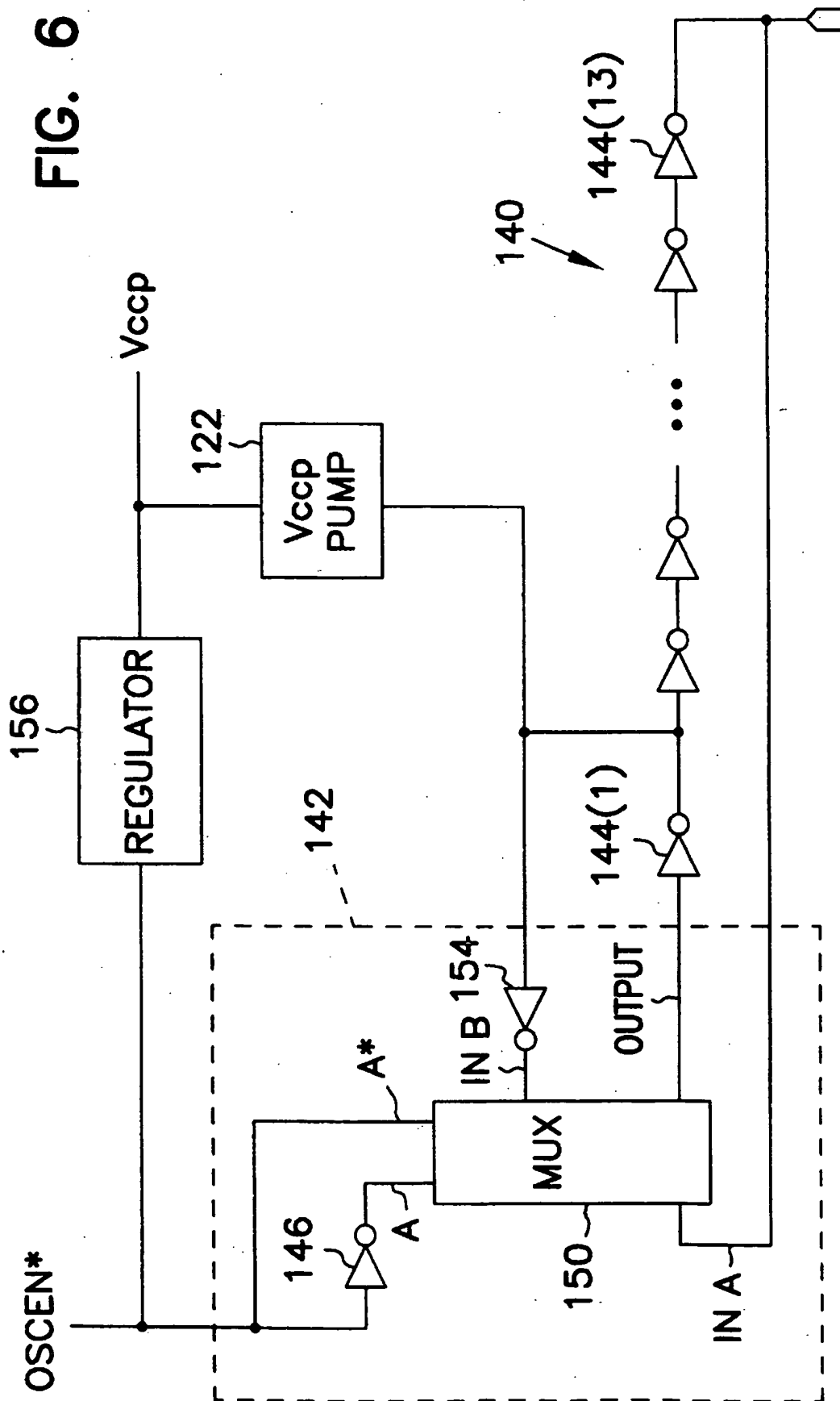


FIG. 6



## RING OSCILLATOR ENABLE CIRCUIT WITH IMMEDIATE SHUTDOWN

### TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuits and in particular the present invention relates to ring oscillator circuits. More particularly, the present invention relates to a ring oscillator enable circuit.

### BACKGROUND OF THE INVENTION

Charge pumps are well known in the art as an on-chip voltage regulator capable of providing a voltage more positive than the most positive external power supply voltage and/or negative voltage in the absence of a negative power supply voltage. The pump voltage is provided by a charge stored on a charge capacitor. The advantages of charge pumps are also well known in the art, for example, such as providing a bias voltage for the substrate of an integrated circuit or n-type and p-type wells, or for providing greater output voltage swings.

Many types of integrated circuit memories require several different power levels for operation. Some of these power levels exceed the available potential range of the external power supplies used to power the circuit. For example, access transistors connected to dynamic memory cells typically use a pumped voltage ( $V_{ccp}$ ) to drive their gates above the most positive power supply voltage. The  $V_{ccp}$  is typically provided by a charge pump and is used to allow a complete charge to be written to the memory cell. If a lower voltage were used as the gate potential, such as the supply voltage  $V_{cc}$ , a threshold voltage ( $V_t$ ) would be lost between the source and drain, such that a full source voltage could not reach the drain.

Most charge pumps provide some type of oscillator circuit. This circuit can be a ring oscillator which provides a square wave or pulse train having voltage swings typically between ground and the most positive external supply voltage,  $V_{cc}$ . The pumped voltage level is partially controlled by the ring oscillator. That is, the pumped charge is generated when the ring oscillator cycles high. The ring oscillator, therefore, has an active half-cycle and an inactive half-cycle. A charge capacitor is typically pre-charged during the inactive half-cycle. The capacitor charge is then pumped to a higher level by charge sharing with another capacitor when the ring oscillator transitions to the active half-cycle. To reduce the amount of inactive time, charge pumps can have more than one phase where each phase operates on either the high or low transition of the ring oscillator.

Typical ring oscillators include an enable circuit which is used in the regulation of the pumped voltage. The enable circuit activates and deactivates the ring oscillator when the pumped voltage exceeds pre-determined upper and lower limits. When the charge capacitor has been discharged to a point where the lower level of  $V_{ccp}$  has been reached, a regulator circuit activates an enable circuit coupled to the ring oscillator and the charge capacitor is re-charged. When the charge on the capacitor reaches the desired upper limit the oscillator is disabled. This process maintains an acceptable level for  $V_{ccp}$ .

A problem occurs when the oscillator fails to turn-off when the enable circuit is triggered. Over-shoot of the charge pump may be experienced when the oscillator completes an additional cycle after the disable signal is received.

This over-shoot makes regulation of the pump voltage difficult and increases the peak to peak ripple experienced in  $V_{ccp}$ .

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a ring oscillator enable circuit which shuts down the ring oscillator immediately to allow for better regulation of  $V_{ccp}$ .

### SUMMARY OF THE INVENTION

The above mentioned problems with ring oscillators and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A ring oscillator enable circuit is described which immediately shuts the ring oscillator off to avoid over-shoot.

In particular, the present invention describes an integrated circuit comprising a ring oscillator having cascaded inverting stages connected in a ring for producing an oscillating output having rising and falling transitions. An enable/disable circuit is coupled to the ring oscillator and has an input signal. The enable/disable circuit is responsive to the input signal for disabling the ring oscillator and prohibiting additional rising and falling transitions. The enable/disable circuit can comprise a feed forward circuit responsive to the input signal, and a feed back circuit responsive to the input signal.

In an alternate embodiment, the oscillating output is provided as the output from one of the plurality of cascaded inverting stages, and a feed forward circuit is comprised of a multiplexer located between the input of the one of the plurality of cascaded inverting stages and an output of a preceding cascaded inverting stage of the ring oscillator. A feed back circuit is comprised of a multiplexer and a feed back inverter connected between the output of the one of the plurality of cascaded inverting stages and the input of the one of the plurality of cascaded inverting stages.

The integrated circuit can include a charge pump circuit coupled to the ring oscillator for producing a pumped voltage, or a voltage regulator circuit for generating the input signal.

In another alternate embodiment a method is provided for controlling a ring oscillator. The method comprises the steps of providing a ring oscillator having cascaded inverting stages formed in a ring for producing an oscillating output having rising and falling transitions, providing an input signal to an enable/disable circuit coupled to the ring oscillator, and disabling the ring oscillator in response to the input signal, such that additional rising and falling transitions are prohibited.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a prior art charge pump;

FIG. 2 is a art ring oscillator;

FIG. 3 is a ring oscillator including an enable circuit;

FIG. 4 is a graph of the  $V_{ccp}$  output from a charge pump using the ring oscillator of FIG. 3;

FIG. 5 is a ring oscillator incorporating the present invention; and

FIG. 6 is an alternate ring oscillator incorporating the present invention.

### DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

A basic single phase charge pump 100 is described with reference to FIG. 1. A ring oscillator 102 provides a square wave oscillating signal having voltage swings between the supply voltage, Vcc, and ground. An inverter 104 may be used to sharpen the edges of the oscillating output signal of the ring oscillator. A capacitor 106 is discharged through the output 110 via diode connected transistor 112. Transistor 108 is coupled to the external power supply voltage, Vcc, at terminal 114. When the ring oscillator 102 produces a voltage close to Vcc, the output of inverter 104 is low and circuit node 116 is approximately at the voltage of the power supply minus a threshold voltage ( $V_{cc}-V_t$ ) as provided by transistor 108. When the ring oscillator transitions to a low voltage, the output of inverter 104 goes high and boosts the charge on capacitor 106. The incremental charge on capacitor 106 is delivered to output 110 through transistor 112. The charge on capacitor 106 is therefore pumped above Vcc to produce Vccp. It is understood that multiple-phase charge pumps can be operated using a single ring oscillator, as known to one skilled in the art. Further, any charge pump design can be used with the present invention and the charge pump described herein is not intended to limit the present invention.

A typical ring oscillator is shown in FIG. 2 and includes an odd number of inverter stages 120(1)–(13) arranged in a serially connecting ring fashion. Thirteen inverter stages are shown in FIG. 2, but the exact number can be any odd number depending upon the delay through each stage and the desired oscillating frequency. The output of each inverter is coupled to the input of the succeeding inverter in the ring. The output of the last inverter 120(13) is coupled to the input of the first inverter 120(1) and forms the oscillating output. The output is coupled to the input of a two phase Vccp charge pump 122. That is, one phase is operated on a rising edge of the ring oscillator output and the other phase is operated on the falling edge.

One of the inverter stages of the ring oscillator of FIG. 2 can be replaced with an enable circuit 124, as shown in FIG. 3. The enable circuit is a pair of cross-coupled NAND gates which form a latch when the ring oscillator is to be disabled. The enable circuit operates as an inverter when the Disable input 126 is low. That is, inverter 128, NAND gate 130 and inverter 132 together act as an inverter when the input 136 of NAND gate 130 is high. To disable the ring oscillator, the Disable input 126 is pulled high. The output of NAND gate 134 will latch low when the output 138 of NAND gate 130 goes high.

The Disable input 126 is controlled by a regulator circuit (not shown) which monitors the Vccp voltage level. If the Vccp voltage reaches a pre-determined Vccp low level, the ring oscillator is enabled to activate the charge pump, see

FIG. 4. If, on the other hand, the Vccp reaches a pre-determined Vccp high level, the ring oscillator is disabled. If the Vccp pump does not turn off when the Disable input 126 goes high, an over-shoot in the Vccp level will occur. As stated above, the variation in the peak to peak ripple of the Vccp level resulting from over-shoot is undesirable.

An over-shoot in the Vccp pump 122 can happen if the Disable input 126 is pulled high shortly after the output of inverter 128 has gone high. For example, if the output from inverter stage 120(12) goes low, the output from the enable circuit 124 goes high. This produces a rising edge and allows one phase of the Vccp pump to charge its pump capacitor. If the Disable input goes high while the output from inverter 120(12) is low, the cross coupled NAND gates 130 and 134 cannot latch node 138 high. The output from inverter 120(12) must go high before NAND gate 134 can latch the output of NAND gate 130 to high state. This allows one low transition to occur on the oscillator output which triggers the other phase of the Vccp charge pump. To eliminate this extra cycle, an enable circuit is provided which stops the ring oscillator independent of the state of the oscillator, see FIG. 5.

A ring oscillator 140 is shown in FIG. 5 which includes an oscillator enable circuit 142 which insures that the output of the ring oscillator shuts down immediately upon notification by a regulator circuit. The ring oscillator is a series of cascading inverters 144(2)–(12). The output of each inverter is coupled to the input of the succeeding inverter in the ring. The output of the last inverter 144(12) is coupled to the oscillator enable circuit 142 which normally acts as an inverter element. The oscillator enable circuit 142 is then coupled to the input of a multiphase Vccp charge pump 122.

The oscillator enable circuit 142 includes an enable input (Oscen\*) which is an inverse logic signal provided by voltage regulator 156. The voltage regulator monitors the Vccp voltage level provided by the Vccp pump 122 and controls the Oscen\* signal as Vccp reaches its predetermined limit levels. The oscillator enable circuit 142 has a feed forward circuit including multiplexer 150 and NAND gate 152, and a feed back circuit including inverter 154 and multiplexer 150. Inverter 146 is provided to produce the complement, or inverse, of the Oscen\* input signal. Both Oscen\* and its complement are used to control multiplexer 150.

During normal oscillator operation, the Oscen\* input is low (control input A\*). The output of inverter 146 (control input A) is therefore high and multiplexer 150 couples the output of inverter stage 144(12) (Input A) to NAND gate 152 via the multiplexer output. The Powerup input to NAND gate 152 is normally high, as explained below. NAND gate 152, thereby, operates as an inverter stage in the ring oscillator.

The Oscen\* input is pulled high by regulator 156 to turn the ring oscillator 140 off. When Oscen\* goes high the output of inverter 146 goes low and multiplexer 150 couples the output of inverter 154 (Input B) to NAND gate 152. The NAND gate is, therefore, latched at its current state such that the oscillator is immediately disabled and cannot continue to cycle. It will be understood that the multiplexer 150 can be replaced with logic circuitry which responds to the Oscen\* signal to selectively couple either the feedback circuit or the feed forward circuit to the next inverter stage.

During a power-up sequence for the integrated circuit, the Powerup input to NAND gate 152 is held low so that the NAND gate output is latched high until the integrated circuit has been sufficiently powered-up. It will be recognized that

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NAND gate 152 can be replaced with a NOR gate having an increase logic power-up input, or an inverter if the power-up control is not desired. For example, FIG. 6 illustrates a ring oscillator 140 which has thirteen inverter stages 144(1)-(13). The oscillator enable circuit 142 uses the output of inverter stage 144(1) as the input for the feed back circuit, as defined by inverter 154 and multiplexer 150. The feed forward circuit, multiplexer 150, receives the output from inverter 144(13) and feeds the signal to inverter 144(1) when *Oscen\** is low. As explained above, when *Oscen\** goes high, inverter 144(1) is latched at its current state using the feed back circuit to disable the ring oscillator and prohibit further oscillations.

The present invention has been described in a ring oscillator having a series of inverting stages with the oscillator enable circuit 142 being coupled to the first inverting stage. It will be understood that any odd number of inverting stages can be used and that the oscillator enable circuit 142 can be located between any of the inverting stages. Although inverters are preferred as inverting stages in the ring oscillator, it will be understood by those skilled in the art that any inverting-type circuit can be used, including but not limited to NAND and NOR gates. Further, the *Vccp* pump coupled to the ring oscillator can be any design and is not limited to a multi-phase charge pump.

#### Conclusion

A ring oscillator has been described for use with a charge pump circuit. The ring oscillator includes an oscillator enable circuit which is controlled by a regulator to maintain a controlled pump voltage. The oscillator enable circuit is not dependent upon the state of the ring oscillator and can immediately disable the oscillator. Additional oscillator cycles are eliminated, thereby, reducing the chance of an over-shoot in the pump voltage. When the pump voltage decreases to a predetermined lower level, the regulator activates the ring oscillator enable circuit. When activated, the enable circuit feed forward circuit can operate as an inverter stage in the ring oscillator. When the pump voltage increases to a predetermined upper level, the regulator de-activates the enable circuit. When de-activated, a feed back circuit latches an inverter stage of the ring oscillator.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, although the oscillator enable circuit has been described using a multiplexer to selectively couple either a feed back circuit or a feed forward circuit to the ring oscillator, a logic circuit could be used to perform the selective coupling operation. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated circuit comprising:

a ring oscillator having a plurality of cascaded inverting stages connected in a ring for producing an oscillating output having rising and falling transitions; and

an enable/disable circuit coupled to the ring oscillator and having an input signal, the enable/disable circuit being

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responsive to the input signal for disabling the ring oscillator and prohibiting additional rising and falling transitions.

2. The integrated circuit of claim 1 wherein the enable/disable circuit comprises:

a feed forward circuit responsive to the input signal; and  
a feed back circuit responsive to the input signal.

3. The integrated circuit of claim 2 wherein:

the oscillating output is provided as the output from one of the plurality of cascaded inverting stages;

the feed forward circuit is comprised of a multiplexer located between the input of the one of the plurality of cascaded inverting stages and an output of a preceding cascaded inverting stage of the ring oscillator; and

the feed back circuit is comprised of the multiplexer and a feed back inverter connected between the output of the one of the plurality of cascaded inverting stages and the input of the one of the plurality of cascaded inverting stages.

4. The integrated circuit of claim 1 further including a charge pump circuit coupled to the ring oscillator for producing a pumped voltage.

5. The integrated circuit of claim 1 further including a voltage regulator circuit for generating the input signal.

6. The integrated circuit of claim 1 wherein the plurality of inverting stages are comprised of a plurality of inverters.

7. An integrated circuit comprising:

a ring oscillator having a plurality of cascaded inverting stages formed in a ring for producing an oscillating output having rising and falling transitions;

one of the plurality of inverting stages being formed as an enable/disable circuit, having an input signal, and being responsive to the input signal for disabling the ring oscillator and prohibiting additional rising and falling transitions;

the enable/disable circuit comprising a feed forward circuit connected to an output of a preceding inverting stage and an input of a succeeding inverting stage, and a feed back circuit;

a charge pump connected to the ring oscillator; and

a voltage regulator coupled to the charge pump for generating the input signal.

8. The integrated circuit of claim 7 wherein:

the feed forward circuit comprises a multiplexer connected to one input of a NAND gate;

the multiplexer being connected to the output of the preceding inverting stage and the NAND gate being connected to the input of the succeeding inverting stage; and

the feed back circuit comprising an inverter connected to the input of the succeeding inverting stage and coupled to the multiplexer.

9. The integrated circuit of claim 7 wherein:

the feed forward circuit comprises a multiplexer connected to one input of a NOR gate;

the multiplexer being connected to the output of the preceding inverting stage and the NOR gate being connected to the input of the succeeding inverting stage; and

the feed back circuit comprising an inverter connected to the input of the succeeding inverting stage and coupled to the multiplexer.

10. The integrated circuit of claim 7 wherein:



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the feed forward circuit comprises a multiplexer connected to an input of an inverter gate;  
the multiplexer being connected to the output of the preceding inverting stage and the inverter gate being connected to the input of the succeeding inverting stage; and  
the feed back circuit comprising an inverter connected to the input of the succeeding inverting stage and coupled to the multiplexer.

11. A method of controlling a ring oscillator, the method comprising the steps of:

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providing a ring oscillator having a plurality of cascaded inverting stages formed in a ring for producing an oscillating output having rising and falling transitions;  
providing an input signal to an enable/disable circuit coupled to the ring oscillator; and  
disabling the ring oscillator in response to the input signal, such that additional rising and falling transitions are prohibited.

\* \* \* \* \*



US005535160A

# United States Patent [19]

Yamaguchi

[11] Patent Number: 5,535,160  
[45] Date of Patent: Jul. 9, 1996

## [54] SEMICONDUCTOR INTEGRATED CIRCUIT

5,375,083 12/1994 Yamaguchi ..... 365/185  
5,394,027 2/1995 Park ..... 365/189.09

[75] Inventor: Atsuo Yamaguchi, Itami, Japan

## FOREIGN PATENT DOCUMENTS

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha,  
Tokyo, Japan

152298 2/1989 Japan .  
153400 3/1989 Japan .  
1102662 4/1989 Japan .  
1151100 6/1989 Japan .  
1192100 8/1989 Japan .  
3181096 8/1991 Japan .

[21] Appl. No.: 269,369

[22] Filed: Jun. 30, 1994

## [30] Foreign Application Priority Data

Jul. 5, 1993 [JP] Japan ..... 5-165672

[51] Int. Cl.<sup>6</sup> ..... G11C 7/00

[52] U.S. Cl. .... 365/189.01; 365/189.09;  
365/218; 365/204; 327/536; 327/537

[58] Field of Search ..... 365/185, 204,  
365/218, 189.09, 189.01, 226; 327/536,  
537

## [56] References Cited

### U.S. PATENT DOCUMENTS

4,601,020 7/1986 Arakawa et al. .... 365/185  
5,214,605 5/1993 Lim et al. .... 365/189.09  
5,313,429 5/1994 Chevallier et al. .... 365/218  
5,363,334 11/1994 Alexander et al. .... 365/189.01

Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Leydig, Voit & Mayer

## [57]

## ABSTRACT

An integrated circuit has a built-in EEPROM which utilizes a high voltage to write or erase data. The integrated circuit operates with a lower power supply voltage. Switches supply a high voltage to bit lines, control gate lines, and word lines. Each switch includes a multi-stage charge pump comprising diode-connected transistors and capacitors. The switch has an enhanced charge capability and can transfer a high voltage from a low power supply voltage. Thus, the switch can operate successfully with a low power supply voltage.

3 Claims, 13 Drawing Sheets

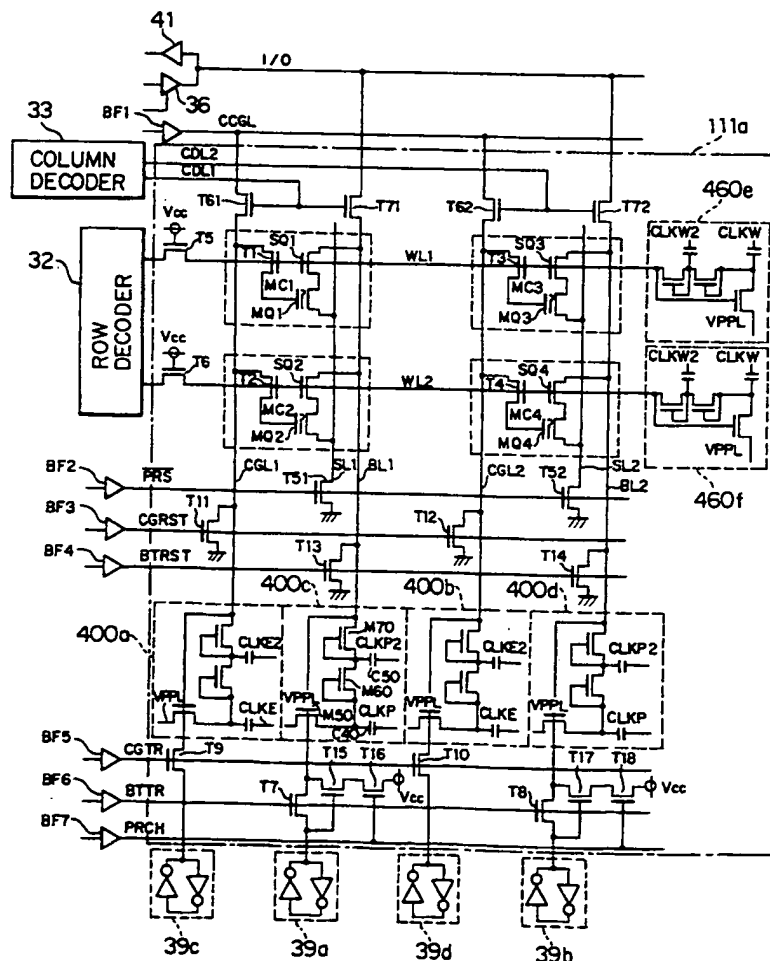


FIG. 1

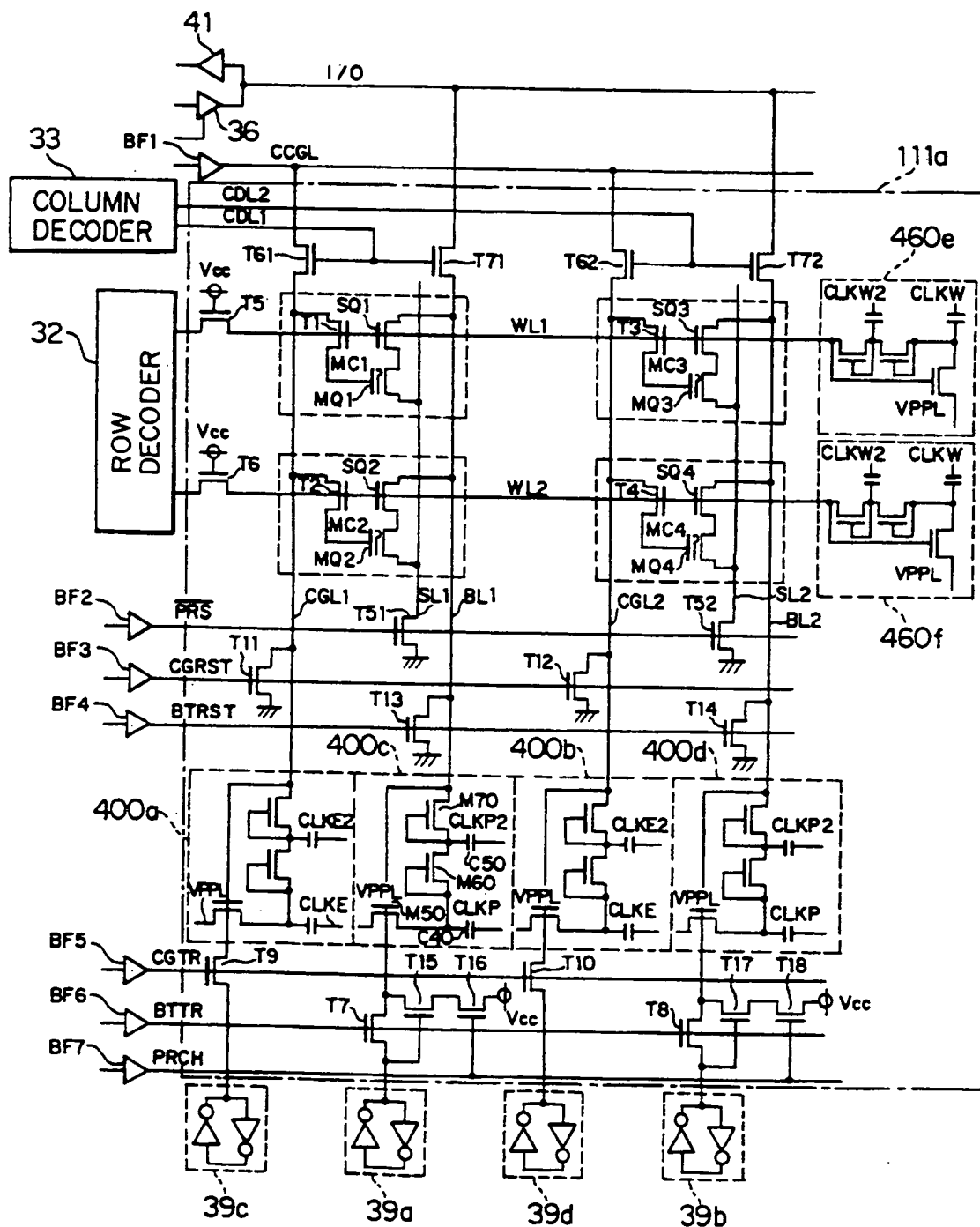


FIG. 2

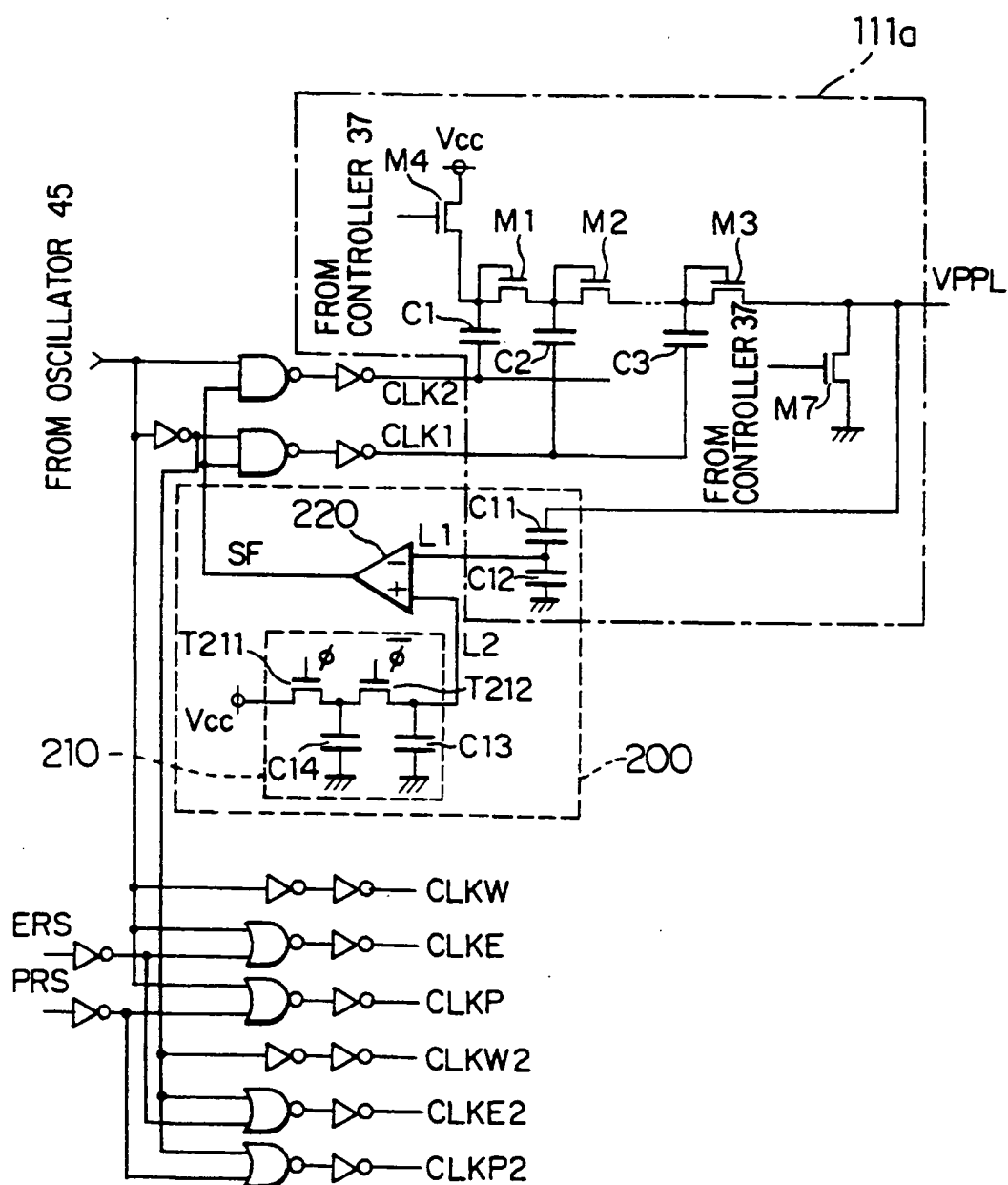


FIG. 3

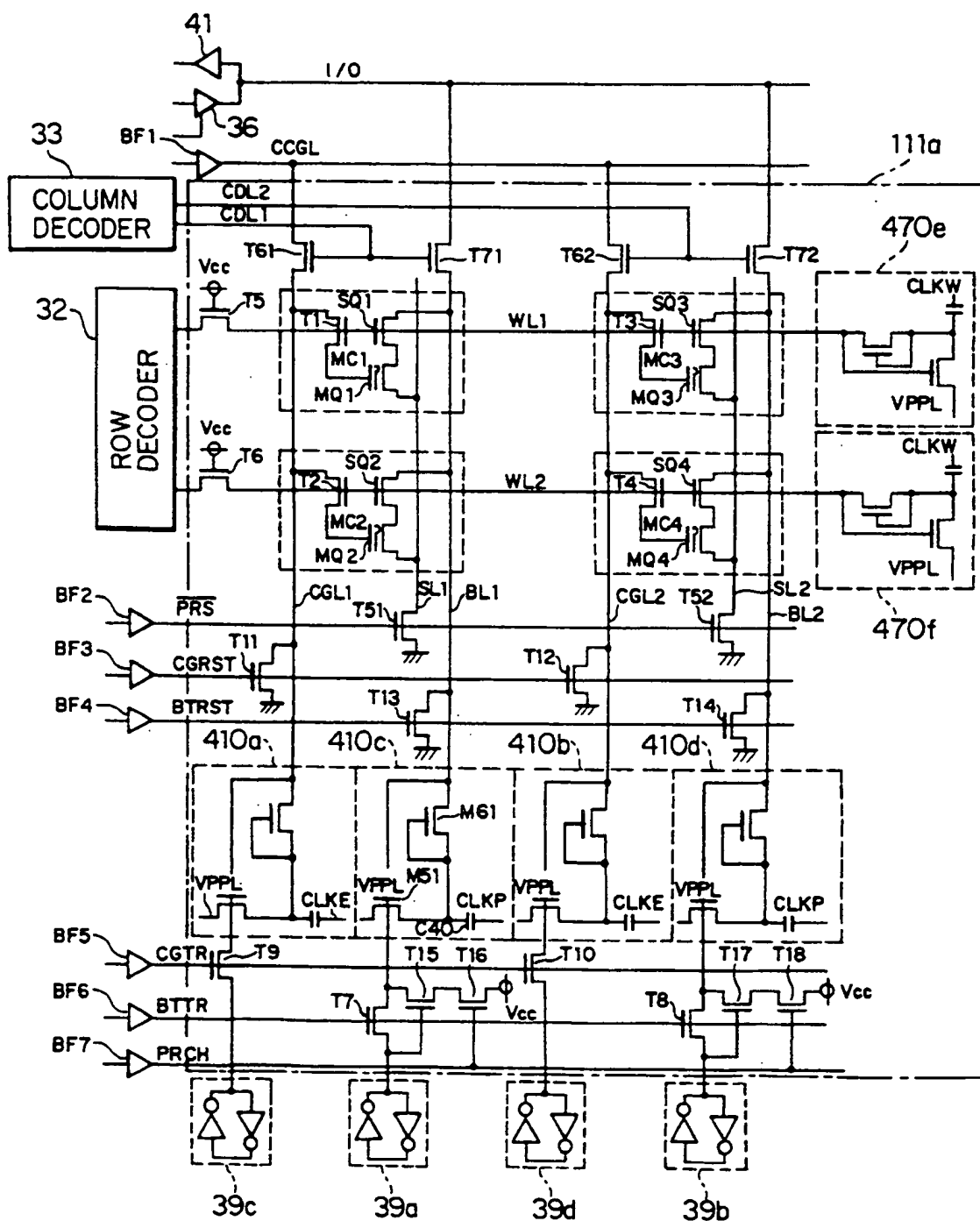


FIG. 4

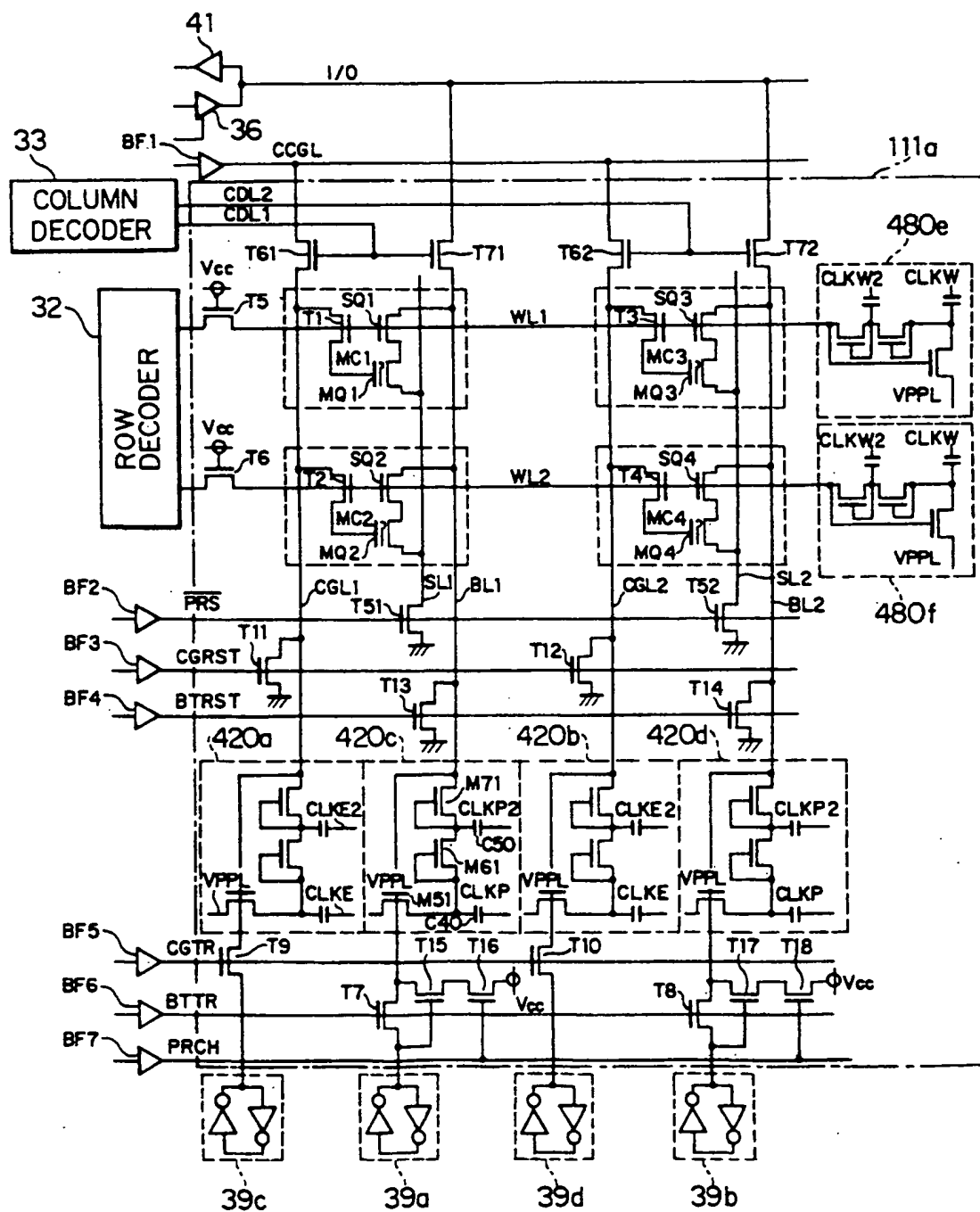
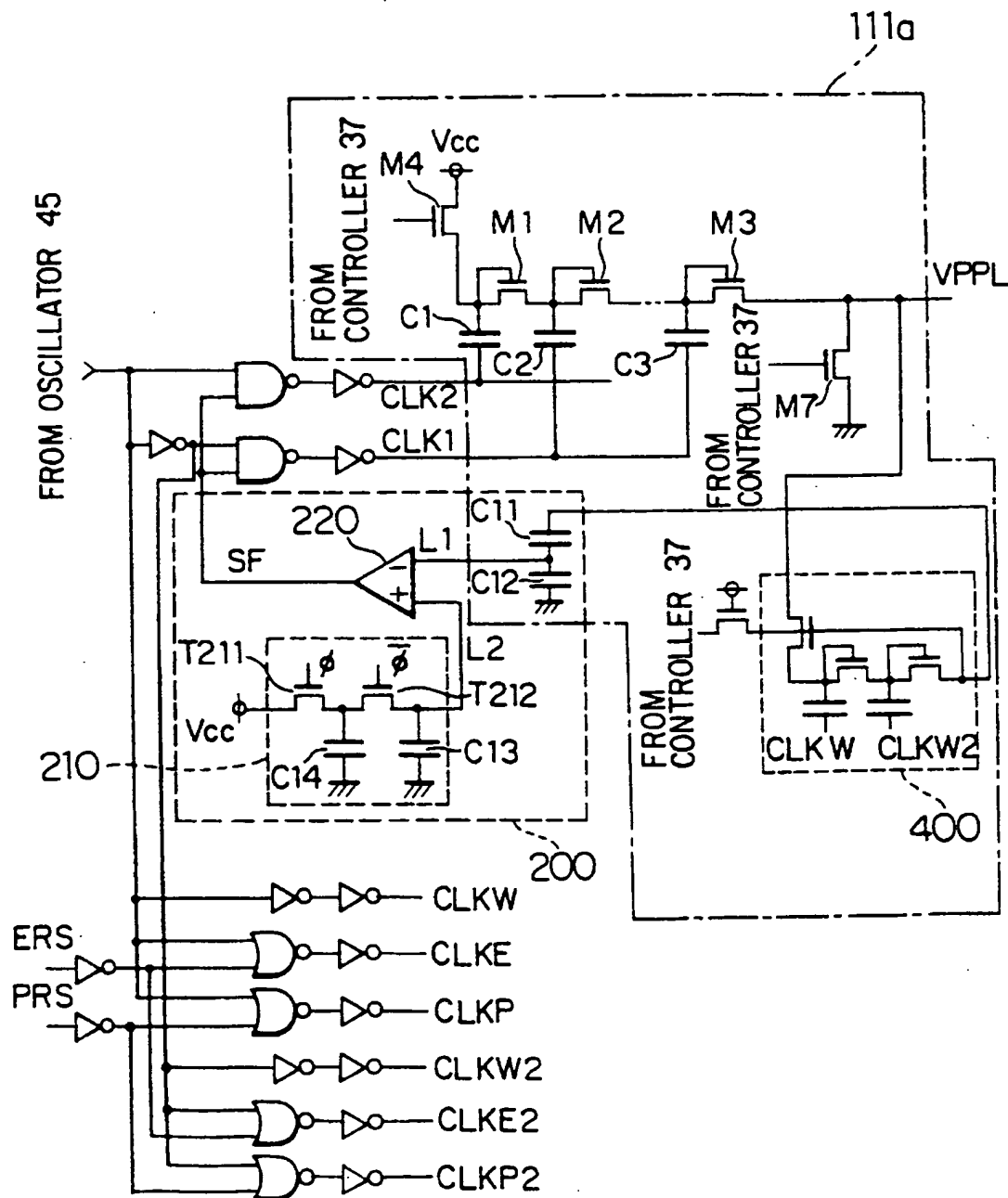
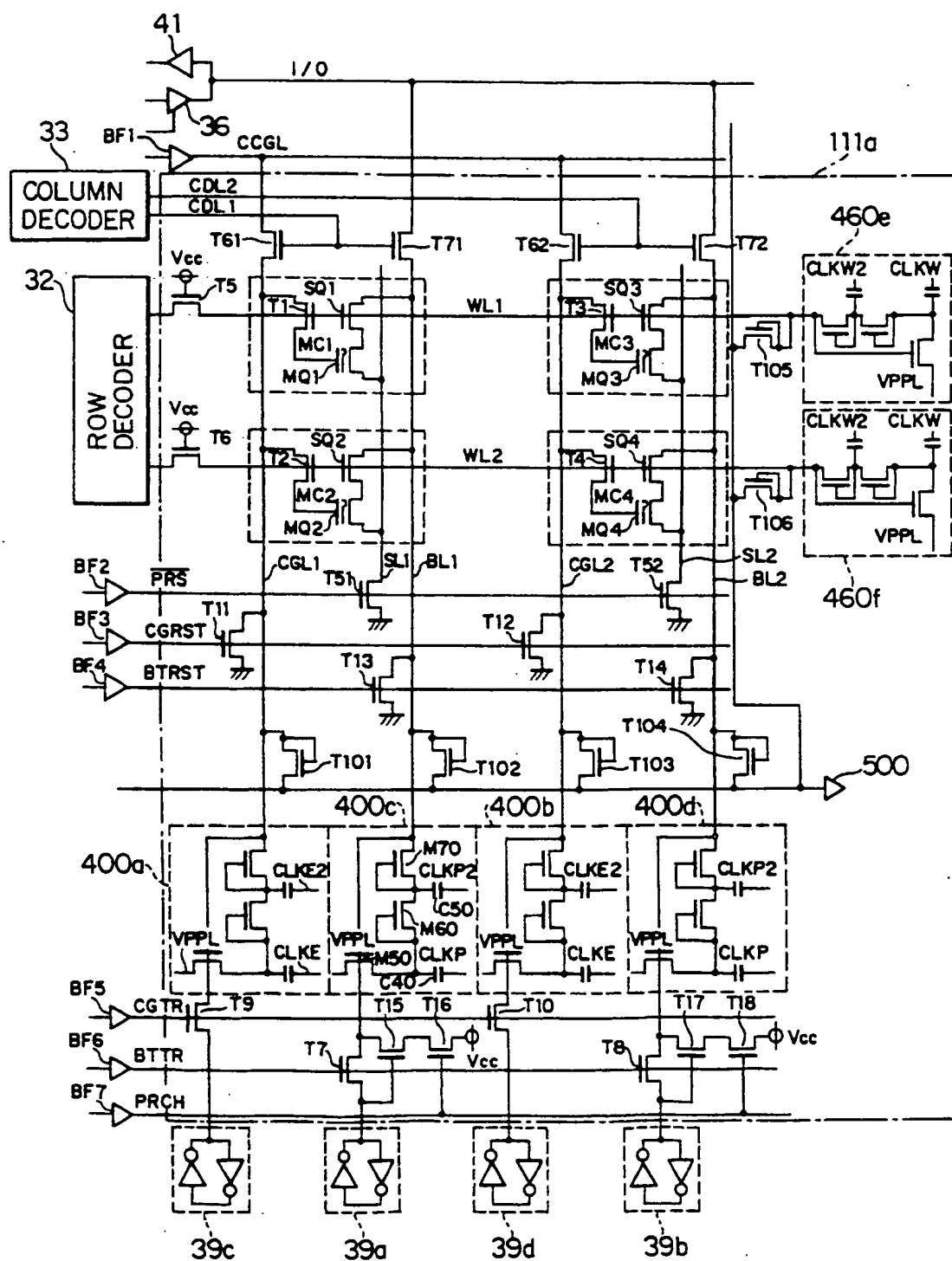


FIG. 5

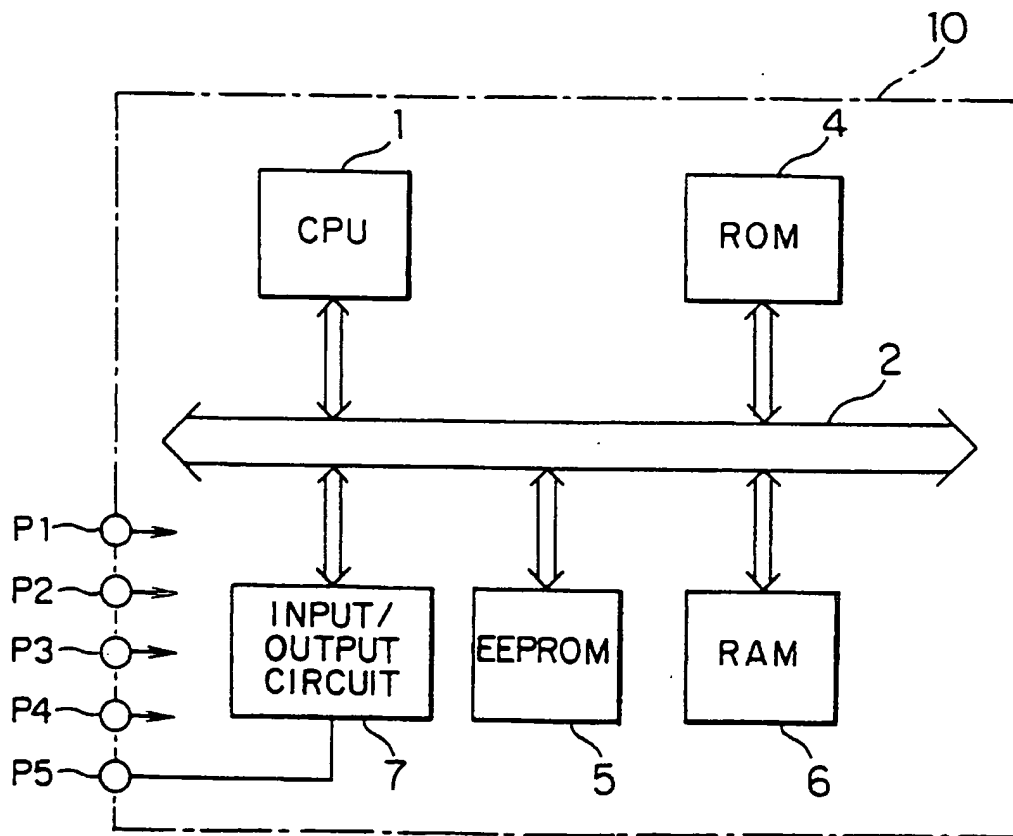


**FIG. 6**

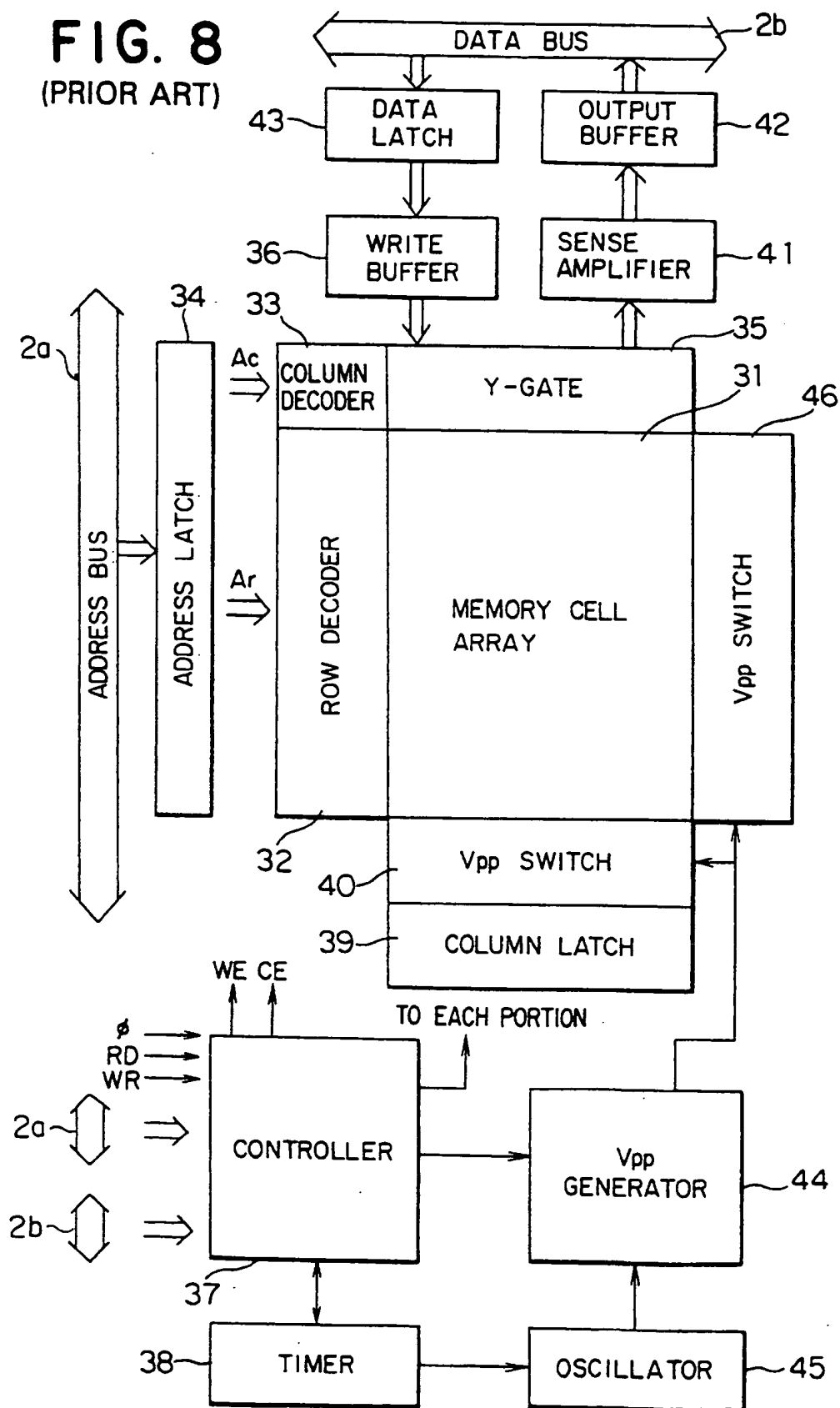




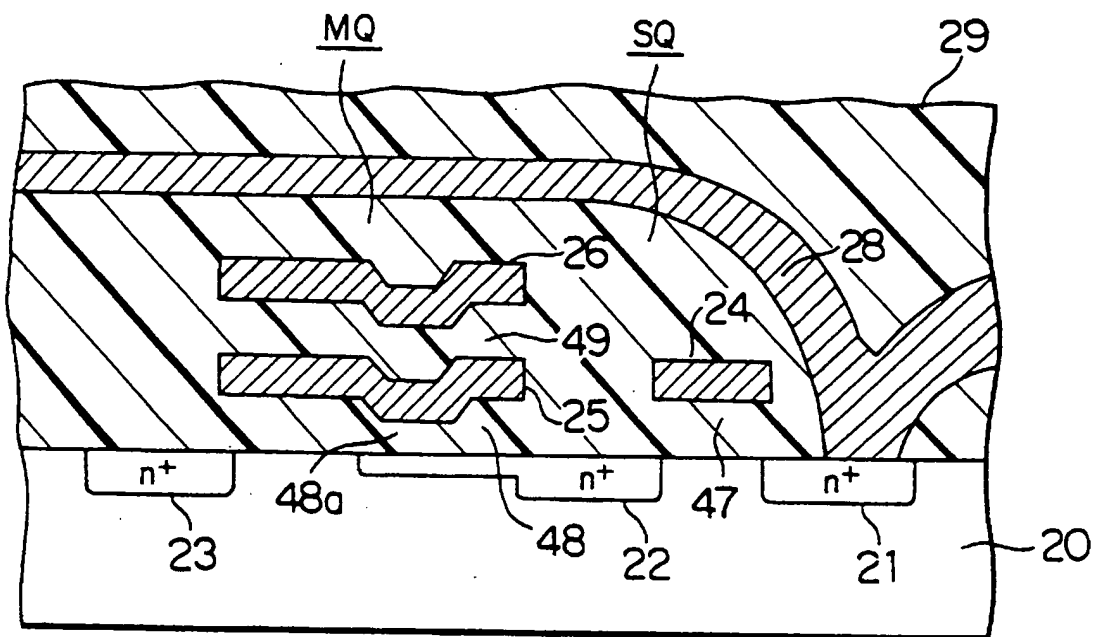
**FIG. 7**  
(PRIOR ART)



**FIG. 8**  
(PRIOR ART)



**FIG. 9A** (PRIOR ART)



**FIG. 9B** (PRIOR ART)

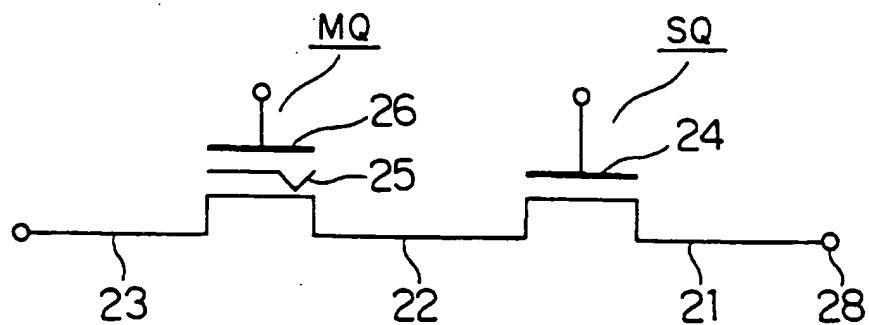
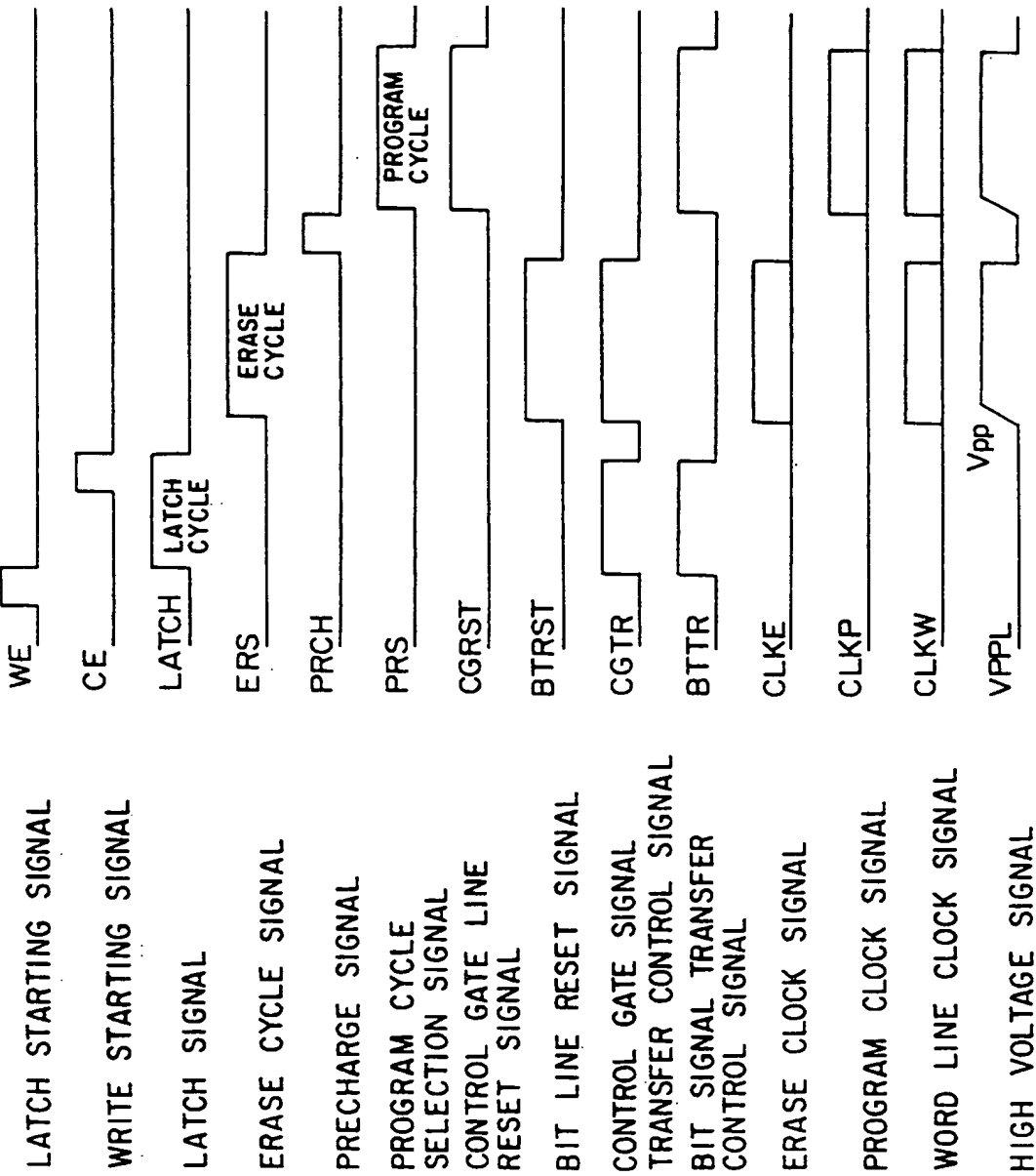
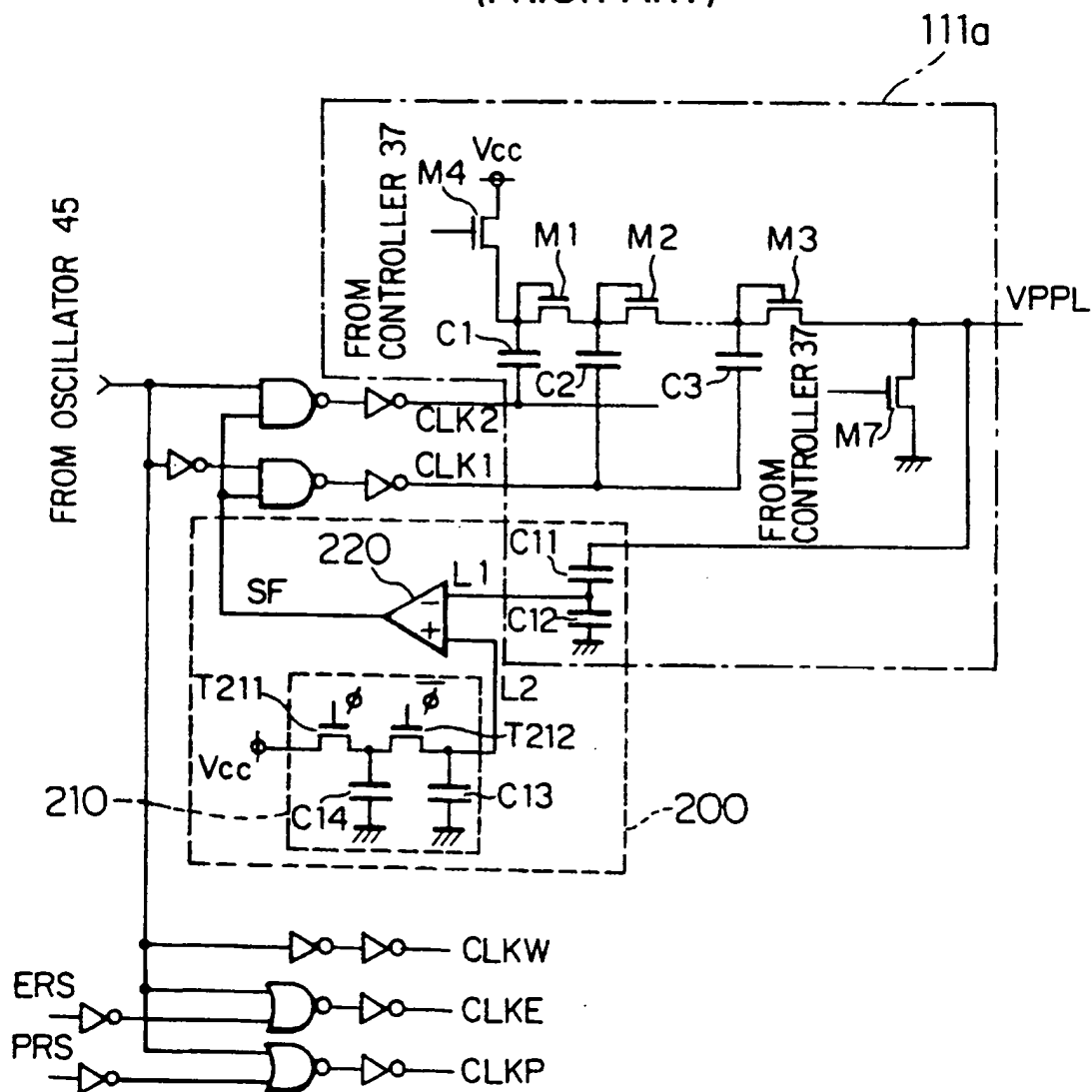
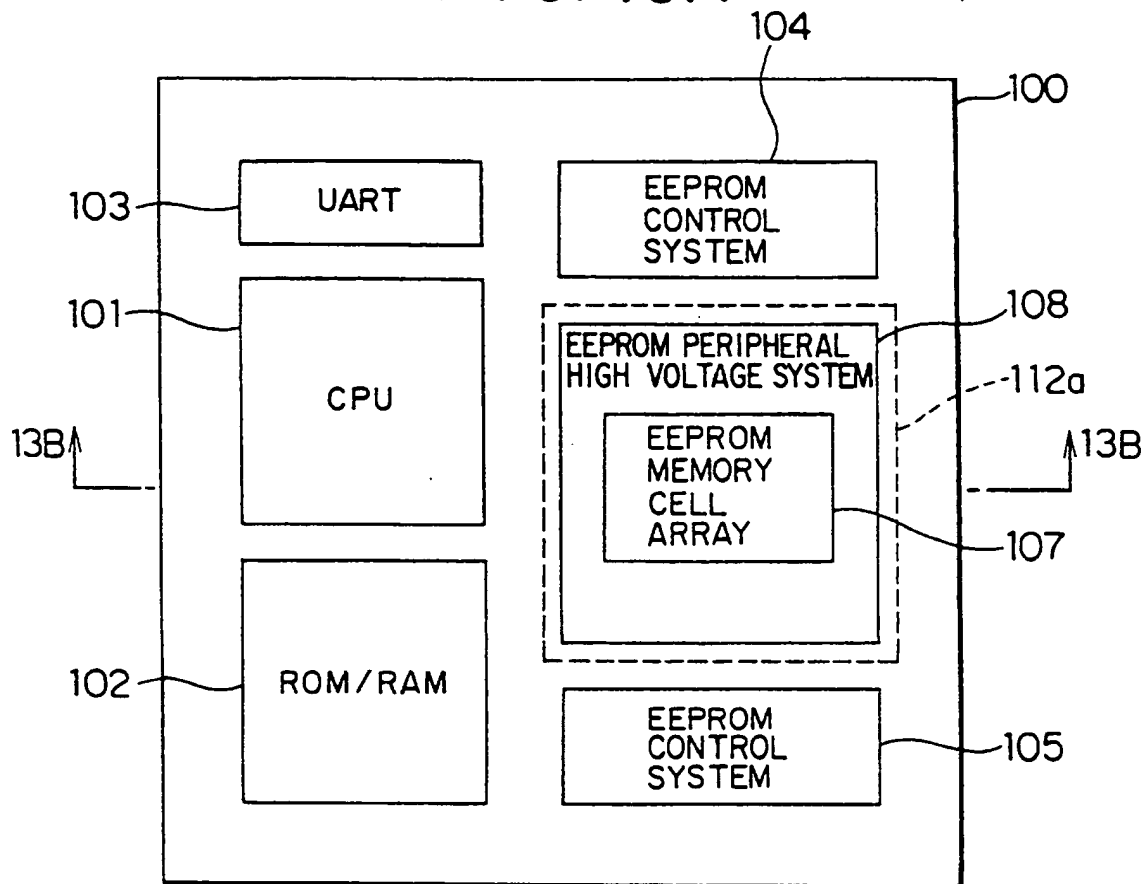
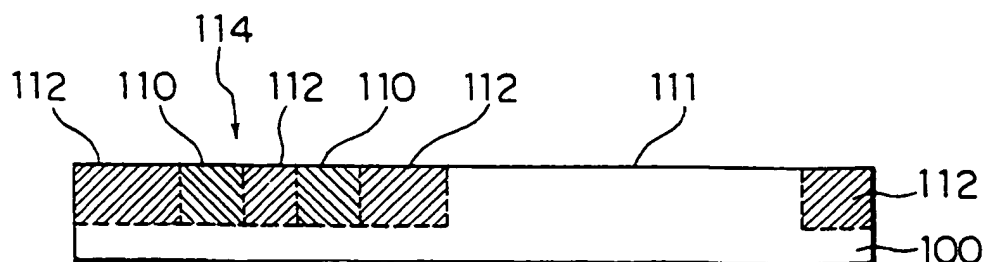




FIG. 11 (PRIOR ART)



**FIG. 12**  
(PRIOR ART)

**FIG. 13A** (PRIOR ART)**FIG. 13B** (PRIOR ART)

## SEMICONDUCTOR INTEGRATED CIRCUIT

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

The present invention relates to a semiconductor integrated circuit and, more specifically, to a technique for expanding the operating voltage of a semiconductor integrated circuit such as a microcomputer having a built-in EEPROM.

## 2. Description of the Related Art

Referring to FIGS. 7-13, the configuration and operation of an EEPROM and its peripheral circuits will be described first taking a microcomputer having a built-in EEPROM as an example.

FIG. 7 is a block diagram illustrating a general configuration of a microcomputer having a built-in EEPROM (Electrically Erasable Programmable Read Only Memory) for use in an IC card. In FIG. 7, reference numeral 10 denotes an IC card or a microcomputer for performing data processing. In the microcomputer 10, reference numeral 1 denotes a CPU or a central processing unit that is responsible for operations and control of data processing. That is, the CPU 1 is responsible for execution and control of a program associated with the data processing. Reference numeral 4 denotes a ROM serving as a program memory for storing a program required for the data processing. That is, the ROM 4 stores a program that executes various functions a user of a card needs. Reference numeral 5 denotes an EEPROM acting as a nonvolatile memory in which personal information of a card user is written and stored. Reference numeral 6 denotes a RAM acting as a temporary memory for temporarily storing data required for the data processing. Reference numeral 7 denotes an input/output circuit for inputting and outputting data from or to peripheral devices. Reference numeral 2 denotes a system bus for making connection between the above-described component elements. Furthermore, P1 denotes a positive power supply terminal, P2 a negative power supply terminal or a ground terminal, P3 a reset input terminal for receiving a reset signal to initialize the CPU 1, P4 a clock input terminal for receiving a clock signal, and P5 an I/O terminal for inputting and outputting data. The I/O terminal P5 is connected to the input/output circuit 7 that is further connected to the system bus 2. The input/output circuit 7 is responsible for data communication via the I/O terminal P5 between the IC card 10 and peripheral devices (not shown).

FIG. 8 is a block diagram illustrating a general configuration of an EEPROM. In this figure, reference numeral 31 denotes a memory cell array comprising memory cells (refer to FIGS. 9 and 10) arranged in a matrix form, in which memory cells on each row are connected in common to a corresponding word line and memory cells on each column are connected in common to a corresponding bit line (refer to FIG. 10 for both word and bit lines). Reference numerals 2a and 2b denote data buses included in the system bus. Selection of word lines is accomplished by a row decoder 32, and selection of bit lines is accomplished by a column decoder 33. The row decoder 32 sets one word line to an H level and sets the other word lines to an L level according to a row address Ar obtained via an address latch 34. The column decoder 33 selectively turns on a Y-gate 35 according to a column address Ac obtained via the address latch 34 so as to electrically connect a bit line to a write buffer 36. The row decoder 32 and the column decoder 33 are enabled or disabled by a controller 37. The address latch 34 latches

an address signal in response to the output from the controller 37, and provides a row address Ar and a column address Ac to the row decoder 32 and the column decoder, respectively.

The controller 37 sets a time width or a pulse duration of a specific signal by using a timer 38. The controller 37 is also responsible for control regarding activation and inactivation of an oscillator 45, a Vpp generator 44, a column latch 39, Vpp switches 40, 46, a sense amplifier 41, the row decoder 32, and the column decoder 33. The controller 37 latches data, that should be written, in the latch 43 according to a control clock signal  $\Phi$  and a write signal WR, and further provides the data to the write buffer 36.

When enabled, the column latch 39 temporarily holds write data given on each bit line. The Vpp switches 40 and 46, when enabled, raise the potentials of a bit line and a control gate line (refer to FIG. 10) connected to the column latch 39, and a word line connected to the row decoder 32 to a high voltage of Vpp. The sense amplifier 41, when enabled, amplifies data that has been stored via the y-gate 35 in a memory cell of the memory cell array 31, and provides the amplified data to an output buffer 42. The output buffer 42, in response to the output from the controller 37, outputs the data that is read out by the sense amplifier 41 onto the data bus 2b as read-out data. The controller 37 controls the address latch 34 and the output buffer 42, according to the control clock signal  $\Phi$  and the read-out signal RD.

FIGS. 9A and 9B illustrate one memory cell included in the memory cell array 31 of the EEPROM shown in FIG. 8, wherein FIG. 9A illustrates its cross-section and FIG. 9B illustrates an equivalent circuit of the cell shown in FIG. 9A. As can be seen from these figures, a memory cell comprises a memory transistor MQ and a selection transistor SQ. As shown in FIG. 9A, n<sup>+</sup>-diffusion regions 21-23 are formed in a p-type semiconductor substrate 20 by diffusing n-type impurities selectively into the semiconductor substrate 20. Reference numeral 29 denotes an insulating layer. A gate 24 is formed above the area between the n<sup>+</sup>-diffusion regions 21 and 23 via an oxide film 47, and a floating gate 25 is formed above a part of n<sup>+</sup>-diffusion region 22 and above the area between the n<sup>+</sup>-diffusion regions 22 and 23 via an oxide film 48. The floating gate 25 has, above the n<sup>+</sup>-diffusion region 22, a portion which is lower than the other portions. The portion of the oxide film 48 disposed under this lower portion of the floating gate 25 is as thin as 100 Å and acts as a tunnelling oxide film 48a. A control gate 26 corresponding to the floating gate 25 is formed above the floating gate 25 via an oxide film 49. A bit line 28 made of an aluminum interconnection layer is also formed above the n<sup>+</sup>-diffusion region 21.

The memory cell having the above-described structure comprises a series connection of an enhancement-type selection transistor SQ and a memory transistor MQ having a variable threshold voltage, as shown in FIG. 9B. The selection transistor SQ has a gate 24, and utilizes n<sup>+</sup>-diffusion regions 21 and 22 as drain and source regions, respectively. The memory transistor MQ has a floating gate 25 and a control gate 26, and utilizes n<sup>+</sup>-diffusion regions 22 and 23 as drain and source regions, respectively.

Writing into the memory transistor MQ is done basically by applying a high voltage to either the drain 22 or the control gate 26, and grounding the other, so as to induce an electric field as high as 10 MV/cm in the tunnelling oxide film 48a, thereby injecting or emitting electrons into or from the floating gate 25. If electrons are injected into the floating gate 25 of the memory transistor MQ, then its threshold



voltage shifts in the positive direction. If electrons are extracted from the floating gate 25, then the threshold voltage shifts in the negative direction. Nonvolatile writing is accomplished by using correspondence between positive and negative threshold voltages as information "1" and "0".

Information is basically read out from the memory transistor MQ as follows. An H-level signal is applied to the gate 24 of a selection transistor SQ of a selected memory cell, and the source 23 of the memory transistor MQ is made a ground potential. Furthermore, a read-out voltage VCG having a magnitude, for example, of about 0V is applied to the control gate 26. In this situation, if the threshold voltage of the memory transistor MQ is positive, then the memory transistor MQ turns off. If the threshold voltage is negative then the memory transistor MQ turns on. If the memory transistor MQ turns on, a current flows from the bit line 28 toward the ground level via the selection transistor SQ and via the memory transistor MQ. This current is converted into a voltage and detected by a sense amplifier 41 (refer to FIG. 8) connected to the bit line 28. Thus, information has been read out. An L-level signal is applied to gates of selection transistors SQ of all non-selected memory cells so that all these selection transistors SQ are turned off. Therefore, in this case, there is no current flowing from the bit line 28 to the ground level, even if memory transistors MQ have a negative threshold voltage.

FIG. 10 illustrates a peripheral circuit of the memory cell array 31 of the EEPROM shown in FIG. 8. For simplicity, only four memory cells MC1, MC2, MC3, and MC4 organized in 1-byte 1-bit fashion are shown in the figure. In the following description, signal lines and signals transmitted through these lines are denoted by the same notations. The memory cells MC1-MC4, as shown in FIG. 9, comprise memory transistors MQ1, MQ2, MQ3, MQ4 and selection transistors SQ1, SQ2, SQ3, SQ4, respectively. The drains of the selection transistors SQ1 and SQ2 are connected to a bit line BL1, and the drains of the selection transistors SQ3 and SQ4 are connected to a bit line BL2. The sources of the memory transistors MQ1 and MQ2 are connected to a source line SL1, and the sources of the memory transistors MQ3 and MQ4 are connected to a source line SL2.

These source lines SL1 and SL2 are grounded via transistors T51 and T52 whose gates are supplied with an inverted program cycle selection signal  $\overline{\text{PRS}}$ . The control gates of the memory transistors MQ1 and MQ2 are connected to a control gate line CGL1 via byte selection transistors T1 and T2, respectively. Similarly, the control gates of the memory transistors MQ3 and MQ4 are connected to a control gate line CGL2 via byte selection transistors T3 and T4, respectively. The gates of the transistors T1, T3, and the gates of the selection transistors SQ1, SQ3 are all connected to a word line WL1. The gates of the transistors T2, T4, and the gates of the selection transistors SQ2, SQ4 are all connected to a word line WL2. One end of the word line WL1 and that of WL2 are connected to the row decoder 32 via high voltage isolation transistors T5 and T6, respectively, wherein a power supply voltage Vcc is applied to the gates of the high voltage isolation transistors T5 and T6.

One end of each of the bit lines BL1, BL2 and one end of each of the control gate lines CGL1, CGL2 are connected to column latches 39a, 39b, 39c, 39d, respectively, via transistors T7, T8, T9, and T10, respectively. The other ends of the control gate lines CGL1 and CGL2 are connected to a common control gate line CCGL via transistors T61 and T62, respectively. The other ends of the bit lines BL1 and BL2 are connected to an input/output line I/O via Y-gate

transistors T71 and T72, respectively. The gates of the transistors T61 and T71 are connected to an output line CDL1 of the column decoder 33. Similarly, the gates of the transistors T62 and T72 are connected to an output line CDL2. The common control gate line CCGL is connected to a buffer BF1, and the input/output line I/O is connected to a write buffer 36 and to the sense amplifier 41. The control gate lines CGL1, CGL2, the bit lines BL1, BL2, and the word lines WL1, WL2 are connected to Vpp switches 40a-40d, 46e, 46f, respectively. The Vpp switches 40a-40d, 46e, 46f are connected to a high voltage line VPPL via which a high voltage of 15-20V is supplied. In response to an applied erase clock signal CLKE, program clock signal CLKP, and word line clock signal CLKW, the Vpp switches 40a-40d, 46e, 46f raise the connected control gate lines CGL1, CGL2, bit lines BL1, BL2, and word lines WL1, WL2 up to the high voltage Vpp if these lines are at an H level. When the word lines WL1 and WL2 are raised to the high voltage Vpp, the row decoder 32 is isolated from the high voltage Vpp by the transistors T5 and T6 whose gates are supplied with the supply voltage Vcc.

A bit signal transfer control signal BTTR is connected to the gates of the transistors T7 and T8, and a control gate signal transfer control signal CGTR is connected to the gates of the transistors T9 and T10. When these signals are at H levels, mutual signal communications are accomplished between the bit lines BL1, BL2, control gate lines CGL1, CGL2, and the column latches 39a, 39b, 39c, 39d. When the bit lines BL1, BL2, and the control gate lines CGL1, CGL2 are raised to the high voltage Vpp, the column latches 39a, 39b, 39c, 39d are isolated from the high voltage Vpp, since the gates of the transistors T7-T10 are at the Vcc level.

The transistors T11 and T12 are connected to the control gate lines CGL1 and CGL2, respectively, and the gates of the transistors T11 and T12 are connected to a control gate line reset signal CGRST. When the control gate line reset signal CGRST rises to an H level, the control gate lines CGL1 and CGL2 falls to an L level. The bit lines BL1 and BL2 are connected to transistor T13 and T14, respectively, and the gates of the transistors T13 and T14 are connected to a bit line reset signal BTRST. When the bit line reset signal BTRST rises to an H level, the bit lines BL1 and BL2 fall to an L level. The bit lines BL1 and BL2 are also connected to transistors T15 and T17, respectively. The transistors T15 and T17 are connected to transistors T16 and T18 respectively. The gates of the transistors T15 and T17 are connected to the column latches 39a and 39b, respectively. The gates of the transistors T16 and T18 are connected to a precharge signal PRCH. When the column latches 39a and 39b are at an H level, if the precharge signal PRCH rises up to an H level, then both bit lines BL1 and BL2 rise to an H level.

The inverted program cycle selection signal  $\overline{\text{PRS}}$ , the control gate line reset signal CGRST, the bit line reset signal BTRST, the control gate signal transfer control signal CGTR, the bit signal transfer control signal BTTR, and the precharge signal PRCH are driven by buffers BF2, BF3, BF4, BF5, BF6, and BF7, respectively.

Referring to FIGS. 8 and 10, read-out operation of the EEPROM will be described below. First, selections of word lines WL, control gate lines CGL, and bit lines BL are performed by the row decoder 32 and the column decoder 33. In the following description, an operation will be explained for the case where a memory cell MC1 is selected by selecting the word line WL1 and by turning on the transistors T61 and T71 so as to select the control gate line CGL1 and the bit line BL1. The inverted program cycle

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selection signal  $\overline{\text{PRS}}$  is raised to an H level, and the source lines SL1 and SL2 are grounded. Furthermore, the controller 37 disables the column latches 39a-39d, the Vpp switches 40a-40d, 46e, 46f, and the write buffer 36. The buffer BF1 supplies a voltage of 0V to the gate of the memory transistor MQ1 via the common control gate line CCGL, transistor T61, and transistor T1. Then, if the memory transistor MQ1 has a positive threshold voltage the memory transistor MQ1 turns off. If the threshold voltage is negative, the transistor MQ1 turns on. The presence or absence of a current flowing through the bit line BL1 due to the turning on or off of the memory transistor MQ1 is detected from the change in the potential on the input/output line I/O by the sense amplifier 41. The potential change detected by the sense amplifier 41 is further amplified, and provided as a read-out output signal. In this way, the read-out operation is performed.

FIG. 11 is a timing chart illustrating various signal waveforms relating to a writing operation of the EEPROM. Referring to FIGS. 8-11, a writing operation will be explained below for the case where the memory cell MC1 is selected. First, a latch cycle starts with a latch starting signal WE to drive a latch signal LATCH to an H level. When the latch cycle starts, the controller 37 enables the column latches 39a-39d, the column decoder 33, and the write buffer 36, and the common control gate line CCGL is set to an H level. On the other hand, the controller 37 disables the row decoder 32 and the sense amplifier 47. In a time period during which the latch signal LATCH is kept at the H level, the transistors T61 and T71, selected by the column decoder 33, turn on, and the data ("H" corresponds to information "0", and "L" corresponds to information "1") held by the data latch 43 is latched by the column latch 39a via the write buffer 36, the input/output line I/O, the bit line BL1, and the transistor T7. Furthermore, an H level is latched by the column latch 39c via the common control gate line CCGL and the control gate line CGL1. Then, once a write starting signal goes to an H level, the signal LATCH changes to an L level, and an erase cycle signal ERS rises, whereby an erase cycle starts. An erasing cycle is such a cycle during which the erasing cycle signal ERS is at an H level, and a program cycle is such a cycle during which the program cycle selection signal PRS (that is an inverted signal of the inverted program cycle selection signal  $\overline{\text{PRS}}$ ) is at an H level. The H-level pulse durations of these signals ERS and PRS are set to proper values by the controller 37 by using the timer 38.

During the erasing cycle, the row decoder 32 is enabled by the controller 37, and only the word line WL1 is set to an H level by the row decoder 32. Furthermore, the column decoder 33 is disabled by the controller 37. A high voltage Vpp having a pulse duration of about 4 msec is then applied on the high voltage line VPPL thereby applying the high voltage Vpp to the Vpp switches 40a-40d, 46e, 46f. Then, the controller 37 makes a high frequency oscillator, which comprises an oscillating circuit 45 and a Vpp generator 44, generate a high frequency erase clock signal CLKE and a word line clock signal CLKW having a frequency of a few MHz, which are supplied to the Vpp switches 40a, 40b, and the Vpp switches 46e, 46f, respectively. Since the inverted program cycle selection signal  $\overline{\text{PRS}}$  is at the H level, the source lines SL1 and SL2 are grounded. In the above-described state, the word line WL1 and the control gate line CGL1 are raised to the high voltage Vpp by the Vpp switches 40a and 46e, respectively. As a result, tunneling occurs between the floating gate 25 (refer to FIG. 9) and the drain region ( $n^+$ -diffusion region 22) of the memory transistor MQ1, whereby electrons are injected into the floating

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gate 25. As a result, the threshold voltage of the memory transistor MQ1 shifts in the positive direction (information "1" is stored). When the erasing cycle is complete, the potential of the control gate line CGL1 is reset to an L level.

The erasing cycle signal ERS then falls, and the precharge signal PRCH rises to an H level. Then, a program cycle starts with rising of the program cycle selection signal PRS. The controller 37 disables the word line clock signal CLKW and the erase clock signal CLKE. Subsequently, the controller 37 provides again a high frequency program clock signal CLKP and a word line clock signal CLKW having a frequency of a few MHz from the high frequency oscillator to the Vpp switches 40c, 40d, and the Vpp switches 46e, 46f, respectively. Since the inverted signal  $\overline{\text{PRS}}$  is at an L level, the source line SL1 is in a floating state. In this situation, if an H level is latched by the column latch 39a, the word line WL1 and the bit line BL1 are raised to the high voltage Vpp. As a result, tunneling occurs between the floating gate 25 (refer to FIG. 9) and the drain region ( $n^+$ -diffusion region 22) of the memory transistor MQ1, whereby electrons are emitted from the floating gate 25. As a result, the threshold voltage of the memory transistor MQ1 shifts in the negative direction (information "0" is stored). On the other hand, in the case where an L level is latched by the column latch 39a, only word line WL1 rises up to the high voltage Vpp, and the threshold voltage of the memory transistor MQ1 is maintained unchanged. In this way, the writing operation is complete.

FIG. 12 is a circuit diagram illustrating the internal configuration of the Vpp generator (high voltage generator) 44 shown in FIG. 8, which will be described below.

The gate and the drain of a transistor M1 are connected to each other. A capacitor C1 is connected to the node at which the gate and the drain are connected. The source of the transistor M1 is connected to the drain of a transistor M2 disposed at the following stage. The gate and the drain of the transistor M2 are also connected to each other, and a capacitor C2 is also connected to the node which connects the gate and drain of the transistor M2. Clock signals CLK2 and CLK1 are applied to the other ends of the capacitors C1 and C2 connected to the drains of the transistors M1 and M2, respectively, wherein the phases of the clock signals CLK2 and CLK1 are opposite each other. Several stages, each having a configuration similar to that described above, are cascaded. The drain of the transistor M1 at the first stage is connected to the source of the transistor M4. The drain of the transistor M4 is connected to the power supply voltage Vcc. The gate of the transistor M4 is controlled by the output signal provided by the controller 37. The charge pump output is provided via the source of the transistor M3 at the end stage. The high voltage Vpp is provided as the output of the Vpp generator 44, and applied to the Vpp switches 40a-40d, 46e, 46f via the high voltage line VPPL so as to raise the control gate lines CGL1, CGL2, the bit lines BL1, BL2, and the word lines WL1, WL2 up to the high voltage according to control signals. The transistor M7 discharges the high voltage Vpp in response to the signal provided by the controller 37.

The Vpp generator 44 also includes a waveform shaping circuit 200, which will be described later.

Now, the configuration of a high voltage switch shown in FIG. 10 will be described taking the high voltage switch 40c as an example. The other high voltage switches are configured in the same manner as that of the high voltage switch 40c, and thus these will not be described. The drain of a transistor M5 is connected to the high voltage, and its source

is connected to the drain of a diode-connected transistor M6. The source of the transistor M5 is further connected to one end of a capacitor C4. The term "diode connection" refers to a configuration in which the gate and the drain of a transistor are connected to each other, forming a diode between the source and the drain. The source of the transistor M6 is connected to the gate of the transistor M5, and further connected to the bit line BL1. The other end of the capacitor C4 is connected to the program clock signal CLKP. Clock signals having the same phase are applied to the clock signal lines CLKP and CLK2. A clock signal having a phase opposite to those applied to lines CLKP and CLK2 is applied to the clock signal line CLK1 (refer to FIG. 12).

Operations of the Vpp generator 44 and of the high voltage switch 40c will be described below. In the Vpp generator 44 shown in FIG. 12, charges are stored in the capacitor C1 when the clock signal CLK2 is at an L level. When the clock signal CLK2 rises, the charges stored in the capacitor C1 are transferred to the capacitor C2 via the transistor M1. When the clock signal CLK2 then falls with the rising clock signal CLK1, charges are further stored in the capacitor C1. At this time, charges stored in the capacitor C2 are transferred to a capacitor of the following stage. In this operation step, no charges are transferred to the capacitor C1 since the transistor M2 acts as a diode. In this way, charges are sequentially transferred according to the clock signals CLK1 and CLK2, and finally, a raised voltage is output via the charge pump output.

In the high voltage switch 40c shown in FIG. 10, when the column latch 39a holds an H level and the signal BTTR is at an H level, the bit line BL1 rises. In this state, when the signal CLKP is at an L level, the transistor M5 turns on, whereby the capacitor C4 is charged by the high voltage Vpp until the transistor M5 turns off. As a result, the signal CLKP rises, whereby the charges stored in the capacitor C4 are transferred to the bit line BL1 via the transistor M6. As a result, the potential at the gate of the transistor M5 connected to the bit line BL1 rises, and thus the capacitor C4 is further charged by the high voltage until the transistor M5 turns off (the signal CLKP is at an L level, in this state). In this way, the operation is performed repeatedly, whereby the bit line BL1 can be raised to the high voltage Vpp according to the signal applied via the column latch 39a.

The other Vpp switches operate in the same manner as in the case of the high voltage switch 40c described above.

The clock signals CLK1, CLK2, CLKW, CLKE, and CLKP are generated based on the signal from the oscillator 45, the erase cycle signal ERS, and the program cycle selection signal PRS.

As described above, a high voltage is applied to the control gate or the drain of a memory transistor MQ via a selection transistor SQ. However, if the output of the high voltage (Vpp) switch is directly applied to the control gate 26 or the drain 22 of a memory transistor MQ, the small time constant associated with the rising waveform of the output of the high voltage Vpp, that is, the rapid rising of the high voltage Vpp causes great damage to the tunneling oxide film 48a. In the worst case, the tunnelling oxide 48a will break down. To avoid the above problem, there is provided a waveform shaping circuit in the Vpp generator 44, for properly setting the rising time constant to a rather large value thereby reducing the damage to the tunnelling oxide film 48a.

FIG. 12 also includes the waveform shaping circuit 200.

As shown in this figure, the output voltage Vpp of the Vpp generator 44 is divided by the capacitors C11 and C12, and

the divided voltage is applied as a sample signal to the negative input of a comparator 220 via an interconnecting line L1. On the other hand, the positive input of the comparator 220 is connected to the output of the power supply voltage Vcc via a switched capacitor 210 and an interconnecting line L2.

The switched capacitor 210 comprises: transistors T211 and T212 connected in series between the power supply voltage Vcc and the interconnecting line L2; a capacitor C14 with one end connected to the node connecting the transistors T211 and T212 and the other end grounded; and a capacitor C13 connected between the interconnecting line L2 and ground. A clock signal  $\Phi$  and an inverted clock signal  $\bar{\Phi}$  are applied to the gates of the transistors T211 and T212, respectively. The drain of the transistor T211 is connected to the power supply voltage Vcc. The source of the transistor T212 is connected to the interconnecting line L2.

With this arrangement, waveform shaping is performed on the rising voltage on the interconnecting line L4 according to a time constant determined by the clock signal  $\Phi$  of the switched capacitor 210 and the capacitors C13 and 14. The waveform-shaped voltage is applied as a reference voltage to the positive input of the comparator 220.

The difference between this reference voltage and the output voltage of the above-described Vpp generator 44 is output as a feedback signal SF by the comparator 220. According to this feedback signal SF, the clock signals CLK1 and CLK2 are controlled so that the high voltage output of the Vpp generator 44 may rise up at a rate similar to that of the reference voltage.

FIG. 13 illustrates a configuration of a semiconductor substrate of a semiconductor integrated circuit for a micro-computer having a built-in EEPROM, according to a conventional technique. FIG. 13A schematically illustrates a layout of functional blocks on a semiconductor substrate, and FIG. 13B is a cross-sectional view of the semiconductor substrate of FIG. 13A taken along line 13B—13B. In this figure, reference numeral 100 denotes a p-type semiconductor substrate on which a semiconductor integrated circuit is formed. Reference numerals 101, 102, 103 denote a CPU, an ROM/RAM, and a UART or an input/output portion, respectively. Reference numerals 104 and 105 denote an EEPROM control system. Reference numerals 107 and 108 denote an EEPROM memory cell array, and an EEPROM peripheral high voltage system, respectively. Reference numerals 110, 111, 112 denote an n-well region, a p-type substrate region, a p-well region, respectively. Reference numeral 114 denotes a twin well region consisting of the n-well region 110 and the p-well region 112.

The EEPROM memory cell array 107 corresponds to the memory cell array 31 in FIG. 8, and to four portions each surrounded by a broken line in FIG. 10 wherein each portion comprises one memory cell MC and a transistor T. The EEPROM peripheral high voltage system 108 corresponds to elements of FIG. 8 including the Vpp switches 40, 46, the Y-gate 35, and a portion (a high voltage portion) of the Vpp generator 44. The EEPROM peripheral high voltage system 108 also corresponds to elements of FIG. 10 including the Vpp switches 40a–40d, the Vpp switches 46e, 46f, the transistors T5–T18, the transistors T51, T52, and the transistors T61, T62, T71, T72. The EEPROM peripheral high voltage system 108 also corresponds to elements of the Vpp generator 44 shown in FIG. 12, including the transistors M1–M4, M7, and the capacitors C1–C3, C11, C12. These corresponding portions of FIGS. 10 and 12 are each surrounded by an alternating long and short dash line 111a.

The EEPROM control systems 104 and 105 correspond to elements of FIG. 8 including the write buffer 36, the sense amplifier 41, the output buffer 42, the data latch 43, the column decoder 33, the row decoder 32, the address latch 34, the column latch 39, the controller 37, the timer 38, the oscillator 45, and the other portion of the Vpp generator 44. The EEPROM control systems 104 and 105 also correspond to elements of FIG. 10 including the write buffer 36, the sense amplifier 41, the buffers BF1-BF7, the column decoder 33, the row decoder 32, and the column latch 39a-39d. The EEPROM control systems 104 and 105 also correspond to the portion of the waveform shaping circuit 200 of FIG. 12 except for the capacitors C1 and C12.

Portions, which are not subjected to the application of the high voltage Vpp, in the CPU 101 the ROM/RAM 102, the UART 103, and the EEPROM control systems 104, 105 are formed with CMOS structures in twin well regions 114 each consisting of an n-well region 110 and a p-well region 112, as shown in FIG. 13A or 13B. On the other hand, elements to which the high voltage Vpp is applied such as the EEPROM memory cell array 107 and the EEPROM peripheral high voltage system 108, are formed with NMOS structures on the p-type substrate region 111. It is desirable that the p-type substrate region 111, in which the EEPROM memory cell array 107 and the EEPROM peripheral high voltage system 108 are formed, be surrounded by a p-well region as shown by the broken line 112a in FIG. 13A.

As described above, the region to which the high voltage Vpp is not applied is formed on the twin well region 114 consisting of the p-well region 112 and the n-well region 110 each formed in the p-type semiconductor substrate so that a high integration density may be obtained by the most advanced technology. Regions to which the high voltage Vpp is applied are formed, for example, with NMOS structures on the p-type substrate region 111 so that the substrate effects may be suppressed whereby the high voltage system may operate successfully. Furthermore, the p-type substrate region 111 is surrounded by the p-well region so as to enhance the resistance to latchup so that latchup effects may be suppressed.

In the above description, a conventional technique of a semiconductor integrated circuit for a microcomputer having a built-in EEPROM has been discussed. However, for example in the Vpp switch 40c shown in FIG. 10, when the high voltage Vpp is selectively supplied to a memory cell, it is required that the amplitude of the clock signal should be greater than the sum of the threshold voltage Vth of the transistor M5 which is responsible for the selection of the memory cell and the threshold voltage Vth of the transistor M6 forming the charge pump. If this condition is not met, the high voltage Vpp does not appear at the output. Since the amplitude of the clock signal is determined by the power supply voltage Vcc, if the power supply voltage Vcc decreases, it becomes impossible to transfer the high voltage Vpp to the output. The threshold voltage Vth increases as the source voltage increases. Therefore, it will become more difficult to transfer the high voltage to the output as the output increases. For these reasons, the Vpp switch (high voltage switch) causes difficulty in reduction of the operating voltage of a semiconductor integrated circuit.

In the Vpp generator, the charge pump output of the Vpp generator is applied to the input of the waveform shaping circuit. However, there is a slight difference in voltage waveform between the charge pump output and the actual output of the Vpp switch. In this sense, the waveform shaping is not accurate. Especially when the Vpp switch has a high capability, the difference in voltage between the

charge pump output and the actual output of the Vpp switch becomes great.

## SUMMARY OF THE INVENTION

An object of the present invention is to solve the above problems. More specifically, it is an object of the present invention to provide a semiconductor integrated circuit or the like having a Vpp switch which can operate with a low power supply voltage to output a high voltage Vpp.

The above objects are achieved by the following aspects of the present invention. According to a first aspect of the present invention, there is provided a semiconductor integrated circuit comprising: an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor capable of electrically writing and erasing data; means for generating a high voltage required to write data into or erase data from the memory cell array; means for selectively supplying the high voltage to a memory cell; and means for controlling the above-described means so as to control operations of writing, reading, and erasing the memory cell array. The means for selectively supplying the high voltage to a memory cell includes a selection transistor, a plurality of charge pump transistors, the drain and the gate of each charge pump transistor being connected to each other, and a plurality of capacitors, wherein the plurality of charge pump transistors and the plurality of capacitors form a multi-stage charge pump.

According to a second aspect of the present invention, there is provided a semiconductor integrated circuit comprising: an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor capable of electrically writing and erasing data; means for generating a high voltage required to write data into or erase data from the memory cell array; means for selectively supplying the high voltage to a memory cell; and means for controlling the above-described means so as to control operations of writing, reading, and erasing data. The means for selectively supplying the high voltage to a memory cell includes a selection transistor, a charge pump transistor, the drain and the gate of the charge pump transistor being connected to each other, and a capacitor, the charge pump transistor and the capacitor forming a charge pump, threshold voltages of the selection transistor and the charge pump transistor being set to different values such that the threshold voltage of the charge pump transistor is lower than the threshold voltage of the selection transistor.

According to a third aspect of the present invention, there is provided a semiconductor integrated circuit comprising: an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor capable of electrically writing and erasing data; means for generating a high voltage required to write data into or erase data from the memory cell array; means for selectively supplying the high voltage to a memory cell; and means for controlling the above-described means so as to control operations of writing, reading, and erasing data. The means for selectively supplying the high voltage to a memory cell includes a selection transistor for performing selection, a plurality of charge pump transistors, the drain and the gate of each charge pump transistor being connected to each other, and a plurality of capacitors, the plurality of charge pump transistors and the plurality of capacitors forming a multi-stage

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charge pump, threshold voltages of the selection transistors and the charge pump transistors being set to different values such that the threshold voltages of the charge pump transistors are lower than the threshold voltages of the selection transistors.

According to a fourth aspect of the present invention, there is provided a semiconductor integrated circuit comprising: an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor capable of electrically writing and erasing data; means for generating a high voltage required to write data into or erase data from the memory cell array; means for selectively supplying the high voltage to a memory cell; means for shaping a waveform of the high voltage so that the high voltage is prevented from rising too quickly; and means for controlling the above-described means so as to control operations of writing, reading, and erasing data. The means for shaping the waveform receiving a high voltage which has passed through the means for selectively supplying the high voltage, the means for shaping the waveform performing the waveform-shaping based on the received high voltage.

According to a fifth aspect of the present invention, there is provided a semiconductor integrated circuit according to the fourth aspect, wherein the means for shaping a waveform includes a dummy circuit of the means for selectively supply the high voltage, the dummy circuit being used only to supply a high voltage to the input of the means for shaping a waveform.

According to a sixth aspect of the present invention, there is provided a semiconductor integrated circuit according to the fourth aspect, wherein the semiconductor integrated circuit further comprises high voltage detection means for detecting the largest of the high voltages which have passed through the means for selectively supplying a high voltage, the high voltage detection means supplying the detected largest high voltage to the input of the means for shaping a waveform.

In the Vpp switch, which acts as means for selectively supplying a high voltage to a memory cell, according to the first aspect of the present invention, there is provided a multi-stage charge pump wherein each stage comprises a capacitor and a transistor whose drain and gate are connected to each other (in a form of diode-connection) so that the charging capability is enhanced, whereby the Vpp switch can operate with a lower power supply voltage Vcc.

In the Vpp switch, which acts as means for selectively supplying a high voltage to a memory cell, according to the second aspect of the present invention, the threshold voltage Vth of a diode-connected charge pump transistor is set to a value lower than the threshold voltage Vth of an on/off selection transistor (in a multi-Vth fashion), such that the threshold voltage of the diode-connected transistor is set to a low value while maintaining the operation capability of the selection transistor, thereby enhancing the charging capability, whereby the Vpp switch can operate with a low power supply voltage Vcc.

In the third aspect of the present invention, the first and second aspects of the present invention are combined such that a Vpp switch, which acts as means for selectively supplying a high voltage to a memory cell, comprises a multi-stage charge pump, and furthermore the threshold voltage Vth of a diode-connected charge pump transistor is set to a value lower than the threshold voltage Vth of an on/off selection transistor, thereby further enhancing the charging-up capability, whereby the Vpp switch can operate with a lower power supply voltage Vcc.

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In the fourth through sixth aspects of the present invention, a slight difference between the voltage generated by a charge pump of high voltage generation means and the output voltage of a Vpp switch, especially a rather large difference occurring when the charging capability of the Vpp switch is enhanced, is suppressed by employing the output of the Vpp switch as a monitoring point of waveform shaping means for preventing the high voltage from rising too quickly, whereby more accurate waveform shaping can be achieved. Especially in the fifth aspect of the present invention, a high voltage generation means includes a dummy Vpp switch which is used only to provide feedback of the high voltage. Furthermore, in the sixth aspect of the present invention, there is provided high voltage detection means for detecting the greatest high voltage among all lines having a Vpp switch in a memory cell array, wherein the detected greatest high voltage is fed back to the input of the waveform shaping means so that waveform shaping is based on the fed-back signal, thereby ensuring that the high voltage may be prevented from rising too quickly.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram illustrating the configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to a first embodiment of the present invention;

FIG. 2 is a circuit diagram illustrating the configuration of a Vpp generator in a semiconductor integrated circuit according to the present invention;

FIG. 3 is a circuit diagram illustrating the configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to a second embodiment of the present invention;

FIG. 4 is a circuit diagram illustrating the configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to a third embodiment of the present invention;

FIG. 5 is a circuit diagram illustrating the configuration of a Vpp generator in a semiconductor integrated circuit according to a fourth embodiment of the present invention;

FIG. 6 is a circuit diagram illustrating the configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to a fifth embodiment of the present invention;

FIG. 7 is a block diagram illustrating a general configuration of a conventional microcomputer having a built-in EEPROM for use in an IC card;

FIG. 8 is a block diagram illustrating a general configuration of the EEPROM of FIG. 7;

FIG. 9A is a cross-sectional view of one memory cell of a memory cell array of the EEPROM of FIG. 8;

FIG. 9B is a circuit diagram illustrating an equivalent circuit of the memory cell of FIG. 9A;

FIG. 10 is a circuit diagram illustrating the configuration of a peripheral portion of the EEPROM memory cell array of FIG. 8;

FIG. 11 is a timing chart illustrating various signals relating to writing operation of an EEPROM;

FIG. 12 is a circuit diagram illustrating the configuration of a Vpp generator of FIG. 7;

FIG. 13A is a schematic diagram illustrating a layout of functional blocks on a semiconductor substrate of a semiconductor integrated circuit for use in a microcomputer having a built-in EEPROM; and

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FIG. 13B is a cross-sectional view of the semiconductor substrate of FIG. 13A taken along line 13B—13B:

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

### EMBODIMENT 1

FIG. 1 is a circuit diagram illustrating a circuit configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to the first aspect of the present invention. Basically, the general configuration of the EEPROM of the semiconductor integrated circuit according to the present invention is the same as that of the EEPROM according to the conventional technique shown in FIG. 8. The general configuration of the semiconductor integrated circuit according to the present invention is also basically the same as that of the integrated circuit according to the conventional circuit shown in FIG. 7 or 13.

In FIG. 1, there are shown Vpp switches 400a–400d, 460e, and 460f which correspond to the conventional Vpp switches 40a–40d, 46e, and 46f, respectively, shown in FIG. 10. The other portion is basically the same as that according to the conventional technique. Since the Vpp switches 400a–400d, 460e, and 460f have the same configuration, the following description will deal with only the Vpp switch 400c.

There is provided a selection transistor M50 responsible for a selection in the operation of selectively supplying a high voltage to a memory cell. There are also provided charge pump transistors M60, M70, and capacitors C40, C50, which form a charge pump consisting of a plurality of stages (two stages, for example). The transistor M60 is diode-connected, and its source is connected to the transistor M70 whose gate and source are directly connected to each other. The source of the transistor M70 is connected to the bit line BL1. A clock signal CLKP2 is applied via the capacitor C50 to the node which connects the transistors M60 and M70, wherein the clock signal CLKP2 has an opposite phase to that of a clock signal CLKP applied to the capacitor C40. The gate of the transistor M50 is connected to the bit line BL1. That is, the Vpp switch of the present embodiment includes a charge pump consisting of a plurality of stages so that enhanced charge pump performance may be obtained.

FIG. 2 illustrates the circuit configuration of the Vpp generator (high voltage generator) 44 for use in the semiconductor integrated circuit according to the present invention (refer to FIG. 8). The Vpp generator 44 differs from the conventional one shown in FIG. 12 in that there are provided additional portions for generating clock signals CLKW2, CLKE2, CLKP2 each having a phase opposite to the phase of respective clock signal CLKW, CLKE, CLKP.

The EEPROM memory cell array includes memory cells MC1, MC2, MC3, and MC4 shown in FIG. 1. The high voltage generation means includes the portion shown in FIG. 2. The means for selectively supplying a high voltage includes the Vpp switches 400a–400d, 460e, and 460f shown in FIG. 1. The control means includes the EEPROM control systems 104 and 105 including portions except for the EEPROM memory cell array and except for the high voltage supplying means of FIG. 1.

The operation of the Vpp switch, which is one of features of the present invention, will be described below taking the Vpp switch 400c of FIG. 1 as an example. In the Vpp switch

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400c, when the column latch 39a has an H level, and the bit signal transfer control signal BTTR is at an H level, the bit line BL1 rises. In this state, if the clock signal CLKP is at an L level, the transistor M50 turns on. As a result, the capacitor C40 is charged by the high voltage Vpp until the transistor M50 turns off. Then, the clock signal CLKP rises, and the opposite-phase clock signal CLKP2 falls, whereby the charges stored in the capacitor C40 are transferred to the capacitor C50 via the transistor M60 until the transistor M60 turns off. When the clock signal CLKP2 then rises, the charges stored in the capacitor C50 flow out into the bit line BL1 via the transistor M70 until the transistor M70 turns off. As a result of this, the potential of the gate of the transistor M50 connected to the bit line BL1 rises, whereby the capacitor C40 is further charged by the high voltage Vpp until the transistor M50 turns off.

In the above operation, the clock signals CLKP and CLKP2 having an amplitude equal to Vcc raise the voltage via the capacitors C40 and C50, and voltage loss occurs due to the threshold voltages Vth of the transistors M50, M60, and M70. From the above rough estimation, it can be seen that the high voltage Vpp can appear at the output of the Vpp switch when  $2 V_{cc} > 3 V_{th}$ . Compared to the conventional Vpp switch which can transmit a high voltage when  $V_{cc} > 2 V_{th}$ , the Vpp switch of the present invention can transmit a high voltage with lower power supply voltage. This means that the Vpp switch of the present invention can operate with a lower power supply voltage Vcc.

### EMBODIMENT 2

FIG. 3 is a circuit diagram illustrating a circuit configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to the second aspect of the present invention. In this embodiment, the threshold voltage Vth of the selection transistor of each Vpp switch is set to a value different from that of the charge pump transistor, wherein the threshold voltage Vth of the charge pump transistor is set to a value lower than the threshold voltage Vth of the selection transistor, so that enhanced charge pump performance may be achieved. In FIG. 3, the Vpp switches according to the present embodiment are denoted by reference numerals 410a–410d, 470e, and 470f. The other portions are basically the same as those according to the conventional technique. Since the Vpp switches 410a–410d, 470e, and 470f have the same configuration, only the Vpp switch 410c will be described below.

There is provided a selection transistor M51 responsible for the selection in the operation of selectively supplying a high voltage to a memory cell. There are also provided a charge pump transistor M61 and a capacitor C40, which form a charge pump. The transistor M61 is diode-connected, and its source is connected to the bit line BL1. The threshold voltage Vth of the selection transistor M51 is set to such a value that the selection transistor M51 may completely turn off when the bit line BL1 is at an L level. The threshold voltage Vth of the charge pump transistor M61 is set to a low value so that the capability of transferring the high voltage Vpp to the bit line BL1 may be enhanced.

If the threshold voltage Vth of the selection transistor M51 is set to Vth1, and that of the charge pump transistor M61 is set to Vth2, then it is possible to transfer the high voltage Vpp when  $V_{cc} > V_{th1} + V_{th2}$ . From the above, it can be seen that if the threshold voltage Vth2 of the charge pump transistor M61 is set to a sufficiently low value, then it is possible to operate with a lower power supply voltage Vcc.



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## EMBODIMENT 3

FIG. 4 is a circuit diagram illustrating a circuit configuration of a peripheral portion of an EEPROM memory cell array in a semiconductor integrated circuit according to the third aspect of the present invention. In a Vpp switch of the present embodiment, there is provided a charge pump comprising a plurality of stages (two stages, for example), and furthermore, the threshold voltage  $V_{th}$  of the selection transistor is set to a value different from that of the charge pump transistor, wherein the threshold voltage  $V_{th}$  of the charge pump transistor is set to a value lower than the threshold voltage  $V_{th}$  of the selection transistor, so that further enhanced charge pump performance may be achieved. In FIG. 4, the Vpp switches according to the present embodiment are denoted by reference numerals 420a-420d, 480e, and 480f. The other portions are basically the same as those according to the conventional technique. Since the Vpp switches 420a-420d, 480e, and 480f have the same configuration, only the Vpp switch 420c will be described below.

In this embodiment, transistors M61, M71, and capacitors C40, C50 form a multi-stage (two stage, for example) charge pump, and furthermore, the threshold voltage of the selection transistor M51 is set to a value different from those of the charge pump transistors M61, M71. If the threshold voltage  $V_{th}$  of the selection transistor M51 is set to  $V_{th1}$ , and those of the charge pump transistors M61 and M71 are set to  $V_{th2}$ , then it is possible to transfer the high voltage Vpp when  $2V_{cc} > V_{th1} + 2V_{th2}$ . This means that if the threshold voltages  $V_{th2}$  of the charge pump transistors M61 and M71 are low enough, then it is possible to operate with a lower power supply voltage Vcc.

In embodiments 1 and 3, the charge pump comprises two stages. However, the present invention is not so limited. The charge pump may comprise an arbitrary number of stages.

## EMBODIMENT 4

FIG. 5 illustrates the circuit configuration of a Vpp generator (refer to FIG. 8) in a semiconductor integrated circuit according to the fourth and fifth aspects of the present invention. A waveform shaping circuit 200 acting as waveform shaping means is a circuit which performs waveform shaping of a high voltage waveform so as to prevent the output of the Vpp switch from rising too quickly. In the conventional Vpp generator, as shown in FIG. 12, the waveform shaping is performed based on the feedback signal from the output of the charge pump comprising the transistors M1-M4, M7, and the capacitors C1-C3. However, there is a slight difference in voltage waveform between the charge pump output and the actual output of the Vpp switch. As described above, especially when the charge pump capability of the Vpp switch is enhanced, the difference in voltage between the charge pump output and the actual output of the Vpp switch becomes large. If the output of the Vpp switch is monitored and applied to the input (the capacitor C11) of the waveform shaping circuit 200, then more accurate waveform shaping can be achieved. In view of the above, in the Vpp generator of this embodiment, there is provided a dummy Vpp switch 400 which is a dummy circuit used only for providing an input signal to the waveform shaping circuit 200, thereby achieving more accurate waveform shaping.

## EMBODIMENT 5

FIG. 6 is a circuit diagram illustrating a circuit configuration of a peripheral portion of an EEPROM memory cell

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array in a semiconductor integrated circuit according to the sixth aspect of the present invention. As the fourth embodiment, this embodiment can also provide more accurate waveform shaping. In this embodiment, instead of a dummy Vpp switch, there are provided output detection transistors T101-T106 (high voltage detection means) as shown in FIG. 6, wherein all bit lines BL1, BL2 extending in the memory cell array in the vertical direction, all control gate lines CGL1, CGL2 (four lines in the case of FIG. 6), and all word lines WL1, WL2 (six lines in the case of FIG. 6) have their own detection transistor for detecting the output of a Vpp switch connected to the respective lines. These output detection transistors T101-T106 are connected in parallel so that the highest output of the detected outputs may be employed as a detection output 500 which is supplied to the input of the waveform shaping circuit 200 (via the capacitor C11) instead of the output of the dummy Vpp switch. With this arrangement, the output of a Vpp switch which generates the highest output is fed back. Waveform shaping is performed based on this fed-back signal, thereby ensuring that quick rising of the high voltage may be suppressed.

As described above, in the Vpp switch acting as means for selectively supplying a high voltage to a memory cell according to the first aspect of the present invention, there is provided a multi-stage charge pump wherein each stage comprises a capacitor and a transistor whose drain and gate are connected so that the charging capability is enhanced, whereby the high voltage Vpp may be transferred with a lower power supply voltage Vcc. Thus, the first aspect of the present invention provides a semiconductor integrated circuit which can operate with a lower power supply voltage Vcc.

In the Vpp switch acting as means for selectively supplying a high voltage to a memory cell, according to the second aspect of the present invention, the threshold voltage  $V_{th}$  of a diode-connected charge pump transistor is set to a value lower than the threshold voltage  $V_{th}$  of an on/off selection transistor, such that the threshold voltage of the diode-connected transistor is set to a low value while maintaining the operation capability of the selection transistor, thereby increasing the charging capability. As a result, the high voltage Vpp can be transferred with a lower power supply voltage Vcc. Thus, the second aspect of the present invention provides a semiconductor integrated circuit which can operate with a lower power supply voltage Vcc.

In the third aspect of the present invention, the first and second aspects of the present invention are combined such that a Vpp switch, acting as means for selectively supplying a high voltage to a memory cell, comprises a multi-stage charge pump, and furthermore the threshold voltage  $V_{th}$  of a diode-connected charge pump transistor is set to a value lower than the threshold voltage  $V_{th}$  of an on/off selection transistor, thereby further enhancing the charging capability. Thus, the third aspect of the present invention provides a semiconductor integrated circuit which can operate with a lower power supply voltage Vcc.

In the fourth through sixth aspects of the present invention, a slight difference between the voltage generated by a charge pump of high voltage generation means and the output voltage of a Vpp switch, especially a rather large difference occurring when the charging-up capability of the Vpp switch is enhanced, is suppressed by employing the output of the Vpp switch as a monitoring point of waveform shaping means for preventing the high voltage from rising too quickly, whereby more accurate waveform shaping can be achieved. Thus, these aspects of the present invention provide a semiconductor integrated circuit having higher reliability.

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Especially in the fifth aspect of the present invention, the above purposes may be readily achieved simply by adding a dummy Vpp switch to high voltage generation means, wherein the dummy Vpp switch is used only to provide feedback of the high voltage.

In the sixth aspect of the present invention, there is provided high voltage detection means for detecting the highest voltage of all lines having a Vpp switch in a memory cell array, wherein the detected voltage is fed back to the input of waveform shaping means so that waveform shaping may be done based on the fed-back signal, thereby ensuring that the high voltage is prevented from rising too quickly. Thus, the sixth aspect of the present invention provides a semiconductor integrated circuit having higher reliability.

What is claimed is:

1. A semiconductor integrated circuit comprising:

an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor for electrically writing and erasing data;

means for generating a high voltage required to write data into and erase data from said memory cell array;

means for selectively supplying the high voltage to a memory cell; and

means for controlling said means for generating and said means for selectively supplying to control writing data into, reading data from, and erasing data from the memory cell array, said means for selectively supplying the high voltage to a memory cell including a plurality of switches, each switch having:

a selection transistor;

a plurality of charge pump transistors, each charge pump transistor having a drain and a gate connected to each other, at least one of the charge pump transistors being connected to said selection transistor; and

a plurality of capacitors, wherein said plurality of charge pump transistors and said plurality of capacitors form a multi-stage charge pump.

2. A semiconductor integrated circuit comprising:

an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor for electrically writing and erasing data;

means for generating a high voltage required to write data into and erase data from said memory cell array;

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means for selectively supplying the high voltage to a memory cell; and

means for controlling said means for generating and said means for selectively supplying to control writing data into, reading data from, and erasing data from the memory cell array, said means for selectively supplying the high voltage to a memory cell including:

a selection transistor;

a charge pump transistor having a drain and a gate connected to each other; and

a capacitor, said charge pump transistor and said capacitor forming a charge pump, said selection transistor being coupled to the charge pump, threshold voltages of said selection transistor and said charge pump transistor being different, with the threshold voltage of said charge pump transistor being lower than the threshold voltage of said selection transistor.

3. A semiconductor integrated circuit comprising:

an EEPROM memory cell array comprising a plurality of memory cells disposed in a matrix, each memory cell including a non-volatile memory transistor for electrically writing and erasing data;

means for generating a high voltage required to write data into and erase data from said memory cell array;

means for selectively supplying the high voltage to a memory cell; and

means for controlling said means for generating and said means for selectively supplying to control writing data into, reading data from, and erasing data from the memory cell array, said means for selectively supplying the high voltage to a memory cell including:

a selection transistor;

a plurality of charge pump transistors, each charge pump transistor having a drain and a gate connected to each other, at least one charge pump transistor being connected to said selection transistor; and

a plurality of capacitors, said plurality of charge pump transistors and said plurality of capacitors forming a multi-stage charge pump, threshold voltages of said selection transistors and said charge pump transistors being different, with the threshold voltages of said charge pump transistors being lower than the threshold voltages of said selection transistors.

\* \* \* \* \*





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**United States Patent** [19][11] **Patent Number:** **5,553,021****Kubono et al.**[45] **Date of Patent:** **Sep. 3, 1996**

[54] **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A VOLTAGE GENERATOR FOR PROVIDING DESIRED INTERVAL INTERNAL VOLTAGES**

[75] **Inventors:** Shooji Kubono, Akishima; Hitoshi Kume, Musashino, both of Japan

[73] **Assignees:** Hitachi, Ltd.; Hitachi ULSI Engineering Corp., both of Tokyo, Japan

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[52] **U.S. Cl.** ..... 365/185.33; 365/206

[58] **Field of Search** ..... 365/185.33, 226, 365/201; 327/536, 537

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,628,487 12/1986 Smayling ..... 365/185

4,694,314 9/1987 Terada ..... 365/185

5,077,518 12/1991 Han ..... 327/537

*Primary Examiner*—A. Zarabian

*Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus

[57] **ABSTRACT**

A semiconductor integrated circuit is provided which includes a charge pump circuit for forming a step-up (boost) voltage higher than a desired internal voltage, a voltage dividing circuit which forms a plurality of divided voltages based on a reference voltage, and a control circuit which intermittently operates the charge pump circuit so that an output voltage of the charge pump circuit provides the desired internal voltage obtained by adding a voltage obtained by multiplying a particular voltage among the plurality of divided voltages by  $n$  to a predetermined divided voltage.

**12 Claims, 14 Drawing Sheets**

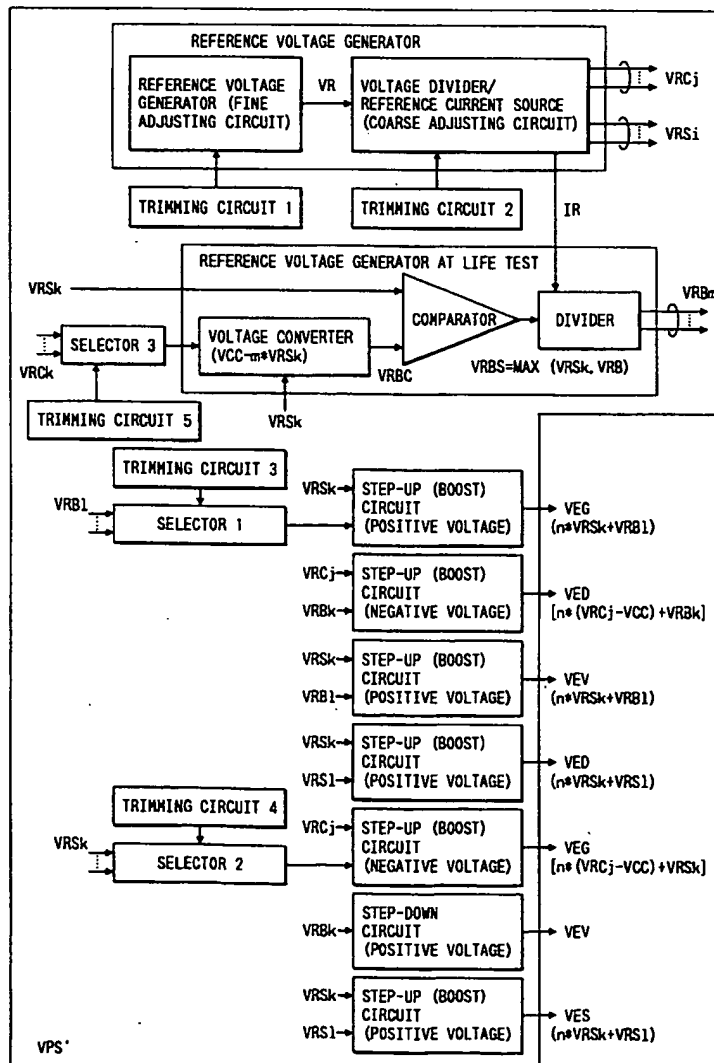


FIG. 1

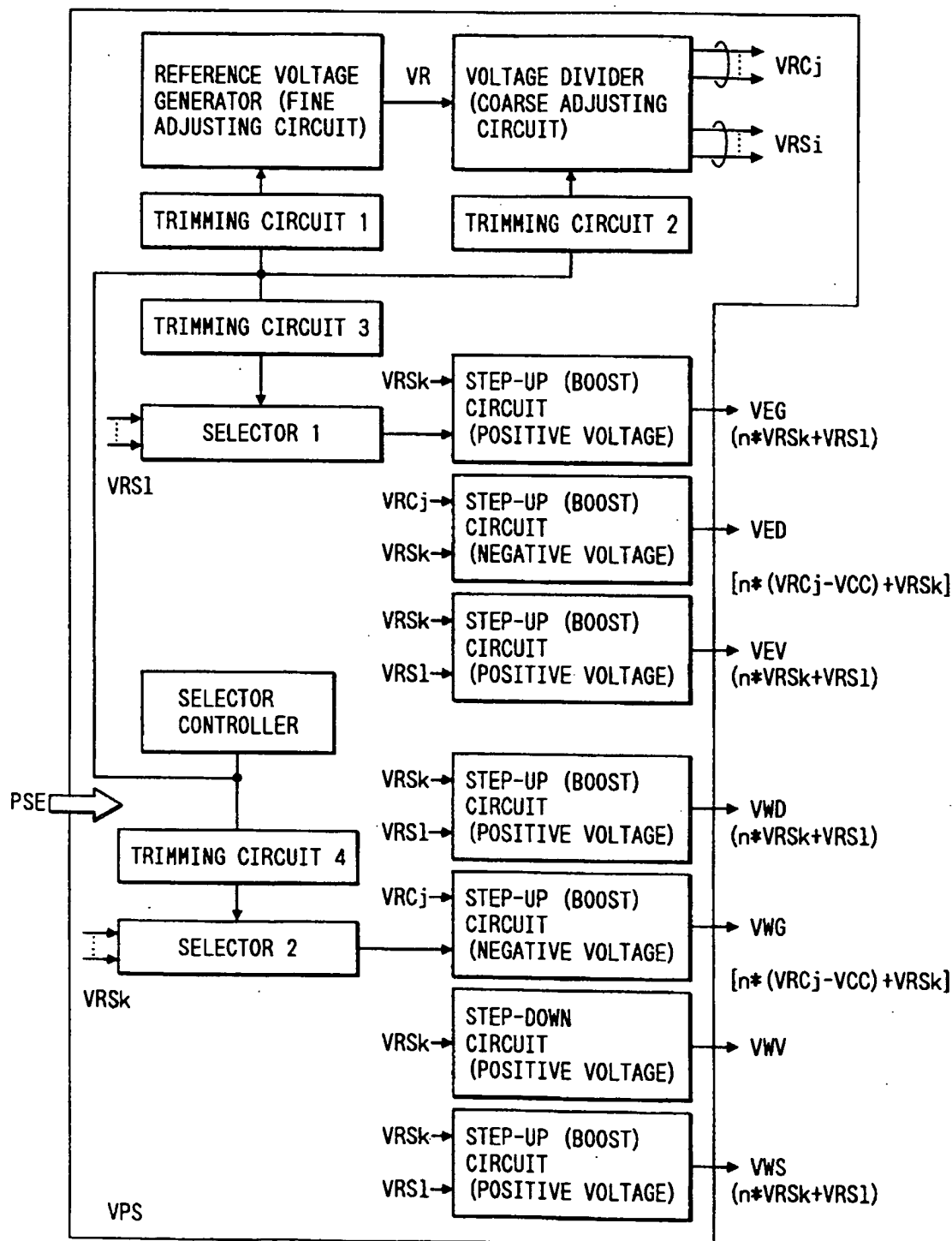
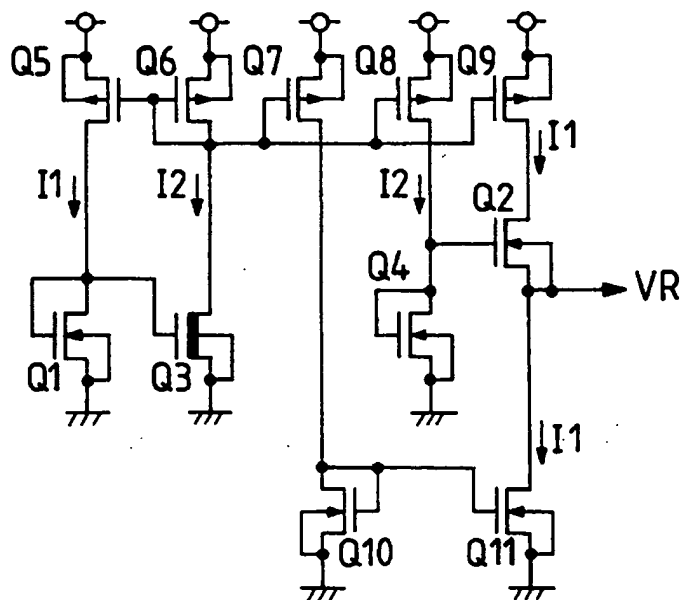


FIG. 2



**FIG. 3**

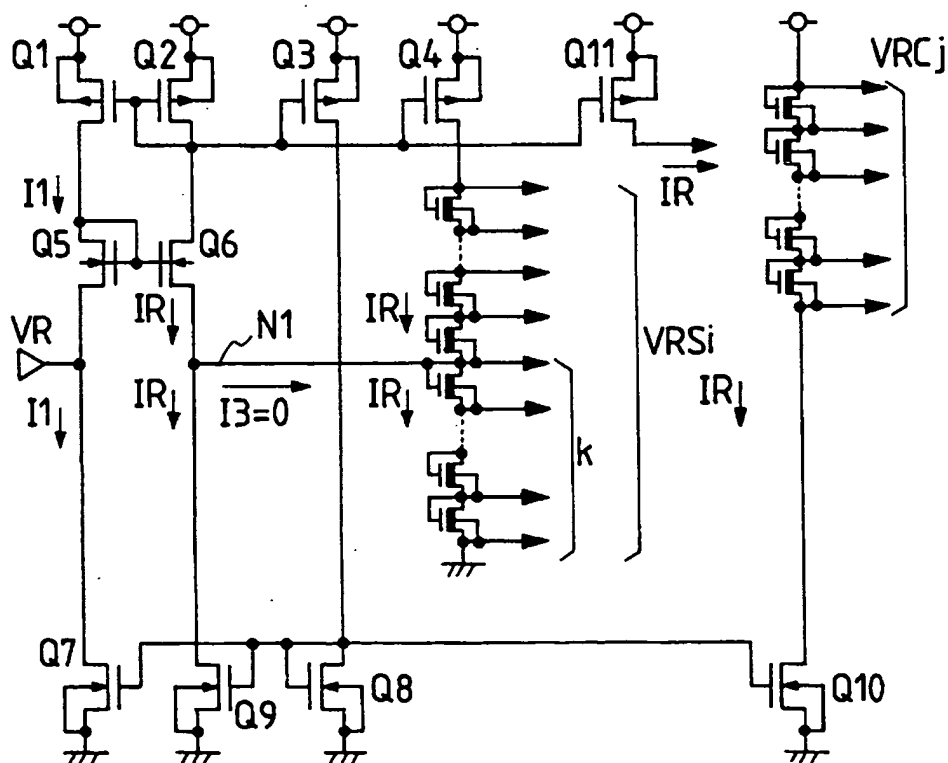


FIG. 4

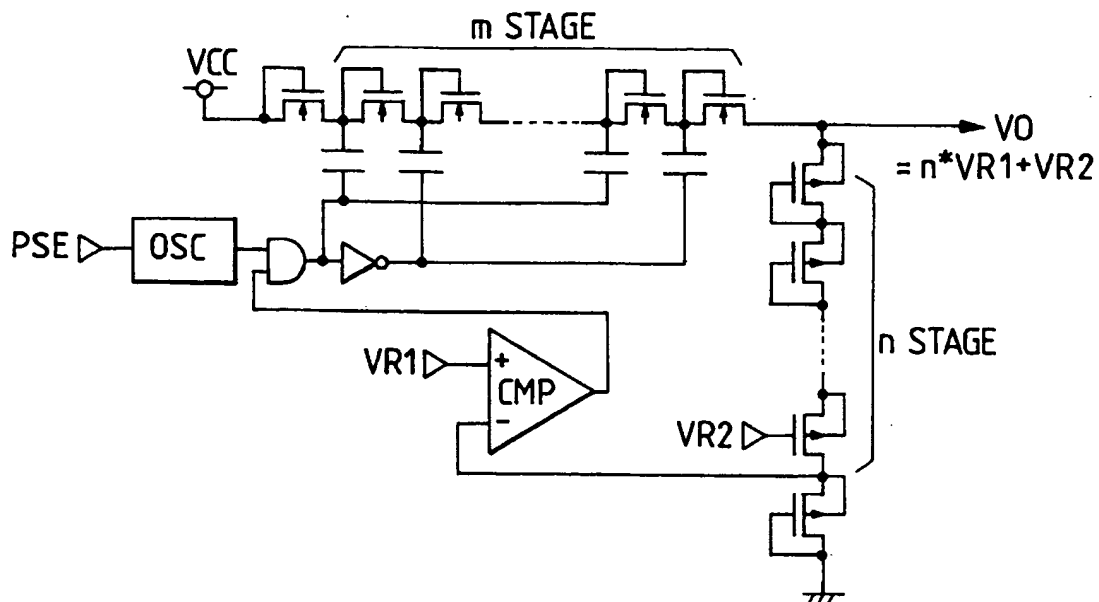


FIG. 5

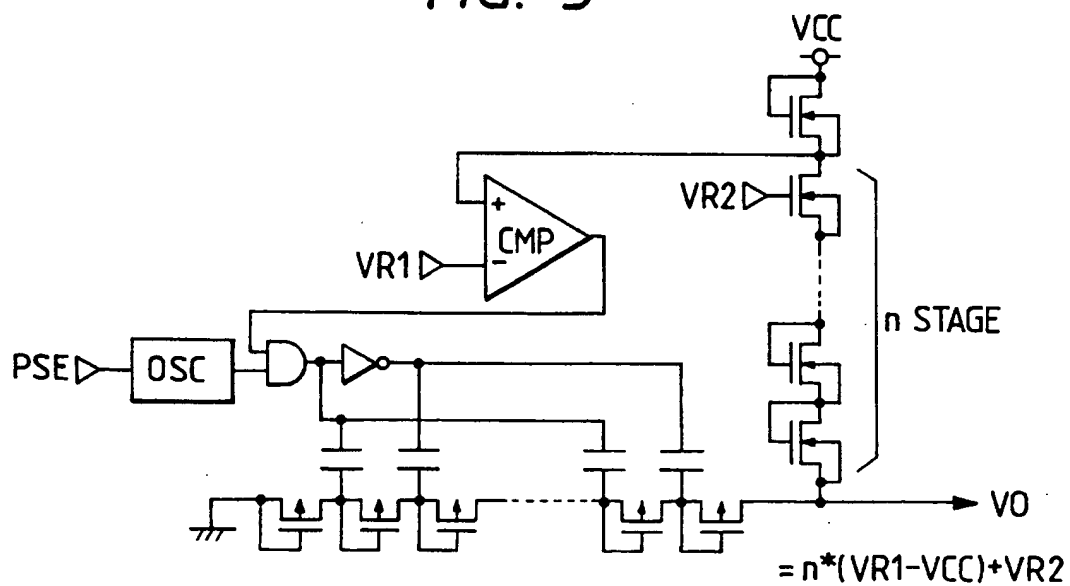


FIG. 6

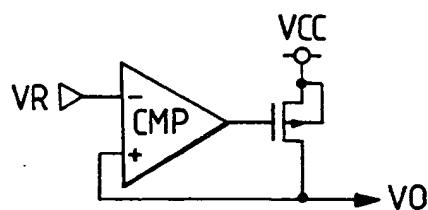
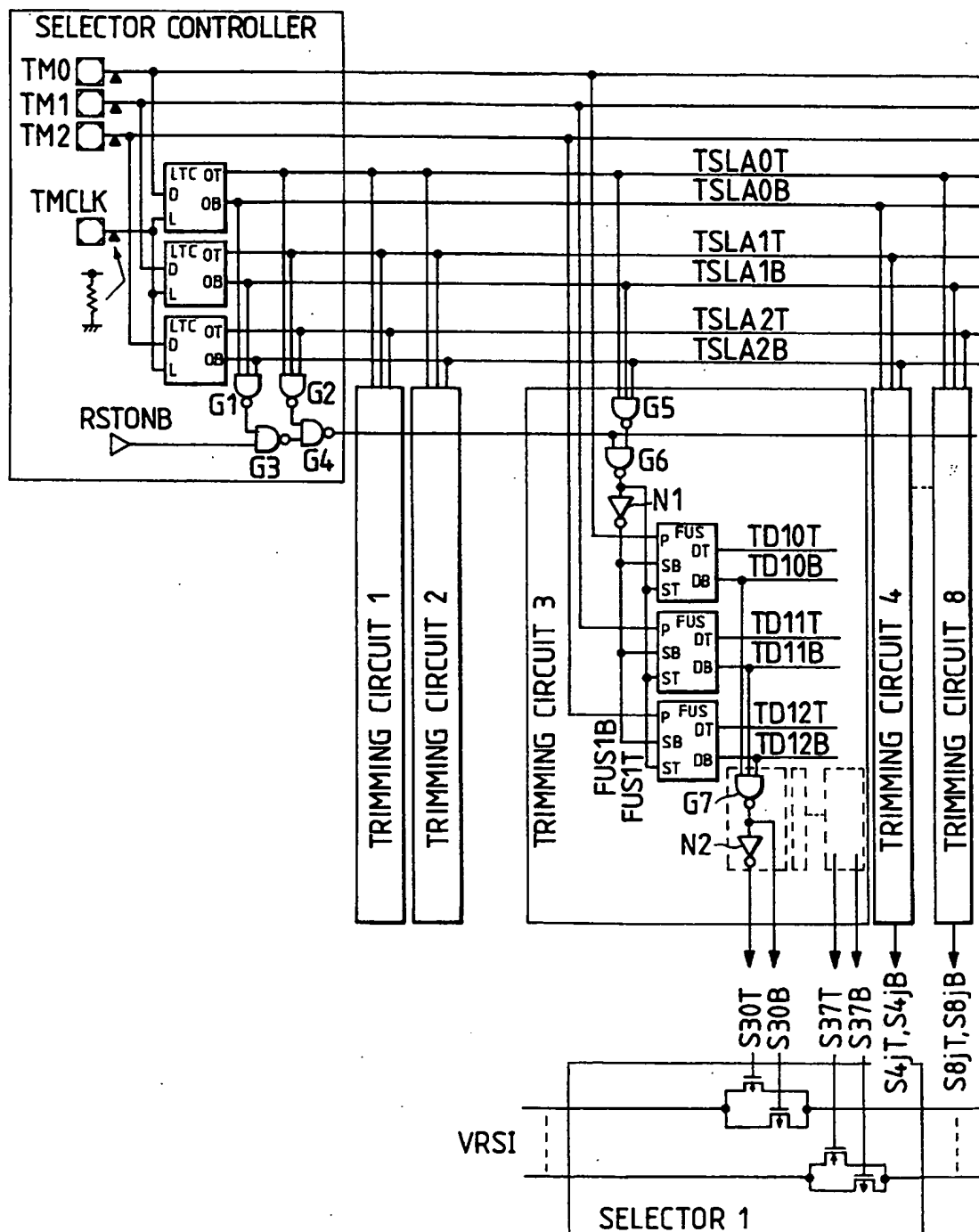


FIG. 7



*FIG. 8*

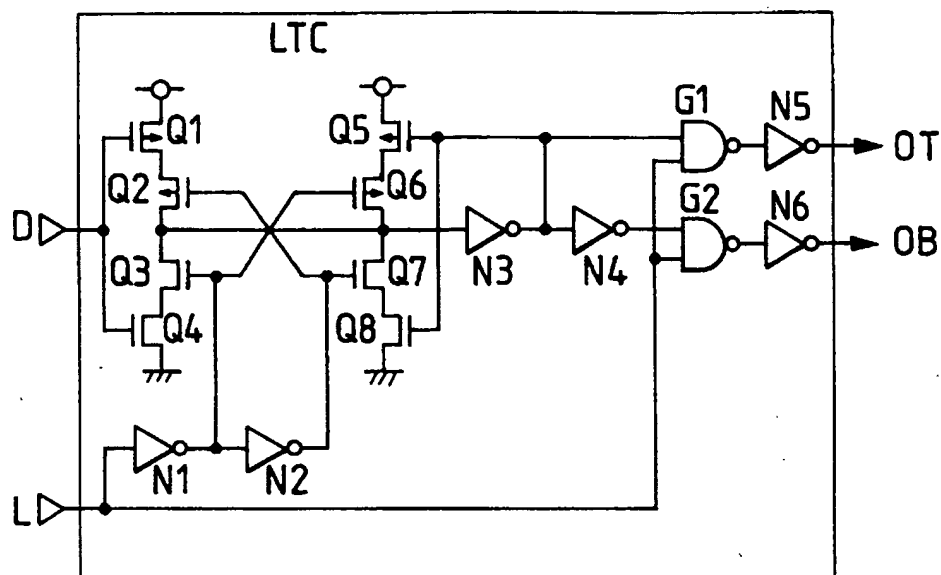


FIG. 9

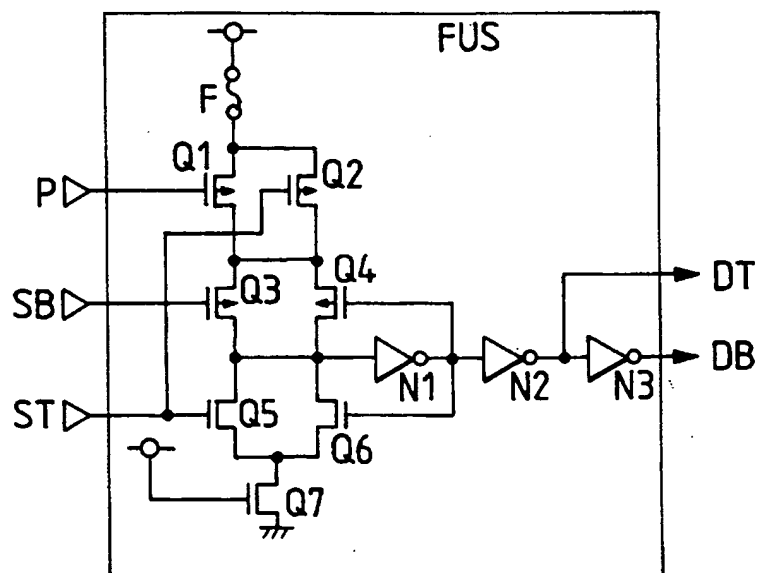


FIG. 10

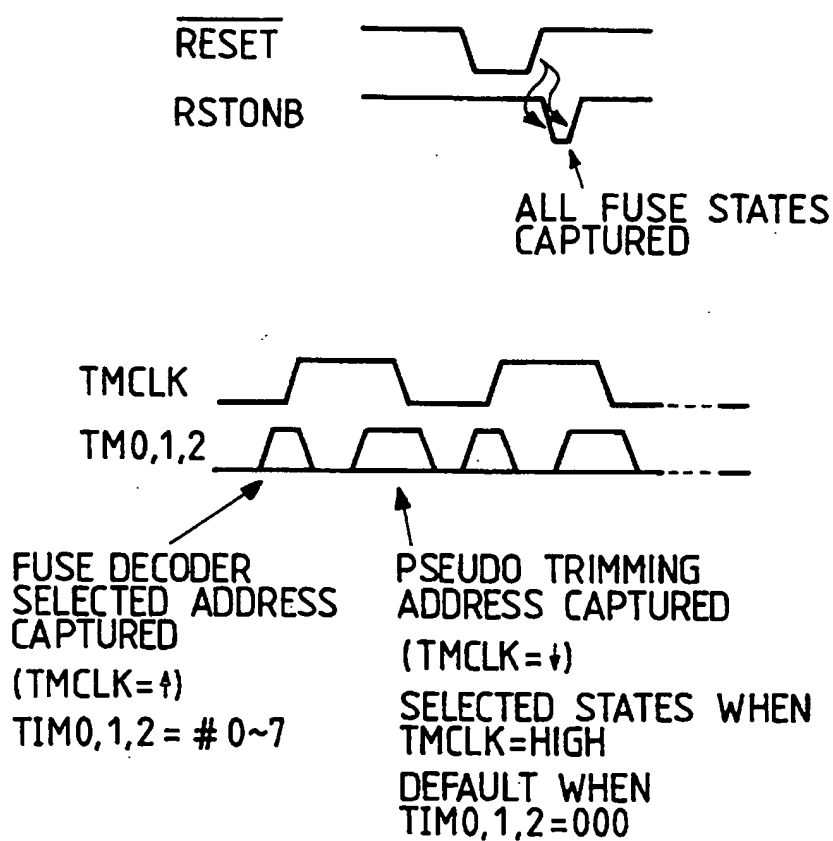


FIG. 11

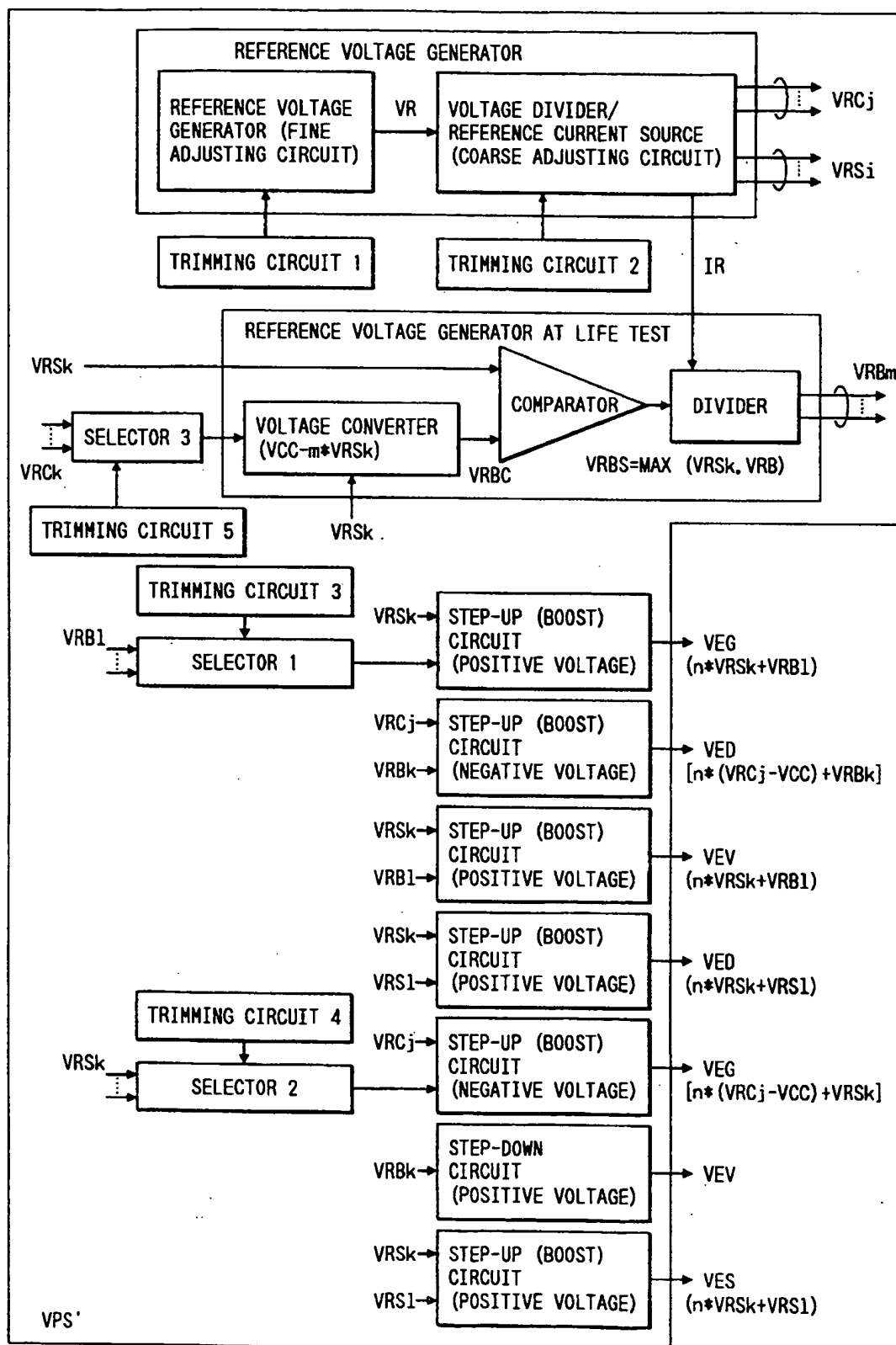




FIG. 12

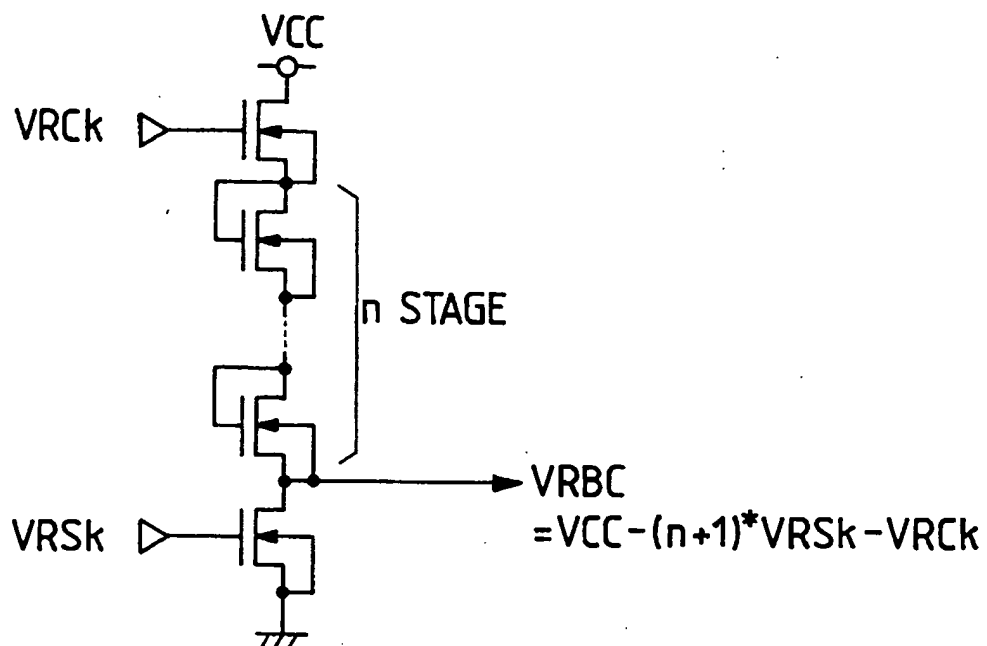


FIG. 13

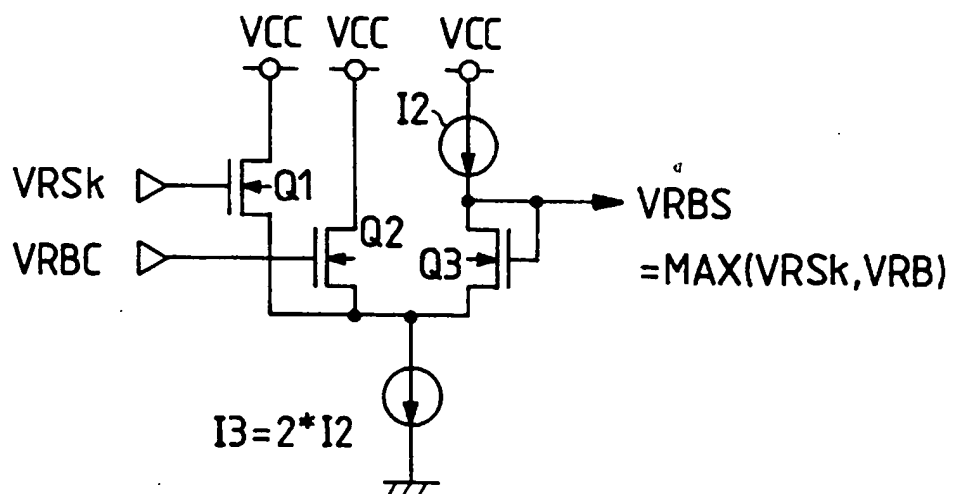


FIG. 14

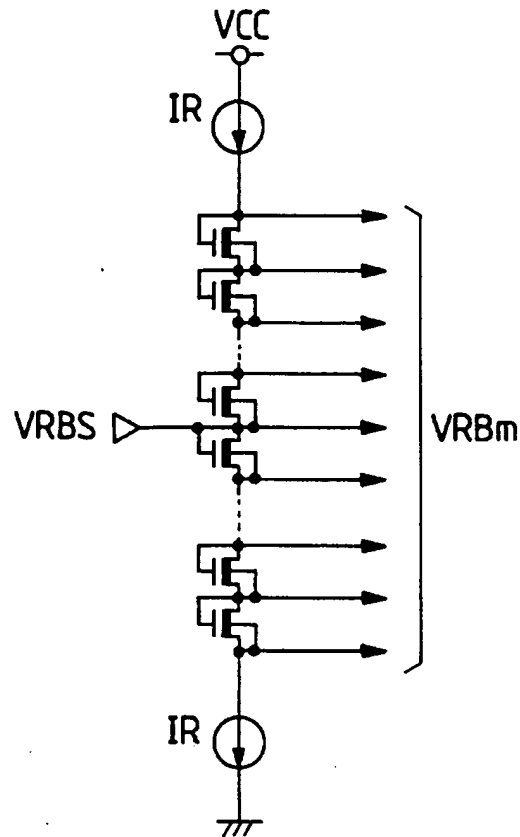


FIG. 15(A)

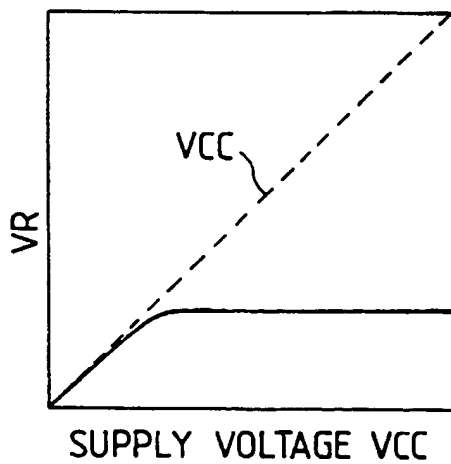


FIG. 15(B)

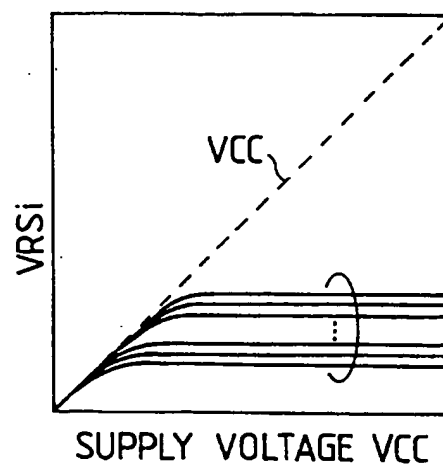


FIG. 16

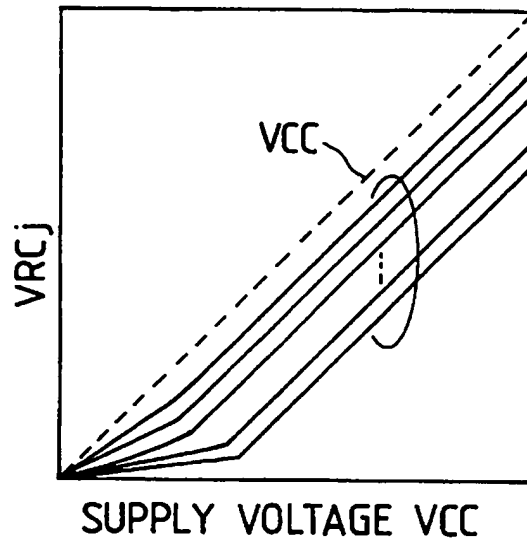


FIG. 17(A)

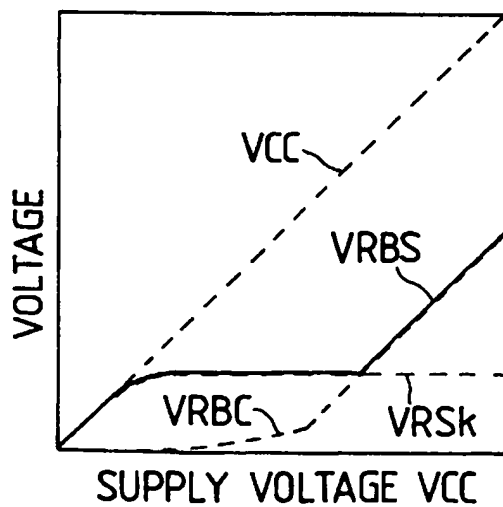


FIG. 17(B)

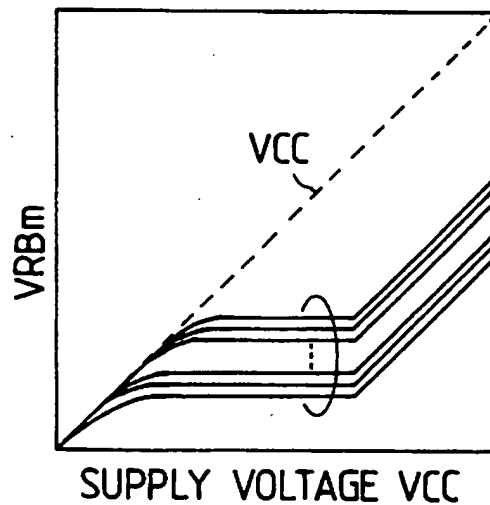


FIG. 18

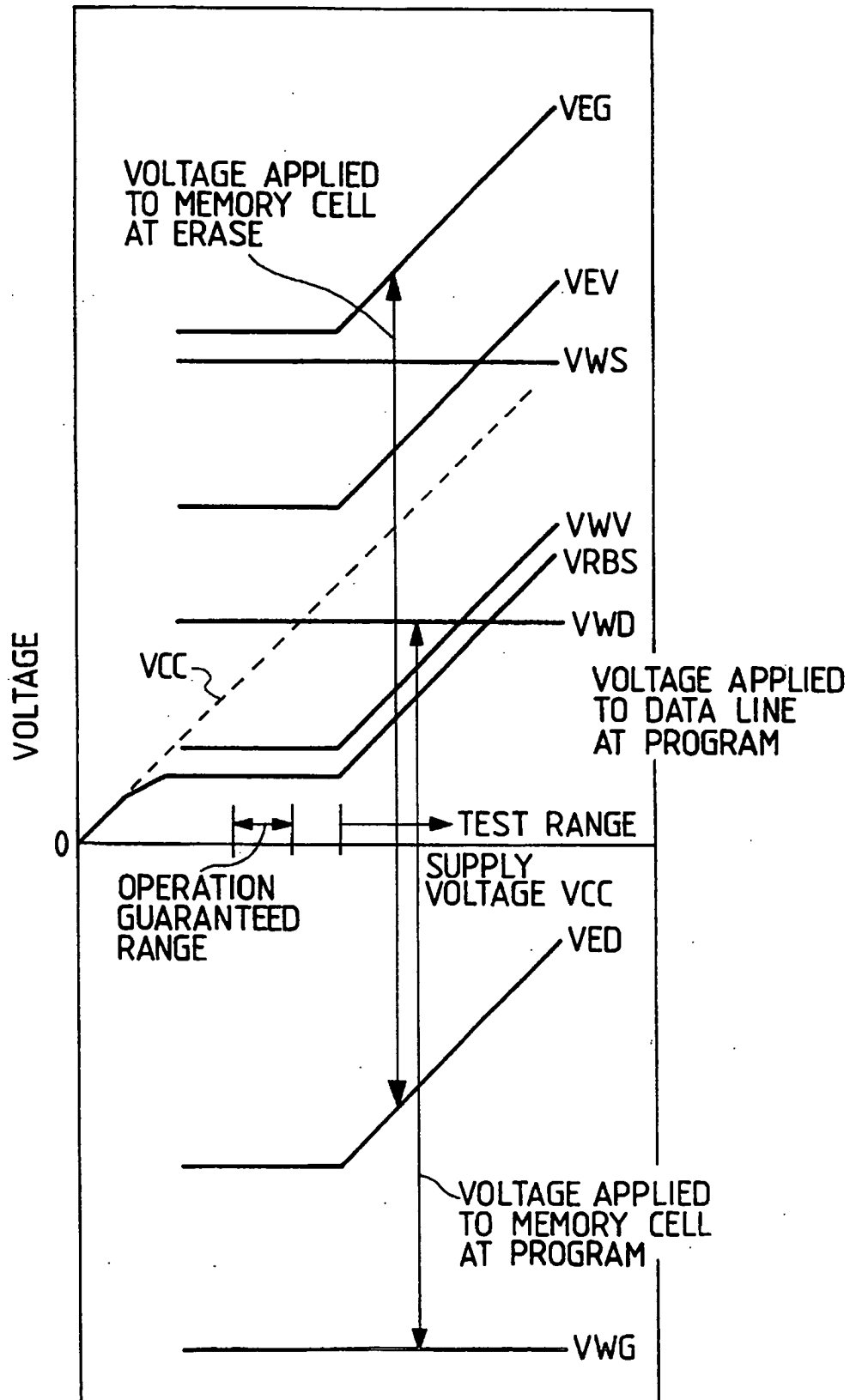
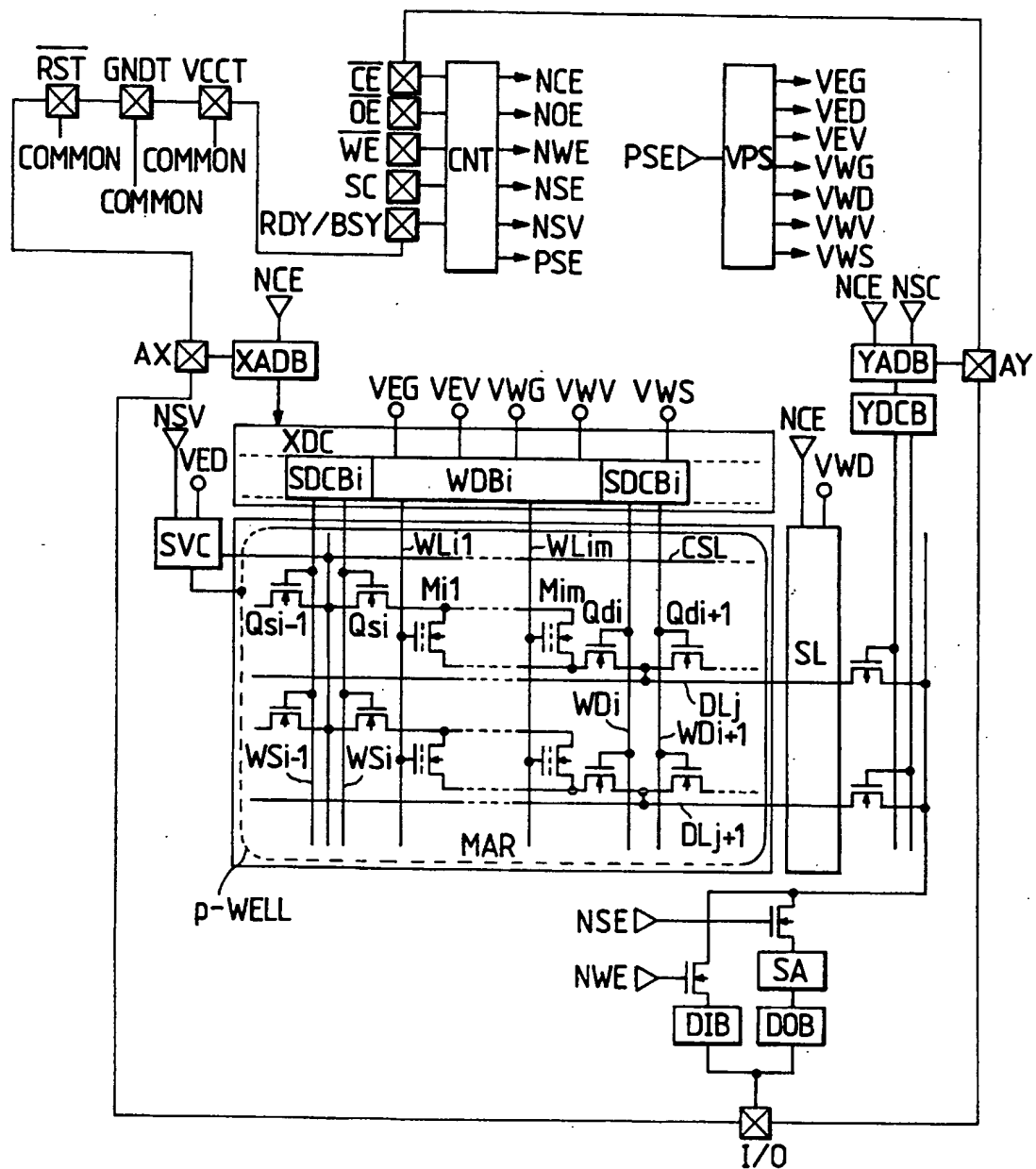
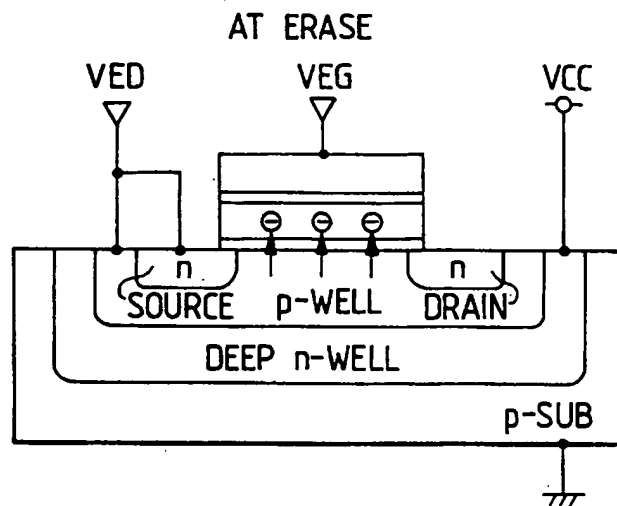
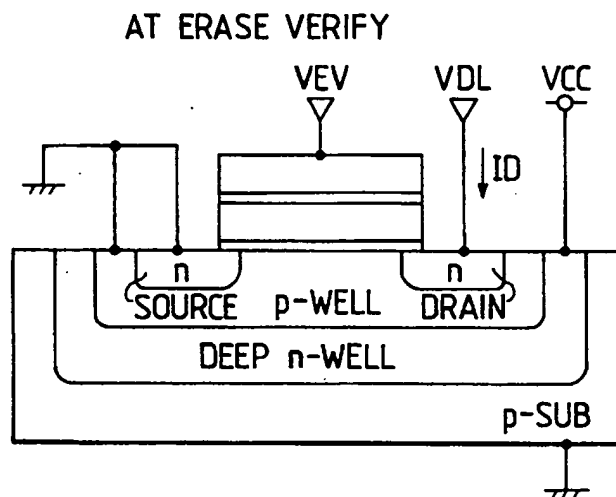
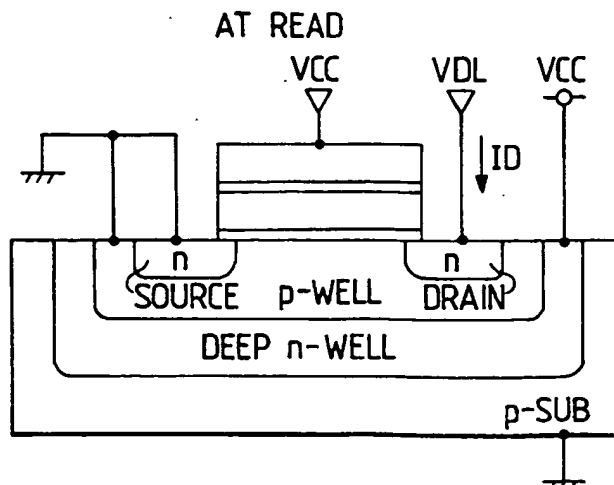


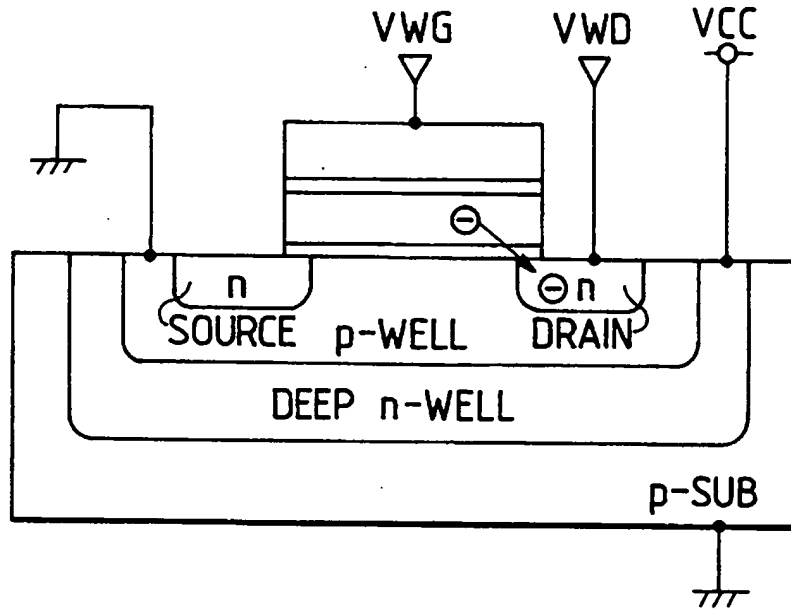
FIG. 19



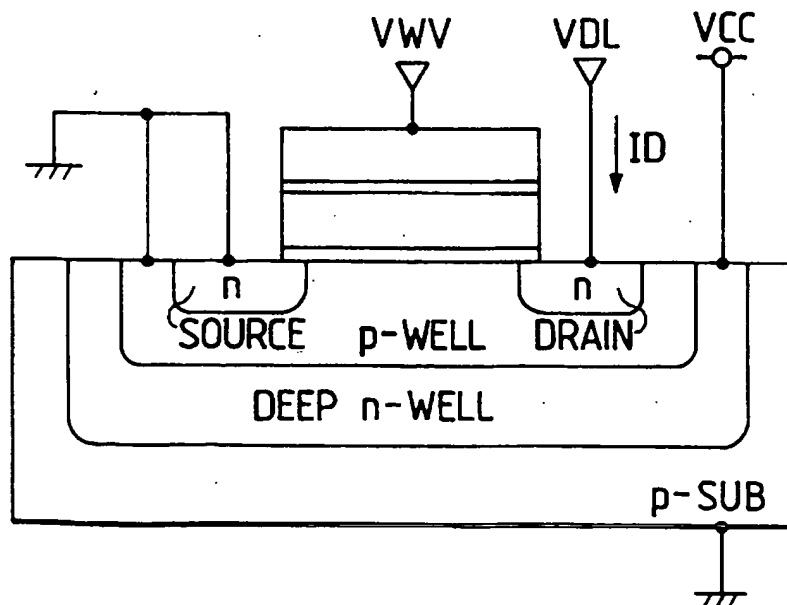
*FIG. 20(A)**FIG. 20(B)**FIG. 20(C)*

*FIG. 21(A)*

AT PROGRAM

*FIG. 21(B)*

AT PROGRAM VERIFY



# SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING A VOLTAGE GENERATOR FOR PROVIDING DESIRED INTERVAL INTERNAL VOLTAGES

## BACKGROUND OF THE INVENTION

This invention relates to a semiconductor integrated circuit device and, more particularly, to a technique effective for use in a semiconductor integrated circuit device such as a collectively erasable nonvolatile memory device (flash EEPROM (Electrically Erasable And Programmable Read-Only Memory)) having internal voltages of a plurality of types.

The flash EEPROM is a nonvolatile memory device having a capability of electrically erasing all of the memory cells of an array or only a selected block of the memory cells formed on a chip at a time. Such a flash EEPROM is described in "IEEE International Solid-State Circuits Conference," pp. 152 and 153, 1980 and "IEEE International Solid-State Circuits Conference," pp. 76 and 77, 1987, and "IEEE, J. Solid-State Circuits," Vol 23, pp. 1157 to 1163, 1988, for example.

## SUMMARY OF THE INVENTION

We have developed a memory transistor having a control gate and a floating gate in which a program operation is also performed by a tunnel current and, contrary to a conventional memory transistor, a charge is injected into the floating gate to raise a threshold voltage over a select level of a word line for an erase operation. In this novel constitution, for the erase operation for the memory transistor, the threshold voltage is higher than the word line select level. Therefore, unlike the conventional memory transistor in which the charge of the floating gate is pulled out into a substrate side to lower the threshold voltage, the novel memory transistor protects other memory cells from being made unreadable by an excess erasure that puts the transistor in the depletion mode, turning on the word line although it is at the deselected level.

However, for a memory transistor such as the novel memory transistor in which a program operation is performed by the tunnel current, it is necessary to minimize the voltage which is applied to a drain of the memory transistor at a read operation, thereby preventing an erroneous erasure from being caused by the tunnel current generated by the read operation. Thus, the memory transistor in which the program operation is performed by the tunnel current requires setting an operating voltage with precision. This in turn requires a circuit for forming many types of voltages on a semiconductor integrated circuit.

It is therefore an object of the present invention to provide a semiconductor integrated circuit device having a power supply circuit capable of forming internal voltages of a plurality of types with precision and high efficiency.

It is another object of the present invention to provide a semiconductor integrated circuit device having a flash non-volatile memory circuit permitting efficient program and erase operations.

The above and other objects, features and advantages of the present invention will become more apparent from the accompanying drawings, in which like reference numerals are used to identify the same or similar parts in several views.

In carrying out the invention and according to one aspect thereof, there is provided a semiconductor integrated circuit device having a power supply circuit comprising a charge pump circuit for forming a step-up (boost) voltage by a desired internal voltage, a voltage dividing circuit for forming divided voltages of a plurality of types based on a reference voltage, and a controlling circuit for intermittently operating the charge pump circuit such that an output voltage of the charge pump circuit becomes a voltage obtained by multiplying a particular voltage among the divided voltages by  $n$  and becomes a desired internal voltage obtained by adding predetermined divided voltages.

According to the above-mentioned constitution, a voltage obtained by multiplying the reference voltage by  $n$  is combined with a fine-adjusting voltage formed by dividing the obtained voltage, thereby efficiently forming a stable, desired voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a voltage generator practiced as one preferred embodiment of the invention;

FIG. 2 is a circuit diagram illustrating a reference voltage generator of FIG. 1 practiced as one preferred embodiment of the invention;

FIG. 3 is a circuit diagram illustrating a voltage divider of FIG. 1 practiced as one preferred embodiment of the invention;

FIG. 4 is a circuit diagram illustrating a power supply circuit of FIG. 1 practiced as one preferred embodiment of the invention;

FIG. 5 is a circuit diagram illustrating the power supply circuit of FIG. 1 practiced as another embodiment of the invention;

FIG. 6 is a circuit diagram illustrating the power supply circuit of FIG. 1 practiced as still another embodiment of the invention;

FIG. 7 is a circuit diagram illustrating a selector control circuit, trimming circuits, and a selector circuit practiced as one preferred embodiment of the invention;

FIG. 8 is a circuit diagram illustrating a latch circuit of FIG. 7 practiced as one preferred embodiment of the invention;

FIG. 9 is a circuit diagram illustrating a fuse circuit of FIG. 7 practiced as one preferred embodiment of the invention;

FIG. 10 is a timing chart describing operations of the circuits of FIG. 7;

FIG. 11 is a block diagram illustrating the voltage generator associated with the invention and practiced as another preferred embodiment thereof;

FIG. 12 is a circuit diagram illustrating a voltage converter of FIG. 11 practiced as one preferred embodiment of the invention;

FIG. 13 is a circuit diagram illustrating a comparator of FIG. 11 practiced as one preferred embodiment of the invention;

FIG. 14 is a circuit diagram illustrating a voltage divider of FIG. 11 practiced as one preferred embodiment of the invention;

FIG. 15 (A) and (B) are voltage characteristics diagrams for describing the invention;

FIG. 16 is another voltage characteristics diagram for describing the invention;



FIG. 17 (A) and (B) are other voltage characteristics diagrams for describing the invention;

FIG. 18 is a voltage characteristics diagram for describing operations of the flash memory associated with the invention;

FIG. 19 is a block diagram illustrating a collectively erasable nonvolatile memory device associated with the invention and practiced as one embodiment of the invention;

FIG. 20 (A), (B) and (C) are sectional views describing operations of the collectively erasable nonvolatile memory device of FIG. 19; and

FIG. 21 (A) and (B) are sectional views describing operations of another memory transistor of FIG. 19.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

This invention will be described in further detail by way of example with reference to the accompanying drawings.

FIG. 19 shows the block diagram illustrating collectively erasable nonvolatile memory device (hereinafter referred to as a flash memory) associated with the invention and practiced as one preferred embodiment thereof. For easier understanding of the invention, a memory array portion MAR is illustrated typically in a constitution of a plurality of memory cells. Each of the circuit blocks and each of the circuit elements of FIG. 19 are formed on a single semiconductor substrate such as a single silicon crystal by means of known semiconductor integrated circuit manufacturing techniques.

The flash memory according to the present invention has two power supply terminals VCCT and GNDT. The terminal GNDT is supplied with a circuit reference voltage GND (0 V for example), while the terminal VCCT is supplied with a supply voltage VCC (3 V for example) higher than the circuit reference voltage. The flash memory according to the present invention, based on the above-mentioned two voltages VCC and GND, generates internal voltages of a plurality of types with precision.

In FIG. 19, an X-address signal AX is entered in an X-address buffer XADB. The address signal captured in the X-address buffer XADB is interpreted by an X decoder SDC. Word lines W1l through W1m are selected by a word line select driver WDBi provided for each block composed of m memory cells. A drain common to memory cells Mil through Mim of the above-mentioned block is connected to a data line Dlj via a select MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) Qdi. A source common to the memory cells Mil through Mim of the block is connected to a common source line CSL via select MOSFET Qsi. The select MOSFET Qdi and Qsi are supplied with a select signal by a main word line select driver SDCBi.

Because potentials of the main word line Wdi to be connected to a gate of the select MOSFET and potentials of the word line W1l through W1m to be connected to a control gate of the memory cells are different for program, erase, and read operations, the word line select driver WDBi has output circuits for putting out select/deselect levels of voltages corresponding to the operation modes.

In the memory array MAR, a memory cell is provided at an intersection between each word line and each data line as mentioned above. However, the data line Dlj is connected to the drain of the plurality of memory cells Mil through Mim via the select MOSFET Qdi. Likewise, the source of the memory cells Mil through Mim constituting one block is

connected to the source line CSL via the select MOSFET Qsi.

The data line is connected to a sense latch SL. The sense latch SL senses a high level or a low level of the data line and latches the data line to a sensed level. For a sense amplifier for the sense latch SL, a circuit generally similar to a CMOS sense amplifier such as used for a known dynamic RAM is used, but the invention is not limited thereto. Namely, the sense amplifier for the latch SL is composed of a pair of CMOS inverters with their inputs and outputs cross-connected and a power switch for supplying an operating voltage and a ground voltage to the plurality of CMOS inverters.

The sense latch SL is also used as a register for holding program data. Namely, the sense latch is connected to an input/output line via a column switch and, in a read operation, data selected by the column switch is sent via the input/output line to a serial amplifier SA and data output circuit DOB to be outputted from an input/output terminal I/O. In a program operation, program data serially entered from the input/output terminal I/O is sent to the input/output line via an input buffer DIB to be captured in the sense latch SL via the column switch, the latch SL operating as a latch circuit corresponding to the data line. When the data have all been captured, the captured data are sent to corresponding data lines simultaneously for the program operation.

The column switch is interpreted by a Y decoder YDCB that receives an output signal of a Y address buffer YADB that receives a Y address signal AY. An input/output node of the sense amplifier is connected to the input/output line by a select signal formed by the Y decoder. A column decoder has an address counter to which an initial value is set by the Y address signal AY, but the invention is not limited thereto. The address counter counts a serial clock SC to generate a continuous Y address, thereby forming a column switch select signal. The program data to be serially entered is entered in synchronization with the above-mentioned serial clock, and read data to be serially outputted is outputted in synchronization with the serial clock.

A controller CNT receives a chip enable signal /CE (it should be noted herein that a slash "/" before a signal name indicates that the signal is an active-low signal, which is conventionally represented by a bar over a signal name; in the accompanying drawing, however, the conventional bar is used for the same purpose), an output enable signal /OE, a program enable signal /WE, and the serial clock SC to generate a variety of timing signals required for internal operations.

In FIG. 19, a voltage generator VPS generates voltages necessary for erasing, writing, and reading the above-mentioned memory cells. That is, the generator VPS supplies voltages VEG, VEV, VWG and VWV to the word line select driver WDBi and a voltage VWS to the main word line select driver SDCBi. Further, the generator VPS supplies a voltage VWD to the sense latch SL and a voltage SVC to a source line voltage supply circuit SVC.

Now, referring to FIGS. 20(A), (B) and (C), there are shown sectional views for describing operations of the flash memory associated with the present invention. FIG. 20 (A) shows an erase state. Here, the flash memory has a stack gate structure with a gate insulation film between a floating gate and a semiconductor substrate made up of a thin oxide film (about 8.5 nm) so that a tunnel current flows through it. For reference, a gate oxide film between the floating gate and a control gate is thicker (about 15 nm) than the above-mentioned gate oxide film. In an erase operation, VEG is

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applied to the control gate and VDE is applied to a source region and the substrate. This generates an electric field high enough for causing the flow of the tunnel current between the substrate and the floating gate, electrons being injected from the substrate side to the floating gate. This turns off the flash memory, in the erase state, for a select level of the word line. Meanwhile, a drain region is opened, the supply voltage VCC is applied to an n-well region that substantially provides a substrate, and the circuit ground GND such as 0 V is applied to an intrinsic substrate p-SUB.

In the memory array MAR of FIG. 19, a plurality of memory cells like Mil through Mim are collected into a single block to make the drain region and the source region common to the memory cells. The select MOSFET Qdi is provided between the common drain region and the data line DLj. The select MOSFET Qdi on the drain region side is turned off when 0 V is applied to the gate in the above-mentioned erase operation. This opens all drain regions of the memory cells Mil through Mim. The select MOSFET Qsi on the source region side is turned on when a high level ("H") is applied to the gate in the erase operation. Therefore, the above-mentioned voltage VED is given between the common source region and the substrate p-well region.

The above-mentioned constitution in which the memory cells are put into blocks, each block being connected to the data line via the select MOSFET and connected to the common source line can reduce a stress to deselected memory cells. That is, a memory cell with the word line selected and the data line deselected or a memory cell with the word line deselected and the data line selected and whose data must be retained is protected, in a program or erase operation, from being applied with the above-mentioned program or erase voltage. In this constitution, the stress is applied only to a small number of memory cells in the block.

In the above-mentioned erase operation, a negative voltage such as the VED (-4 V) is applied to the substrate p-well and the select voltage VEG such as +12 V is supplied to the word line, which makes a collective erase operation on a word line basis. In the above-mentioned embodiment, one word line provides a storage unit such as one sector. One sector consists of 512 bytes, but not limited thereto. Namely, one word line (it should be noted that one word line does not mean physically one line) is connected with  $512 \times 8$ —about 4K memory cells. In this case, if eight memory arrays are provided, since one word line is assigned with 512 memory cells, a word line select operation can be performed at relatively a high speed with a word driver having a comparatively small current drive capacity.

FIG. 20 (B) shows a verify state. The VEV is applied to the control gate, the VCC to the n-well region, and the VDL to the drain. Then, the circuit ground potential is supplied to the source region, the p-well region, and the substrate. If a drain current ID flows for the above-mentioned voltage VEV, its threshold voltage is determined to be lower than the voltage VEV, resulting in an insufficient erase. Therefore, the above-mentioned erase operation of FIG. 20 (A) is performed again to make the threshold voltage in the erase state greater than the VEV.

FIG. 20 (C) shows a read state. The VCC is applied to the control gate and the n-well region and the VDL is applied to the drain. The circuit ground potential is applied to the source region, p-well region, and the substrate. If the drain current ID flows for the voltage VCC, it is determined that the memory cell is in a program state; if not, it is determined that the memory cell is in an erase state. At this moment, the voltage VDL is given to the drain. The VDL is a relatively

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low potential as small as about 1 V, thereby preventing a soft program operation from being performed by the flowing of the tunnel current caused by the read voltage VDL and the select voltage VCC.

FIG. 21 (A) shows a program state. The VWG is applied to the control gate and the FWD is applied to the drain region. When no program operation is performed, 0 V is applied to the drain region. The voltage VWD of the control gate is -9.5 V and the voltage VWD of the drain region is 4.5 V. This generates an electric field high enough for flowing a tunnel current between the floating gate and the drain region, thereby charging electrons from the floating gate to the drain region. The deselected word line is set to the VCC (+3 V); therefore the tunnel current is prevented from being flowing if the drain voltage VWD of the deselected memory cell having the common drain region is given.

FIG. 21 (B) shows a program verify state. The VWV is applied to the control gate and the VDL is applied to the drain region. The circuit ground potential is given to the source region and the p-well region. If the drain current ID does not flow for the above-mentioned VWV, it is determined that its threshold voltage is higher than the voltage VWV, resulting in insufficient programming. Therefore, the program operation of FIG. 21 (A) is performed again to make the threshold voltage in the program state be lower than the VWV. Repeating the program verify operation and the program operation prevents the depletion mode from being caused by an excess programming.

Referring to FIG. 1, there is shown a block diagram illustrating a voltage generator VPS practiced as one preferred embodiment of the invention. This embodiment has a constitution for efficiently forming, with precision, voltages of a variety of types necessary for erasing, writing, and reading the memory cells as mentioned above.

To be more specific, a reference voltage generator generates a precision reference voltage VR (0.7 V for example) corresponding to a MOSFET threshold voltage to be described later. To obtain a desired voltage by correcting a process dispersion of the reference voltage VR, a trimming circuit 1 is provided. The trimming circuit 1 has a fuse to be described later. By selectively connecting, in parallel, MOSFETs forming the reference voltage VR, an equivalent channel width L is adjusted, thereby providing a fine adjustment of the reference voltage VR with an error of  $\pm 1\%$ .

The reference voltage VR is sent to a divider to be divided into a variety of voltages VRCj and VRSi which are positive and negative around the reference voltage VR. Actually, this voltage divider does not divide the reference voltage VR itself but forms the voltages in increments of (0.1 V around the reference voltage VR to be described later. The voltages obtained by the divider are also trimmed by a trimming circuit 2 to be set to voltages in increments of 0.1 V against the process dispersion. The above-mentioned divided voltages VRCj are voltages with the supply voltage VCC used as reference and formed in increments of 0.1 V in a range of -0.1 V to -2.0 V around the VCC. The above-mentioned divided voltages VRSi are formed in increments of 0.1 V in a range of 0.1 V to 2.0 V around the circuit ground potential.

Of the voltages VRSi with the ground potential as a reference voltage, a plurality of voltages VRSi necessary for forming a voltage VEG are entered in a selector 1. The selector 1 selects one voltage specified by a trimming circuit 3 and supplies the selected voltage to a corresponding Step-up (boost) circuit. As will be described, the Step-up (boost) circuit is intermittently operated so that the an output voltage of a charge pump circuit becomes an output voltage

VEG obtained by adding a voltage obtained by multiplying the above-mentioned selected voltage VRSI by  $n$  to a voltage obtained by selecting a VRSk from the above-mentioned voltages VRSi by connection. The selector 1 is used to select the small number of voltages VRSI necessary for forming the above-mentioned VEG from many voltages VRSi formed by the above-mentioned divider, thereby simplifying the circuitry. This constitution forms the selector 1 and the trimming circuit 3 with a minimum number of necessary circuits.

The voltage VED is formed by adding a voltage obtained by multiplying a signal selected from the divided voltages VRCj by  $n$  to a voltage selected from the divided voltages VRSi. The selection of these divided voltages is made by connection. The voltage VEV is also formed by adding the divided voltage VRSk and its  $n \times$  step up voltage to the divided voltage VRSI.

Basically, voltages VWD, VWG, VWV and VWS are also formed by combinations of the above-mentioned divided voltages. However, the divided voltages VRSk used for forming these voltages are voltages specified by the selector 2 from among the plurality of voltages selected from the above-mentioned divided voltages VRSi for simplified circuits. The selector 2 selects one signal by a select signal formed by a trimming circuit 4 and outputs the selected signal.

It will be apparent that the factor  $n$  is different for each voltage to be formed and the VRSk and VRSI selected by connection to be entered in corresponding voltage generators are selected according to corresponding output voltages.

Step-up (boost) circuits and a Step-down circuit for forming voltages VEG, VED, VEV, VWG, VWV and VWS perform step-up and step-down operations based on a select signal PSE supplied from the controller CNT. That is, only a Step-up (boost) circuit or step-down transfer supplied with the select signal PSE performs the step-up or step-down operation.

Referring to FIG. 2, there is shown a circuit diagram of the reference voltage generator of FIG. 1. In the figure, each MOSFET indicated by an arrow pointing in a channel portion at a gate is an n-channel MOSFET, while each MOSFET indicated by an arrow pointing at the opposite direction is a p-channel MOSFET.

A MOSFET Q3 with the pointing arrow blotted black is an n-channel MOSFET in depletion mode. A current I2 that flows through the MOSFET Q3 flows to a p-channel MOSFET Q6 formed in a diode. A mirror current I1 that flows to a p-channel MOSFET Q5 in a current mirror with the p-channel MOSFET Q6 is supplied to an n-channel MOSFET Q1 formed in a diode.

The above-mentioned currents I2 and I1 are formed by the above-mentioned MOSFET Q6 and a MOSFET Q8 and a MOSFET Q9 formed in a current mirror. The current I2 is supplied to a MOSFET Q4 and the current I1 is supplied to a MOSFET Q2. A source of the MOSFET Q2 is supplied with the above-mentioned current I1 through the p-channel MOSFET Q7 and a current mirror circuit formed by n-channel MOSFETs Q10 and Q11. A source of the above-mentioned MOSFET Q4 is connected to ground potential and a gate and a drain thereof are made common; thereby forming this transistor in a diode. The gate and the drain made common are connected to a gate of the MOSFET Q2 to get the reference voltage VR from the source of the MOSFET Q2.

The reference voltage VR is output as a differential voltage (VGS4-VGS2) between a voltage VGS4 between

gate and source of the MOSFET Q4 and a voltage VGS2 between gate and source of the MOSFET Q2.

The MOSFET Q1 through Q4 operates in a saturated region and the following two equations (1) and (2) are established with respect to the currents I1 and I2:

$$I1 = (1/2) \times (W1/L1) \times \beta n \times (VGS1 - Vth1)^2 \quad (1)$$

$$= (1/2) \times (W2/L2) \times \beta n \times (VGS2 - Vth2)^2$$

$$I1 = (1/2) \times (W3/L3) \times \beta n \times (VGS3 - Vth3)^2 \quad (2)$$

$$= (1/2) \times (W4/L4) \times \beta n \times (VGS4 - Vth4)^2$$

where, W1/L1 through W4/L4 are size ratios between channel width  $W$  and channel length  $L$  of MOSFET Q1 through Q4 and  $\beta n$  stands for a channel conductivity of the n-channel MOSFETs. VGS1 through VGS4 are voltages between gate and source of the MOSFET Q1 through Q4 and Vth1 through Vth4 are threshold voltages of the MOSFET Q1 through Q4.

In the circuit of FIG. 2, the threshold voltages of the MOSFET Q2 and Q4 are equally set like Vth2=Vth4 and the size ratios are set as shown in equation (3) below:

$$(\alpha:1=W1/L1:W2/L2=W3/L3:W4/L4) \quad (3)$$

In the above-mentioned condition, the reference voltage VR is obtained from equation (4) as follows:

$$VR = VGS4 - VGS2 = \alpha^{1/2} \times (Vth1 - Vth3) \quad (4)$$

As seen from equation (4), the reference voltage VR can be obtained from the size ratio  $\alpha$  and a threshold voltage difference (Vth1-Vth3) between MOSFETs Q1 and Q3. In other words, when making different the threshold voltages of the MOSFET Q1 and Q3 by ion implantation or the like, a resulting process dispersion is corrected by adjusting the size ratio  $\alpha$ . Consequently, the MOSFETs Q1, Q2, Q3 and Q4 are formed as follows:

Generally, channel lengths  $L$  of MOSFETs are the same. A conductance of a particular MOSFET is set by varying its channel width  $W$ . Therefore, if the channel widths W2 and W4 or substantial sizes of the MOSFETs Q2 and Q4 are set to 1, a desired reference voltage VO is provided by adjusting the sizes of the MOSFETs Q1 and Q3. For this reason, the MOSFETs Q1 and Q3 are represented in one MOSFET in FIG. 2; actually, however, a plurality of MOSFETs are formed on the semiconductor substrate, in which the number of MOSFETs to be arranged in parallel is determined by a switch MOSFET to be switch-controlled by a control voltage formed by a programming device such as the fuse constituting the trimming circuit 1 of FIG. 1.

When correcting the process dispersion of (Vth1-Vth3), the number of adjusting MOSFETs to be arranged in parallel may be set to a fixed MOSFET by a control signal such as the above-mentioned fuse. To do so, it is required for the MOSFETs Q1 and Q3 to form beforehand the fixed MOSFET having channel widths W1 and W3 slightly smaller than those of the MOSFETs Q2 and Q4 and the plurality of adjusting MOSFETs having a channel width minute enough for correcting the process dispersion.

The above-mentioned equation (4) indicates that a differential voltage such as (Vth1-Vth3) can be amplified by  $\alpha^{1/2}$ . Therefore, setting the channel widths of the MOSFETs Q1 and Q3 to a value greater than those of the MOSFETs Q2 and Q4 by  $\alpha$  provides the reference voltage VR amplified by  $\alpha^{1/2}$ . To do so, the fixed MOSFET sized by a basic factor of  $\alpha$  may be connected with small-sized MOSFETs for correcting the above-mentioned process dispersion selectively arranged in parallel by a control signal formed by the

programming device such as the fuse constituting the above-mentioned trimming circuit 1.

Referring to FIG. 3, there is shown a circuit diagram of the voltage divider of FIG. 1. In the figure, some of circuit symbols assigned to the MOSFETs are the same as those used in FIG. 2 for easier reading. However, it should be noted that each symbol in FIG. 3 represents a separate circuit function. This holds true with other circuit diagrams.

An n-channel MOSFET Q5, with its gate and drain connected, is formed into a diode. For this MOSFET Q5, an n-channel MOSFET Q6 with its gate connected to the gate of the MOSFET Q5 is provided. As compared with the MOSFET Q5, the MOSFET Q6 is larger in size ratio (W/L) and has a current amplifying function corresponding to the size ratio.

The MOSFET Q5 is provided at its source and drain with a current source for flowing a current I1 formed by a current mirror circuits composed of p-channel MOSFETs Q2 and Q1 and n-channel MOSFET Q9 and Q7. The MOSFET Q6 is provided at its source with a constant current source for flowing a current IR corresponding to the above-mentioned size ratio, and at its drain with a MOSFET Q2 constituting the above-mentioned current mirror circuit.

The reference voltage VR formed by the reference voltage circuit of FIG. 2 is supplied to the source of the above-mentioned MOSFET Q5. An output voltage VN1 is obtained from the source (node N1) of the MOSFET Q6. Making the size ratio (W5/L5:W6/L6) of the MOSFETs Q5 and Q6 a current ratio I1:IR makes equal voltages between gates and sources of the MOSFETs Q5 and Q6, thereby providing VR=VN1. This in turn provides the output voltage source VN1 that outputs the same voltage as the input reference voltage VR.

The current IR is flowed from the MOSFET Q4 by the current mirror circuit. The current IR is then supplied to depletion-type MOSFETs arranged in series to operate as a resistance element. These depletion-type MOSFETs are commonly connected at their gates and drains. When the current IR is flowed through the MOSFET Q6 by the MOSFETs Q3, Q8 and Q9, no current flows through the output node N1 of the MOSFET Q6 and k series depletion-type MOSFET circuits, thereby permitting to apply the reference voltage VR to the k MOSFETs.

The above-mentioned constitution provides divided voltages in VR/k step by outputting divided voltages from the k MOSFETs. Based on the above-mentioned reference voltage VR, the supply voltage side can provide a level-shifted voltage to be raised in the VR/k step. If the total number of the above-mentioned series MOSFETs is j, a maximum voltage will be (j/k)VR. Varying the total number can simultaneously adjust a plurality of divided voltages as a whole. The trimming circuit 2 of FIG. 1 is used to adjust the number of the series MOSFETs k.

The current IR formed as described above flows to depletion-type MOSFETs arranged in series on the supply voltage VCC side through a current mirror MOSFET Q10. This provides a divided voltage VRCj based on the supply voltage VCC.

Referring to FIG. 4, there is shown a circuit diagram illustrating the power supply circuit of FIG. 1 practiced as one preferred embodiment of the invention. This circuit generates a positive voltage such as the voltage VEG of FIG. 1. A charge pump circuit consists of m stages to form a step-up voltage so that an output voltage VO is slightly higher than a desired voltage. The charge pump circuit is supplied with a pulse generated by an oscillator OS through a gate circuit. Controlling this gate circuit by an output of a

voltage comparator CMP permits intermittently operating the charge pump circuit.

The oscillator OSC is controlled by the control signal PSE, but not limited thereto. For example, if the above-mentioned flash memory on which the voltage generator is mounted is in standby mode or read mode in which the output voltage VO is not required, the oscillator OSC itself is stopped from operating by the control signal PSE, thereby realizing power saving.

A total number of n p-channel MOSFETs formed in diode connections (hereinafter referred to as diode MOSFETs) and one p-channel MOSFET are connected in series between an output terminal of the charge pump circuit and the ground potential. Of these diode MOSFETs, a source voltage of a MOSFET provided on the ground potential side is supplied to an inverted input (-) of the voltage comparator CMP. A non-inverted input (+) of the comparator CMP is applied with the above-mentioned reference voltage VR1. This reference voltage VR1 is selected by the trimming circuit 1 from among the voltages formed by the above-mentioned voltage divider or selected by circuit connection. The voltage VR1 is higher than a threshold voltage of the above-mentioned diode MOSFETs. A gate of the above-mentioned one p-channel MOSFET is applied with a voltage VR2 for fine adjustment. The fine-adjusting voltage VR2 is higher than the voltage VR1 in order to secure an operating voltage of the MOSFET provided on the ground potential side. That is, as shown in FIG. 3, when seen from the circuit ground potential, the voltage VR2 is a divided voltage formed by k or more MOSFETs.

When no current flows through the above-mentioned diode MOSFETs arranged in series, an output signal from the voltage comparator CMP goes high, upon which an oscillation pulse is sent from the oscillator OSC to the charge pump circuit, starting a step-up operation. When a resulting step-up voltage causes a current to flow through the above-mentioned series of diodes to make a source voltage of the MOSFET provided on the ground potential side reach the above-mentioned voltage VR1, the output of the voltage comparator CMP is inverted to close the gate circuit. This stops charge-pumping operation and keeps the state. At this moment, a voltage between the source and gate of the MOSFET on the ground potential side is equal to the reference voltage VR1. Therefore, because the voltage VR2 is applied to the gate to cause the same current to flow through the n MOSFETs including the above-mentioned one p-channel MOSFET, voltages between the gates and sources become equal, resulting in a voltage of n×the voltage VR1. And because the gate of one MOSFET is applied with the fine-adjusting voltage VR2, the voltages between the gates and sources of the n MOSFETs provide a voltage such as n×VR1+VR2. In FIG. 4, the multiplication sign (×) is represented by an asterisk (\*). Namely, when the output voltage VO becomes n×VR1+VR2, the charge pump circuit stops charge-pumping; when the output voltage drops from the voltage n×VR1+VR2, the charge pump circuit starts charge-pumping. The voltage n×VR1+VR2 is formed by this intermittent charge pump operation.

Referring to FIG. 5, there is shown a circuit diagram of the power supply circuit of FIG. 1 practiced as another embodiment of the invention. This embodiment forms a negative voltage such as the voltage VWG of FIG. 1. A charge pump circuit consists of a plurality of stages like the charge pump of FIG. 4 and forms a step-up voltage so that an output voltage VO is slightly higher in an absolute value than a desired voltage. The charge pump circuit is applied with a pulse generated by an oscillator OSC through a gate

circuit. Controlling the gate circuit by an output of a voltage comparator CMP permits to operate the charge pump circuit intermittently.

A total number of  $n$  n-channel MOSFETs formed in diodes and one n-channel MOSFET are connected in series between an output terminal of the charge pump circuit and the ground potential. Of these diode MOSFETs, a source voltage of a MOSFET provided on the ground potential side is supplied to a non-inverted input (+) of the voltage comparator CMP. An inverted input (-) of the comparator CMP is applied with the above-mentioned reference voltage VR1. This reference voltage VR1 is selected by the trimming circuit 1 from among the voltages formed by the above-mentioned voltage divider or selected by circuit connection. The voltage VR1 is a voltage higher than a threshold voltage of the above-mentioned diode MOSFETs, relative to the supply voltage VCC. A gate of the above-mentioned one MOSFET is applied with a VR2 for fine adjustment. This fine-adjusting voltage VR2 is a fine-adjusting voltage formed by voltage divider of FIG. 1 as compared to a voltage set by the  $n$  MOSFETs in increments of  $n$  states. In this embodiment, a voltage obtained by adding voltage  $n \times (VR1 - VCC)$  to the fine-adjusting voltage VR2, relative to the supply voltage VCC, can also be formed.

Referring to FIG. 6, there is shown a circuit diagram of the power supply circuit of FIG. 1 practiced as still another embodiment of the invention. FIG. 6 shows an impedance converting circuit from which the input voltage VR is outputted without change. This converter is used in a circuit for forming the voltage VWV of FIG. 1. The input voltage VR is applied to an inverted input (-) of a voltage comparator CMP composed of a differential circuit. A resulting output voltage is applied to a gate of an n-channel output MOSFET to obtain an output voltage VO at its source. The obtained output voltage is fed back to a non-inverted input (+) of the CMP. This constitution controls a gate voltage of the output MOSFET so that the output voltage VO matches the input voltage VR, thereby performing impedance conversion through this output MOSFET of source follower type.

Referring to FIG. 7, there is shown a circuit diagram of the selector control circuit, the trimming circuit, and the selector of FIG. 1 practiced as preferred embodiments of the invention. The selector control circuit is provided with electrodes TM0, TM1, and TM2 having both a capability of specifying one of the trimming circuits and a capability of entering a fuse blow signal on a pseudo basis. Each of these electrodes TM0 through TM3 is provided with a pull-down resistor represented in a black triangle, thereby keeping the electrode normally at low level.

A selector specifying signal entered at each of the electrodes TM0 through TM2 is captured in each latch circuit LTC. When a signal coming from an electrode TMCLK is low, the latch LTC passes the input signal captured at an input terminal D as shown in FIG. 8; when the above-mentioned signal is high, the latch holds the above-mentioned captured signal.

That is, in a probing process or the like, the electrode TMCLK is held low and the signal for specifying up to six selectors is supplied by the electrodes TM0 through TM2 to make the electrode TMCL high, which is held in the latch circuit LTC. By the above-mentioned 3-bit signal, up to eight selectors can be specified. However, when all three bits are zeros, it indicates an all reset state; when all three bits are ones, the signal is used to inhibit pseudo trimming in hold state.

As shown in a timing chart of FIG. 10, when the TMCLK rises, fuse decoder select addresses MT0 through MT2 for

specifying one of the trimming circuits are captured in the latch circuits LTC. This causes the selector control circuit to form a select signal for selecting one of the trimming circuits and puts the pseudo blow signal composed of the signals TM0 through TM2 into a fuse circuit FUS in which the pseudo blow signal is held in a latch circuit. Subsequently, the TMCLK is turned low, a next fuse decoder select address is entered, the entered address is held in the latch circuit, and blow information corresponding to the held address is entered. When a reset signal /RESET supplied to a reset terminal RST goes from low to high, a signal RSTONB goes low for a certain period of time in which the fuse is blown and corresponding fuse information is latched. Because the internal signal /RESET goes low when the power is turned on, the circuit is initialized.

Referring to FIG. 9, there is shown a circuit diagram of the fuse circuit practiced as one embodiment of the invention. A fuse F is provided on the supply voltage VCC side. At another side of the fuse F, a p-channel MOSFET Q1 for pseudo blow and a p-channel MOSFET Q2 for normal operation are arranged in parallel. At other sides of these MOSFETs Q1 and Q2, sources of a p-channel MOSFETs Q3 and Q4 are connected. Drains of the MOSFETs Q3 and Q4 are connected to drains of n-channel MOSFETs Q5 and Q6. The drains of these MOSFETs Q3 through Q6 are commonly connected to provide an output node. Between the n-channel MOSFETs Q5 and Q6 and circuit ground potential, an n-channel MOSFET Q7 functioning as a high resistance element is provided. The supply voltage VCC is regularly applied to a gate of the MOSFET Q7.

A timing pulse ST for reading whether the fuse F has been blown or not is supplied to a gate of the n-channel MOSFET Q5 and a gate of the p-channel MOSFET Q2. The timing pulse ST is also supplied to a gate of the p-channel Q3 as an inverted signal SB via an inverter, not shown. A potential at the above-mentioned output node is entered in an inverter N1. An output signal from this inverter N1 is fed back to a gate of the p-channel MOSFET Q4 on one hand and to a gate of the n-channel MOSFET Q6 on the other hand. The output signal of the inverter N1 is supplied to inverters N2 and N3. A signal DT is outputted from the inverter N2 and an inverted signal DB is outputted from the inverter N3.

When the timing pulse ST is turned high, the MOSFETs Q5 and Q3 are turned on and the MOSFET Q2 is turned off. At this moment, a pseudo blow signal is low and the MOSFET Q1 is on. If the fuse F has not been blown, a high-level signal is put in the inverter N2 because a resistance value of the MOSFET Q5 is larger than that of the fuse F. The output signal of the inverter N1 goes low to turn on the p-channel MOSFET Q3, thereby effecting latching. At this moment, the n-channel MOSFET Q6 is turned off by the low-level output signal of the inverter N1, thereby preventing a direct current from flowing into the fuse F. When the above-mentioned read operation has been completed, the timing pulse ST goes low and both the MOSFETs Q3 and Q5 are turned off.

If the fuse F is blown when the timing pulse ST is high, the low-level signal is put in the inverter N1 by the MOSFET Q7 in the on state. This makes high the output signal of the inverter N1 to turn on the n-channel MOSFET Q5, thereby effecting latching. The high-level signal of the inverter N1 turns off the p-channel MOSFET Q4. Even if a leak current is to flow with a high resistance value although the fuse F has been blown, power saving can be effected because the MOSFET Q3 is off.

To effect a pseudo blown state, the signal P is turned high. This prevents a current pulse from being formed in the state

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in which the fuse F is not blown, so that the input to the inverter N1 is set to low, which can be held.

Referring to FIG. 11, there is shown a block diagram illustrating the voltage generator associated with the invention and practiced as another embodiment thereof. In this embodiment, a high voltage in proportion to a rise in the supply voltage VCC is generated for a life test to perform troubleshooting of initial faults. In this case, relative voltages between control gate and channel and between control gate and gate must be the same as in normal operation for writing data to a memory cell or erasing data from it, the relative voltages are composed of voltages made higher in proportion to the supply voltage VCC and voltages made constant regardless of the supply voltage.

In the embodiment of FIG. 11, a voltage generator VPS' is obtained by adding a reference voltage generator for life testing to the reference voltage generator of FIG. 1. A voltage converter forms a voltage VRBC relative to the supply voltage VCC. A selector 3 selects, by means of a trimming circuit 5, divided voltages VRCK from among divided voltages VRCj formed relative to the supply voltage VCC and sends the selected divided voltages to the voltage converter, the number of the divided voltages VRCK being smaller than the number of the divided voltages VRCj.

Referring to FIG. 12, there is shown an actual circuit diagram of the above-mentioned voltage converter. As shown in the figure, the voltage converter is composed of an n-channel MOSFET supplied at its gate with a reference voltage VRSk selected by connection, n n-channel MOSFET diodes connected in series with the above-mentioned n-channel MOSFET, and a MOSFET provided between the other end of the above-mentioned n-channel MOSFET and the supply voltage VCC and applied at its gate with the voltage VRCK coming from the selector 3. These MOSFETs are all equal in size. The voltage converter sends out an output voltage VRBC from a drain of a MOSFET provided on the ground potential side of the above-mentioned circuit.

This voltage converter operates as follows. First, the MOSFET applied at its gate and source with the reference voltage VRSk flows a reference current, which also flows into the MOSFETs arranged in series, thereby making equal voltages of the gates and sources of the n diode MOSFETs to the above-mentioned reference voltage VRSk. Since the reference voltage VRCK that varies according to the supply voltage VCC is applied to the gate of the MOSFET on the supply voltage side, a voltage level-shifted by voltages between gates and sources of the n+1 MOSFETs relative to the reference voltage VRCK is outputted. Because the current formed by the MOSFET applied at its gate and source with the reference voltage VRSk flows in each of the above-mentioned MOSFETs, the output voltage VRBC is a voltage obtained by  $VCC - (n+1) \times VRSk - VRCK$ .

In FIG. 11, the voltage VRBC that varies with the supply voltage VCC is supplied to comparator. The comparator is applied at the other input with the reference voltage VRSk. The comparator does not perform a voltage comparing operation in a normal sense but selects the higher of the two voltages and outputs the selected voltage.

Referring to FIG. 13, there is shown a circuit diagram of the above-mentioned comparator practiced as one embodiment of the invention. The above-mentioned voltages VRSk and VRBC are applied to gates of differentially arranged n-channel MOSFETs Q1 and Q2 respectively. An n-channel MOSFET Q3 is provided with its source made common with sources of the MOSFETs Q1 and Q2. The MOSFETs Q3 is made common at its gate and drain to flow a current of a constant current source I2. These MOSFETs Q1 through Q3

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are equal in size. A constant current source I3 is provided to the common source of the MOSFETs Q1 through Q3. A current of the constant current source I3 is set to a value twice as high as the current of the constant current source I2. These constant current sources I2 and I3 are set to the above-mentioned current ratio based on the MOSFET size ratio by using a current mirror circuit based on the reference current source.

When the  $VRSk > VRBC$ , the MOSFET Q1 is turned on. Consequently, the same current I2 flows through the MOSFETs Q1 and Q3. This causes the voltage VRSk applied to the gate of the MOSFET Q1 to be outputted via the gate and source of the MOSFET Q1 and the source and gate of the MOSFET Q3. Conversely, if the  $VRSk < VRBC$ , the MOSFET Q2 is turned on. Consequently, the same current I2 flows through the MOSFETs Q2 and Q3. This causes the voltage VRBC applied to the gate of the MOSFET Q2 to be outputted via the gate and source of the MOSFET Q2 and the source and gate of the MOSFET Q3. Thus, the output voltage VRBS is made equal to the higher of the two voltages VRSk and VRBC.

In FIG. 11, voltages VEG, VED, VEV, VWD, and VWV are formed from the above-mentioned divided voltage VRBm instead of the divided voltages VRSi and VRSi of FIG. 1. If the supply voltage VCC is raised over a certain level for life testing, these divided voltages of FIG. 11 become voltages that vary based on the reference voltage VRBC to be raised corresponding to the supply voltage VCC.

Referring to FIGS. 15 and 16, there are shown voltage characteristics diagram. FIG. 15 (A) shows the voltage characteristic of the reference voltage VR. As shown, over an operating voltage, the reference voltage is constant regardless of the rise in the supply voltage VCC. FIG. 15 (B) shows the voltage characteristic of the divided voltage VRSi formed based on the reference voltage VR. The divided voltage VRSi consists of a plurality of voltages, each being constant corresponding to the circuit ground potential. FIG. 16 shows the voltage characteristic of the divided voltage VRCj formed based on the reference voltage VR. The divided voltage VRCj consists of a plurality of voltages, each being constant corresponding to the supply voltage VCC.

Referring to FIG. 17, there are shown voltage characteristics of the reference voltage generator at life testing of FIG. 11. As shown in FIG. 17 (A), when the supply voltage VCC reaches the operating voltage, the voltage VRBC varies accordingly. Because the above-mentioned reference voltage VRSk is constant, the reference voltage VRBS to be outputted around the inversion of potential relationships due to the rise in the supply voltage VCC is switched from the VRSk to the VRBC. In FIG. 17 (B), based on the above-mentioned switching, the divided voltage VRBm is switched over a certain voltage from a Constant voltage to a voltage dependent on the supply voltage VCC.

Referring to FIG. 8, there is shown voltage characteristics for describing operations of a collectively erasable EEPROM (flash memory) using the voltage generator of FIG. 11. In an operation guaranteed range with the supply voltage being relatively low, each voltage is set so that the voltage has a constant relationship with a variation of the supply voltage.

When the supply voltage VCC is raised over the above-mentioned operation guaranteed range and a test range is reached, each voltage rises in proportion to the rise in the supply voltage VCC. At this moment, a voltage VWD applied to data line and a control gate potential VWG for



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program are kept constant. This is because the program voltage cannot be held constant unless the VWD is held constant since the memory cell gate voltage at program is constant. Meanwhile, a voltage for erasure is set so that an erase operation is performed at a voltage similar to one in the operation guaranteed range by maintaining constant the relationship of the VEG and VED to the supply voltage VCC.

TABLE 1

Supply voltage	At normal operation				At life test		Remarks
	Setting value	VR1	n	VR2	VR2	Setting value	
VCC	3-3.6					6.5	
VEG	12.0	1.5	7	1.5	3.5	14.0	
VED	-4.0	-1.6 + VCC	3	0.8	2.8	-2.0	
VEG- VED	16.0					16.0	Erase voltage
VEV	5.3	1.7	2	1.9	3.9	7.3	
VWG	-9.5	-1.5 + VCC	7	1.0	1.0	-9.5	
VWD	4.5					4.5	Write data line
VWD- VWG	14.0					14.5	Write voltage
VWV	1.5			1.5	3.5	3.5	
VWS	7.2	1.4	4	1.6	1.6	7.2	

Table 1 lists actual setting values of the above-mentioned voltages. The reference voltages VR1 and VR2 and n correspond to the reference voltages and the number of stages of series MOSFETs in FIG. 4 and FIG. 5. Numerals 3-3.6 of the supply voltage VCC mean 3.0 V to 3.6 V.

From the above-mentioned embodiments of the invention, following effects are obtained:

(1) The charge pump circuit for forming a step-up voltage higher than a desired voltage adding is intermittently operated so that the desired internal voltage is obtained by adding a voltage obtained by multiplying a particular voltage among a plurality of divided voltages formed based on a reference voltage by n to a predetermined divided voltage, thereby efficiently forming any stable voltages.

(2) For a circuit for forming the above-mentioned desired internal voltage obtained by adding the two voltages, a MOSFET applied at its gate with the above-mentioned adjusting divided voltage is provided in the n MOSFET diodes provided between the output terminal of the charge pump circuit and the ground potential or supply voltage of the voltage generator and a MOSFET diode is inserted in series to match its drain voltage with the reference voltage. This simple constitution of the MOSFETs diodes and the voltage comparator can form any desired voltages.

(3) The above-mentioned voltage generator is used to provide desired supply voltages by operating the charge pump circuit intermittently, thereby contributing to power saving.

(4) A threshold voltage difference between the enhancement-type MOSFET and the depletion-type MOSFET is used and fine adjustment is performed based on the size ratio between these MOSFETs, thereby providing the desired reference voltage with precision against process dispersion.

(5) For a reference voltage to be put in the above-mentioned voltage comparator, a voltage selected, by the select signal formed by detecting whether the fuse has been blown or not, from among the divided voltages formed by the above-mentioned voltage divider is used, thereby providing a desired voltage with precision including process dispersion.

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(6) The above-mentioned reference voltage generator includes a reference voltage generator for life testing based on the supply voltage and, when the supply voltage is raised over a predetermined voltage, the reference voltage for life testing is used, thereby efficiently providing troubleshooting of initial faults.

(7) In a memory cell, an erase operation is performed by injecting a charge from the substrate side to the floating gate via the tunnel insulating film based in the relative potential relationship between the control gate and the substrate. Based on the above-mentioned relative potential relationship between the control gate and the substrate, the charge is discharged from the floating gate to the drain side via the above-mentioned tunnel insulating film for a program operation. For a collectively erasable nonvolatile memory circuit composed of such memory cells, the charge pump circuit for forming a step-up voltage higher than a desired internal voltage is intermittently operated as a power supply circuit for forming a plurality of voltages required for programming, erasing and reading data with such memory cells. The charge pump circuit is operated so that the desired internal voltage is obtained by adding a voltage obtained by multiplying a particular voltage among the plurality of divided voltages formed based on the reference voltage by n to a predetermined divided voltage. This constitution can efficiently form a variety types of voltages.

(8) The reference voltage generator for life testing based on a supply voltage as the reference voltage is provided. When the supply voltage is raised over a predetermined voltage, the reference voltage for life testing is used. A memory cell application voltage at erase and program operations in the life testing is varied relative to the above-mentioned supply voltage to form a constant voltage. This constitution permits the program and erase operations while performing an acceleration test.

While the preferred embodiments of the present invention have been described using specific terms, such description is for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the appended claims. For example, the controller for intermittently operating the charge pump circuit may be any controller that performs control so that the output voltage provides the desired voltage based on the above-mentioned reference voltage. Further, the constitution of the memory cells constituting the flash memory may be any if the erase and program operations are made by the tunnel current as described above.

This invention is widely applicable to any semiconductor integrated circuit devices that require a variety of internal voltages.

The following describes effects to be obtained by typical inventions disclosed herein. The charge pump circuit for forming a step-up voltage higher than a desired voltage adding is intermittently operated so that the desired internal voltage is obtained by adding a voltage obtained by multiplying a particular voltage among a plurality of divided voltages formed based on a reference voltage by n to a predetermined divided voltage, thereby efficiently forming any stable voltages.

For a circuit for forming the above-mentioned desired internal voltage obtained by adding the two voltages, a MOSFET applied at its gate with the above-mentioned adjusting divided voltage is provided in the n MOSFET diodes provided between the output terminal of the charge pump circuit and the ground potential or supply voltage of the voltage generator and a MOSFET diode is inserted in series to match its drain voltage with the reference voltage.

This simple constitution of the MOSFETs diodes and the voltage comparator can form any desired voltages.

The above-mentioned voltage generator is used to provide desired supply voltages by operating the charge pump circuit intermittently, thereby contributing to power saving.

A threshold voltage difference between the enhancement-type MOSFET and the depletion-type MOSFET is used and fine adjustment is performed based on the size ratio between these MOSFETs, thereby providing the desired reference voltage with precision against process dispersion.

For a reference voltage to be put in the above-mentioned voltage comparator, a voltage selected, by the select signal formed by detecting whether the fuse has been blown or not, from among the divided voltages formed by the above-mentioned voltage divider is used, thereby providing a desired voltage with precision including process dispersion.

The above-mentioned reference voltage generator includes a reference voltage generator for life testing based on the supply voltage and, when the supply voltage is raised over a predetermined voltage, the reference voltage for life testing is used, thereby efficiently providing troubleshooting of initial faults.

In a memory cell, an erase operation is performed by injecting a charge from the substrate side to the floating gate via the tunnel insulating film based in the relative potential relationship between the control gate and the substrate. Based on the above-mentioned relative potential relationship between the control gate and the substrate, the charge is discharged from the floating gate to the drain side via the above-mentioned tunnel insulating film for a program operation. For a collectively erasable nonvolatile memory circuit composed of such memory cells, the charge pump circuit for forming a step-up voltage higher than a desired internal voltage is intermittently operated as a power supply circuit for forming a plurality of voltages required for writing, erasing and reading data with such memory cells. The charge pump circuit is operated so that the desired internal voltage is obtained by adding a voltage obtained by multiplying a particular voltage among the plurality of divided voltages formed based on the reference voltage by  $n$  to a predetermined divided voltage. This constitution can efficiently form a variety types of voltages.

The reference voltage generator for life testing based on a supply voltage as the reference voltage is provided. When the supply voltage is raised over a predetermined voltage, the reference voltage for life testing is used. A memory cell application voltage at erase and program operations in the life testing is varied relative to the above-mentioned supply voltage to form a constant voltage. This constitution permits the program and erase operations while performing an acceleration test.

What is claimed is:

1. A flash memory comprising:

a memory array wherein memory cells are disposed at intersections between a word line and a data line in a matrix, said memory cells being erased by injecting an electric charge from a substrate into a floating gate via a tunnel insulating film based on a relative potential relationship between a control gate and said substrate and programmed by discharging the electric charge from the floating gate into a drain via said tunnel insulating film based on a relative potential relationship between said control gate and said drain; and

a power supply circuit which forms a plurality of voltages necessary for programming, erasing, and reading said memory cells, wherein said power supply circuit comprises:

a reference voltage generating circuit which generates a reference voltage;

a voltage dividing circuit which forms a plurality of divided voltages based on said reference voltage;

a voltage supply circuit which outputs a desired internal voltage by adding a voltage obtained by multiplying one of said plurality of divided voltages by  $n$  to a predetermined divided voltage selected from said plurality of divided voltages for fine voltage adjustment, wherein said voltage supply circuit includes:

a charge pump circuit,

$n$  first metal-oxide semiconductor field-effect transistors each having a diode connection and disposed in series between an output terminal of said charge pump circuit and one of a ground potential and a supply voltage,

a voltage comparator which receives said one of said plurality of divided voltages and a drain or source voltage of a second metal-oxide semiconductor field-effect transistor coupled to one of said ground potential and supply voltage, and

a gate circuit which limits an input pulse to be supplied to said charge pump circuit by an output voltage of said voltage comparator,

wherein one of said first metal-oxide semiconductor field-effect transistors that is inserted in said  $n$  metal-oxide semiconductor field-effect transistors in series is applied at a gate thereof with said predetermined divided voltage.

2. A flash memory according to claim 1, further comprising a second reference voltage generating circuit for generating a test reference voltage which is higher than said reference voltage during a life test.

3. A semiconductor integrated circuit device comprising:

a reference voltage generating circuit which generates a reference voltage;

a voltage dividing circuit which forms a plurality of divided voltages based on said reference voltage; and

a power supply circuit which outputs a desired internal voltage by adding a voltage obtained by multiplying one of said plurality of divided voltages by  $n$  to a predetermined divided voltage selected from said plurality of divided voltages for fine voltage adjustment, wherein said power supply circuit includes:

a charge pump circuit,

$n$  first metal-oxide semiconductor field effect transistors each having a diode connection and disposed in series between an output terminal of said charge pump circuit and one of a ground potential and a supply voltage,

a voltage comparator which receives said one of said plurality of divided voltages and a drain or source voltage of a second metal-oxide semiconductor field-effect transistor coupled to one of said ground potential and supply voltage, and

a gate circuit which limits an input pulse to be supplied to said charge pump circuit by an output voltage of said voltage comparator,

wherein one of said first metal-oxide semiconductor field-effect transistors that is inserted in said  $n$  metal-oxide semiconductor field-effect transistors in series is applied at a gate thereof with said predetermined divided voltage.

4. A semiconductor integrated circuit device according to claim 3, wherein said second metal-oxide semiconductor field-effect transistor also has a diode connection and is



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connected in series with said n first metal-oxide semiconductor field-effect transistors.

5. A semiconductor integrated circuit device according to claim 4, wherein said second metal-oxide semiconductor field-effect transistor is coupled in series between said n first metal-oxide semiconductor field-effect transistors and one of said ground potential and said supply voltage.

6. A semiconductor integrated circuit device according to claim 3, further comprising a control circuit which intermittently operates said power supply circuit.

7. A semiconductor integrated circuit device according to claim 6, wherein said control circuit includes a voltage comparator having one input coupled to the output of the power supply circuit and another input coupled to receive a reference voltage, wherein said control circuit turns said power supply circuit on and off to maintain a predetermined constant output voltage for said power supply circuit.

8. A flash memory according to claim 1, further comprising a control circuit which intermittently operates said voltage supply circuit.

9. A flash memory according to claim 8, wherein said control circuit includes a voltage comparator having one input coupled to the output of the voltage supply circuit and another input coupled to receive a reference voltage, wherein said control circuit turns said voltage supply circuit

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on and off to maintain a predetermined constant output voltage for said voltage supply circuit.

10. A semiconductor integrated circuit device according to claim 3, wherein said reference voltage generating circuit generates said reference voltage on the basis of a threshold voltage difference between an enhancement-type metal-oxide semiconductor field-effect transistor and a depletion-type metal-oxide semiconductor field-effect transistor, said reference voltage generating circuit being fine-adjusted based on a size ratio between said enhancement-type metal-oxide semiconductor field-effect transistor and said depletion-type metal-oxide semiconductor field-effect transistor.

11. A semiconductor integrated circuit device according to claim 3, wherein the reference voltage to be applied to said voltage comparator is a voltage selected by a select signal formed by detection of whether a fuse has been blown from among the plurality of divided voltages formed by said voltage dividing circuit.

12. A semiconductor integrated circuit device according to claim 3, further comprising a second reference voltage generating circuit for generating a test reference voltage which is higher than said reference voltage during a life test.

\* \* \* \* \*



US005589793A

**United States Patent** [19]**Kassapian**[11] **Patent Number:** **5,589,793**[45] **Date of Patent:** **Dec. 31, 1996**[54] **VOLTAGE BOOSTER CIRCUIT OF THE CHARGE-PUMP TYPE WITH BOOTSTRAPPED OSCILLATOR**[75] **Inventor:** **Christian G. Kassapian, Marseille, France**[73] **Assignee:** **SGS-Thomson Microelectronics S.A., Saint Genis Pouilly, France**[21] **Appl. No.:** **128,871**[22] **Filed:** **Sep. 29, 1993**[30] **Foreign Application Priority Data**

Oct. 1, 1992 [FR] France ..... 92 11751

[51] **Int. Cl.<sup>6</sup>** ..... **H03K 3/00**[52] **U.S. Cl.** ..... **327/536; 327/258; 327/259; 327/530; 327/291; 327/295; 327/239; 327/306**[58] **Field of Search** ..... **307/262, 264, 307/263, 363, 296.2, 513; 331/57, 46; 327/291, 258, 589, 596, 536, 548, 534, 535, 144, 145, 295, 259, 239, 306, 530**[56] **References Cited****U.S. PATENT DOCUMENTS**

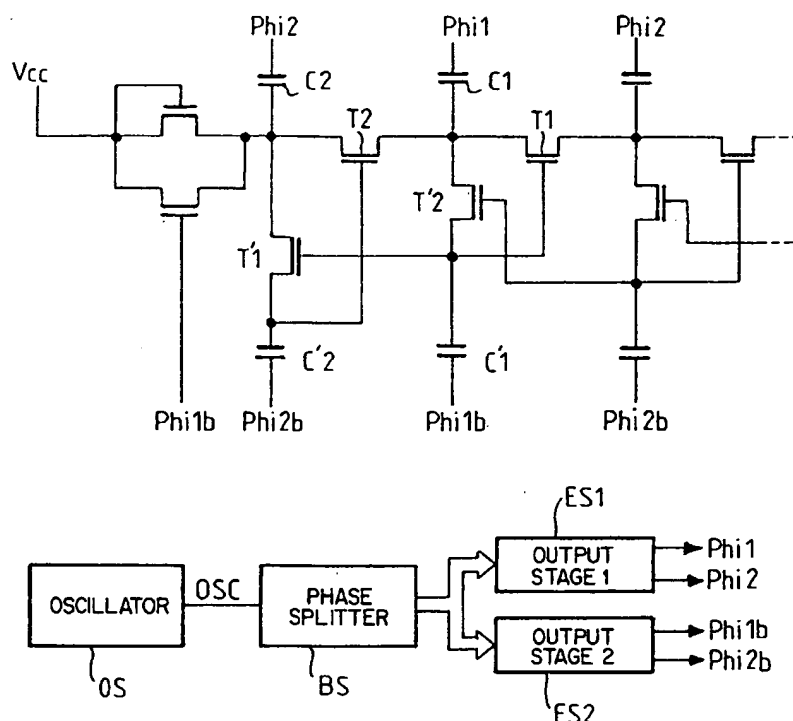
4,409,496	10/1983	Baba	327/536
5,097,226	3/1992	Pascucci et al.	331/57
5,202,588	4/1993	Matsuo et al.	327/536
5,394,372	2/1995	Tanaka et al.	327/536

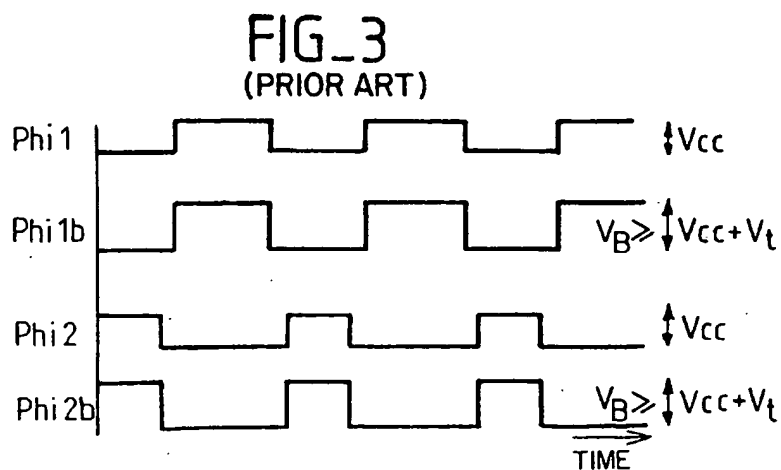
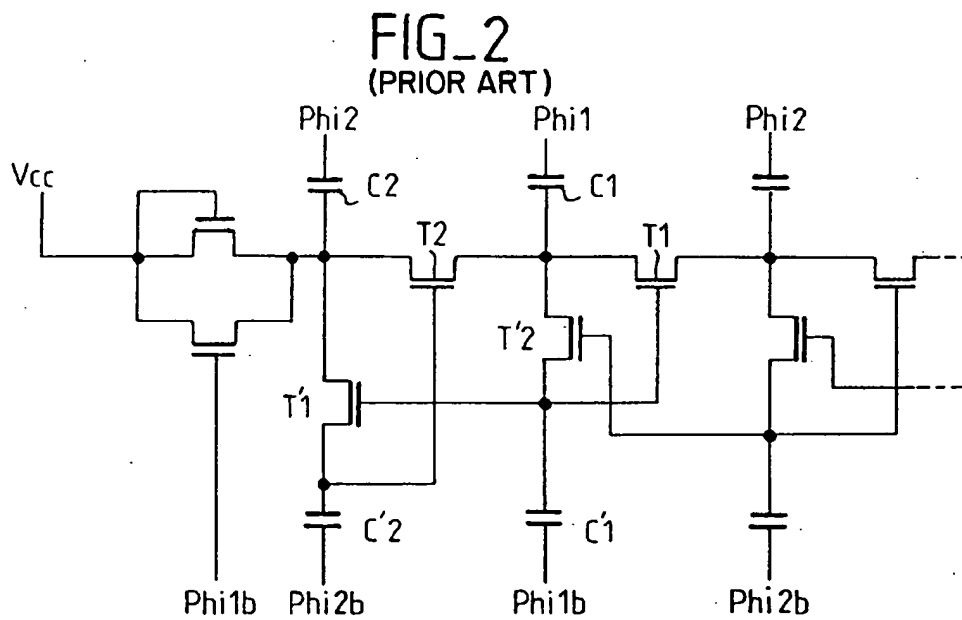
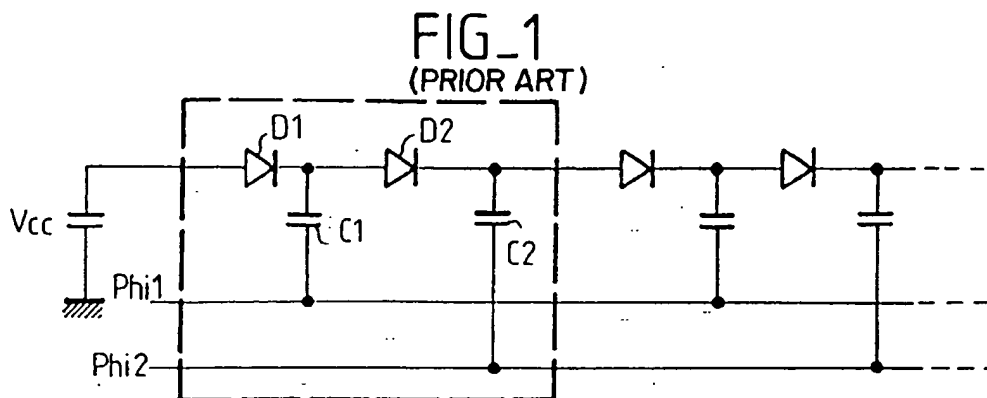
**FOREIGN PATENT DOCUMENTS**

0350462	1/1990	European Pat. Off.	
0445083	9/1991	European Pat. Off.	
2379198	8/1978	France	
0090129	7/1980	Japan	302/556
2096422	4/1990	Japan	327/259

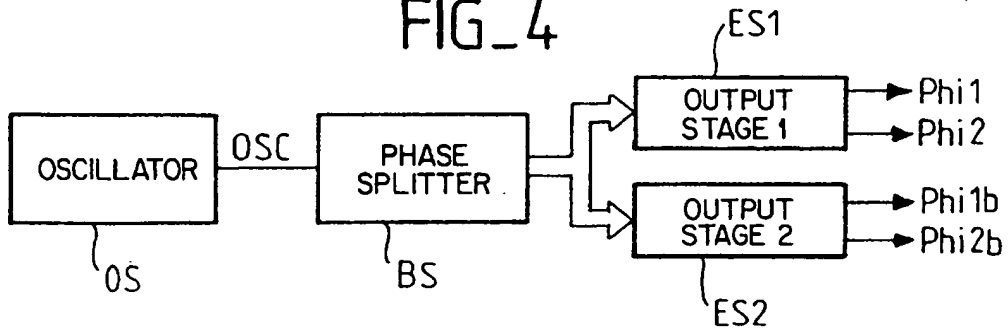
**Primary Examiner**—Timothy P. Callahan**Assistant Examiner**—Dinh T. Le**Attorney, Agent, or Firm**—David M. Driscoll; James H. Morris; Brett N. Dorny[57] **ABSTRACT**

The invention relates to charge-pump circuits used for the generation, in an integrated circuit, of an internal supply voltage  $V_{pp}$  which is considerably greater than the external supply voltage  $V_{cc}$ . In a charge pump configuration with capacitors and transistors, certain transistors must be driven by bootstrapped logic signals, i.e., having a logic level which is greater than  $V_{cc}$  in order to overcome the threshold voltage of the transistors. According to the invention, there is an oscillator followed by a phase splitter stage which is in turn followed by a bootstrap amplifier stage. The oscillator is a ring oscillator having a number of logic gates which is as small as possible, preferably only three. A satisfactory frequency stability of the charge pump is thus obtained and therefore its design is made easier and its adaptability to various electronic circuits is improved.

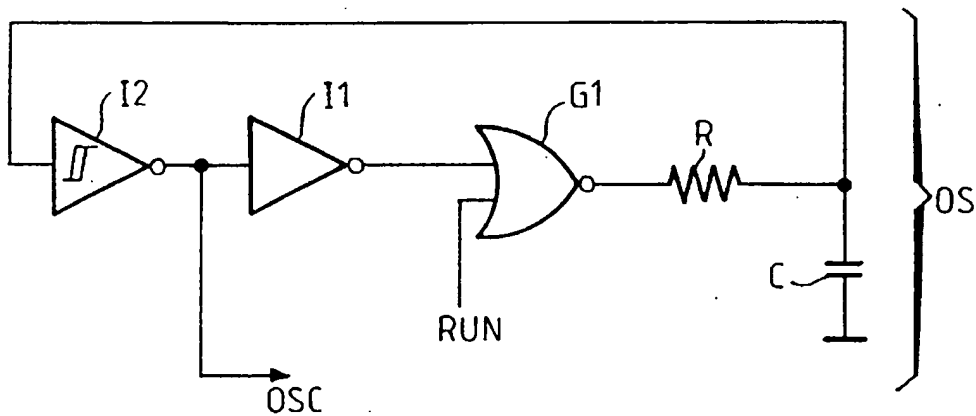
**23 Claims, 4 Drawing Sheets**



FIG\_4



FIG\_5



FIG\_6

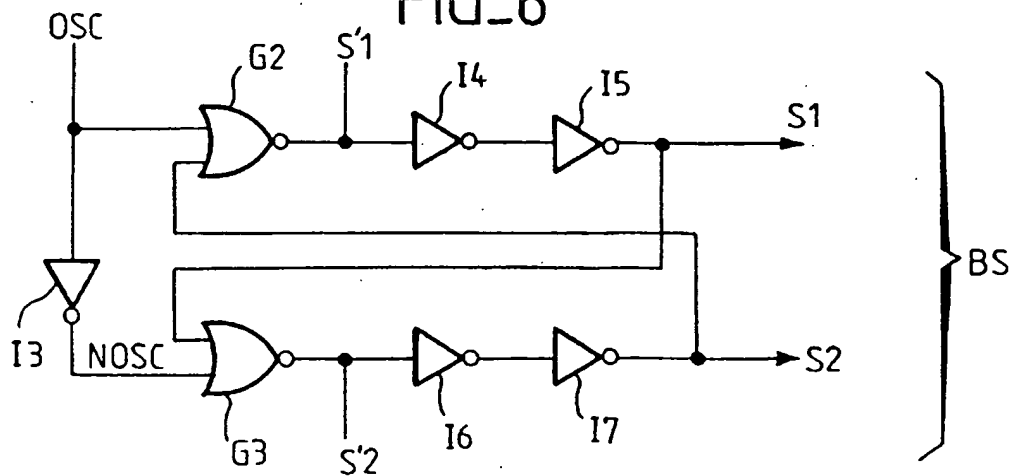
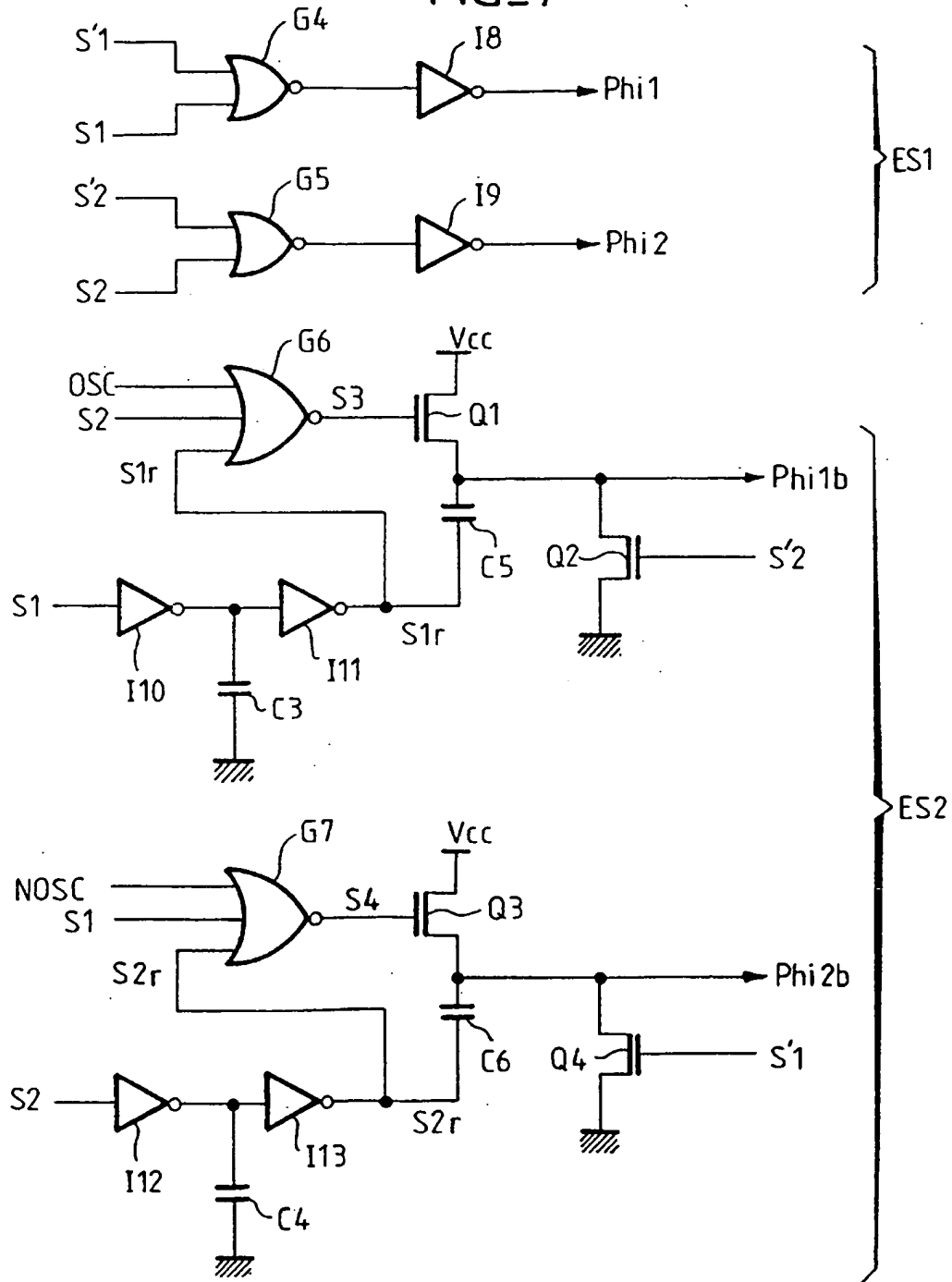
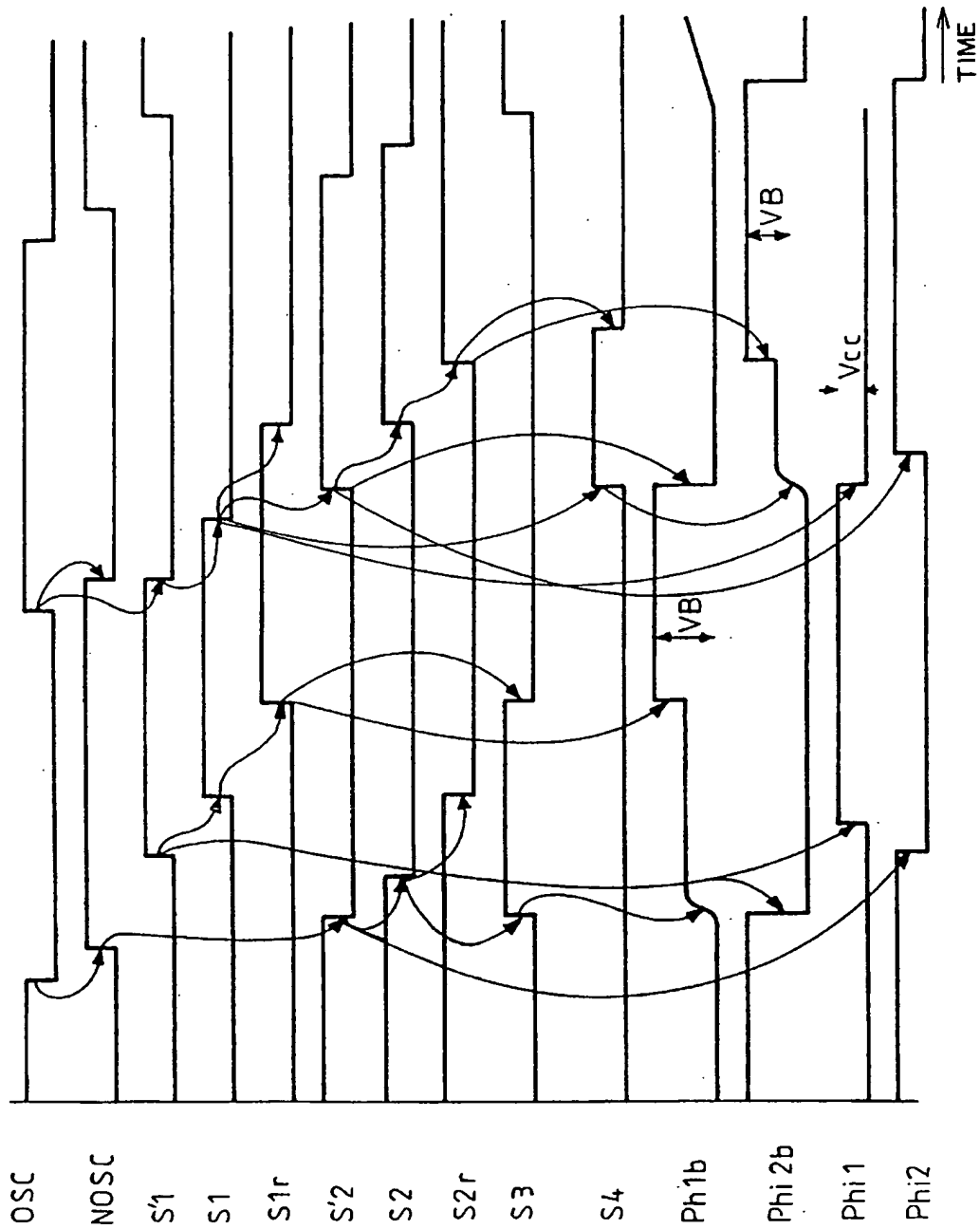


FIG. 7



FIG\_8



# VOLTAGE BOOSTER CIRCUIT OF THE CHARGE-PUMP TYPE WITH BOOTSTRAPPED OSCILLATOR

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to electronic circuits supplied with a voltage  $V_{cc}$  in which a voltage greater than  $V_{cc}$  must be generated.

### 2. Discussion of the Related Art

A typical example is that of integrated circuits comprising non-volatile memories with floating-gate transistors; programming such memories requires a programming voltage  $V_{pp}$  much greater than the normal supply voltage  $V_{cc}$ . In order to allow the user to use this memory with only one supply voltage  $V_{cc}$ , measures are taken for the integrated circuit to have an internal means to generate the voltage  $V_{pp}$  from  $V_{cc}$ . Typically,  $V_{cc}$  has a value of 5 volts or even less and  $V_{pp}$  has a value of 15 volts or more. The future trend is toward a voltage  $V_{cc}$  lower than 2 volts, while  $V_{pp}$  can be above 15 volts.

The circuit for the generation of  $V_{pp}$  is a voltage booster circuit whose principle is that of the "charge pump".

The block diagram of the charge pump is shown in FIG. 1. The charge pump comprises a series of diode and capacitor stages and switches providing for the switching of the capacitor connections between  $V_{cc}$  and ground and depending on two non-overlapping periodic phases  $\Phi_{i1}$ ,  $\Phi_{i2}$ . Each stage includes two capacitors  $C1$  and  $C2$  and two diodes  $D1$  and  $D2$ . In the first phase of  $\Phi_{i1}$ , the first capacitor  $C1$  is charged to the supply voltage  $V_{cc}$ . In the second phase of  $\Phi_{i2}$ , it is partly discharged into the second capacitor  $C2$ . Then  $C1$  is charged ( $\Phi_{i1}$ ) again. The diodes prevent the second capacitor  $C2$  from discharging, so that its load progressively increases until it reaches a value which exceeds  $V_{cc}$  (up to a theoretical maximum of  $2 V_{cc}$  if the voltage drops in the diodes are not taken into account).

In order to obtain a higher voltage,  $n$  successive stages are cascade-connected. The obtained voltage amounts to  $(n+1)V_{cc}$  or, more precisely, if the threshold voltage  $V_d$  of the diodes is taken into account, to  $(n+1)(V_{cc}-V_d)$ .

In order to obtain a sufficient output voltage value with the smallest possible number  $n$  of stages, it has already been suggested to replace the diodes  $D1$  and  $D2$  with transistors, across which no significant voltage drop is created because their resistance is negligible when they are in conductive mode. The block diagram in FIG. 2 shows this. Since the transistors have a threshold voltage  $V_t$  (minimum gate-to-source voltage below which they are not conductive), certain transistors are arranged to have their gates driven by a voltage level which is higher than  $(V_{cc}+V_t)$ . Thus they are made conductive (i.e., no significant voltage drop across them) even if their sources and their drains are at  $V_{cc}$ , which eliminates the threshold voltage problem. With a charge pump comprising  $n$  stages, an output voltage up to  $(n+1)V_{cc}$  can be obtained, which is more favourable than the result of diode circuits. But it implies that the gates of certain transistors can be driven using a voltage slightly greater than  $V_{cc}$ .

For this reason, the charge pump diagram in FIG. 2 shows two drive signal pairs:  $\Phi_{i1}$  and  $\Phi_{i2}$  on the one hand as shown in FIG. 1, which switch between two voltage levels 0 and  $V_{cc}$ ; and  $\Phi_{i1b}$  and  $\Phi_{i2b}$  on the other hand, synchronized with  $\Phi_{i1}$  and  $\Phi_{i2}$  respectively, but switching

between voltage levels 0 and  $V_B$ , where  $V_B$  has a greater level than  $V_{cc}$ , preferably greater than or equal to  $V_{cc}+V_t$ . FIG. 3 shows schematically the switching phases of the charge pump according to FIG. 2.

A significant parameter of the charge pump is its "fan-out", which is the number of loads it can supply without any excessive output voltage attenuation. Computations show that the fan-out is inversely proportional to the number of stages of the pump and is proportional to the switching frequency of the pump, i.e., the frequency of signals  $\Phi_{i1}$ ,  $\Phi_{i2}$ ,  $\Phi_{i1b}$ ,  $\Phi_{i2b}$ .

Therefore, the switching frequency must be quite stable, or at least it should decrease as little as possible when the number of stages of the pump increases. It is also desirable that the switching frequency be as stable as possible with respect to the supply voltage  $V_{cc}$ .

In order to generate switching drive signals  $\Phi_{i1}$ ,  $\Phi_{i2}$ ,  $\Phi_{i1b}$ , and  $\Phi_{i2b}$ , it has already been suggested to use comparatively complex oscillator circuits which have the disadvantage of a poor frequency stability, both with respect to the supply voltage changes and also with respect to the number of stages or, more generally, to the structure of the charge pump they actually control.

Therefore, the circuits utilized in the prior art have a charge pump frequency which depends on the number of the charge pump stages in a significant way, which makes the circuit design rather difficult and thus general-purpose diagrams, capable of being transposed from one circuit to another one, cannot be drawn for the charge pump.

It is an object of this invention to provide an improved charge pump diagram.

## SUMMARY OF THE INVENTION

The present invention provides a charge pump making use of multiple transistor and capacitor stages with a transistor switching control circuit. The switching control circuit comprises a ring oscillator delivering a signal at a frequency  $F$  and is followed by a phase splitter stage in order to deliver from the oscillator output two non-overlapping switching phases at the oscillator frequency. The control circuit further comprises a first output stage to deliver from the signals generated by the splitter stage two non-overlapping signals  $\Phi_{i1}$  and  $\Phi_{i2}$  capable of switching between a zero voltage and a voltage  $V_{cc}$  and a second bootstrapped output stage to deliver from signals coming from the splitter stage two signals  $\Phi_{i1b}$  and  $\Phi_{i2b}$ , capable of switching in synchronously with  $\Phi_{i1}$  and  $\Phi_{i2}$ , but between a zero voltage and a voltage  $V_B$  greater than  $V_{cc}$ .

Oscillators capable of delivering the signals  $\Phi_{i1}$ ,  $\Phi_{i2}$ ,  $\Phi_{i1b}$ , and  $\Phi_{i2b}$  were available in the prior art, but these oscillators did not separate the oscillation, non-overlapping and bootstrap-type amplification functions; the non-overlapping and bootstrap amplification functions were inserted in the oscillation loop. This resulted in the frequency instability which is corrected for by the invention. That was for example typically the case for a circuit described in a EP-A-0 445 083 patent application. There amplifiers  $D$  and  $D'$  are inserted in oscillator loops.

Preferably, the ring oscillator is an oscillator with only three logic gates, one of which is a threshold inverter gate. This type of oscillator, which minimizes the number of logic gates, offers the advantage of generating a frequency which has little dependence on the supply voltage.

Other features and advantages of the invention are more readily apparent from the following detailed description taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a charge pump having diodes and capacitors;

FIG. 2 illustrates a charge pump having transistors and capacitors;

FIG. 3 illustrates switching signals associated with the charge pump according to FIG. 2;

FIG. 4 illustrates a switching control circuit according to the invention;

FIG. 5 illustrates an oscillator diagram useful for the implementation of the invention;

FIG. 6 illustrates a phase splitter circuit diagram useful for the implementation of the invention;

FIG. 7 illustrates a diagram of bootstrapped and non-bootstrapped output stages, which can be used in the switching control circuit according to the invention;

FIG. 8 illustrates the logic signals in various spots of the circuit according to the invention.

## DETAILED DESCRIPTION

FIG. 4 shows the general arrangement of the switching control circuit used in a charge pump according to the invention.

The charge pump is a pump such as that shown in FIG. 2. It comprises multiple cascaded stages, including transistors and capacitors, and a switching control circuit generating the four switching phases  $\Phi_{i1}$ ,  $\Phi_{i2}$ ,  $\Phi_{i1b}$ , and  $\Phi_{i2b}$ .  $\Phi_{i1}$  and  $\Phi_{i2}$  are two complementary though non-overlapping phases, switching between two values, which substantially are 0 and  $V_{cc}$  ( $V_{cc}$  being the supply voltage of the circuit).  $\Phi_{i1b}$  and  $\Phi_{i2b}$  are phases substantially synchronized with  $\Phi_{i1}$  and  $\Phi_{i2}$ , respectively, and switching between two voltage values, which substantially are 0 and  $V_B$ , where  $V_B$  is greater than  $V_{cc}$  and preferably greater than  $V_{cc} + V_t$  ( $V_t$  is the threshold voltage of the transistors driven by phases  $\Phi_{i1b}$  and  $\Phi_{i2b}$ ). While  $\Phi_{i1}$  and  $\Phi_{i2}$  are non-bootstrapped signals,  $\Phi_{i1b}$  and  $\Phi_{i2b}$  are bootstrapped signals capable of exceeding the voltage  $V_{cc}$ . The term "bootstrap" refers to a technique for generating a logic signal which is artificially enhanced with respect to its normal value, in general by means of a capacitor which is precharged prior to being series-connected between the signal to be enhanced and the terminal on which the enhanced signal is to appear.

The switching control circuit according to FIG. 4 therefore gives the four phases  $\Phi_{i1}$ ,  $\Phi_{i2}$ ,  $\Phi_{i1b}$ , and  $\Phi_{i2b}$ . It comprises an oscillator OS generating a periodic signal OSC having a frequency  $F$ , a phase splitter circuit BS to generate, from the signal OSC, various complementary though non-overlapping signals at the frequency  $F$ , and, lastly, two output stages ES1 and ES2 making use of these signals to generate signals  $\Phi_{i1}$  and  $\Phi_{i2}$  which are not bootstrapped (stage ES1) and signals  $\Phi_{i1b}$  and  $\Phi_{i2b}$ , which are bootstrapped (stage ES2).

Preferably, the oscillator is a ring oscillator with a very small number of logic gates, preferably only three, for optimum stability with respect to changes in the supply voltage. The preferred diagram is that in FIG. 5. It preferably includes inverter I1, which has its output connected to the first input of NOR gate G1, which has its input driven by a signal RUN; the signal RUN enables or disables the oscillator operation. The G1 NOR gate output is connected through an RC time-constant circuit to the input of another inverter, preferably a threshold inverter (in particular, a

Schmitt trigger). The output of inverter I2, which is fed back to the input of inverter I1, forms the output of the oscillator generating the signal OSC. The oscillation frequency mainly depends on the respective values of R and C and on the threshold of inverter I2 and, to a lesser extent, on the switching times of the inverters I1 and I2 and gate G1.

The phase splitter stage BS is preferably made up as shown in FIG. 6. It receives, as an input signal, the signal OSC generated by the oscillator OS. This signal is inverted in an inverter I3 to generate a signal NOSC. The positive-going edges of NOSC are slightly delayed with respect to the negative-going edges of OSC and, in the same way, the negative-going edges of NOSC are slightly delayed with respect to the positive going edges of OSC, owing to the delay inevitably induced by inverter I3.

The timing diagrams of the periodic switching signals generated by the circuitry according to the invention are shown in FIG. 8 and they can be referred to for a better understanding of the circuit operation. The same reference marks were intentionally chosen to designate the circuit nodes and the switching signals appearing at these nodes, both in the above-mentioned diagram and in the following explanations.

The phase splitter circuit BS, whose function consists of generating two complementary non-overlapping periodic phases at frequency  $F$ , has two outputs S1 and S2. They are non-overlapping and complementary in that the positive-going edge of S1 begins after the end of the negative-going edge of S2, and the negative-going edge of the following S1 appears before the next positive-going edge of S2.

The signal OSC is applied to an input of a NOR gate G2, another input of which receives the signal S2. Inversely, the signal NOSC is applied to a NOR gate G3, another input of which receives the signal S1.

The output of NOR gate G2 forms the output S'1 of the stage BS, this output is used afterwards for the generation of signals  $\Phi_{i1}$  and  $\Phi_{i2}$ . The signal S'1 has a positive-going edge triggered by the negative-going edge of S2 and a negative-going edge triggered by the signal OSC.

In the same way, the output of G3 forms output S'2 of the stage. The signal S'2 has a negative-going edge triggered by the signal NOSC and a positive-going edge triggered by the signal S1.

The signal S'1 is inverted in two cascaded successive inverters I4 and I5, the input of the first one being connected to the output of gate G2 and the output of the second one forming the output S1. In the same way, the signal S'2 is inverted in two cascaded successive inverters I6 and I7, the input of the first one being connected to the output of gate G3 and the output of the second one being connected to the output S2.

Both signals S1 and S2 are delayed (by the two respective inverters) with respect to signals S'1 and S'2. The signals S'1 and S'2 form two non-overlapping complementary phases, as signals S1 and S2 do.

The preferred arrangement of the output stages, bootstrapped and non-bootstrapped, is illustrated in FIG. 7.

The non-bootstrapped stage ES1, which generates signals  $\Phi_{i1}$  and  $\Phi_{i2}$ , receives as inputs the four signals S1, S'1, S2 and S'2 from the phase splitter stage. S1 and S'1 are applied to the inputs of NOR gate G4; the output of gate G4 is inverted in inverter I8 to generate the signal  $\Phi_{i1}$ . The signal  $\Phi_{i1}$  switches between two logic levels 0 and  $V_{cc}$  because the inverter I8 is supplied with a voltage  $V_{cc}$ .

In the same way, the signals S2 and S'2 are applied to the input of a NOR gate G5 whose output is inverted by inverter



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I9 to generate the signal Phi2 which switches between 0 and Vcc and is complementary to Phi1 and non-overlapping with Phi1.

The bootstrapped output stage is slightly more complex. It receives as inputs the signals S1 and S2 as well as the signals OSC and NOSC. In addition, Besides, it receives the signals S'1 and S'2.

The signal S1 is delayed by a delay circuit comprising, for instance, series inverters I10 and I11, and a capacitor C3 being connected between the output of the first inverter (I10) and ground, according to the arrangement shown in FIG. 7. The delayed signal appears at the output of I11 and is called S1r. In the same way, the signal S2 is delayed by an identical delay circuit (I12, I13, C4); the delayed signal is designated S2r. The induced delay is slightly greater (owing to C3 or C4) than that induced by the two series-connected inverters.

The stage ES2 comprises, in addition to the delay circuits, two NOR gates G6 and G7 with three inputs each. The gate G6 receives the OSC signal, the signal S2, and the signal S1r. Its output S3 generates a square pulse while the signal OSC is at the low level. The square pulse has a positive-going edge triggered by the negative-going edge of S2, and a negative-going edge triggered by the positive-going edge of the following S1r. Conversely, the NOR gate G7 receives NOSC, S1, and S2r. Its output S4 delivers, while OSC is at the high level, a square pulse whose positive-going edge is triggered by the negative-going edge of S1 and whose negative-going edge is triggered by the positive-going edge of S2r.

The square pulses S3 and S4 are used for the achievement of the precharging phase of stage ES2 outputs Phi1b and Phi2b, respectively, prior to the bootstrapped switching phase, which is triggered by signals S1r and S2r, respectively.

To this end, the output S3 of the NOR gate G6 is connected to the control gate of transistor Q1 whose source is connected to the supply Vcc and whose drain is connected to the output Phi1b. A capacitor C5 is connected between the output S1r of the delay circuit (I10, I11, C3) and Phi1b. During the square pulse S3, the transistor Q1 is made conductive and Phi1b rises to level Vcc; since, at this time, the signal S1r is at the low level, the capacitor C5 tends to get charged to Vcc. Afterwards, towards the end of the square pulse S3, the transistor Q1 changes to the off-state, which isolates the output Phi1b from the terminal Vcc, and S1r rises to the high level Vcc, which abruptly raises the potential of Phi1b to above Vcc, due to the energy previously stored in C5. The bootstrap effect is thus achieved on the signal Phi1b.

The signal Phi1b is reset by transistor Q2, which is connected between the output Phi1b and ground and is made conductive by signal S'2.

The generation of the bootstrapped signal Phi2b is by the same method, using an array Q3, C6, Q4 identical with array Q1, C5, Q2, and receiving the signals S2r, S'1, S4 instead of S1r, S'2 and S3.

With the arrangement according to the invention, the oscillator OS is only loaded by inverter I3, gate G2, and gate G6. Its frequency is little affected by such a small load.

The outputs Phi1, Phi2, Phi1b, and Phi2b are loaded by the n stages of the charge pump, but their ability to control these n stages depends only on the dimensioning of the final components (transistors and capacitors) of the output stages and these final components do not affect the oscillator load.

Having thus described one particular embodiment of the invention, various alterations, modifications, and improve-

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ments will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A charge pump comprising:

- a stage of a voltage-boosting circuit comprising a transistor and a capacitor; and
- a transistor switching control circuit coupled to the stage and controlling the switching of the transistor, the transistor switching control circuit comprising:
  - a ring oscillator generating an oscillator signal at an oscillator frequency;
  - a phase splitter stage receiving the oscillator signal and generating a plurality of non-overlapping phase-split signals substantially at the oscillator frequency;
  - a non-bootstrapped output stage, receiving the plurality of non-overlapping phase-split signals, and generating a plurality of non-bootstrapped non-overlapping output signals that switch between a zero voltage and a supply voltage substantially at the oscillator frequency; and
  - a bootstrapped output stage, receiving the plurality of non-overlapping phase-split signals, and generating a plurality of bootstrapped non-overlapping output signals that switch between the zero voltage and a voltage of greater magnitude than the supply voltage substantially synchronously with the non-bootstrapped non-overlapping output signals.

2. The charge pump of claim 1 wherein the ring oscillator comprises no more than three logic gates.

3. The charge pump of claim 2 wherein at least one of the logic gates in the ring oscillator is a threshold inverter.

4. The charge pump circuit of claim 1, wherein the ring oscillator generates the oscillator signal independent from the phase-split stage, the non-bootstrapped output stage, and the bootstrapped output stage, to prevent interference between the oscillator signal and the bootstrapped output signals and the non-bootstrapped output signals.

5. The charge pump of claim 1, wherein:

the plurality of non-overlapping phase-split signals includes a first signal and a second signal that are non-overlapping with respect to one another, and a third signal and a fourth signal that are non-overlapping with respect to one another; and

the non-bootstrapped output stage includes a circuit having an input that receives the plurality of non-overlapping phase-split signals, the circuit combining the first signal and the third signal and combining the second signal and the fourth signal to generate the plurality of non-bootstrapped non-overlapping output signals.

6. A charge pump comprising:

means using a switching technique for creating a voltage of greater magnitude than a supply voltage; and  
means for controlling the switching technique, comprising:

first means for receiving an oscillator signal at an oscillator frequency and generating a plurality of intermediate signals;

second means for receiving the plurality of intermediate signals and generating a first plurality of phase-split signals, each of the first plurality of phase-split signals switching between a first voltage and a second voltage; and

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third means for receiving the plurality of intermediate signals and generating a second plurality of phase-split signals, each of the second plurality of phase-split signals switching between the first voltage and a third voltage that is different from the second voltage.

7. The charge pump of claim 6 wherein the first plurality of phase-split signals are non-overlapping and the second plurality of phase split signals are non-overlapping.

8. The charge pump of claim 6 wherein the second voltage is the supply voltage.

9. The charge pump of claim 6 wherein each of the first plurality of phase-split signals has a frequency that is substantially equal to the oscillator frequency, and wherein each of the second plurality of phase-split signals has a frequency that is substantially equal to the oscillator frequency.

10. The charge pump of claim 6, wherein the second means includes means for combining at least two of the plurality of intermediate signals to generate the first plurality of phase-split signals.

11. A charge pump comprising: means using a switching technique for creating a voltage of greater magnitude than a supply voltage; and

means for controlling the switching technique comprising:

oscillator means for generating an oscillator signal at an oscillator frequency;

phase-split means for receiving the oscillator signal and generating a plurality of non-overlapping phase-split signals at the oscillator frequency;

non-boosting generator means for receiving the plurality of non-overlapping phase-split signals and generating a plurality of non-bootstrapped non-overlapping output signals switching between a zero voltage and the supply voltage substantially at the oscillator frequency; and

boosting generator means for receiving the plurality of non-overlapping phase-split signals and generating a plurality of bootstrapped non-overlapping output signals, the bootstrapped non-overlapping output signals switching between the zero voltage and a voltage of greater magnitude than the supply voltage and switching substantially synchronously with the non-bootstrapped non-overlapping output signals.

12. The charge pump circuit of claim 11, wherein the oscillator means generates the oscillator signal independent from the phase-split means, the non-boosting generator means, and the boosting generator means, to prevent interference between the oscillator signal and the bootstrapped signals and the non-bootstrapped signals.

13. The charge pump of claim 11, wherein:

the plurality of non-overlapping phase-split signals includes a first signal and a second signal that are non-overlapping with respect to one another, and a third signal and a fourth signal that are non-overlapping with respect to one another; and

the non-boosting generator means includes means for combining the first signal and the third signal, and for combining the second signal and the fourth signal, to generate the plurality of non-bootstrapped non-overlapping output signals.

14. A charge pump comprising:

a voltage-boosting circuit;

first means for receiving an oscillator signal and generating a plurality of intermediate signals;

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second means, coupled to the voltage-boosting circuit and responsive to the plurality of intermediate signals, for providing a first plurality of phase-split signals to the voltage-boosting circuit, each of the first plurality of phase-split signals switching between a first voltage and a second voltage; and

third means, coupled to the voltage-boosting circuit and responsive to the plurality of intermediate signals, for providing a second plurality of phase-split signals to the voltage-boosting circuit, each of the second plurality of phase-split signals switching between a first voltage and a third voltage that is different from the second voltage.

15. The charge pump of claim 14, further comprising an oscillator, coupled to the first means, the oscillator having an output that provides the oscillator signal, the oscillator generating the oscillator signal independently from the first, second and third means.

16. The charge pump of claim 14, wherein the first plurality of phase-split signals includes a plurality of non-overlapping bootstrapped signals and the second plurality of phase split signals includes a plurality of non-overlapping, non-bootstrapped signals, the non-overlapping, non-bootstrapped signals having a voltage that switches at the oscillator frequency between a zero voltage and a supply voltage, the plurality of non-overlapping bootstrapped signals having a voltage that switches at the oscillator frequency between the zero voltage and a voltage of greater magnitude than the supply voltage.

17. The charge pump of claim 16, further comprising an oscillator, coupled to the first means, the oscillator having an output that provides the oscillator signal, the oscillator generating the oscillator signal independently from the first, second, and third means.

18. The charge pump of claim 14, wherein:

the plurality of intermediate signals includes a first signal and a second signal that are non-overlapping with respect to one another, and a third signal and a fourth signal that are non-overlapping with respect to one another; and

the second means includes means for combining the first signal and the third signal, and for combining the second signal and the fourth signal, to generate the first plurality of phase-split signals.

19. An apparatus comprising:

a charge pump circuit for creating an output voltage of greater magnitude than a supply voltage in response to signals received at an input of the charge pump circuit; and

a control circuit, coupled to the charge pump circuit, the control circuit having an input that receives an oscillator signal at an oscillator frequency, a first output that provides a first plurality of phase-split signals to the input of the charge pump circuit, each of the first plurality of phase-split signals switching between a first voltage and a second voltage, and a second output that provides a second plurality of phase-split signals to the input of the charge pump circuit, each of the second plurality of phase-split signals switching between a first voltage and a third voltage that is different from the second voltage;

wherein the control circuit includes;

a phase splitter, having an input that receives that receives the oscillator signal, a first output that provides a first plurality of internal signals, and a second output that provides a second plurality of internal signals;

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a first output stage, having an input that receives the first plurality of internal signals and the second plurality of internal signals and an output that provides the first plurality of phase-split signals; and

a second output stage, having an input that receives the first plurality of internal signals and the second plurality of internal signals and an output that provides the second plurality of phase-split signals.

20. The apparatus of claim 19 wherein the second voltage is the supply voltage.

21. The apparatus of claim 19 wherein each of the first plurality of phase-split signals has a frequency that is substantially equal to the oscillator frequency, and wherein

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each of the second plurality of phase-split signals has a frequency that is substantially equal to the oscillator frequency.

22. The apparatus of claim 19, further comprising an oscillator having an output that provides the oscillator signal to input of the control circuit.

23. The apparatus of claim 19 wherein the first plurality of phase-split signals includes two signals that are non-overlapping, and the second plurality of phase split signals includes two signals that are non-overlapping.

\* \* \* \* \*



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## United States Patent [19]

Nadd

[11] Patent Number: 5,672,992

[45] Date of Patent: Sep. 30, 1997

## [54] CHARGE PUMP CIRCUIT FOR HIGH SIDE SWITCH

[75] Inventor: Bruno C. Nadd, Puyvert, France

[73] Assignee: International Rectifier Corporation,  
El Segundo, Calif.

[21] Appl. No.: 420,301

[22] Filed: Apr. 11, 1995

[51] Int. Cl.<sup>5</sup> ..... H03K 17/16[52] U.S. Cl. .... 327/390; 327/391; 327/437;  
327/537; 327/589[58] Field of Search ..... 327/108, 389,  
327/390, 391, 427, 434, 437, 534, 536,  
537, 589

## [56] References Cited

## U.S. PATENT DOCUMENTS

4,691,129	9/1987	Einzinger et al.	
4,703,196	10/1987	Arakawa	327/126
4,731,552	3/1988	Miyamoto	327/306
4,883,976	11/1989	Deane	327/536
4,902,919	2/1990	Spohrer et al.	327/108
4,952,827	8/1990	Leipold et al.	
5,023,474	6/1991	Wilcox	327/109
5,028,811	7/1991	Le Roux et al.	327/110
5,142,171	8/1992	Nunogawa et al.	
5,184,035	2/1993	Sugibayashi	327/536

5,258,662	11/1993	Skovmand	327/544
5,359,244	10/1994	Hopkins	327/434
5,369,320	11/1994	Satani et al.	327/108
5,371,418	12/1994	Leipold et al.	327/109
5,404,053	4/1995	Poma et al.	327/108
5,446,406	8/1995	Gantioler et al.	327/42
5,467,047	11/1995	Robb	327/377

## FOREIGN PATENT DOCUMENTS

0602708	6/1994	European Pat. Off.
4403201	8/1994	Germany

Primary Examiner—Terry Cunningham

Attorney, Agent, or Firm—Ostrolenk, Faber, Gerb & Soffen,  
LLP

## [57] ABSTRACT

A high side monolithic switching circuit integrated into a silicon chip is described in which the charge pump is connected to the ground terminal by a constant current circuit and floats relative to the ground terminal to reduce noise generation. The charge pump is connected to a  $V_{cc}$  terminal by an auxiliary power MOSFET having its gate connected to the charge pump output circuit. The conventional charge pump diodes are implemented as MOSFET devices which can be easily integrated into the common monolithic chip. A clamping circuit across the charge pump permits the use of a low voltage, small area capacitor for a high voltage device.

32 Claims, 9 Drawing Sheets

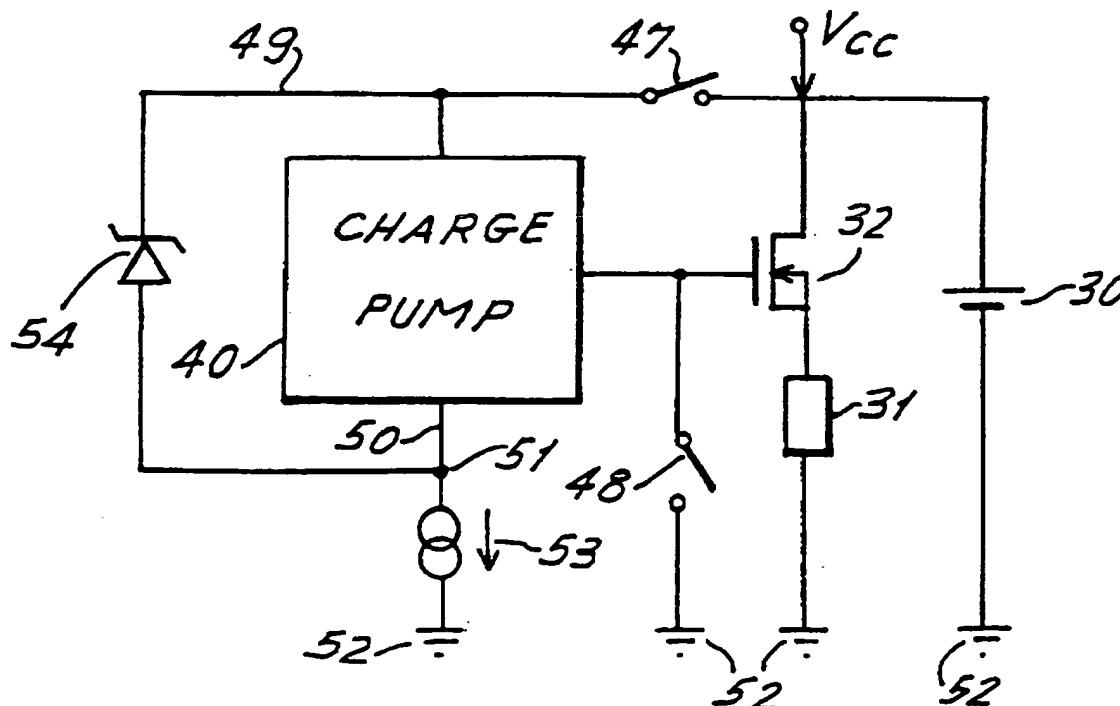


FIG. 1 PRIOR ART

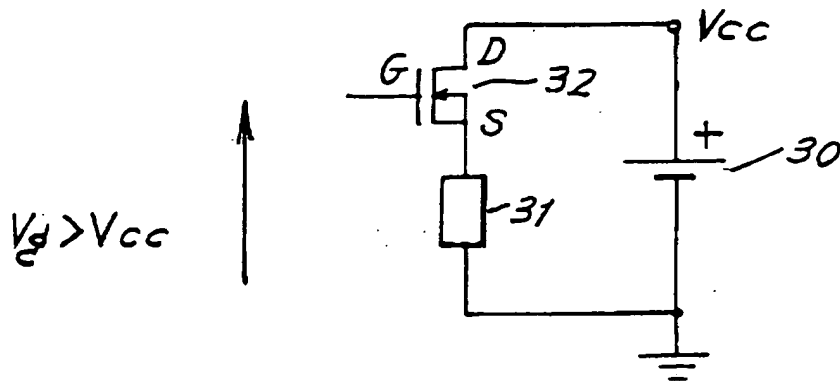


FIG. 2 PRIOR ART

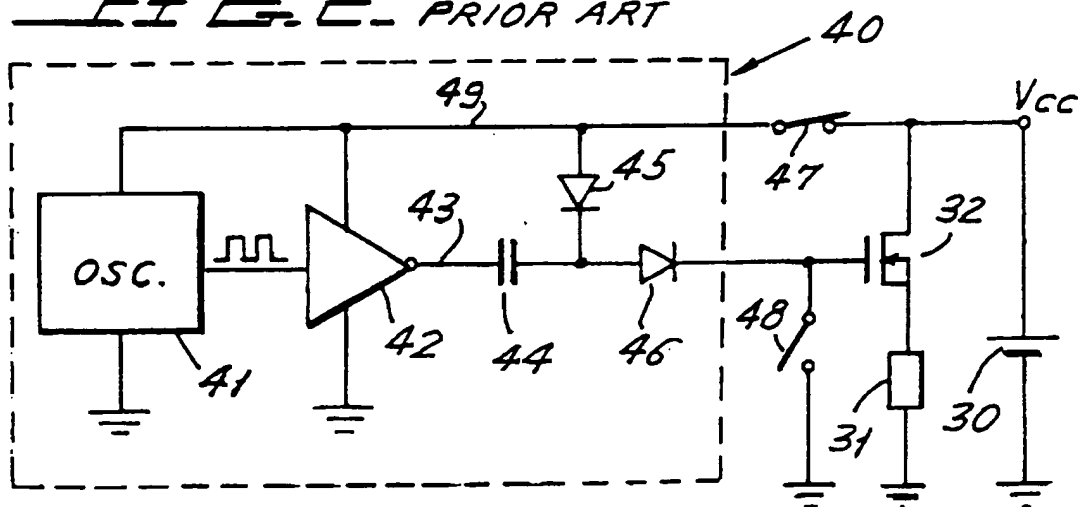


FIG. 3  
PRIOR ART

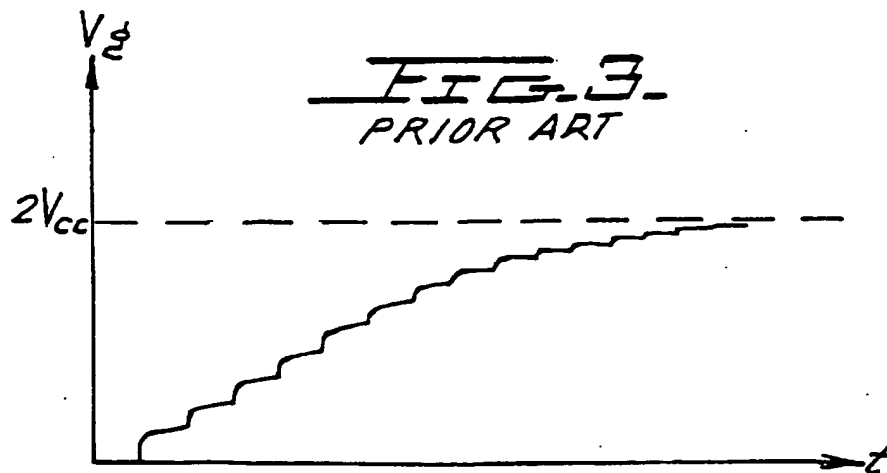


FIG. 4

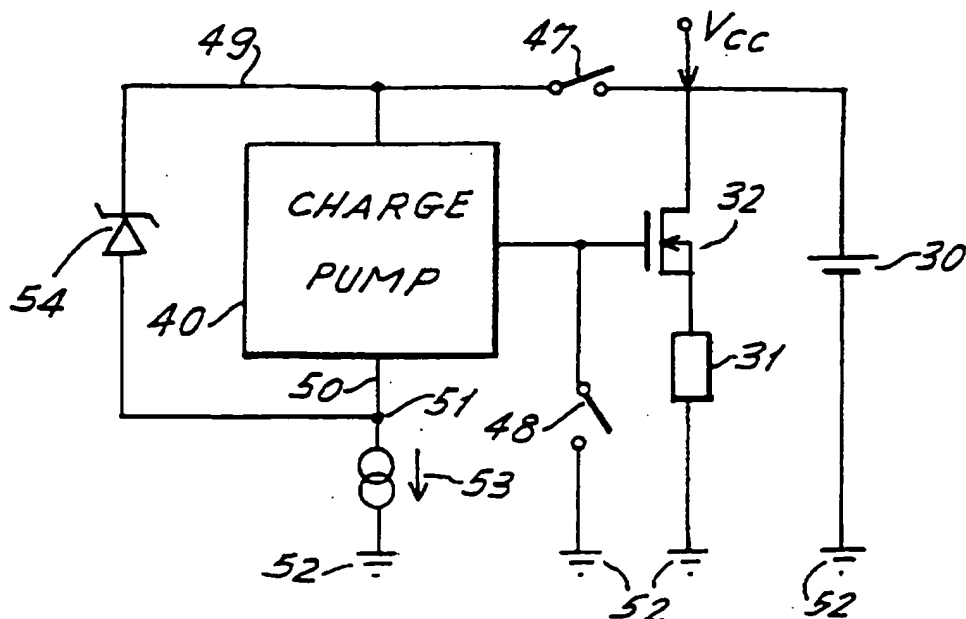


FIG. 4a

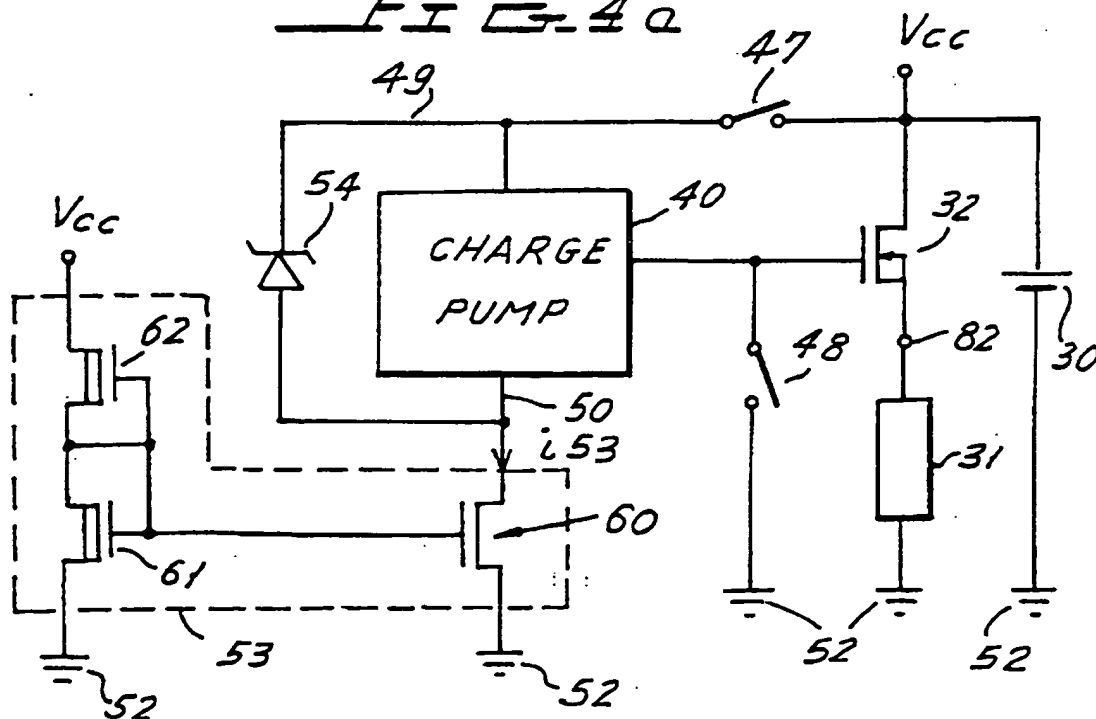


FIG. 5a

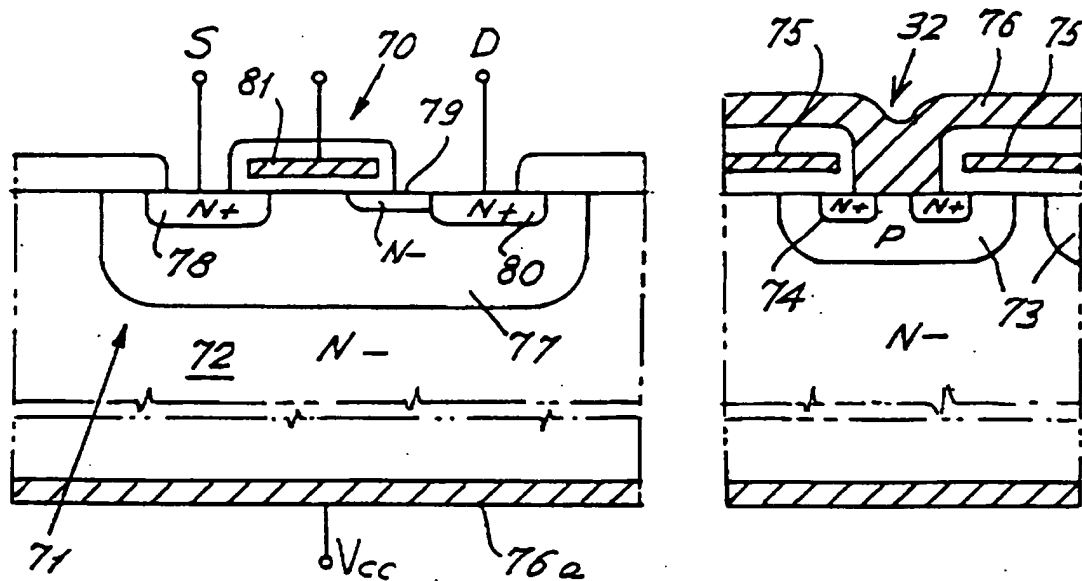


FIG. 5.

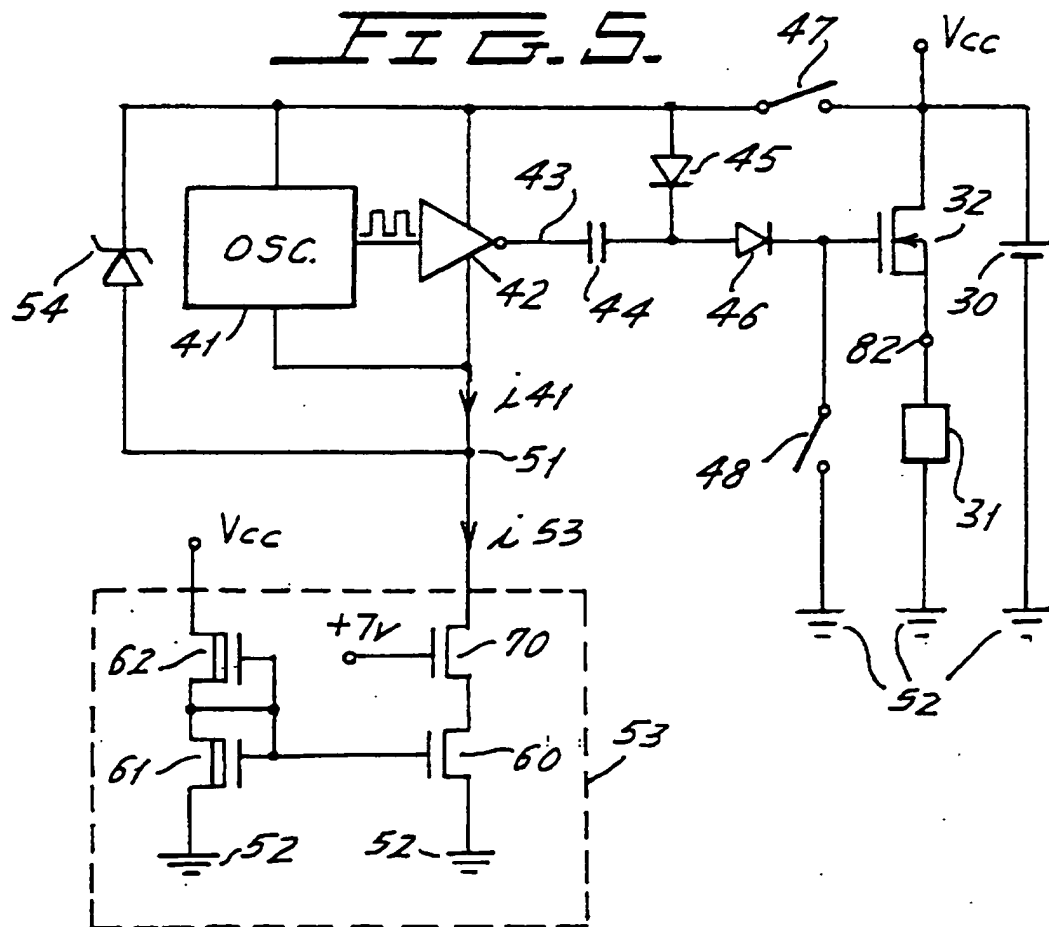


FIG. 6.

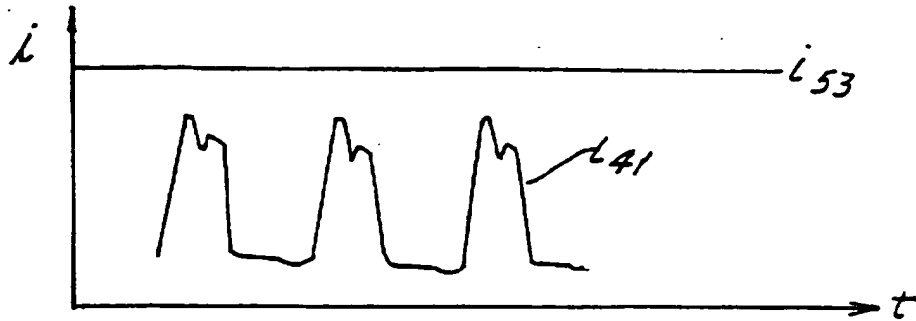


FIG. 7.

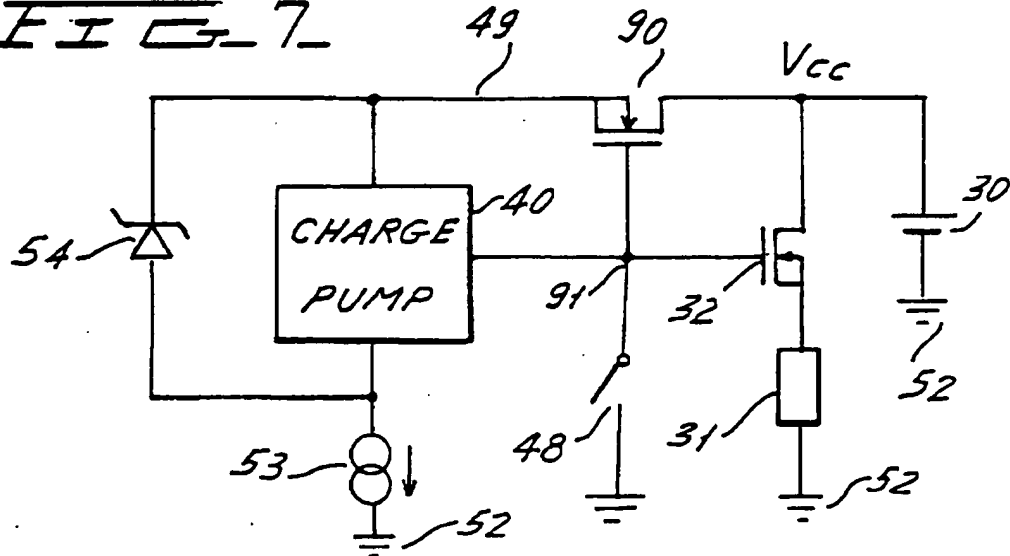


FIG. 8.

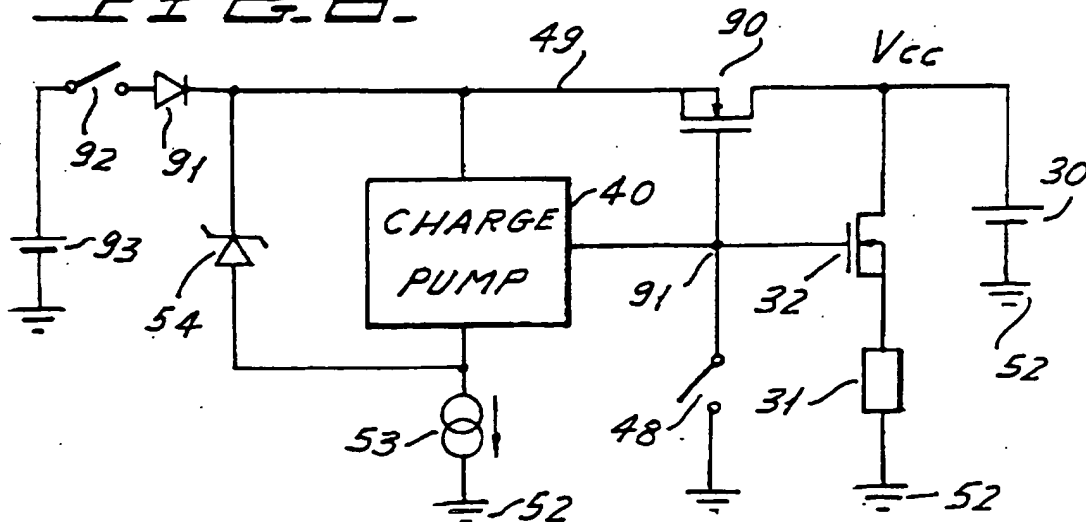




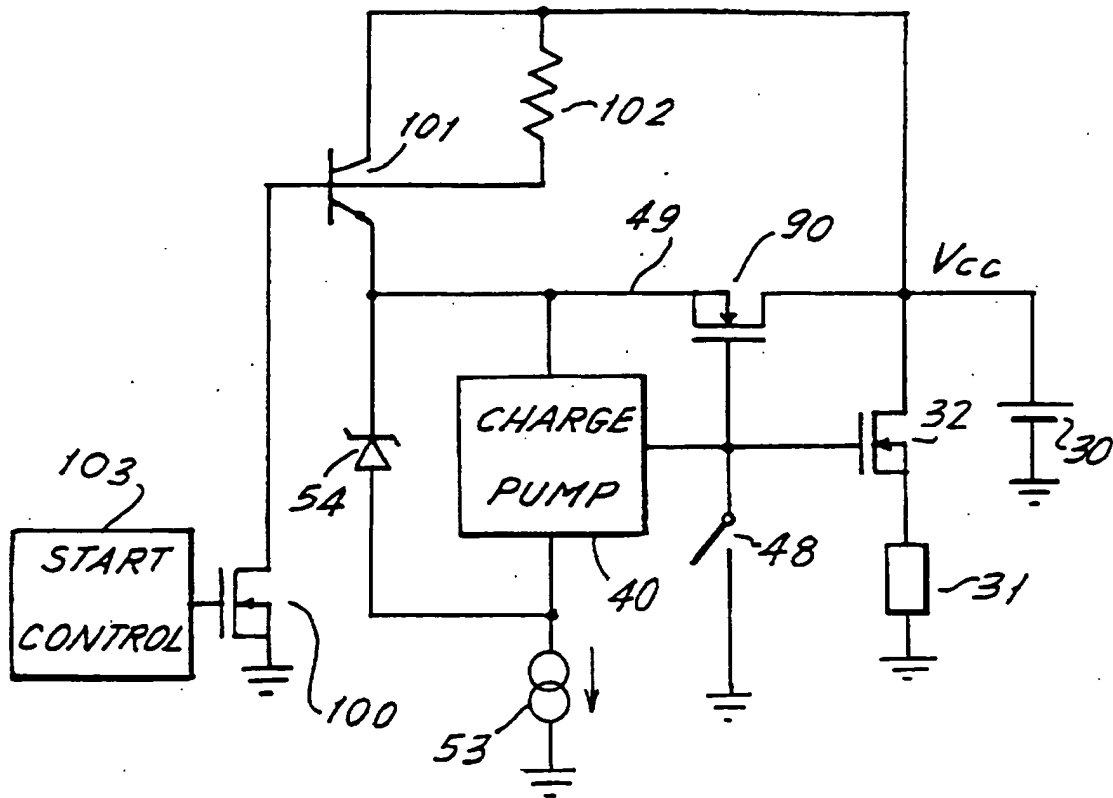
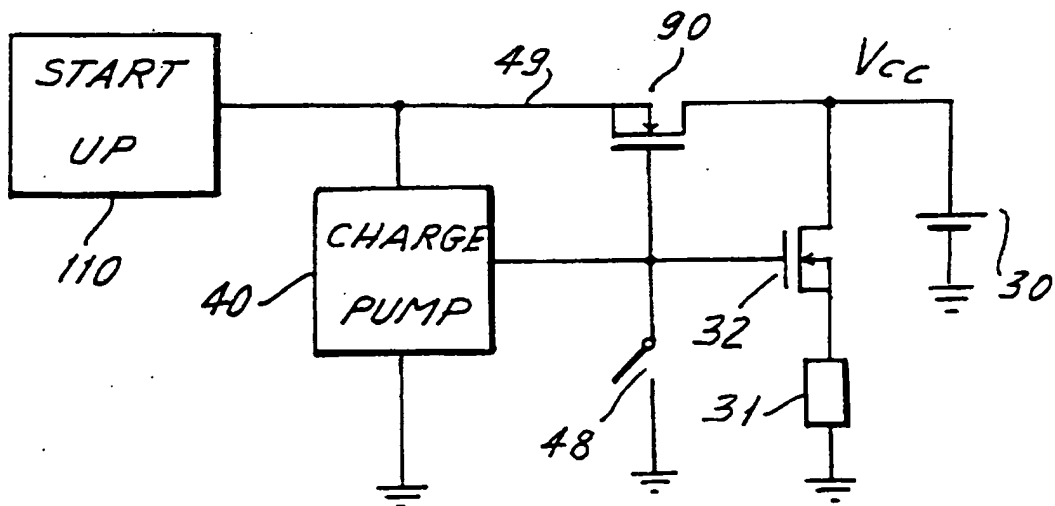
FIG. 9.FIG. 10.

FIG. 11.

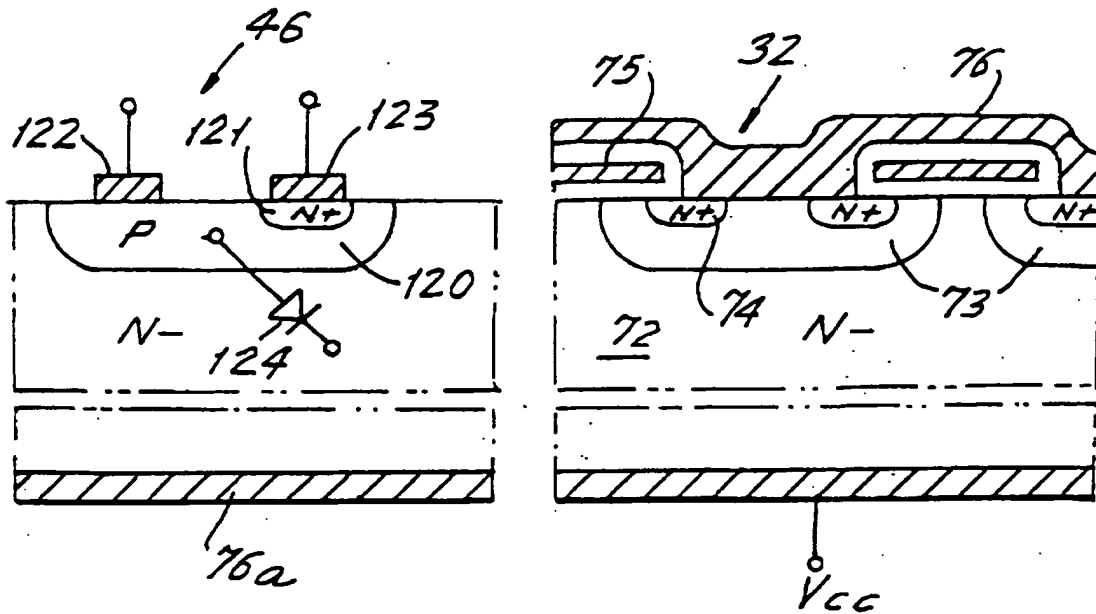


FIG. 12.

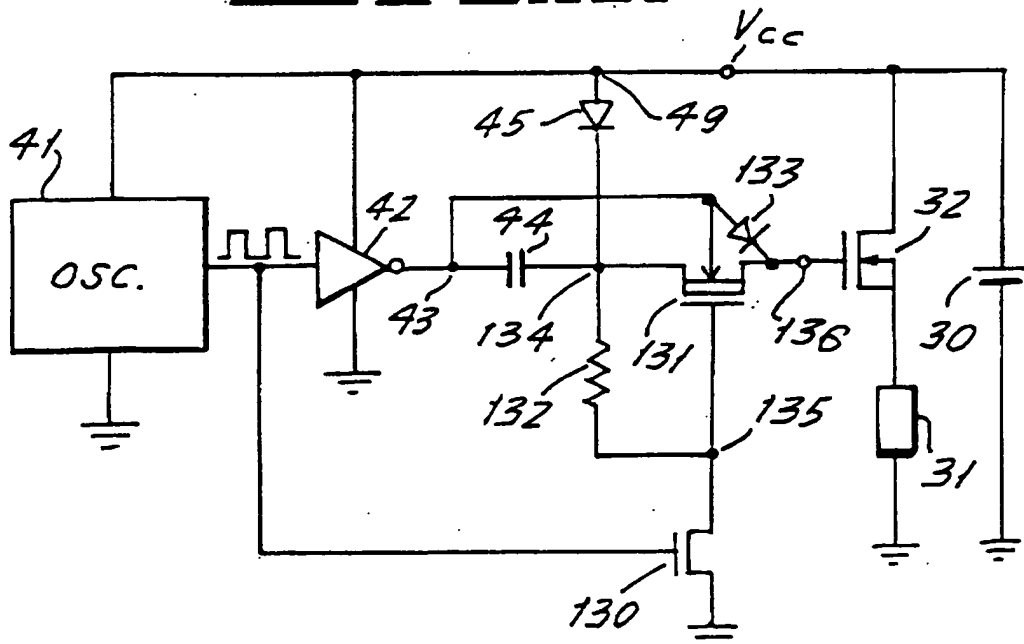


FIG. 14

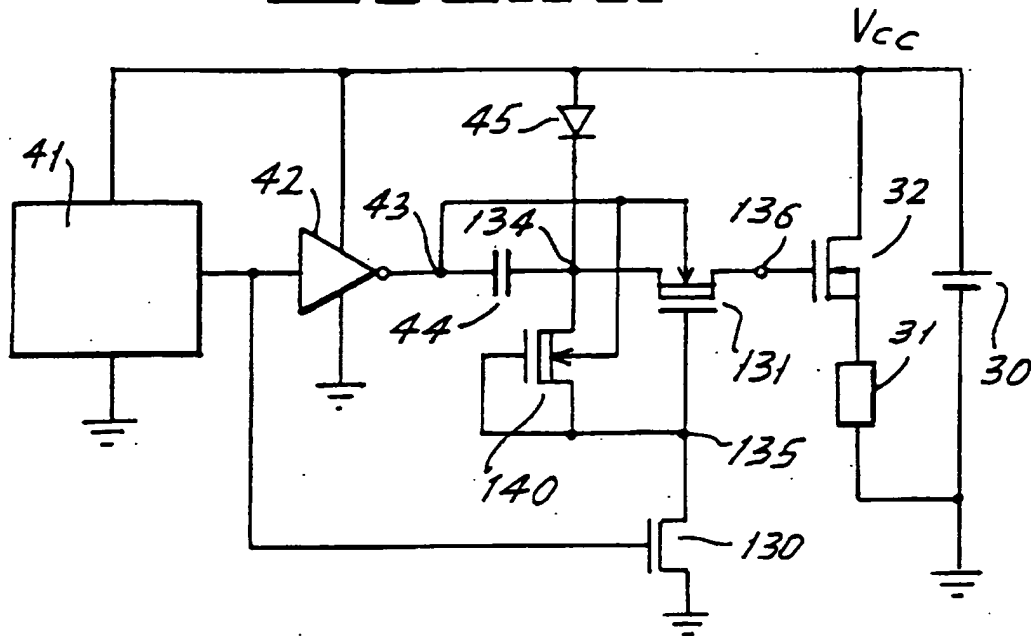


FIG. 13a

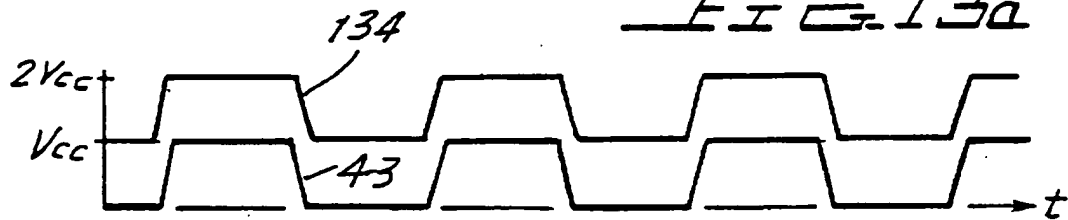


FIG. 13b

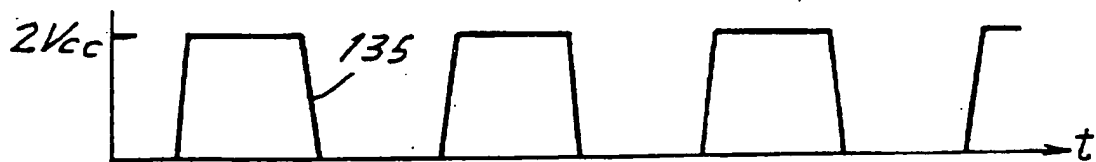


FIG. 13c

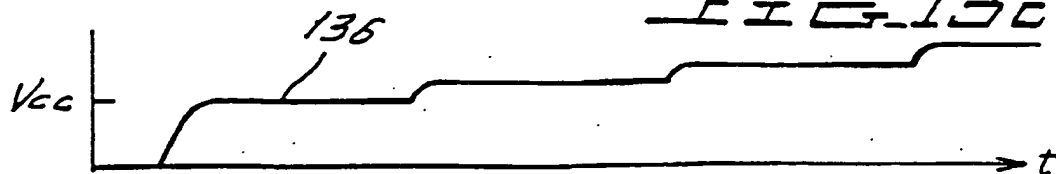


FIG. 15.

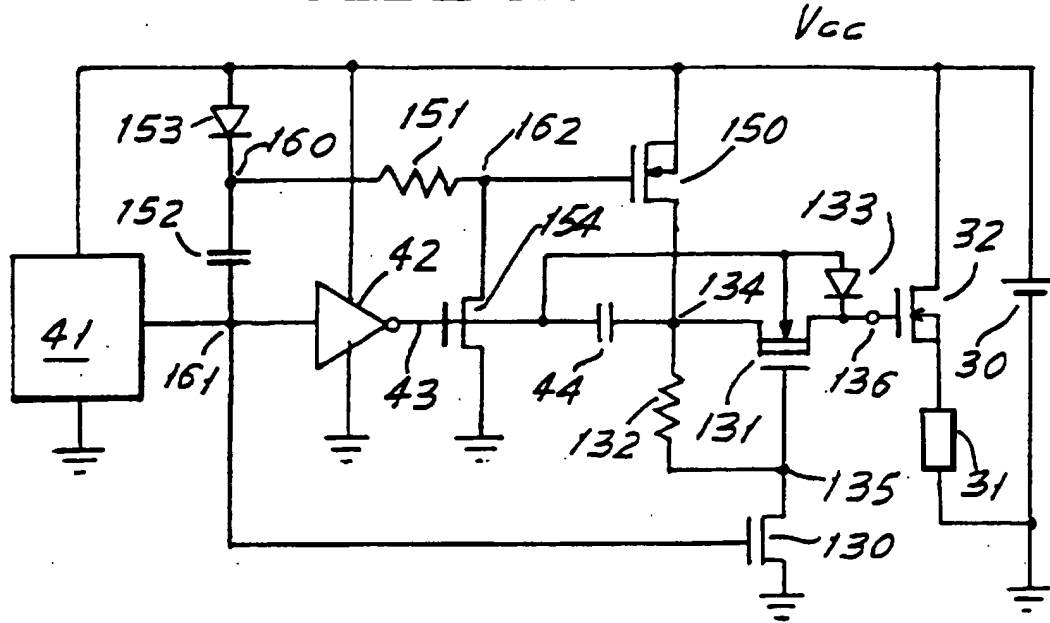


FIG. 16a.

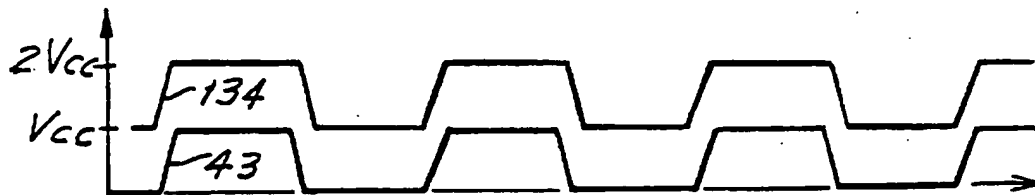


FIG. 16b.

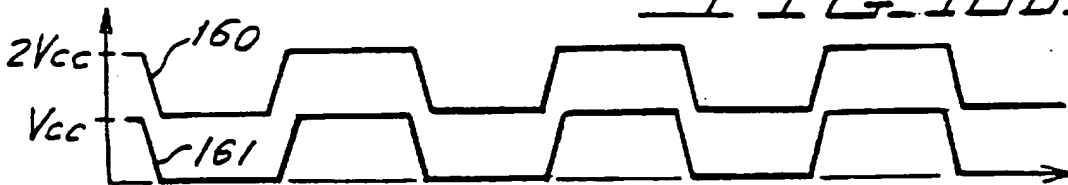
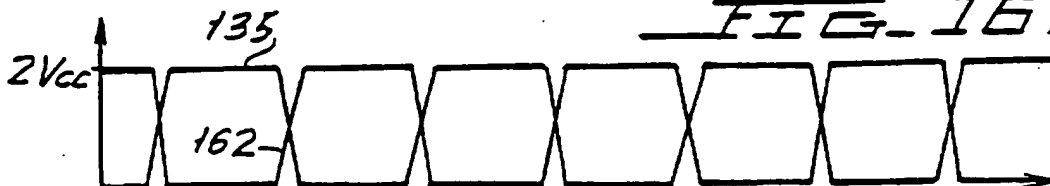
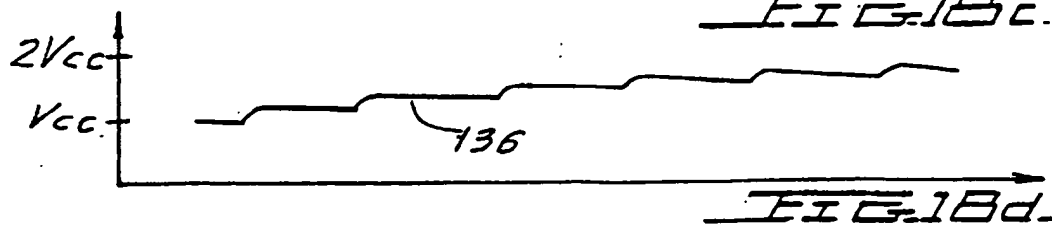
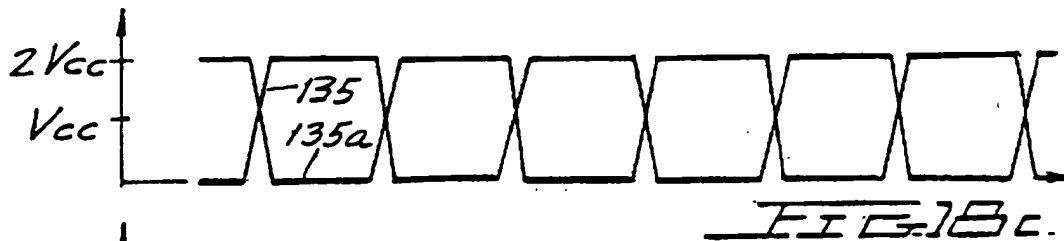
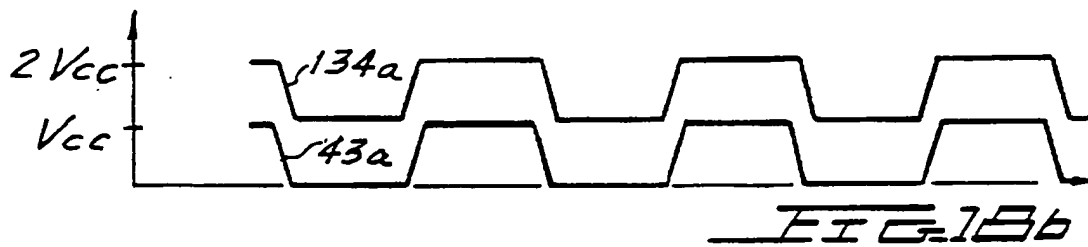
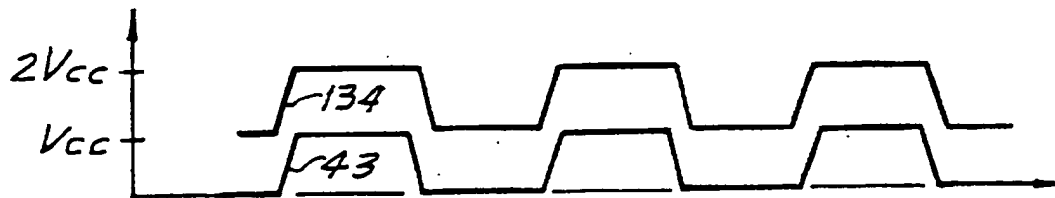
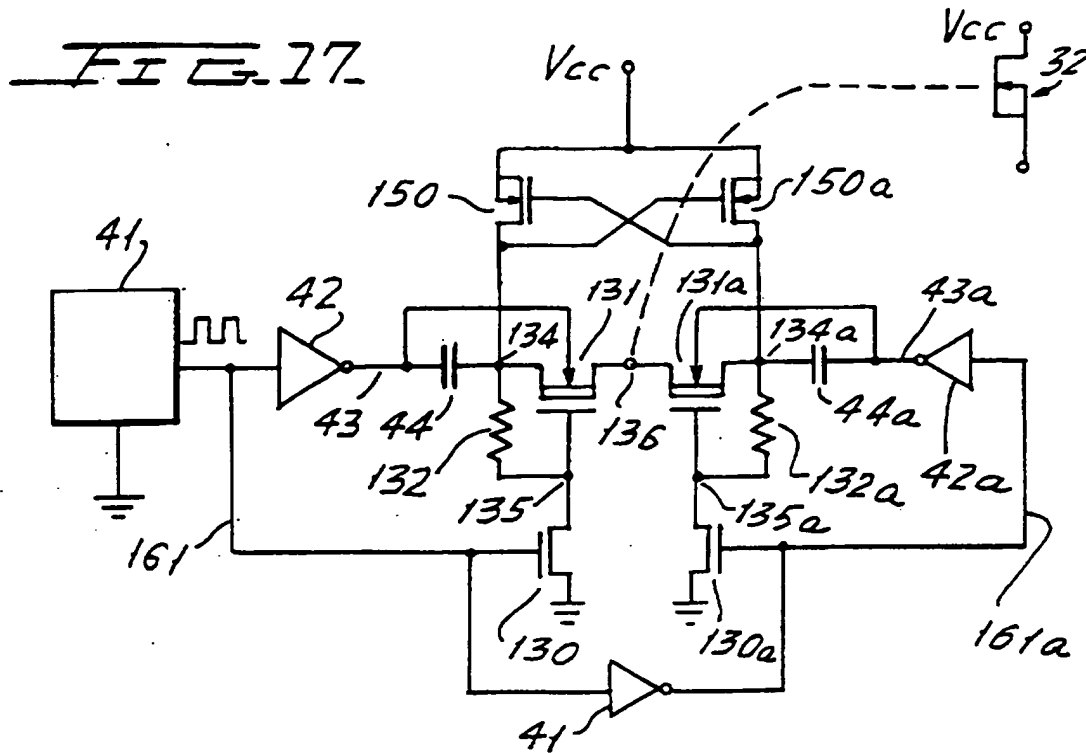


FIG. 16c.





## CHARGE PUMP CIRCUIT FOR HIGH SIDE SWITCH

### BACKGROUND OF THE INVENTION

This invention relates to high side switches, and more particularly relates to a novel circuit for the charge pump of such circuits which has reduced noise, increased efficiency and is more easily integrated into a common semiconductor chip which includes the power device of the high side switch.

High side switches are well-known for numerous applications in which a load with a grounded terminal must be driven from a power supply and which includes a MOSgated power device having a gate terminal which requires a potential higher than that of the power supply to turn on the switch. A "charge pump" circuit is commonly provided to produce the higher voltage needed to turn on the MOS gate controlled ("MOSgated") power device when commanded to do so by an input signal. Such devices are commonly integrated circuit chips in which the power MOSgated device, charge pump and other control circuits are integrated in a common semiconductor chip.

Presently available high side drivers have several problems including the following:

Severe noise is generated in both the supply voltage and ground pins in many applications, due to the high frequency (1 MHz) charging and discharging of the voltage doubling capacitor in the charge pump.

The charge pump capacitor requires an excessively thick oxide and silicon area when integrated into a silicon chip for high supply voltage applications, for example, those greater than 12 volts.

The turn-off switch needed to disconnect the power MOSgated device from the charge pump in the device "off" condition is difficult to implement in an N channel chip embodiment where high voltage P channel control MOSFETs are not available.

The monolithic implementation of the voltage doubler diode in the charge pump is difficult, and it cannot be integrated as a simple P/N diode in the N<sup>-</sup> epitaxial substrate of a conventional integrated circuit employing a self-isolated vertical conduction process.

The output voltage of the charge pump circuit is reduced by the diode forward voltage drops in the charge pump doubler circuit, which has a major effect in low voltage applications.

The present invention provides a novel charge pump circuit for high side switches which has low noise and high efficiency, and is more easily integratable in the same chip containing the power MOSgated device.

### BRIEF DESCRIPTION OF THE INVENTION

In accordance with the present invention, a novel charge pump circuit is provided for a high side switch in which the charge pump is disconnected from the ground terminal of the integrated circuit and is connected instead to a floating node. The floating node is then connected to the integrated circuit ground by a constant current source. Therefore, the current from the source terminal pin is constant, thus reducing noise at the ground and source voltage pins.

Since the charge pump is connected to a floating node, it is possible to clamp the charge pump voltage to a low voltage, even though the output voltage of the device is higher. Therefore, the voltage across the charge pump capacitor is low, even for a high voltage device, and its size is limited.

As a further feature of the invention, a turn-off control switch connected between the charge pump input terminal and the supply source terminal is implemented as an N channel control MOSFET in an integrated circuit chip containing an N channel MOSgated power device section. The control N channel MOSFET is then connected to a positive feedback circuit to the charge pump. A novel starter circuit is employed to initially turn on the control N channel MOSFET.

As a still further feature of the invention, the voltage doubler diodes are implemented as synchronous rectifiers consisting of a MOSFET in place of one diode, and a resistor and MOSFET for the other diode. These components are easily integrated into the N<sup>-</sup> epitaxial substrate of an integrated circuit containing an N channel MOSgated main power device.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a known high side switch.

FIG. 2 shows a prior art charge pump circuit, formed as a voltage doubler, which is used for the circuit of FIG. 1 to provide gate drive for the MOSgated power device.

FIG. 3 shows the gate voltage provided to the MOSgated power device of FIG. 2 as a function of time.

FIG. 4 shows the novel high side circuit of the invention in which any desired charge pump circuit is connected to a floating node.

FIG. 4a shows the circuit of FIG. 4 with a preferred embodiment for a constant current circuit connecting the floating node of any desired charge pump circuit to the integrated circuit ground.

FIG. 5 shows the circuit of FIG. 4 with the charge pump of FIG. 2, and with a modified constant current circuit embodiment.

FIG. 5a shows a preferred implementation in silicon of an added transistor in the constant current circuit of FIG. 5 to enable the device to withstand high voltage.

FIG. 6 shows the current of the constant current circuit, superimposed on the charge pump output current for the circuit of FIG. 5 to demonstrate the reduced noise level at the power and ground pins of the circuit.

FIG. 7 shows the circuit of FIG. 4, modified to employ an auxiliary MOSFET to implement the off switch, schematically shown in FIGS. 4 and 5.

FIG. 8 shows the circuit of FIG. 5 which is modified to contain the auxiliary power MOSFET of FIG. 7 and a novel start-up circuit.

FIG. 9 shows the circuit of FIG. 8 with a modified start-up circuit.

FIG. 10 is a block diagram of a high side circuit, which employs the novel auxiliary MOSFET of FIGS. 7, 8 and 9, in combination with a novel start-up circuit and a known type of grounded charge pump.

FIG. 11 is a cross-section of a portion of an integrated circuit chip which contains a charge pump diode connected to the main device gate to show the problems of its integration into the chip.

FIG. 12 shows the charge pump circuit of FIG. 2 in which the diode connected to the power MOSFET gate is replaced by a transistor and resistor which are easily integratable into a common silicon chip with the power MOSgated device.

FIGS. 13a, 13b and 13c show the operation of the circuit of FIG. 12 on a common time base.

FIG. 14 shows the circuit of FIG. 12 in which the resistor of the resistor-transistor combination is replaced by a depletion mode transistor.

FIG. 15 shows an improvement of the circuit of FIG. 14 to permit the application of the full voltage of  $2V_{cc}$  to the gate of the power device.

FIGS. 16a, 16b and 16c show waveforms which describe the operation of the circuit of FIG. 15.

FIG. 17 shows the circuit of FIG. 15 with a push-pull implementation.

FIGS. 18a to 18d are waveforms on a common time base to explain the operation of the circuit of FIG. 17.

### DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to FIG. 1, there is shown a typical prior art high side switching circuit. Such circuits are used in many applications, for example, automotive, in which it is necessary to drive a load having a grounded terminal. Thus, in FIG. 1, a battery 30 is connected to load 31 through an N channel power MOSFET 32. The negative terminal of battery 30 and one side of load 31 are connected to a common ground, for example, an automobile chassis. The positive terminal of battery 30 is at a voltage  $V_{cc}$ , which may be 12 volts. The power MOSFET 32 may be any other desired MOSgated device, such as an IGBT, or MOSgated thyristor or the like.

When MOSFET 32 is in the on state, its source is close to the power supply potential  $V_{cc}$ . In order to have a low drain-to-source voltage drop, it is necessary to bias the gate G of MOSFET 32 at a potential of 5 to 10 volts above the potential of source S, which is 5 to 10 volts above  $V_{cc}$ . In most cases, particularly where the high side switch is implemented as a stand-alone IC, no supply voltage above  $V_{cc}$  is available in the system, and a voltage above  $V_{cc}$  has to be generated on the chip. This is commonly done by a capacitive voltage multiplier, often called a charge pump.

FIG. 2 shows a known voltage doubler circuit 40 commonly used in high side switches, connected to the high side switch of FIG. 1. The doubler circuit 40 employs a square wave oscillator circuit 41, the output of which is bufferized by buffer 42. The output node 43 of buffer 42 is connected to capacitor 44 which is connected to and charged through diode 45 from source  $V_{cc}$ . The node between capacitor 44 and diode 45 is connected to diode 46 which is, in turn, connected to the gate of MOSFET 32. Two switching devices, shown as switches 47 and 48, are provided in which switch 47 is operable to connect and disconnect node 49 from power supply 30 and switch 48 closes in the MOSFET 32 off state to pull the gate of MOSFET 32 to ground (or to the source of MOSFET 32).

The charge pump 40 operates as follows:

When node 43 at the output of buffer 42 is low, capacitor 44 is charged from  $V_{cc}$  through diode 45. When the node 43 at the output of buffer 42 is high, the charge of capacitor 44 is transferred to the gate of MOSFET 32, through diode 46. The voltage on the gate of MOSFET 32 then increases in step fashion, as shown in FIG. 3, and the voltage at the gate of MOSFET 32 approaches  $2V_{cc}$  to turn on MOSFET 32.

To turn off MOSFET 32, switch 48 closes to pull the gate voltage to ground and switch 47 is opened to isolate node 49 from the power supply.

The circuit of FIG. 2 has the following drawbacks:

1. The charging and discharging of capacitor 44 at high frequency, typically 1 MHz, generates high frequency current in the  $V_{cc}$  and ground pin nodes and related package pins of the IC 40, causing severe noise problems in many applications.
2. It is difficult to implement switch 47 into a single silicon chip for the entire circuit with most available processes, especially when no P channel MOSFETs are available.
3. It is difficult to extend the use of the circuit to applications with high  $V_{cc}$  voltages because the full  $V_{cc}$  is applied across capacitor 44. Therefore, to implement capacitor 44 in an integrated circuit for high voltage, prohibitively thick oxides and greater silicon area are required.

FIG. 4 shows a first embodiment of the present invention, in which the circuit of FIG. 2 is modified by connecting the ground lead 50 of charge pump 40 (shown as a block in FIG. 4) to a floating node 51. The floating node 51 is then connected to ground 52 by a constant current source circuit 53. A voltage regulator, for example, a zener diode 54 connects nodes 49 and 51.

The charge pump 40 can be of any desired type, including, but not limited to that of FIG. 2. A significant feature of the circuit of FIG. 4 is that the charge pump 40 is connected to floating node 51 instead of the ground node 52. The current in the ground pins and  $V_{cc}$  pins of the circuit will therefore be pure direct current, in view of the constant current source 53, so that the operation of charge pump 40 generates no noise at these pins.

FIG. 4a shows the circuit of FIG. 4 with constant current source 53 implemented as MOSFET 60, the gate of which is driven by cascade control MOSFETs 61 and 62 which are enhancement and depletion mode MOSFETs respectively.

FIG. 5 shows the circuit of FIG. 4, using the charge pump of FIG. 2 and a modified constant current source. More specifically, the current source in FIG. 5 includes an added N channel MOSFET 70 which is easily integrated, as will be later described.

In the circuit of FIGS. 4, 4a and 5, the supply voltage  $V_{cc}$  is greater than the knee voltage of zener diode 54. If the current in the constant current circuit 53 is greater than the current  $i_{d1}$  of charge pump 41 then, as shown in FIG. 6, the current in the ground and  $V_{cc}$  pins (or terminals) of the IC circuit will be a pure direct current. Therefore, the high frequency current of the charge pump generates zero or very low noise. Presently available high side switches, such as the IR6000, made by International Rectifier Corporation, and the BTS410E made by Siemens have peak-to-peak  $V_{cc}$ /ground currents in excess of 0.1 milliampere. Circuits employing the floating node 53 of FIGS. 4, 4a and 5 have a noise of 20 microamperes peak-to-peak which is hardly discernable from background noise.

A further advantage of the circuits of FIGS. 4, 4a and 5 is that the voltage across capacitor 44 is limited to the zener voltage ( $V_{cc} - V_{z1}$ ) where  $V_{z1}$  is the voltage at node 51. Therefore, a high voltage charge pump circuit can be built with low voltage capacitors with thin oxides and smaller die area without sacrificing reliability. By way of example, the circuit of FIG. 5 may operate with a  $V_{cc}$  of up to 60 volts while the voltage applied to the charge pump capacitor is limited to 7 volts.

As previously mentioned, the constant current circuit 53 in FIG. 5 contains an added MOSFET 70. MOSFET 70 is a relatively high voltage MOSFET to be used in high voltage applications to remove high voltage from MOSFET 60. A

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fixed gate voltage, for example, 7 volts, is applied to the gate of MOSFET 70 and it is easily integrated into the common chip which contains all other circuit elements of FIG. 5.

The implementation of MOSFET 70 as a lightly doped drain MOSFET is shown in FIG. 5a which is a cross-section of a portion of the chip. Thus, the chip 71 has a lightly doped N<sup>-</sup> substrate 72 which receives all of the junctions which make up the circuit. The power section of the chip which defines the power MOSFET 32 consists of any desired junction pattern and can be a vertical conduction device having a plurality of spaced P base diffusions 73 which contain respective sources, such as N<sup>+</sup> source 74. The channel regions of each of bases 73 are covered by a MOSgate 75 which may be a polysilicon gate. The gate 75 is conventionally insulated from source electrode 76 which contacts each of the bases 73 and their respective sources 74. A drain electrode 76a is formed on the bottom of chip 72 and is connected to V<sub>cc</sub>.

P-wells, such as P-well 77, are also diffused into the same chip to contain control circuits for the main power device. FIG. 5a shows one such P-well 77 which contains MOSFET 70. Thus, MOSFET 70 is an N channel device comprising an N<sup>+</sup> source diffusion 78, an N<sup>-</sup> drain diffusion 79 and an N<sup>+</sup> drain contact diffusion 80. Its polysilicon gate 81 extends across the P channel region between diffusions 78 and 79. Thus, the MOSFET 70 is easily formed in chip 71, using many of the same process steps which form the power section 32.

The chip 71 is conventionally housed after its completion and externally available terminal pins extend through the housing to the various electrodes of the device. Thus, a V<sub>cc</sub> terminal pin will be connected to the drain electrode 76a and a source terminal pin will be connected to the source electrode at node 82 in FIGS. 4a and 5. A ground terminal pin will also be connected to the ground nodes in the chip 71 which are shown in the circuit of FIGS. 4a and 5.

FIG. 7 shows the circuit of FIG. 4 with the switch 47 implemented as an auxiliary N channel power MOSFET 90 which can easily be integrated into the IC chip 71 of FIG. 5a with any conventional power MOSFET process since MOSFETs 32 and 90 have a common drain.

Switch 48 in FIG. 7 is implemented as a lateral NMOS transistor with a lightly doped drain, similar to MOSFET 70.

During steady state operation of the circuit of FIG. 7, charge pump 40 provides a voltage at node 91 which is connected to the gate of power MOSFET 90 which is 5 to 10 volts above V<sub>cc</sub>. MOSFET 90 is thus turned fully on and the charge pump 40 receives power from V<sub>cc</sub>.

In order to turn on the circuit of FIG. 7, a start-up circuit is needed, as shown in FIG. 8, to initially pull up node 49 to start the charge pumping action. Thus, in FIG. 8, a start up circuit consisting of diode 91, switch 92 and voltage source 93 are provided. Voltage source 93 has a low voltage which may be derived from V<sub>cc</sub>. Switch 92 may be implemented as a low voltage transistor.

In operation of the circuit of FIG. 8, at turn on, switch 92 closes to provide an initial voltage to charge pump 40. The charge pump 40 will then begin to supply itself from V<sub>cc</sub> through transistor 90 which is turned on and the circuit will operate as previously described.

FIG. 9 shows another embodiment of the start-up circuit of FIG. 8 and employs transistors 100 and 101 and resistor 102. In operation of the circuit of FIG. 9, at turn-on, the gate of transistor 100 is pulled to ground by start control circuit 103. The base of bipolar transistor 101 is pulled up by resistor 102 which is implemented as a depletion mode transistor which has a high resistance value equivalent to

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about 1 megohm. Thus, node 49 is pulled up to (V<sub>cc</sub>-0.6) volts, starting the charge pump 40 operation.

The novel auxiliary MOSFET 90 and any desired start-up circuit 110 can be used with the circuit of FIG. 2 in which the charge pump 40 is referenced to ground, as well as with the novel charge pump circuit with a floating node as in FIG. 4. FIG. 10 is a block diagram of such a circuit.

The charge pump circuit of the preceding figures employs diode 46 in the charging circuit. It is difficult and sometimes impossible to integrate this diode into a monolithic integrated circuit. FIG. 11 shows an attempt to integrate diode 46 into the P-well 120 in the N<sup>-</sup> substrate 72 of FIG. 5a. Diode 46 is formed by N<sup>+</sup> diffusion 121 in well 120. Electrodes 122 and 123 are connected to regions 120 and 121 respectively to form the electrodes of the diode 46. Since the epitaxial substrate 72 is the drain of power MOSFET 32, and is connected to V<sub>cc</sub>, diode 46 cannot be integrated as a simple PN diode because its anode has to be able to float several volts above V<sub>cc</sub>. However, this is impossible because of the parasitic diode 124 between the anode of diode 46 and V<sub>cc</sub>. A simple integration of diode 46 is therefore impossible.

Another drawback of the diodes 45 and 46 in the charge pump of FIG. 2 is that they reduce the output voltage of the charge pump 40 by their forward voltage drops to (2 V<sub>cc</sub>-2 V<sub>p</sub>) (where 2 V<sub>p</sub> is the forward voltage drop of diodes 45 and 46). This can be a substantial reduction for low V<sub>cc</sub> applications such as laptop computers or automotive applications.

FIG. 12 shows a modified charge pump circuit in which diode 46 is replaced by more easily integratable components and with a reduced forward voltage drop in the output of the charge pump circuit. Thus, diode 46 is replaced by enhancement mode transistor 130, depletion mode transistor 131, resistor 132, and a substrate diode 133 of transistor 131. These components are easily integrated into the substrate 72 of FIG. 11.

The operation of the circuit of FIG. 12 is described as follows, in connection with FIGS. 13a, 13b and 13c which show the voltages at nodes 134-43, 135, and 136 respectively. Thus, the first time the output of buffer 42 at node 43 goes high, the node 136 at the gate of MOSFET 32 charges up to (V<sub>cc</sub>-V<sub>p</sub>), through the substrate diode 133 of depletion mode transistor 131. When the output at node 43 goes low, capacitor 44 charges up through diode 45. During this period, transistor 131 is in its off state; its source at node 134 and its drain at node 136 being at (V<sub>cc</sub>-V<sub>p</sub>) while its gate at node 135 and its substrate are at 0 volts. Thus, transistor 131 is off and the gate of power MOSFET 32 is isolated from the remainder of the circuit.

When node 43 goes high, node 134 rises to (2 V<sub>cc</sub>-V<sub>p</sub>). Transistor 130 then turns off, enabling the gate of transistor 131 to reach the potential of its source through resistor 132. Since transistor 131 is a depletion mode device, it turns on with 0 volts between gate and source. Therefore, the charge on capacitor 44 will transfer to the gate of MOSFET 32 through transistor 131.

This process continues each cycle until the node 136 potential shown in FIG. 13c reaches the limit of (2 V<sub>cc</sub>-V<sub>p</sub>). Note that this limit is higher than that of the prior art circuit of FIG. 2 by one diode drop V<sub>p</sub> because there is only one diode in the current path. Furthermore, transistors 130, 131 and resistor 132 may be easily integrated into the IC because the substrate of transistor 131 never exceeds V<sub>cc</sub>.

FIG. 14 shows an embodiment of the circuit of FIG. 12 in which resistor 132 of FIG. 12 is replaced by a depletion mode MOSFET 140 which is easily integrated into the IC substrate.



FIG. 15 shows a modification of the circuit of FIG. 12 which even further reduces the voltage drop of the output of the charge pump at the gate of MOSFET 32 and eliminates all diode drops. Thus, transistor 150, resistor 151, capacitor 152, diode 153 and transistor 154 are added to the circuit of FIG. 15 to avoid the drop produced by diode 45 in FIG. 12. Note that MOSFET 150 replaces diode 45 of the circuit of FIG. 12.

The operation of the circuit of FIG. 15 is best understood from the curves of FIGS. 16a, 16b and 16c. The potentials at nodes 134-43, 160-161 and 135-162 respectively in FIG. 15 are shown in FIGS. 16a, 16b and 16c. The first time the output at node 43 goes high, the gate of power MOSFET 32 at node 136 charges to  $(V_{cc}-V_p)$  through the substrate diode 133 of depletion mode transistor 131. At the same time, node 161 is low and capacitor 152 is charged up to  $(V_{cc}-V_p)$  through diode 153.

When node 161 goes high, node 43 goes low. Since capacitor 152 is already charged to  $(V_{cc}-V_p)$ , node 160 will be boosted to  $(2V_{cc}-V_p)$ . Since transistor 154 is off, node 162 will also be boosted to  $(2V_{cc}-V_p)$  and transistor 150 will be fully "on." Capacitor 44 will then charge up to  $V_{cc}$  through transistor 150. For the same reasons described in connection with the circuit of FIG. 12, transistor 131 will be off during this time and the gate of MOSFET 32 is isolated from the circuit.

When node 43 next goes high, transistor 154 turns on and node 162 falls to 0 volts, turning off transistor 150, allowing node 134 to rise to  $2V_{cc}$ . For the same reasons as in FIG. 12, transistor 131 turns on and the charge on capacitor 44 will transfer through the transistor 131 to the gate of MOSFET 32.

The same process repeats each cycle until the voltage at node 136 reaches  $2V_{cc}$ . Thus, the voltage at node 136 is  $2V_f$  higher than that of the charge pump of FIG. 2 because there is no diode in the current path.

FIG. 17 shows the basic circuit of FIG. 8 implemented as a push-pull circuit. The two halves of the circuit are symmetric, the left-hand side of the circuit using the same numerals as in FIG. 8 and the right-hand side of the circuit using the same numerals with the suffix "a". Only a portion of the high side switch is shown, particularly the power MOSFET 32 having its gate connected to node 136 as shown by the dotted-line connection.

The operation of the circuit of FIG. 17 is best understood by reference to FIGS. 18a, 18b, 18c and 18d which show the voltages at nodes 134-43, 134a-43a, 135-135a and 136 in FIG. 17 respectively. It will be seen in FIGS. 18a, 18b and 18c that the potentials at nodes 134, 43 and 135 are in opposite phase to the potentials at nodes 134a, 43a and 135a respectively.

When node 43 is low, node 43a is at  $V_{cc}$  and node 134a is at  $2V_{cc}$ . Therefore, transistor 150 is fully "on" and capacitor 44 is charged up to  $V_{cc}$  through transistor 150. During this period, transistor 130 is "on" so that transistor 131 is "off." Similarly, transistor 130a is "off" so that transistor 131a is "on" and the charge of capacitor 44a is transferred to the node 136 and the gate of power MOSFET 32.

Node 43 then goes to  $V_{cc}$  and node 134 is boosted to  $2V_{cc}$ . This turns transistor 150a fully "on," which turns "off" transistor 150 and prevents the discharge of capacitor 44 through transistor 150. Since transistor 150a is "on" and node 43a is low, capacitor 44a will be charged up to  $V_{cc}$  through transistor 150a. During this period, transistor 130a is "on" so transistor 131a is "off." Similarly, transistor 130 is "off" so transistor 131 is "on" and the charge of capacitor 44 is transferred to the gate of power MOSFET 32.

The same process takes place at each clock half cycle until the voltage on the gate of MOSFET 32 reaches the limit of  $2V_{cc}$ . As in the circuit of FIG. 12, the output voltage of the charge pump is unaffected by any diode drop because there is no diode in the current path.

Note that the circuit of FIG. 17 doubles the apparent frequency of the charge pump and thus reduces the ripple at node 136 by a factor of 2.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; and a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing, in conjunction with said constant current source sinking current from said charge pump, a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device.

2. The circuit of claim 1 wherein said gate controlled MOS power semiconductor device is a power MOSFET.

3. The circuit of claim 1 which further includes voltage clamp means connected between said first and second power terminals of said charge pump circuit to limit the voltage therebetween.

4. The circuit of claim 3 wherein said voltage clamp means comprises a zener diode.

5. The circuit of claim 1 wherein said charge pump circuit comprises, in combination: a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit and having an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, a charge storage capacitor, a first diode and a second diode; said inverter buffer having an output connected in series with said capacitor and said first diode to said control electrode of said gate controlled MOS power device; said second diode connected from said  $V_{cc}$  input voltage terminal to the node between said capacitor

and said first diode whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second diode and, when said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first diode to said control terminal of said gate controlled MOS power device.

6. The circuit of claim 5 which further includes voltage clamp means connected between said first and second power terminals of said charge pump circuit to limit the voltage therebetween.

7. The circuit of claim 6 wherein said voltage clamp means comprises a zener diode.

8. The circuit of claim 3 wherein said charge pump circuit comprises, in combination: a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit and having an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, a charge storage capacitor, a first diode and a second diode; said inverter buffer having an output connected in series with said capacitor and said first diode to said control electrode of said gate controlled MOS power device; said second diode connected from said  $V_{cc}$  input voltage terminal to the node between said capacitor and said first diode whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second diode and, when said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first diode to said control terminal of said gate controlled MOS power device.

9. The circuit of claim 1 wherein said gate controlled MOS power semiconductor device, said charge pump circuit, and said current source are integrated into a monolithic semiconductor chip.

10. The circuit of claim 1 wherein said charge pump circuit comprises, in combination, a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit, an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, and a charge storage capacitor; said inverter buffer having an output connected to said capacitor; a first coupling circuit means coupling said capacitor to said control electrode of said gate controlled MOS power semiconductor device; a second coupling circuit means for coupling said  $V_{cc}$  input voltage terminal to the node between said capacitor and said first coupling circuit means whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second coupling means and, when said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first coupling means to said control terminal of said gate controlled MOS power semiconductor device.

11. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor

device is closed; a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; and first switching means operable to connect and disconnect said charge pump first power terminal to said  $V_{cc}$  input voltage terminal and second switching means for connecting and disconnecting said control electrode of said gate controlled MOS power device to said ground terminal when said first switching means disconnects and connects said pump first power terminal to said  $V_{cc}$  input terminal respectively.

12. The circuit of claim 11 wherein said gate controlled MOS power semiconductor device, said charge pump circuit, said first switching means and said current source are integrated into a monolithic semiconductor chip.

13. The circuit of claim 11 wherein said gate controlled MOS power semiconductor device, said charge pump circuit, said voltage clamp means and said current source are integrated into a monolithic semiconductor chip.

14. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; voltage clamp means connected between said first and second power terminals of said charge pump circuit to limit the voltage therebetween; and first switching means operable to connect

and disconnect said charge pump first power terminal to said  $V_{cc}$  input voltage terminal and second switching means for connecting and disconnecting said control electrode of said gate controlled MOS power device to said ground terminal when said first switching means disconnects and connects said pump first power terminal to said  $V_{cc}$  input terminal respectively.

15. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; and first switching means operable to connect and disconnect said charge pump first power terminal to said  $V_{cc}$  input voltage terminal and second switching means for connecting and disconnecting said control electrode of said gate controlled MOS power device to said ground terminal when said first switching means disconnects and connects said pump first power terminal to said  $V_{cc}$  input terminal respectively; wherein said charge pump circuit comprises, in combination: a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit and having an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, a charge storage capacitor, a first diode and a second diode; said inverter buffer having an output connected in series with said capacitor and said first diode to said control electrode of said gate controlled MOS power device; said second diode connected from said  $V_{cc}$  input voltage terminal to the node between said capacitor and said first diode whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second diode and, when said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first diode to said control terminal of said gate controlled MOS power device.

16. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals

and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; and a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; and wherein said constant current circuit comprises a first control MOSFET having drain and source electrodes connected to said second power terminal of said charge pump circuit and said ground terminal respectively and a cascaded enhancement mode MOSFET and depletion mode MOSFET connected between an auxiliary voltage source and said ground terminal; the node between said enhancement mode and depletion mode MOSFETs connected to their respective gates and to the gate of said first control MOSFET.

17. The circuit of claim 16 which further includes a second control MOSFET in combination with said first MOSFET to increase the voltage between said second power terminal of said charge pump circuit and said ground terminal without breakdown of said first control MOSFET.

18. The circuit of claim 16 which further includes voltage clamp means connected between said first and second power terminals of said charge pump circuit to limit the voltage therebetween.

19. The circuit of claim 17 which further includes voltage clamp means connected between said first and second power terminals of said charge pump circuit to limit the voltage therebetween.

20. The circuit of claim 18 wherein said voltage clamp means comprises a zener diode.

21. The circuit of claim 19 wherein said voltage clamp means comprises a zener diode.

22. The circuit of claim 17 wherein said charge pump circuit comprises, in combination: a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit and having an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, a charge storage capacitor, a first diode and a second diode; said inverter buffer having an output connected in series with said capacitor and said first diode to said control electrode of said gate controlled MOS power device; said second diode connected from said  $V_{cc}$  input voltage terminal to the node between said capacitor and said first diode whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second diode and, when

said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first diode to said control terminal of said gate controlled MOS power device.

23. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; add an auxiliary power MOSFET having first and second power terminals and a gate terminal; said first and second power terminals of said auxiliary power MOSFET connected to said first power terminal of said charge pump circuit and said  $V_{cc}$  input voltage terminal respectively; said gate terminal of said auxiliary power MOSFET connected to said control electrode of said gate controlled MOS power semiconductor device.

24. The circuit of claim 23 which further includes starter circuit means coupled between a auxiliary supply voltage source and said charge pump circuit for starting said charge pump circuit before said auxiliary power MOSFET conducts.

25. The circuit of claim 23 wherein said gate controlled MOS power semiconductor device, said charge pump circuit, said auxiliary power MOSFET and said current source are integrated into a monolithic semiconductor chip.

26. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load which, when said grounded load is connected to said load terminal and said  $V_{cc}$  input is connected to said source of power, is energized from said source of power when said gate controlled MOS power semiconductor device is closed; and a ground terminal connectable to said grounded load; said

charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said second power terminal of said charge pump circuit connected to said ground terminal, whereby said output terminal of said charge pump circuit is connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; a grounding switch connected to said control electrode of said MOS gated power device for grounding said control electrode when said grounding switch is closed; and an auxiliary power MOSFET having first and second power terminals and a gate terminal; said first and second power terminals of said auxiliary power MOSFET connected to said first power terminal of said charge pump circuit and said  $V_{cc}$  input voltage terminal respectively; said gate terminal of said auxiliary power MOSFET connected to said control electrode of said gate controlled MOS power semiconductor device so that when said grounding switch is closed, said gate terminal of said auxiliary power MOSFET is grounded, thereby turning off said auxiliary power MOSFET to entirely electrically isolate said charge pump circuit from said supply voltage.

27. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load which, when said grounded load is connected to said load terminal and said  $V_{cc}$  input is connected to said source of power, is energized from said source of power when said gate controlled MOS power semiconductor device is closed; and a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said second power terminal of said charge pump circuit connected to said ground terminal, whereby said output terminal of said charge pump circuit is connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device; a grounding switch connected to said control electrode of said MOS gated power device for grounding said control electrode when said grounding switch is closed; an auxiliary power MOSFET having first and second power terminals and a gate terminal; said first and second power terminals of said auxiliary power MOSFET connected to said first power terminal of said charge pump circuit and said  $V_{cc}$  input voltage terminal respectively; said gate terminal of said auxiliary power MOSFET connected to said control electrode of said gate controlled MOS power semiconductor device so that when said grounding switch is closed, said gate terminal of said auxiliary power MOSFET is grounded, thereby turning off said auxiliary power MOSFET to electrically isolate said charge pump circuit from said supply voltage; and starter circuit means coupled between an auxiliary supply voltage source and said charge pump circuit for starting said charge pump circuit before said auxiliary power MOSFET conducts.

28. A high side switch circuit comprising, in combination: a gate controlled MOS power semiconductor device having

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first and second power electrodes and a control electrode; a charge pump circuit having first and second power terminals and an output terminal; a constant current source circuit having input and output terminals; a  $V_{cc}$  input voltage terminal connected to said first power electrode of said gate controlled MOS power semiconductor device and connectable to a source of power; a load terminal connected to said second power electrode of said gate controlled MOS power semiconductor device and connectable to a grounded load that is capable of being energized from said source of power when said gate controlled MOS power semiconductor device is closed; a ground terminal connectable to said grounded load; said charge pump circuit being operable to produce an output voltage at its said output terminal which is higher than said  $V_{cc}$  input voltage; said first power terminal of said charge pump circuit being connected with said  $V_{cc}$  input voltage terminal; said second power terminal of said charge pump circuit connected to said input terminal of said constant current circuit; said output terminal of said constant current circuit connected to said ground terminal, whereby said second power terminal has a floating potential and the currents at said  $V_{cc}$  input voltage terminal and at said ground terminal are constant so that noise at said  $V_{cc}$  input terminal and at said ground terminal is reduced; said output terminal of said charge pump circuit being connected to said control electrode of said gate controlled MOS power semiconductor device for providing a voltage sufficiently higher than the voltage of said second terminal to turn on said gate controlled MOS power semiconductor device: wherein said charge pump circuit comprises, in combination, a square wave oscillator connected to and operated from said first and second power terminals of said charge pump circuit, an oscillator output terminal, an inverter buffer connected to said oscillator output terminal, and a charge storage capacitor; said inverter buffer having an output connected to said capacitor; a first coupling circuit means coupling said

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capacitor to said control electrode of said gate controlled MOS power semiconductor device; a second coupling circuit means for coupling said  $V_{cc}$  input voltage terminal to the node between said capacitor and said first coupling circuit means whereby, when the output of said inverter buffer is low, said capacitor is charged from the voltage at said  $V_{cc}$  terminal and through said second coupling means and, when said output of said inverter buffer is high, the voltage of said capacitor plus the voltage of said  $V_{cc}$  terminal are applied in series through said first coupling means to said control terminal of said gate controlled MOS power semiconductor device; and wherein said first coupling means comprises a depletion mode MOSFET having source and drain terminals connected to said capacitor and to said control electrode of said gate controlled MOS power semiconductor device respectively, said depletion mode MOSFET having a substrate diode connected to the output of said inverter buffer; a resistive circuit means connected from said capacitor to the gate of said depletion mode MOSFET, and a second control MOSFET connected from said gate of said depletion mode MOSFET to said ground terminal and having a gate connected to said oscillator output terminal.

29. The circuit of claim 28 wherein said second coupling means is a diode.

30. The circuit of claim 28 wherein said resistive circuit means comprises a second depletion mode MOSFET having a gate connected to the gate of said first-mentioned depletion mode transistor and a substrate connected to the substrate of said first-mentioned depletion mode MOSFET.

31. The circuit of claim 10 wherein said second coupling circuit means includes a control MOSFET.

32. The circuit of claim 28 wherein said second coupling circuit means includes a control MOSFET.

\* \* \* \* \*



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# United States Patent [19] Martin

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[54] **FREQUENCY-VARIABLE OSCILLATOR  
CONTROLLED HIGH EFFICIENCY  
CHARGE PUMP**

5,038,325 8/1991 Douglas et al. .... 365/189.06  
5,389,898 2/1995 Taketoshi et al. .... 331/57  
5,426,334 6/1995 Skovmand .... 327/544  
5,461,591 10/1995 Kim et al. .... 327/534

[75] Inventor: **Chris G. Martin, Boise, Id.**

*Primary Examiner*—Siegfried H. Grimm  
*Attorney, Agent, or Firm*—Fletcher & Associates

[73] Assignee: **Micron Technology, Inc., Boise, Id.**

[57] **ABSTRACT**

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[58] Field of Search ..... **331/57, 179, 75;  
365/203, 189.09; 327/536**

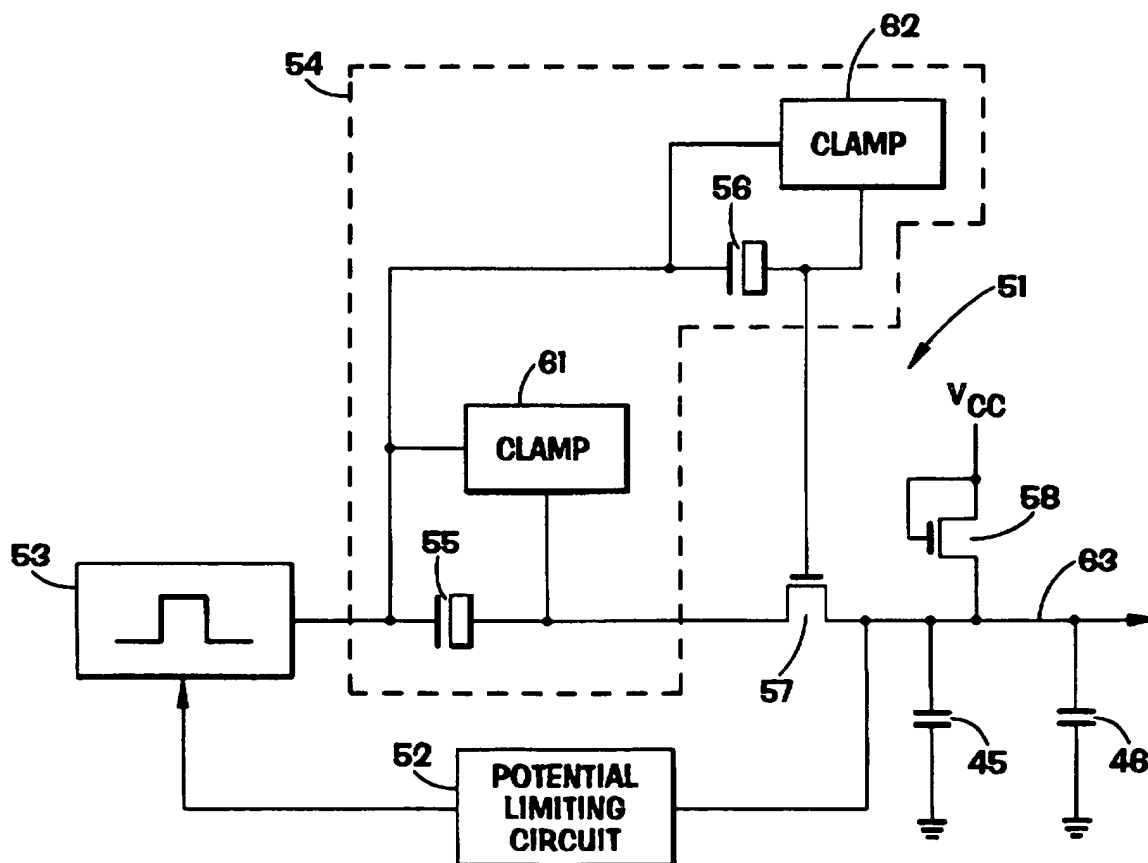
[56] **References Cited**

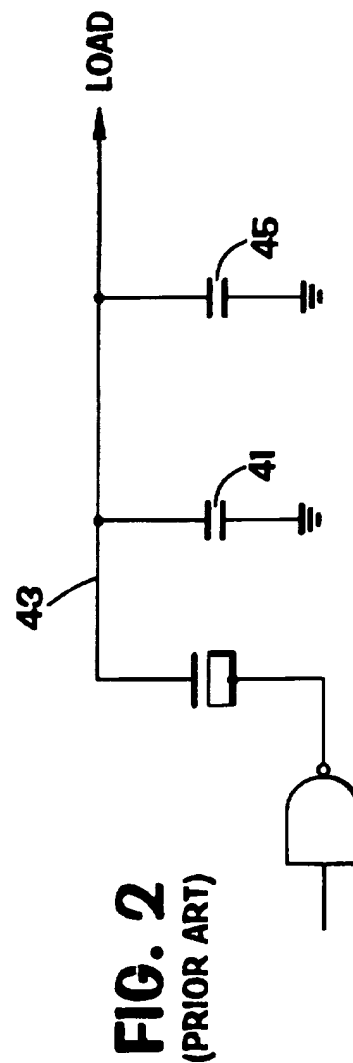
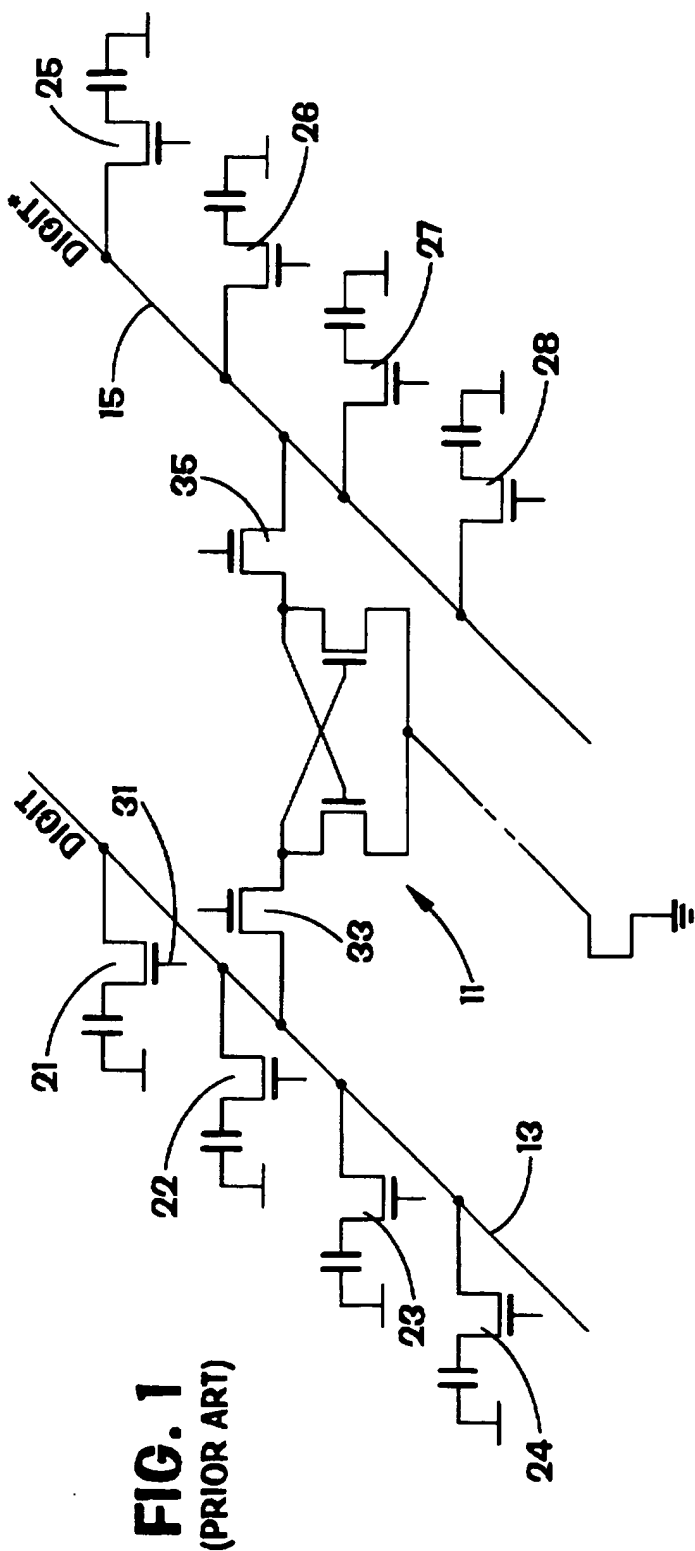
**U.S. PATENT DOCUMENTS**

4,105,950 8/1978 Dingwall ..... 331/57  
4,517,532 5/1985 Neidorff ..... 331/57  
4,631,421 12/1986 Inoue et al. .... 327/537  
5,023,465 6/1991 Douglas et al. .... 365/203

An integrated circuit semiconductor device includes a charge pump to provide current at a potential which is greater than a supply potential. The charge pump utilizes an oscillator, which causes the charge pump to cycle, and thereby provide a continuous output at an elevated potential. In order to optimize efficiency of the charge pump, the oscillator is able to change its frequency in response to output potential. In the preferred embodiments, this is accomplished by selectively inserting a supplemental portion into a ring oscillator loop. When used with an integrated circuit device, such as a DRAM, the current from the charge pump may be supplied to nodes on isolation devices and nodes on word lines, thereby improving the performance of the DRAM without substantially changing the circuit configuration of the DRAM array.

**13 Claims, 5 Drawing Sheets**





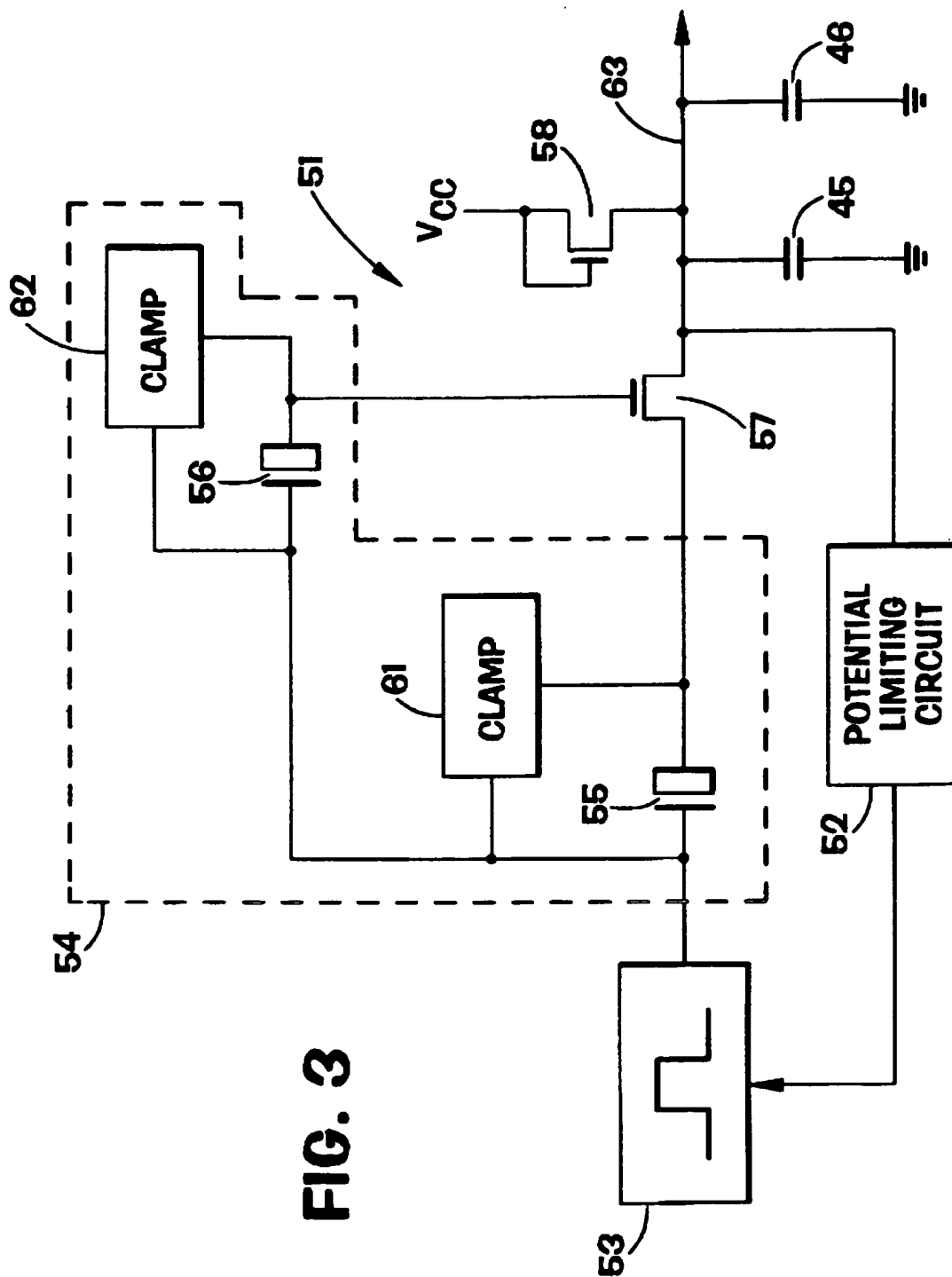
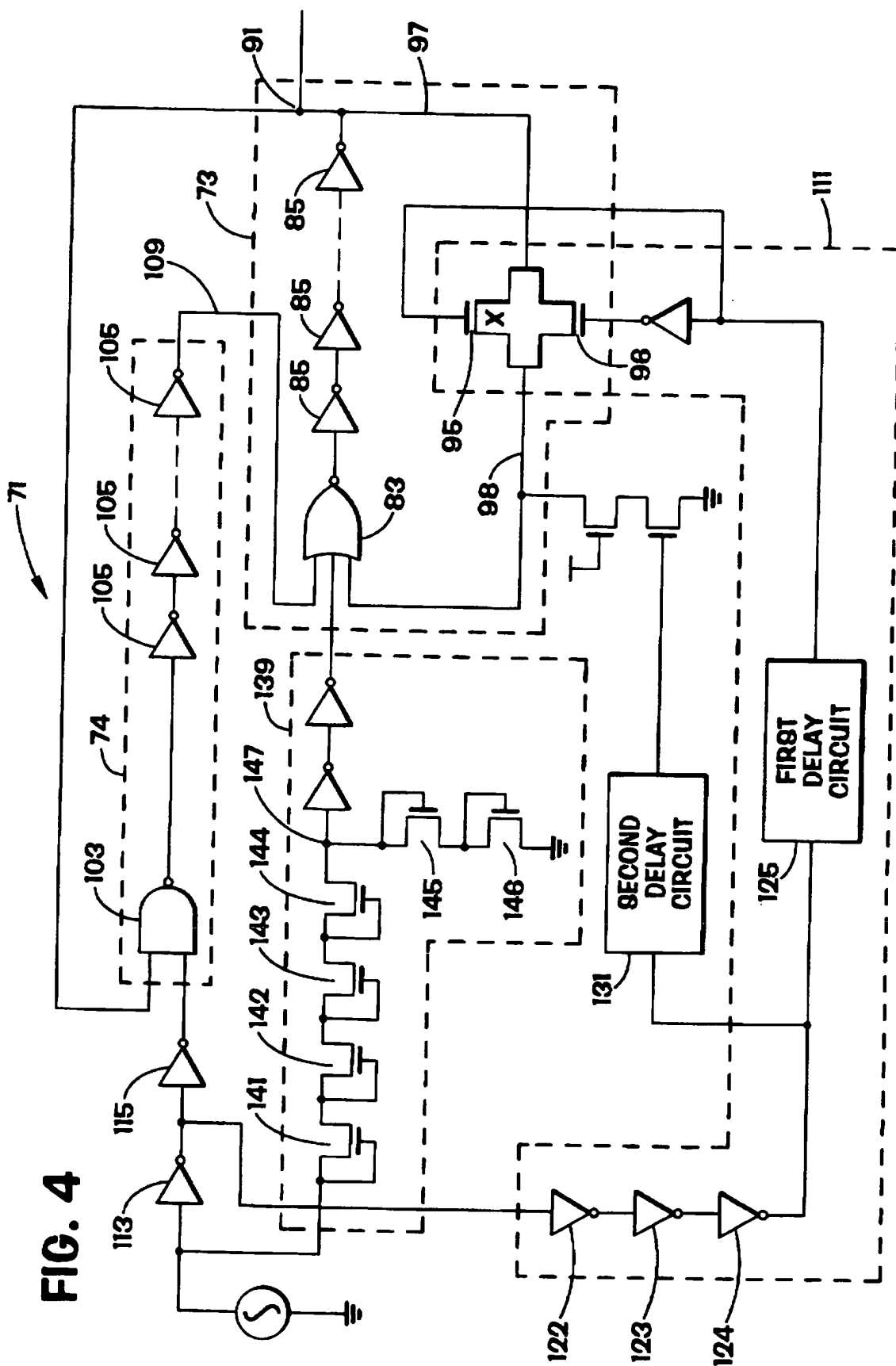


FIG. 3





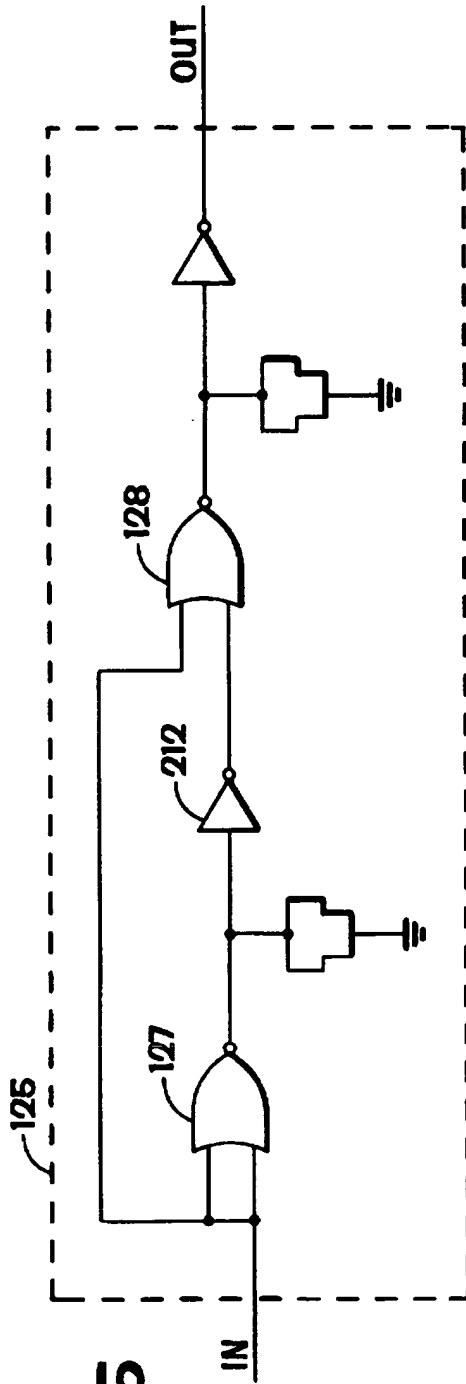


FIG. 5

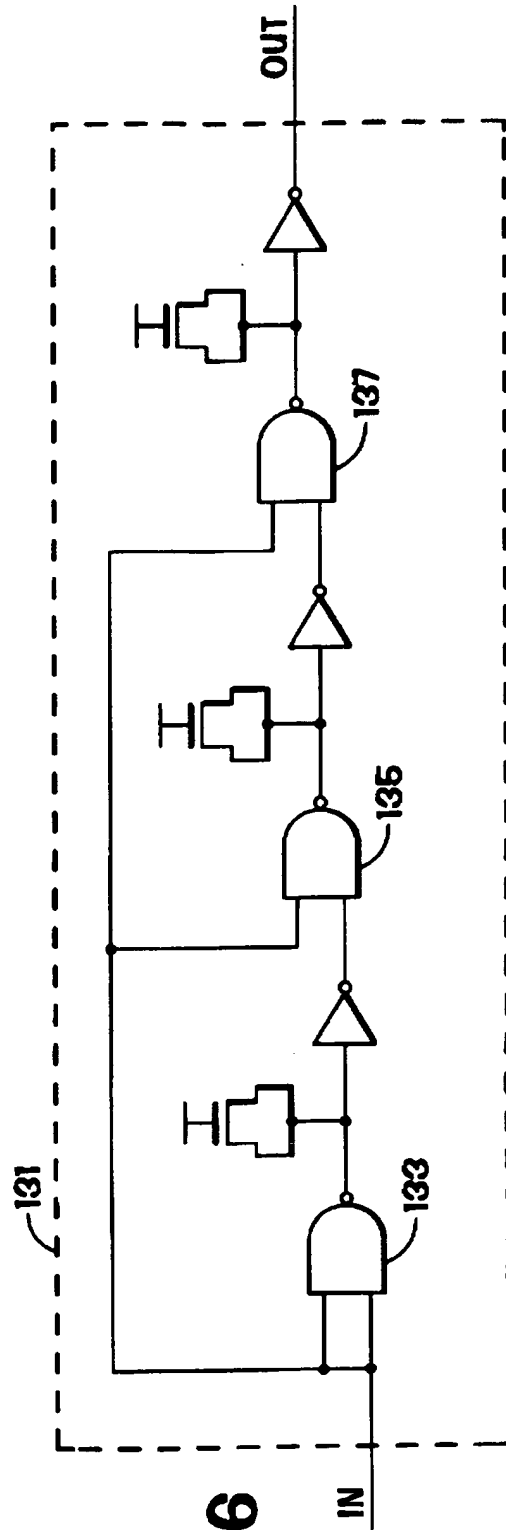


FIG. 6

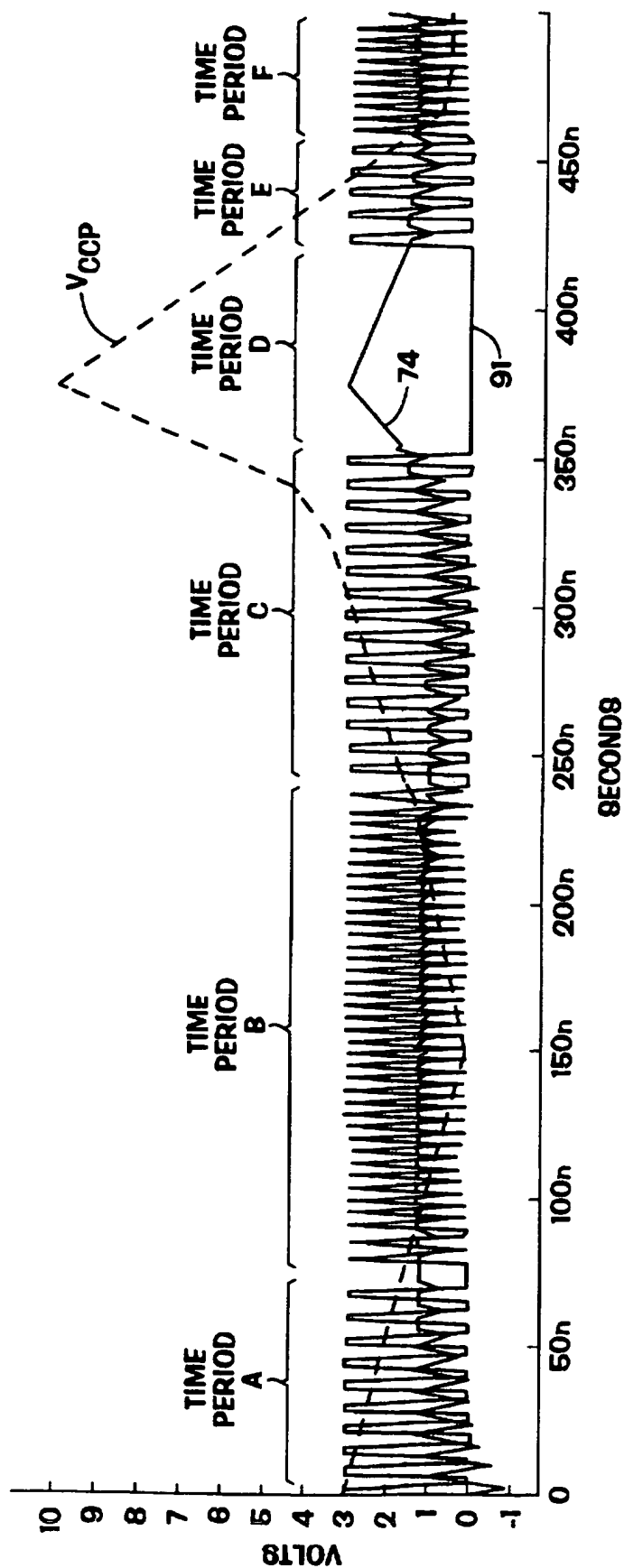


FIG. 7

# FREQUENCY-VARIABLE OSCILLATOR CONTROLLED HIGH EFFICIENCY CHARGE PUMP

## FIELD OF THE INVENTION

This invention relates to semiconductor integrated circuit devices and more particularly charge pump boost circuits. The invention is particularly applicable to dynamic random access memory devices ("DRAMs") in which the charge pump is used for providing current to voltage-sensing amplifiers ("sense amps") which are part of the integrated circuits.

## BACKGROUND OF THE INVENTION

Even though semiconductor integrated circuit devices, including the present invention, are comprised of various materials which are either conductive, insulating or semiconductive electrically, such circuit devices are usually simply referred to as "semiconductor devices." One of the semiconductive materials typically used is silicon, which is utilized in either single-crystal silicon form or in polycrystalline silicon form (i.e., as "polysilicon" or "poly").

In the operation of certain semiconductor devices, it is necessary to "draw up" a node of the sense amps to a potential above  $V_{CC}$  the basic operating voltage of the device. In the context of the present invention, these nodes to be drawn up occur on isolation ("iso") devices on an array of a memory device and on word lines for an array. Memory devices with word lines, which use such iso devices on an array, include DRAMs. A conventional arrangement of DRAM memory cells with a sense amp is shown in FIG. 1, which is discussed in greater detail hereinafter. Other types of memory devices, such as static RAMs and video RAMs also may have similar circuit arrangements. An iso device operates to isolate, electrically, circuitry for providing digits during a "digit load" from a sense amp so that during digit load the sense amp can amplify the digit load signal faster without having to first overcome the effects of a directly coupled load. More specifically, where the iso device comprises an n-channel transistor connected in series along a digit line, the iso device can be used to control the RC loading on the sense amp. By turning the iso device to the OFF state, the digit line is separated into two pans, each pan presenting a reduced RC load in comparison with the load of the whole digit line as is presented to the sense amp when the iso device transistor is in the ON state.

Generally, with respect to the design of iso devices, it is known that "gating" an iso device with a higher potential, i.e., increasing  $V_{GS}$  speeds (i.e., reduces) read time and reduces the required size of the iso device. Typically, in a DRAM, the iso device is used with either multiplexed or non-multiplexed sense amps. In the case of multiplexed sense amps, reducing the size of the iso device (by increasing  $V_{GS}$ ) allows the circuit layout to be configured with the iso-devices "on pitch" (two pitch) rather than in a four pitch pattern. This simplifies layout design because the two pitch layout provides a configuration in which, for each sense amp, both iso devices are individually aligned with that sense amp. With four pitch layout patterns, more than one sense amp must be balanced as a unit. The decrease in device width is obtained because increasing potential to gate gives the device a greater effective electrical transistor width as is necessary to keep discharge time short and response speed high.

In the prior art, bootstrapping had been used in order to charge nodes of a circuit (such as iso nodes) to an increased potential. A bootstrap circuit provides an increased voltage

level at a particular time in response to a particular sequence of events, such as the receipt of a series of timing signals. A charge pump circuit, on the other hand, provides a continuous output and an increased potential. The continuous high-potential output of a charge pump circuit essentially means that the charge pump's output is not especially dynamic and that the timing sensitivities of the output do not limit its utility in providing elevated voltage to circuit nodes. This is particularly important when a high-potential node is used (as is frequently the case) for the word line of a DRAM memory device, since the timing for selecting and addressing the word line is critical to the access speed of the DRAM. Because the bootstrap circuit provides the increased voltage in a timed manner, individual bootstrap circuits must be provided for each of several nodes, each of which requires current at elevated potentials at specific different times. The charge pump, with its continuous output, can be used for supplying current to any of these nodes without similar timing restrictions.

Also, unlike bootstrap circuits, charge pumps do not involve problems of proximate spacing. A bootstrap circuit is positioned by the portion of the device which obtains elevated potential from that bootstrap circuit, that individual bootstrap circuit being dedicated to a particular driven circuit. Because bootstrap circuits are dedicated to particular driven circuits and positioned thereby to facilitate the operation of the particular driven circuit, the amount of total effective circuit area of the driven circuits is necessarily increased. This increase could occur even where the driven circuits include relatively small individual transistors. Charge pumps can provide elevated potential to many nodes and need not be positioned proximately.

Prior art charge pumps consist of an oscillator and capacitor. The use of an oscillator and capacitor along with a single clamp circuit provides a relatively constant elevated potential, but is somewhat inefficient when compared to a bootstrap circuit.

With respect to additional design considerations, an ideal auxiliary circuit for performing a function such as voltage elevation should automatically respond to circuit conditions which make the auxiliary circuit unsuitable for its application. For example, a voltage boosting circuit would ideally attenuate its increased potential output or be bypassed as external system voltage becomes sufficiently high to make the use of the boosting circuit undesirable.

U.S. Pat Nos. 5,023,465 and 5,038,325 describe charge pumps in which a minimum potential is maintained by providing a bypass circuit at the charge pumps's outputs, which include an overvoltage shutdown circuit that functions to disable the charge pumps when output potential exceeds a predetermined level. In each case, the auxiliary circuits to the charge pumps do not change the functional performance of charge pump circuitry itself, while that circuitry is in operation.

An additional circuitry feature, which does affect a basic functional performance characteristic of a charge pump, relates to the oscillator frequency. Certain DRAM parts made by the assignee of the present invention, Micron Technology, Inc., for example, have been designed with a metal mask option which permits production changes in the oscillation frequency of the oscillator used to drive the DRAM charge pump. Such a design allows the charge pump to be set with respect to (1) the time required to achieve an elevated voltage, and (2) the elevated voltage attainable, by selecting the charge pump's drive frequency from among available frequencies. This feature only affects the initial

selection of the drive frequency on a one-time basis, however, usually prior to fabrication.

Accordingly, the known practices for using a charge pump circuit to provide elevated voltage have benefits over bootstrap circuits, but have disadvantages with respect to efficiency, and responsiveness to contingencies during operation and in multi-product design. The present invention addresses the aforementioned problem confronted using prior art charge pump circuits.

### SUMMARY OF THE INVENTION

In accordance with the present invention, an integrated circuit device includes a charge pump to provide current at a potential which is greater than a supply potential. The current is supplied to certain nodes on the integrated circuit device in order to enhance the performance of the integrated circuit device.

When used with an integrated circuit device, such as a DRAM, the current from the charge pump may be supplied to any of several nodes on isolation devices and nodes on word lines. This allows the nodes to be operated at an elevated potential, thereby improving the performance of the DRAM. This enhanced performance is achieved without substantially tailoring the design of the charge pump to match any particular isolation device or word line nodes, and while maintaining sufficient separation between the charge pump circuit and nodes of the DRAM to be driven, and flexibility in the charge pump design so that, in the event that the use of the charge pump proves to be inopportune, the charge pump can be bypassed by minor changes in the masks used to produce the integrated circuit device. This configuration allows the same basic mask layout to be used in different DRAMs designed to operate under different parameters.

Likewise, in accordance with the principles and teaching of this invention, and in keeping with one of its aspects, the charge pump is provided with an overvoltage shutoff circuit. The overvoltage shutoff circuit permits the charge pump to operate under conditions of low supply voltage when an elevated voltage is needed from the charge pump, but allows charge pump to be effectively bypassed when supply voltage is sufficiently high to make bypass desirable.

In accordance with a further aspect of the invention, the charge pump is designed to operate at a higher efficiency by the use of a pair of clamp circuits. An oscillator provides an output to a pair of capacitors. Each capacitor is bypassed respectively by one of the clamp circuits, and the clamp circuits are separately timed. The output of the first capacitor is also connected to an output transistor which is gated by the second clamp circuit connected in parallel to the second capacitor. The controlled gating of the output transistor permits the clamp circuit to maintain a continuous output at an elevated potential, while reducing power loss caused by impedances within the charge pump circuit.

By using the charge pump as a source of elevated potential, the circuit layout of the DRAM array is simplified and the potential boosting circuitry can be located outside of the array, on the periphery of the integrated circuit.

### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 shows a conventional configuration of sense amps in a DRAM array;

FIG. 2 schematically shows a configuration of a charge pump;

FIG. 3 is a schematic block diagram of a charge pump with overcharge protection, which can be constructed with

an oscillator circuit made in accordance with the teachings of the present invention;

FIG. 4 is a detailed schematic diagram showing the oscillator circuit for a charge pump according to the present invention;

FIGS. 5 and 6 are schematic diagrams showing the first and second delay circuits of FIG. 4 in greater detail; and

FIG. 7 is a timing diagram showing the relationship of node potential and oscillator frequency for the operation of a charge pump constructed in accordance with the principles of the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a sense amp 11 is connected between Digit and Digit\* lines 13 and 15 on a DRAM array. Digit and Digit\* lines 13 and 15 are connected to an array of memory cells, such as cells 21-28, which are also shown.

The memory cells 21-28 are connected to Digit and Digit\* lines 13 and 15 through word lines, such as word line 31, comprising the gate of the transistor associated with one of memory cells 21-28. Iso devices 33 and 35 are used to gate the current between the sense amp 11 and either of the Digit and Digit\* lines 13 and 15 in order to permit the sense amp 11, which is a differential amplifier, to sense the relative levels of the Digit and Digit\* lines 13 and 15. By selectively gating one of the memory cells 21-28 to either of Digit and Digit\* lines 13 and 15, it is possible to detect the memory storage level in the memory cell. The memory storage level of the selected memory cell on the connected line will be either higher or lower than the potential of the other and unconnected line. The bit represented by the level of the selected cell is a logical high (one) or low (zero), depending on whether it is higher or lower, respectively, than the level of the unconnected line.

In order to increase the sensitivity of the differential amp 11 and to permit the differential amp 11 to more rapidly respond to the differential potential between Digit and Digit\* lines 13 and 15, the iso devices 33 and 35 must have a relatively large effective transistor width. One way to accomplish effectively larger transistor width without actually increasing the physical size of iso devices 33 and 35 is to gate the iso devices 33 and 35 at a slightly elevated potential, i.e., to have  $V_{GS}$  greater than  $V_{CC}$ . Having  $V_{GS}$  greater than  $V_{CC}$  reduces resistance between gate and source, thereby increasing effective transistor width.

That is, preferably, the gating of iso devices 33 and 35 of the higher  $V_{GS}$  potential is by means of a signal line to iso devices 33 and 35. The inclusion of the signal line, which is part of an address circuit and makes the iso devices larger, involves further size considerations and requires a specific design trade off; as a rule, smaller iso devices advantageously increase sensing speed but cause a disadvantageous increase in the time required for Digit and Digit\* lines to fully discharge to ground. Bigger iso devices discharge more quickly, allowing Digit and Digit\* lines to be written to opposite states faster, but yield a decrease in sensing speed. However, the slow discharge problem associated with a smaller iso device of a given desired drive ability can be addressed by elevating  $V_{GS}$ . Thus, addressing the reduced-resistance and time-to-discharge issues by elevating  $V_{GS}$  results in a relatively smaller iso device which is easier to design into high density circuitry.

With respect to other features of the context in which the invention is applicable, FIG. 2 shows a schematic diagram of an auxiliary circuit for elevating potential at a circuit

node. The node 43 at which the auxiliary circuit is coupled to the node to be elevated has an inherent capacitance, indicated by capacitor 45, resulting primarily from the line capacitance of the load. The amount of inherent capacitance represented by capacitor 45 may be unpredictable until the circuit is constructed, but this capacitance is believed to stabilize the potential from the auxiliary circuit and, in effect, function as an integral part of the auxiliary circuit. The charge pump of the present invention provides a way to vary the frequency and, thus, variation in the inherent and useful capacitance of the charge pump is possible. However, an inherent capacitance exists and will be maintained for any frequency choice.

FIG. 3 shows a basic circuit for a charge pump into which the present invention can be incorporated. This circuit is described in the assignee's U.S. Pat. Nos. 5,023,465 and 5,038,325. This circuitry is used in a preferred embodiment of the invention which further includes the oscillator described in detail below with reference to FIG. 4.

The charge pump 51 includes an oscillator 53 that is powered by a signal level voltage source  $V_{CC}$ . The oscillator 53 provides its output to a pulse circuit 54. The pulse circuit 54 responds to the oscillator 53 in a manner which results in the pulse circuit 54 providing a potential output at an output node 63 at a boosted level  $V_{CCP}$  as compared to the signal level voltage source  $V_{CC}$  in response to an oscillating signal from the oscillator 53. The pulse circuit 54 includes three switching circuits illustrated as a first clamp circuit 61, a second clamp circuit 62, and a transistor 57. The clamp circuits 61, 62 are connected across capacitors 55, 56, respectively.

The charge pump 51 is designed to operate at a higher efficiency by the use of the pair of clamp circuits 61, 62. The oscillator 53 provides an output to the capacitors 55, 56. Each capacitor 55, 56 is bypassed respectively by one of the clamp circuits 61, 62, and the clamp circuits 61, 62 are separately timed. The output of the first capacitor 55 is also connected to the transistor 57, which is gated the second clamp circuit 62. The controlled gating of the transistor 57 permits the charge pump to maintain a continuous output at an elevated potential  $V_{CCP}$  with respect to the signal level voltage source  $V_{CC}$ , while reducing power loss caused by impedances within the charge pump circuit 51.

A decoupling capacitor 46 is coupled to the output node 63 to help maintain a steady boosted output. A potential limiting circuit 52 is coupled between the output node 63 and the oscillator 53 to prevent the potential at the output node 63 from exceeding a predetermined value. If the potential provided by the charge pump 51 at the output node 63 is inadequate, a diode-connected transistor 58 is used to bypass the charge pump 51.

In order to reduce operating current in the semiconductor device, it is desired to determine the minimum power and corresponding frequency required to provide a sufficient boosted potential output from the charge pump to the device. The minimum frequency is a function of the physical parameters of the component circuit elements, and may be variably and dynamically set by adjusting the frequency of oscillator 53. By so doing, it is possible to construct a charge pump which, if operated at a first frequency, provides a reduced output, and if operated at a second higher frequency, provides an increased output. The present invention provides a means to control the output of the charge pump in the aforementioned manner.

With respect to power requirements for a DRAM, it is known that different read and write cycles cause an increase

or decrease in power demand, and that the need for an increased charge pump output also can be caused by changes in supply potential  $V_{CC}$ . However, it is not necessary in making the charge pump responsive to determine dynamically the state of all power demand variables. It is sufficient for a dynamically responsive charge pump to determine a fixed number, for example, two load states to which the charge pump output ( $V_{CC \text{ req}}$ ) can be made to correspond. It is necessary to determine the maximum load at which a boosted output of the charge pump ( $V_{CC \text{ req}}$ ) must be provided; and it is advantageous to determine a steady state or quiescent operating mode, during which  $V_{CC \text{ req}}$  is provided to a reduced load. With the present invention, the output of charge pump 51 is adjusted to correspond to load states by adjusting the oscillator frequency of oscillator 53 used to drive the pulse circuit 54. This is preferably accomplished by selectively bypassing a portion of the ring oscillator circuitry of oscillator 53 in accordance with the output potential or output load of the charge pump 51.

FIG. 4 shows a configuration of the oscillator 53 in which a ring oscillator 71 includes a primary loop 73 and a secondary loop portion 74. As will be seen, the primary loop 73 functions alone during a fast mode of operation, and it functions in combination with the secondary loop portion 74, to form a larger loop, during a slow mode of operation.

Primary loop 73 consists of a NOR gate 83 and a first plurality of invertors 85. The circuit is effectively a delay line which transmits pulses to an output node 91. Pulse signals at the output node 91 are either transmitted through the secondary loop portion 74 and back to primary loop 73 through NOR gate 83 or through transistors 95 and 96 back to only primary loop 73 through NOR gate 83. In either case, the receipt of the pulse signal at NOR gate 83 results in the signal being transmitted through the first plurality of invertors 85, and therefore results in a repetitively pulsed output at the output node 91. The number of invertors comprising plurality 85 should be EVEN; the plurality may comprise, for example, 20 invertors. This pulsed output is used as an oscillator or pulse signal to drive the pulse circuit 54 of the charge pump 51 (see FIG. 2).

Transistors 95 and 96 form a part of a bypass circuit, which includes lines 97 and 98, for allowing transmission of pulses from the output node 91 to NOR gate 83, bypassing secondary loop portion 74.

Secondary loop portion 74 consists of a NAND gate 103 and a second plurality of invertors 105. Pulse signals at the output node are provided to the NAND gate 103, which in turn provides signals to the second plurality of invertors 105. The number of invertors comprising plurality 105 should be ODD; the plurality may comprise, for example, 17 invertors. The second plurality of invertors 105 provide an input, at node 109, to NOR gate 83. The secondary loop portion effectively delays the pulses at the output node 91 from being transmitted to NOR gate 83, thereby slowing the pulse repetition rate, and therefore, reducing the oscillation frequency at the output node 91.

When secondary loop portion 74 is not bypassed and operates to reduce the oscillation frequency at the output node 91, the bypass circuit through transistors 95 and 96 is shut off. This prevents signals being transmitted directly back to NOR gate 83 through transistors 95 and 96 at that time. That avoids the faster pulse repetition rate obtained by transmitting pulses through transistors 95 and 96.

For purposes of explanation, NAND gate 103 corresponds to the oscillation control according to the invention. However, the invention can be practiced without NAND

gate 103 by using other components. Indeed, any other components which may be used suitably to provide the function of NAND gate 103 in controlling secondary loop portion 74 according to the principles of the present invention are acceptable for use as the oscillation control apparatus.

Transistors 95 and 96 form a part of a bypass control circuit 111. The bypass circuit (which includes transistors 95 and 96, and lines 97 and 98 and also a series connection of invertors and a delay circuit, which are described below) is activated in response to a sensed potential which corresponds to a predetermined output potential of the charge pump 51. That is, when the potential at the output node 91 is of a certain level relative to the desired output  $V_{CCP}$  as described below, the activation of the bypass circuit will take place. As described above in connection with one embodiment, the activation of the bypass circuit increases the oscillation frequency of the ring oscillator 71 by removing secondary loop portion 74 from the operative oscillator loop.

When the output potential  $V_{CCP}$  of the charge pump 51 falls below a predetermined level, that indicates that the charge pump 51 must increase its output, and therefore, the ring oscillator 71 must provide an increased oscillation frequency. The increased oscillation frequency will increase the output of the charge pump 51, and consequentially increase  $V_{CCP}$ .

While the bypass circuit through transistors 95 and 96 is activated, NAND gate 103 transmits a continuous signal (at a 0 logic level), and therefore the secondary loop portion 74 is made quiescent. An input inverter 113 and a secondary trigger inverter 115 provide a signal to NAND gate 103, which allows NAND gate 103 to respond to signals from the output node 91. Input inverter 113 responds if charge pump output signal  $V_{CCP}$  supplied to the inverter 113 is at a predetermined level which is sufficient to trigger the inverter 113. If the potential to  $V_{CCP}$  to input inverter 113 is below the predetermined level (of  $V_{CCP}$ ), then NAND gate 103 receives a logical 0 and the secondary loop portion 74 is forced quiescent (the continuous 0 logic level). This is the desired result, since in the preferred embodiment, the primary loop 73 does not receive signals from the secondary loop portion 74 when providing the increased oscillation frequency. Bypass control circuit 111 receives the inverted signal and is responsive to the input inverter 113. The bypass control circuit 111 receives the inverted signal from input inverter 113, which is again inverted through invertors 122, 123 and 124. This signal is provided to a First Delay Circuit 125, which causes transistors 95 and 96 to conduct when the potential to input inverter 113 is below the predetermined level of  $V_{CCP}$ . As shown in FIG. 5, First Delay Circuit 125 includes NOR gates 127 and 128 and other components, which achieve the above-described control of transistors 95 and 96. First Delay Circuit 125 is configured so that the state of the input to NOR gate 127 will affect the delay of the output from the inverter connected to the output of NOR gate 128, as herein described. When the input to NOR gate 127 goes from HIGH to LOW, the inverter output will go from HIGH to LOW relatively slowly, following a path through all the components of circuit 125. When the input to NOR gate 127 goes from LOW to HIGH, the inverter output transitions from LOW to HIGH with less delay, following a path which bypasses NOR gate 127 and the inverter in series with it and going to NOR gate 128 directly and then to the inverter.

The bypass control circuit 111 causes transistors 95 and 96 to open the bypass circuit when the secondary loop

portion 74 is functioning. The bypass control circuit 111 prevents signals being transmitted directly back to NOR gate 83 through transistors 95, 96 at that time. That avoids the faster pulse repetition rate obtained by transmitting pulses through those transistors 95 and 96. A Second Delay Circuit 131 responds to the signal from inverter 124 to ground the outputs of transistors 95 and 96, thereby permitting NOR gate 83 to respond to signals at the output of secondary loop portion 74. This operation of the Second Delay Circuit 131 occurs when bypass control circuit 111 is holding transistors 95 and 96 open. FIG. 6 shows Second Delay Circuit 131 in greater detail. Second Delay Circuit 131 includes NAND gates 133, 135, and 137 and is configured so that the state of the input to NAND gate 133 will affect the delay of the output from the inverter connected to the output of NAND gate 137, as herein described. When the input to NAND gate 133 goes from LOW to HIGH, the inverter output will be delayed through all the devices of the delay circuit. When the input to NAND gate 133 goes from HIGH to LOW, the inverter output will be delayed only briefly, the signal following a path which bypasses NAND gates 133 and 135 and going to NAND gate 137 directly and then to the inverter. The delay realized with the above described delay circuits keep node 98 in a predictable state during transitions between frequencies.

An overvoltage circuit 139 uses diodes 141, 142, 143 and 144 to sense a rise in  $V_{CCP}$  above a predetermined limit. In that event, a continuous signal is provided to NOR gate 83, causing the primary loop 73 to go quiescent until  $V_{CCP}$  drops below the predetermined limit. In the absence of a voltage sufficient to bias diodes 141-144 (i.e., zero volts or anything below the predetermined amount corresponding to the combined bias voltage), diodes 145 and 146 will pull node 147 to ground keeping the oscillator ON. At or above the predetermined voltage, node 147 will rise causing the oscillator to go OFF.

It is anticipated that current from another bypass circuit (not shown) would maintain potential at the output of the charge pump 51 in order to prevent  $V_{CCP}$  from dropping to ground. One method of maintaining potential is a diode-connected transistor. The diode connected transistor is an n channel device connected to a supply voltage node  $V_{CCP}$ . The transistor will conduct power as long as  $V_{CCP} < (V_{CC} - V_T)$ . It is off whenever  $V_{CCP} > (V_{CC} - V_T)$ . This portion of the circuit also helps charge up  $V_{CCP}$  on power up.

#### Oscillator Frequency Output Illustrated

FIG. 7 shows a timing diagram of potential levels generated by the inventive oscillator circuit 71. This diagram represents a computer-generated depiction of the operation of an actual fabricated circuit. The line designated  $V_{CCP}$  shows the potential at the input to inverter 113, which is used to drive the oscillator 71. In actuality, the input potential  $V_{CCP}$  is in part controlled by the oscillator 71. Line 91 is the potential at the output node 91.

The left-most side of the diagram shown in FIG. 7 shows the operation of both the primary loop 73 and the secondary loop portion 74.  $V_{CCP}$  is at a range at which the ring oscillator 71 is required to operate at a moderate boost mode of operation using primary loop 73 and secondary loop portion 74. This is shown at time period A.

Time period B shows the operation of the circuit when  $V_{CCP}$  drops below a predetermined potential. This causes the oscillator 71 to operate in a supplemental boost mode of operation to increase the output of charge pump 51. The secondary loop portion 74 goes quiescent and primary loop

73 oscillates more rapidly as a result of feedback conduction through transistors 95 and 96. The rapid oscillation of the primary loop 73 continues until  $V_{CCP}$  increases to above the predetermined potential. The predetermined potential is the potential supplied to the inverter 113 which is sufficient to trigger the inverter 113.

Time period C shows the operation of the ring oscillator 71 when  $V_{CCP}$  has again reached the predetermined potential. As in the case of time period A, both primary loop 73 and secondary loop portion 74 are operating, and transistors 95 and 96 open the bypass circuit.

Time period D shows the operation of the overvoltage circuit 139, wherein a continuous signal is provided to NOR gate 83, causing the primary loop 73 to go quiescent until  $V_{CCP}$  drops below the predetermined limit. Secondary loop portion 74 is also bypassed. While  $V_{CCP}$  is shown rising to substantial levels, it is anticipated that this would not occur during normal operation.

Finally, time period E shows the moderate boost mode of operation, followed by the supplemental boost mode of operation during period F when the potential  $V_{CCP}$  drops. While the potential  $V_{CCP}$  is shown dropping to 0, it is anticipated that this would normally occur only when a memory part is shut down.

While the invention was developed for use with DRAM memories, it is anticipated that the invention would be useful in other circuits in which a boosted power supply is needed. It is also anticipated that the circuit may be adapted for use with other circuits in which a variable frequency is required.

I claim:

1. In a semiconductor circuit device having at least one signal line which is prechargeable to at least one operating level, a signal level voltage source for providing current at a signal level potential, a circuit connected to the signal line for accepting an elevated potential above a potential of the signal level voltage source, and a precharge circuit for precharging the signal line, the precharge circuit comprising:

- a) an oscillator for receiving current from the signal level voltage source and providing an oscillating output having an oscillation frequency;
- b) a capacitor connected between the oscillator and an intermediate output node;
- c) at least one switching circuit connected in parallel with the capacitor between the oscillator and the intermediate output node for providing a charge pump output in response to the oscillating output, the charge pump output being provided at said elevated potential, the oscillator being responsive to an operating condition of the semiconductor circuit device to change the oscillation frequency of the oscillator, thereby effecting a change in the charge pump output of the switching circuit.

2. The device of claim 1, wherein the oscillator comprises:

- a) a primary loop having a first plurality of inverters;
- b) a secondary loop portion having an additional second plurality of inverters; and
- c) a circuit, coupled to said primary loop and said secondary loop portion and responsive to the charge pump output, for selectively causing only said primary loop to respond to feedback signals from the primary loop when the charge pump output is below a predetermined level, and for selectively causing both said primary loop and secondary loop portion to respond to feedback signals from the primary loop when the charge pump output is above the predetermined level, thereby changing

ing the oscillation frequency output by the oscillator in response to the charge pump output.

3. The device of claim 2, wherein:

said oscillator operates at a first higher frequency when said primary loop is responsive to feedback signals from said primary loop only and otherwise operates at a second lower frequency when operating, and wherein said circuit further includes a bypass circuit for permitting signals corresponding to output signals from the primary loop only to be fed back to the primary loop when the charge pump output is below the predetermined level and for opening said bypass circuit to provide signals from said secondary loop portion to the primary loop when the charge pump output is above the predetermined level.

4. The semiconductor device as described in claim 1, further comprising:

- a) a second switching circuit including an output transistor having a source and drain connected in series with the capacitor between the intermediate output node and an output node; and
- b) a third switching circuit for controlling the second switching circuit by gating the output transistor.

5. The semiconductor device as described in claim 4, further comprising: a second capacitor connected in parallel with the third switching circuit.

6. The semiconductor device as described in claim 5, further comprising:

- a potential maintenance transistor connected to conduct from the signal level voltage source at times when potential at the output node falls below a predetermined potential with respect to the potential of the output node, and to present an open circuit when potential at the output node is greater than the potential of the signal level voltage source.

7. The semiconductor device as described in claim 5, further comprising:

- a potential maintenance transistor having a source and drain connected in series between the signal level voltage source and the output node, the potential maintenance transistor being connected with its gate to the signal level voltage source.

8. The semiconductor device as described in claim 4, further comprising:

- a) means to maintain the output node at a predetermined minimum potential by conducting current from the signal level voltage source; and
- b) a potential limiting circuit responsive to potential at the output node, for attenuating the output of the precharge circuit to limit the potential at the output node.

9. The semiconductor device as described in claim 4, further comprising:

- a decoupling capacitor connected to the output node for providing a storage capacity sufficient to maintain said elevated potential at a potential above the signal level potential during a substantial portion of an operating cycle of the semiconductor circuit device.

10. In a semiconductor circuit device having at least one signal line which is prechargeable to at least one operating level, a signal level voltage source for providing current at a signal level potential, a circuit connected to the signal line for accepting an elevated potential above a potential of the signal level voltage source, and a precharge circuit for precharging the signal line, the precharge circuit comprising:

- a) an oscillator for receiving current from the signal level voltage source and providing an oscillating output having an oscillation frequency;



## 11

- b) a first capacitor connected between the oscillator and an intermediate output node;
  - c) a first switching circuit connected in parallel with the capacitor between the oscillator and the intermediate output node for providing a charge pump output in response to the oscillating output, the charge pump output being provided at said elevated potential, the oscillator being responsive to an operating condition of the semiconductor circuit device to change said oscillation frequency of the oscillator, thereby, effecting a change in the charge pump output of the switching circuit;
  - d) a second switching circuit including an output transistor having a source and drain connected in series between the intermediate output node and an output node;
  - e) a third switching circuit for controlling the second switching circuit by gating the output transistor;
  - f) a second capacitor connected in parallel with the third switching circuit;
  - g) means to maintain the output node at a predetermined minimum potential by conducting current from the signal level voltage source; and
  - h) a potential limiting circuit responsive to potential at the output node for attenuating the output of the precharge circuit to limit the potential at the output node.
11. In a semiconductor circuit device having at least one signal line prechargeable to operating levels, a signal level voltage source providing current at a signal level potential, a circuit connected to the signal line which accepts an elevated potential above a potential of the signal level

## 12

voltage source, and a precharge circuit which precharges the signal line, the precharge circuit comprising:

- a) an oscillator for receiving current from the signal level voltage source and for providing an oscillating output having an oscillation frequency, the oscillation frequency being variable in response to the voltage level of an input signal to the precharge circuit;
- b) a capacitor connected between the oscillator and a first node;
- c) an output switching circuit connected in series with said capacitor, between said capacitor and an output node; and
- d) a first clamp circuit connected in parallel with said capacitor and providing a timed output in response to the oscillating output.

12. The semiconductor device as described in claim 11, wherein:

the output switching circuit includes an output transistor having a source and drain connected in series between the first node and the output node and wherein the device further comprises a second clamp circuit for controlling the output switching circuit in a timed sequence with respect to said timed output, the second clamp circuit controlling the output switching circuit by gating the output transistor.

13. The semiconductor device as described in claim 12, further comprising:

- a second capacitor connected in parallel with the second clamp circuit.

\* \* \* \* \*



**Gonzalez**

**[45] Date of Patent: Dec. 16, 1997**

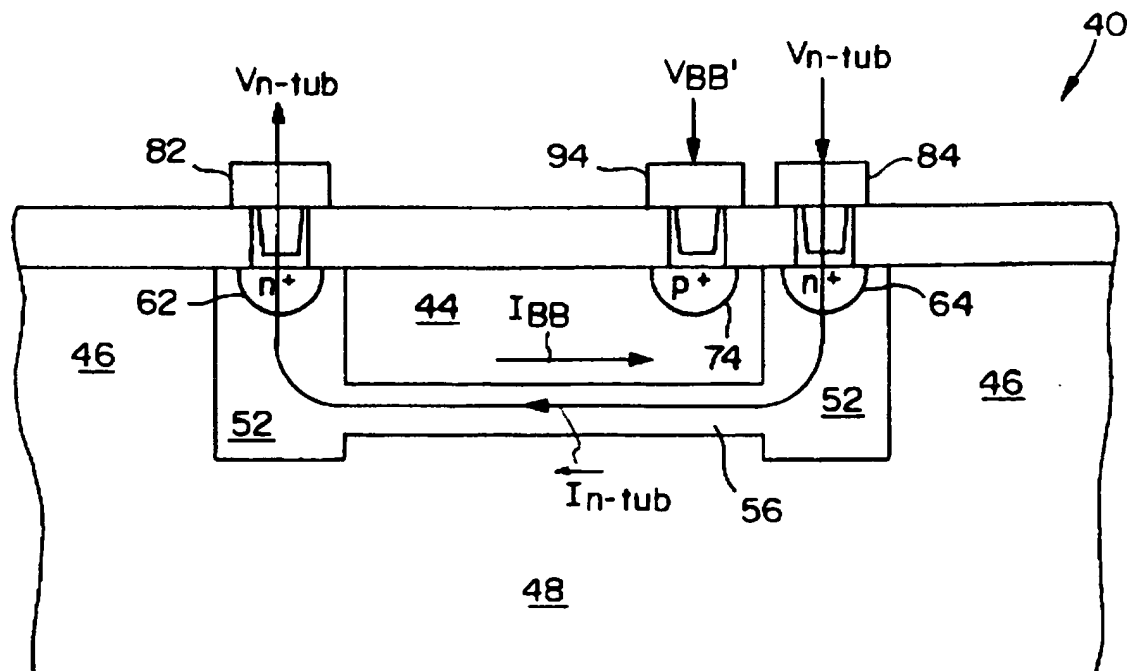


FIG. 1  
PRIOR ART

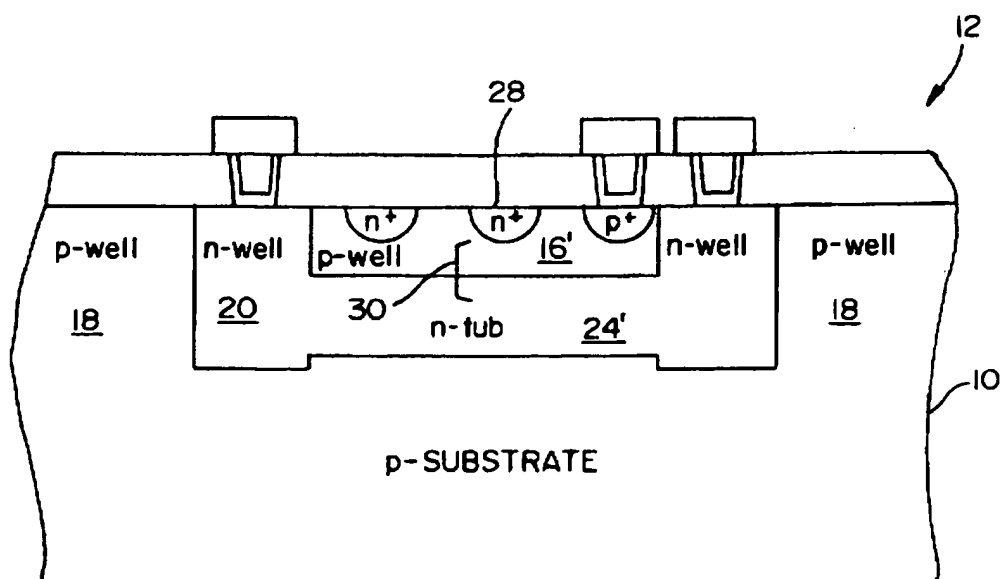
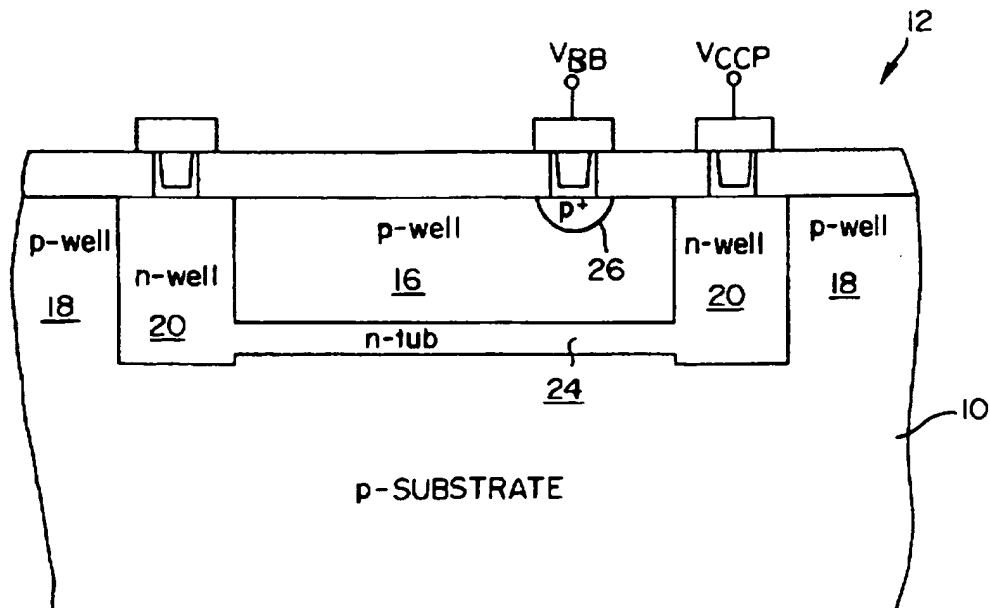


FIG. 2  
PRIOR ART

FIG. 3

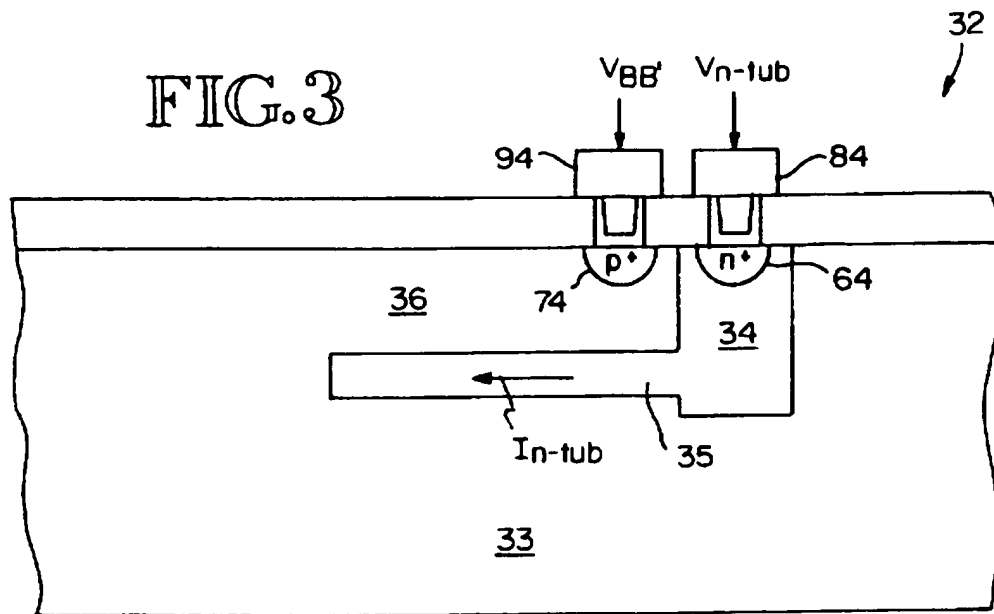
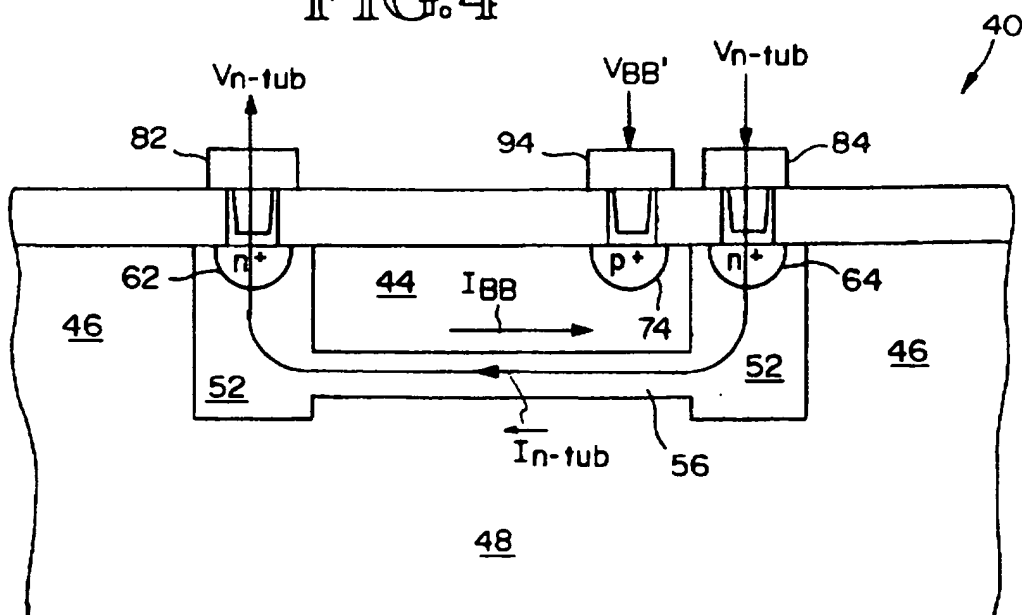


FIG. 4



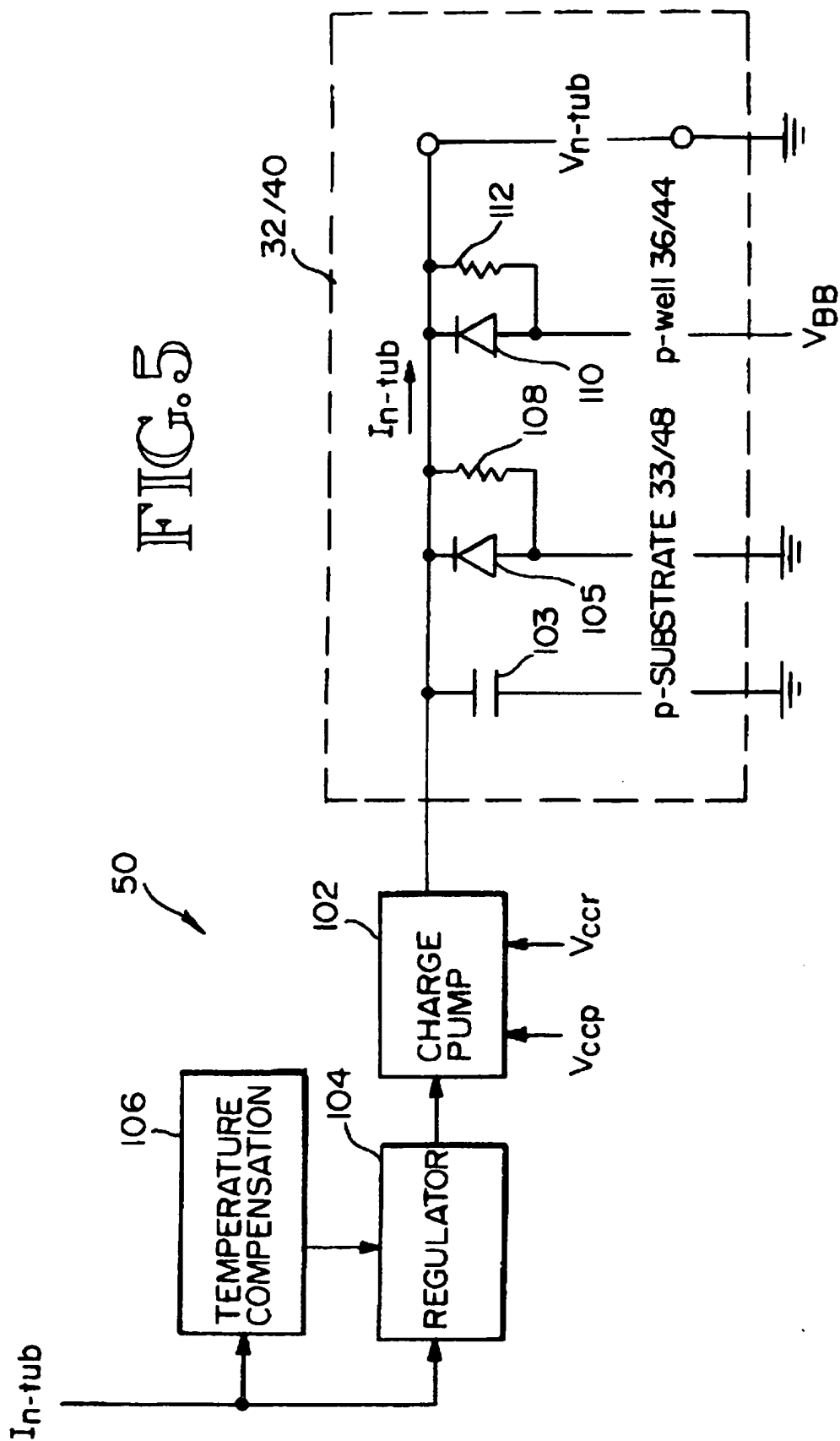


FIG. 6

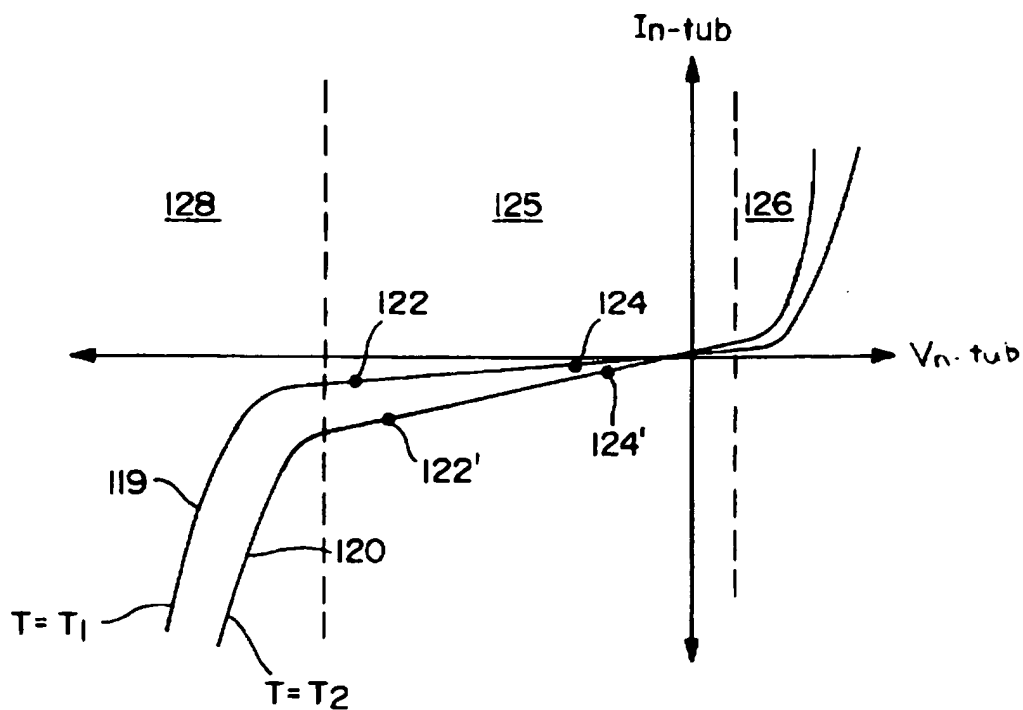
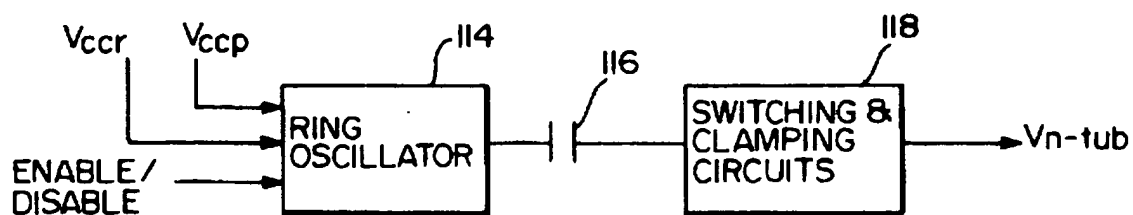


FIG. 7

## CHARGE-PUMPING TO INCREASE ELECTRON COLLECTION EFFICIENCY

### BACKGROUND OF THE INVENTION

This invention relates to methods and apparatus for biasing a semiconductor region, and more particularly to a method and apparatus for improving electron collection efficiency at a semiconductor region to reduce junction leakage.

Integrated circuits (IC) commonly are fabricated on a semiconductor wafer. The wafer typically is cut to form multiple semiconductor substrates or "IC chips". Semiconductor devices are formed on the wafer. Although the label semiconductor is used, the devices are fabricated from various materials, including electrical conductors (e.g., aluminum, tungsten), electrical semiconductors (e.g., silicon) and electrical non-conductors (e.g., silicon dioxide). The semiconductive silicon wafer is subjected to deposition, etching, planarizing and lithographic processes to achieve the many semiconductor devices.

In fabricating semiconductor devices, substrates typically are doped to form various n-type and p-type regions. One layout structure is a well. FIG. 1 shows a p-type substrate 10 having a triple well. A center p-well 16 is surrounded by an n-well 20, which in turn is surrounded by another p-well 18. An n-tub 24 conjoins the n-well 20 and is formed below the p-well 16. The center p-well 16 is separated from the p-substrate 10 by the n-tub 24. Typically one or more other doped regions 26 are included in the center p-well 16 to form an array of devices.

During normal operation the n-tub 24 is biased to improve performance of a device array in the p-well 16. Specifically, the biasing voltage sets up an energy potential well in the n-tub 24 which collects electrons. As electrons fall into the energy potential well they go into a lower energy state. Such electron collection reduces leakage of electrons across the junction into the p-well 16. For an array of DRAM cells, for example, the electron collection allows for a longer refresh period. Accordingly it is desired that electron collection at the n-tub 24 be efficient.

The wider and deeper the energy potential well created, the more electrons that are collected. The factors determining the energy potential well performance include the biasing voltage and the doping level of the n-tub. Conventionally the biasing voltage is limited to the supply voltage level. The doping level typically is limited to keep the n-tub from spreading too close to the surface.

When forming the p-well 16 and n-tub 24, the p-substrate 10 typically is doped in an area which is to become the n-tub. The n-tub, thus, defines a separation between pre-existing p-type regions. The doping process is an implantation of atoms. Implantation power defines how deep into the substrate the atoms are injected. Dosage level defines the number of atoms being injected, which affects the width of the n-tub junction for a given diffusion time. Typically the implantation power is limited, (e.g., 3 MeV maximum power), and correspondingly a maximum depth is defined. To maximize electron collection efficiency it would seem that very high doping levels would be desired. However, because the doping level affects the width of the n-tub junction, excessive doping would expand the n-tub junction too close to the surface. More particularly, the n-tub junction would expand too close to other n-type regions formed or to be formed in the center p-well. FIG. 2 shows such an example. Beyond a given n-tub 24' thickness, an adjacent p-well 16' separation gets too small. Specifically, the p-well

16' separating the n-tub 24' from a nearby n-type region 28 in the p-well 16' becomes less than a minimum spacing required for region isolation. For a separation in the p-well 16' region between n-tub 24' and n-type area 28 which is less than the threshold separation, the local area defines an undesired "parasitic" leakage path, (in effect, an undesired npn device 30). Typically, to avoid such a leakage path, the dosage for the n-tub is scaled back during the design process to keep the n-tub thickness to an acceptable level. A disadvantage of scaling the dosage back, however, is that the n-tub is comparatively less effective in collecting electrons.

Accordingly, there is need for improving collection of electrons at an n-tub.

### SUMMARY OF THE INVENTION

According to the invention, an n-tub is charge pumped via an n-well to increase electron collection efficiency at the n-tub. This increases the bias of the n-tub beyond conventional levels. Specifically, whereas prior methods limit the bias voltage to be up to the supply voltage magnitude,  $V_{cc}$ , charge pumping enables boosted bias voltages at the n-tub which are as high as  $2V_{cc}$ . The increased biasing of the n-tub creates an energy potential well of increased width and depth. Thus, more electrons are able to fall into the well and move to a lower energy level. This results in improved effectiveness of the n-tub. With the n-tub being more effective, less electrons are able to cross a junction into the adjacent p-well. Thus, junction leakage current is reduced. This improves performance of devices residing in the p-well.

According to one aspect of the invention, a charge pumping circuit applies the biasing voltage,  $V_{n-tub}$ , at an n-well. The n-well is conjoined to the n-tub and located adjacent to the p-well of interest.

According to another aspect of the invention, the resulting current in the n-tub,  $I_{n-tub}$ , is monitored to determine when to pump charge into the n-tub. The pumping biases the n-tub to voltages as high as twice the supply voltage magnitude, ( $2V_{cc}$ ).

According to another aspect of the invention, the n-tub current  $I_{n-tub}$  is compared to a minimum current threshold and a maximum current threshold. The charge pump is disabled when the current  $I_{n-tub}$  exceeds the maximum threshold and is turned on before the current  $I_{n-tub}$  goes below the minimum threshold. The maximum threshold is for keeping the n-tub from exhibiting an undesirable standby current. The minimum threshold is to keep the n-tub biased enough to achieve a desired electron collection efficiency.

In a preferred embodiment, a host integrated circuit includes adjacent first and second well structures, a tub structure, a charge pump circuit and a regulator circuit. The first well structure and the substrate are of a first doping type. The second well and tub structure are of a second doping type, and are conjoined. The first doping type is either one of p-type or n-type and the second doping type is the other one of p-type or n-type. The first well structure is separated from the substrate by the tub structure. A biasing voltage, (e.g.,  $V_{n-tub}$ ), is applied to the tub structure via the second well creating an tub current, (e.g.,  $I_{n-tub}$ ).

The charge pump circuit has an enable state and a disable state. During the enable state the charge pump circuit pumps charge into the tub structure to bias the tub structure to a bias voltage magnitude exceeding substrate supply voltage magnitude (i.e.,  $V_{n-tub} > V_{cc}$ ). The regulator circuit monitors the n-tub current to test the n-tub current relative to a minimum current threshold and a maximum current threshold. The

charge pump circuit responds to the regulator circuit to switch into the disable state when n-tub current magnitude rises to the maximum current threshold. The charge pump circuit switches from the disable state to the enable state when n-tub current magnitude falls to the minimum current threshold. The regulator circuit prevents the charge pump circuit from forward biasing the tub structure.

One advantage of the invention is that any decrease in electron collection effectiveness caused by compromising dosage of the n-tub is made up for by charge pumping the n-tub to accept more electrons. Thus, the charge-pumped structure exhibits improved n-tub electron collection effectiveness. These and other aspects and advantages of the invention will be better understood by reference to the following detailed description taken in conjunction with the accompanying drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a conventional semiconductor triple well;

FIG. 2 is a cross-sectional view of a defective semiconductor triple well;

FIG. 3 is a cross-sectional view of an integrated circuit having an n-tub charge pumped according to an embodiment of this invention;

FIG. 4 is a cross-sectional view of a triple well having an n-tub charge pumped according to an embodiment of this invention;

FIG. 5 is an electrical block diagram and partial schematic of the circuits of FIG. 3 or FIG. 4 according to an embodiment of this invention;

FIG. 6 is a block diagram of the charge pump of FIG. 5; and

FIG. 7 is a chart of current versus voltage characteristic curves for the n-tub of FIGS. 3 and 4.

### DESCRIPTION OF SPECIFIC EMBODIMENTS

#### Overview

FIG. 3 shows a portion of a semiconductor integrated circuit 32 at an intermediate step in its fabrication process. A p-type substrate 33 has an n-well 34 and an n-tub 35 formed so as to define a p-well 36. The n-tub 35 is charge-pumped during operation. Specifically, a hiss voltage is applied at a contact 84 resulting in a hiss voltage signal at n-well 34 and n-tub 35. The charge pumping creates a hiss voltage at the n-tub 35 which is as high as twice supply voltage magnitude ( $V_{cc}$ ). This increased biasing increases the energy potential well of the n-tub and counters any inherent inefficiency characteristic attributable to the n-tub doping level. The result is effective electron collection at the n-tub. Typically an array of devices are formed in the p-well 36 and/or n-well

#### Triple Well Embodiment

FIG. 4 shows a triple well 40 embodiment of this invention. The triple well structure is a device layout on a semiconductor substrate. For convenience and clarity the structure is illustrated and described for two p-wells on a p-substrate separated by an n-well. An n-tub isolates a central p-well from the p-substrate. Alternative embodiments, however, include two n-wells on an n-type substrate separated by a p-well. A p-tub isolates the central n-tub from the n-substrate.

The triple well structure is implemented in various embodiments for many alternative devices. Exemplary

devices include SRAMs, DRAMs, flash memory cells, processor components, logic devices and other devices for CMOS, MOS and other semiconductor technologies. Typically an array of devices is formed in the center well.

The triple well 40 is formed by a center p-well 44 and an outer p-well 46 separated by an intermediary n-well 52. The wells are formed on a p-type substrate 48. The central p-well 44 is isolated from the substrate 48 by an n-tub 56. The n-tub 56 extends from beneath the center p-well 44 to the concentric surrounding n-well 52. Also illustrated are more densely doped regions 62, 64, 74 adjacent to electrical contacts 82, 84, 94. The n-doped region 62 of n-well 52 is adjacent to contact 82. The n-doped region 64 of n-well 52 is adjacent to contact 84. The p-doped region 74 of p-well 44 is adjacent to contact 94. Although not illustrated, in specific embodiments any one or more of the p-wells 44-46 further includes one or more doped regions of the same or opposite polarity. Similarly, in specific embodiments the n-well 52 further includes one or more doped regions of the same or opposite polarity. These additionally doped regions define an array of devices.

According to conventional operation, the n-well 52 receives a supply voltage  $V_{cc}$  as a biasing voltage. (see comparative structures in FIG. 1). According to the invention, however, the n-well 52 is coupled to a charge pump which creates a bias voltage  $V_{n-wb}$  as high as  $2V_{cc}$ .

#### Charge Pumping Schematic

FIG. 5 shows the electrical schematic of the substrate 33/48 with related circuitry 50 according to an embodiment of this invention. The substrate 33/48 is represented schematically as (i) a capacitor 103 defined by the junction between the n-tub 35/56 and p-substrate 33/48, (ii) a diode 105 and resistor 108 defined by the junction leakage between the n-tub 35/56 and p-substrate 33/48, and (iii) a diode 110 and resistor 112 defined by the junction leakage between the n-tub 35 and the p-well 36/44. The related circuitry 50 includes a charge pump 102, regulator circuit 104, and a temperature compensation circuit 106.

The charge pump 102 injects electrons into the n-tub 35/56 via the n-well 34/54. Referring to FIG. 6, in one embodiment the charge pump 102 includes a ring oscillator 114, a capacitor 116 (e.g., MOS capacitor or polysilicon to polysilicon capacitor) and switching and clamping circuits 118. The ring oscillator 114 receives the voltage  $V_{cc}$  and an enable/disable signal. When enabled, the ring oscillator 114 generates pulses for charging the capacitor 116. The capacitor 116 outputs a signal which in effect stretches the pulses. The switching and clamping circuits 118 then serve to shape the resulting signal to approximate a dc signal. The result is a signal with voltage,  $V_{n-wb}$ , and a current,  $I_{n-wb}$ .

Referring again to FIG. 5, the regulator circuit 104 determines when the charge pump is enabled or disabled. When the n-tub current,  $I_{n-wb}$ , dwindles to a minimum threshold the regulator circuit 104 activates the charge pump 102. When the n-tub current reaches a maximum threshold the regulator circuit 104 disables the charge pump 102.

In one embodiment the temperature compensation circuit 106 defines the minimum and maximum thresholds as a function of substrate temperature. In other embodiments only the minimum thresholds is varied as a function of substrate temperature. The compensation circuit 106 is formed by known semiconductor-resident circuit structures. The charge pump 102, regulator circuit 104 and temperature compensation circuit 106, like the triple well 40 are integral to the host semiconductor.



## Charge Pumping Method

The purpose of charge pumping the n-tub 35/56 is to bias the region to collect more electrons. In pumping to high bias voltages (e.g., greater than  $V_{cc}$ ) it is desirable to avoid adversely impacting the center p-well 36/44. In one embodiment the outer p-well 46 is grounded, while a voltage  $V_{BB}$  is applied to center p-well 36/44 and a bias voltage  $V_{n-sub}$  is applied to the n-well 34/52 (embodiment illustrated). In an alternative embodiment the outer p-well 42 receives a voltage  $V_{BB}$ , while the center p-well 44 is grounded and a bias voltage  $V_{n-sub}$  is applied to the n-well 52. One does not want a high bias voltage  $V_{n-sub}$  (e.g.,  $V_{n-sub} > V_{cc}$ ) to cause adverse impact to the current in the center p-well 36/44. Accordingly, the n-tub current,  $I_{n-sub}$ , is monitored and compared to threshold currents to determine whether to enable or disable the charge pump 102.

The n-tub current,  $I_{n-sub}$ , is input to the regulator circuit 104. If the current  $I_{n-sub}$  reaches a maximum current threshold, the regulator circuit 104 disables the charge pump 102 to avoid an Undesirable standby current in the center well 36/44. As the current magnitude falls in response to a falling bias at the n-tub 35/52, the current  $I_{n-sub}$  approaches a minimum current threshold. Once the minimum current threshold is reached the regulator circuit 104 enables the charge pump. The minimum current threshold is selected as a level corresponding to a minimum tolerated electron collection efficiency at the n-tub 35/56.

The minimum current threshold varies with the temperature of the circuitry. Accordingly, in some embodiments the temperature compensation circuit 106 is included for varying the minimum threshold as a function of temperature.

FIG. 7 shows current voltage characteristic curves 119, 120 for biasing the n-tub. Note that the minimum current threshold 122 and the maximum current threshold 124 occur in the relatively flat region 125. One does not want to bias the n-tub into the forward biased region 126. Forward bias would result in undesirable standby current. One also does not want to bias the n-tub 35/56 into the avalanche breakdown region 128. Reverse bias into region 128 would undesirably compromise electron collection efficiency of the n-tub 35/56. Also note that there are different characteristic curves 119, 120 for differing operating temperatures. However, one still may desire to maintain a fixed maximum threshold. In other embodiments only the minimum current threshold or both the minimum and maximum current thresholds are varied.

## Meritorious and Advantageous Effects

One advantageous effect of the invention is that any compromise in electron collection effectiveness caused by reduced doping of the n-tub 35/56 is made up for by charge pumping the n-tub to accept more electrons. A meritorious effect is that circuits embodied in the center well 36/44 have improved operating efficiency.

Although a preferred embodiment of the invention has been illustrated and described, various alternatives, modifications and equivalents may be used. For example, although the triple well structures described and illustrated are p-type wells on p-type substrates, n-type wells on n-type substrates are used in alternative embodiments. Therefore, the foregoing description should not be taken as limiting the scope of the inventions which are defined by the appended claims.

What is claimed is:

1. A method for biasing a tub region of an integrated circuit, the integrated circuit comprising a substrate in which are formed a first well a second well and the tub region, the

first well having a first contact and being of a first doping the second well having a second contact, being adjacent to the first well and being of a second doping type, the first doping type being either one of p-type or n-type and the second doping type being the other one of p-type or n-type, the tub region underlying the first well and being conjoined to the second well the method comprising the steps of:

applying a first signal to the first well; pumping charge into the tub structure via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude.

in which the step of pumping is performed by a charge pump circuit integral to the substrate, the charge pump circuit having an enable state and a disable state, the charge pump circuit performing pumping when in the enable state, the charge pump circuit not performing pumping when the charge pump circuit is in the disable, and in which said pumping of charge into the tub structure is discontinued during the disable state.

2. A method for biasing a tub region of an integrated circuit the integrated circuit comprising a substrate in which are formed a first well a second well and the tub region the first well having a first contact and being of a first do in the second well having a second contact being adjacent to the first well and being of a second doping type, the the first doping type being either one of p-type or n-type and the second doping type being the other one of p-type or n-type the tub region underlying the first well and being joined to the second well, the method comprising the steps of:

applying a first signal to the first well;

pumping charge into the tub structure via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude, in which the step of pumping is performed by a charge pump circuit integral to the substrate the charge pump circuit having an enable state and a disable state, the charge pump circuit performing pumping when in the enable state, the charge pump circuit not performing pumping when the charge pump circuit is in the disable state;

testing the first current relative to a maximum current threshold; and

switching the charge pump circuit into a disable state when first current magnitude rises to the maximum current threshold.

3. A method for biasing a tub region of an integrated circuit the integrated circuit comprising a substrate in which are formed a first well a second well and the tub region the first well having a first contact and being of a first doping type the second well having a second contact, being adjacent to the first well and being of a second doping type the first doping type being either one of p-type or n-type and the second doping type being the other one of p-type or n-type, the tub region underlying the first well and being conjoined to the second well the method comprising the steps of:

applying a first signal to the first well;

pumping charge into the tub structure via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude, in which the step of pumping is performed by a charge pump circuit integral to the substrate, the charge pump circuit having an enable state and a disable state the charge pump circuit performing pumping when in the enable state, the charge pump circuit not performing pumping when the charge pump circuit is in the disable state;

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testing the first current relative to a minimum current threshold; and

switching the charge pump circuit from the disable state to the enable state when first current magnitude falls to the minimum current threshold.

4. A method for biasing a tub structure of an integrated circuit, the integrated circuit comprising a substrate in which are formed a first well, a second well and the tub structure, the first well having a first contact and being of a first doping type, the second well having a second contact, being adjacent to the first well and being of a second doping type, the first doping type being either one of p-type or n-type and the second doping type being the other one of p-type or n-type, the tub structure underlying the first well and being conjoined to the second well, the method comprising the steps of:

applying a bias signal to the second well, the bias signal causing a first current at the tub structure;

testing the first current relative to a minimum current threshold and a maximum current threshold; and

controlling a charge pump circuit having an enable state and a disable state, the step of controlling comprising switching the charge pump circuit into a disable state when first current magnitude rises to the maximum current threshold and switching the charge pump circuit from the disable state to the enable state when first current magnitude falls to the minimum current threshold; and

wherein the step of applying a bias signal comprises pumping charge into the tub structure, when the charge pump circuit is in the enable state, to bias the tub structure to a bias voltage magnitude exceeding the supply voltage magnitude.

5. The method of claim 4, in which the step of controlling further comprises preventing forward biasing of the tub structure.

6. A semiconductor substrate comprising:

a first well of the first doping type;

a second well of a second doping type, the first doping type being either one of p-type or n-type and the second doping type being the other one of p-type or n-type;

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a tub structure of the second doing type conjoining the second well and underlying the first well;

a charge pump circuit which pumps charge into the tub structure via the second well to define a first current which biases the tub structure to a bias voltage magnitude exceeding substrate supply voltage magnitude; and

a regulator circuit monitoring the first current to test the first current relative to a minimum current threshold and a maximum current threshold; and

wherein the charge pump circuit has an enable state and a disable state, the charge pump circuit responding to the regulator circuit to switch into the disable state when first current magnitude rises to the maximum current threshold, the charge pump circuit switching from the disable state to the enable state when first current magnitude falls to the minimum current threshold, the charge pump circuit, when in the enable state, pumping the charge into the tub structure to bias the tub structure to a bias voltage magnitude exceeding the supply voltage magnitude.

7. The method of claim 1, in which the step of pumping charge comprises pumping charge as a second signal into the tub region via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude, wherein the second signal is not input to the first well.

8. The method of claim 2, in which the step of pumping charge comprises pumping charge as a second signal into the tub region via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude, wherein the second signal is not input to the first well.

9. The method of claim 3, in which the step of pumping charge comprises pumping charge as a second signal into the tub region via the second contact and the second well to bias the tub region to a bias voltage magnitude exceeding supply voltage magnitude, wherein the second signal is not input to the first well.

\* \* \* \* \*



US005757170A

**United States Patent** [19]  
**Pinney**

[11] **Patent Number:** 5,757,170  
 [45] **Date of Patent:** \*May 26, 1998

[54] **METHOD AND APPARATUS FOR  
 REDUCING CURRENT SUPPLIED TO AN  
 INTEGRATED CIRCUIT USEABLE IN A  
 COMPUTER SYSTEM**

4,388,537 6/1983 Kanuma ..... 307/296  
 5,065,361 11/1991 Yoshizawa et al. .... 307/296.1  
 5,173,683 12/1992 Brighenti et al. .... 340/505  
 5,412,308 5/1995 Brown ..... 323/267  
 5,446,367 8/1995 Pinney ..... 323/267

[75] **Inventor:** David L. Pinney, Boise, Id.

*Primary Examiner*—Adolf Berhane  
*Attorney, Agent, or Firm*—Seed and Berry LLP

[73] **Assignee:** Micron Technology, Inc., Boise, Id.

[\*] **Notice:** The term of this patent shall not extend beyond the expiration date of Pat. No. 5,446,367.

# [57] ABSTRACT

An integrated circuit of the present invention includes power regulating circuitry for reducing preregulator bias current. In one embodiment, power regulating circuitry includes a two stage preregulator for supplying current to a charge pump and a primary regulator. The first stage includes a high power operational amplifier for quickly establishing substrate bias and other pumped voltages before primary voltage is coupled to the remainder of the integrated circuit. Preregulated and pumped voltages are used to establish a reference voltage for the primary regulator. The second stage preregulator includes a low power series regulator to power the charge pumps and so maintain the reference voltage. When the primary regulator has generated the primary voltage level, the power regulating circuitry couples the primary voltage to the remainder of the integrated circuit and disables the first stage preregulator. Using circuitry and operating methods of the present invention, the total operating and standby current supplied to the integrated circuit no longer includes the bias currents related to the operation of the high power operational amplifier.

[21] **Appl. No.:** 726,032

[22] **Filed:** Oct. 7, 1996

## Related U.S. Application Data

[63] Continuation of Ser. No. 496,741, Jun. 29, 1995, Pat. No. 5,563,499, which is a continuation of Ser. No. 67,194, May 25, 1993, Pat. No. 5,446,367.

[51] **Int. CL<sup>6</sup>** ..... G05F 1/40

[52] **U.S. Cl.** ..... 323/266; 327/538

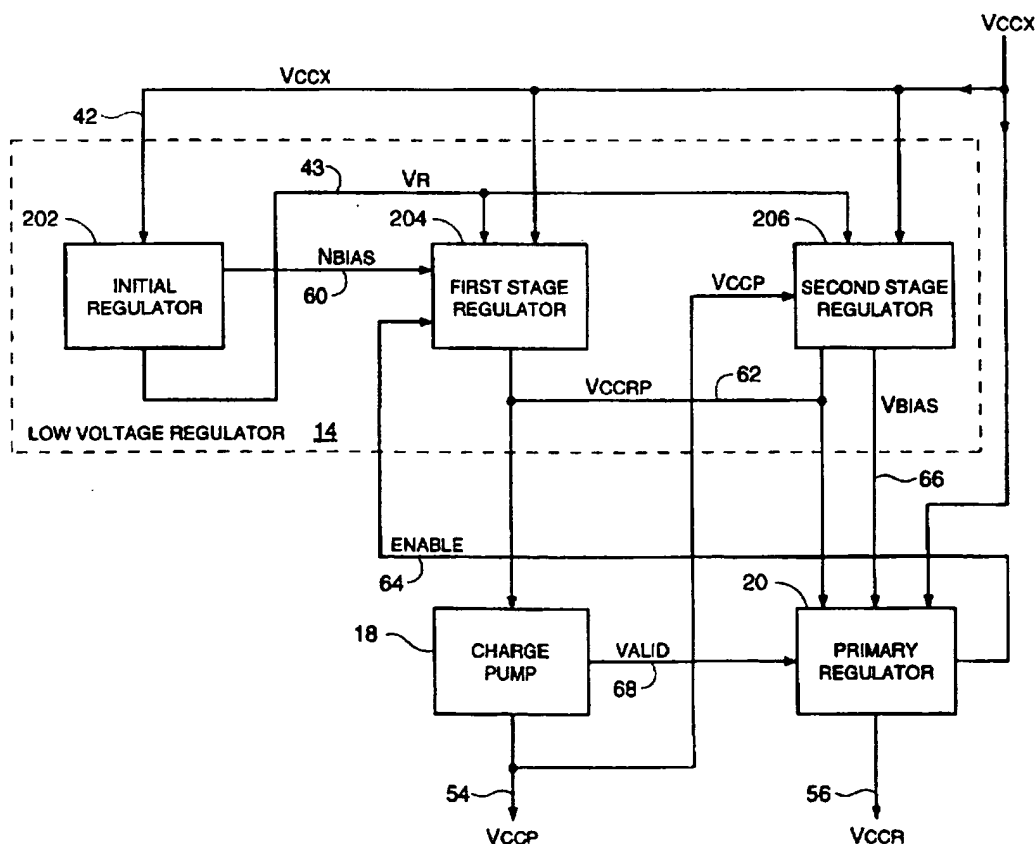
[58] **Field of Search** ..... 323/266, 224, 323/313, 267, 272; 327/530, 538

## [56] References Cited

### U.S. PATENT DOCUMENTS

3,806,791 4/1974 Johnson ..... 323/DIG. 1  
 4,129,788 12/1978 Chavannes ..... 307/11

**38 Claims, 7 Drawing Sheets**



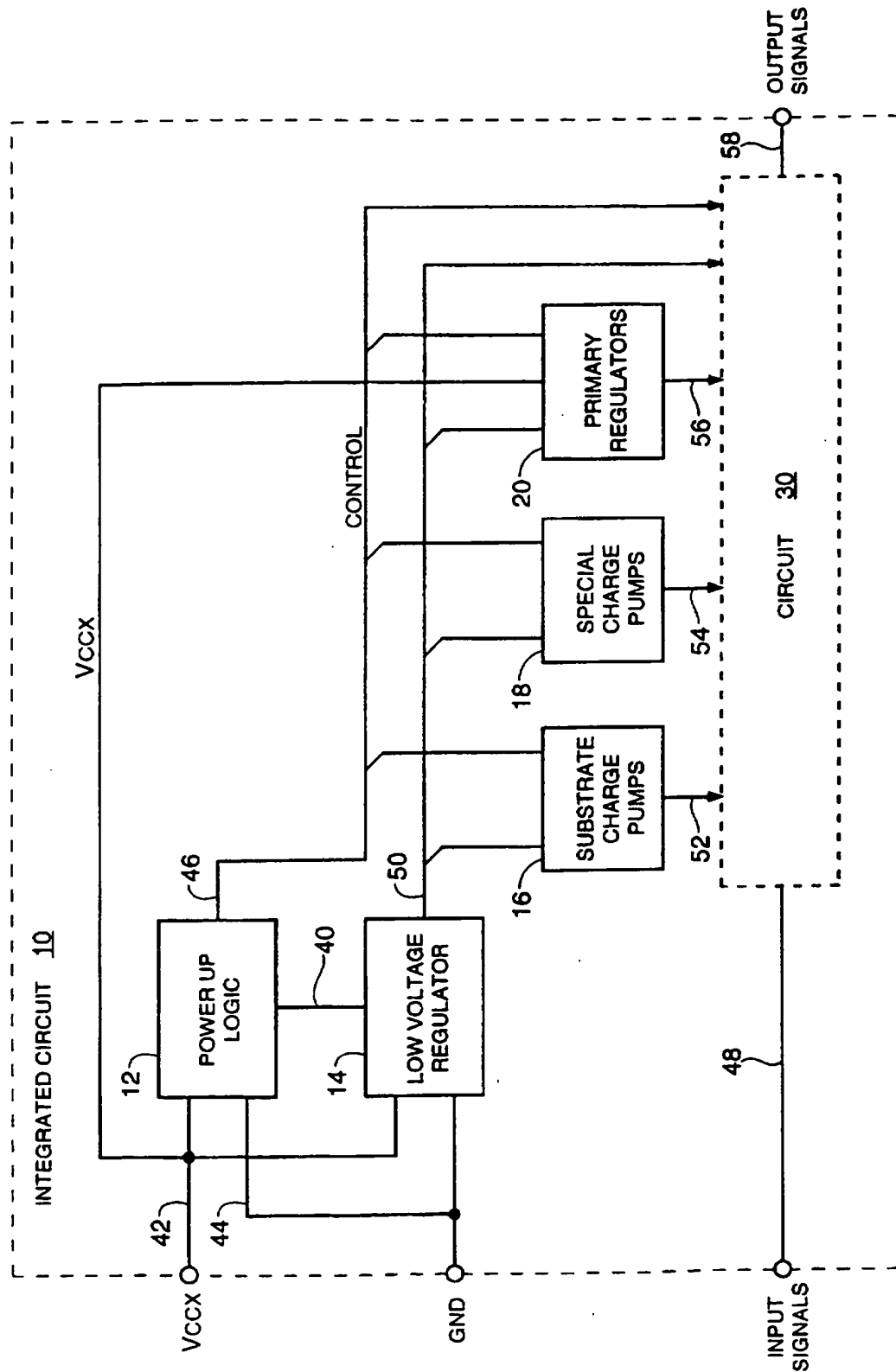


FIG. 1

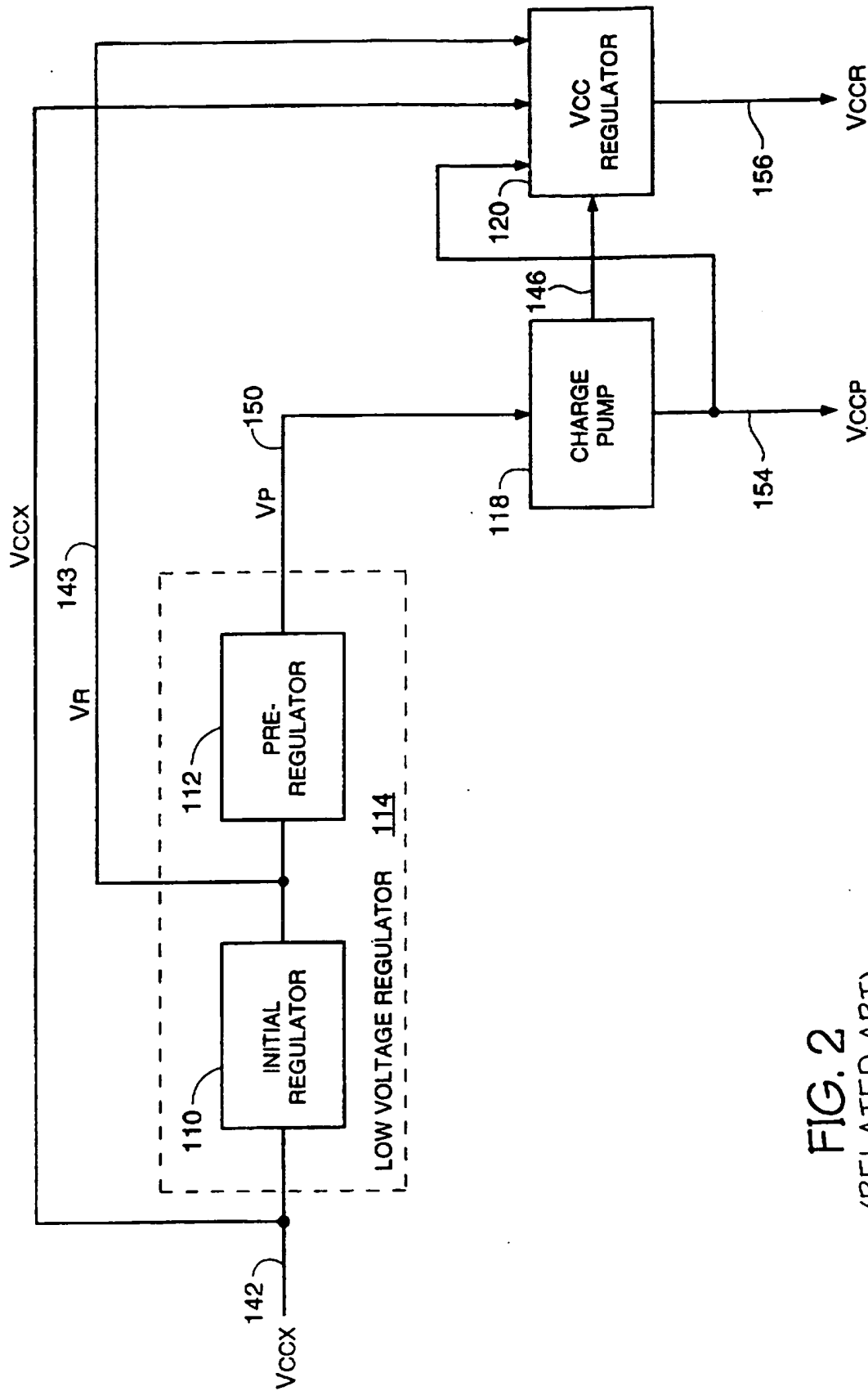


FIG. 2  
(RELATED ART)

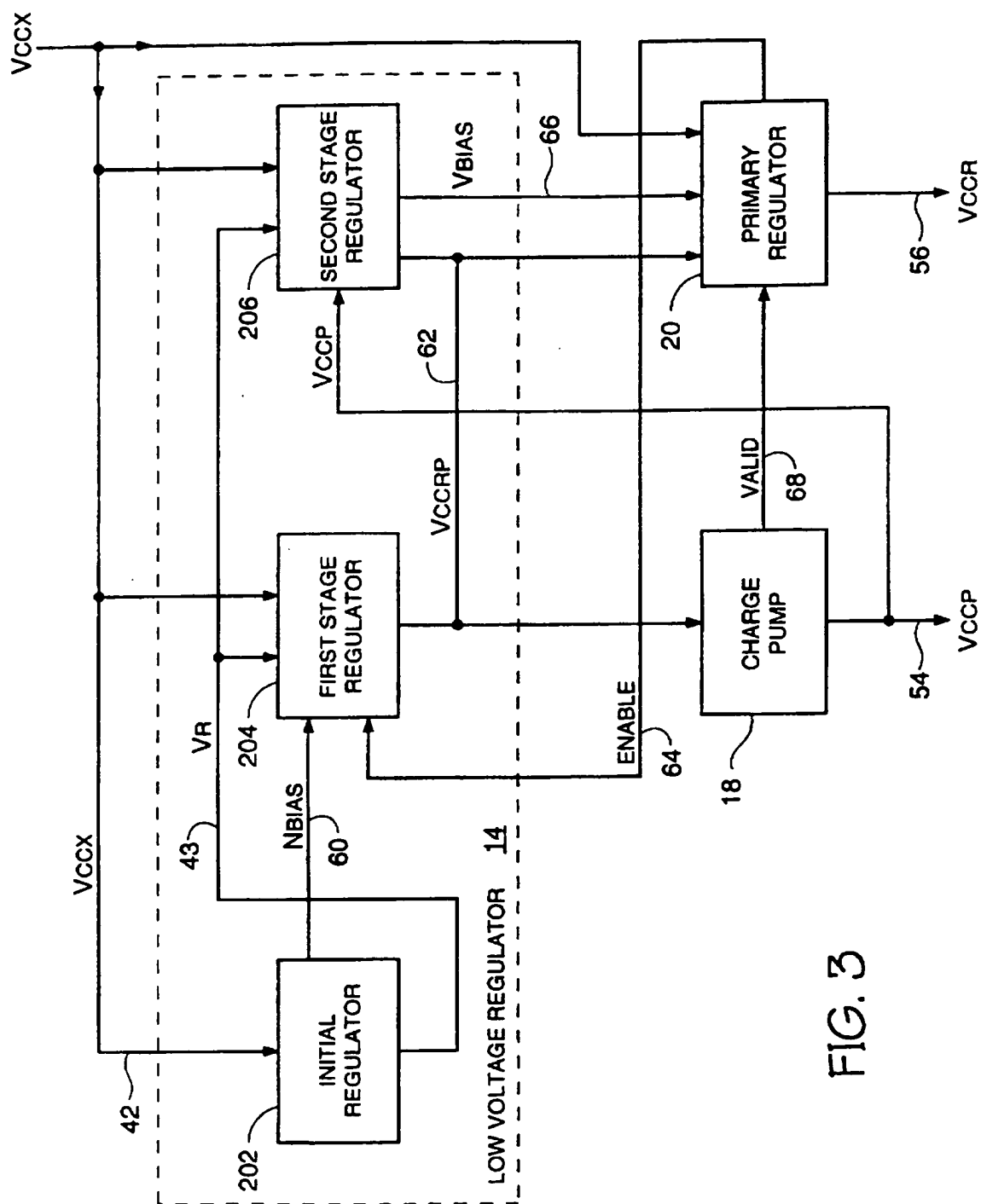


FIG. 3

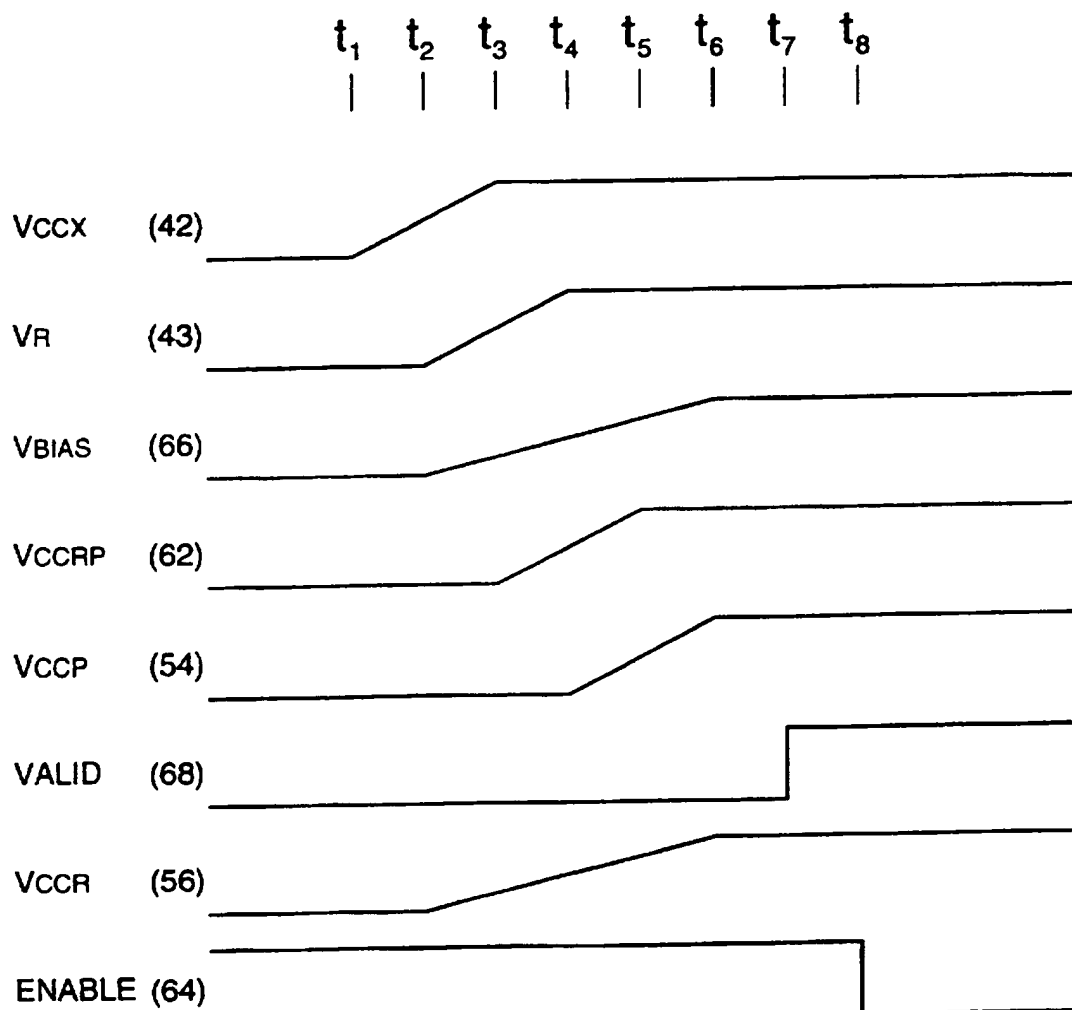


FIG. 4

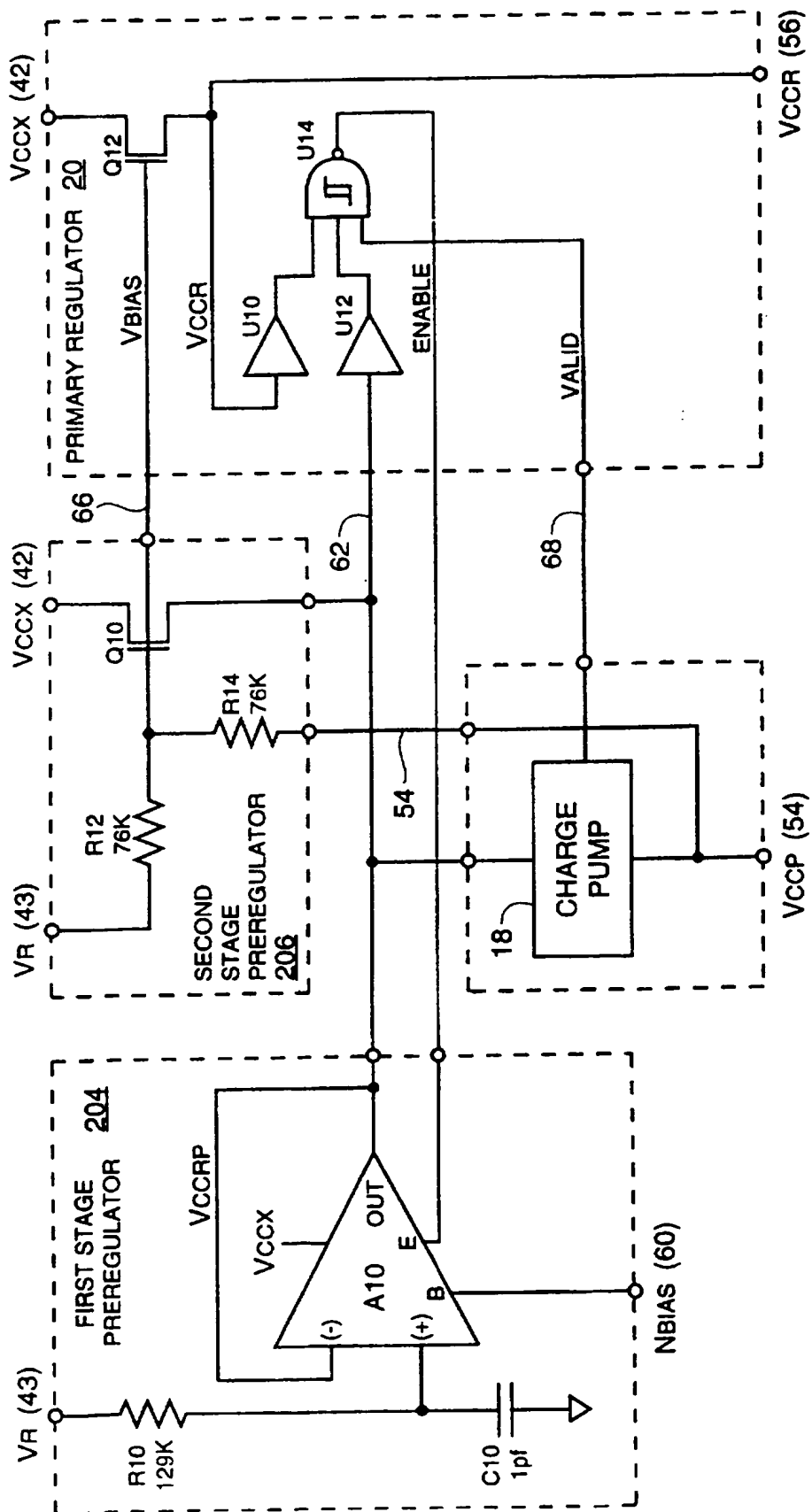


FIG. 5



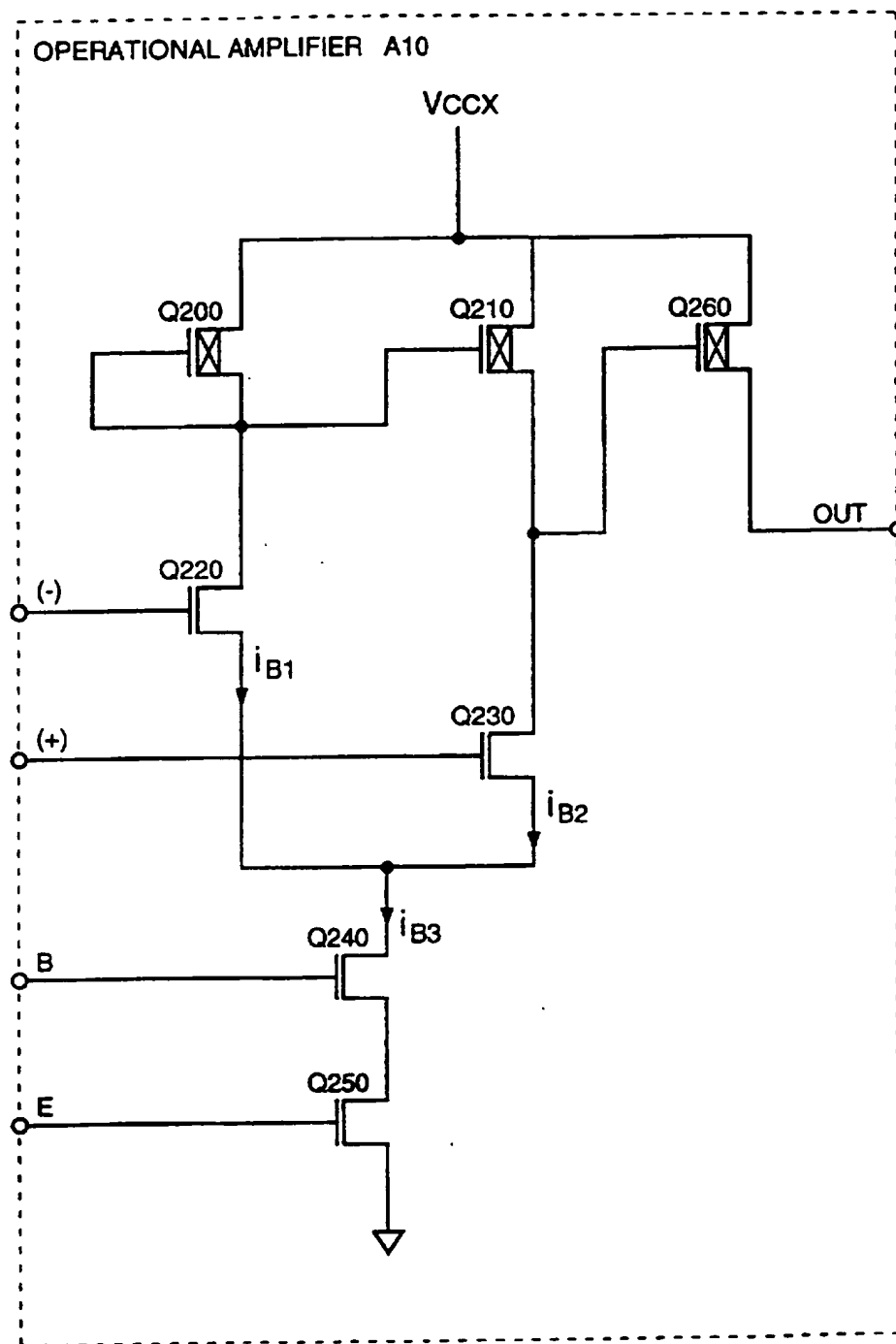


FIG. 6

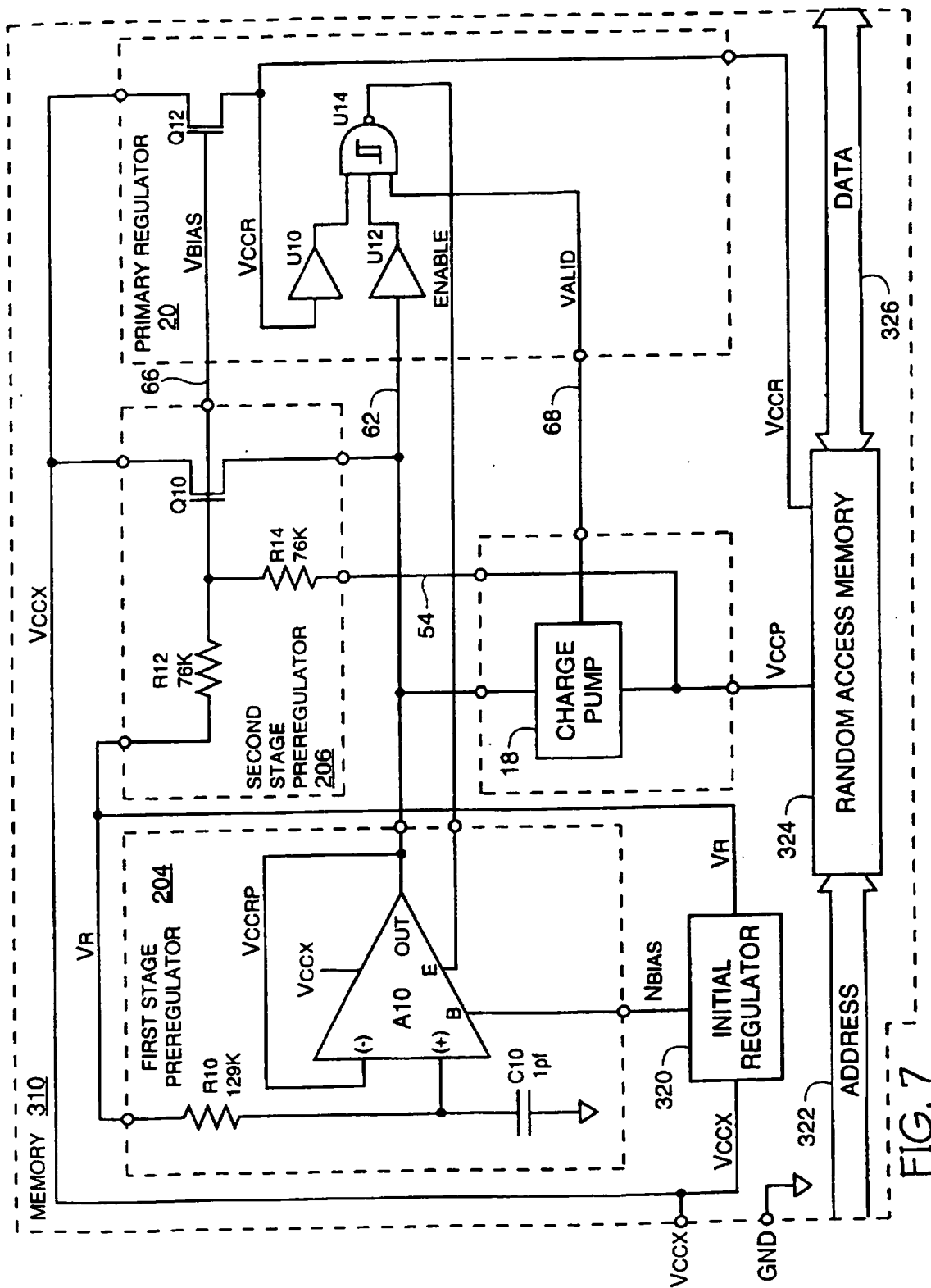


FIG. 7

# METHOD AND APPARATUS FOR REDUCING CURRENT SUPPLIED TO AN INTEGRATED CIRCUIT USEABLE IN A COMPUTER SYSTEM

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 08/496,741, filed Jun. 29, 1995, U.S. Pat. No. 5,563,499 which application claims priority from U.S. patent application Ser. No. 08/067,194, filed May 25, 1993, issued as U.S. Pat. No. 5,446,367.

## FIELD OF THE INVENTION

The present invention relates generally to integrated circuits, and more particularly, to integrated circuits that employ on-chip voltage regulation.

## BACKGROUND

The typical integrated circuit is designed to connect to a single external supply voltage. Within the integrated circuit several internal voltages are often used for example to bias the substrate, to power subcircuits, and to charge circuitry having distributed and parasitic capacitance. The integrated circuit design, therefore, includes voltage regulators for developing the internal voltages from the single externally supplied voltage. Each voltage regulator operates at a given efficiency, usually in the range of 50 to 80 percent. The losses inherent in less than 100 percent efficiency are expended as heat. In addition, some conventional voltage regulator circuits require continuous current flow for establishing bias voltages. For integrated circuits including dynamic random access memory, for example, the current drawn from the external voltage supply when the circuit is idle is almost entirely the bias current required for voltage regulation.

FIG. 2 is a functional block diagram of a voltage regulator circuit for a conventional integrated circuit. The externally supplied voltage VCCX on line 142 is input to an initial regulator 110. Initial regulator 110 includes a series pass regulator designed to drive high impedance loads. Initial regulator 110 is coupled to preregulator 112 and VCC regulator 120. Preregulator 112 and VCC regulator 120 include series pass regulators that are physically larger than the regulator used in initial regulator 110. These larger regulators more efficiently pass larger currents to lower impedance loads than the smaller regulator of initial regulator 110. However, as a consequence of the ability to regulate larger currents, these larger regulators dissipate more energy as heat and require larger bias currents than a smaller regulator. From 50 to 98 percent of the total standby power dissipation of a conventional integrated circuit dynamic memory device is dissipated by the circuit performing the function of preregulator 112. Preregulator 112 in the conventional circuit must be carefully designed.

The design of preregulator 112 is constrained by several design goals. Preregulator 112 should have low impedance drive capability to support rapid changes in load current supplied to charge pump 118. Second preregulator 112 should be located in an area of the integrated circuit where power dissipation in the form of heat can be tolerated. As an analog circuit, preregulator 112 should be located in an area of the integrated circuit away from digital circuitry so that interference between the analog and digital circuits is minimal. Coupling of substrate currents is one example of

unintended coupling that can be reduced by physically separating analog and digital circuits.

In the conventional design of preregulator 112, sophisticated circuitry is employed to avoid underdamped output voltage to charge pump 118 when supply voltage VCCX or load current to charge pump 118 changes suddenly. Such circuitry conventionally takes the form of an operational amplifier requiring large bias currents (for example 5 milliamps) to support a large series pass transistor (for example 10,000 microns by 1.5 microns). The complexity of the operational amplifier adds to space requirements for preregulator 112 and adds to the bias current requirement, the power dissipation, and the heat generated by preregulator 112.

To assure accurate performance of the operational amplifier, conventional integrated circuit design techniques require additional mask steps and tighter tolerance controls for the fabrication processes involved as compared to the mask steps and process controls required for the remainder of the integrated circuit. Additional mask steps and process controls add to the expense of integrated circuit manufacture, increase fabrication time, and decrease yield.

Some applications require integrated circuits having low operating and low standby power consumption. In applications, including for example, portable computers, low power consumption is desirable while operating and highly desirable while portions of the computer are idle. The summation of the bias current drawn by each integrated circuit in the computer is a significant continuous current drain on the battery. Bias currents, therefore, contribute to limited battery operation, contribute to increased cost for sufficient battery supplies for particular applications, and make some applications infeasible.

Thus, there remains a need for an integrated circuit design having improved voltage regulation circuitry characterized by lower bias current consumption. A design is needed for providing regulated voltage to the subcircuits of an integrated circuit while requiring less bias current, while occupying less area of the integrated circuit, while dissipating lower power and generating less heat, and while responding to abrupt changes in supply and load conditions without generating underdamped output voltage.

## SUMMARY

Accordingly, an integrated circuit in one embodiment of the present invention includes a preregulator, a regulator, timing logic, and a subcircuit of the integrated circuit that uses regulated power. The integrated circuit receives an input power signal from an external power supply.

The preregulator receives a flow of input current from the input power signal and generates a reference signal. In one embodiment the reference signal is developed from a stable voltage output from a band gap reference circuit. In another embodiment, the reference signal is developed from the output of a charge pump.

The regulator regulates the input power signal using the reference signal as a reference for regulation and thereby generates a regulated power signal for the subcircuit.

Timing logic determines when the regulated power is being adequately provided and generates a control signal. The control signal is coupled to the preregulator. The preregulator is designed to respond to the control signal by limiting the flow of input current to the preregulator. In one embodiment, the preregulator includes two circuits: one circuit consuming lower bias current than the other. When the control signal is received, the circuit consuming more

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bias current is partially or completely disabled so that total bias current consumption is reduced.

According to a first aspect of such an integrated circuit, the preregulator includes an operational amplifier for high speed regulation of large in-rush currents and a series regulator characterized by low bias current consumption. By disabling the operational amplifier after initial current requirements have been satisfied, the total operating power dissipation for the integrated circuit is reduced.

According to another aspect, an integrated circuit design incorporating an operational amplifier in the preregulation circuitry can be designed and developed in less time because the functional requirements of the operational amplifier are simplified.

According to yet another aspect, interference between the operational amplifier and digital circuits on the integrated circuit is reduced when the operational amplifier is disabled. The design of the operational amplifier is simplified because interference is less important.

According to another embodiment, a dynamic random access memory (DRAM) for operation from an external supply of about 5 volts includes a preregulator and regulator of the present invention for low power consumption. Functional circuits on the DRAM integrated circuit operate at a voltage about 3 volts. Lower total power consumption is achieved by supplying internal voltage from a low power series regulator after meeting the need for supplying the internal voltage from a high power operational amplifier regulator.

The present invention may be practiced according to a method for reducing input power supply current from an input power signal supplied to a subcircuit of an integrated circuit. The integrated circuit includes a first preregulator and a second preregulator which operates with less input power supply current than the first preregulator, a regulator, a charge pump, and a subcircuit. The method includes the steps of: supplying power from the input power signal through the first preregulator to the charge pump until the subcircuit receives regulated power from the regulator; supplying power from the input power signal through the second preregulator to the charge pump; developing a regulator control signal at least in part responsive to the output of the charge pump; and supplying regulated power from the input power signal through the regulator to the subcircuit in response to the regulator control signal.

According to a first aspect of such a method, by supplying the charge pump from the second stage of the preregulator, the first stage of the preregulator is no longer necessary. Power consumption can, therefore, be reduced by ceasing to supply power from the first stage preregulator. When power is no longer being supplied by the first stage regulator, the flow of bias currents to the first stage preregulator can be limited or disabled.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a functional block diagram of an integrated circuit of the present invention.

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FIG. 2 is a functional block diagram of the power regulation circuitry of a conventional integrated circuit.

FIG. 3 is a functional block diagram of a portion of the power regulation circuitry of the integrated circuit of FIG. 1.

FIG. 4 is a timing diagram showing signals related to the power regulation circuitry of FIG. 3.

FIG. 5 is a schematic diagram of a portion of the circuitry shown in FIG. 3.

FIG. 6 is a schematic diagram of operational amplifier A10 shown in FIG. 5.

FIG. 7 is a diagram of a memory according to an embodiment of the present invention.

In each functional block diagram, a group of signals is shown as a single line. A single line between functional blocks represents one or more control or power signals. Signals that appear on several figures and have the same mnemonic are directly or indirectly coupled together.

In each timing diagram the vertical axis represents analog power and control signal levels and binary logic levels; the horizontal axis represents time. Neither axis is drawn to scale. The vertical axis is intended to show the transition from active (asserted) to passive (non-asserted) levels of each logic signal. The voltages corresponding to the levels of the various analog and digital signals are not necessarily identical among the various signals.

#### DESCRIPTION OF THE INVENTION

FIG. 1 is a functional block diagram of an integrated circuit of the present invention. Integrated circuit 10 is an integrated circuit having conventional functions shown generally as circuit 30, and connections for input power signals (VCCX) on line 42, ground signals (GND) on line 44, an input shown generally as input signals on line 48 and an output shown generally as output signals on line 58. The need for an output signal depends on the function of circuit 30. Line 58 may be deleted when the function of circuit 30 does not require provision of an output signal. As shown, circuit 30 uses power signals and control signals for initialization and operation.

Power signals provided to circuit 30 are derived from power signals on line 42. When circuit 30 requires multiple power signals for operation, integrated circuit 10 includes low voltage regulator 14 and primary regulators 20. Low voltage regulator 14 provides intermediate power signals on line 50, coupled as required to substrate charge pumps 16, special charge pumps 18, and primary regulators 20. Substrate charge pumps 16 provide power signals on line 52 coupled to circuit 30. Special charge pumps 18 provide power signals on line 54 coupled to circuit 30. Primary regulators 20 provide power signals on line 56 coupled to circuit 30. When circuit 30 requires fewer power signals for operation, intermediate power signals on line 50 may be eliminated and related simplifications may be employed as is well known in the art. Taken together, signals on lines 50-56 provide operative power to circuit 30, enabling it to perform its intended functions.

Low voltage regulator 14 receives power and control signals on line 40 provided by power up logic 12. Control signals on line 40 enable the operation of low voltage regulator 14. Similarly, control signals on line 46, provided by power up logic 12 enable the operation of substrate charge pumps 16, special charge pumps 18, and primary regulators 20. The sequence of enablement of these several functional blocks depends on the circuitry of each functional block and upon the power signal sequence requirements of circuit 30.

The functions of power up logic 12 in another equivalent embodiment, not shown, are incorporated into threshold detectors and sequencing logic in low voltage regulator 14, in charge pumps 16 and 18, and in primary regulators 20. In one example of such an embodiment, charge pumps 18 detect when power signals on line 54 are valid and supply a validity signal to primary regulators 20. Primary regulators 20 include shunt circuitry known to those skilled in the art to hold regulated power signals on line 56 at ground until a predetermined time, for example, after validity signals are received from charge pumps 18.

In another equivalent embodiment of the invention, circuit 30 does not use bias or power signals that would require a charge pump for generation. In such a case, substrate charge pumps 16 and special charge pumps 18 are not implemented; and reference voltages, if needed by as primary regulator 20, are provided by low voltage regulator 14.

FIG. 2 is a functional block diagram of the power regulation circuitry of a conventional integrated circuit. Refer to the background section for a discussion of FIG. 2.

FIG. 3 is a functional block diagram of the power regulation circuitry of the integrated circuit of FIG. 1. Low voltage regulator 14 is shown in more detail whereas charge pump 18 and primary regulator 20 are carried over from FIG. 1 in order to show interface signals in more detail. Ground signal 44 is not shown explicitly but is coupled to each functional block as is well known to those skilled in the art.

A charge pump of the type suitable for use in the circuitry shown in FIGS. 1, 3, and 5 is shown in U.S. Pat. No. 4,388,537, "Substrate Bias Generation Circuit" to Kanuma, incorporated herein by reference. Those having ordinary skill in the art will recognize that a buffer similar to U10 shown and described in reference to FIG. 5 can be added to the Kanuma design for generation of the VALID signal.

Low voltage regulator 14 includes initial regulator 202, first stage preregulator 204, and second stage preregulator 206. In general a preregulator is a regulator or a source whose output is used by another regulator. As a source, a preregulator generates a reference voltage or current or generates a control signal, depending on design choices and the needs of circuit 30. A regulator is a device that provides a signal characterized by a stable value. For example, a voltage regulator provides a signal having a voltage that is maintained between narrow tolerances, independent of supply and load variation. Thus, the preregulating means of integrated circuit 10 includes low voltage regulator 14 and charge pump 18 because charge pump 18 provides a voltage VCCP as a reference to second stage preregulator 206, as will be discussed below.

Low voltage regulator 14 receives input power signal VCCX on line 42. In one embodiment, VCCX is a direct current voltage of 5 volts with a current supply capability of several hundred milliamps. VCCX powers initial regulator 202 which generates bias voltage NBIAS on line 60 and reference signal VR on line 43. First stage preregulator 204 receives input power signal VCCX on line 42. When enabled by the ENABLE signal on line 64, first stage preregulator responds to reference signal VR on line 43 and bias voltage NBIAS on line 60 to generate a regulated voltage VCCRP on line 62. VCCRP supplies power to charge pump 18 and acts as a reference voltage for timing purposes to be discussed below with primary regulator 20. VCCRP in one embodiment is about 3.3 volts.

The ENABLE signal on line 64, when removed or not asserted, operates to limit the flow of input current to first

stage preregulator 204. In one embodiment, first stage preregulator 204 is turned off so that it draws no current from input power signal VCCX.

Second stage preregulator 206 receives input power signal VCCX on line 42. In response to reference signal VR, second stage preregulator 206 generates regulated voltage VCCRP on bus line 62 and regulator control signal VBIAS on line 66. Since the output of second stage preregulator 206 is connected with the output of first stage preregulator 204, the respective output currents sum on bus line 62. Therefore, the current drawn from bus line 62 when first stage preregulator 204 is turned off is supplied entirely by second stage preregulator 206.

Charge pump 18 receives power signal VCCRP on bus line 62 to generate and maintain pumped voltage VCCP on line 54. When pumped voltage VCCP has reached a stable condition, charge pump 18 generates the VALID signal on line 68. The stable value of VCCP depends on the design of integrated circuit 10. In one embodiment, for example, a voltage in the range -0.7 to -1.1 volts is output by a substrate charge pump. In other embodiments the voltage output of special charge pumps are, for example, a voltage of 5.4 volts or a voltage about one VT (0.7 volts) above VCC. Pumped voltage VCCP is used by circuit 30 in one embodiment to maintain the substrate below ground potential, in another embodiment to bias memory word lines to a potential above the voltage of power signal VCCR on line 56, and in another embodiment as a regulated power signal to satisfy the special bias and power requirements of circuit 30. Pumped voltage VCCP is used in the embodiment shown in FIG. 3 by second stage preregulator 206 as a reference voltage for the development of the VBIAS regulator control signal on line 66.

Primary regulator 20 receives input power signal VCCX on line 42. In response to regulator control signal VBIAS on line 66, primary regulator 20 generates regulated power signal VCCR on line 56. In one embodiment, VCCR is a voltage of about 3.3 volts with the capability to supply several hundred milliamps of current to circuit 30.

Primary regulator 20 includes timing circuitry for generating the ENABLE signal on line 64. In one embodiment, the timing circuitry is responsive to the magnitude of the VCCRP voltage on 62, the magnitude of the VCCR voltage on line 56, and the presence of the VALID signal on line 68. In an equivalent embodiment, the ENABLE signal is developed from timing delays measured from the application of input power signal VCCX. In yet another equivalent embodiment, the ENABLE signal is developed in response to a combination of timing delays, signal detection, and magnitude comparisons. The purpose of limiting the bias current drawn by first stage preregulator 204, and thus reducing input power supply current to integrated circuit 10, can be accomplished in a preferred embodiment by turning off first stage preregulator 204 as soon as power signal VCCR on line 56 initially reaches a stable condition. This technique is preferred because it minimizes bias current consumption. Other embodiments that employ timing circuitry to accomplish this purpose by generating or removing the ENABLE signal at other times are equivalent. Before describing a circuit embodiment of the process of reducing input power supply current to integrated circuit 10, we now turn to a timing description of that process.

FIG. 4 is a timing diagram showing signals related to the power regulation circuitry of FIG. 3. After input power signal VCCX is applied to integrated circuit 10 at time t1, the voltage increases to a stable operating level at time t3. By

time t2 the voltage of input power signal VCCX is sufficient for initial regulator 202 to begin generating reference signal VR. The voltage of reference signal VR increases to a stable operating level at time t4. By time t3, the voltage of reference signal VR is sufficient for first stage preregulator 204 to begin raising the voltage on bus line 62 as represented by power signal VCCRP. By time t4, the voltage of power signal VCCRP is sufficient for charge pump 18 to begin generating regulated power signal VCCP. For the embodiment wherein VBIAS is generated responsive to VR and VCCP, second stage preregulator 206 generates VBIAS beginning at time t2. The voltage of signal VBIAS increases to a stable operating level at time t6 when the voltage of regulated power signal VCCP has reached a stable operating level. In response to regulator control signal VBIAS, primary regulator 20 generates regulated power signal VCCR which reaches a stable operating level at time t6. At time t7, charge pump 18 detects that its output, VCCP, is at a stable operating level and generates the VALID signal. In response to signal detection and magnitude comparisons already discussed in relation to timing circuitry included in primary regulator 20, the ENABLE signal is generated at time t8.

Although the timing diagram represents the sequence of signals for one embodiment, some variation of the sequence is within the scope of the present invention. For example, as will be understood by those of skill in the art, the response times of initial regulator, first and second stage preregulator, charge pump, and primary regulator may vary with the complexity, capacitance, and drive capability of the respective circuitry so that the sequence of events between times t1 and t7 may vary. In addition, the regulated power signals VCCP and VCCR may be withheld from circuit 30 by shunt (clamp) circuits until each or both have reached stable operating levels, for example, at time t6. Because the time axis is not to scale, some of the events described in sequence occur simultaneously in equivalent embodiments.

FIG. 5 is a schematic diagram of a portion of the circuitry shown in FIG. 3. Reference signal VR is generated by a circuit, not shown, having limited current drive capability. In one embodiment, signal VR is developed by a band gap reference circuit. For an explanation of band gap reference circuits, see "A Precision Reference Voltage Source," Karel E. Kuijk, IEEE Journal of Solid State Circuits June 1973. As a source for signal VR, other equivalent circuits are well known in the art for example circuits including an operational amplifier, a differential amplifier, or a charge pump. Reference signal VR is filtered by resistor R10 and capacitor C10 and applied to operational amplifier A10. Operational amplifier A10 provides unity gain buffering so that the output power signal VCCRP on line 62 has a voltage corresponding to reference signal VR with increased current drive capability. The current supplied by operational amplifier A10 is conducted on bus 62 to power charge pump 18.

Charge pump 18 generates regulated power signal VCCP at a pumped voltage level as described with reference to FIG. 3.

Resistors R12 and R14 operate as a voltage divider to provide the VBIAS signal on line 66 with a voltage between the voltage of VR and VCCP. Because both VR and VCCP have regulated voltage characteristics, the voltage VBIAS is a regulated scaled result determined in part by the values of resistors R12 and R14. Thus, resistors R12 and R14 cooperate as means for scaling reference signal VR to provide regulator control signal VBIAS with a voltage between the voltage of reference signal VR and regulated power signal VCCP.

The VBIAS signal on line 66 controls the conductivity of transistor Q10 so that the current passing through the

source-drain channel is regulated. The gate of transistor Q10 is a so called control terminal of transistor Q10. Transistor Q10, therefore, operates as a regulator, supplying current onto bus 62.

Bus 62 conducts current supplied by either or both amplifier A10 and regulator Q10. When amplifier A10 is disabled, current from Q10 supplies charge pump 18 and the timing circuitry of primary regulator 20.

Transistor Q12 operates as a regulator in a manner identical to the operation of transistor Q10. In an equivalent embodiment, regulated power signal VCCR is generated with a voltage different from the voltage of power signal VCCRP by connecting the gate of Q12 to an alternate source of bias voltage as is well known in the art.

The ENABLE signal controls the operation of amplifier A10. The ENABLE signal is generated by timing means shown, in FIG. 5 as logic buffers U10 and U12, and NAND gate U14. Buffer U10 outputs a logic level corresponding to whether VCCR exceeds a threshold voltage. In an alternate embodiment, an analog comparator or level translator is used in place of the logic buffer. The function of the buffer is to compare the magnitude of the voltage of the VCCR signal to a threshold voltage and to generate an output binary logic signal as a result of the comparison. The input validly differs from the threshold when, in the case of positive input and threshold voltages the input is in excess of the threshold. Likewise, when the input and threshold voltages are negative, the input validly differs from the threshold when the input is further negative than the threshold.

Buffer U12 operates in a manner similar to buffer U10, comparing the magnitude of the voltage of the VCCRP to a threshold voltage and generating an output binary logic signal as a result of the comparison.

NAND gate U14 combines the result of magnitude comparisons performed by buffers U10 and U12 with the VALID signal on line 68, generated by charge pump 18. The ENABLE signal is a high voltage until the signals on all three inputs to gate U14 are logic '1' whereupon the ENABLE signal is a low voltage. The effect of the voltage level of the ENABLE signal in a preferred embodiment is best understood with reference to the schematic of operational amplifier A10.

FIG. 6 is a schematic diagram of operational amplifier A10 shown in FIG. 5. The circuit of operational amplifier A10 is a differential amplifier having balanced loads Q200 and Q210 which provide currents  $i_{b1}$  and  $i_{b2}$ . The difference in input voltages on the gates of transistors Q220 and Q230 cause the ratio of these two currents to vary according to the difference. These two currents sum to form current  $i_{b3}$ , into a bias circuit formed in part by transistors Q240, Q250.

As shown in FIG. 5, the gate of transistor Q240 is coupled to the NBIAS signal on line 60, generated by initial regulator 110. Because Q250 is in series with transistor Q240 and current  $i_{b3}$  must pass through transistor Q250 in full, the ENABLE signal coupled to the control terminal (gate) of transistor Q250, when at a low voltage will reduce the flow of current  $i_{b3}$ . In a preferred embodiment, Q250 is turned off so that virtually no current passes through its source-drain channel. By turning off transistor Q250, no bias current is drawn from input power signal VCCX into operational amplifier A10. Thus, the total current drawn by integrated circuit 10 from input power signal VCCX is reduced by interrupting the flow of bias current to amplifier A10.

In an equivalent embodiment, the flow of bias current to low voltage regulator 14 shown in FIGS. 1 and 3 is limited by alternate limiting means including, for example, circuitry

to pinch off the source-drain channel of a regulator transistor, a load transistor, a biasing transistor, or a similar control transistor; circuitry for coupling a control signal to the gate or an equivalent control terminal; or circuits for coupling such a control signal to an additional gate of the same device for the purpose of independent control. Equivalently, means for limiting current include switching devices for interrupting current flow and back biasing circuits for increasing a voltage to interfere with current flow.

The transistor Q260 shown in FIG. 6 typically occupies an area about an order of magnitude larger than the average size of transistors Q220 through Q250. The large size is necessary for satisfying in-rush current needed by charge pumps. By operating amplifier A10 primarily during the time before circuit 30 is powered and disabling amplifier A10 shortly thereafter, transistor Q260 can be located with less concern for signal interference.

FIG. 7 is a diagram of a memory according to an embodiment of the present invention. Random access memory 324 provides data signal 326 representing data stored at an address corresponding to address signal 322. Random access memory 324 is powered by regulated power signal VCCP. Power signal VCCP supplies an elevated voltage to word lines in random access memory 324.

A wide range of alternate embodiments are equivalent to the embodiments described above. For example, circuit 30 (a subcircuit of integrated circuit 10) in alternate embodiments includes an analog circuit, a logic circuit, a memory, a signal processor, a microprocessor, a microcomputer, a signal converter (such as analog to digital, digital to synchro, and the like), a device for communications, for process control, for display, for monitoring safety conditions, or for monitoring conditions related to security. The benefit of reducing input current to an integrated circuit has primary application to battery operated systems, but has important applications in all systems for meeting energy conservation goals.

The foregoing description discusses preferred embodiments of the present invention, which may be changed or modified without departing from the scope of the present invention.

For example, P-channel FETs discussed above may be replaced with N-channel FETs (and vice versa) in some applications with appropriate polarity changes in controlling signals as required. Moreover, the P-channel and N-channel FETs discussed above generally represent active devices which may be replaced with bipolar or other technology active devices.

Still further, those skilled in the art will understand that the logical elements described above may be formed using a wide variety of logical gates employing any polarity of input or output signals and that the logical values described above may be implemented using different voltage polarities. As an example, an AND element may be formed using an AND gate, a NAND gate, or a wired-AND connection when all input signals exhibit a positive logic convention or it may be formed using an OR gate, a NOR gate, or a wired-OR connection when all input signals exhibit a negative logic convention.

These and other changes and modifications are intended to be included within the scope of the present invention.

While for the sake of clarity and ease of description, several specific embodiments of the invention have been described; the scope of the invention is intended to be measured by the claims as set forth below. The description is not intended to be exhaustive or to limit the invention to

the form disclosed. Other embodiments of the invention will be apparent in light of the disclosure to one of ordinary skill in the art to which the invention applies.

The words and phrases used in the claims are intended to be broadly construed.

A "circuit" or "subcircuit" refers generally to integrated circuits and includes but is not limited to a packaged integrated circuit, an unpackaged integrated circuit, a combination of packaged or unpackaged integrated circuits or both, a microprocessor, a microcontroller, a memory, a register, a flip-flop, a charge-coupled device, combinations thereof, and equivalents.

A "signal" refers to mechanical and/or electromagnetic energy conveying information. When elements are coupled, a signal can be conveyed in any manner feasible in light of the nature of the coupling. For example, if several electrical conductors couple two elements, then the relevant signal comprises the energy on one, some, or all conductors at a given time or time period. When a physical property of a signal has a quantitative measure and the property is used by design to control or communicate information, then the signal is said to be characterized by having a "value." For a binary (digital) signal, the two characteristic values are called logic "levels."

I claim:

1. A voltage regulator for supplying a regulated voltage to an integrated circuit, comprising:

a first regulator having a power supply input terminal, a first regulated voltage output terminal, and a control input terminal, the first regulator being adapted to supply to the integrated circuit a first regulated voltage at the first regulated voltage output terminal from a first power supply voltage applied to the power supply input terminal, the power drawn by the first regulator from the first power supply input terminal being controlled by a power control signal applied to the control input terminal;

a second regulator having a power supply input terminal, and a second regulated voltage output terminal, the second regulator being adapted to supply to the integrated circuit a second regulated voltage at the second regulated voltage output terminal from a second power supply voltage applied to the power supply input terminal; and

a power control circuit coupled to the second regulated voltage output terminal of the second regulator and the control input terminal of the first regulator, the power control circuit generating the power control signal to reduce the power drawn by the first regulator from the first power supply input terminal responsive to the magnitude of the second regulated voltage being within a predetermined range of values.

2. The voltage regulator of claim 1 wherein the first and second power supply input terminals are coupled to each other to form a common node.

3. The voltage regulator of claim 1 wherein the integrated circuit includes a power bus, and wherein the first and second regulated voltage output terminals are coupled to the power bus.

4. The voltage regulator of claim 1 further comprising a charge pump generating a charge pump voltage at a charge pump voltage terminal having a magnitude that is greater than the magnitude of a charge pump supply voltage applied to a power supply input of the charge pump, the power supply input of the charge pump being coupled to the first regulated voltage output terminal of the first regulator, and the charge pump voltage terminal being coupled to the integrated circuit.

5. The voltage regulator of claim 4 wherein the second regulator further includes a first voltage reference input coupled to the charge pump voltage terminal, the magnitude of the second regulated voltage being a function of the magnitude of the charge pump voltage applied to the first voltage reference input.

6. The voltage regulator of claim 5 wherein the second regulator further includes a second voltage reference input receiving a fixed reference voltage, and wherein the magnitude of the second regulated voltage is a function of a comparison between the magnitude of the fixed reference voltage and the magnitude of the charge pump voltage applied to the first voltage reference input.

7. The voltage regulator of claim 1 further comprising a charge pump generating a charge pump voltage at a charge pump voltage terminal having a magnitude that is greater than the magnitude of a charge pump supply voltage applied to a power supply input of the charge pump, the power supply input of the charge pump being coupled to the second regulated voltage output terminal of the second regulator, and the charge pump voltage terminal being coupled to the integrated circuit.

8. The voltage regulator of claim 1 wherein at least one of the first and second regulated voltage output terminals is coupled to the power terminal of the integrated circuit through a charge pump, the charge pump generating a charge pump voltage at a charge pump voltage terminal, the power supply input of the charge pump being coupled to the at least one of the first and second regulated voltage output terminals of the first and second regulators, respectively, and the charge pump voltage terminal being coupled to the power terminal of the integrated circuit.

9. The voltage regulator of claim 1 wherein the power control circuit is coupled to the charge pump voltage terminal of the charge pump, and wherein the power control circuit further inhibits generating the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value unless the magnitude of the charge pump voltage is within a predetermined range.

10. The voltage regulator of claim 1 wherein the power control circuit generates the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value.

11. The voltage regulator of claim 1 wherein the first regulator, the second regulator, and the power control circuit are fabricated on the same substrate as the integrated circuit.

12. The voltage regulator of claim 1 wherein the first regulator comprises:

- a differential amplifier having an output coupled to the first regulated voltage output terminal and a pair of inputs coupled to the first regulated voltage output terminal and a fixed reference voltage, respectively; and

- a current limiting circuit coupled to the power control circuit, the current limiting circuit controlling the current supplied to the differential amplifier responsive to the magnitude of the power control signal.

13. A voltage regulator for supplying a regulated voltage to a power terminal of an integrated circuit, comprising:

- a first regulator having a power supply input terminal adapted to be coupled to a power source, a first regulated voltage output terminal coupled to the power terminal of the integrated circuit to supply a first regulated voltage to the integrated circuit, and a control input terminal, the power supplied to the integrated circuit by the first regulator being controlled by a power control signal applied to the control input terminal;

- a second regulator having a power supply input terminal adapted to be coupled to the power source, and a

second regulated voltage output terminal coupled to the power terminal of the integrated circuit to supply a second regulated voltage to the integrated circuit, the power capacity of the second regulator being less than the power capacity of the first regulator and the efficiency of the second regulator being greater than the efficiency of the first regulator; and

- a power control circuit coupled to the second regulated voltage output terminal of the second regulator and the control input terminal of the first regulator, the power control circuit generating the power control signal to reduce the power supplied to the integrated circuit by the first regulator responsive to the magnitude of the second regulated voltage being within a predetermined range of values.

14. The voltage regulator of claim 13 wherein the first and second regulated voltage output terminals are coupled to the power terminal of the integrated circuit through a charge pump, the charge pump generating a charge pump voltage at a charge pump voltage terminal having a magnitude that is greater than the magnitude of a charge pump supply voltage applied to a power supply input of the charge pump, the power supply input of the charge pump being coupled to the first and second regulated voltage output terminals of the first and second regulators, respectively, and the charge pump voltage terminal being coupled to the power terminal of the integrated circuit.

15. The voltage regulator of claim 14 wherein the second regulator further includes a first voltage reference input coupled to the charge pump voltage terminal, the magnitude of the second regulated voltage being a function of the magnitude of the charge pump voltage applied to the first voltage reference input.

16. The voltage regulator of claim 15 wherein the second regulator further includes a second voltage reference input receiving a fixed reference voltage, and wherein the magnitude of the second regulated voltage is a function of a comparison between the magnitude of the fixed reference voltage and the magnitude of the charge pump voltage applied to the first voltage reference input.

17. The voltage regulator of claim 14 wherein the power control circuit is coupled to the charge pump voltage terminal of the charge pump, and wherein the power control circuit further inhibits generating the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value unless the magnitude of the charge pump voltage is within a predetermined range of values.

18. The voltage regulator of claim 13 wherein the power control circuit generates the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value.

19. The voltage regulator of claim 13 wherein the first regulator, the second regulator, and the power control circuit are fabricated on the same substrate as the integrated circuit.

20. The voltage regulator of claim 13 wherein the first regulator comprises:

- a differential amplifier having an output coupled to the first regulated voltage output terminal and a pair of inputs coupled to the first regulated voltage output terminal and a fixed reference voltage, respectively; and

- a current limiting circuit coupled to the power control circuit, the current limiting circuit controlling the current supplied to the differential amplifier responsive to the magnitude of the power control signal.

21. A memory device, comprising:

- a memory circuit having an address bus adapted to receive a memory address, and a data bus adapted to send and



receive data, the memory circuit being adapted to receive at least one power supply voltage supplying power to the memory circuit;

a first regulator circuit having a power supply input terminal, a first regulated voltage output terminal coupled to the memory circuit, and a control input terminal, the first regulator circuit being adapted to supply a first regulated voltage to the memory circuit at the first regulated voltage output terminal from a first power supply voltage applied to the power supply input terminal, the power supplied to the memory circuit by the first regulator circuit being controlled by a power control signal applied to the control input terminal of the first regulator circuit;

a second regulator circuit having a power supply input terminal, and a second regulated voltage output terminal coupled to the memory circuit, the second regulator circuit being adapted to supply a second regulated voltage to the memory circuit at the second regulated voltage output terminal from a second power supply voltage applied to the power supply input terminal; and

a power control circuit coupled to the second regulated voltage output terminal of the second regulator circuit and the control input terminal of the first regulator, the power control circuit generating the power control signal to reduce the power supplied to the memory circuit by the first regulator circuit responsive to the magnitude of the second regulated voltage being within a predetermined range of values.

22. The memory device of claim 21 wherein the first and second power supply input terminals are coupled to a common node of the memory circuit.

23. The memory device of claim 21 wherein the memory circuit includes a power bus, and wherein the first and second regulated voltage output terminals are coupled to the power bus of the memory circuit.

24. The memory device of claim 21 further comprising a charge pump generating a charge pump voltage at a charge pump voltage terminal having a magnitude that is greater than the magnitude of a charge pump supply voltage applied to a power supply input of the charge pump, the power supply input of the charge pump being coupled to the first regulated voltage output terminal of the first regulator circuit, and the charge pump voltage terminal being coupled to the memory circuit.

25. The memory device of claim 24 wherein the second regulator circuit further includes a first voltage reference input coupled to the charge pump voltage terminal, the magnitude of the second regulated voltage being a function of the magnitude of the charge pump voltage applied to the first voltage reference input.

26. The memory device of claim 25 wherein the second regulator circuit further includes a second voltage reference input receiving a fixed reference voltage, and wherein the magnitude of the second regulated voltage is a function of a comparison between the magnitude of the fixed reference voltage and the magnitude of the charge pump voltage applied to the first voltage reference input.

27. The memory device of claim 21 further comprising a charge pump generating a charge pump voltage at a charge pump voltage terminal having a magnitude that is greater than the magnitude of a charge pump supply voltage applied to a power supply input of the charge pump, the power supply input of the charge pump being coupled to the second regulated voltage output terminal of the second regulator circuit, and the charge pump voltage terminal being coupled to the memory circuit.

28. The memory device of claim 21 wherein at least one of the first and second regulated voltage output terminals is

coupled to the memory circuit through a charge pump, the charge pump generating a charge pump voltage at a charge pump voltage terminal, the power supply input of the charge pump being coupled to the at least one of the first and second regulated voltage output terminals of the first and second regulator circuits, respectively, and the charge pump voltage terminal being coupled to the memory circuit.

29. The memory device of claim 21 wherein the power control circuit is coupled to the charge pump voltage terminal of the charge pump, and wherein the power control circuit further inhibits generating the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value unless the magnitude of the charge pump voltage is within a predetermined range.

30. The memory device of claim 21 wherein the power control circuit generates the power control signal responsive to the magnitude of the second regulated voltage exceeding a predetermined value.

31. The memory device of claim 21 wherein the first regulator circuit, the second regulator circuit, and the power control circuit are fabricated on the same substrate as the memory circuit.

32. The memory device of claim 21 wherein the first regulator circuit comprises:

a differential amplifier having an output coupled to the first regulated voltage output terminal and a pair of inputs coupled to the first regulated voltage output terminal and a fixed reference voltage, respectively; and

a current limiting circuit coupled to the power control circuit, the current limiting circuit controlling the current supplied to the differential amplifier responsive to the magnitude of the power control signal.

33. The memory device of claim 21 wherein the memory circuit comprises a dynamic random access memory circuit.

34. A method of supplying a regulated voltage to an integrated circuit, comprising:

supplying a first regulated voltage to the integrated circuit, the power supplied to the integrated circuit by the first regulator being controllable;

supplying a second regulated voltage to the integrated circuit;

examining the magnitude of the second regulated voltage; and

reducing the power supplied to the integrated circuit by the first regulated voltage responsive to the magnitude of the second regulated voltage being within a predetermined range of values.

35. The method of claim 34 wherein the steps of supplying first and second regulated voltages to the integrated circuit comprise supplying the first and second regulated voltages to a common node of the integrated circuit.

36. The method of claim 34 further comprising:

coupling the first and second regulated voltages to a power input of a charge pump;

using the charge pump to generate a charge pump voltage having a magnitude that is greater than the magnitude of the voltage coupled to the power input of the charge pump; and

coupling the charge pump voltage to the integrated circuit.

37. The method of claim 36 further comprising:

examining the magnitude of the charge pump voltage; and maintaining the power supplied to the integrated circuit by the first regulated voltage at a reduced level unless the magnitude of the charge pump voltage is within a predetermined range.

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38. The method of claim 34 wherein the step of reducing the power supplied to the integrated circuit by the first regulated voltage responsive to the magnitude of the second regulated voltage being within a predetermined range of values comprises reducing the power supplied to the inte-

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grated circuit by the first regulated voltage responsive to the magnitude of the second regulated voltage exceeding a predetermined value.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,757,170  
DATED : May 26, 1998  
INVENTOR(S) : Pinney

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

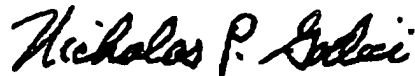
Column 5, line 16

"by as primary"

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Signed and Sealed this  
Twenty-ninth Day of May, 2001

Attest:



NICHOLAS P. GODICI

Attesting Officer

Acting Director of the United States Patent and Trademark Office



US005786617A

**United States Patent** [19]

Merrill et al.

[11] Patent Number: **5,786,617**[45] Date of Patent: **Jul. 28, 1998****[54] HIGH VOLTAGE CHARGE PUMP USING LOW VOLTAGE TYPE TRANSISTORS**

[75] Inventors: **Richard B. Merrill**, Daly City;  
**Whu-ming Young**, Palo Alto, both of Calif.

[73] Assignee: **National Semiconductor Corporation**,  
 Santa Clara, Calif.

[21] Appl. No.: **556,295**

[22] Filed: **Oct. 5, 1995**

**Related U.S. Application Data**

[63] Continuation of Ser. No. 221,602, Apr. 1, 1994, abandoned.

[51] Int. Cl.<sup>6</sup> ..... **H01L 27/092**

[52] U.S. Cl. .... **257/371; 257/376; 257/396; 257/500**

[58] Field of Search ..... **257/368, 369, 257/371-373, 375, 376, 500, 501**

**[56] References Cited****U.S. PATENT DOCUMENTS**

4,403,395	9/1983	Curran	29/571
4,724,221	2/1988	Jochems	437/26
4,825,275	4/1989	Tomasetti	
4,969,020	11/1990	Matsushita et al.	257/376
5,031,019	7/1991	Kosaka et al.	257/376
5,036,229	7/1991	Tran	307/497
5,047,358	9/1991	Kosiak et al.	257/369
5,060,044	10/1991	Tomasetti	257/375
5,319,604	6/1994	Imondi et al.	365/230.06
5,323,043	6/1994	Kimura et al.	
5,475,335	12/1995	Merrill et al.	327/536

**FOREIGN PATENT DOCUMENTS**

0450797	10/1991	European Pat. Off.
5190783	1/1992	Japan

**OTHER PUBLICATIONS**

Sippl et al *Computer Dictionary and Handbook*, Howard Sams & Co. Inc, Indianapolis, 1980, pp. 473, 603.  
 Fairchild 1987 *Linear Data Book*, pp. 9-40, 9-45.

A. Koroncai, et al., "A 69-V CMOS DC/DC converter for ISDN applications", *IEEE Journal of Solid-State Circuits*, Jun. 1988 vol. 23, No. 3, pp. 824-829. (abstract).

K. Murakami, et al., "Development of a digital input interface IC for automotive electronic control unit", *40th IEEE Vehicular Technology Conference*, May 1990, pp. 124-127. (abstract).

Y. Miyahara, et al., "EIA RS-232C driver/receiver mu PD4711C/GS", *NEC Technical Journal*, Oct. 1987, vol. 40, No. 10, pp. 66-69. (abstract).

John Goldie, et al., "Inter-Operation of the DS14C335 with +5V UARTs", Jan. 1993, *National Semiconductor*.

Y. Okazaki, et al., "Characteristics of a New Isolated p-Well Structure Using Thin Epitaxy Over the Buried Layer and Trench Isolation", *IEEE Trans. on Electron Devices*, vol. 39, No. 12, Dec. 1992.

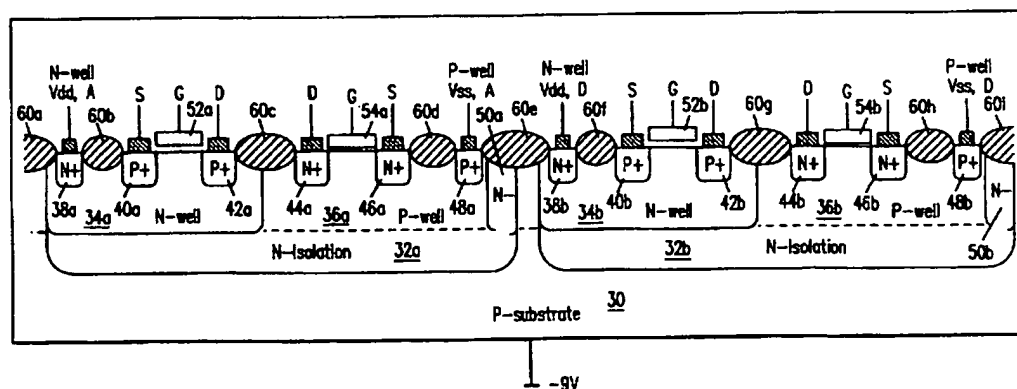
M. Declercq, et al., "TP 10.6: 5V-to-75V CMOS Output Interface Circuits", *IEEE Intl. Solid-State Circuits Conf.*, Feb. 1993, pp. 162-163.

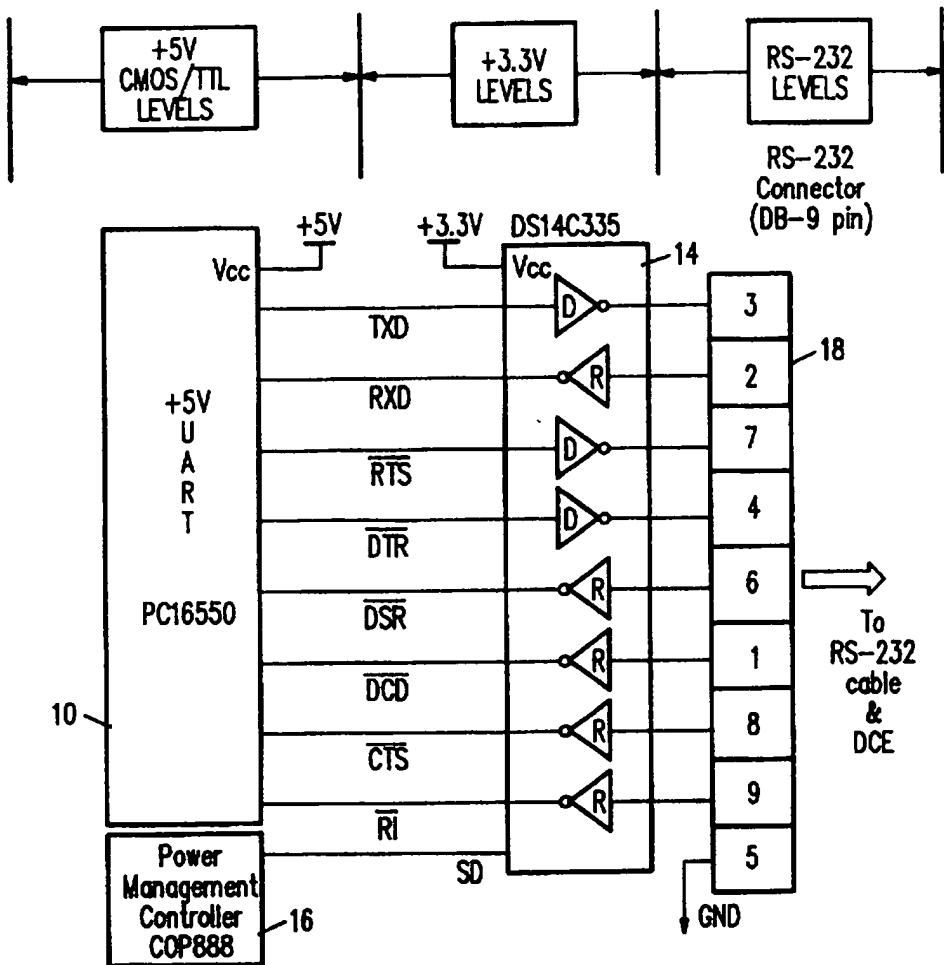
*Primary Examiner*—Gene M. Munson

*Attorney, Agent, or Firm*—Skjerven, Morrill, MacPherson Franklin & Friel; Norman R. Klivans

**[57] ABSTRACT**

An integrated circuit includes an N isolation buried layer underlying high density and low voltage type P channel and N channel transistors to define islands of arbitrary voltage on the substrate. Thus such transistors, which otherwise are capable only of low voltage operation, become capable of operating at high voltage relative to the substrate. This allows integration, on a single chip, of high voltage circuit elements with low voltage and high density transistors all formed by the same fabrication process sequence. In one example this allows creation of an 18 volt range charge pump using a CMOS process which normally provides only 3 volt operating range transistors. This then allows integration on a single integrated circuit chip of a complex digital logic function such as a UART (universal asynchronous receiver and transmitter) with a high voltage function such as an RS-232 interface, including integrated capacitors for the RS-232 interface charge pump.

**6 Claims, 9 Drawing Sheets**



PRIOR ART  
FIG. 1

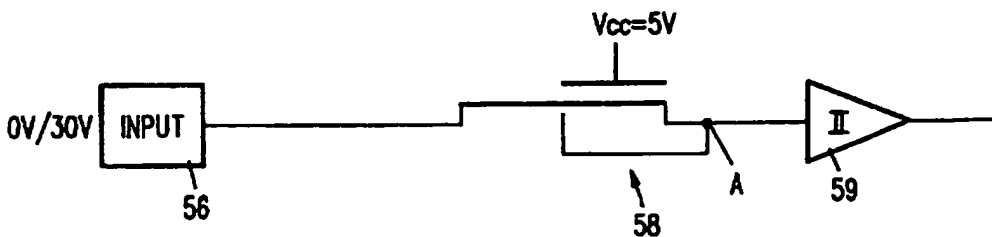


FIG. 3

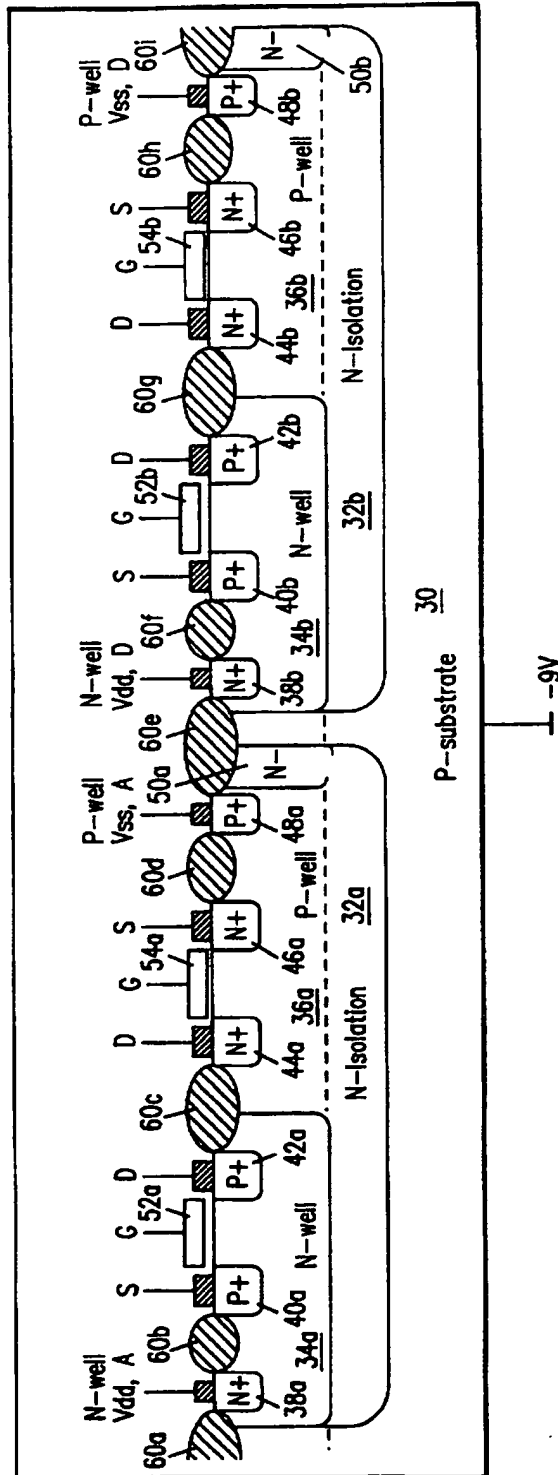


FIG. 2

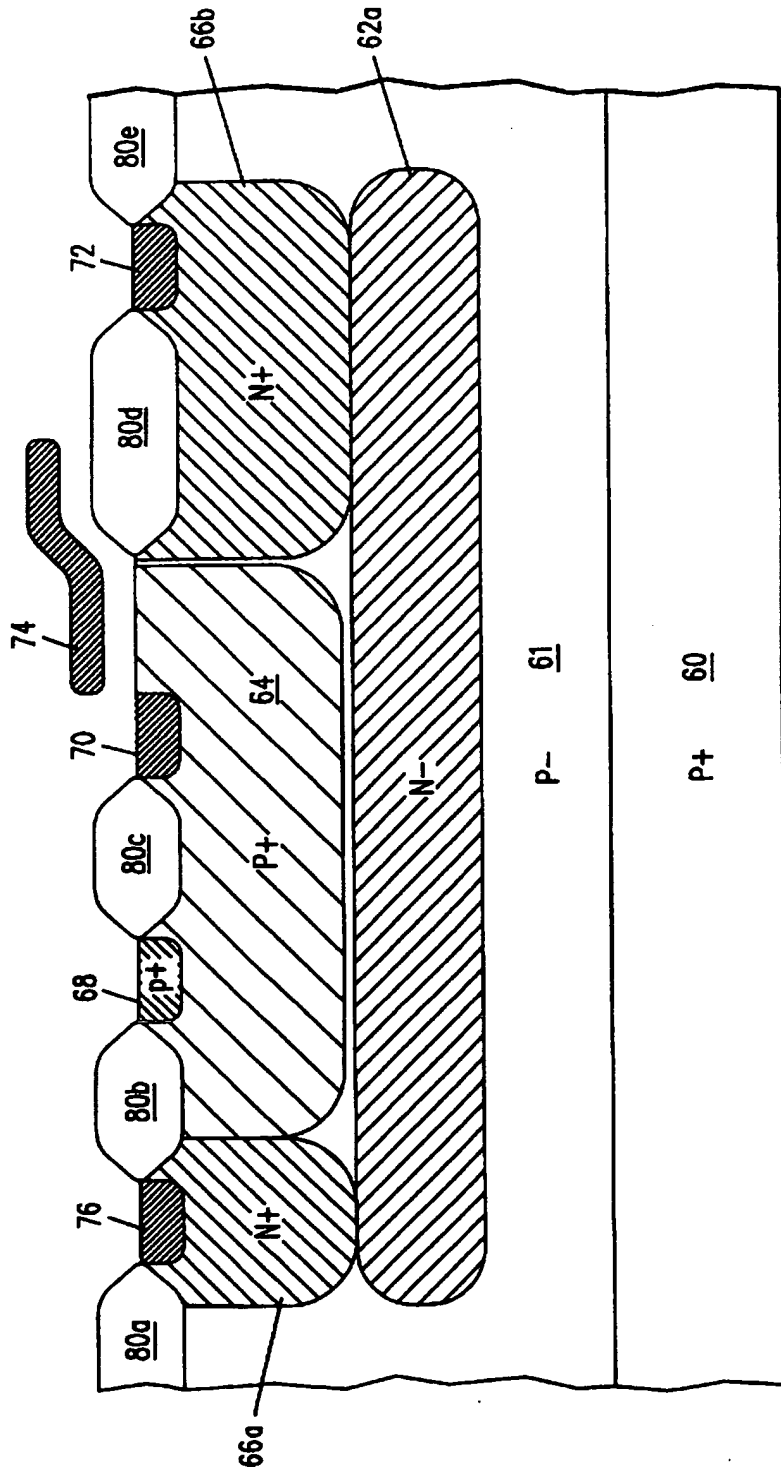


FIG. 4a

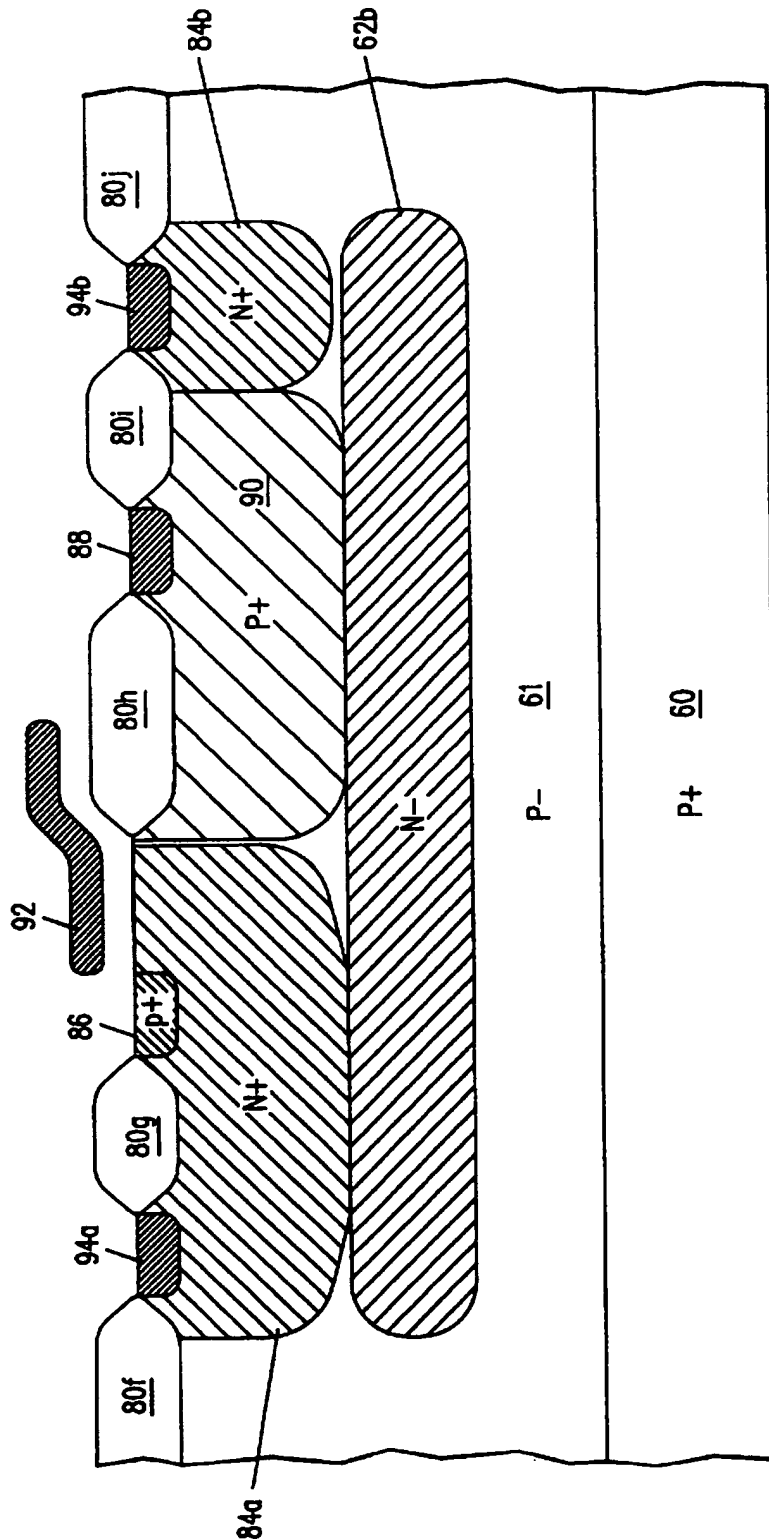
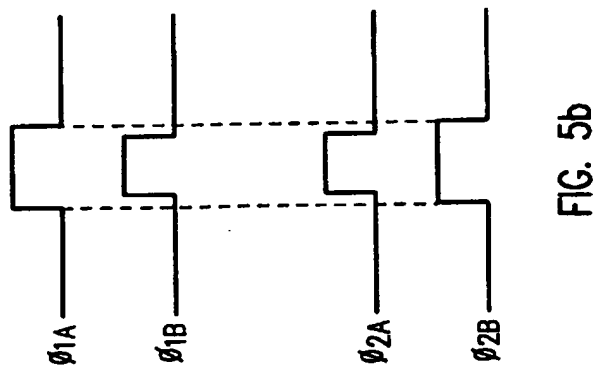
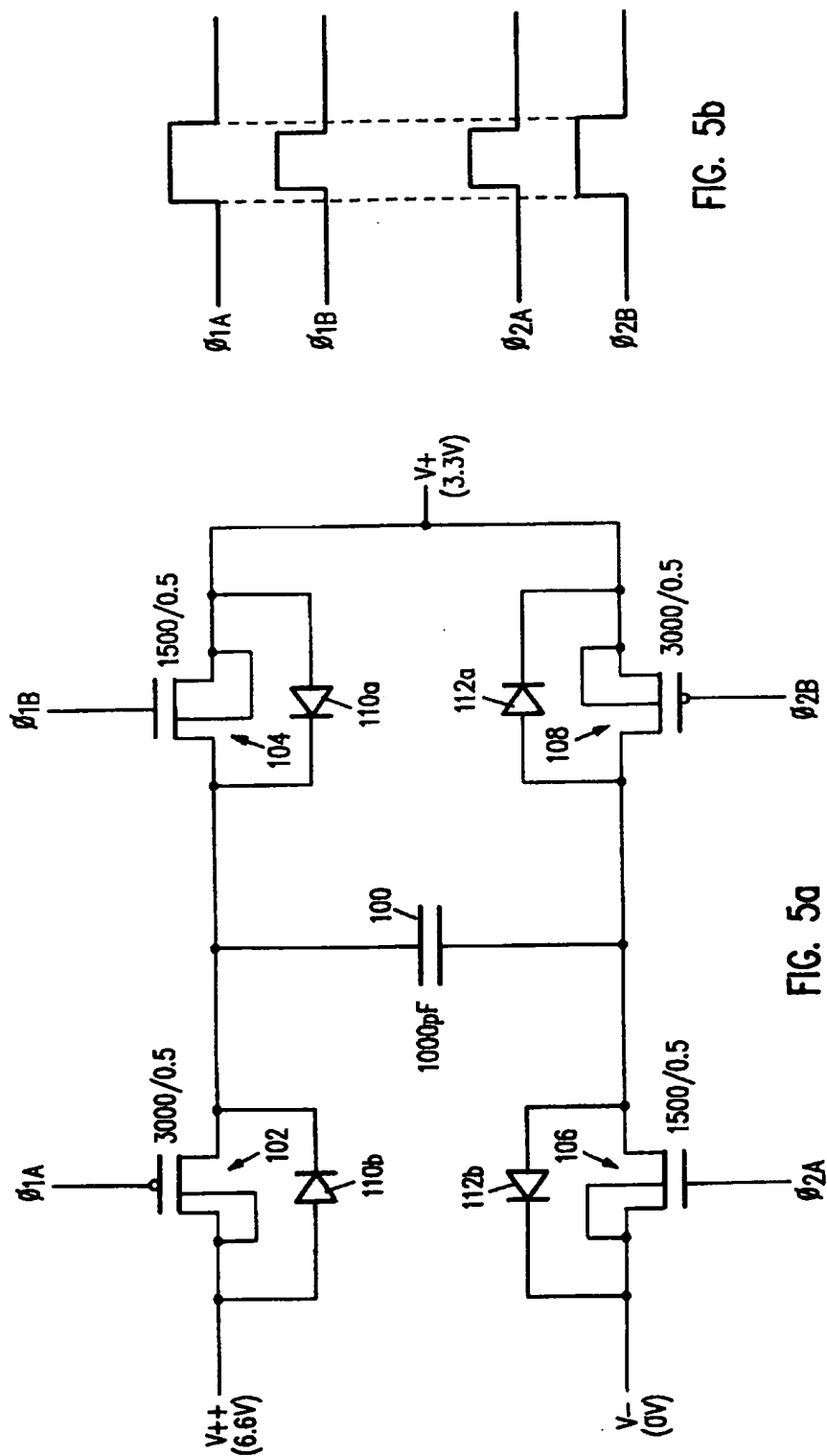
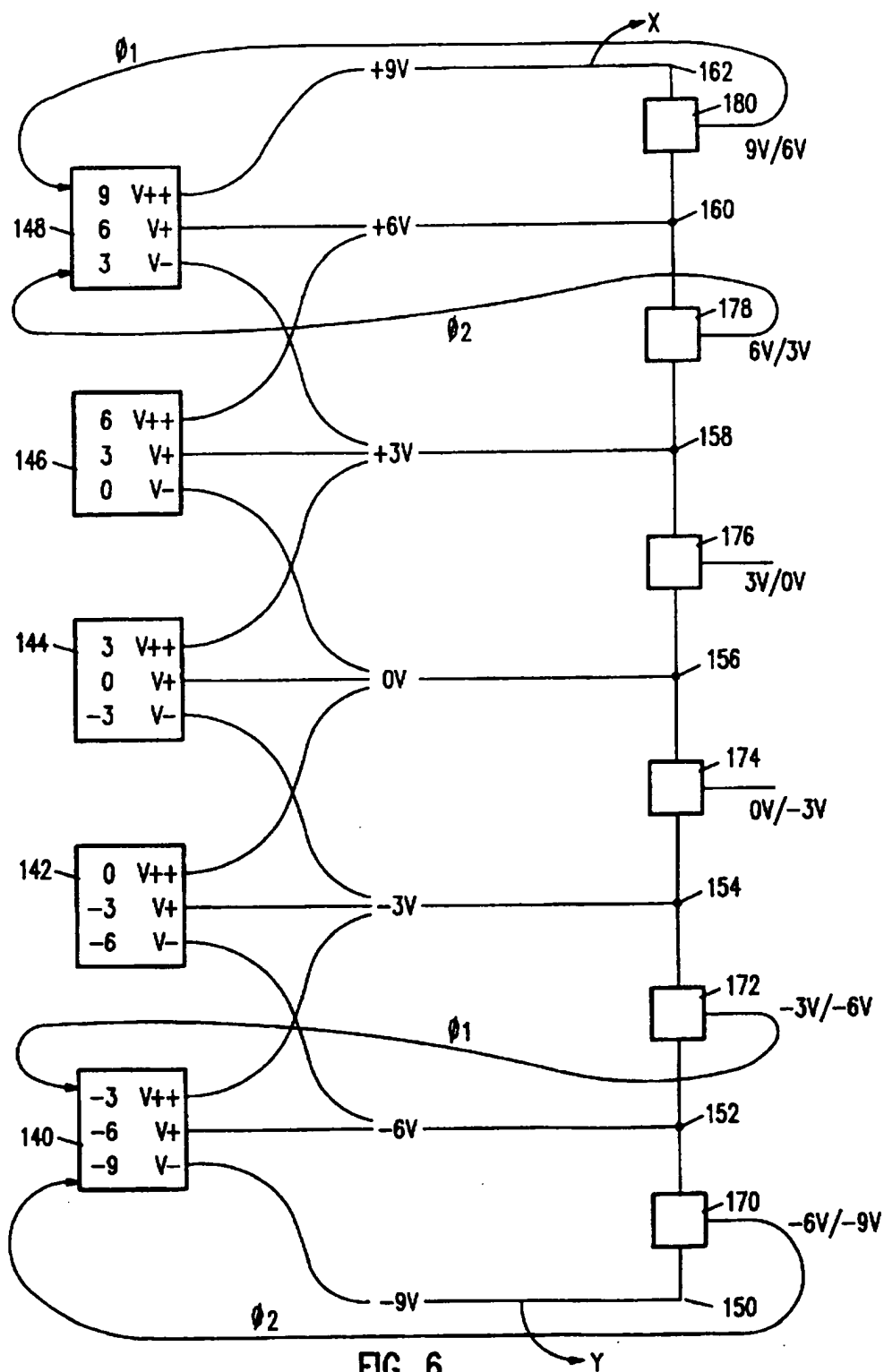


FIG. 4b







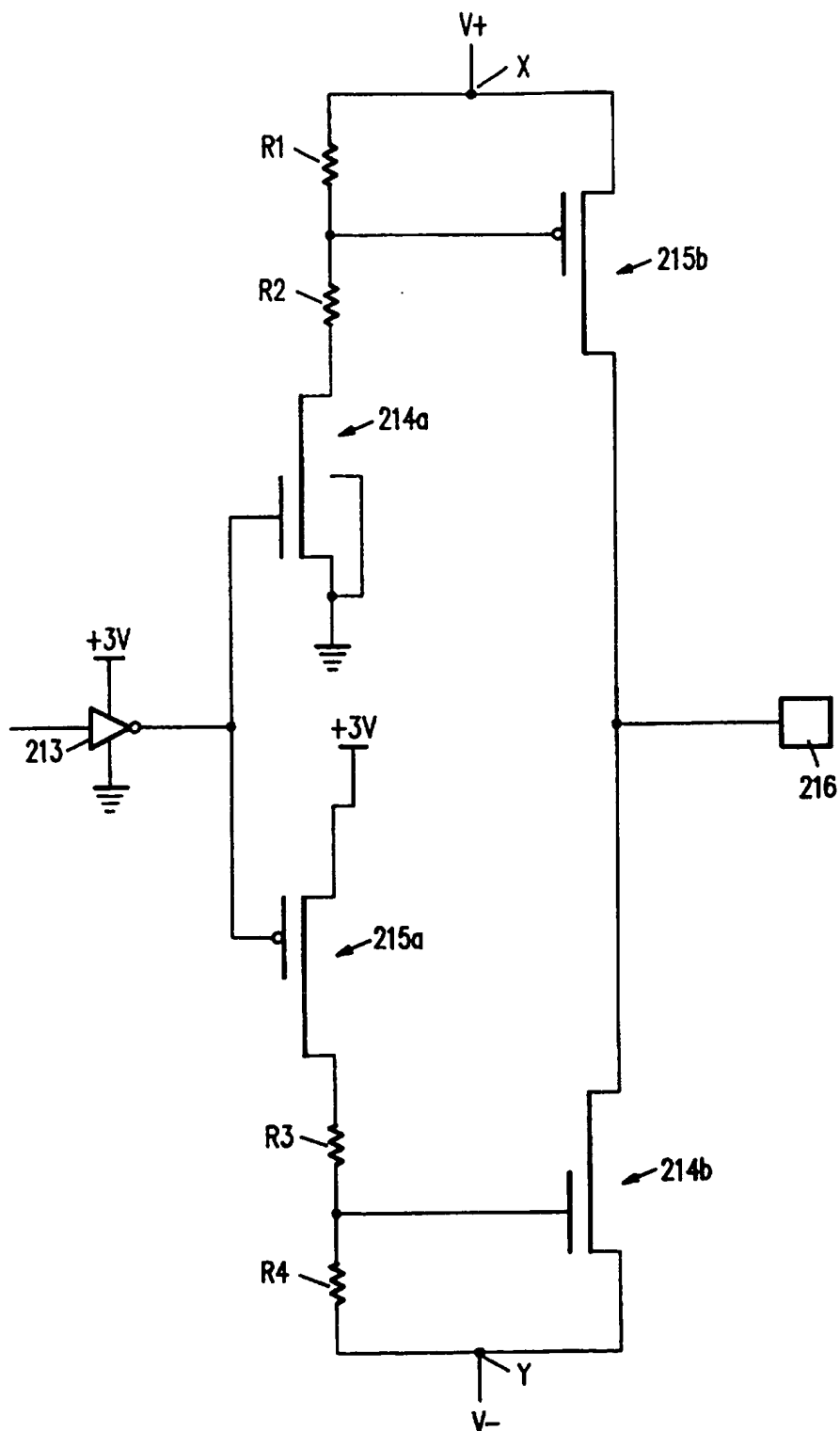


FIG. 7

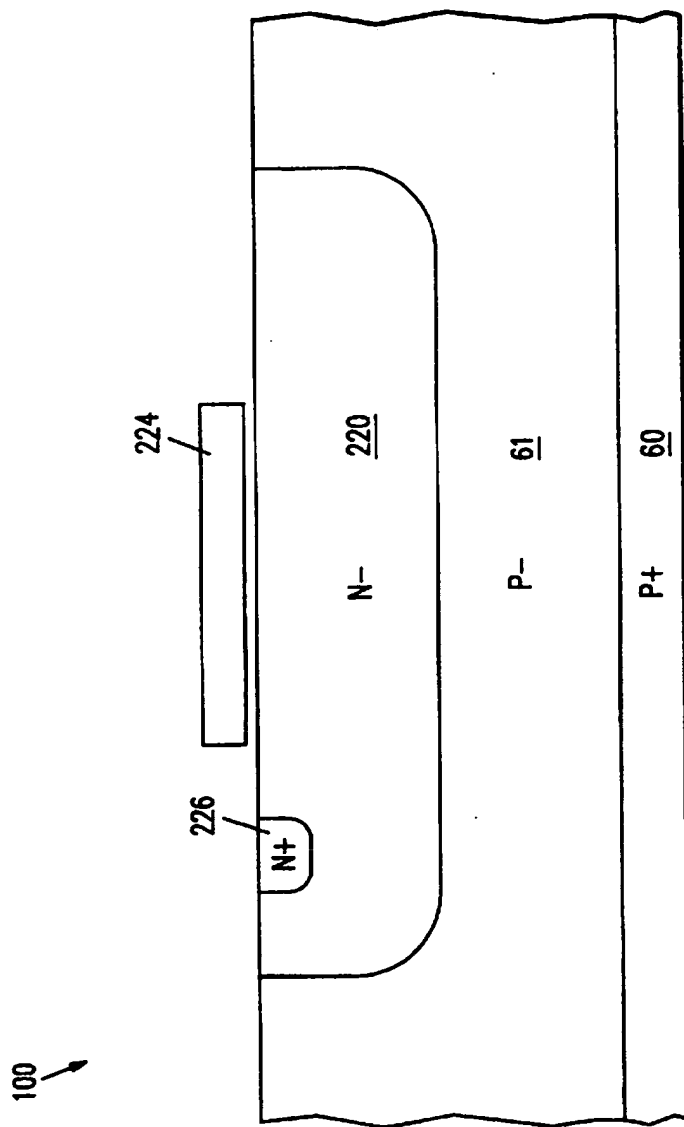


FIG. 8

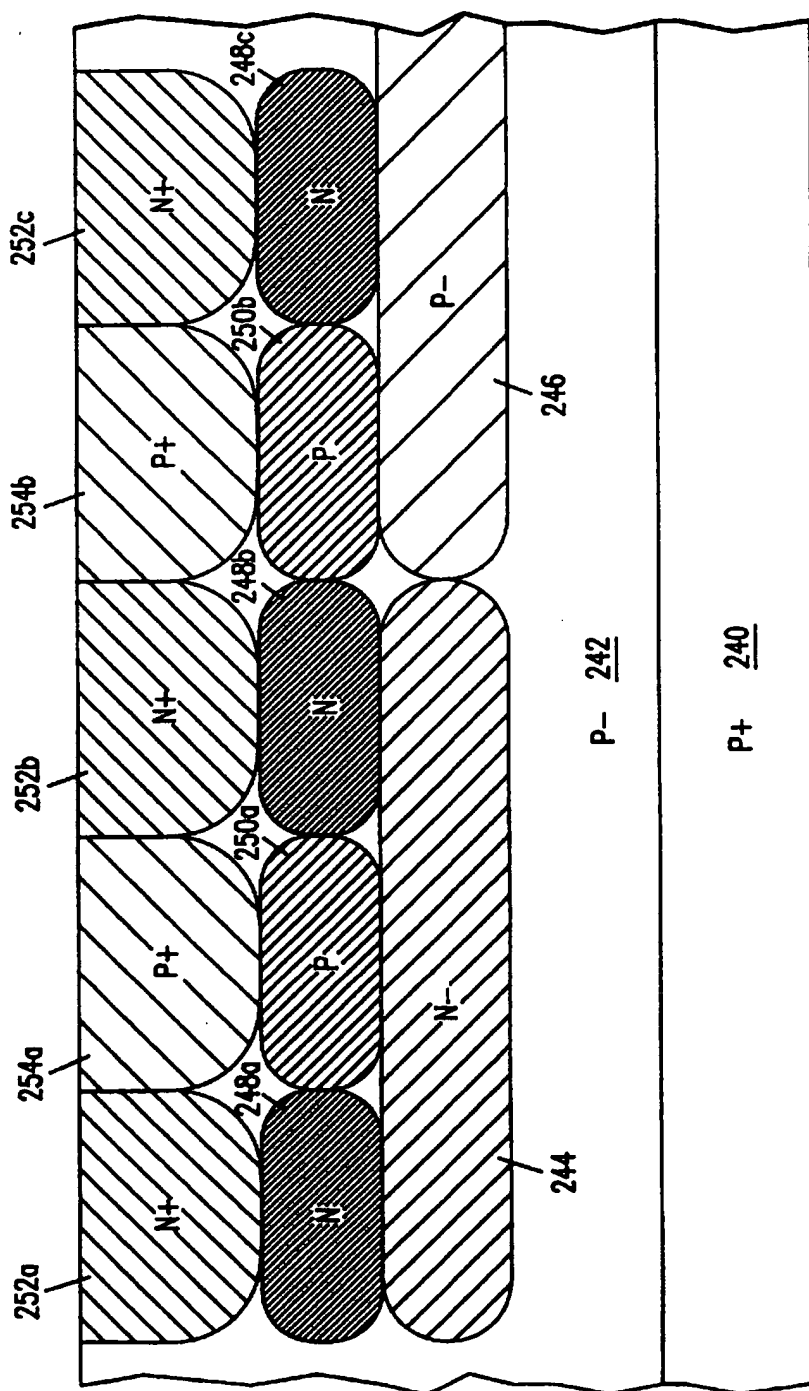


FIG. 9

## HIGH VOLTAGE CHARGE PUMP USING LOW VOLTAGE TYPE TRANSISTORS

This application is a continuation of application Ser. No. 08/221,602, filed Apr. 1, 1994; now abandoned.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

This invention relates to integrated circuits and more specifically to a high voltage charge pump circuit including transistors formed by a low voltage CMOS semiconductor fabrication process.

#### 2. Description of the Prior Art

It is well known in the field of integrated circuits to fabricate field effect transistors capable of operating at a high voltage. Other field effect transistors which are capable of operating at only a low voltage have the advantage of a higher capacitance and current carrying capability per unit area. Typically, such low voltage transistors are also advantageously considerably smaller in terms of surface area (of higher density) and also involve shallower diffusions than do the high voltage transistors; they are thus easier and less expensive to fabricate. Most digital logic semiconductor circuits use such low voltage (i.e., 2 to 5 volts source-to-gate potential) field effect transistors. In contrast, the high voltage field effect transistors typically require thicker gate oxide, deeper diffusions, and greater surface area in order to withstand the higher voltages (typically exceeding 5 volts source-to-gate potential). The processes to fabricate respectively low voltage and high voltage field effect transistors thus differ considerably, and in the prior art such high and low voltage transistors cannot be fabricated using the same series of process steps.

This becomes a significant limitation when one wants to combine in a single integrated circuit both a high voltage circuit and a low voltage circuit. In that case, it is known to provide a high voltage/low voltage interface as described in the publication "5V-to-75V CMOS Output Interface Circuits", Declercq et al., 1993 IEEE International Solid State Circuits Conference, p. 162-163. This publication describes combining low cost, low voltage standard CMOS logic with high voltage CMOS output buffers on the same chip, using a standard unmodified low voltage CMOS processing technology and using level shift techniques to meet the constraints on the gate control signal voltages. Thus the gate-to-source voltage swing of the output devices (which are the high voltage transistors) are within the safe operating limits of the low voltage transistors.

However, it has been found that this solution has several drawbacks. One is that the N channel transistors, typically formed in a P well in the semiconductor substrate, are not effectively isolated electrically from the substrate. Also, problematically for high voltage P channel transistors, there is punch through to the substrate. This is because the N well is relatively shallow beneath the P-field drain region in accordance with the low voltage fabrication technique. This limits the voltage that the P channel transistors can withstand (i.e., to below 30 V).

Therefore, there is a need to combine high density low voltage standard CMOS logic transistors with CMOS transistors operating at high voltage on the same chip and fabricated using a low voltage CMOS technology, without the drawbacks of the technique of the above-referenced publication.

### SUMMARY OF THE INVENTION

In accordance with the invention, an N type buried doped electrical isolation layer is formed in a integrated circuit

substrate, underlying both P channel and N channel low voltage type transistors. This isolation layer creates on the substrate isolated areas of arbitrary voltages, and thereby allows some of the transistors, which are otherwise of a low voltage architecture, to operate at high voltages relative to a potential level of the source region or transistor well or substrate. (It is to be understood that in contrast the gate-to-source potential is process related.) These transistors allow fabrication on a single integrated circuit of a charge pump having a high voltage output, fabricated by what otherwise is a low voltage CMOS type process. Thus this process is compatible with low voltage logic-type CMOS transistors formed on the same chip and in the same sequence of processing steps. In other words, in accordance with the invention isolated power/ground P-channel and N-channel transistor pairs are fabricated which operate at any potential relative to a common substrate.

The combination on a single chip of such a high voltage charge pump with digital logic operating at low voltage allows the combination of a UART (universal asynchronous receiver/transmitter) circuit with a high voltage RS-232 driver circuit on the single chip. This can also eliminate the external capacitors normally required for such a high voltage RS-232 driver circuit, and substitute on-chip capacitors, due to the high operating frequency of the circuit and the thin (high dielectric) gate oxide which advantageously are by-products of the basic CMOS low voltage fabrication process.

This combination of the low voltage UART circuit and the high voltage RS-232 driver circuit on one integrated circuit chip is exemplary of the advantages of the invention, in combining low voltage CMOS logic circuitry with high voltage input/output devices on a single chip using essentially a low voltage fabrication process. Thus advantageously one can take a fine line (fine geometry, i.e. sub-1 micron) CMOS fabrication process and adapt it to a high voltage circuit. The generic application is where high density CMOS logic (low voltage) interfaces to a high voltage circuit. One typical application is for automobile electronics, where a 12 volt circuit is frequently used for carrying data signals as well as power.

The use of the isolation buried layer located below both the N channel transistors and the P channel transistors in the high voltage "islands" provides considerably higher working voltage than in the prior art low voltage CMOS processes.

Also in accordance with the invention, there is a cascaded set of individual charge pump stages in the charge pump, and each stage includes the transistors operating at high voltage as described above. This generates, from a single low voltage source, an incremental set of output voltages with a range considerably greater than that of the input voltage using a switching network. For instance, with a 3 volt input voltage it is possible with 5 charge pump stages to provide a +9 volt/-9 volt range. Each charge pump stage has its own circuits completely isolated by the isolation layer in the semiconductor substrate.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a prior art circuit including a UART chip and an RS-232 driver chip.

FIG. 2 shows a portion of a semiconductor substrate incorporating in accordance with the invention an N-isolation layer under MOS transistors.

FIG. 3 shows use of the transistors of FIGS. 4a and 4b.

FIG. 4a shows an N channel high voltage transistor with the N isolation layer.

FIG. 4b shows a P channel high voltage transistor with the N isolation layer.

FIG. 5a shows a charge pump cell.

FIG. 5b shows timing for the cell of FIG. 5a.

FIG. 6 shows a cascaded charge pump.

FIG. 7 shows a high voltage driver and level shift circuit.

FIG. 8 shows a capacitor structure.

FIG. 9 shows a cross section of a semiconductor structure in accordance with the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 shows a prior art circuit combining (1) a UART chip 10 (e.g. National Semiconductor part number PC16550) which operates as shown, typically at +5 volts CMOS/TTL voltage levels connected to (2) an RS-232 driver/receiver chip 14 (e.g. National Semiconductor part number DS14C335) which operates internally at high voltages. The signal lines between the UART 10 and RS-232 driver 14 are shown, conventionally labeled TXD, RXD, etc. Also included in this circuit is conventional power management controller chip 16 (e.g. National Semiconductor part number COP8888). The functionality and structure of each of these parts is known in the art. In this prior art, the UART 10 and RS-232 driver 14 of necessity are on separate chips. Although the RS-232 driver 14 is shown as operating at +3.3 volts, in fact it requires typically an internal voltage supply of +9 volts to -9 volts to drive the signals to the RS-232 connector 18, which as shown connects to an RS-232 cable and to typically digital communication equipment (DCE) for use e.g. in a computer network.

The driver circuitry in the RS-232 driver 14 provides a translation from the TTL/CMOS voltage levels to the RS-232 driver output voltage levels at 3.3 volts. The receiver portion of chip 14 accepts standard RS-232 input voltage levels and translates them back to TTL/CMOS compatible output voltage levels for input to UART chip 10.

In accordance with the invention, the circuitry of these two chips 10, 14 plus some external components (capacitors) is combined onto a single chip, saving both space and power, making this single chip ideal for use in portable applications such as a notebook computer. The method and structure by which this exemplary combination of transistors operating at high and low voltages is formed on a single chip are disclosed hereinafter.

This combination is achieved using an N type doped isolation buried layer formed in the chip substrate. Such an isolation layer is known for use in low voltage CMOS circuitry. See for instance "Characteristics of a New Isolated P-Well Structure Using Thin Epitaxy Over the Buried Layer and Trench Isolation", Okazaki et al., *IEEE Transactions on Electron Devices*, Vol. 39, No. 12, December 1992, pp. 2758-2764. This publication describes using an N+ buried layer on top of which is grown an N type epitaxial layer in which is formed the active portions of the transistors. In the prior art, such isolation layers typically isolate P wells so as to reduce cross talk, in order to provide general isolation of the P wells on an N well CMOS fabrication process. It is believed that such an isolation layer has not been used in the prior art in the context of fabricating transistors capable of operating at arbitrary voltage levels. That is, the prior art use was for logic-type CMOS transistors, typically operating at 3 volts or less differential between the drain and the source or well or substrate of the transistors, but where isolation from a high voltage portion of the chip was not involved.

FIG. 2 shows in accordance with the invention use of the N isolation buried layer beneath MOS P channel and N channel transistor pairs, in order to create completely isolated circuits. In accordance with the invention this isolation is used for the RS-232 driver/UART interface. As described above, the RS-232 driver requires that -9 volts be switched on chip to +9 volts, meaning that the P- substrate is connected to a negative 9 volt potential. Unacceptable back bias would occur on the UART N channel transistors, resulting in high threshold voltage and performance degradation, without this N-isolation. Also, as described in detail below, multiple  $V_{cc}/V_{ss}$  (power/ground) voltage levels are used to partition the +9 volt/-9 volt supply range into nominally 3 volt increments so that an optimized CMOS fabrication process for 3.3 volt transistors can be used in the charge pump circuitry.

As shown in FIG. 2, N isolation layer 32a, 32b which is a buried layer formed on a P- doped substrate 30, provides isolated power and ground for the various islands (groups) of transistors shown for a portion of the UART. Substrate 30 is biased to -9 volts as shown. The first portion 32a of the N-isolation layer isolates two transistors associated with the UART, one formed in N doped well (tub) 34a and the second formed in P doped well 36a. The first transistor in N well 34a includes P+ doped source region 40a, P+ doped drain region 42a, and conductive gate electrode 52a. The respective contacts are labelled S, D, and G. Also shown is conventional N well contact region 38a which is N+ doped and connected to a low voltage  $V_{dd}$  e.g. 3.3 volts (nominally 3 volts).

A second transistor formed in the P well 36a with reversed conductivity types includes N+ doped drain region 44a, N+ doped source region 46a, gate electrode 54a, P+ doped source region 46a, and P+ doped P well contact region 48a connected to  $V_{ss}$  which is ground (0 volts). Structures 60a, . . . 60i are the conventional field oxide regions; the conventional gate oxide layer is not illustrated, for simplicity.

On the right hand side, an identical set of transistors for the RS-232 driver is shown with corresponding reference numbers but having the "b" suffix. On the right hand side overlying the N isolation layer 32b, the N well contact region 38b is connected to the RS-232 driver voltage  $V_{dd}$  (+9 volts) and the P well contact region 48b is connected to the RS-232 driver voltage  $V_{ss}$  (+6 volts). Thus the left hand side represents the transistors operating at low voltage and the right hand represents the transistors operating at high voltage, as described above. This isolation effect is achieved by the N isolation layers 32a, 32b.

FIGS. 4a and 4b illustrate isolated high voltage transistors differing somewhat from those of FIG. 2. An application of the transistors of FIGS. 4a and 4b is shown in FIG. 3. An input signal of 0 to 30 volts is applied at input node 56 to the source terminal of transistor 58, the gate terminal of which is connected to supply voltage  $V_{cc}$  of 5 volts. Node A charges to  $V_{cc}-V_{TN}$  (where  $V_{TN}$  is the transistor threshold voltage).  $V_{cc}-V_{TN}=5\text{ V}-0.7\text{ V}=4.3\text{ V}$  at node A for the isolated transistors of FIGS. 4a and 4b. In contrast, for a prior art non-isolated transistor, the value of  $V_{cc}-V_{TN}=5\text{ V}-2\text{ V}=3\text{ V}$  at node A. Thus the 4.3 V signal is a better logic "1" ("high") than is the prior art 3 V. The 4.3 V signal in this example is an input signal to Schmitt trigger 59.

FIG. 4a shows how the above described N isolation buried layer and a low voltage CMOS process N well transistor are combined to create a completely isolated N channel transistor capable of operating at arbitrary (e.g.

high) voltages relative to the substrate, and here referred to for convenience as a "high voltage transistor". The transistors of FIGS. 4a and 4b hence illustrate another use of the N isolation layer to create transistors capable of operating at such arbitrary voltages relative to the substrate. This structure as in FIG. 4a includes substrate 60 which is doped P+ and biased in operation to -9 V. Overlying P+ substrate 60 is P- epitaxial layer 61. In the central portion of P- epitaxial layer 61 the N doped isolation ("N-ISO") buried layer 62a is formed. Overlying layer 62a is P- doped well 64 which is laterally isolated by N- doped wells 66a, 66b. Formed on the upper portion of epitaxial layer 61 is P+ doped body region 68, N+ doped source region 70, and N+ doped drain region 72. Overlying the principal surface of the structure is conventional doped polysilicon gate electrode 74, which is isolated by a conventional (low voltage) relatively thin gate oxide layer (not shown). Also formed in N-well 66a is a conventional N-well N+ doped contact region 76. Also shown are field oxide regions 80a, 80b, 80c, 80d and 80e.

The corresponding P channel high voltage transistor shown in FIG. 4b (also formed on substrate 60 and using the same set of process steps as the transistor of FIG. 4a) includes the N-isolation layer 62b used in combination with a P well transistor. This transistor solves a problem with prior art P well transistors, namely the problematic low breakdown voltage between the P+ doped drain region 88 and the P- doped epitaxial layer 61. Also shown are N- doped wells 84a, 84b, P+ doped source region 86, P- doped well 90, gate electrode 92, N+ doped N-well contact regions 94a, 94b, and field oxide regions 80f, 80g, 80h, 80i, and 80j.

FIG. 5a shows a circuit cell (stage) for a charge pump which attains the voltage levels needed for the RS-232 driver circuit described above. This circuit is similar to that of the cascaded charge pump which is in the National Semiconductor RS-232 driver circuit (part number DS14C335), in that initially the bottom plate of pump capacitor 100 is charged up to 3.3 volts while the top plate is at 0 volts. Then the top plate is disconnected and the bottom plate (towards the lower part of the drawing) is charged up an additional 3.3 volts, resulting in a potential of 6.6 volts between the top and bottom plates. Transistors 104 and 106 are N channel transistors, and transistors 102 and 108 are P channel transistors. Transistors 102, 104, 106, 108 act as switches operated respectively by clock signals  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  to connect/disconnect the top and bottom plates of capacitor 100. The size (length by width) of the gate electrode of each transistor is shown (in  $\mu\text{m}$ ) by the numerals adjacent each transistor symbol.

Parasitic Schottky diodes 110a, 110b, 112a, 112b are used for the pump stage startup period, since the clock signals  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  operating to pump the pump stage to the next higher voltage level (and which are respectively pulses varying between 6 volts and 3 volts and 3 volts and 0 volts), are not available until the pump capacitor 100 charges up. Thus transistors 104 and 108 will not be operating as switches during the startup period. During the startup period, the action of Schottky diodes 110a and 112a bypasses the switching action of respective transistors 104 and 108. Similarly, diodes 110b, 112b bypass respective transistors 102, 106. The operation of the charge pump is that the supply voltages  $V_{++}=0$  (at 3.3 volts) and  $V_-$  (0 volts) result in an output voltage  $V_{++}$  of 6.6 volts. The clock signals  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  are provided by an e.g. on-chip oscillator (not shown here and described in more detail below) operating for example at a frequency of approximately 50 MHz and a 50% duty cycle.

Thus advantageously the charge pump stage of FIG. 5a is in effect a self-contained (isolated) entity operating within

its own particular nominal 3 volt pump increment. The transistors 102, 104, 106 and 108, being of the low voltage type are advantageously fabricated using a fine line i.e. 0.5 micron ( $\mu\text{m}$ ) process, thus being relatively small in size and hence economical of chip surface area. This is in contrast to the prior art high voltage charge pump transistors in the RS-232 driver chip of FIG. 1 which are typically of the size 10,000  $\mu\text{m}$  by 4  $\mu\text{m}$ .

The charge pump cell of FIG. 5 operates in two phases. with the clock signals  $\phi_{1A}$ ,  $\phi_{1B}$  operating from 3 volts to 6 volts and the clock signals  $\phi_{2A}$ ,  $\phi_{2B}$  operating from 0 volts to 3 volts. In the first phase clock signals,  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  are high so that transistor 104 is on, which means that the upper plate of transistor 100 is connected to node  $V_+$  (3.3 volts). Since clock signals  $\phi_{2A}$ ,  $\phi_{2B}$  are also high, this connects the lower plate of capacitor 100 to node  $V_-$  (0 volts).

In the second phase, clock signals  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  are low. Thus in the second phase transistor 102 is on, connecting the upper plate of capacitor 100 to node  $V_{++}$  and similarly with clock signals  $\phi_{2A}$ ,  $\phi_{2B}$  low, the lower plate of capacitor 100 is connected to node  $V_+$ .

The timing relationships between clock signals  $\phi_{1A}$  and  $\phi_{1B}$ , and between  $\phi_{2A}$ , and  $\phi_{2B}$  are illustrated in FIG. 5b, with the horizontal axis being time, and the vertical axis being signal amplitude.

In the charge pump cell of FIG. 5a, the value of capacitor 100 is determined as being a capacitance equal to the current divided by the change of voltage with respect to time. In this example the current (a function of the clock speed and capacitor 100 value) is a useful level of 10 milliamps, and the change in voltage is 0.2 volts per 20 nanoseconds (corresponding to 50 MHz clock frequency). Thus the capacitance is 1,000 pF. To determine the size of a semiconductor capacitor structure providing this capacity, given a capacitance of gate oxide of 3.1 pF per  $\mu\text{m}^2$ , one requires  $3 \times 10^2 \mu\text{m}^2$  (465 square mils) to provide the required 1000 pF.

FIG. 6 shows an embodiment of a cascaded charge pump, in this case using five charge pump stages 140, . . . . 148. Each charge pump stage has the three output terminals as in FIG. 5a, again labeled  $V_-$ ,  $V_+$  and  $V_{++}$ . In this example each stage provides a nominal 3 volt charge pump increment (understood to actually be, as in FIG. 5a, the 3.3 volt increment provided by the CMOS transistors of the type shown in FIG. 2). It is to be understood that the number of stages is dependent on the output voltage to be achieved, and charge pump stages can readily be added, up to the breakdown voltage of the isolation regions (i.e.,  $\pm 20$  V relative to the substrate). Thus for FIG. 6 the output voltage range is nominally from -9 volts at node 150 (also designated node "Y") to +9 volts at node 162 (also designated node "X"), with intermediate nominal voltages of -6 volts, -3 volts, 0 volts, +3 volts and +6 volts respectively at nodes 152, 154, 156, 158, and 160. In this case it is desired to provide output voltages of other than the maximum and minimum. Thus a switching network shown here as a set of logic selector elements (each having a switching function) 170, 172, 174, 176, 178 and 180 is provided to switch between each pair of voltages, i.e. logic element 180 switches between nominal output voltage 9 volts at node 162 and a nominal 6 volts at node 160.

As shown (only partly for simplicity), the output signal of logic element 180 is fed back as the  $\phi_1$  (actually  $\phi_{1A}$ ,  $\phi_{1B}$ ) clock signal in order to drive the pump stage 148, while the output signal of logic element 178 is fed back as the  $\phi_2$



(actually  $\phi_{2A}$ ,  $\phi_{2B}$ ) clock signal to also drive pump stage 148. Thus each logic element 170, . . . , 180 includes appropriate internal logic such as a set of ring oscillators and associated flip-flops to provide the non-overlapped clock signals  $\phi_{1A}$ ,  $\phi_{1B}$ ,  $\phi_{2A}$ ,  $\phi_{2B}$  of FIG. 5b. (The remaining feedback clock signals are omitted from FIG. 6 for simplicity.)

Thus the circuit of FIG. 6 provides a supply of nominally +9 volts to -9 volts, partitioned into (in this case) nominal 3 volt increments. Each of the supply voltage/ground voltage combinations of transistors described above, separated by the nominal 3 volt increments, has its own circuits completely isolated by the isolation layer of FIG. 2.

FIG. 7 is an example of combined high voltage output and level shifter circuitry using voltages supplied by the charge pump circuitry and using the high voltage transistors in accordance with the invention. A signal to be output is provided to conventional buffer 213, the output of which is connected to the gate of each of high voltage N-channel transistor 214a and P-channel transistors 215a, both of the type illustrated in FIG. 2. Transistors 214a, 214b in combination with resistors R1, R2, R3, R4 are the level shifter. Additionally, high voltage P-channel transistor 215b and N-channel transistor 214b, also of the type shown in FIG. 2, provide the high voltage output to node 216. The high voltage (V+) node X corresponds to node X (ref. no. 162) in FIG. 6; the low voltage (V-) node Y corresponds to node Y (ref. no. 150) in FIG. 6.

A polysilicon/N-doped region structure for capacitor 100 of FIG. 5a is shown in cross section in FIG. 8. Formed in P-doped epitaxial layer 61 on substrate 60 is an N-doped well 220 over which is formed (with an intermediate gate oxide layer, not shown), a polysilicon doped conductive electrode 224 to which is connected one lead of the capacitor, with the second lead being connected to the N+ doped region 226.

It is to be appreciated that in the charge pump of FIG. 5a, capacitor 100 (the semiconductor structure illustrated in FIG. 8) is formed on the same substrate 60 as are the remainder of the circuit elements (i.e., capacitor 100 is an on-chip capacitor). This is in contrast to the prior art where typically external (off-chip) capacitors are needed for such a charge pump to provide the necessary capacitance. However, here it is possible to use an integrated circuit (on chip) capacitor because the circuit, due to its relatively small CMOS feature size, is capable of operating at very high frequency, and also because the thin gate oxide typical of low voltage transistors permits a thin dielectric layer (hence having a high dielectric constant) in the capacitor. Thus using for instance a 100 Å thick gate oxide layer as the dielectric layer in the capacitor and operating the capacitor at 50 MHz substantially increases the available capacitance over that of a prior art integrated circuit capacitor.

A process for forming respectively the transistors of FIGS. 2, 4a, 4b and the capacitor of FIG. 8 is described hereinafter. It is to be understood that this is merely one example of a process for forming these structures, and hence is illustrative and not limiting.

The following steps 1-37 describe the process flow to form the N isolation layer and the associated N and P wells, as well as an intervening separation layers.

1. A conventional silicon wafer substrate which is lightly P doped is provided. A pad oxide layer 250 Å thick is conventionally grown on the principal surface thereof.

2. A pad nitride layer 1150 Å thick is formed on the pad oxide layer.

3. A first N isolation photoresist layer is deposited over the pad nitride layer, and then this photoresist layer is conven-

tionally exposed using a first N isolation layer clear field mask to define the extent of a first N isolation layer.

4. After the exposed photoresist is developed, a nitride etch step etches through the exposed portion of the pad nitride layer, exposing a portion of the pad oxide.

5. A P-type implant is made of boron at a concentration of  $5E12$  at an energy of 90 kV. This implant is to form a P isolation layer (described below in conjunction with FIG. 9) adjacent to the first N- isolation layer and underlying non-isolated portions of the resulting structure.

6. Oxide is selectively grown over the principal surface to a thickness of 2500 Å on part of the surface; on remaining portions of the surface (those not exposed to previous implanting) the oxide grows to a lesser thickness.

7. The remaining portions of the pad nitride layer are conventionally stripped.

8. The first N isolation layer implant is made of arsenic at a concentration of  $2E13$  at an energy of 180 kV.

9. The first N isolation implant is driven in at  $1,000^\circ\text{C}$ . for 20 minutes.

10. A back seal oxide layer is grown conventionally over both the principal surface and backside of the substrate, to a thickness of 2,000 Å.

11. A back seal nitride deposition forms a layer of nitride 1,850 Å thick over both the principal surface and the backside surface of the substrate.

12. The back seal nitride layer on the principal surface is blanket etched.

13. The back seal oxide layer on the principal surface is also blanket etched.

14. A first epitaxial layer is grown to a thickness of 1.5  $\mu\text{m}$  over the principal surface, having a conductivity of 3.5 ohm-centimeter due to arsenic present in the epitaxial layer.

The following steps 15 through 27 essentially replicate previous steps 1-13, except for different dosage and energy levels for the P and N type implants. Steps 15 through 27 form separation layers and step 28 forms a second epitaxial layer on the first epitaxial layer.

15. A second pad oxide layer 250 Å thick is grown over the surface of the first epitaxial layer.

16. A second pad nitride layer 1,150 Å thick is deposited over the second pad oxide layer.

17. A second N masking step using photoresist defines the extent of the N separation layer.

18. The second pad nitride layer is to expose a portion of the second pad oxide layer etch.

19. A second P type implant is made of boron at a concentration of  $2E13$  at 90 kV to form a P separation layer adjacent to the N separation layer.

20. A second layer of oxide is selectively grown to a thickness of 2500 Å over the principal surface as in step 6.

21. The remaining portions of the second pad nitride layer are stripped.

22. A second N layer implant is made of arsenic at a concentration of  $6E15$ , at 75 kV for the N separation layer.

23. The second N layer is driven at  $1000^\circ\text{C}$ . for 20 minutes.

24. A second back seal oxide layer is grown to a thickness of 2,000 Å.

25. A second back seal nitride layer is deposited to a thickness of 1,850 Å.

26. The principal surface nitride layer is blanket etched.

27. The second principal surface oxide layer is blanket etched.

28. A second epitaxial layer is grown over the first epitaxial layer to a thickness of 1.87  $\mu\text{m}$ , and doped with arsenic to a conductivity of 4 ohms-centimeter.

The following subsequent steps form the N and P wells, as shown in FIGS. 2, 4a, and 4b.

29. A twin well pad oxide layer is grown to a thickness of 450 Å over the principal surface.

30. A twin well nitride layer is deposited to a thickness of 1350 Å over the twin well pad oxide.

31. A twin well mask step takes place using a dark field mask to conventionally pattern a photoresist layer to define the extent of the N and P wells.

32. The twin well nitride layer is etched.

33. An N well implant takes place through the etched nitride layer, implanting phosphorous at a concentration of  $7.3\text{E}12$  at 80 kV.

34. Oxide is selectively grown to a thickness of 5.600 Å over the principal surface.

35. The remaining portions of the twin well layer nitride are stripped.

36. A P well implant is made of boron at a concentration of  $3.1\text{E}12$  at 50 kV.

37. A twin well drive-in step drives in the N well and P well implants; this drive-in is such that it also grows a thin oxide layer of 160 Å thickness.

The resulting structure is shown in FIG. 9, differing somewhat from that of FIGS. 2 or 4a, 4b by including the first P doped layer 246 underlying non-isolated portions of the structure. Substrate 240 and first epitaxial layer 242 are conventional. N isolation layer 244 and first P layer 246 underly respectively the isolated and non-isolated portions of the structure. N well 252a is an isolation ring; P well 254a is an isolated P well; N well 252b is an isolated N well; P well 254b and N well 252c are not isolated. N separation layers 248a, 248b, and 248c prevent out-diffusion of underlying dopant into the overlying N wells, while P separation layers 250a, 250b prevent out-diffusion of underlying dopant into the overlying P wells. That is, the P and N doped separation layers provide counter doping.

The remaining steps (not described in detail) are a conventional CMOS process to form the active portions of the transistors. These steps are well known in the art and will be apparent to one of ordinary skill in the art in view of the completed structures of FIGS. 2, 3, 4a, 4b as well as FIG. 8 and hence are not further described.

The above description is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of the above description and are intended to be encompassed within the scope of the appended claims.

We claim:

1. An integrated circuit, comprising:

a semiconductor substrate having a principal surface and doped to have a first conductivity type;

a plurality of transistors formed in the substrate in isolated areas of arbitrary voltages, each transistor comprising:

a source and drain region spaced apart in the substrate and each extending to the principal surface, each doped to have the first conductivity type and each formed in a well region of a second conductivity type;

a gate electrode overlying the principal surface between the source and drain regions; and

an isolation layer doped to have the second conductivity type, formed in the substrate and underlying the source, drain, well region and gate electrode and spaced apart from the source and drain regions and from a backside surface of the substrate;

wherein the well region of a first of the transistors is connected to a supply voltage of +3.3 volts, and the well region of a second of the transistors is connected to a supply voltage of +9 volts, and the substrate is connected to a negative voltage supply.

2. The integrated circuit of claim 1, the well region of each transistor extending from the principal surface towards the isolation layer and laterally surrounding the source region.

3. The integrated circuit of claim 1, the well region of each transistor extending from the principal surface towards the isolation layer and laterally surrounding the drain region and source region.

4. The integrated circuit of claim 3, at least one of the transistors further comprising:

a separation layer doped to have the second conductivity type and extending between the isolation layer and the well region.

5. The integrated circuit of claim 1, further comprising a third transistor formed in the substrate in an isolated area of arbitrary voltage and connected to an intermediate supply voltage of about +6 volts.

6. The integrated circuit of claim 1, wherein the negative supply voltage is about -9 volts.

\* \* \* \* \*



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**United States Patent** [19]  
**Young**

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[45] **Date of Patent:** **Mar. 30, 1999**

[54] **LOW LOSS, REGULATED CHARGE PUMP WITH INTEGRATED FERROELECTRIC CAPACITORS**

[75] **Inventor:** Dennis Young, Colorado Springs, Colo.

[73] **Assignee:** Ramtron International Corporation, Colorado Springs, Colo.

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[22] **Filed:** Jun. 6, 1995

[51] **Int. Cl.<sup>6</sup>** ..... G05F 1/10

[52] **U.S. Cl.** ..... 327/536; 327/537; 327/538

[58] **Field of Search** ..... 327/536, 537, 327/589, 538, 540

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,839,787	6/1989	Kojima et al.	363/60
4,935,644	6/1990	Tsujimoto	307/296.2
5,039,877	8/1991	Chern	307/296.2
5,126,590	6/1992	Chern	307/296.2
5,182,529	1/1993	Chern	331/57
5,422,586	6/1995	Tedrow et al.	327/306
5,546,031	8/1996	Seesink	327/536
5,546,044	8/1996	Calligaro et al.	327/543

**OTHER PUBLICATIONS**

On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique, *IEEE Journal of Solid-State Circuits*, vol. SC-11 No. 3, Jun. 1976, Dickson.

*Primary Examiner*—Timothy P. Callahan

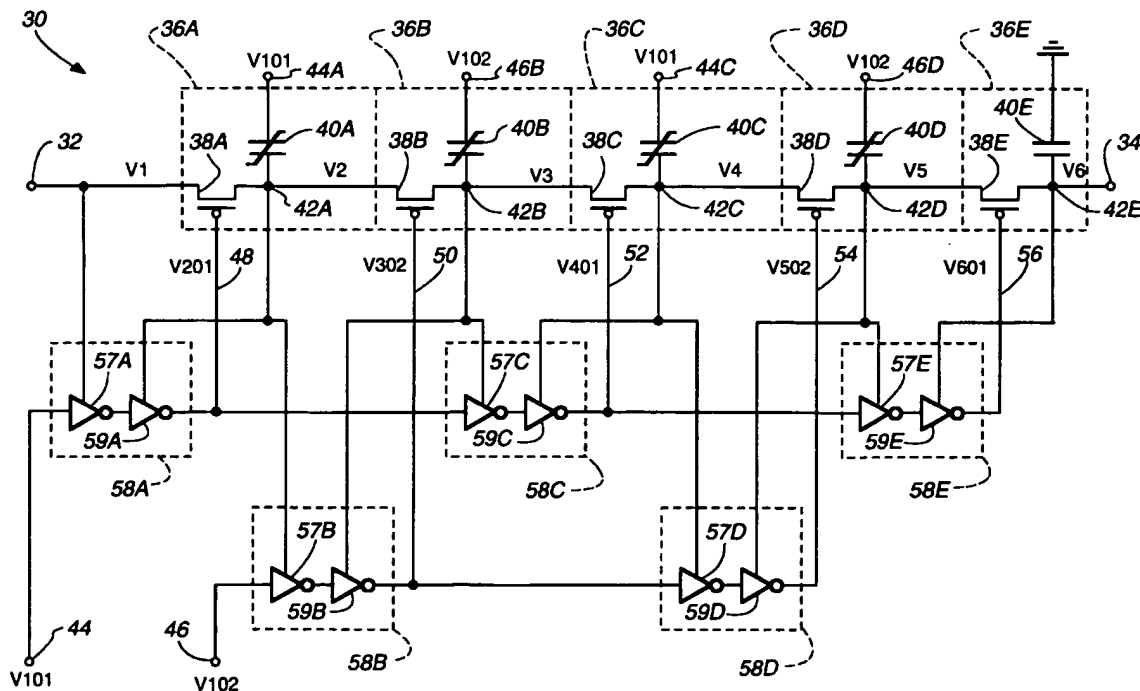
*Assistant Examiner*—Jung Ho Kim

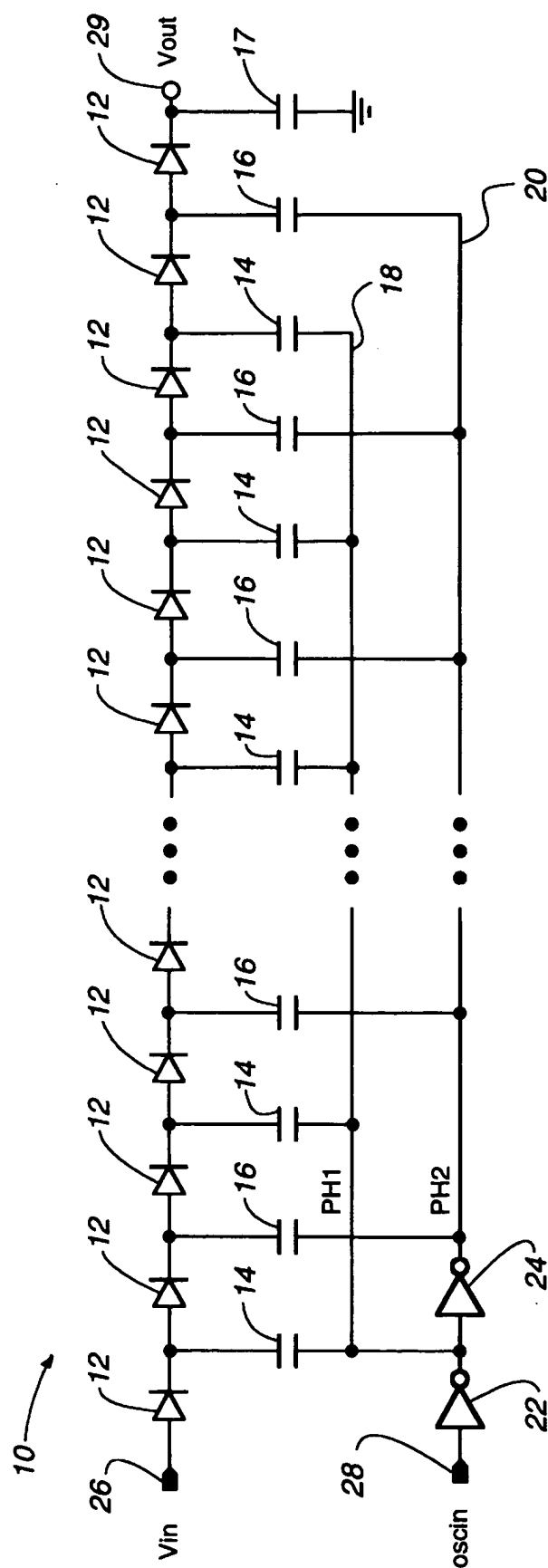
*Attorney, Agent, or Firm*—Peter J. Meza; William J. Kubida; Holland & Hart LLP

[57] **ABSTRACT**

A charge pump for increasing the value of an input voltage includes a plurality of serially coupled charge pump stages, wherein each charge pump stage includes a P-channel pass transistor coupled to a first end of a capacitor. The gates of the P-channel pass transistors and the second ends of the capacitors in odd-numbered charge pump stages receive a first phase clock signal, and the gates of the pass transistors and the second ends of the capacitors in even-numbered charge pump stages receive a second phase clock signal, except that the second end of the capacitor in the last charge pump stage is coupled to ground. To increase the value of the capacitors in an integrated circuit embodiment all of the capacitors, except for the capacitor in the last stage, are ideally ferroelectric capacitors. In a preferred embodiment, the charge pump is one component in a regulated charge pump system that also includes a voltage regulator and a controlled oscillator. In operation, the voltage regulator determines whether the boosted output voltage is greater or less than a predetermined target output voltage and accordingly selectively controls the operation of the oscillator. In turn, the charge pump is enabled to selectively charge pump the input voltage to provide a boosted output voltage if the boosted output voltage is less than a predetermined low target output voltage. Charge pumping is disabled if the boosted output voltage is greater than a predetermined high target output voltage.

**22 Claims, 8 Drawing Sheets**





**Fig. 1**  
**Prior Art**

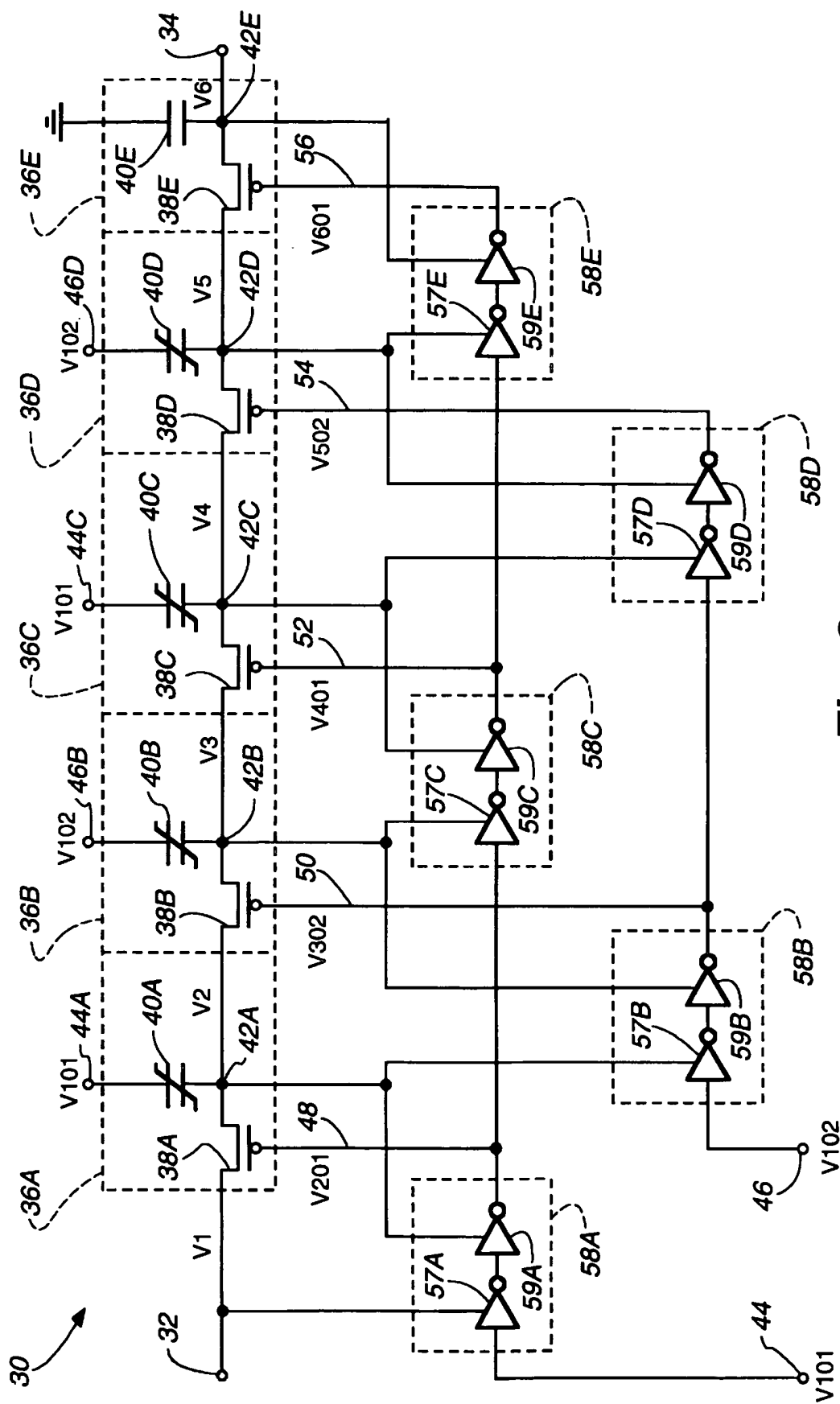
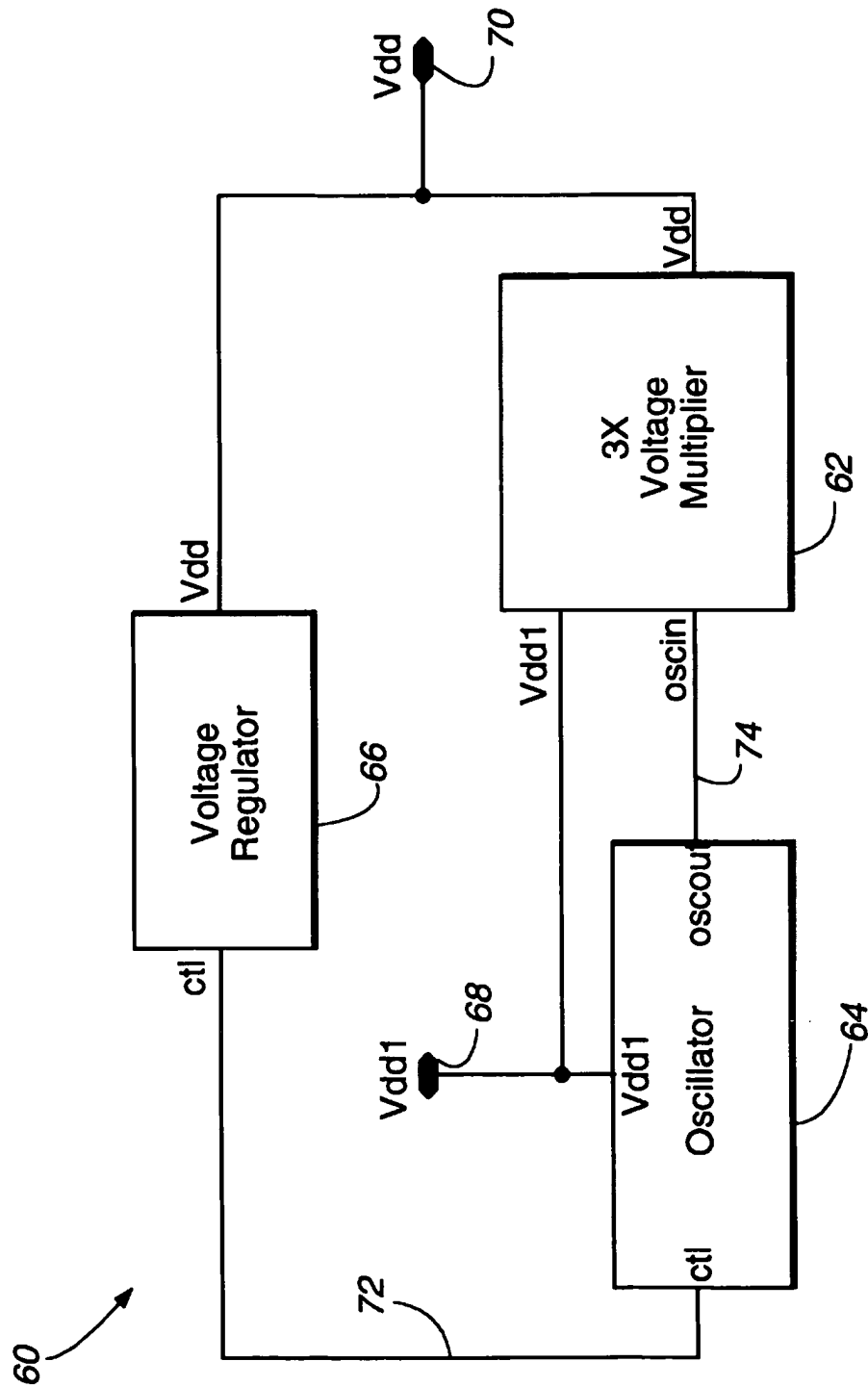


Fig. 2



**Fig. 3**

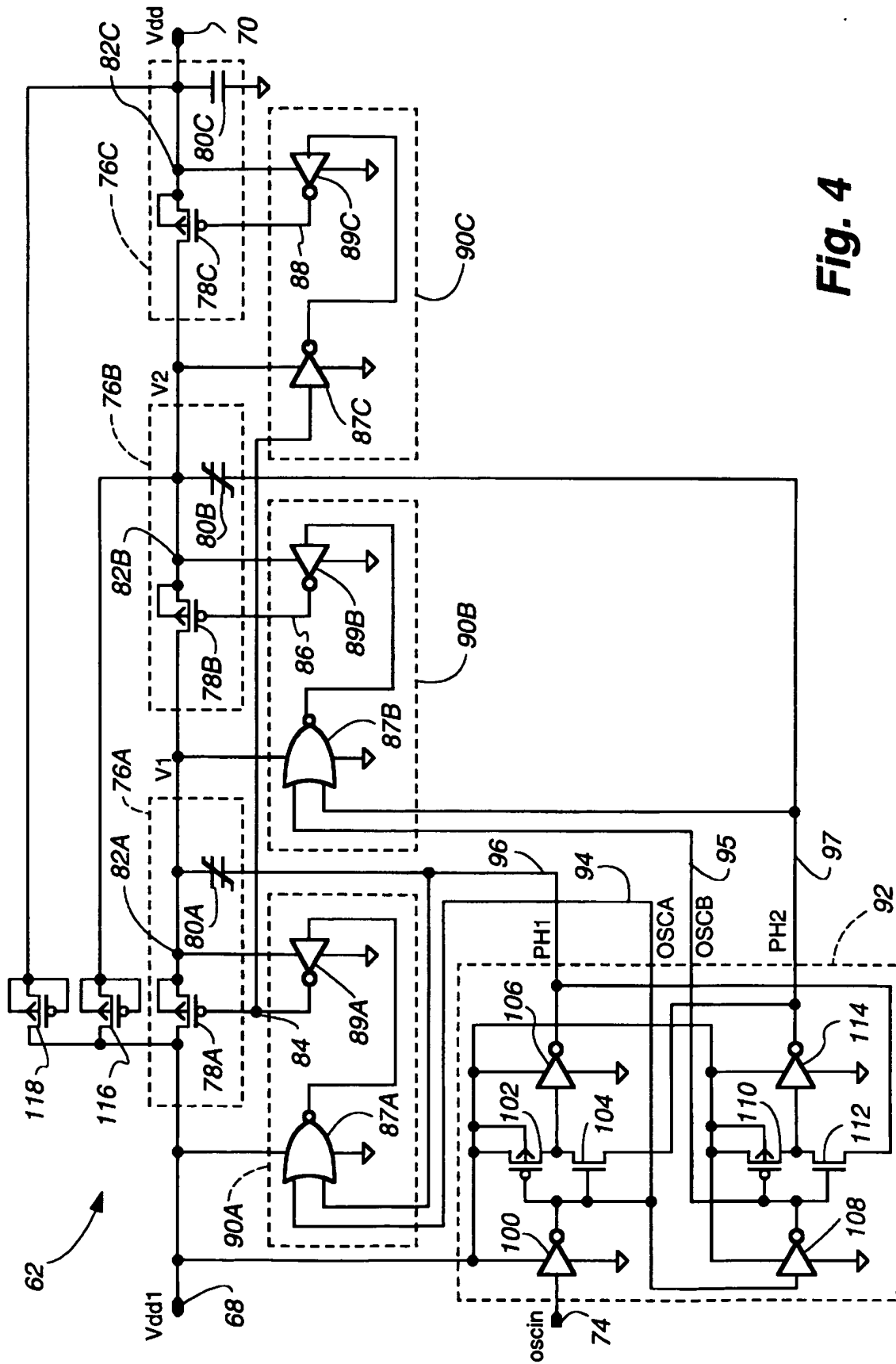
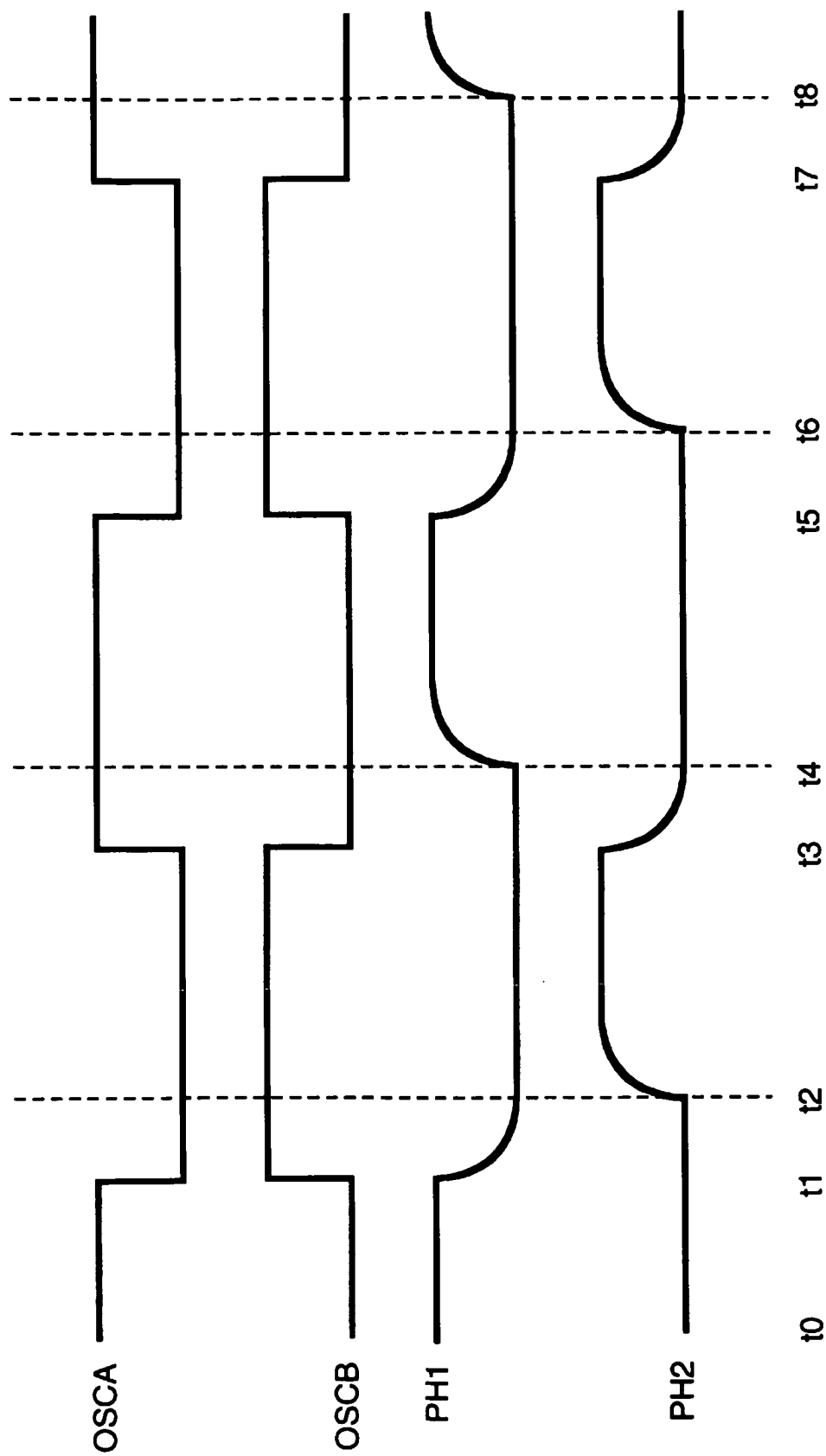


Fig. 4



**Fig. 5**



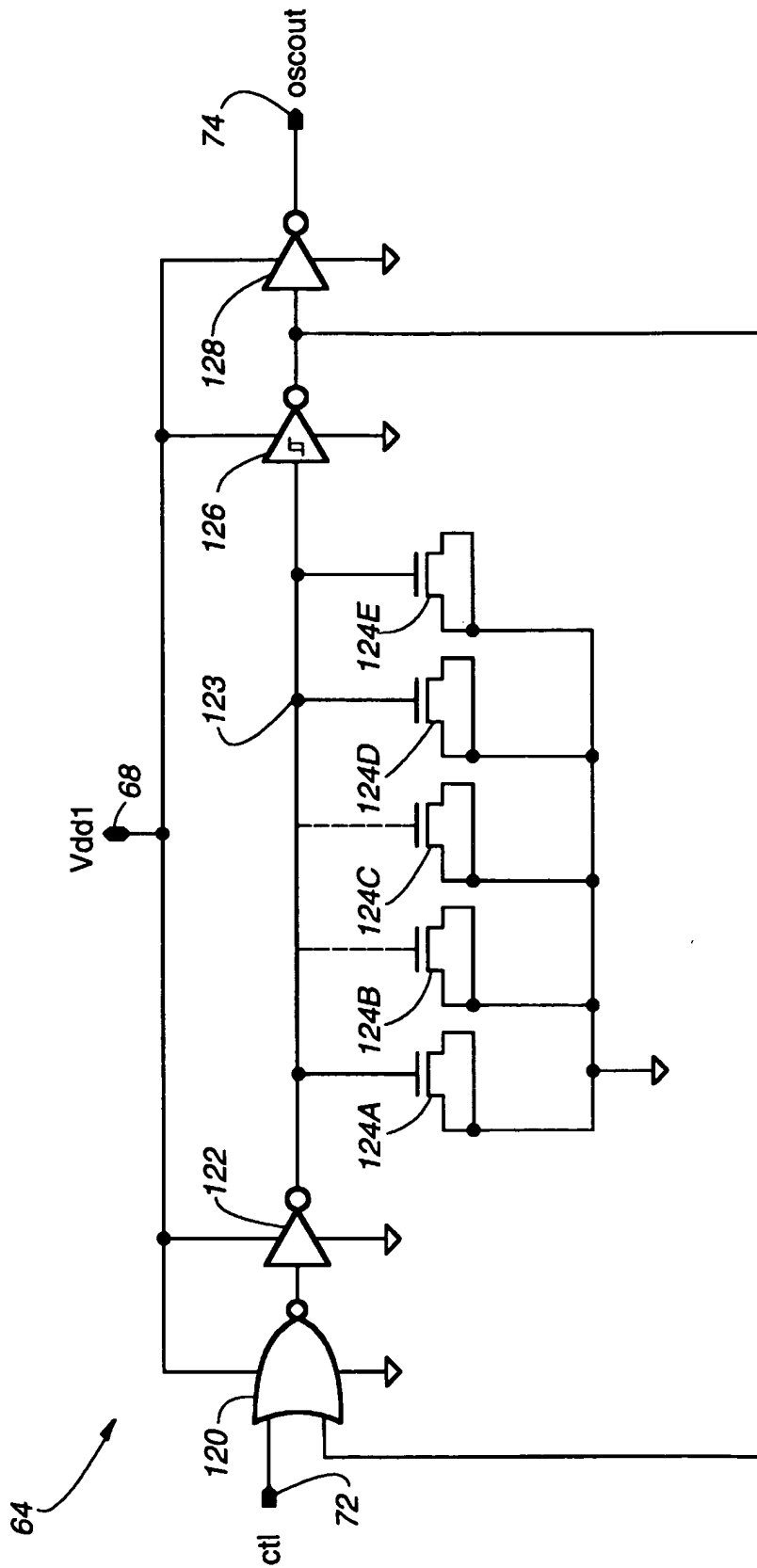


Fig. 6

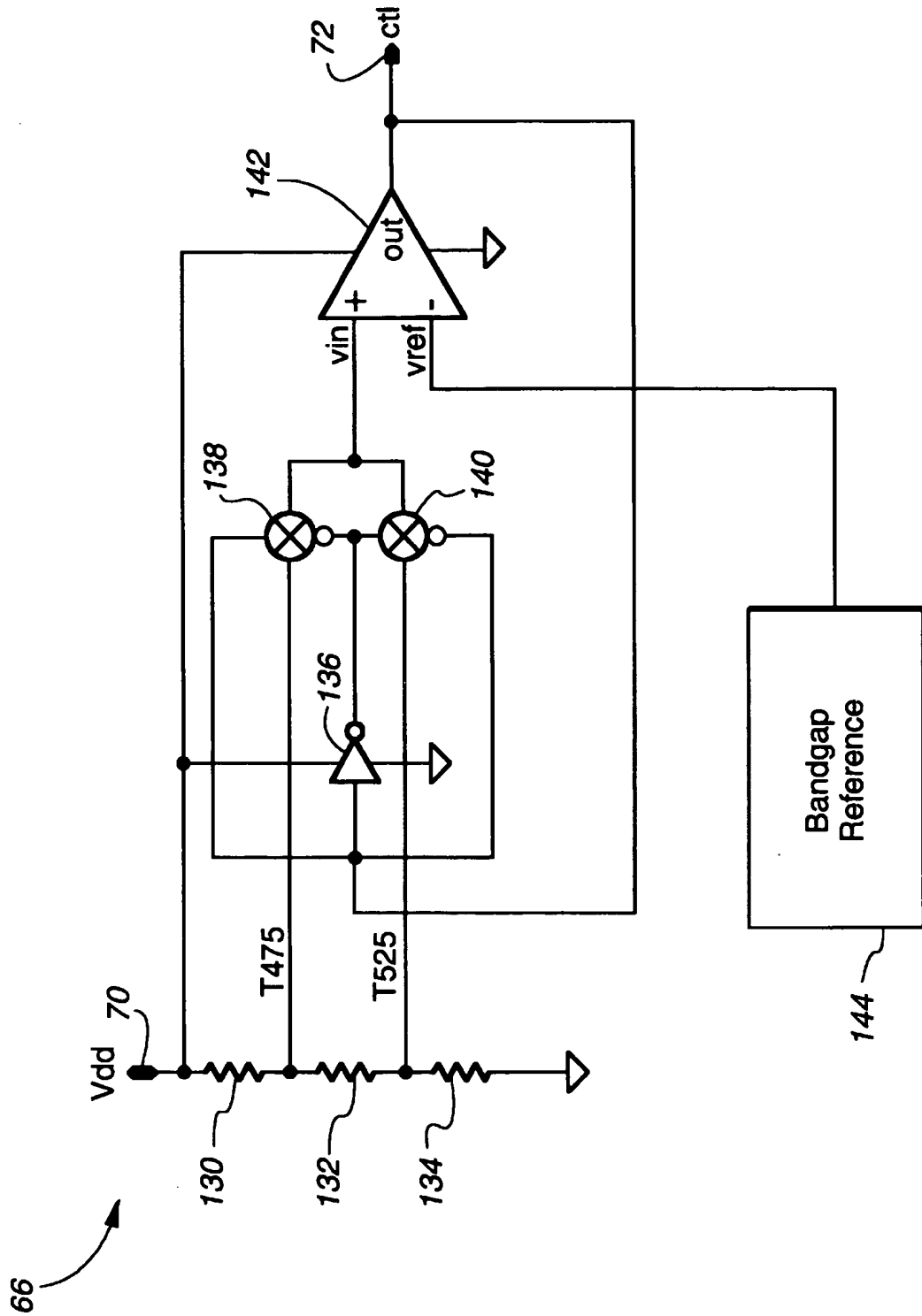


Fig. 7

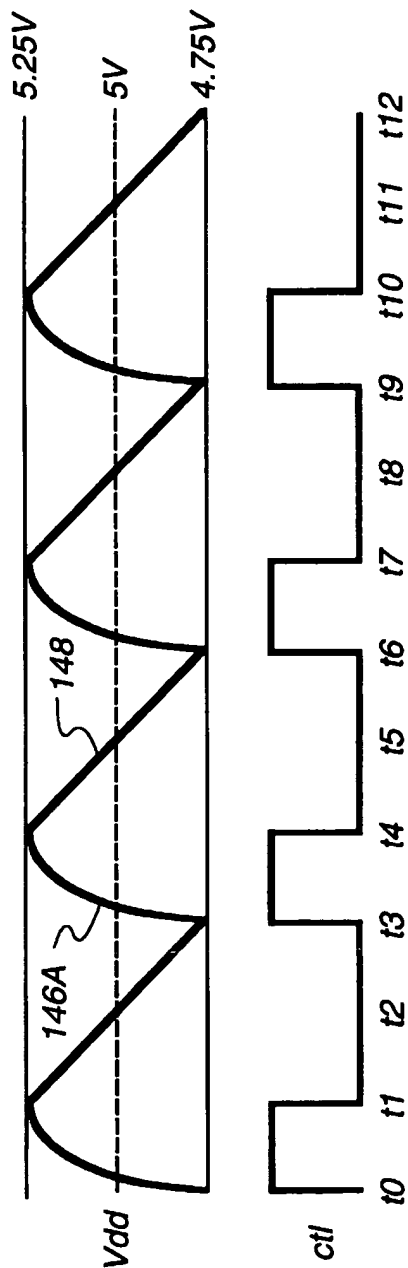


Fig. 8A

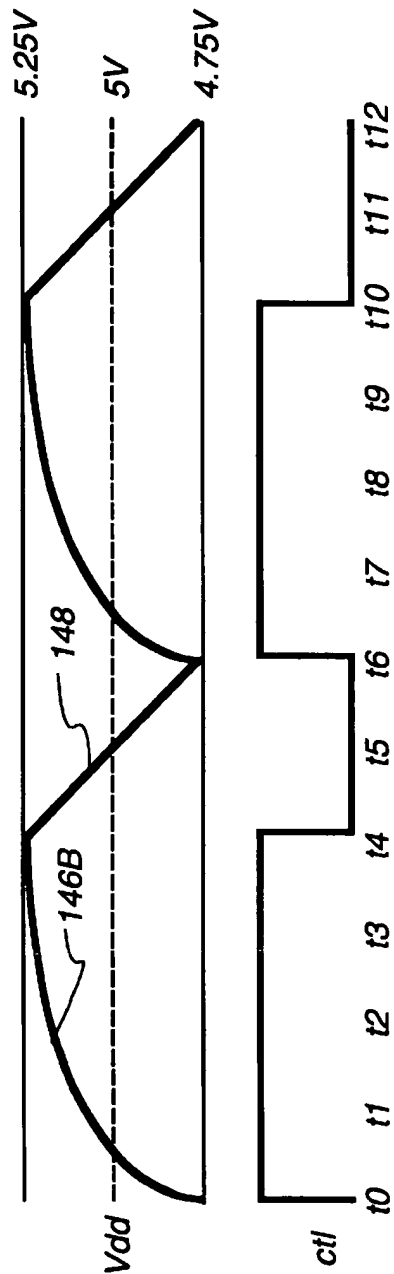


Fig. 8B

# LOW LOSS, REGULATED CHARGE PUMP WITH INTEGRATED FERROELECTRIC CAPACITORS

## BACKGROUND OF THE INVENTION

This invention relates generally to charge pumps. More particularly, the present invention relates to integrated circuit charge pumps having low voltage loss per stage and having a voltage regulated output.

A prior art charge pump 10 is shown in FIG. 1 for "pumping" a low voltage input into a higher voltage output, which can be, and usually is, higher than any external voltage supply available to an integrated circuit containing the charge pump. Charge pump 10 includes a chain of serially-connected diodes 12 in which the cathode of a diode 12 in the chain is coupled to the anode of a next diode 12 in the chain. The anode of a first diode 12 in the chain forms the voltage input,  $V_{in}$ , at node 26, and the cathode of a last diode 12 in the chain forms the voltage output,  $V_{out}$ , at node 29. Output node 29 is terminated with a capacitor 17, which is in turn coupled to ground. The cathodes of odd-numbered diodes 12 are coupled via parallel-connected capacitors 14 to bus 18. Bus 18 provides a first phase clock signal designated PH1. The cathodes of even-numbered diodes 12 are coupled via parallel-connected capacitors 16 to bus 20. Bus 20 provides a second phase clock signal designated PH2, wherein the first and second phase clock signals are 180 degrees out of phase, or "antiphase". The first and second phase clock signals can be provided directly, or through a single oscillator input designated "oscin" at node 28. The two phase clock signals are then provided by the outputs of serially-connected inverters 22 and 24. The combination of a diode 12 with either a capacitor 14 or 16 forms a single charge pump stage.

The two clocks signals PH1 and PH2 have equal peak voltage amplitudes and are capacitively coupled to alternate cathode nodes along the diode chain. Charge pump 10 operates in a manner similar to a bucket-brigade delay line, by pumping packets of charge along the diode chain as the coupling capacitors 14 and 16 are successively charged and discharged during each half of the clock cycle. Unlike the bucket-brigade delay line, however, the voltages in the diode chain are not reset after each pumping cycle so that the average node potentials increase progressively from the input to the output of the diode chain. The output voltage at node 29 will exhibit some ripple determined by the value of output capacitor 17, the voltage magnitude of the clock signals PH1 and PH2, as well as other factors.

While charge pump 10 can be fabricated on an integrated circuit if desired, the output voltage at node 29 is unregulated and is therefore limited to an integer multiple of the input voltage in the typical circuit configuration. The output voltage at node 29 also varies as a function of the input voltage range. Further, since diodes 12 are used in the charge pump stages, the efficiency of the charge pump for low input voltages is compromised since a portion of the voltage increase attained with each charge pump stage is dissipated by the forward voltage drop (" $V_{BE}$ ") of each diode 12. If a large increase in voltage is required, a corresponding large number of charge pump stages are required because of the inherent loss of voltage due to the  $V_{BE}$  loss in each stage. Finally, while charge pump 10 can be technically fabricated on an integrated circuit, the die size is likely to be uneconomically large because of the corresponding large size of typically used integrated silicon dioxide capacitors.

What is desired is an improved integrated circuit charge pump having a regulated output that is efficient and has a

minimum number of charge pump stages to attain the desired output voltage.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to voltage regulate the output of a charge pump to a value not dependent upon an integer multiple of the input voltage, or on the range of the input voltage.

It is another object of the invention to minimize the number of charge pump stages needed and increase the overall efficiency of the charge pump by decreasing the voltage loss in each charge pump stage.

It is another object of the invention to minimize the die size of an integrated circuit charge pump.

It is an advantage of the invention that it is easily fabricated on an integrated circuit, with few or no external devices required.

According to the present invention a charge pump for increasing the value of an input voltage includes a plurality of serially coupled charge pump stages, wherein each charge pump stage includes a P-channel pass transistor coupled to a first end of a capacitor. The gates of the P-channel pass transistors and the second ends of the capacitors in odd-numbered charge pump stages receive a first phase clock signal, and the gates of the pass transistors and the second ends of the capacitors in even-numbered charge pump stages receive a second phase clock signal, except that the second end of the capacitor in the last charge pump stage is coupled to ground. The peak value of the clock signal voltage applied to the gates of the pass transistor in a charge pump stage increases with each successive charge pump stage and is approximately equal to the voltage at the output of the stage. In this manner, the P-channel transistor in each charge pump is completely turned off during alternate charge pump cycles so that accumulated charge is not lost. Additionally, the first and second phase clock signals for driving the capacitors in the charge pump stages are non-overlapping, which also prevents the loss of accumulated charge. The peak value of the clock signal voltage applied to the second ends of each of the capacitors is approximately equal to the voltage on the charge pump input node. To increase the value and minimize the area of the capacitors in an integrated circuit embodiment, all of the capacitors are ideally ferroelectric capacitors. To further reduce die size, the last capacitor can be external to the integrated circuit charge pump.

The charge pump further includes circuitry for providing the P-channel transistor gate voltages. This circuitry includes a first plurality of serially coupled buffer stages associated with odd-numbered charge pump stages, the output of a buffer stage providing the voltage to the gate of the pass transistor in the respective charge pump stage, and the input of a first buffer stage receiving the first phase clock signal voltage. A second plurality of serially coupled buffer stages is associated with even-numbered charge pump stages, the output of a buffer stage providing the voltage to the gate of the pass transistor in the respective charge pump stage, and the input of a first buffer stage receiving the second phase clock signal voltage. Ideally, the buffer stages each comprise a first inverter stage serially coupled to a second inverter stage, wherein the power terminal of the first inverter stage is coupled to the input of the respective charge pump stage, and the power terminal of the second inverter stage is coupled to the output of the respective charge pump stage. Ideally, the charge pump also includes diode circuitry coupled to the input of the first charge pump stage for initializing the output of each of the charge pump stages.

In a preferred embodiment, the charge pump is one component in a regulated charge pump system including a voltage input node and a voltage output node. The input of the charge pump is coupled to the voltage input node, and the output of the charge pump is coupled to the voltage output node. The charge pump further includes an oscillator input for receiving a single oscillator signal which is internally converted into the two anti-phase clock signals. When an oscillator signal is received on this input, charge pumping begins and the output signal is boosted within a few clock cycles. When the oscillator signal is removed, the output voltage of the charge pump gradually decays due to circuit current requirements, circuit loading, and parasitic leakage currents. A voltage regulator has an input coupled to the voltage output node and a control output for providing a signal indicative of whether the charge pump output voltage is above or below a desired output voltage, modified by a preset internal hysteresis range. An oscillator has a power terminal coupled to the voltage input node, a control input coupled to the voltage regulator control output, and an output coupled to the oscillator input of the charge pump. In operation, the voltage regulator determines whether the boosted output voltage is greater or less than a predetermined target output voltage and accordingly selectively controls the operation of the oscillator. In turn, the charge pump is enabled to selectively charge pump the input voltage to provide a boosted output voltage if the boosted output voltage is less than a predetermined low target output voltage. Charge pumping is disabled if the boosted output voltage is greater than a predetermined high target output voltage.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art charge pump circuit;

FIG. 2 is a schematic diagram of a charge pump circuit according to the present invention;

FIG. 3 is a block diagram of a voltage regulated charge pump system according to the present invention including a charge pump, an oscillator, and a voltage regulator;

FIG. 4 is a detailed schematic diagram for the charge pump circuit shown in block diagram form in FIG. 3;

FIG. 5 is a timing diagram associated with certain nodes of the charge pump shown in FIG. 4;

FIG. 6 is a detailed schematic diagram for the oscillator circuit shown in block diagram form in FIG. 3;

FIG. 7 is a detailed schematic diagram for the voltage regulator circuit shown in block diagram form in FIG. 3; and

FIG. 8 is a timing diagram for the charge pump system shown in FIG. 3.

#### DETAILED DESCRIPTION

Referring now to FIG. 2, a charge pump 30 includes a charge pump input node 32 for receiving a low voltage. A charge pump output node 34 supplies a boosted voltage, which can be higher than available power supply voltages. Charge pump 30 includes a plurality of serially coupled charge pump stages 36A through 36E. Although five such stages are shown, any number greater than one can be used in charge pump 30, depending upon the desired output

voltage required at node 34. The input of charge pump stage 36A forms the charge pump input node 32, and the output of charge pump stage 36E forms the charge pump output node 34.

Each charge pump stage 36A-36E includes a pass transistor 38A-38E. The first and second current nodes (source or drain) of transistors 38A-38E respectively form charge pump stage 36A-36E input and output. A capacitor 40A-40E has a first end being coupled to the respective charge pump stage 36A-36E output. The gates of the pass transistors 38A, 38C, and 38E and the second ends of the capacitors 40A and 40C in odd-numbered charge pump stages (charge pump stages 36A, 36C, and 36E in FIG. 2 correspond to odd numbers 1, 3, and 5 in the sequence of serially coupled charge pump stages) receive a first phase clock signal. The gates of pass transistors 38A, 38C, and 38E receive clock signals designated V2Ø1 on conductor 48, V4Ø1 on conductor 52, and V6Ø1 on conductor 56. Although the phase of these signals is the same, the peak voltage is not, as is described in further detail below. The second ends of capacitors 40A and 40C receive a clock signal designated V1Ø1 at respective nodes 44A and 44C. The second end of capacitor 40E, while in an "odd" charge pump stage, is in the final charge pump stage 36E in the sequence and is coupled to ground. Capacitor 40E acts as a final "peak detector" to provide a DC output voltage (with acceptable levels of ripple) at output node 34. The gates of the pass transistors 38B and 36D and the second ends of the capacitors 40B and 40D in even-numbered charge pump stages (charge pump stages 36B and 36D in FIG. 2 correspond to even numbers 2 and 4 in the sequence of serially coupled charge pump stages) receive a second phase clock signal, which is out of phase by 180 degrees from the first clock signal ("antiphase", with approximately a 50% duty cycle). The gates of pass transistors 38B and 38D receive clock signals designated V3Ø2 on conductor 50, and V5Ø2 on conductor 54. Although the phase of these signals is the same, the peak voltage is not, as is described in further detail below. The second ends of capacitors 40B and 40D receive a clock signal designated V1Ø2 at respective nodes 46B and 46D.

The peak value of the clock signal applied to the gates of the pass transistors 38A-38E at conductors 48-56 in charge pump stages 36A-36E increases with each successive charge pump stage, although the phase of the clock signal alternates. The peak value of the voltage applied to the gates of pass transistors 38A-38E is approximately equal to the peak voltage at the output of the corresponding charge pump stage 36A-36E. Having the output node and the gate node at the same voltage potential during one half of the clock signal assures that the pass transistor 38A-38E completely turns off for that portion of the clock signal and no developed charge leaks "backwards" through the chain of charge pump stages 36A-36E.

The peak value of the clock signal applied to the second ends of each of capacitors 40A-40D at nodes 44A-46D is approximately equal, although the phase of the clock signals alternates. The peak value of the clock signal applied to the second ends of each of capacitors 40A-40D is ideally approximately equal to the input voltage on the charge pump input node 32, simply because this is a readily available voltage. Although other voltages can be used, for example one-half of the input node voltage, this will force more complexity in the design because of the need for additional voltage dividers and/or voltage regulator circuits.

To obtain the highest dielectric constant, and therefore the minimum die area needed, capacitors 40A-40D are ideally

integrated circuit ferroelectric capacitors, used in the non-switched linear mode. Capacitor 40E is shown to be a non-ferroelectric external capacitor having sufficient capacitance to reduce ripple at output node 34 to acceptable levels. Capacitor 40E can also be an integrated circuit ferroelectric capacitor, but because of the high value of capacitance typically needed for the peak detect function, an analysis should be done to ascertain whether or not it is economically feasible to include capacitor 40E on the integrated circuit. In charge pump 30, transistors 38A–38E are ideally P-channel MOS transistors. Charge pump 30 can be reconfigured, however, to use N-channel MOS transistors if, for example, a dual-well semiconductor process is used.

Charge pump 30 further includes circuitry for supplying the first and second phase clock signals of varying peak voltages to the gates of pass transistors 38A–38E in the respective charge pump stages 36A–36E from the two input clock signals V1Ø1 at node 44 and V1Ø2 at node 46. The two input clock signals ideally have the same peak voltage, which is the same as the input DC voltage on node 32, i. e. “V1” volts. The two input clock signals are also antiphase, and are non-overlapping. The clock signal generating circuitry includes a first plurality of serially coupled buffer stages 58A, 58C, and 58E associated with odd-numbered charge pump stages 36A, 36C, and 36E. The output of a buffer stage is coupled to the input of a next buffer stage and provides the clock signal to the gate of the pass transistor in the respective charge pump stage. For example, the output of buffer stage 58C is coupled to the input of buffer stage 58E and provides the clock signal to the gate of pass transistor 38C in charge pump stage 36C via conductor 52. The input of the first buffer stage 58A receives the first phase clock signal V1Ø1 at node 44. A second plurality of serially coupled buffer stages 58B and 58D is associated with even-numbered charge pump stages 38B and 38D. The output of buffer stage 58B is coupled to the input of a buffer stage 58D and provides the second phase clock signal V1 to the gate of the pass transistor in the respective charge pump stage, the input of a first buffer stage receiving the second phase voltage.

Each of buffer stages 58A–58E include a first inverter stage 57A–57E serially coupled to a second inverter stage 59A–59E. The power terminal of the first inverter stage 57A–57E is coupled to the input of the respective charge pump stage 36A–36E. For example, the power terminal of inverter 57A is coupled to node 32, which is the input of charge pump stage 36A; the power terminal of inverter 57E is coupled to node 42D, which is the input of charge pump stage 36E. The power terminal of the second inverter stage 59A–59E is coupled to the output of the respective charge pump stage 36A–36E.

For example, the power terminal of inverter 59A is coupled to node 42A, which is the output of charge pump stage 36A; the power 20 terminal of inverter 59E is coupled to node 42E, which is the output of charge pump stage 36E.

It is important to note that the switching threshold of inverters 57A–57E and 59A–59E be carefully adjusted so that the next inverter in the sequence will switch when driven with the output pulse from the previous inverter in the sequence. For example, the peak output voltage from inverter 59A is “V2” volts, and must drive inverter 57C, which is operated from “V3” volts. Therefore, the input threshold of inverter 57C must be set so that an input voltage of V2 volts is recognized as a valid logic “one” input. As another example, the peak output voltage from inverter 57D is “V4” volts, and must drive inverter 59D, which is operated from “V5” volts. Therefore, the input threshold of

inverter 59D must be set so that an input voltage of V4 volts is recognized as a valid logic “one” input.

For a greater understanding of the operation of charge pump 30, assume that an input voltage at node 32 is one volt and a desired output voltage at node 34 is five volts. The following operating conditions are found at various circuit nodes:

TABLE I

## Operating Condition for Five Stage Charge Pump

Node Number(s)	Label	Operating Condition
44, 44A, 44C	V1Ø1	1 V Peak Clock Signal, 1st Phase
46, 46B, 46D	V1Ø2	1 V Peak Clock Signal, 2nd Phase
48	V2Ø1	2 V Peak Clock Signal, 1st Phase
50	V3Ø2	3 V Peak Clock Signal, 2nd Phase
52	V4Ø1	4 V Peak Clock Signal, 1st Phase
54	V5Ø2	5 V Peak Clock Signal, 2nd Phase
56	V6Ø1	5 V Peak Clock Signal, 1st Phase
32	V1	1 V DC Input Voltage
42A	V2	Switched Signal, 1–2 V, 1st Phase
42B	V3	Switched Signal, 2–3 V, 2nd Phase
42C	V4	Switched Signal, 3–4 V, 1st Phase
42D	V5	Switched Signal, 4–5 V, 2nd Phase
34, 42E	V6	5 V DC Output Voltage

## A Preferred Embodiment: Voltage Regulated Charge Pump

Referring now to FIG. 3, a regulated charge pump system 60 includes a voltage input node 68, which receives the low input voltage Vdd1. A voltage output node 70 provides the higher output, charge pumped voltage Vdd. A three stage charge pump 62 (also known as a “voltage multiplier”) has an input coupled to the voltage input node 68, an output coupled to the voltage output node 70, and an oscillator input for receiving the oscin clock signal on conductor 74. As is further explained below, three stage charge pump 62 is similar to the five stage charge pump 30 shown in FIG. 2, except that charge pump 62 receives a single clock signal at the oscillator input, and is converted internally into two antiphase clock signals, as well as other variants of the clock signal for operating the charge pump. A voltage regulator 66 has an input coupled to the voltage output node 70 and a control output for providing the “ctl” control signal on conductor 72. An oscillator 64 has a power terminal coupled to the voltage input node 68, a control input coupled to the voltage regulator control output through conductor 72, and an output coupled to the oscillator input of the charge pump through conductor 74. The circuit configuration and operation of charge pump 62, oscillator 64, and voltage regulator 66 are described in further detail below.

The detailed circuit diagram for charge pump 62 is shown in FIG. 4. In pertinent part, charge pump 62 includes three serially coupled charge pump stages 76A, 76B, and 76C. The output of charge pump stage 76A is coupled to the input of charge pump stage 76B at node 82A. The voltage at node 82A is designated “V1”. The output of charge pump stage 76B is coupled to the input of charge pump stage 76C at node 82B. The voltage at node 82B is designated “V2”. The input of charge pump stage 76A forms the charge pump input at node 68 for receiving the Vdd1 input voltage. The output of charge pump stage 76C forms the charge pump output at node 70 for generating the Vdd output voltage.

Each charge pump stage 76A–76C includes a P-channel pass transistor 78A–78C. Note that the “body” connection of the P-channel transistors is coupled to the output of the respective charge pump stage. Each charge pump stage 76A–76C further includes a capacitor coupled to the P-channel pass transistor at nodes 82A–82C. Note that

capacitors 80A and 80B are ferroelectric capacitors since the dielectric strength is high, providing a desirable high value capacitor such as 0.01 microfarads when fabricated on an integrated circuit. The exact value of capacitors 80A and 80B will vary depending upon the application, and are determined by the amount of time available to reach the desired output voltage, the output load current requirements, and the switching frequency of the clock signals. The final "peak detecting" capacitor 80C is ideally a higher value than capacitors 80A and 80B such as 0.1 microfarads and is external to the integrated circuit containing charge pump 62 to minimize cost. Note that output node 70 must be connected to an external pin, which further militates in favor of making capacitor 80C an external capacitor. The exact value of capacitor 80C can of course vary according to the application, and is primarily determined by the output load current requirement.

Charge pump 62 further includes circuitry for supplying the anti-phase clock signals to the gates of the pass transistors in the respective charge pump stages, as well as to capacitors 80A and 80B. This circuitry includes logic stages 90A, 90B, and 90C as well as a four-output phase generator 92. Logic stages 90A and 90B both include a two input NOR gate 87A, 87B coupled to an inverter 89A, 89B. The inputs of NOR gate 87A receives the OSCA and PH1 clock signals from phase generator 92. The inputs of NOR gate 87B receives the OSCB and PH2 clock signals from phase generator 92. The operation of phase generator 92, as well as the timing of the OSCA, OSCB, PH1, and PH2 clock signals is described in further detail below, especially with reference to the timing diagram of FIG. 5. Inverter 89A drives the gate of P-channel pass transistor 78A at node 84, and inverter 89B drives the gate of P-channel pass transistor 78B at node 86. Logic stage 90C includes serially coupled inverters 87C and 89C. The input of inverter 87C is coupled to node 84, which is the output of inverter 89A. The output of inverter 89C drives the gate of P-channel pass transistor 78C.

Note that each of logic stages 90A-90C has two power terminals, the first of which is coupled to the input of corresponding charge pump stage 76A-76C, and the second of which is coupled to the output of corresponding charge pump stage 76A-76C. In logic block 90A, the input threshold of inverter 89A is set such that the Vdd1 output voltage level supplied by NOR gate 87A is recognized as a logic "one" level. In logic block 90B, the input threshold of inverter 89B is set such that the V1 output voltage level supplied by NOR gate 87B is recognized as a logic "one" level. In logic block 90C, the input threshold of inverter 89C is set such that the Vdd1 output voltage level supplied by NOR gate 87A is recognized as a logic "one" level.

Phase generator 92 includes a first section for generating the OSCA and PH1 clocks signals, which are 180 degrees out of phase with the input "oscin" clock signal at node 74. The first section includes inverter 100, an inverter consisting of transistors 102 and 104, and inverter 106. Inverter 100 receives the "oscin" clock signal at node 74 and provides an inverted OSCA clock signal on conductor 94, which drives one input of NOR gate 87A. Inverter 102, 104 receives the inverted clock signal and drives the input of inverter 106. Inverter 102, 104 is shown as a P-channel transistor 102 and N-channel transistor 104. Note that the "body" of P-channel transistor 102 is coupled to the source, and in turn, to input node 68. Further note that source of N-channel transistor 104 is coupled the output of inverter 114 and not to ground. This connection is to establish a non-overlapping function as is explained in further detail below. The output of inverter 102,

104 drives the input of inverter 106. The output of inverter 106 provides the PH1 clock signal on conductor 96 to the input of NOR gate 87A as well as ferroelectric capacitor 80A. The second section includes inverter 108, an inverter consisting of transistors 110 and 112, and inverter 114. Inverter 108 receives the OSCA clock signal through conductor 94 and provides a non-inverted OSCB clock signal on conductor 95, which drives one input of NOR gate 87B. Inverter 110, 112 receives the non-inverted clock signal and drives the input of inverter 114. Inverter 110, 112 is shown as a P-channel transistor 110 and N-channel transistor 112. Note that the "body" of P-channel transistor 110 is coupled to the source, and in turn, to input node 68. Further note that source of N-channel transistor 112 is coupled the output of inverter 106 and not to ground. This connection is to establish a non-overlapping function as is explained in further detail below. The output of inverter 110, 112 drives the input of inverter 114. The output of inverter 114 provides the PH2 clock signal on conductor 97 to the input of NOR gate 87B as well as ferroelectric capacitor 80B. The power terminals of inverters 100, 106, 108, and 114 are all coupled to input node 68 and are thus powered by the Vdd1 input voltage.

Charge pump 62 further includes initialization circuitry coupled to charge pump Vdd1 input node 68 (which is also the input of the first charge pump stage 76A) for initializing the output of each of the charge pump stages 76B and 76C. Diode-connected transistor 116 has an anode coupled to input node 68 and a cathode coupled to the output of charge pump stage 76B at node 82B. Diode-connected transistor 118 has an anode coupled to input node 68 and a cathode coupled to the output of charge pump stage 76C at node 82C (also identified as charge pump output node 70). Note that the gate and body of each of transistors 116 and 118 are coupled together and to the source to form a diode. In operation, a DC voltage is supplied to input node 68. This voltage, minus a diode voltage drop, is applied to nodes 82B and 82C. In this way, the charge pump stage output voltages must only be pumped up from the Vdd1 value, and not from ground. Thus, the initialization circuitry minimizes the number of cycles needed to establish the final charge pump output voltage at node 70. Within a few cycles, the voltages at the output of charge pump stages 76B and 76C (V2 and Vdd in FIG. 4) is greater than the input Vdd1 voltage and diode-connected transistors 116 and 118 both turn off.

Referring now to FIG. 5, a timing diagram illustrates the OSCA, OSCB, PH1, and PH2 waveforms generated by phase generator 92. The "oscin" clock signal waveform is identical to the OSCB waveform. It should first be noted that the OSCA and OSCB waveforms are simply antiphase square waves. They are not non-overlapping, but have a substantially 50% duty cycle. At time to the OSCA and PH1 clock signals are both at a logic "one" level; clock signals OSCB and PH2 are both at a logic "zero" level. At time t1 both clock signals OSCA and OSCB switch to opposite logic levels. Clock signal PH1 begins to decay immediately. The decay waveshape is due to the capacitive loading of capacitor 80A. At time t1, clock signal PH2 remains at a logic zero level. At time t2, clock signal PH1 is substantially decayed to ground potential, and PH2 begins to switch. Recall that the PH1 clock signal is used to drive the source of N-channel transistor 112, which in turn is used to generate the PH2 clock signal. In other words, inverter 110, 112 does not switch until the source of transistor 112 is returned close to ground potential. At time t3 clock signals OSCA and OSCB again switch. Clock signal PH2 immediately decays, but clock signal PH1 does not begin charging until time t4. The

behavior of the clock signal waveforms at times t1-t4 is repeated for an illustrated second cycle at times t5-t8. It can be seen from the waveforms of FIG. 5 that the PH1 and PH2 clock signals, which are used to drive capacitors 80A and 80B, respectively, are non-overlapping. This is desirable since the capacitors are switched in a manner that conserves charge at nodes 82A and 82B. Capacitors 80A and 80B are only switched when transistors 78A and 78B are completely off.

Charge pump 62 operates in the regulated charge pump system 60 shown in block diagram form in FIG. 3. Two other circuit blocks, a controlled oscillator 64 and voltage regulator 64 are described in further detail below. For a greater understanding of charge pump 62 in the regulated charge pump system 60 assume that an input voltage at node 68 has a voltage input range of 1.9 volts to 4.9 volts and a desired output voltage at node 70 of 5 volts, plus or minus 0.25 volts. Tables II below sets forth the voltages at various charge pump circuit nodes for an input voltage at the low end of the range, i.e. 1.9 volts. Table III below sets forth the voltages at various charge pump circuit nodes for an input voltage at the high end of the range, i.e. 4.9 volts. The 1st Phase nomenclature in Tables II and III refers to a signal being in phase with the "oscin" input clock signal, and the 2nd Phase nomenclature in Tables II and III refers to a signal being out of phase with the "oscin" input clock signal.

TABLE II

Operating Condition for Three Stage Charge Pump (Vdd1 = 1.9 volts)		
Node Number(s)	Label	Operating Condition
94	OSCA	1.9 V Pk Clock Signal, 2nd Phase
95	OSCB	1.9 V Pk Clock Signal, 1st Phase
96	PH1	1.9 V Pk Clock Signal, 2nd Phase
97	PH2	1.9 V Pk Clock Signal, 1st Phase
68	Vdd1	1.9 V DC Input Voltage
82A	V1	Switched Signal, 1.9-3.8 V
82B	V2	Switched Signal, 3.8-5.7 V
82C, 70	Vdd	5 V +/- 0.25 DC Output Voltage

Note that the unregulated output voltage at node 82C would have been 5.7 volts DC, which is three times the input voltage of 1.9 volts DC.

TABLE III

Operating Condition for Three Stage Charge Pump (Vdd1 = 4.9 volts)		
Node Number(s)	Label	Operating Condition
94	OSCA	4.9 V Pk Clock Signal, 2nd Phase
95	OSCB	4.9 V Pk Clock Signal, 1st Phase
96	PH1	4.9 V Pk Clock Signal, 2nd Phase
97	PH2	4.9 V Pk Clock Signal, 1st Phase
68	Vdd1	4.9 V DC Input Voltage
82A	V1	Switched Signal, 4.9-9.8 V
82B	V2	Switched Signal, 9.8-14.7 V
82C, 70	Vdd	5 V +/- 0.25 DC Output Voltage

Note that the unregulated output voltage at node 82C would have been 14.7 volts DC, which is three times the input voltage of 4.9 volts DC.

The output voltage Vdd at node 70 is regulated in a preferred embodiment of the present invention. Two additional circuit blocks, controlled oscillator 64 and voltage regulator 66, provide the voltage regulation. Turning now to FIG. 6, oscillator 64 includes a two input NOR gate 120, wherein one of the inputs receives the "ctl" signal at node

72. The "ctl" signal controls oscillator 64 so that when the "ctl" signal is at a logic one level, an oscillating signal designated "oscout" (which can also be deemed a "controlled clock signal") is presented at output node 74. When the "ctl" signal is at a logic zero level, the controlled clock signal at node 74 is absent and a ground potential is presented. The output of NOR gate 120 drives the input of inverter 122. The output of inverter 122 drives intermediate node 123, which is coupled to a plurality of capacitor-coupled transistors 124A-124E. The gate capacitance of each of the transistors 124A-124E is provided by using the gate as a first capacitor plate and the shorted drain and source as the second capacitor plate. Five capacitor-coupled transistors are shown in FIG. 6, wherein transistors 124A, 124D, and 124E are hard-wired to intermediate node 123. A total capacitance of about one picofarad is presented by these three transistors for an oscillating frequency of about one megahertz at 1.9 volts. Additional transistors 124B and 124C can be coupled to intermediate node 123 by metal mask programming on the integrated circuit for an additional capacitance of about 1.7 picofarads. Capacitor-coupled transistors 124A-124E are binarily weighted and can be added or subtracted as desired for a given application. Although five such transistors are shown in FIG. 6, any number can be used. A higher number will give finer granularity in the selection of oscillation frequency. An acceptable range of frequency for the "oscout" clock signal is from about one megahertz to about two megahertz. Intermediate node 123 is also coupled to the input of Schmitt trigger inverter 126, which converts the substantially sinusoidal oscillating signal at intermediate node 123 into a full logic level square wave signal. The output of inverter 123 is coupled back to the other input of NOR gate 120 as positive feedback, which creates the oscillation. The output of inverter 126 is also coupled to the input inverter 128. The output of inverter 128 in turn, is the output node 74 of oscillator 64. The power terminals of NOR gate 120, inverter 122, Schmitt trigger inverter 126, and inverter 128 are all coupled to node 68 for receiving the Vdd1 lower voltage input voltage.

Turning now to FIG. 7, a voltage regulator 66 includes a resistor string 130, 132, 134, coupled to the regulator input at node 70. The resistor string has first and second taps designated T475 and T525. The tap voltages represent the "low" and "high" values of desired voltage regulation. The "ctl" output signal is a logic one value in response to the Vdd output voltage dropping below 4.75 volts, and is a logic zero value in response to the Vdd output voltage climbing above 5.25 volts. The target regulated voltage is thus 5 volts, plus or minus 0.25 volts. The actual tap voltages are calculated with reference to the bandgap voltage of 1.2 volts provided by a bandgap reference generator 144. Ideally resistor 130 has a value of 747K ohms, resistor 132 has a value of 24K ohms, and resistor 134 has a value of 228K ohms. Other resistance values, of course, can be used and are determined by the desired tap values for other applications, as well as operating current specifications. A first multiplexer 138 has an input coupled to the T475 tap, an output, and two complementary control inputs. A second multiplexer 140 has an input coupled to the T525 tap, an output, and two complementary control inputs. A comparator 142 has a positive input coupled to the outputs of the multiplexers 138 and 140, a negative input for receiving the bandgap voltage, and an output forming the control output of the voltage regulator at node 72 and for controlling the control inputs of the multiplexers 138 and 140. The multiplexers are controlled either directly by the output of comparator 142 or through inverter 136.



In operation, the regulated charge pump system 60 of FIG. 3 generates a boosted, regulated voltage Vdd at node 70 by determining whether the boosted output voltage Vdd is greater or less than a predetermined target output voltage, within preset hysteresis limits, and then selectively charge pumping the Vdd1 input voltage at node 68 to provide a boosted output voltage if the boosted output voltage is less than the predetermined target output voltage, within the preset hysteresis limit. The charge pumping of the Vdd1 input voltage is suspended if the boosted output voltage is greater than the predetermined target output voltage, again within the preset hysteresis limit.

The voltage regulation operation can be clearly seen in the combined timing/waveform diagrams of FIG. 8A and FIG. 8B. In FIG. 8A the output voltage Vdd waveform is shown having four complete cycles, corresponding to a high input voltage such as 4.9 volts. A leading edge portion 146A of the waveform indicates that charge pump 62 is enabled and the output voltage Vdd is increasing. Once the 5.25 volt upper hysteresis threshold is attained, charge pump 62 is disabled and a linear trailing edge portion 148 of the Vdd waveform is shown. The trailing edge portion 148 continues until the 4.75 volt lower hysteresis threshold is attained, and charge pump 62 is once again enabled. The corresponding "ctl" waveform is also shown in FIG. 8A. The ctl waveform is active high during the leading edge portions 146A of the Vdd waveform. In FIG. 8B the output voltage Vdd waveform is shown having only two complete cycles, corresponding to a low input voltage such as 1.9 volts. A much longer leading edge portion 146B of the waveform indicates that charge pump 62 is enabled and the output voltage Vdd is increasing. Once the 5.25 volt upper hysteresis threshold is attained, charge pump 62 is disabled and the same linear trailing edge portion 148 of the Vdd waveform is shown. This is because the linear trailing edge decay is primarily determined by the total current load on charge pump 62. The trailing edge portion 148 continues until the 4.75 volt lower hysteresis threshold is attained, and charge pump 62 is once again enabled. The corresponding "ctl" waveform is also shown in FIG. 8B. The ctl waveform is active high during the leading edge portions 146A of the Vdd waveform. Note the greater active high duty cycle of the ctl waveform in FIG. 8B, corresponding to charge pump 62 being enabled for a longer time to attain the same output voltage.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it is appreciated by those having skill in the art that the invention can be modified in arrangement and detail without departing from such principles. For example, the clock signal frequencies and voltages, number of charge pump stages, output voltage level and regulation limits can all be changed to suit a particular application. Additionally, the voltage polarities used, and type of transistors used in the various circuits presented herein can all be changed by modifications known to those having ordinary skill in the art. I therefore claim all modifications and variation coming within the spirit and scope of the following claims.

I claim:

1. A charge pump comprising:

a charge pump input node for receiving a first voltage;  
a charge pump output node for generating a second voltage; and

a plurality of serially coupled charge pump stages each having an input and an output, wherein the output of a charge pump stage is coupled to the input of a next charge pump stage, the input of a first charge pump stage forming the charge pump input node, and the

output of a last charge pump stage forming the charge pump output node, wherein each charge pump stage comprises:

a pass transistor having a gate, and first and second current nodes respectively coupled to the charge pump stage input and output; and

a capacitor having first and second ends, the first end being coupled to the charge pump stage output,

wherein the gates of the pass transistors and the second ends of the capacitors in odd-numbered charge pump stages receive a first phase voltage, and the gates of the pass transistors and the second ends of the capacitors in even-numbered charge pump stages receive a second phase voltage, except that the second end of the capacitor in the last charge pump stage is coupled to ground.

2. A charge pump as in claim 1 in which the peak value of the voltage applied to the gates of the pass transistor in the charge pump stages increases with each successive charge pump stage.

3. A charge pump as in claim 1 in which the peak value of the voltage applied to the gates of the pass transistor in a charge pump stage is approximately equal to the voltage at the output of the stage.

4. A charge pump as in claim 1 in which the peak value of the voltage applied to the second ends of each of the capacitors is approximately equal.

5. A charge pump as in claim 1 in which the peak value of the voltage applied to the second ends of each of the capacitors is approximately equal to the first voltage on the charge pump input node.

6. A charge pump as in claim 1 in which all of the capacitors, except for the capacitor in the last stage, are ferroelectric capacitors.

7. A charge pump as in claim 1 in which all of the transistors are P-channel MOS transistors.

8. A charge pump as in claim 1 further comprising means for supplying the first and second phase voltages to the gates of the pass transistors in the respective stages.

9. A charge pump as in claim 8 in which the supplying means comprises:

a first plurality of serially coupled buffer stages associated with odd-numbered charge pump stages, each buffer stage having an input and an output, wherein the output of a buffer stage is coupled to the input of a next buffer stage and provides the voltage to the gate of the pass transistor in the respective charge pump stage, the input of a first buffer stage receiving the first phase voltage; and

a second plurality of serially coupled buffer stages associated with even-numbered charge pump stages, each buffer stage having an input and an output, wherein the output of a buffer stage is coupled to the input of a next buffer stage and provides the voltage to the gate of the pass transistor in the respective charge pump stage, the input of a first buffer stage receiving the second phase voltage.

10. A charge pump as in claim 9 in which the buffer stages each comprise a first inverter stage serially coupled to a second inverter stage.

11. A charge pump as in claim 10 in which a power terminal of the first inverter stage is coupled to the input of the respective charge pump stage.

12. A charge pump as in claim 10 in which a power terminal of the second inverter stage is coupled to the output of the respective charge pump stage.

13. A charge pump as in claim 1 in which the number of charge pump stages is equal to three.

## 13

14. A regulated charge pump comprising:

a voltage input node;

a voltage output node;

a charge pump having an input coupled to the voltage input node, an output coupled to the voltage output node, and an oscillator input, in which the charge pump comprises a plurality of serially coupled charge pump stages each having an input and an output, wherein the output of a charge pump stage is coupled to the input of a next charge pump stage, the input of a first charge pump stage forming the charge pump input node, and the output of a last charge pump stage forming the charge pump output node, wherein each charge pump stage comprises a pass transistor having a gate, and first and second current nodes respectively coupled to the charge pump stage input and output, and a capacitor having first and second ends, the first end being coupled to the charge pump stage output, wherein the gates of the pass transistors and the second ends of the capacitors in odd-numbered charge pump stages receive a first phase voltage, and the gates of the pass transistors and the second ends of the capacitors in even-numbered charge pump stages receive a second phase voltage, except that the second end of the capacitor in the last charge pump stage is coupled to ground;

a voltage regulator having an input coupled to the voltage output node and a control output; and

an oscillator having a power terminal coupled to the voltage input node, a control input coupled to the voltage regulator control output, and an output coupled to the oscillator input of the charge pump.

15. A regulated charge pump as in claim 14 further comprising means for supplying the first and second phase voltages to the gates of the pass transistors in the respective stages.

16. A regulated charge pump as in claim 15 in which the supplying means further comprises means for supplying non-overlapping first and second phase voltages to the capacitors in the charge pump stages.

17. A regulated charge pump as in claim 14 further comprising means coupled to the input of the first charge pump stage for initializing the output of each of the charge pump stages.

18. A regulated charge pump comprising:

a voltage input node;

a voltage output node;

a charge pump having an input coupled to the voltage input node, an output coupled to the voltage output node, and an oscillator input;

a voltage regulator having an input coupled to the voltage output node and a control output in which the voltage

## 14

regulator comprises a resistor string coupled to the regulator input having first and second taps, a first multiplexer having an input coupled to the first tap, an output, and a control input, and a second multiplexer having an input coupled to the second tap, an output, and a control input, and a comparator having a first input coupled to the outputs of the first and second multiplexers, a second input for receiving a bandgap voltage, and an output forming the control output of the voltage regulator and for controlling the control inputs of the first and second multiplexers; and

an oscillator having a power terminal coupled to the voltage input node, a control input coupled to the voltage regulator control output, and an output coupled to the oscillator input of the charge pump.

19. A regulated charge pump as in claim 18 in which the charge pump comprises:

a plurality of serially coupled charge pump stages each having an input and an output, wherein the output of a charge pump stage is coupled to the input of a next charge pump stage, the input of a first charge pump stage forming the charge pump input node, and the output of a last charge pump stage forming the charge pump output node, wherein each charge pump stage comprises:

a pass transistor having a gate, and first and second current nodes respectively coupled to the charge pump stage input and output; and

a capacitor having first and second ends, the first end being coupled to the charge pump stage output,

wherein the gates of the pass transistors and the second ends of the capacitors in odd-numbered charge pump stages receive a first phase voltage, and the gates of the pass transistors and the second ends of the capacitors in even-numbered charge pump stages receive a second phase voltage, except that the second end of the capacitor in the last charge pump stage is coupled to ground.

20. A regulated charge pump as in claim 19 further comprising means for supplying the first and second phase voltages to the gates of the pass transistors in the respective stages.

21. A regulated charge pump as in claim 20 in which the supplying means further comprises means for supplying non-overlapping first and second phase voltages to the capacitors in the charge pump stages.

22. A regulated charge pump as in claim 19 further comprising means coupled to the input of the first charge pump stage for initializing the output of each of the charge pump stages.

\* \* \* \* \*



US005212456A

**United States Patent** [19][11] Patent Number: **5,212,456**

Kovalcik et al.

[45] Date of Patent: **May 18, 1993****[54] WIDE-DYNAMIC-RANGE AMPLIFIER  
WITH A CHARGE-PUMP LOAD AND  
ENERGIZING CIRCUIT****[75] Inventors:** Thomas J. Kovalcik, Barrington; Paul  
W. Latham, II, Durham, both of  
N.H.**[73] Assignee:** Allegro Microsystems, Inc.,  
Worcester, Mass.**[21] Appl. No.:** 753,483**[22] Filed:** Sep. 3, 1991**[51] Int. Cl.<sup>5</sup>** ..... H03F 3/45**[52] U.S. Cl.** ..... 330/261; 330/253;  
330/257; 307/296.2**[58] Field of Search** ..... 330/261, 307, 253, 257;  
307/296.2, 303.2**[56] References Cited****U.S. PATENT DOCUMENTS**

4,425,550	1/1984	Smith et al.	330/107
4,581,546	4/1986	Allan	307/296.2
4,591,738	5/1986	Bailas, Jr. et al.	307/296 R
4,871,979	10/1989	Shearer et al.	330/257
5,003,197	3/1991	Nojima et al.	307/296.2
5,059,815	10/1991	Bill et al.	307/296.2

**OTHER PUBLICATIONS**A. B. Grebene, "Bipolar and MOS Analog Integrated  
Circuit Design", Text Book, 1984, John Wiley & Sons,  
pp. 514-517.J. B. Boyd et al., "Low Voltage, Low Cost, High Speed  
Charge Pump with High/Low Gain Operations," IBM  
Technical Disclosure Bulletin, vol. 28, No. 2, Jul. 1985,  
pp. 900-901.*Primary Examiner*—Paul M. Dzierzynski*Assistant Examiner*—Tan Dinh**[57] ABSTRACT**

An amplifier has a first stage employing a pair of differentially connected NMOS amplifier transistors, a second stage composed of a bipolar current mirror circuit and two charge pumps. Each charge pump may be a switching voltage multiplier circuit without the conventional output capacitor. The outputs of the two charge pumps are connected, respectively, to the collector of the current-mirror output transistor and to the commonly connected sources of the NMOS amplifier transistors. Each charge pump serves as both a pulse-voltage energizing source and a load to the amplifier. The amplifier is incorporated with a high-current NMOS transistor in an integrated circuit, wherein one differential input of the amplifier is connected to the source of the driver transistor at which an external load, e.g. a motor, may be connected. The output (collector) of the differential amplifier is connected to the gate of the NMOS driver transistor so that the load current through the driver transistor is held regulated to a value proportional to the input or reference voltage that is applied to the other input of the differential amplifier. The peak pulse voltage of each charge pump is greater than the DC supply voltage from which the driver transistor and the two charge pumps are energized so that the dynamic range of both the input control voltage and the amplifier output to the gate of the NMOS driver transistor is much greater than the DC supply voltage to the integrated circuit.

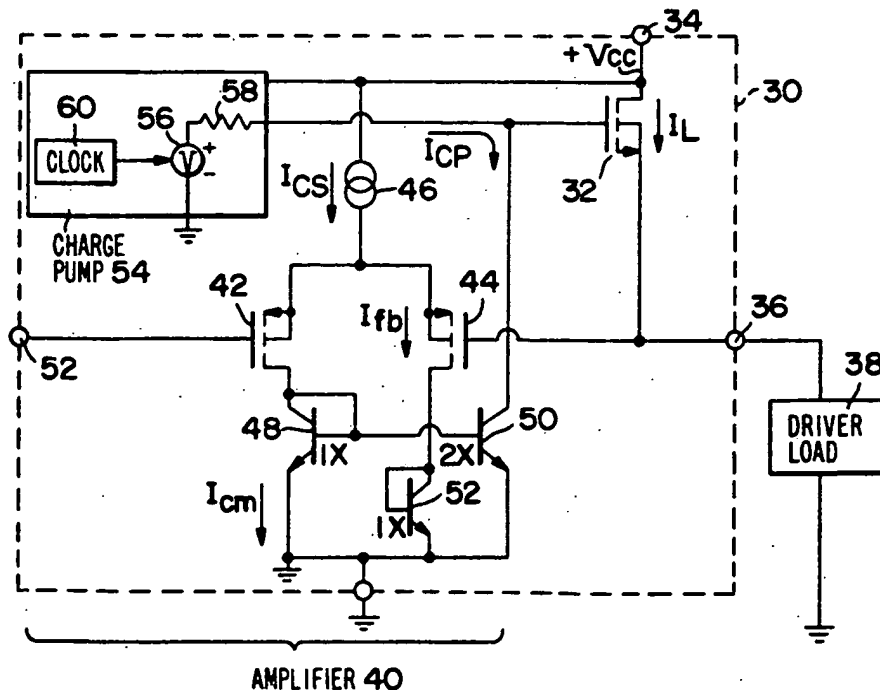
**13 Claims, 2 Drawing Sheets**

FIG. 1  
(PRIOR ART)

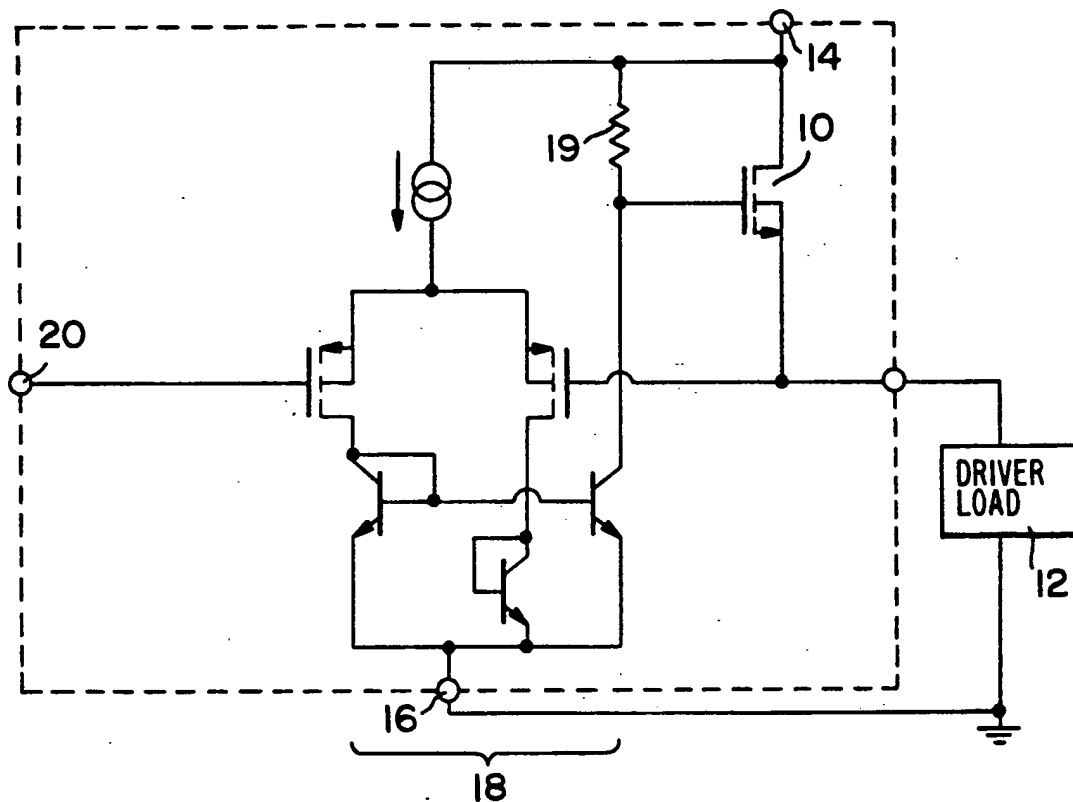
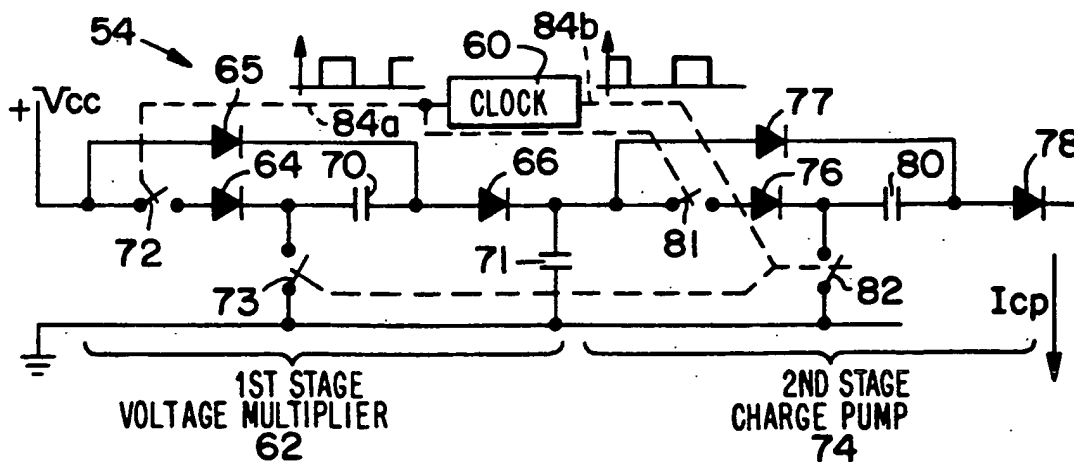
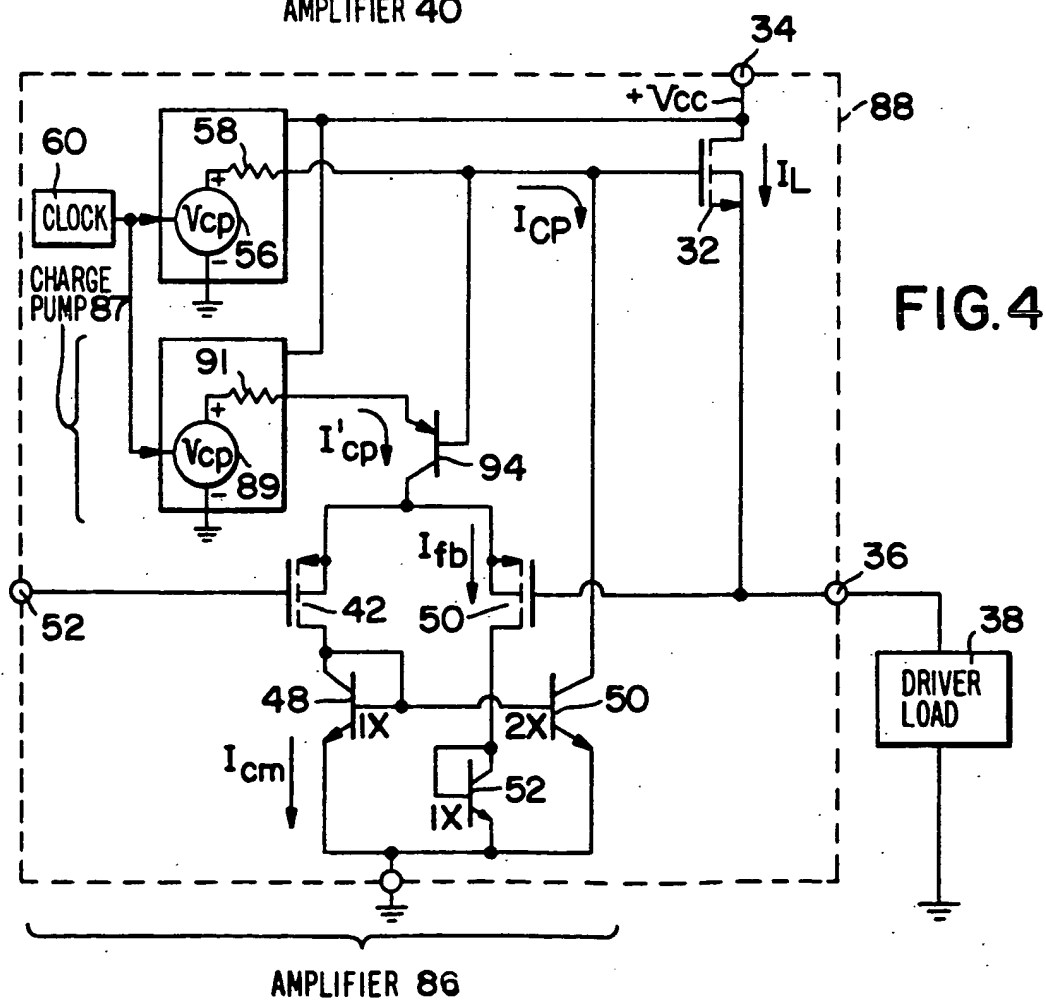
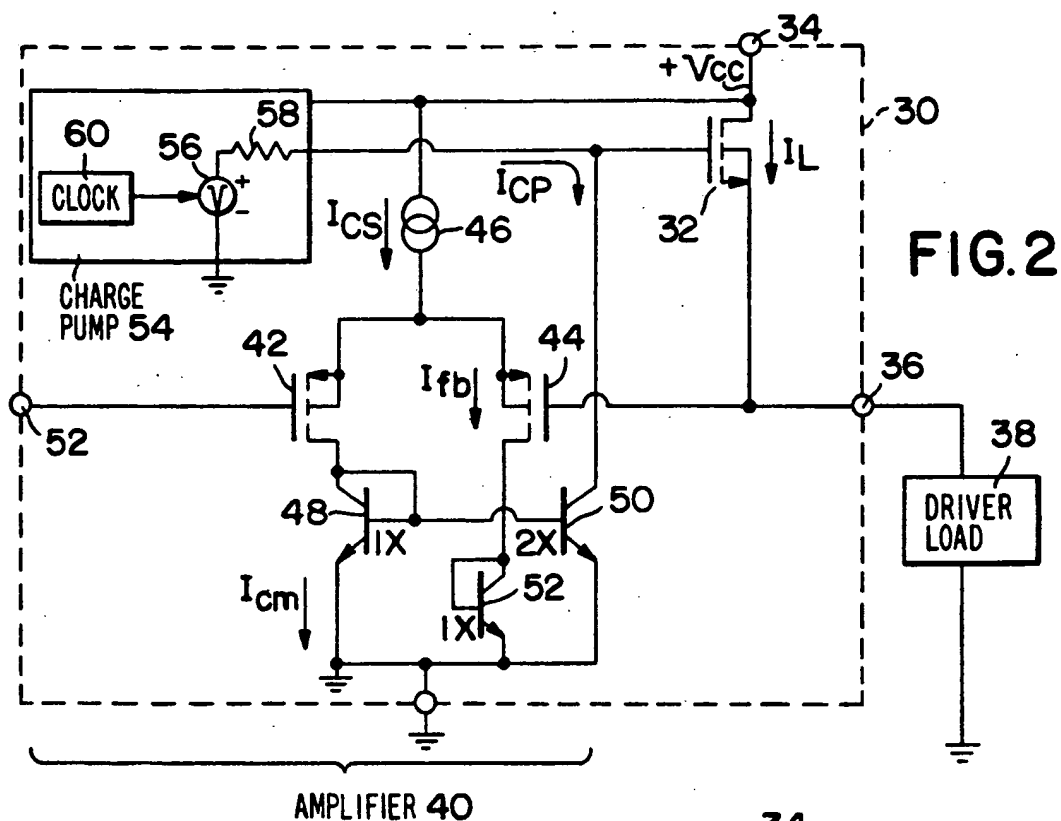


FIG. 3





# WIDE-DYNAMIC-RANGE AMPLIFIER WITH A CHARGE-PUMP LOAD AND ENERGIZING CIRCUIT

## BACKGROUND OF THE INVENTION

This invention relates to electronic signal amplifiers and more particularly to such an amplifier wherein a charge pump serves as the load and source of operating energy.

There is shown in FIG. 1 a typical prior art driver circuit in which an NMOS high-side driver transistor 10 controls the current through a load 12 that is connected to the source of the driver transistor 10. The driver 10 and driver load 12 are connected between a voltage energizing terminal 14, at which a positive voltage  $V_{cc}$  may be applied, and a circuit ground point 16. A differential amplifier 18, having a load resistor 19, is connected in a feedback loop between the source and the gate of the driver transistor 10 for establishing a current in the driver load 12, which driver load current is proportional to the input voltage of the feedback amplifier 18 at input terminal 20.

This driver circuit illustrates a problem in prior art circuits wherein it is desired to energize a high current driver transistor from a voltage source ( $V_{cc}$ ) capable of supplying the necessary high currents to the load, while at the same time it may be desirable to energize relatively low-power driver-control circuits, such as the amplifier 18 in FIG. 1, from a source of voltage that is much greater than  $V_{cc}$  in order to provide a greater dynamic range of input and output driver-control signals.

This problem is typically solved by providing a second energizing voltage source (not shown) for supplying separately the needed higher voltage to the driver control circuits. The considerable additional expense of providing the second and higher voltage supply source is often avoided leading to compromises in amplifier performance, and therefore driver circuit performance. This additional expense is especially objectionable when the driver transistor and the driver control circuits are to be integrated in a single silicon chip.

It is an object of this invention to provide an amplifier circuit capable of having a greater dynamic range of input and output signals than the magnitude of the supply voltage that is used to energize the amplifier.

It is a further object of this invention to provide such an amplifier as a driver-control-signal amplifier in a low cost integrated circuit wherein both the wide dynamic range amplifier and the driver may both be energized from the same voltage source.

## Summary of the Invention

A generic "transistor" to be described herein includes bipolar and field effect transistors (FET's). Such a generic transistor is said to have a control terminal, a high-impedance output terminal and a low-impedance output terminal. These three terms as used herein are to be defined as follows. When the transistor is a FET, the control terminal is the gate, the high-impedance output terminal is the drain and the low-impedance terminal is the source. When the transistor is a bipolar transistor these three terms are respectively the base, collector and emitter.

An amplifier circuit to be described herein will be said to have a high impedance output when it is taken either as a collector or a drain of an output transistor.

Likewise the amplifier will be said to have a low-impedance output when it is taken from an emitter or a FET source.

A linear amplifier circuit of this invention includes a final stage with a high-impedance output, a charge pump having a high output impedance connected to the amplifier output, and an oscillator for producing signal pulses, preferably at a constant frequency. The charge pump is connected to the DC voltage supply conductor for being energized therefrom, and has an input connected to the oscillator for being switched thereby.

The charge pump is for producing at the output under open circuit conditions, voltage pulses at the frequency of the oscillator, which voltage pulses have peak values substantially greater than a DC voltage that may be applied to the DC voltage supply conductor. The output of the charge pump is connected to one of the high-impedance output terminals of the amplifier transistor whereby the substantial source impedance of the charge pump serves as the load and the voltage pulses of the charge pump serve as an energy source to the linear amplifier. The charge pump thus operates approximately as a pulsed current source, the substantial source impedance thereof being at least commensurate with or much greater than the source impedance of the amplifier transistor to which it is connected.

By another measure, the substantial source impedance of the charge pump is preferably large enough that the voltage drop across it, due to current flowing through the output of the charge pump, reduces the peak voltage at that output by more than 50 percent relative to the peak magnitude of the voltage pulses.

Linear amplifiers of this invention may include bipolar or FET amplifier transistors or both and may include a charge pump connected in the output of the last amplifier stage or in the first stage or both. Linear amplifiers of this invention are capable of being energized by a DC supply voltage while providing a greater dynamic input and output voltage range that greatly exceeds the supply voltage, and may therefore advantageously be incorporated in an integrated circuit or used in a system wherein other circuits are included that require a low-voltage high-current DC supply which is suitable for also powering this high resilience amplifier. Furthermore, voltage multiplier and charge pump stages typically include small value capacitors of non-critical value that can readily be provided within an integrated circuit.

The linear amplifier of this invention is particularly well suited for use in an integrated driver circuit. The driver transistor, e.g. a power MOSFET, has a control terminal, e.g. the gate, connected to the output of the linear amplifier; has one high-impedance output terminal, e.g. the drain, connected to the same DC voltage supply conductor that also is the source of energy for the charge pump; and has another but low-impedance output terminal, e.g. the source, connected to the integrated-circuit chip driver-output pad to which an external load, e.g. a motor, may be connected. An input of the amplifier is connected to the driver-output pad to which an external load may be connected, and the high-impedance output of the amplifier is connected to the input terminal of the driver transistor.

In the integrated driver circuit it is preferred that the amplifier is a differential amplifier having a second input to which a reference of control signal voltage may be applied, so that the load current in the driver will be

proportional to the control voltage. Thus an integrated closed-loop regulated driver is provided wherein the amplifier output signal to the driver transistor may have a voltage range much greater than the amplitude of the DC supply voltage to the integrated circuit.

When the driver transistor is a power MOSFET, the bandwidth of the amplifier is controlled by MOSFET gate capacitance and the charge pump source resistance. The gate capacitance is also the charge pump load filter. Good regulation is achieved by choosing the charge pump clock rate to be much larger than the loop bandwidth.

Additional dynamic range in the regulating feedback amplifier by additionally powering the amplifier with a second charge pump energized from the same voltage supply pad and connected to a low-impedance output of the first stage in the linear amplifier, thereby additionally permitting a much greater effective swing in amplifier input control voltage as well. Furthermore the linear amplifier is now a dynamic amplifier, having gain only at the moments when a voltage (and thus a current) pulse is being generated in the second charge pump. When the two charge pumps are clocked by the same on-board oscillator or are otherwise synchronized, the simultaneous currents from the first charge pump and from the output of the linear amplifier that meet at the driver input terminal help to reduce the clock "noise" there. The linear amplifier with the two charge pumps requires little integrated circuit chip area, does not require the use of external discrete components and provides good regulated-driver performance at relatively low cost.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a prior art driver circuit providing an output current that is regulated with respect to the input voltage.

FIG. 2 shows a first regulating driver circuit of this invention including a feedback amplifier with a charge-pump load and energizing circuit.

FIG. 3 shows a circuit diagram of a charge pump employed in the driver circuits of FIG. 2 and FIG. 4.

FIG. 4 shows a second regulating driver circuit of this invention including a feedback amplifier with two charge pumps that each constitute amplifier loads and energizing sources.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 2, a silicon integrated circuit 30 includes an NMOS driver transistor 32 connected drain to source between the voltage supply terminal 34 and the output terminal 36 to which a load 38, e.g. a motor, is connected. An amplifier 40 has a pair of differentially connected NMOS transistors 42 and 44 having their sources connected via the current source 46 to the voltage supply terminal 34 at which a voltage +Vcc is to be applied. The amplifier 40 additionally includes a current mirror circuit composed of an input-branch NPN transistor 48 and an output-branch NPN transistor 50. The NPN transistor 48 is connected to the drain of the differential amplifying NMOS transistor 42 and a diode connected NPN transistor 52 is connected for amplifier balance to the drain of the other differential amplifying NMOS transistor 50. The driver load current  $I_L$  will be proportional to the input voltage applied to the input terminal 52.

The amplifier 40 has a load consisting of a charge pump 54 connected between the collector of the NPN transistor 50 and the voltage supply terminal 34. The charge pump 54 is shown having a Thevenin-equivalent voltage source 56 and a Thevenin-equivalent source resistance 58, a free-running oscillator or pulse generator 60 connected to the voltage source 56 to produce current pulses  $I_{cp}$  of the clock frequency,  $f_c$ , through the NPN current mirror circuit stage of amplifier 40. The magnitude of the charge-pump load current  $I_{cp}$  is twice the magnitude of current  $I_{cm}$  since the base-emitter junction area ( $1\times$ ) of the transistor 50 is ( $2\times$ ) twice that of the transistor 48. The sum of  $I_{cm}$  and  $I_{fb}$  always equals the current source current  $I_{cs}$ .

Referring to FIG. 3, a charge pump circuit is shown corresponding to the equivalent-circuit 54 in FIG. 2. The charge-pump circuit has two stages. The first stage 62 is a standard voltage multiplier circuit, e.g. as described (FIG. 10.23(b) at page 517) in the text book entitled "Bipolar and MOS Analog Integrated Circuit Design" by Alan B Grebene, 1984, John Wiley & Sons; pages 514-517. It includes the three diodes 64, 65, and 67, the two capacitors 70 and 71, and the two clock-actuated switches 72 and 73. The voltage across the output capacitor 71 has a peak value of nearly twice the input voltage  $V_{cc}$ .

Still referring to FIG. 3, the second stage 74 serves as a charge pump stage and includes three diodes 76, 77 and 78, one capacitor 80, and two clock-actuated switches 81 and 82. In general, charge pump 54 may consist of only one stage, namely the charge pump second stage 74; or additional voltage multiplier stages may be included for obtaining even a higher source voltage.

The clock output 84a consists of periodic voltage pulses of frequency  $f$ . When the output voltage at clock output 84a is high the switches 72 and 81 are closed, while at the same time the complementary output voltage at clock output 84b is low keeping switches 81 and 82 open. Switches 72 and 81 are off when switches 73 and 83 are on, and visa versa. The switches 72, 73, 81 and 82 are preferably transistor switches.

The voltage across the capacitor 71 of stage 62 is a positive DC voltage usually with a relatively small amount of ripple superimposed on it. If the ripple is assumed to be negligible, the input voltage to the second charge pump stage 74 can be assumed to be  $2V_{cc}$ , and the Thevenin equivalent voltage of the second stage 74 becomes approximately  $4V_{cc}$  looking back into the output (cathode of diode 78) of stage 74. That Thevenin voltage source 56 is depicted in FIG. 2, the equivalent voltage therefrom having the form of voltage pulses (about  $4V_{cc}$  peak) of clock frequency  $f$ . The source impedance of the charge pump, or a Thevenin equivalent source resistance is  $R_{eq} = 1/f \cdot C_s$ . The average output current is  $I_{cp(av.)} = 4V_{cc}/I_{cp(av.)}$ .  $C_s$  is any capacitance added (not shown) to the driver circuit that tends to load but smooth the charge pump output current  $I_{cp}$ . For example, physically large NMOS driver transistor 10 (FIG. 1) will have a large on-board gate capacitance. This gate capacitance will also provide a significant smoothing of the charge pump current  $I_{cp}$  and thus will smooth the driver gate voltage and driver load current through load 38.

In addition to serving as the charge pump filter, the driver gate capacitance  $C_s$  in conjunction with the charge pump resistance  $R_{eq}$  determine the bandwidth of the amplifier 40 and thus the feedback loop. Good

regulation of the driver load current  $I_L$  through load 38 is achieved by choosing the charge pump clock rate to be much larger than the loop bandwidth.

In the second and most preferred embodiment of this invention as shown in FIG. 4, additional dynamic range of the feedback amplifier 86 may be obtained by energizing the differential NMOS stage (comprised of NMOS transistors 42 and 44) with a second charge pump 87 as is depicted in the integrated circuit chip 88 of FIG. 4.

The charge pump 87 may be identical to the first charge pump 54, e.g. that of FIG. 3 in the driver circuit FIG. 2, except that the insignificant stray capacitance at the output of the second charge pump 87 will have essentially no smoothing effect. In this case, the Thevenin equivalent voltage 89 of charge pump 87 will also be about  $4V_{cc}$  but since the stray capacitance  $C_s$  will be small the Thevenin source resistance 91 will be much larger than that of equivalent resistance 58 leading to good common-mode rejection of the "clock" noise from the charge pumps.

Consequently, in view of the larger source resistance 91 in charge pump 87, a larger common-mode rejection of those common-mode pulses is provided in amplifier 86 (than in amplifier 40 of FIG. 2).

The charge pump 87 may have its output directly connected to the sources of the differential pair of NMOS transistors 42 and 44, but it is preferred to make that connection through the PNP transistor 94 having its base connected to the gate of the NMOS driver transistor 32. In this way the PNP transistor provides even a higher source impedance and thus amplifier 86 has even a greater common-mode rejection. The amplifier 86 which sinks the first charge-pump current  $I_{cp}$  now has gain only at the switching instant when a pulse of charge-pump current  $I_{cp}'$  from the second charge pump 87 is present. Also, the charge pumps 54 and 87 preferably share the same clock 60 as shown in FIG. 4.

The use of a separate charge pump 87 for energizing the differential amplifying transistors, the employment of the PNP transistor 94 for making that connection and the synchronous clocking of the two charge pumps, although not essential, are all contributors to reduction of "clock" noise appearing at the gate of the NMOS driver transistor 32.

What is claimed is:

1. A linear voltage amplifier circuit comprising:

a DC voltage supply conductor;

a final amplifier stage having a high impedance-output;

an oscillator for producing signal pulses;

a charge pump circuit means connected to said DC voltage supply conductor for being energized therefrom, having an input connected to said oscillator, and having an output with a substantial source impedance,

for producing, at said charge-pump-means output under open circuit conditions, voltage pulses at the frequency of said oscillator signal pulses, said voltage pulses having peak values substantially greater than the voltage applied to said DC voltage supply conductor, said high impedance-output of said final amplifier stage being connected to said charge-pump-means output, said substantial source impedance of said output of said charge pump circuit means serving as a load to said final-amplifier-stage transistor and the high voltage pulses of said

charge-pump means serving as a high voltage energizing source to said amplifier transistor.

2. The amplifier of claim 1 wherein said oscillator is a free-running type oscillator for operating at a fixed frequency.

3. The amplifier of claim 1 wherein said charge-pump means consists of diodes, capacitors, and switches for being actuated by said oscillator signal pulses.

4. The amplifier of claim 1 wherein said charge-pump means is a standard voltage multiplier circuit without the output capacitor.

5. The amplifier of claim 1 wherein said substantial source impedance of said charge-pump-means output is large enough that the voltage drop across it due to current flowing through said charge-pump-means output reduces the peak voltage at the charge-pump-means output by more than 50 percent so that the charge-pump means operates approximately as a pulse-current source.

6. An integrated driver circuit of the kind formed in a silicon chip that includes (a) a driver transistor having a control terminal and two output terminals; (b) a supply voltage pad to which one of said driver-transistor output terminals is connected; (c) a driver-circuit output pad to which the other of said driver-transistor output terminals is connected and to which an external driver load may be connected; and (d) a linear amplifier means having one input connected to said driver circuit output pad and including one high-impedance output connected to said driver-transistor input terminal, for regulating the voltage at said driver-circuit output pad, wherein the improvement comprises:

one charge pump circuit means connected to said supply voltage pad for receiving excitation therefrom and having a high-impedance output connected to said one output of said amplifier means for providing an energizing voltage and load impedance to said one output of said amplifier means, said linear amplifier means being additionally for sinking the output current from said one charge pump means, said energizing voltage of said one charge pump means being a series of voltage pulses having a peak amplitude that is substantially greater than a DC supply voltage that may be externally applied to said supply voltage pad.

7. The integrated driver circuit of claim 6 wherein said driver transistor is a field effect transistor.

8. The integrated driver circuit of claim 6 wherein said linear amplifier means includes a differential-amplifier stage with two inputs, one of said two inputs corresponding to said one input connected to said driver circuit output pad, so that the load current in said driver transistor will be regulated with respect to a voltage that may be applied to the other of said two inputs of said differential amplifier stage.

9. The integrated driver circuit of claim 8 wherein said differential-amplifier stage includes a pair of differentially connected field effect transistors, the gates of said pair of transistors corresponding to said two inputs, respectively; said driver circuit additionally comprising a standard current source connected between said voltage supply pad and the sources of said differentially connected field effect transistors.

10. The integrated driver circuit of claim 8 wherein said one output of said linear amplifier-means has a source-impedance which is commensurate with the source impedance of said one charge-pump-means output, said linear amplifier means including another out-



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put having a low-impedance, and said driver circuit additionally comprising a second charge pump means connected to said supply voltage pad for receiving excitation therefrom and having an output connected to said another output of said linear amplifier means for providing energizing voltage pulses and a high-impedance load to said another output of said amplifier means.

11. The integrated driver circuit of claim 10 wherein said differential-amplifier stage is the first linear-amplifier stage, said two differentially connected field effect transistors having their sources connected to the circuit point corresponding to said another low-impedance output of said linear amplifier means.

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12. The integrated driver circuit of claim 10 additionally comprising an oscillator having an output connected to said one and to a second charge pump means for synchronously clocking said charge pump means.

13. The integrated driver circuit of claim 10 additionally comprising a synchronizing transistor means through which said output of said second charge pump means is connected to said another output of said linear amplifier means; said synchronizing transistor having means being further connected to said output of said one pulsing charge pump means for effecting connection between said second charge pump means and said linear amplifier means only during periods when there exists one of said pulses in said one charge pump means.

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Sept. 30, 1969

E. H. BERRY ET AL

3,470,443

POSITIVE DC TO NEGATIVE DC CONVERTER

Filed Dec. 7, 1967

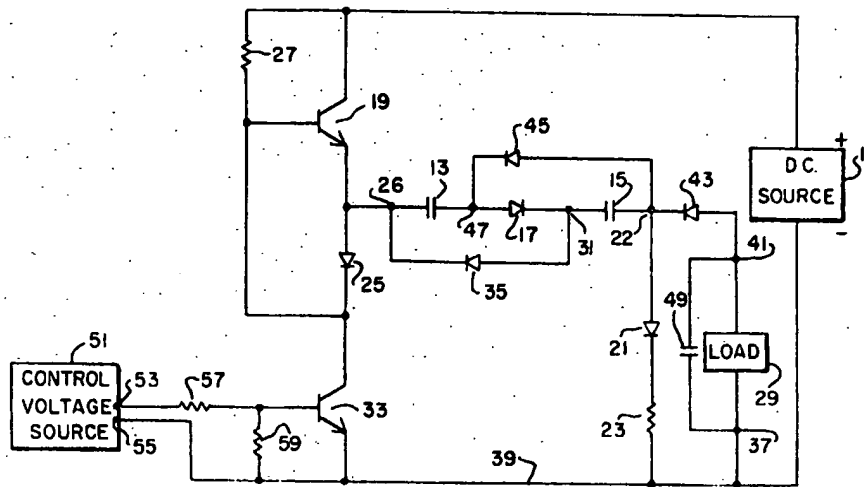


FIG. 1

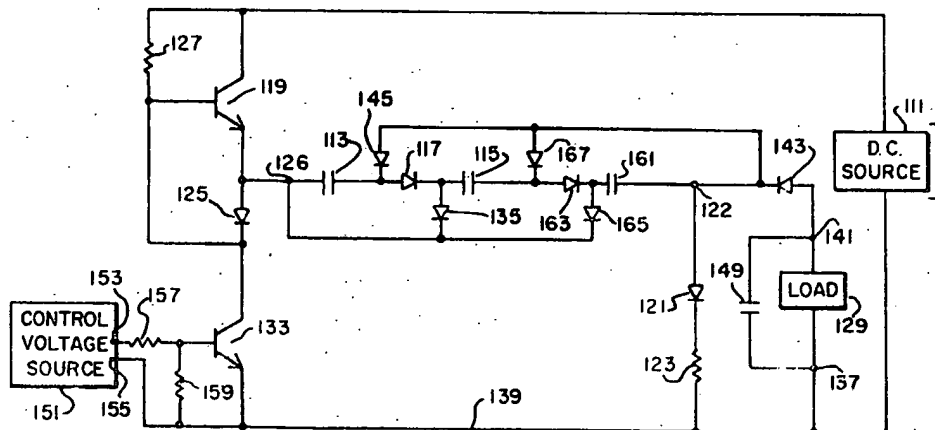


FIG. 2

EUGENE H. BERRY,  
FRANK J. NOLA,  
INVENTOR(S)

BY *Attorney*  
ATTORNEYS

1

3,470,443

**POSITIVE DC TO NEGATIVE DC CONVERTER**  
Eugene H. Berry, Arab, and Frank J. Nola, Huntsville, Ala., assignors to the United States of America as represented by the Administrator of the National Aeronautics and Space Administration

Filed Dec. 7, 1967, Ser. No. 688,807

Int. Cl. H02m 3/22, 3/08

U.S. CL 321-2

3 Claims

## ABSTRACT OF THE DISCLOSURE

An apparatus for converting the output of a positive DC voltage source to a negative DC voltage of lower magnitude across a load having a common reference point with the source where a plurality of capacitors are charged in series and discharged in parallel. Half wave rectifier means connecting the plurality of capacitors in series and in parallel and first and second transistor switches extending between the positive terminal of the DC source and ground for alternately connecting one end of the capacitance circuit to the positive terminal of the DC source and ground. Unidirectional conducting means connecting the opposed end of the capacitance circuit to ground and to the load so as to steer the charging current to ground and to steer the discharging current through the load.

## ORIGIN OF THE INVENTION

The invention described herein was made by employees of the United States Government and may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefor.

## BACKGROUND OF THE INVENTION

This invention relates generally to voltage conversion and more particularly to devices for converting positive direct current voltage to negative direct current voltage of lower amplitude.

In many applications there exists the need for changing the magnitude and polarity of a positive direct current voltage source to obtain a negative secondary source that is referenced to the same ground as the primary source. For example, in spacecraft vehicle installations it is generally necessary to step down the 28 volt direct current source usually installed therein to obtain a low level negative power supply to power operational amplifiers. Also because of the common use of direct coupled circuitry in operational amplifiers a common reference point between the positive DC source and the negative secondary source is required. The usual method is to use a DC to AC converter coupled to a transformer, and a rectifier coupled to the output thereof to provide a direct current output. These devices are quite expensive, bulky and are usually very heavy, all of which limitations are of considerable importance particularly in spacecraft vehicle installations.

Accordingly, one of the objects of this invention is to provide apparatus for changing the magnitude and polarity of a direct current voltage without the use of transformers.

Another object of this invention is to obtain a secondary source of power wherein the secondary source has a common reference point with the primary source.

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## SUMMARY OF THE INVENTION

According to the present invention it has been found that a positive to negative DC converter can be made which has none of the aforementioned shortcoming by employing a plurality of capacitors that are adapted to be alternately charged by a DC source while in series and discharged to a load having a common ground with the DC source while in parallel. The use of a capacitance circuit is made possible by the novel technique of connecting the capacitors in series and in parallel by half wave rectifier means so as to provide a common point that may be alternately connected to the positive terminal of the DC source and ground. This technique coupled with the use of half wave rectifiers for steering the capacitor charging current to ground and for steering the capacitor discharge current to the load permits the development of a negative voltage across the load that is referenced to the same ground as the DC source.

## DESCRIPTION OF THE DRAWINGS

The invention, both as to its organization and operation together with further objects and advantages thereof may best be understood by reference to the following description taken in accordance with the accompanying drawing in which:

FIGURE 1 is a schematic representation of one embodiment of the invention; and

FIGURE 2 is a schematic representation of another embodiment of the invention showing how various ratios of input voltage to output voltage may be achieved.

## DESCRIPTION OF THE EMBODIMENT

In FIGURE 1 there is shown a source of direct current 11, the output voltage of which is to be converted to a different magnitude and polarity. A pair of equal capacitance electrical capacitors 13 and 15 connected in series by half wave rectifier 17, are connected across the terminals of source 11 by means of NPN transistor 19, half wave rectifier 21 and current limiting resistor 23. The collector of transistor 19 is connected to the positive terminal of source 11 and the emitter of transistor 19 is connected to terminal 26 of capacitor 13 and to the anode of half wave rectifier 25. The base of transistor 19 is connected to the positive terminal of the voltage source 11 by resistor 27 and is also connected to the cathode of rectifier 25. Terminal 22 of capacitor 15 is coupled to the anode of rectifier 21 while the cathode of rectifier 21 is coupled to the negative terminal of the source 11 by resistor 23 and lead 39.

To provide means for connecting capacitor 13 and 15 in parallel configuration with the load 29, half wave rectifiers 35 and 45 are provided. Terminal 31 of capacitor 15 is connected to terminal 26 of capacitor 13 by rectifier 35 and terminal 22 of capacitor 15 is connected to terminal 47 of capacitor 13 by rectifier 45. Terminal 26 of capacitor 13 is connected to the collector of NPN transistor 33 by rectifier 25 while the emitter of transistor 33 is connected to terminal 37 of load 29 and to the negative terminal of the DC source 11 by lead 39. A filter capacitor 49 is connected across the load terminals 37 and 41 and terminal 41 is connected to the anode of rectifier 43. The cathode of rectifier 43 is connected to junction 22 of capacitor 15.

To control the conduction of transistor switches 19 and 33, a reversible polarity control voltage source 51, such as a sine wave generator, is provided. The voltage appearing across the output terminals 53 and 55 of the control voltage source is applied across the serial connection of resistors 57 and 59. The midpoint of resistors 57 and 59 is connected to the base of transistor 33 and output terminal 55 of the control voltage source 51 is connected to the emitter of transistor 33 by lead 39.

Transistors 19 and 23 are operated in either the fully on or fully off condition, synchronized in a 180 degree phase relationship so that when transistor 19 is conducting transistor 33 is nonconductive and when transistor 19 is nonconductive transistor 33 is conductive. In operation on the negative half cycle of the control voltage source 51 terminal 53 will be negative with respect to terminal 55 and a reverse bias will be applied to the emitter-base electrodes of transistor 33 causing transistor 33 to be nonconductive. The potential of the collector electrode of transistor 33 will rise sufficiently to allow emitter-base current to flow in transistor 19, causing transistor to assume a fully on state of conduction and terminal 26 of capacitor 13 will be effectively connected to the positive terminal of the DC source 11.

The capacitors 13 and 15 will thus be charged in series to substantially the output voltage of source 11 through the current path consisting of the collector emitter path of transistor 19, capacitor 13, rectifier 17, capacitor 15, rectifier 21 and current limiting resistor 23 with the voltage across each capacitor equal to one half of the source voltage. It will be understood that resistor 23 is provided to protect transistor 19 and rectifiers 17 and 21 from a current in excess of their rated peak instantaneous current when capacitors 13 and 15 are initially connected across the source in an uncharged state.

On the positive half cycle of the control voltage source 51 terminal 53 will be positive with respect to terminal 55 allowing emitter base current to flow in transistor 33 to switch transistor 33 to a fully on state of conduction. With transistor 33 fully on, transistor 19 will be switched to a fully off state and terminal 26 of capacitor 13 will be disconnected from the positive terminal of the DC source 11 and simultaneously connected to terminal 37 of the load 29 and to the negative terminal of the DC source 11 by lead 39.

Capacitor 13 will thus partially discharge through rectifier 25, the emitter-collector path of transistor 33, lead 39, the load 29, rectifier 43 and rectifier 45 while capacitor 15 will partially discharge through rectifier 35, rectifier 25, the collector emitter path of transistor 33, lead 39, the load 29 and rectifier 43. Since the capacitors 13 and 15 are in parallel connection through rectifiers 45 and 35 while being discharged, the negative output voltage presented to the load is substantially one half the voltage of the source 11. Preferably the switching action of transistors 19 and 33 is at an extremely rapid rate so that capacitor 49 can readily eliminate variations in the voltage across the load produced by the switching action described above.

Manifestly, the addition of additional sections of capacitors and half wave rectifiers will provide conversion ratios proportional to the number of sections added. For example, the embodiment shown in FIGURE 2 illustrates the manner of connection when it is desired to obtain a ratio different from 2:1, in this case the conversion ratio is 3:1. As shown in FIGURE 2, wherein reference numerals having the same last two digits designate identical component parts, an additional capacitor 161 is provided which is connected in series with capacitors 113 and 115 by half wave rectifier 163 and is connected in parallel with capacitors 113 and 115 by rectifiers 165 and 167.

The operation of this embodiment is the same as that of FIGURE 1, the capacitors 113, 115 and 161 being connected in series through rectifiers 117 and 163 when transistor 119 is conducting and transistor 33 is noncon-

ducting and being discharged to the load 129 when transistor 133 is conducting and transistor 119 is nonconductive. A voltage conversion of 3:1 is effected in this manner since the voltage across each of the capacitors is one-third that of the total voltage across the capacitors when they are in series connection.

It will now be seen that the present invention provides very efficient means of converting a positive DC voltage to a negative DC voltage of lower amplitude wherein the second source is referenced to the same point as the primary source. Also, it is seen that the conversion is accomplished without the use of transformers.

The invention is not to be restricted to the specific structural details, arrangement of parts, or circuit connections herein set forth, as various modifications therein may be effected without departing from the spirit and scope of this invention.

What is claimed is:

1. Apparatus for converting a positive direct current voltage to a negative direct current voltage of lower magnitude comprising:

a plurality of capacitor means;

first half wave rectifier means connecting said capacitor means in series;

second half wave rectifier means connecting said capacitor means in parallel;

a DC source;

a load having a common reference point with said DC source;

means coupling said serial connection of capacitor means across said DC source, including third rectifier means and first switch means, for providing a charging current path for said capacitor means;

means coupling said parallel connection of capacitor means across said load including fourth rectifier means and second switch means for providing a discharging current path for said capacitor means; and means actuating said first and second switch means in 180 degree phase relationship.

2. Apparatus for converting a positive direct current voltage to a negative direct current voltage source of lower magnitude comprising:

a direct current voltage source having positive and negative output terminals;

a load having first and second input terminals;

means connecting said first load input terminal to said negative direct current source output terminal;

a switching terminal;

a plurality of capacitor means;

first half wave rectifier means connecting said capacitor means in series;

second half wave rectifier means connecting said capacitor means in parallel;

third half wave rectifier means connecting said serial connection of capacitor means between said switching terminal and said negative direct current source output terminal;

fourth half wave rectifier means connecting said parallel connection of capacitor means between said second load input terminal and said switching terminal; and

means for effectively transferring the switching terminal back and forth between the positive direct current source output terminal and the first load input terminal to charge said capacitor means through said first and third half rectifier means when the connection of said switching terminal is to the positive direct current output terminal and to discharge the capacitor means through said second and fourth half wave rectifier means when the connection of said switching terminal is to the first load input terminal.

3. The apparatus of claim 2 wherein said last named means includes:

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a first transistor switch connecting said switching terminal to said positive direct current output terminal; a second transistor switch connecting said switching terminal to said first load input terminal; and control means for driving said first and second transistors alternately between cut-off and saturation in 180 degree relationship to one another.

References Cited

UNITED STATES PATENTS

2,773,200 12/1956 Gugli ..... 321—15 X

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OTHER REFERENCES

Scientific and Technical Aerospace Reports, Capacitive Divider, issue #9, May 8, 1965, p. 1430.

JOHN F. COUCH, Primary Examiner

W. H. BEHA, Jr., Assistant Examiner

U.S. Cl. X.R.

10 307—110, 138; 321—15

[54] **REGULATED POWER SUPPLY WITH  
DIODE CAPACITOR MATRIX**

[76] Inventor: **Aubrey H. Smith**, 6619 Pershing  
Boulevard, Kenosha, Wis. 53140  
[22] Filed: **Dec. 15, 1971**  
[21] Appl. No.: **208,488**

**Related U.S. Application Data**

[62] Division of Ser. No. 131,624, April 6, 1971.  
[52] U.S. Cl. .... **307/109, 323/1, 323/22 T,  
323/22 Z**  
[51] Int. Cl. .... **H02m 3/06**  
[58] Field of Search .... **307/109, 110, 127,  
307/236, 262; 320/1, 323/1, 16, 19, 22 Z;  
328/140**

[56] **References Cited  
UNITED STATES PATENTS**

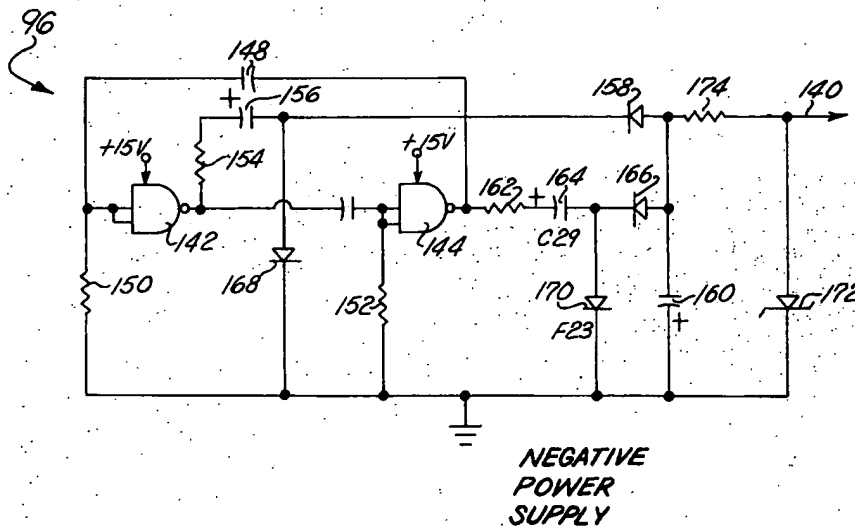
3,240,958	3/1966	Kerios et al. ....	307/110
3,553,480	1/1971	Lehmann et al. ....	307/110
3,375,378	3/1968	Vandemore et al. ....	320/1 X
3,500,342	3/1970	Bissett et al. ....	230/1 X
3,631,259	12/1971	Kiyota ....	320/1 X

**Primary Examiner—A. D. Pellinen**  
**Attorney—R. J. McCloskey**

[57] **ABSTRACT**

A regulated power supply is provided capable of energizing various components of a control system. The regulated power supply includes a negative power supply which comprises an astable multivibrator and a diode-capacitor matrix for directly converting a positive voltage to a regulated negative voltage.

**6 Claims, 2 Drawing Figures**



Patented May 1, 1973

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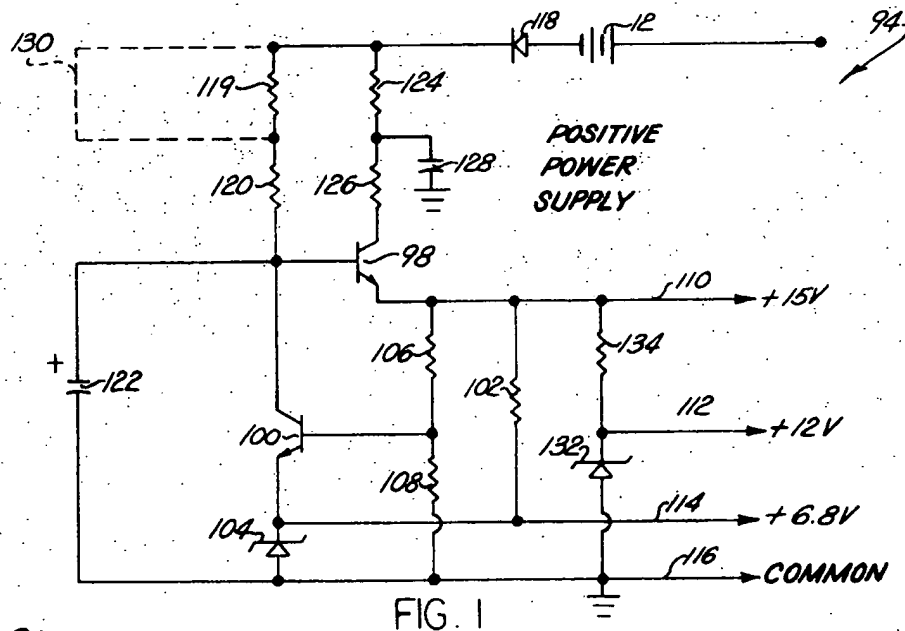


FIG. 1

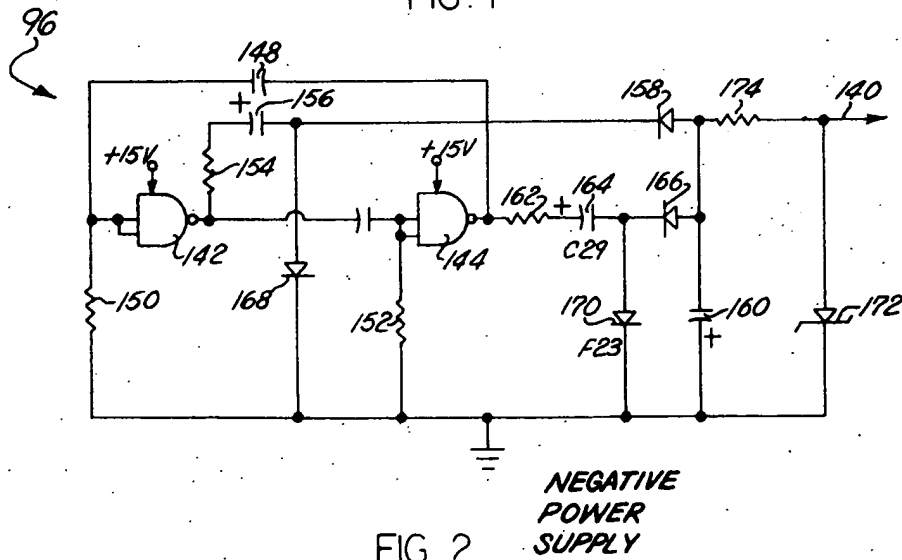


FIG. 2

# REGULATED POWER SUPPLY WITH DIODE-CAPACITOR MATRIX

This is a divisional of application Ser. No. 131,624 filed Apr. 6, 1971.

An object of the present invention is to provide a new and improved control system for controlling the energy directed from a power source to a load including a regulated negative power supply comprising an astable multivibrator and a diode-capacitor matrix connected to the astable multivibrator for inverting the positive voltage supplied to the astable multivibrator directly to a regulated negative voltage.

A further object of the present invention is to provide a power supply for producing a regulated voltage including a power source, an astable multivibrator having a first gate and a second gate, each of the gates being connectable to the power source and having first and second output conditions, the first gate having the first output condition when the second gate has the second output condition and the first gate having the second output condition when the second gate has the first output condition, first energy storage means connected to the output of the first gate, second energy storage means connected to the output of the second gate, third energy storage means connected to the first and second energy storage means and operable to apply a predetermined voltage, the first energy storage means charging when the first gate is in the first condition and discharging when the first gate is in the second condition, the second energy storage means charging when the second gate is in the first condition and discharging when the second gate is in the second condition, the third energy storage means being charged by the first energy storage means when the first gate is in the second condition and being charged by the second energy storage means when the second gate is in the second condition, the third energy storage means being charged by the first and second energy storage means to the predetermined voltage and regulating means connected across the third energy storage means for regulating the voltage applied by the third energy storage means.

Further objects and advantages of the present invention will become apparent from the following detailed description of the present invention taken in conjunction with the following drawings wherein:

FIG. 1 is a schematic illustration of the positive power supply;

FIG. 2 is a schematic illustration of the negative power supply;

A regulated power supply is provided to energize the various components of a control system. The power supply includes a positive power supply 94 and a negative power supply 96. The positive power supply 94 has three outputs therefrom having potentials of plus 12 volts, plus 6.8 volts and 15 volts. The negative power supply has a single output of a minus 6.8 volts.

The positive power supply 94 which is more fully illustrated in FIG. 1, includes transistors 98 and 100. Transistor 98 is a series-regulating variable-impedance transistor whose conductivity is controlled by the collector current of transistor 100. A resistor 102 is connected between the emitter of transistor 98 and the emitter of transistor 100. The resistor 102 limits the amount of current flowing through Zener diode 104 which is connected to the emitter of transistor 100. The

current flow through resistor 102 plus the emitter current of transistor 100 establishes the reference voltage for the Zener diode 104 which in this case is plus 6.8 volts. The base of transistor 100 provides a feedback network for the power supply and is connected to a pair of resistors 106 and 108 which form a voltage divider network have values such that line 110 will always be a plus 15 volts and the base of transistor 100 will be at 6.8 volts plus the base emitter voltage drop of transistor 100. An increase in the potential at the base of transistor 100 will tend to decrease the potential at the emitter of transistor 98 and a decrease in potential at the base of transistor 100 will tend to increase the potential at the emitter of transistor 98 to thereby hold line 110 at plus 15 volts. Thus, the transistors 98 and 100 cooperate to form a negative feedback amplifier utilizing zener diode 104 as a reference.

A battery 12 is connected to the positive power supply 94 through a diode 118 which acts as an isolation diode to prevent negative voltage pulses from occurring in the power supply. When positive pulses occur, resistors 119 and 120 cooperate with the capacitor 122 to form a noise attenuation circuit for the base of transistor 98 and resistors 124 and 126 and capacitor 128 form a noise attenuation circuit for the collector of transistor 98. Since it is desired to utilize the regulated power supply with batteries having different potentials which may range approximately from 18 to 80 volts a jumper 130 is provided to bypass resistor 119. Generally, when the power supply 94 is used with a battery 12 having a potential above 36 volts the jumper 130 will not be utilized, but if a battery potential below 36 volts is utilized the jumper 130 will be connected across resistor 119 to isolate the resistor from the circuit.

The available outputs of the positive power supply 94 are plus 15 volts along line 110, plus 12 volts along line 112, plus 6.8 volts along line 114 and ground potential along line 116. The 12 volt output along line 112 is obtained by applying the 15 volt supply across the Zener diode 132. A resistor 134 is series connected with the Zener diode 132 to limit the current flow to the Zener diode 132.

Since many control system utilize operational amplifiers in stable high gain circuits, the provision of a negative power supply to operate the amplifiers is critical. The common way of producing a negative power supply is to utilize an inverter to drive a small transformer. However, the utilization of a transformer yields a bulky and costly configuration. The present control system utilizes an astable multivibrator for driving a diode-capacitor matrix illustrated in FIG. 2, which inverts the positive power supplied to the multivibrator directly to a negative voltage. This method is not only economical but also requires very little space.

The astable multivibrator includes a pair of NAND gates 142 and 144 each having a plus 15 volt input from the positive power supply 94. A pair of capacitors 156 and 148 introduce feedback to the astable multivibrator. Resistors 150 and 152 are respectively connected to the input of the NAND gate 142 and the NAND gate 144. The resistors 150 and 152 are unequal to assure starting of the multivibrator formed by the NAND gates 142 and 144 upon the application of a potential thereto. When the output of the NAND gate 142 is



high, the output of NAND gate 144 will be low and conversely when the output of NAND gate 144 is high the output of NAND gate 142 will be low.

Connected to the output of gate 142 is a resistor 154 and a capacitor 156. Capacitor 156 is connected through diode 158 to a capacitor 160. Connected to the output of gate 144 is a resistor 162 and a capacitor 164. The capacitor 164 is connected to the capacitor 160 through a diode 166. When the output of gate 142 is high, the capacitor 156 will charge, to approximately 15 volts with a polarity indicated by the plus sign in FIG. 2, through resistor 154 and through a diode 168 which is connected to the ground. When the output of gate 142 goes to low or ground, the capacitor 156 will attempt to discharge through the path including the output of gate 142, resistor 154, diode 158 and capacitor 160. The result of discharging of capacitor 156 through capacitor 160 is that the charge on capacitor 156 will be distributed between capacitors 160 and 156 according to the law of division of charge for capacitors. The polarity of the charge applied to capacitor 160 by capacitor 156 will be that shown by the plus sign in FIG. 2 associated with capacitor 160.

While capacitor 156 is charging capacitor 160, the NAND gate 144 will be in its high state charging capacitor 164 through the path including resistor 162 and a diode 170 which is connected to ground. The capacitor 164 will be charged to approximately 15 volts with the polarity indicated by the plus sign in FIG. 2 associated with capacitor 164. When the astable multivibrator changes state again and the output of gate 144 goes to ground, the capacitor 164 will discharge through the path consisting of the output of gate 144, resistor 162, diode 166 and capacitor 160. The discharging of capacitor 164 will again charge the capacitor 160 to a polarity indicated by the plus sign in FIG. 2. Thus, it should be apparent that the capacitor 156 will charge capacitor 160 during half of the period of oscillation of the astable multivibrator and capacitor 164 will charge capacitor 160 during the other half of the period. The result is a full wave output applied to capacitor 160. Connected across capacitor 160 is a Zener diode 172 having its cathode connected to the ground line. The Zener diode regulates the output from capacitor 160 to line 140, the output line of the negative power supply 96. A resistor 174 is connected to the anode of the Zener diode 172 to limit the current through the diode. Accordingly, the line 140 maintains a minus 6.8 volt potential thereon from capacitor 160.

This power supply includes a positive power supply and a negative power supply for energizing various system components. The negative power supply includes an astable multivibrator and a diode-capacitor matrix which operates to directly invert a positive voltage to thereby provide a negative voltage at the output terminal thereof.

I now claim:

1. A power supply for producing a regulated voltage comprising, a power source, an astable multivibrator having a first gate and a second gate, each of said gates being connectable to the power source and having first and second output conditions, said first gate having said first output condition when said second gate has said second output condition and said first gate having said second output condition when said second gate has

said first output condition, first energy storage means connected to the output of said first gate, second energy storage means connected to the output of said second gate, third energy storage means connected to said first and second energy storage means and operable to apply a predetermined voltage, said first energy storage means charging when said first gate is in said first condition and discharging when said first gate is in said second condition, said second energy storage means charging when said second gate is in said first condition and discharging when said second gate is in said second condition, said third energy storage means being charged by said first energy storage means when said first gate is in said second condition and being charged by said second energy storage means when said second gate is in said second condition, said third energy storage means being charged by said first and second energy storage means to said predetermined voltage, and voltage regulating means connected across said third energy storage means for regulating the voltage applied by said third energy storage means.

2. A power supply for producing a regulated voltage as defined in claim 1 wherein said first energy storage means includes a first capacitor, said second energy storage means includes a second capacitor, and said third energy storage means includes a third capacitor, said third capacitor being charged to a predetermined negative voltage with respect to the power source.

3. A power supply for producing a regulated voltage as defined in claim 2 further including a first diode having its cathode connected to said first capacitor and its anode connected to said third capacitor, and a second diode having its cathode connected to said second capacitor and its anode connected to said third capacitor, said first and second diodes controlling the flow of current to said third capacitor to enable said third capacitor to be charged to the negative voltage with respect to the power source.

4. A power supply for producing a regulated voltage as defined in claim 3 further including a third diode having its anode connected to said first capacitor and its cathode connected to ground, a fourth diode having its anode connected to said second capacitor and its cathode connected to a ground and wherein said voltage regulating means includes a Zener diode connected across said third capacitor for regulating the voltage output therefrom.

5. A regulated power supply for producing a regulated voltage comprising, a positive power source for establishing a positive potential, an astable multivibrator connected to the positive power source, a diode-capacitor matrix connected to the output of said astable multivibrator for inverting the positive potential supplied to said astable multivibrator directly to a negative voltage and voltage regulating means connected to said diode capacitor matrix for regulating said negative voltage established by said diode capacitor matrix, wherein said astable multivibrator includes a first gate and a second gate, said diode-capacitor matrix including a first capacitor connected to the output of said first gate, a first diode having its cathode connected to said first capacitor, a third capacitor connected to the anode of said first diode, a second capacitor connected to the output of said second gate, and a second diode having its cathode connected to said second capacitor,

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said third capacitor being connected to the anode of said second diode and applying a negative voltage.

6. A regulated negative power supply for use with a power source as defined in claim 5 wherein said voltage regulating means includes a Zener diode connected across said third capacitor for regulating the negative voltage applied by said third capacitor.

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[54] CONTROLLED VOLTAGE MULTIPLIER  
PROVIDING PULSE OUTPUT

[75] Inventor: Wilson Greatbatch, Clarence, N.Y.

[73] Assignee: Wilson Greatbatch, Ltd., Clarence,  
N.Y.

[22] Filed: Apr. 29, 1970

[21] Appl. No.: 32,942

[52] U.S. Cl. .... 321/15; 307/110

[51] Int. Cl. .... H02m 3/02

[58] Field of Search ..... 307/110; 321/2, 15, 18;  
128/419 P

[56] References Cited

UNITED STATES PATENTS

1,734,917	11/1929	Peck .....	321/15 X
2,419,574	4/1947	Lehmann .....	307/110 X
2,905,881	9/1959	Aron .....	321/15 X
3,331,014	7/1967	Greenberg et al. ....	321/18 X
3,435,320	3/1969	Lee et al. ....	321/2

OTHER PUBLICATIONS

"Electronics," pp. 97, 98, Mar. 21, 1966.

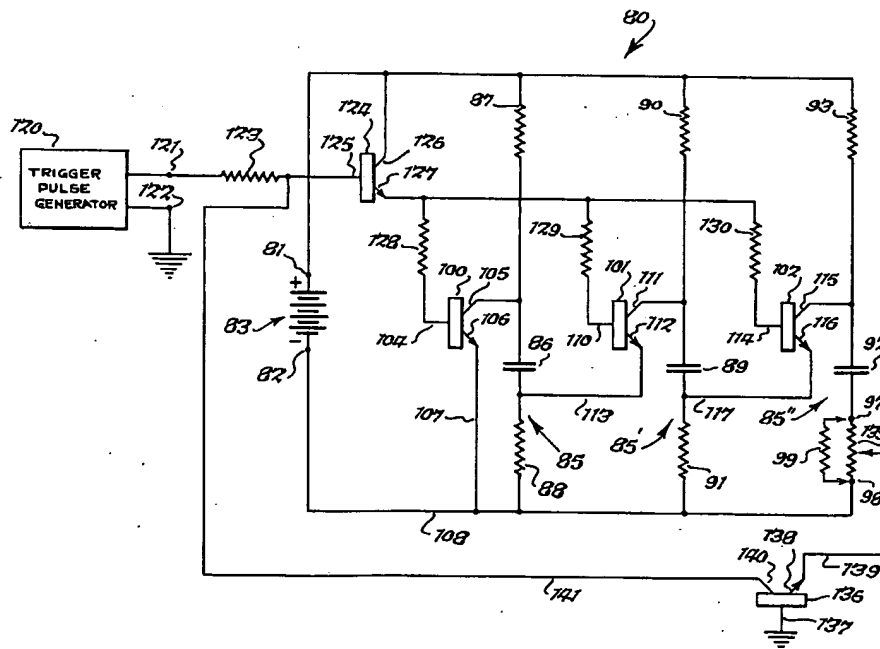
"Electronics," p. 104, Mar. 2, 1970.

Primary Examiner—William H. Beha, Jr.  
Attorney, Agent, or Firm—Christel & Bean

[57] ABSTRACT

A voltage multiplier comprising a pair of input terminals adapted for connection to a source of voltage to be multiplied and a plurality of circuit branches connected in parallel with the terminals, each of the branches including a capacitor and resistance means for developing a voltage on the branch. A pair of output terminals adapted to be connected to a load are connected in series with one of the capacitors whereby the path of current charging that capacitor is through the load. A corresponding plurality of controlled switches such as transistors are connected to corresponding ones of the capacitors, and the switches and capacitors are connected together to define a series discharge path including the pair of output terminals when the switches are operated by trigger means in the form of a pulse generator connected to the control terminal of each of the switches. The voltage multiplier can be provided with regulating means in the form of a potentiometer connected to the output terminals and in controlling relation to a transistor switch for disconnecting the trigger means when the voltage on the output terminals reaches a predetermined magnitude.

18 Claims, 2 Drawing Figures



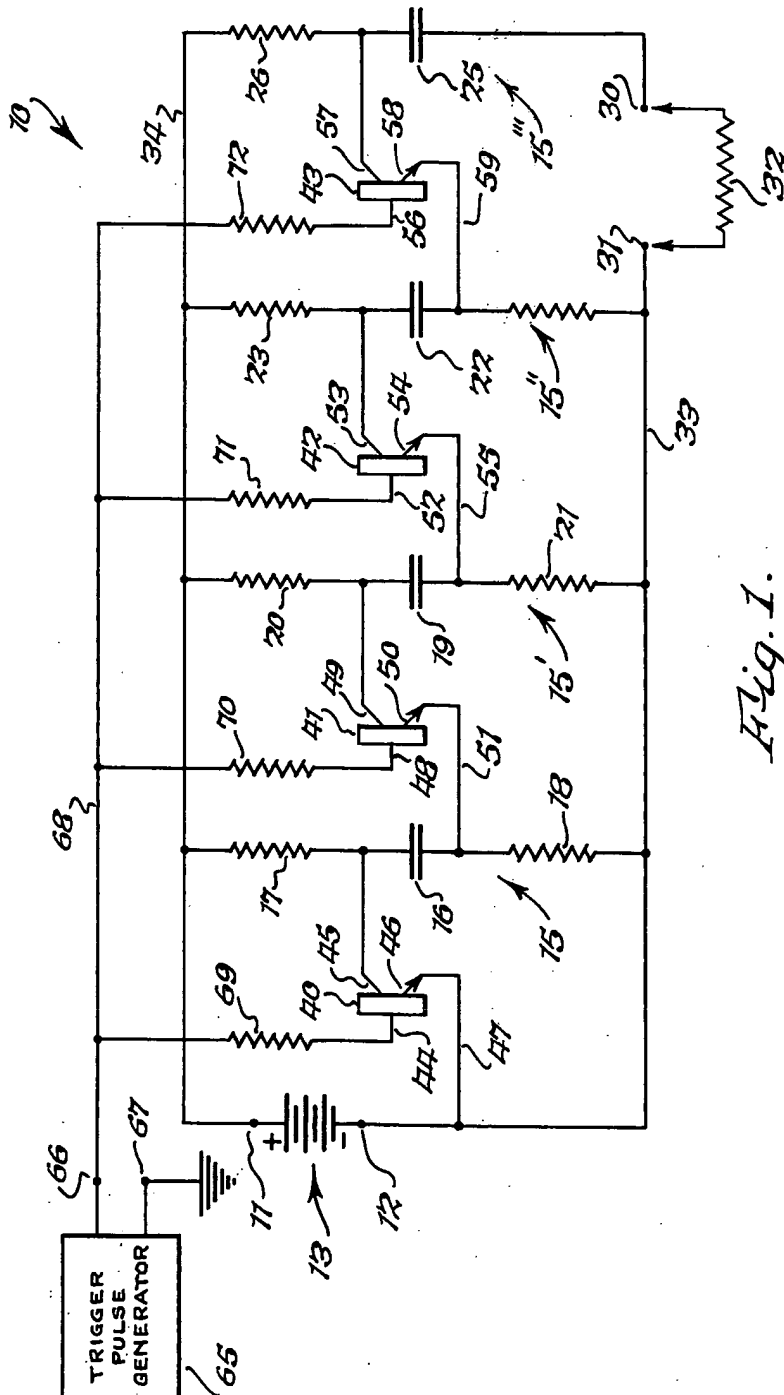
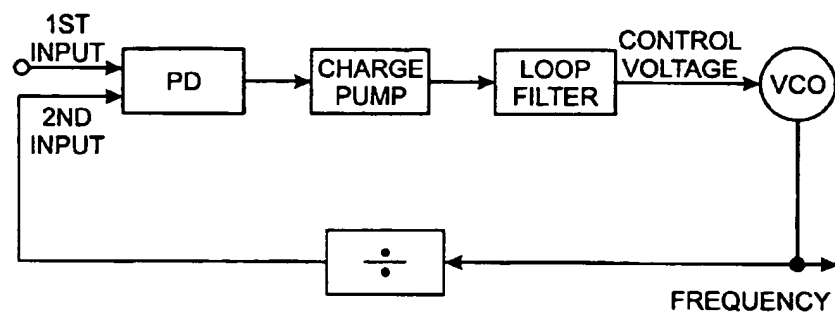


Fig. 1.

INVENTOR  
*Wilson Greatbatch*  
 BY  
*Christel & Bean*  
 ATTORNEYS

**Fig. 1**  
(PRIOR ART)



**Fig. 2**  
(PRIOR ART)

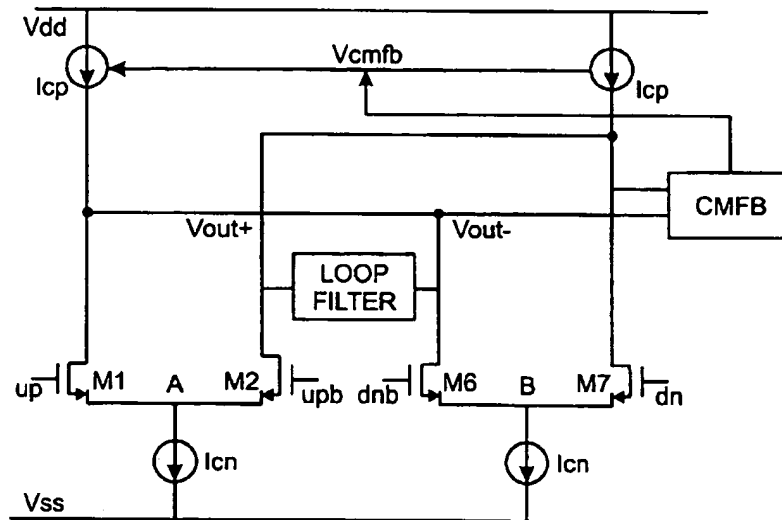


Fig. 3  
(PRIOR ART)

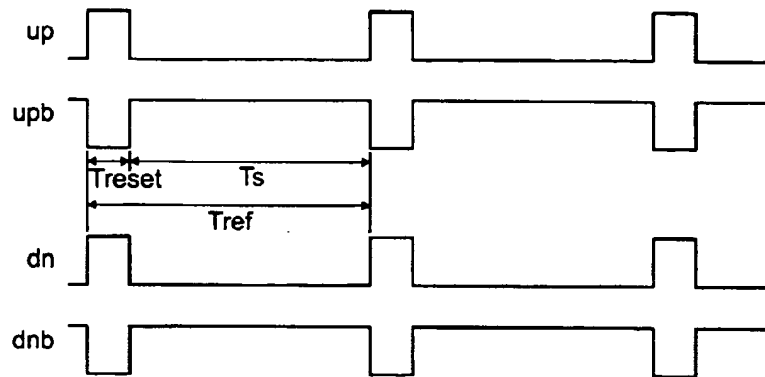


Fig. 5

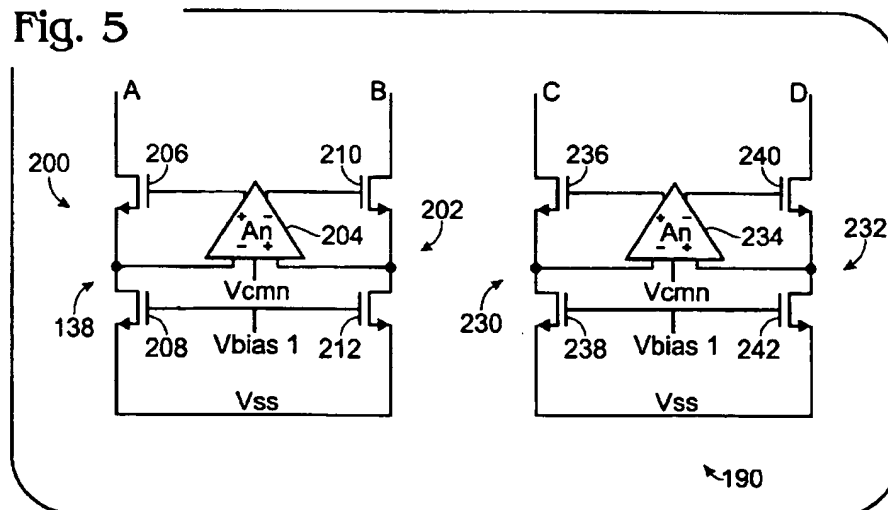


Fig. 4

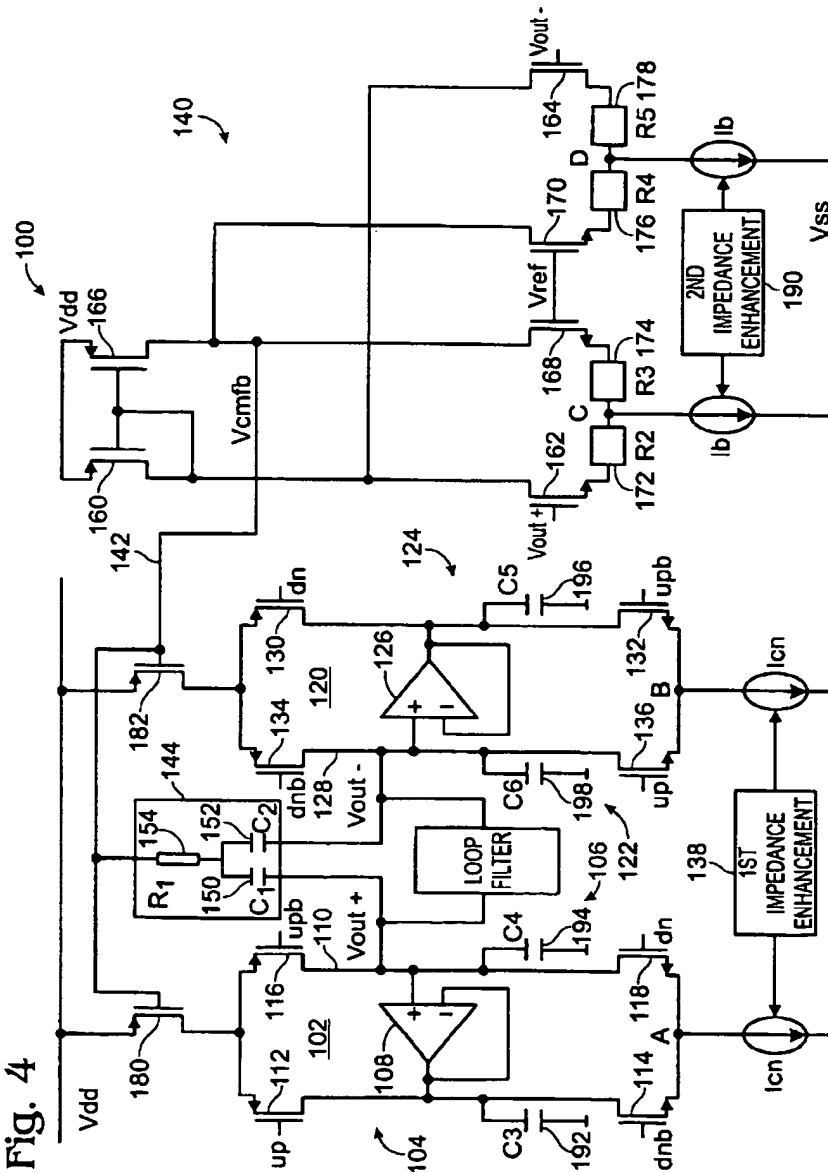


Fig. 6

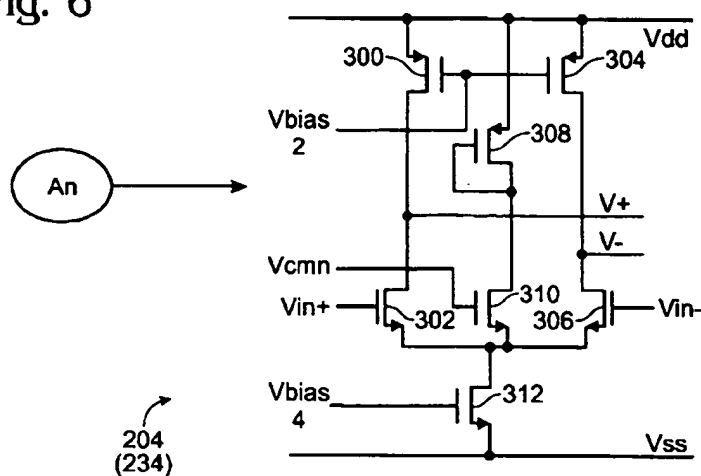


Fig. 7

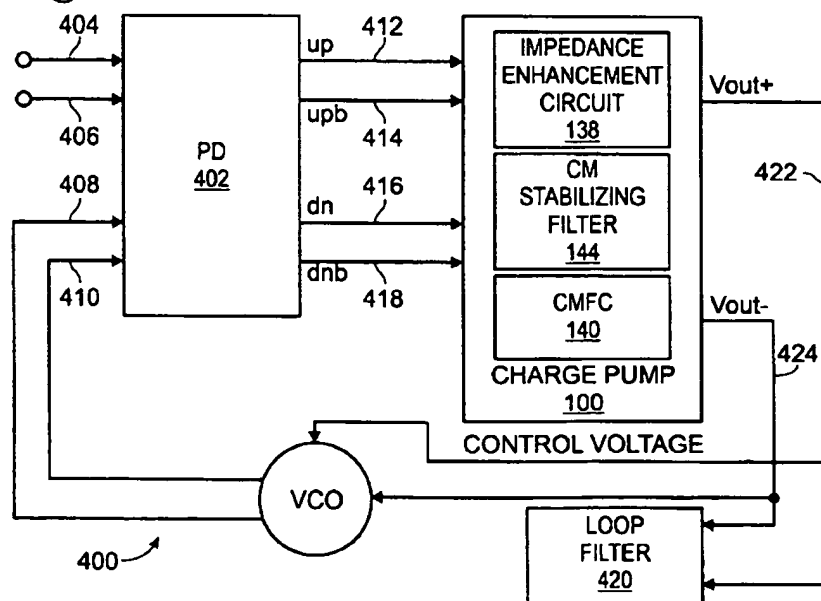
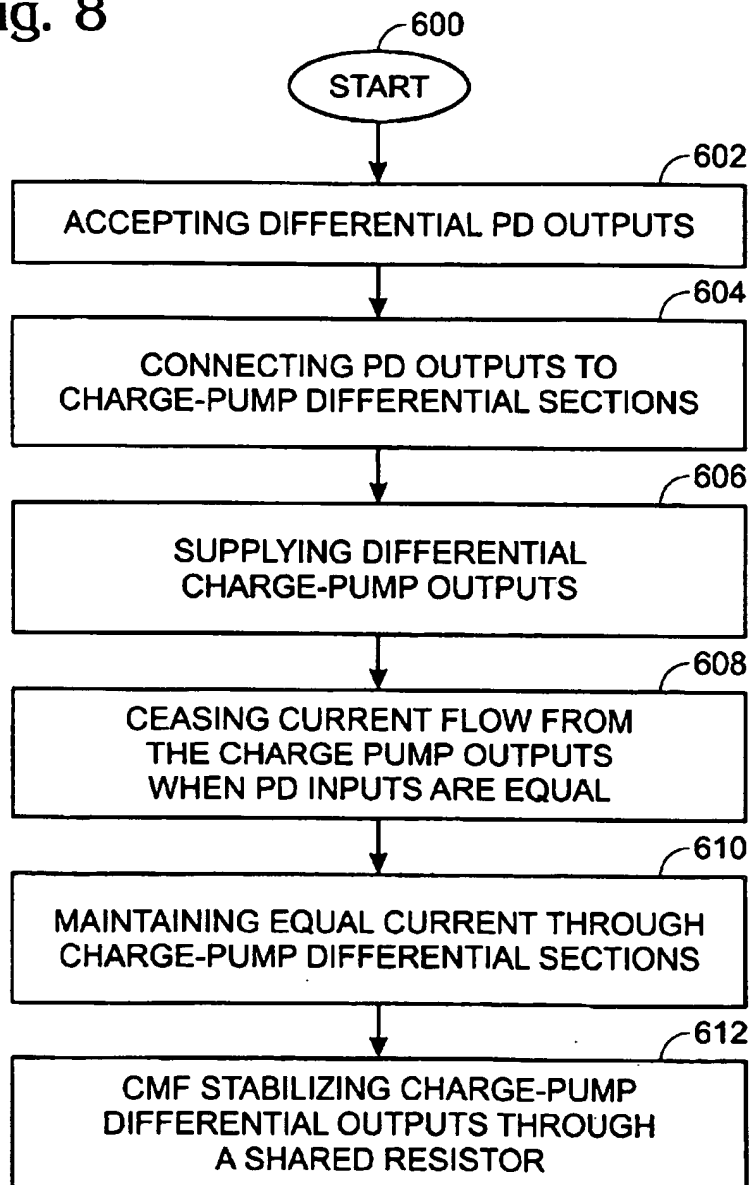




Fig. 8



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# HIGH-PERFORMANCE LOW-NOISE CHARGE-PUMP FOR VOLTAGE CONTROLLED OSCILLATOR APPLICATIONS

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention generally relates to CMOS transistor circuitry and, more particularly, to an improved differential charge-pump suitable for use in a phase-locked loop (PLL) control system.

### 2. Description of the Related Art

FIG. 1 is a schematic block diagram of a conventional phase locked loop (prior art). A phase detector (or frequency detector) receives a first input signal, such as might be supplied on a serial data stream or a clock source, and compares it to a second input signal supplied by the divider. The phase detector (PD) generates an output that is responsive to difference in timing between the two input signals. The charge-pump is typically added to improve the response of the PLL, as the phase detector output does not necessarily have enough drive to instantaneously charge (or discharge) the loop filter reactances. The loop filter is typically a low-pass filter, and is used to control the overall loop response. The voltage controlled oscillator (VCO) supplies an output frequency that is responsive to the input voltage level. The loop is locked when the phase detector inputs match. The divider may be inserted in the path between the VCO and the phase detector.

Charge-pump PLL architecture offers two important advantages: 1) the capture range is only limited by the VCO output frequency range; 2) the static phase error is zero if mismatches and offsets are negligible, as the charge-pumps provide an infinite gain for a static phase difference at the input of the PFD. A wide acquisition range is often necessary because the VCO center frequency may vary considerably with process and temperature. In many applications, the acquisition range of a conventional PLL is inadequate. Since the output of charge-pump is directly connected to the loop filter, the VCO performance is highly dependent upon the quality of charge-pump. Noise generated or transferred by the charge-pump appears as VCO phase noise. Furthermore, a low output swing charge-pump translates into a smaller VCO tuning range, and smaller PLL acquisition range. To build a PLL with low jitter and a large capture range, a high performance low-noise charge-pump is required.

FIG. 2 is a schematic drawing illustrating a conventional differential charge-pump (prior art). Any noise generated by power supplies, radiated frequency sources, or conducted frequency sources, introduced into PLL signal voltages, can be translated into VCO frequency jitter. These noise susceptibilities can be reduced through the use of differential signals. Noise that becomes superimposed on a differential signal is effectively cancelled. To that end, differential charge-pumps have been designed to condition the differential outputs of a phase detector.

FIG. 3 is a timing diagram illustrating the output of the phase detector in the lock condition (prior art). Tref is the total time period of reference clock and Treset is the reset pulse width for avoiding death zone in phase detector. As shown in FIG. 2, the outputs of the charge-pump, Vout+ and Vout-, are always connected to loop filter, during both the Treset and Ts periods. In other words, the noise contributed from charge-pump is added to the VCO control voltage, through the loop filter, at all times. Obviously, this archi-

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itecture can be a source of jitter. The other drawback of this approach is that the output voltage range is limited by both p-type and n-type current sources: Icp and Icn. In general, those current sources consist of cascaded transistors with small voltage output swings.

It would be advantageous if a differential charge-pump could be made more responsive for use in large output voltage swing PLL applications.

It would be advantageous if a differential charge-pump could be disconnected from the loop filter when a PLL was locked, to reduce VCO jitter.

## SUMMARY OF THE INVENTION

The present invention is an improved differential charge-pump. The fully differential charge-pump provides a lower output noise and increased output swing, as compared to conventional designs. The performance of the improved charge-pump makes it suitable for use in CMOS OC-192 transceiver applications, for example.

Accordingly, a method is provided for conditioning the phase detector output in a PLL including a phase detector, a charge-pump, and a loop filter. The method comprises: accepting a pair of differential phase detector (PD) output signals (up/upb and dn/dnb); connecting each pair of differential PD outputs to first and second charge-pump differential sections; supplying differential charge-pump outputs (Vout+/Vout-) in response to the pair of differential PD output signals; and, disconnecting the charge-pump differential section outputs from the loop filter inputs when the PD differential outputs (up/dn and upb/dnb) are equal (when the loop is locked).

In some aspects, supplying differential charge-pump outputs (Vout+/Vout-) in response to the pair of differential PD output signals includes sourcing a first current through the first charge-pump differential section and sourcing a second current through the second charge-pump differential section. Then, the method further comprises maintaining the first current equal to the second current.

Additional details of the above-described charge-pump are provided below.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a conventional phase locked loop (prior art).

FIG. 2 is a schematic drawing illustrating a conventional differential charge-pump (prior art).

FIG. 3 is a timing diagram illustrating the output of the phase detector in the lock condition (prior art).

FIG. 4 is a schematic diagram of the present invention PLL charge-pump.

FIG. 5 is a schematic illustrating exemplary impedance enhancement circuitry, such as may be used to enable the impedance enhancement circuit of FIG. 4.

FIG. 6 is a schematic illustrating an exemplary differential amplifier, such as might be used to enable the first differential amplifier (An) of FIG. 5.

FIG. 7 is a schematic block diagram depicting the present invention phase-locked loop (PLL).

FIG. 8 is a flowchart illustrating the present invention method for conditioning a phase detector output, in a PLL including a phase detector, a charge-pump, and a loop filter.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 4 is a schematic diagram of the present invention PLL charge-pump. The charge-pump 100 comprises a first

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differential section 102 including two cascaded transistor pairs 104 and 106. A first unity-gain operational amplifier (op amp) 108 is interposed between the cascaded pairs 104 and 106. An output (Vout+) is connected to a loop filter first port on line 110. Each transistor is connected to a corresponding one of a pair of differential phase detector outputs (up/upb and dn/dnb). That is, transistor 112 is connected to up, transistor 114 is connected to dnb, transistor 116 is connected to upb, and transistor 118 is connected to dn.

A second differential section 120 includes two cascaded transistor pairs 122 and 124, with a second unity-gain op amp 126 interposed between the cascaded pairs. An output (Vout-) is connected to a loop filter second port on line 128, differential to the first differential section first output on line 110. Each transistor is connected to a corresponding one of the pair of differential phase detector outputs (up/upb and dn/dnb). That is, transistor 130 is connected to dn, transistor 132 is connected to upb, transistor 134 is connected to dnb, and transistor 136 is connected to up.

A first impedance enhancement circuit 138 sources current for the first and second differential sections 102/120. A common-mode feedback circuit (CMFB) 140 has differential inputs connected to the first and second differential section outputs (Vout+/Vout-) on lines 110 and 128, respectively, and an output (Vcmfb) on line 142. A common-mode feedback stabilizing filter 144 is interposed between common-mode feedback circuit output (Vcmfb) on line 142 and the first and second differential section outputs (Vout+/Vout-) on lines 110 and 128, respectively.

FIG. 5 is a schematic illustrating exemplary impedance enhancement circuitry, such as may be used to enable the impedance enhancement circuit 138 of FIG. 4. The first impedance enhancement circuit 138 includes a cascaded transistor pair 200 connected to source current for the first differential section (at node A). A cascaded transistor pair 202 is connected to source current for the second differential section (at node B). A first differential amplifier 204 (An) is interposed between the transistors pairs 200/202.

More specifically, a first field effect transistor (FET) 206 has a drain connected to the first differential section (at node A). The "arrows" represent the FET source. An arrow pointing towards the gate represents a PMOS FET, while an arrow pointing away from the gate represents an NMOS FET. A second FET 208 has a drain connected to the first FET 206 source, a source connected to a reference voltage supply (Vss), and a gate connected to a first bias voltage (Vbias1). A third field FET 210 has a drain connected to the second differential section at node B. A fourth FET 212 has a drain connected to the third FET 210 source, a source connected to the reference voltage supply (Vss), and a gate connected to the first bias voltage (Vbias1).

The first differential amplifier 204 includes a positive input (Vin+) connected to the source of the third FET 210, a negative input (Vin-) connected to the source of the first FET 206, a positive output (V+) connected to the gate of the first FET 206, and a negative output (V-) connected to the gate of the third FET 210. Note that the specific impedance enhancement circuit embodiment will be dependent upon PLL design goals. Alternately stated, there are other impedance enhancement embodiments that might prove useful with the charge-pump of FIG. 4.

Returning to FIG. 4, the common-mode feedback stabilizing filter 144 may include a first capacitor C1 (150) having a first terminal connected to the first differential section output (Vout+) on line 110. A second capacitor C2 (152) has a first terminal connected to the second differential

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section output (Vout-) on line 128 and a second terminal connected to the first capacitor 150 second terminal. A first resistor R1 (154) has a first terminal connected to the second terminals of the first and second capacitors 150/152, and a second terminal connected to the common-mode feedback circuit output (Vcmfb) on line 142.

The first differential section 102 includes a fifth FET 112 having a source operatively connected to a first power supply (Vdd) and a gate connected to a first phase detector (PD) output (up). As used herein, the term "operatively connected" means indirectly connected or connected through an intervening element. A sixth FET 114 has a drain connected to the drain of the fifth FET 112, a source connected to the drain of the first FET 112, and a gate connected to a second differential PD output (dnb).

A seventh FET 116 has a source operatively connected to the first power supply (Vdd) and a gate connected to a first PD differential output (upb). An eighth FET 118 has a drain connected to the drain of the seventh FET 116 and the output (Vout+) on line 110. The eighth FET 118 has a source connected to the drain of the first FET (see FIG. 5) and a gate connected to a second PD output (dn). The first unity gain amplifier 108 has a positive input connected to the drain of the seventh FET 116, a negative input connected to the drain of the fifth FET 112, and an output connected to the drain of the fifth FET 112.

The second differential section 120 includes a ninth FET 130 having a source operatively connected to the first power supply (Vdd) and a gate connected to the second PD output (dn). A tenth FET 132 has a drain connected to the drain of the ninth FET 130, a source connected to the drain of the third FET (see FIG. 5), and a gate connected to the first differential PD output (upb).

An eleventh FET 134 has a source operatively connected to the first power supply (Vdd) and a gate connected to the second PD differential output (dnb). A twelfth FET 136 has a drain connected to the drain of the eleventh FET 134 and the output (Vout-) on line 128. The twelfth FET 136 has a source connected to the drain of the third FET (see FIG. 5) and a gate connected to the first PD output (up). The second unity gain amplifier 126 has a positive input connected to the drain of the eleventh FET 134, a negative input connected to the drain of the ninth FET 130, and an output connected to the drain of the ninth FET 130.

FIG. 6 is a schematic illustrating an exemplary differential amplifier, such as might be used to enable the first differential amplifier 204 (An) of FIG. 5. A thirteenth FET 300 has a source connected to the first power supply (Vdd) and a gate connected to a second bias voltage (Vbias2). A fourteenth FET 302 has a drain connected to the drain of the thirteenth FET 300 and the gate of the first FET (V+, see FIG. 5), and a gate connected to the drain of the fourth FET (Vin+, see FIG. 5). A fifteenth FET 304 has a source connected to the first power supply (Vdd) and a gate connected to the second bias voltage (Vbias2).

A sixteenth FET 306 has a drain connected to the drain of the fifteenth FET 304 and the gate of the third FET (V-, see FIG. 5), a gate connected to the drain of the second FET (Vin-, see FIG. 5), and a source connected to the source of the fourteenth FET 302. A seventeenth FET 308 has a source connected to the first power supply (Vdd) and a drain connected to its gate. An eighteenth FET 310 has a drain connected to the drain of the seventeenth FET 308, a gate connected to a third bias voltage (Vcmn), and a source connected to the source of the fourteenth FET 302. A nineteenth FET 312 has a drain connected to the source of

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the fourteenth FET 302, and gate connected to a four bias voltage ( $V_{bias4}$ ), and a source connected to the reference voltage ( $V_{ss}$ ).

Returning to FIG. 4, an exemplary common-mode feedback circuit 140 is detailed. However, it should be understood that other common-mode feedback designs might be used effectively. As shown, the common-mode feedback circuit 140 includes a twentieth FET 160 having a source connected to the first power supply ( $V_{dd}$ ) and a drain connected to its gate. A twenty-first FET 162 has a drain connected to the drain of the twentieth FET 160 and a gate connected to the first differential section output ( $V_{out+}$ ) on line 110. The line is not shown connected in the interest of clarity. A twenty-second FET 164 has a drain connected to the drain of the twentieth FET 160 and a gate connected to the second differential section output ( $V_{out-}$ ) on line 128.

A twenty-third FET 166 has a source connected to the first power supply ( $V_{dd}$ ) and a gate connected to the gate of the twentieth FET 160. A twenty-fourth FET 168 has a drain connected to the drain of the twenty-third FET 166 and a gate connected to a fifth bias voltage ( $V_{ref}$ ). A twenty-fifth FET 170 has a drain connected to the drain of the twenty-third FET 166 and a gate connected to the fifth bias voltage ( $V_{ref}$ ).

A second resistor ( $R2$ ) 172 has a first terminal connected to the source of the twenty-first FET 162. A third resistor ( $R3$ ) 174 has a first terminal connected to the source of the twenty-fourth FET 168 and the second terminal connected to the second terminal of the resistor 172. A fourth resistor ( $R4$ ) 176 has a first terminal connected to the source of the twenty-fifth FET 170. A fifth resistor ( $R5$ ) 178 has a first terminal connected to the source of the twenty-second FET 164. The first terminal of the fifth resistor 178 is also connected to the second terminal of the fourth resistor 176.

A twenty-sixth FET 180 has a source connected to the first power supply ( $V_{dd}$ ), a gate connected to the drain of the twenty-third FET 166 and the first resistor 154 second terminal ( $V_{cfmb}$ ), and a drain connected to the sources of the fifth and seventh FETs 112/116. A twenty-seventh FET 182 has a source connected to the first power supply ( $V_{dd}$ ), a gate connected to the drain of the twenty-third FET 166 ( $V_{cfmb}$ ), and a drain connected to the sources of the ninth and eleventh FETs 130/134.

In some aspects, the charge-pump 100 further comprises a second impedance enhancement circuit 190 having inputs connected to the second and third resistor 172/174 second terminals (node C), and the fourth and fifth resistor 176/178 second terminals (node D).

In other aspects, the first differential section 102 further includes a third capacitor ( $C3$ ) 192 with a first terminal connected to the drain of the fifth FET 112 and a second terminal connected to ground, or a reference voltage. A fourth capacitor ( $C4$ ) 194 has a first terminal connected to the drain of the seventh FET 116 and a second terminal connected to ground. Likewise, the second differential section 120 may include a fifth capacitor ( $C5$ ) 196 with a first terminal connected to the drain of the ninth FET 130 and a second terminal connected to ground. A sixth capacitor ( $C6$ ) 198 has a first terminal connected to the drain of the eleventh FET 134 and a second terminal connected to ground.

Returning to FIG. 5, an exemplary second impedance enhancement circuit is depicted. Note, that although the second impedance circuit 190 is shown to be the same as the first impedance enhancement circuit 138, the two circuits need not necessarily be identical. As shown, the second impedance enhancement circuit 190 includes a cascaded

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transistor pair 230 connected to source current for the twenty-first and twenty-fourth FETs (see FIG. 4) at node C. A cascaded transistor pair 232 is connected to source current for the twenty-second and twenty-fifth FETs (see FIG. 4) at node D. A second differential amplifier 234 is interposed between the transistors pairs 230/232.

More specifically, the second impedance enhancement circuit 190 includes a twenty-eighth FET 236 having a drain connected to the second and third resistor second terminals (see FIG. 4) at node C. A twenty-ninth FET 238 has a drain connected to the twenty-eighth FET 236 source, a source connected to the reference voltage supply ( $V_{ss}$ ), and a gate connected to the first bias voltage ( $V_{bias1}$ ). A thirtieth FET 240 has a drain connected to the fourth and fifth resistor second terminals (see FIG. 4) at node D. A thirty-first FET 242 has a drain connected to the thirtieth FET 240 source, a source connected to the reference voltage supply ( $V_{ss}$ ), and a gate connected to the first bias voltage ( $V_{bias1}$ ). The second differential amplifier 234 includes a positive input ( $V_{in+}$ ) connected to the source of the thirtieth FET 240, a negative input ( $V_{in-}$ ) connected to the source of the twenty-eighth FET 236, a positive output ( $V_{+}$ ) connected to the gate of the twenty-eighth FET 236, and a negative output ( $V_{-}$ ) connected to the gate of the thirtieth FET 240.

Returning to FIG. 6, the second differential amplifier 234 can be enabled exactly the same as the first differential amplifier 204. A full description will be omitted in the interest of brevity, except to note that the second differential amplifier 234 would include a thirty-second FET as FET 300, a thirty-third FET as FET 302, a thirty-fourth FET as FET 304, a thirty-fifth FET as FET 306, a thirty-sixth FET as FET 308, a thirty-seventh FET as FET 310, and a thirty-eighth FET as FET 312. Note that is some other aspects of the invention, the second differential amplifier 234 may be configured differently than the first differential amplifier 204.

FIG. 7 is a schematic block diagram depicting the present invention phase-locked loop (PLL). The PLL 400 comprises a phase detector (PD) 402 having pair of differential inputs on lines 404/406 and 408/410, and a pair of differential outputs on lines 412/414 and 416/418 (up/upb and dn/dnb). The PLL 400 includes the charge-pump 100 described above in the explanation of FIGS. 4 through 6. Briefly, the charge-pump includes first and second differential sections, a first impedance enhancement circuit 138 sourcing current for the first and second differential sections, a common-mode feedback circuit 140, and a common-mode feedback stabilizing filter 144. In the interest of brevity, the details of the above-mentioned circuits will not be repeated here.

A loop filter 420 has differential ports connected to the charge-pump first and second differential section outputs ( $V_{out+}/V_{out-}$ ) on lines 422 and 424. A voltage controlled oscillator (VCO) 426 has differential inputs connected to the loop filter differential ports on lines 422 and 424 and a frequency output on lines 408/410 responsive to the VCO differential inputs on lines 422/424.

#### FUNCTIONAL DESCRIPTION

The present invention high performance CMOS charge-pump operates with extremely low noise and a large voltage output swing. Further, the charge-pump design is less susceptible to mismatching.  $V_{dd}$  and  $V_{ss}$  are power supply and ground, respectively. The loop filter is differentially connected to the output of charge-pump in a manner that reduces, by half, the size of loop filter's capacitors. The common-mode feedback loop consists of transistors 116,

180, 134, 182, elements R1, C1, C2, and transistors 162, 168, 170, and 164. This loop forces the output common-mode voltage of charge-pump to be same as common-mode reference voltage Vref. The common-mode feedback loop is stabilized with elements R1, C1, and C2. In order to achieve good matching and reduce the resistor size, the two capacitors (C1 and C2) share a single compensation resistor R1.

Note that the output of charge-pump only connects to the loop filter when up and dn are both high. In the other words, the loop filter is completely disconnected from charge-pump during time period Ts (see FIG. 3). Also note that Ts is much longer than Treset, which is only about 10% of Tref. Consequently, the total noise contributed from charge-pump is decreased dramatically. The output swing is also improved because there is only one transistor 180/182 in the current (p-type) path. A very large VCO tuning range is created in response to the large voltage differentials that are possible between Vout+ and Vout-. In prior art circuitry, the large voltage differences at nodes A and B can dramatically degrade current gain, as the current Icn at node A differs from the current Icn at node B. To address this problem, the present invention has added an impedance enhancement circuit to match the output impedances of current sources. In this manner, the two Icn currents remain the same, regardless of voltage difference between the nodes A and B. Likewise, a second impedance enhancement circuit has been added to address large differential voltages likely to occur between nodes C and D. The second impedance enhancement circuit generally performs the same functions as the first impedance enhancement circuit. That is, the second impedance enhancement circuit maintains equal Ib currents through nodes C and D.

FIG. 8 is a flowchart illustrating the present invention method for conditioning a phase detector output, in a PLL including a phase detector, a charge-pump, and a loop filter. Although the method is depicted as a sequence of numbered steps for clarity, no order should be inferred from the numbering unless explicitly stated. It should be understood that some of these steps may be skipped, performed in parallel, or performed without the requirement of maintaining a strict order of sequence. The method starts at Step 600.

Step 602 accepts a pair of differential phase detector (PD) output signals (up/upb and dn/dnb). Step 604 connects each pair of differential PD outputs to first and second charge-pump differential sections. Step 606 supplies differential charge-pump outputs (Vout+Vout-) in response to the pair of differential PD output signals. Step 608 disconnects the charge-pump differential section outputs from the loop filter inputs when the PD differential outputs (up/dn and up/dn) are equal. That is, the differential outputs are disconnected when the PLL is locked.

In some aspects, supplying differential charge-pump outputs (Vout+Vout-) in response to the pair of differential PD output signals in Step 606 includes sourcing a first current through the first charge-pump differential section and sourcing a second current through the second charge-pump differential section. Then, Step 610 maintains the first current equal to the second current. In other aspects, Step 612 common-mode feedback stabilizes the differential charge-pump outputs (Vout+Vout-) through a shared resistor.

A low-noise high-performance differential charge-pump has been described. Simplified circuits were presented to exemplify the inventions. However, the invention is not limited to merely these examples. Other variations and embodiments of the invention will occur to those skilled in the art.

We claim:

1. A phase-locked loop (PLL) charge-pump comprising:
  - a first differential section including two cascaded transistor pairs, with a first unity-gain operational amplifier (op amp) interposed between the cascaded pairs, an output (Vout+) connected to a loop filter first port, and where each transistor is connected to a corresponding one of a pair of differential phase detector outputs (up/upb and dn/dnb);
  - a second differential section including two cascaded transistor pairs, with a second unity-gain op amp interposed between the cascaded pairs, an output (Vout-) connected to a loop filter second port, differential to the first differential section first output, and where each transistor is connected to a corresponding one of the pair of differential phase detector outputs (up/upb and dn/dnb);
  - a first impedance enhancement circuit sourcing current for the first and second differential sections;
  - a common-mode feedback circuit having differential inputs connected to the first and second differential section outputs (Vout+/Vout-), and an output (Vcmfb); and,
  - a common-mode feedback stabilizing filter interposed between common-mode feedback circuit output (Vcmfb) and the first and second differential section outputs (Vout+/Vout-).
2. The charge-pump of claim 1 wherein the first impedance enhancement circuit includes:
  - a cascaded transistor pair connected to source current for the first differential section;
  - a cascaded transistor pair connected to source current for the second differential section; and,
  - a first differential amplifier interposed between the transistors pairs.
3. The charge-pump of claim 2 wherein the first impedance enhancement circuit includes:
  - a first field effect transistor (FET) having a drain connected to the first differential section;
  - a second FET having a drain connected to the first FET source, a source connected to a reference voltage supply (Vss), and a gate connected to a first bias voltage (Vbias1);
  - a third field FET having a drain connected to the second differential section;
  - a fourth FET having a drain connected to the third FET source, a source connected to the reference voltage supply (Vss), and a gate connected to the first bias voltage (Vbias1); and,
 wherein the first differential amplifier includes a positive input (Vin+) connected to the source of the third FET, a negative input (Vin-) connected to the source of the first FET, a positive output (V+) connected to the gate of the first FET, and a negative output (V-) connected to the gate of the third FET.
4. The charge-pump of claim 3 wherein the common-mode feedback stabilizing filter includes:
  - a first capacitor having a first terminal connected to the first differential section output (Vout+);
  - a second capacitor having a first terminal connected to the second differential section output (Vout-) and a second terminal connected to the first capacitor second terminal; and,
  - a first resistor having a first terminal connected to the second terminals of the first and second capacitors and

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a second terminal connected to the common-mode feedback circuit output (Vcmfb).

5. The charge-pump of claim 4 wherein the first differential section includes:

a fifth FET having a source operatively connected to a first power supply (Vdd) and a gate connected to a first phase detector (PD) output (up);

a sixth FET having a drain connected to the drain of the fifth FET, a source connected to the drain of the first FET, and a gate connected to a second differential PD output (dnb);

a seventh FET having a source operatively connected to the first power supply (Vdd) and a gate connected to a first PD differential output (upb);

an eighth FET having a drain connected to the drain of the seventh FET and the output (Vout+), a source connected to the drain of the first FET, and a gate connected to a second PD output (dn); and,

wherein the first unity gain amplifier has a positive input connected to the drain of the seventh FET, a negative input connected to the drain of the fifth FET, and an output connected to the drain of the fifth FET.

6. The charge-pump of claim 5 wherein the second differential section includes:

a ninth FET having a source operatively connected to the first power supply (Vdd) and a gate connected to the second PD output (dn);

a tenth FET having a drain connected to the drain of the ninth FET, a source connected to the drain of the third FET, and a gate connected to the first differential PD output (upb);

an eleventh FET having a source operatively connected to the first power supply (Vdd) and a gate connected to the second PD differential output (dnb);

a twelfth FET having a drain connected to the drain of the eleventh FET and the output (Vout-), a source connected to the drain of the third FET, and a gate connected to the first PD output (up); and,

wherein the second unity gain amplifier has a positive input connected to the drain of the eleventh FET, a negative input connected to the drain of the ninth FET, and an output connected to the drain of the ninth FET.

7. The charge-pump of claim 6 wherein the first differential amplifier includes:

a thirteenth FET having a source connected to the first power supply (Vdd) and a gate connected to a second bias voltage (Vbias2);

a fourteenth FET having a drain connected to the drain of the thirteenth FET and the gate of the first FET (V+), and a gate connected to the drain of the fourth FET (Vin+);

a fifteenth FET having a source connected to the first power supply (Vdd) and a gate connected to the second bias voltage (Vbias2);

a sixteenth FET having a drain connected to the drain of the fifteenth FET and the gate of the third FET (V-), a gate connected to the drain of the second FET (Vin-), and a source connected to the source of the fourteenth FET;

a seventeenth FET having a source connected to the first power supply (Vdd) and a drain connected to its gate;

an eighteenth FET having a drain connected to the drain of the seventeenth FET, a gate connected to a third bias voltage (Vcmn), and a source connected to the source of the fourteenth FET; and,

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a nineteenth FET having a drain connected to the source of the fourteenth FET, and gate connected to a four bias voltage (Vbias4), and a source connected to the reference voltage (Vss).

8. The charge-pump of claim 7 wherein the common-mode feedback circuit includes:

a twentieth FET having a source connected to the first power supply (Vdd) and a drain connected to its gate;

a twenty-first FET having a drain connected to the drain of the twentieth FET and a gate connected to the first differential section output (Vout+);

a twenty-second FET having a drain connected to the drain of the twentieth FET and a gate connected to the second differential section output (Vout-);

a twenty-third FET having a source connected to the first power supply (Vdd) and a gate connected to the gate of the twentieth FET;

a twenty-fourth FET having a drain connected to the drain of the twenty-third FET and a gate connected to a fifth bias voltage (Vref);

a twenty-fifth FET having a drain connected to the drain of the twenty-third FET and a gate connected to the fifth bias voltage (Vref);

a second resistor having a first terminal connected to the source of the twenty-first FET;

a third resistor with a first terminal connected to the source of the twenty-fourth FET and the second terminal connected to the second resistor second terminal;

a fourth resistor with a first terminal connected to the source of the twenty-fifth FET;

a fifth resistor with a first terminal connected to the source of the twenty-second FET, the fifth resistor first terminal also connected to the second terminal of the fourth resistor;

a twenty-sixth FET having a source connected to the first power supply (Vdd), a gate connected to the drain of the twenty-third FET and the first resistor second terminal (Vcmfb), and a drain connected to the sources of the fifth and seventh FETs; and,

a twenty-seventh FET having a source connected to the first power supply (Vdd), a gate connected to the drain of the twenty-third FET (Vcmfb), and a drain connected to the sources of the ninth and eleventh FETs.

9. The charge-pump of claim 8 further comprising:

a second impedance enhancement circuit having inputs connected to the second and third resistor second terminals, and the fourth and fifth resistor second terminals.

10. The charge-pump of claim 9 wherein the second impedance enhancement circuit includes:

a cascaded transistor pair connected to source current for the twenty-first and twenty-fourth FETs;

a cascaded transistor pair connected to source current for the twenty-second and twenty-fifth FETs; and,

a second differential amplifier interposed between the transistors pairs.

11. The charge-pump of claim 10 wherein the second impedance enhancement circuit includes:

a twenty-eighth FET having a drain connected to the second and third resistor second terminals;

a twenty-ninth FET having a drain connected to the twenty-eighth FET source, a source connected to the reference voltage supply (Vss), and a gate connected to the first bias voltage (Vbias1);

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- a thirtieth FET having a drain connected to the fourth and fifth resistor second terminals;
- a thirty-first FET having a drain connected to the thirtieth FET source, a source connected to the reference voltage supply (Vss), and a gate connected to the first bias voltage (Vbias1); and,
- wherein the second differential amplifier includes a positive input (Vin+) connected to the source of the thirtieth FET, a negative input (Vin-) connected to the source of the twenty-eighth FET, a positive output (V+) connected to the gate of the twenty-eighth FET, and a negative output (V-) connected to the gate of the thirtieth FET.
12. The charge-pump of claim 11 wherein the second differential amplifier includes:
- a thirty-second FET having a source connected to the first power supply (Vdd) and a gate connected to the second bias voltage (Vbias2);
  - a thirty-third FET having a drain connected to the drain of the thirty-second FET and the gate of the twenty-eighth FET (V+), and a gate connected to the drain of the thirty-first FET (Vin+);
  - a thirty-fourth FET having a source connected to the first power supply (Vdd) and a gate connected to the second bias voltage (Vbias2);
  - a thirty-fifth FET having a drain connected to the drain of the thirty-fourth FET and the gate of the thirtieth FET (V-), a gate connected to the drain of the twenty-ninth FET (Vin-), and a source connected to the source of the thirty-third FET;
  - a thirty-sixth FET having a source connected to the first power supply (Vdd) and a drain connected to its gate;
  - a thirty-seventh FET having a drain connected to the drain of the thirty-sixth FET, a gate connected to the third bias voltage (Vcmn), and a source connected to the source of the thirty-third FET; and,
  - a thirty-eighth FET having a drain connected to the source of the thirty-third FET, and gate connected to a fourth bias voltage (Vbias4), and a source connected to the reference voltage (Vss).
13. The charge-pump of claim 12 wherein the first differential section further includes:
- a third capacitor with a first terminal connected to the drain of the fifth FET and a second terminal connected to ground; and,
  - a fourth capacitor with a first terminal connected to the drain of the seventh FET and a second terminal connected to ground; and,
- wherein the second differential section further includes:
- a fifth capacitor with a first terminal connected to the drain of the ninth FET and a second terminal connected to ground; and,
  - a sixth capacitor with a first terminal connected to the drain of the eleventh FET and a second terminal connected to ground.
14. A phase-locked loop (PLL) comprising:
- a phase detector (PD) having pair of differential inputs and a pair of differential outputs (up/upb and dn/dnb);
  - a charge-pump including:
    - a first differential section including two cascaded transistor pairs, with a first unity-gain operational amplifier (op amp) interposed between the cascaded pairs, an output (Vout+) connected to a first loop filter input, and where each transistor is connected to a

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- corresponding one of the pair of differential phase detector outputs (up/upb and dn/dnb);
- a second differential section including two cascaded transistor pairs, with a second unity-gain op amp interposed between the cascaded pairs, an output (Vout-) connected to a second loop filter input, differential to the first loop filter input (Vout+), and where each transistor is connected to a corresponding one of the pair of differential phase detector outputs (up/upb and dn/dnb);
  - a first impedance enhancement circuit sourcing current for the first and second differential sections;
  - a common-mode feedback circuit having differential inputs connected to the first and second differential section outputs (Vout+/Vout-), and an output (Vcmfb); and,
  - a common-mode feedback stabilizing filter interposed between common-mode feedback circuit output (Vcmfb) and the first and second differential section outputs (Vout+/Vout-);
  - a loop filter having differential ports connected to the charge-pump first and second differential section outputs (Vout+/Vout-); and,
  - a voltage controlled oscillator (VCO) having differential inputs connected to the loop filter differential ports and a frequency output responsive to the VCO differential inputs.
15. The PLL of claim 14 wherein the first impedance enhancement circuit includes:
- a cascaded transistor pair connected to source current for the first differential section;
  - a cascaded transistor pair connected to source current for the second differential section; and,
  - a first differential amplifier interposed between the transistors pairs.
16. The PLL of claim 15 wherein the first impedance enhancement circuit includes:
- a first field effect transistor (FET) having a drain connected to the first differential section;
  - a second FET having a drain connected to the first FET source, a source connected to a reference voltage supply (Vss), and a gate connected to a first bias voltage (Vbias1);
  - a third field FET having a drain connected to the second differential section;
  - a fourth FET having a drain connected to the third FET source, a source connected to the reference voltage supply (Vss), and a gate connected to the first bias voltage (Vbias1); and,
- wherein the first differential amplifier includes a positive input (Vin+) connected to the source of the third FET, a negative input (Vin-) connected to the source of the first FET, a positive output (V+) connected to the gate of the first FET, and a negative output (V-) connected to the gate of the third FET.
17. The PLL of claim 16 wherein the common-mode feedback stabilizing filter includes:
- a first capacitor having a first terminal connected to the first differential section output (Vout+);
  - a second capacitor having a first terminal connected to the second differential section output (Vout-) and a second terminal connected to the first capacitor second terminal; and,

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a first resistor having a first terminal connected to the second terminals of the first and second capacitors and a second terminal connected to the common-mode feedback circuit output ( $V_{cmfb}$ ).

18. In a phase-locked loop (PLL) including a phase detector, a charge-pump, and a loop filter, a method for conditioning the phase detector output, the method comprising:

accepting a pair of differential phase detector (PD) output signals (up/upb and dn/dnb);

connecting each pair of differential PD outputs to first and second charge-pump differential sections;

supplying differential charge-pump outputs ( $V_{out+}/V_{out-}$ ) in response to the pair of differential PD output signals; and,

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ceasing current flow between the charge-pump differential section outputs and the loop filter inputs when the PD differential outputs (up/dn and upb/dnb) are equal.

19. The method of claim 18 wherein supplying differential charge-pump outputs ( $V_{out+}/V_{out-}$ ) in response to the pair of differential PD output signals includes sourcing a first current through the first charge-pump differential section and sourcing a second current through the second charge-pump differential section; and,

the method further comprising:

maintaining the first current equal to the second current.

20. The method of claim 18 further comprising:

mode feedback stabilizing the differential charge-pump outputs ( $V_{out+}/V_{out-}$ ) through a shared resistor.

\* \* \* \* \*





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**Perry**

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(45) **Date of Patent:** **Dec. 14, 2004**

(54) **SYNCHRONOUS RECTIFIER DRIVE  
CIRCUIT AND POWER SUPPLY INCLUDING  
SAME**

(75) **Inventor:** **Marty Perry, Tucson, AZ (US)**

(73) **Assignee:** **Artesyn Technologies, Inc., Boca  
Raton, FL (US)**

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Nov. 20, 2000, now Pat. No. 6,570,268.

(51) **Int. Cl.<sup>7</sup>** ..... **H00M 3/335**

(52) **U.S. Cl.** ..... **363/21.06; 363/17; 363/21.14;  
363/26; 363/127**

(58) **Field of Search** ..... **363/17, 21.06,  
363/21.14, 26, 65, 67, 68, 89, 127**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,274,539 A \* 12/1993 Steigerwald et al. .... 363/20  
5,625,541 A 4/1997 Rozman  
5,663,877 A 9/1997 Dittli et al.  
5,999,417 A 12/1999 Schlecht  
6,011,703 A 1/2000 Boylan et al.  
6,061,255 A 5/2000 Chik et al.

6,069,804 A 5/2000 Ingman et al.  
6,091,616 A 7/2000 Jacobs et al.  
6,130,828 A \* 10/2000 Rozman ..... 363/21.06  
6,169,683 B1 1/2001 Farrington  
6,188,592 B1 2/2001 Farrington et al.  
6,256,214 B1 7/2001 Farrington et al.  
6,288,920 B1 9/2001 Jacobs et al.  
6,297,970 B2 10/2001 Hemen et al.  
6,330,169 B2 12/2001 Mullett et al.  
6,342,737 B1 1/2002 Brodeur  
6,370,044 B1 4/2002 Zhang et al.  
6,490,183 B2 \* 12/2002 Zhang ..... 363/89  
6,535,400 B2 3/2003 Bridge  
6,570,268 B1 \* 5/2003 Perry et al. .... 307/38  
6,671,193 B1 \* 12/2003 Pelkonen ..... 363/53  
6,747,880 B2 \* 6/2004 Grover ..... 363/21.06

\* cited by examiner

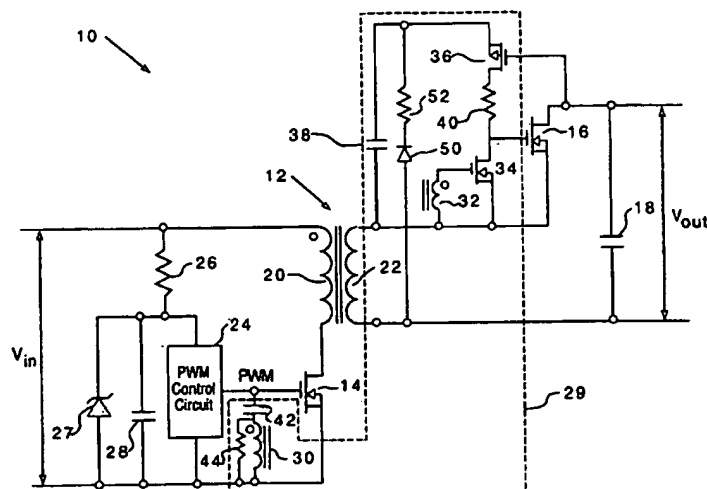
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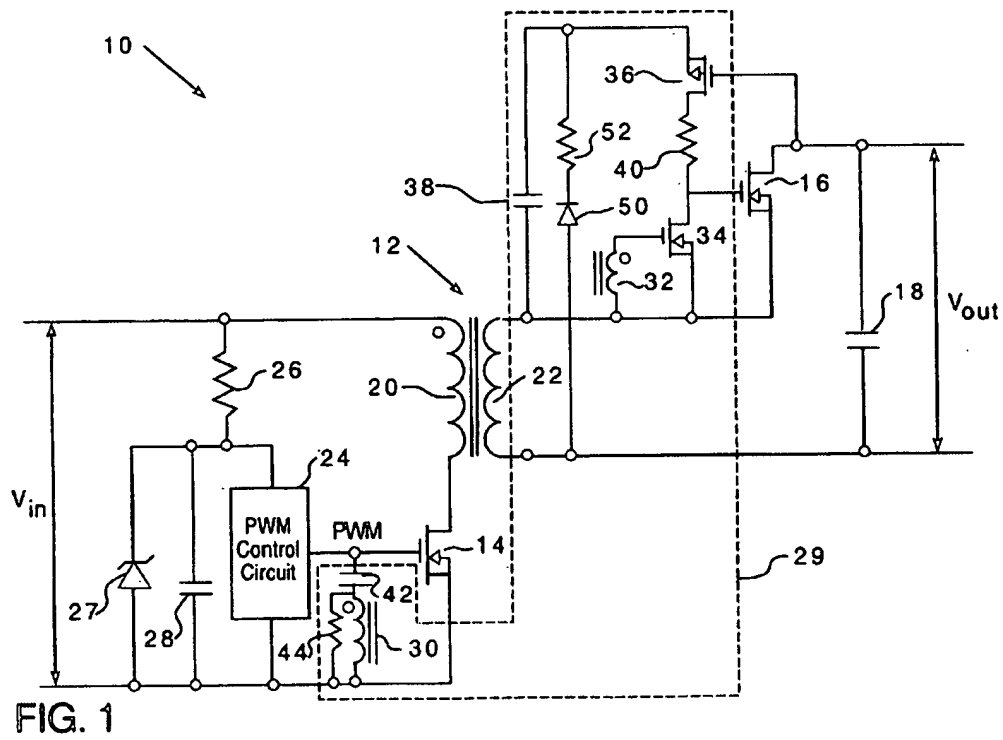
(74) *Attorney, Agent, or Firm*—Kirkpatrick & Lockhart  
LLP

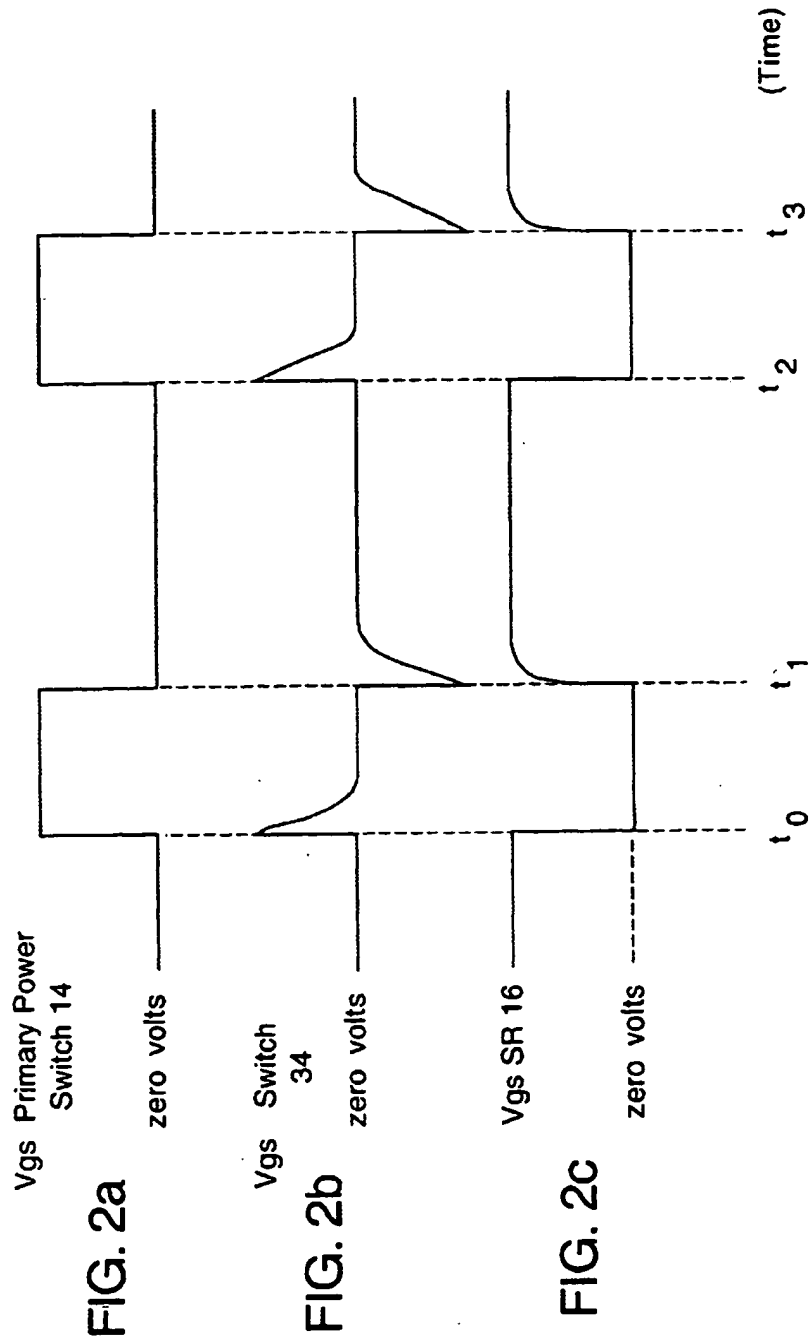
(57) **ABSTRACT**

A drive circuit for a synchronous rectifier of a switch mode power converter is disclosed. The switch mode power converter may include a main power transformer and a primary switch for cyclically coupling the main power transformer to an input source. The drive circuit may comprise a turn-on switch, a turn-off switch, a charge pump and a pulse transformer. The charge pump may be coupled to a secondary winding of the main power transformer. The turn-on switch is for turning on the synchronous rectifier and may be coupled to the charge pump. The pulse transformer may include primary and secondary windings, wherein the primary winding is responsive to a control signal supplied to the primary switch. The turn-off switch is for turning off the synchronous rectifier and may include a control terminal coupled to the secondary winding of the pulse transformer.

**20 Claims, 9 Drawing Sheets**







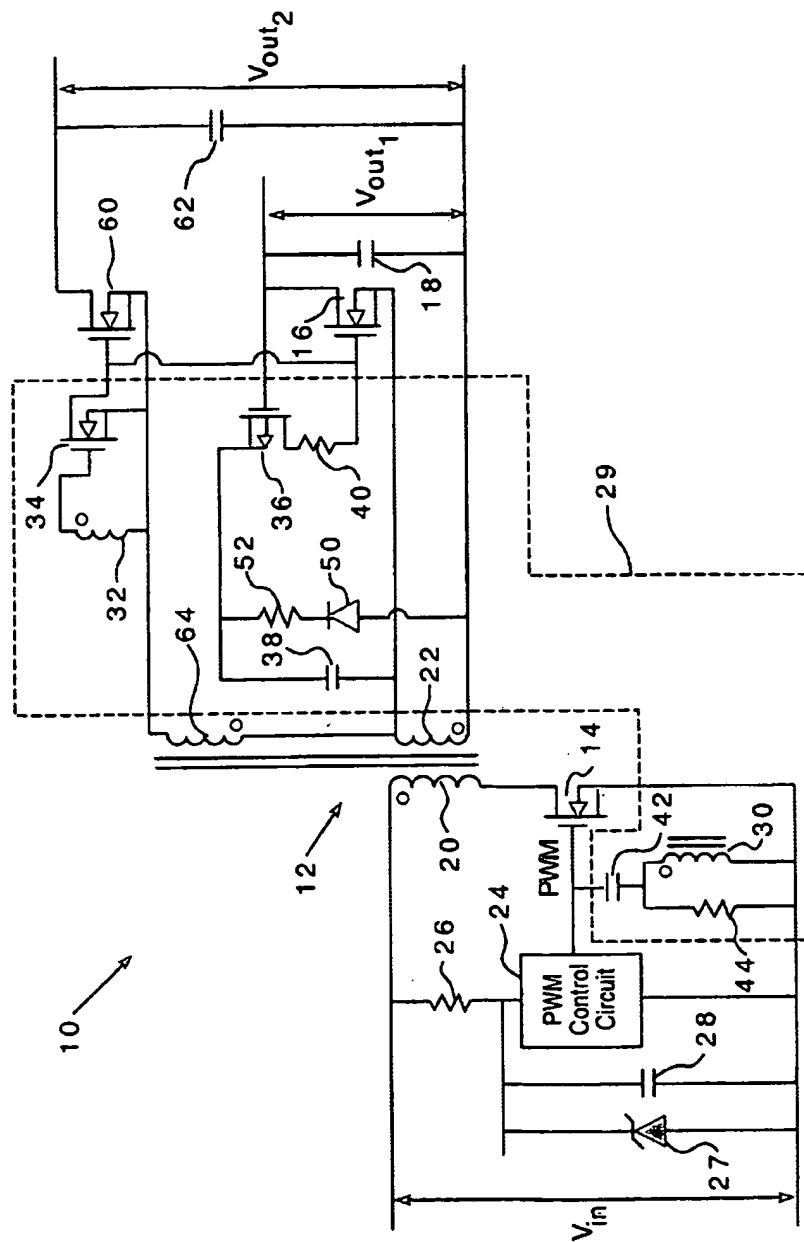


FIG. 3

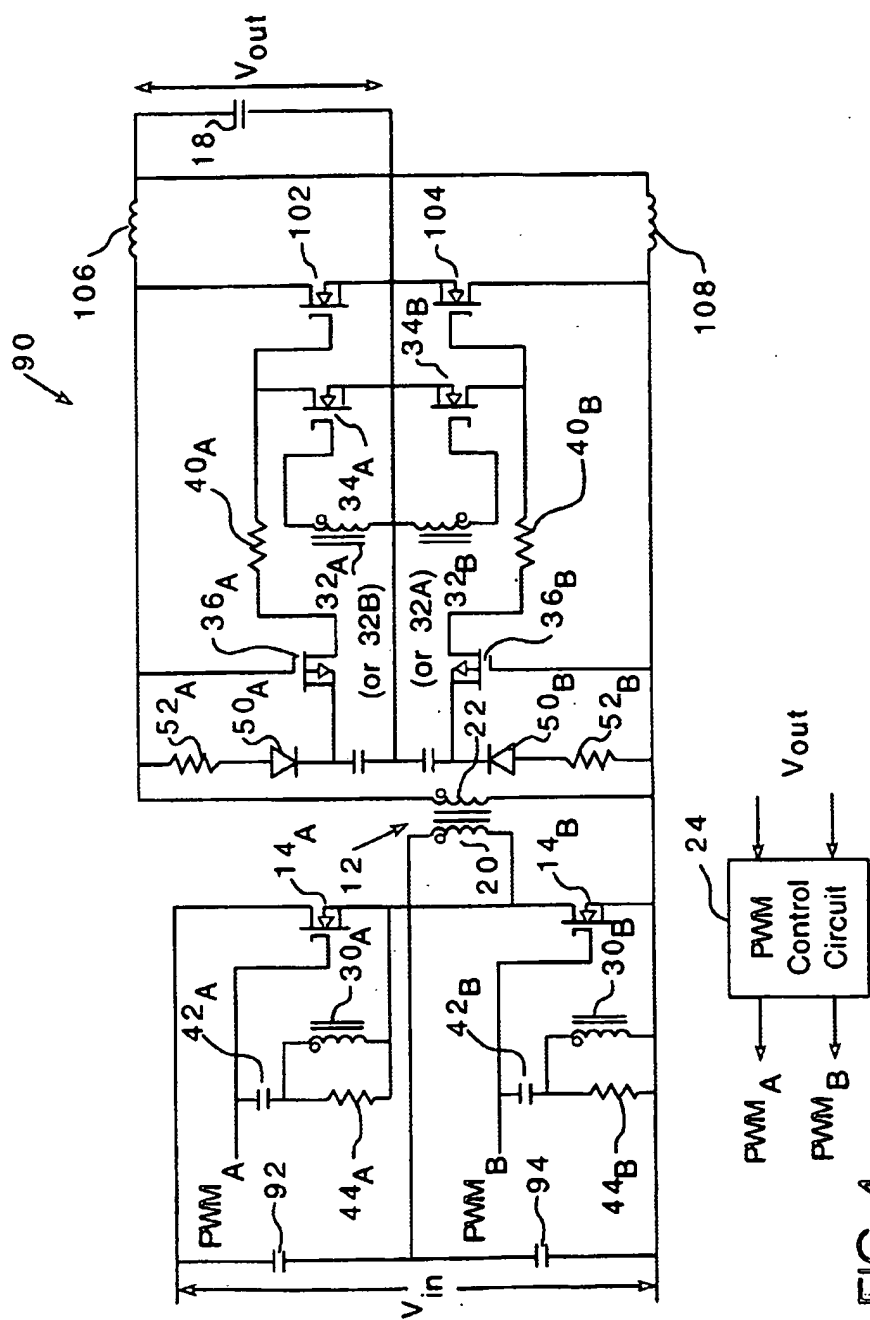


FIG. 4

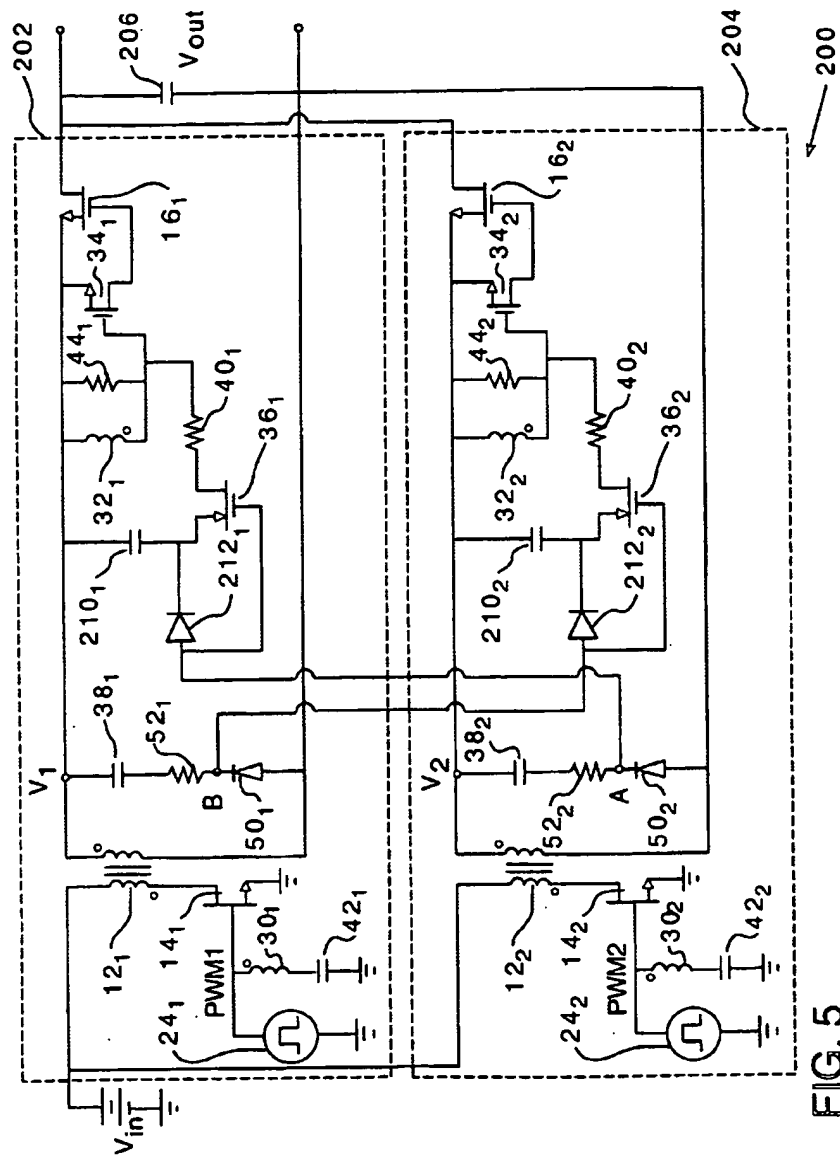
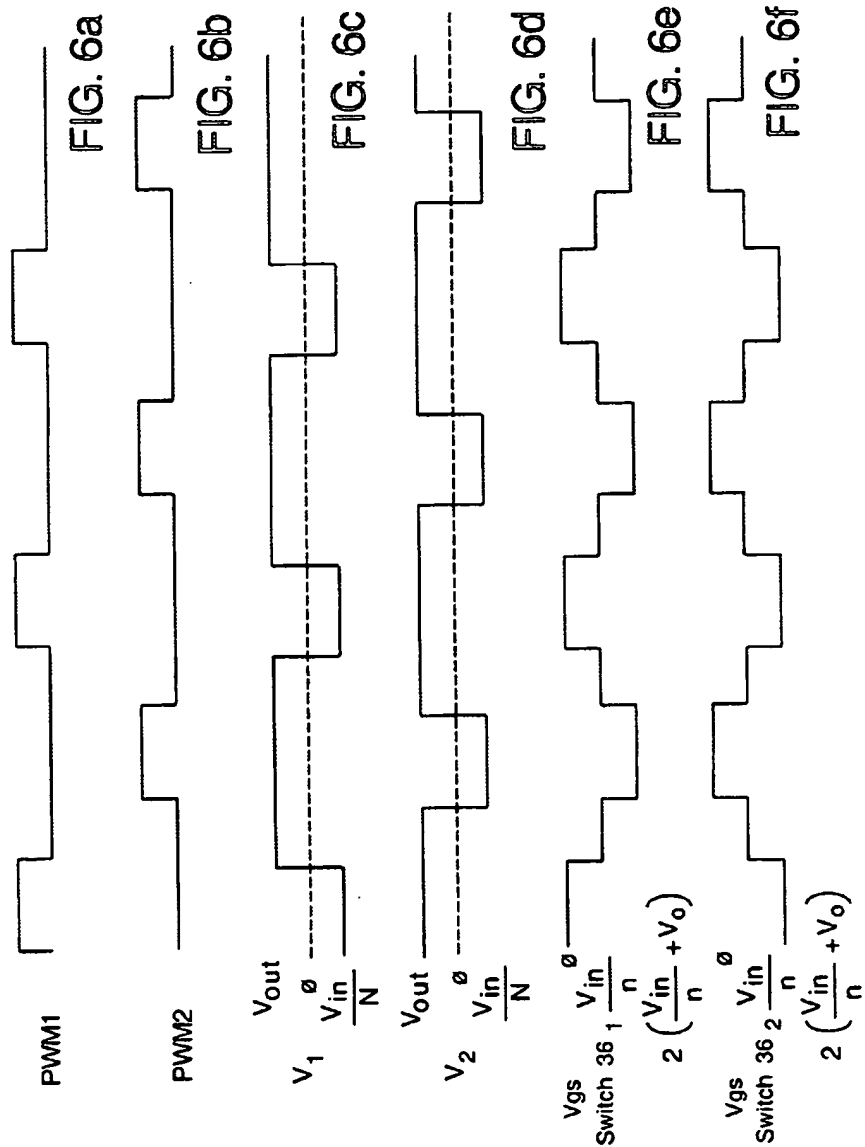


FIG. 5



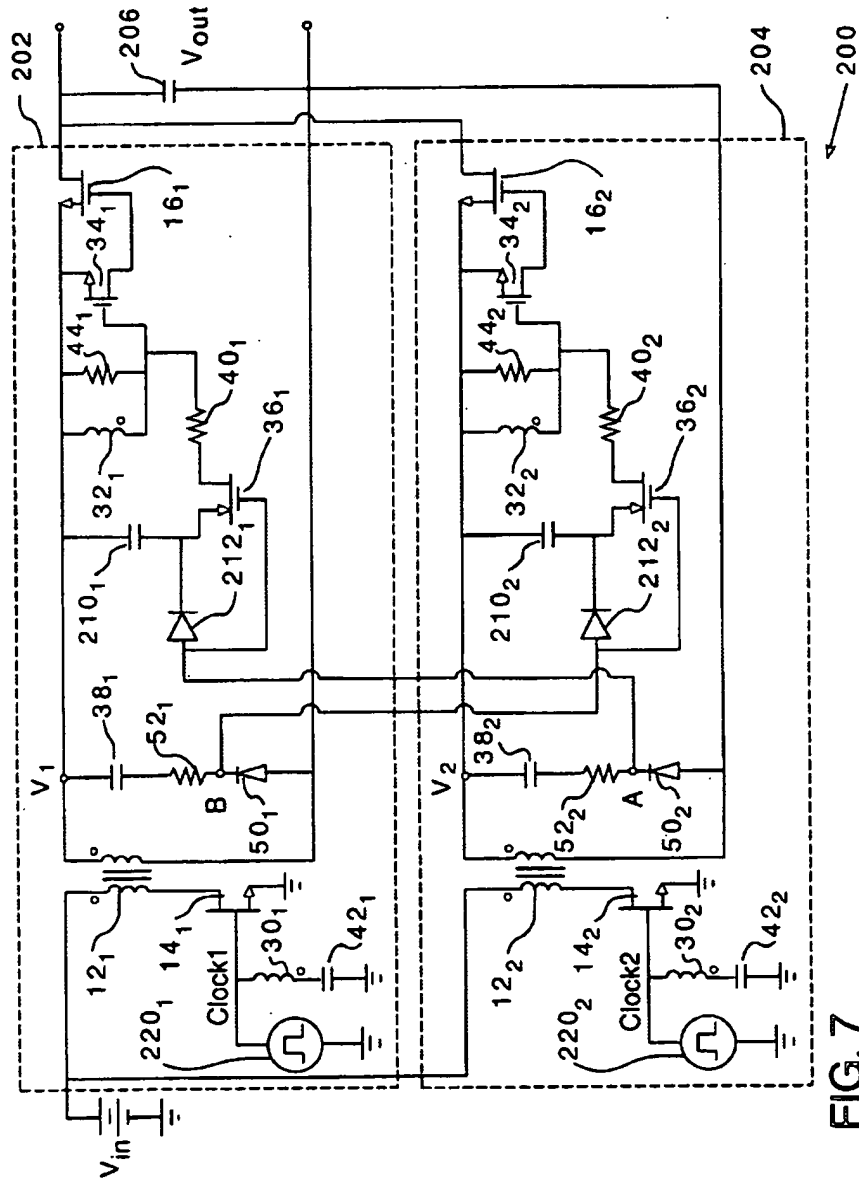


FIG. 7



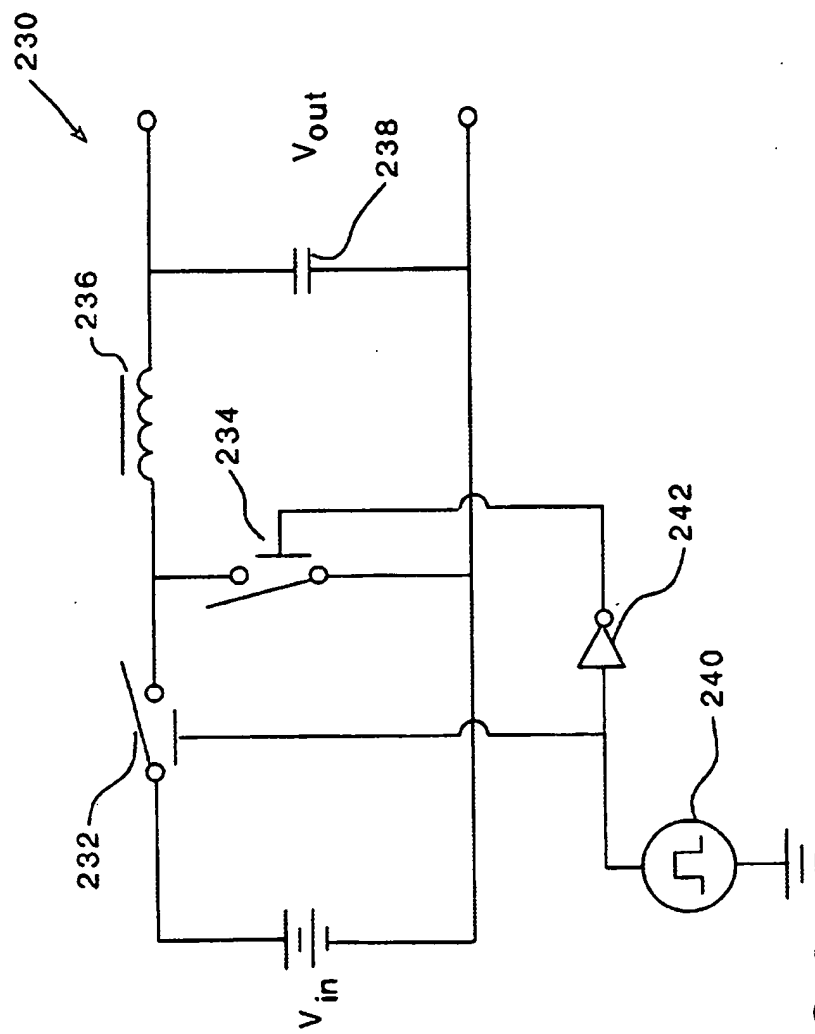


FIG. 8

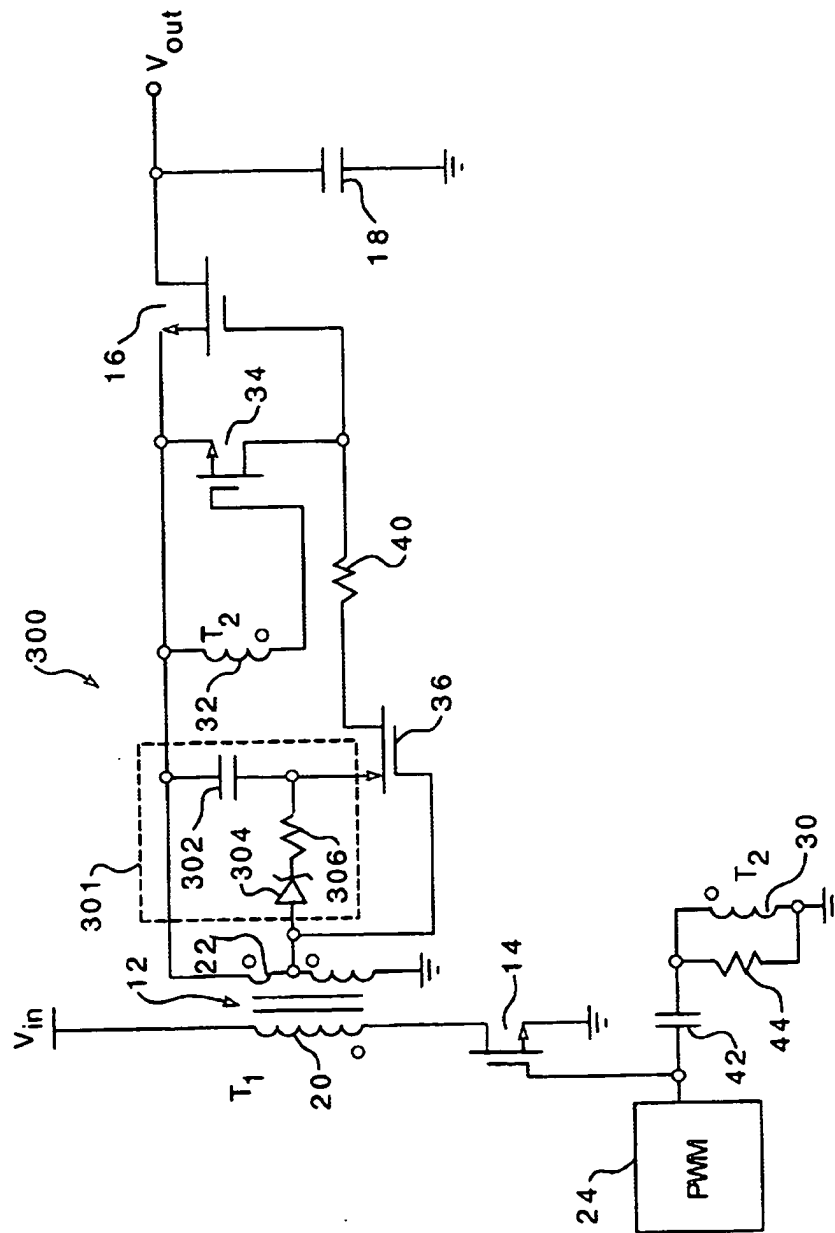


FIG. 9

# **SYNCHRONOUS RECTIFIER DRIVE CIRCUIT AND POWER SUPPLY INCLUDING SAME**

This application is a continuation-in-part of Ser. No. 09/716,506 filed Nov. 20, 2000 now U.S. Pat. No. 6,570,268.

## **BACKGROUND OF INVENTION**

### **1. Field of Invention**

The present invention relates generally to power conversion electronics and, more particularly, to synchronous rectifier drive circuits.

### **2. Description of the Background**

DC-to-DC power converters are power processing circuits which convert an unregulated input DC voltage to a regulated DC output voltage. Switch-mode DC-to-DC power converters typically include an inverter, a transformer having a primary winding coupled to the inverter, and a rectifying circuit coupled to a secondary winding of the transformer. The inverter typically includes a switching device, such as a field effect transistor (FET), that converts the DC input voltage to an alternating voltage, which is magnetically coupled from the primary winding of the transformer to the secondary winding. The rectifying circuit rectifies the alternating voltage on the secondary winding to generate a desired DC output voltage.

It is known to use synchronous rectifiers (SRs) employing metal-oxide-semiconductor field effect transistors (MOSFETs) to convert the alternating voltage of the secondary winding to the unipolar DC output voltage. The advantage of synchronous rectification is that the forward voltage drop, and hence the power loss, across a MOSFET SR is much less than that of diode devices used in the rectifying circuit. Such SR circuits, however, typically require gate drive circuitry to render the MOSFET at a low resistance during forward conduction and, more importantly, to render it non-conductive during reverse bias. This is because, unlike a diode, a SR may be conductive in both directions (i.e., forward and reverse). Thus, if not properly controlled, reverse current can flow through a MOSFET SR, thereby negatively affecting the efficiency of the power converter.

One known technique to control the gate drive of a MOSFET SR is to couple the alternating voltage from the secondary winding of the transformer to the gate terminal of the MOSFET SR to thereby turn the device on and off in response to the voltage across the secondary winding. This scheme is commonly referred to as "self-driven synchronous rectification." Although usually effective, it is possible that when the voltage on the secondary winding reverses and the gate terminal of the SR is driven off, a delay in turn-off of the SR will provide a period of reverse current in the SR. This has a deleterious "shorting" effect on the secondary winding, which may limit the turn off voltage and further delay commutation of the SR. Additionally, it is difficult to generate the proper on-state SR bias level in the self-driven configuration.

Further drawbacks with self-driven SR schemes exist. Self-driven circuits typically do not provide sufficiently fast turn-on and turn-off the SR. Rather, self-driven circuits typically provide slowly rising and slowly falling gate signals that transition the SR through a linear region during which  $I^2R$  losses are more significant. In addition, self-driven circuits do not achieve optimal timing. That is, for one, the turn-on current is not applied immediately after the

SR becomes biased to conduct such that any conduction of the internal body diode of the SR is minimized, thereby reducing losses. This is because self-driven circuits rely on the winding voltage to turn on, and during the rise of current in the SR the winding voltage may be reduced by leakage inductance in the transformer. Also, proper timing of the SR suggests that the gate of the SR be discharged a small delay period before the voltage reverses across the SR. The delay period provides for the turn off time of the SR and ensures that the device is off when reverse bias is applied, preventing any flow of reverse current. Self-driven circuits, however, use the reverse bias voltage itself to initiate turn off and, therefore, no delay is possible. Thus, during the turn off time of the SR, reverse current may flow.

Additionally, self-driven circuits often do not provide a suitable gate voltage to the SR. Ideally, when turning the SR ON, the gate of the SR should receive sufficient voltage to lower the on resistance of the SR to the minimum value. But the gate voltage should not be so high as to damage the gate of the SR. In addition, the source of the voltage for the drive circuit should be referenced to the control terminal (i.e., gate) of the SR and should be able to supply a high pulse current. Self-driven circuits, however, require that the configuration of the SRs be adapted to match the available winding voltage. Further, the pulse current from the windings may be limited by the leakage inductance of the transformer. Furthermore, self-driven circuits apply the winding voltage directly to the gate of the SR. This voltage must be scaled to the converter output voltage, which may be either insufficient or extreme for the gate of the SR.

One known technique to overcome the shortcomings of self-driven synchronous rectifiers is to employ a gate drive circuit coupled to the control terminal of the synchronous rectifier (SR). Gate drive circuits, however, are complicated to implement, thus reducing reliability and increasing cost. Further, conventional gate drive circuits often do not overcome all of the drawbacks identified above for self-driven circuits, such as rapid turn on and turn off, proper timing, suitable gate voltage. In addition, it is difficult to implement a gate drive circuit driven by the alternating voltage of the transformer that is capable of driving two synchronous rectifiers of a dual output power converter or provide the proper bias levels in low voltage output converters.

Accordingly, there exists a need in the art for a SR gate drive circuit that achieves rapid turn on and turn off of the SR so as to reduce, and even obviate, the delay in turn-off of a SR, to thereby minimize, or eliminate, any period of reverse conduction of the SR and the subsequent shorting effect. There further exists a need for a gate drive circuit that is capable of providing the required SR bias level, even for low output converters.

## **SUMMARY OF THE INVENTION**

In one general aspect, the present invention is directed to a drive circuit for a synchronous rectifier (SR) for a switch mode power converter. The power converter may include, as switch mode power converters do, a main power transformer and a primary switch for cyclically coupling an input source to the main power transformer. The primary switch may be controlled by a control signal, such as according to a pulse width modulation (PWM) scheme. The SR is for rectifying a voltage across the secondary of the main power transformer.

According to one embodiment, the drive circuit includes turn-on and turn-off switches, a charge pump and a pulse transformer. The turn-on switch is for turning on the SR

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during the intended time period of forward conduction. The turn-off switch is for turning off the SR. The charge pump is coupled to a secondary winding of the main power transformer and is used to provide drive and a power supply for the turn-on switch. The pulse transformer includes primary and secondary windings, wherein the primary winding is responsive to the control signal supplied to the primary switch and the secondary winding of the pulse transformer is coupled to the control terminal of the turn-off switch. The charge pump shifts the winding voltage to an appropriate reference level for the control terminal of the SR. The number of turns on the secondary winding of the main power transformer can be adapted to match the charge pump output to the requirement of the SR gate. That is, the drive voltage of the charge pump may be higher or lower than the converter output.

As will be apparent from the following description, embodiments of the present invention provide a SR drive circuit that achieves rapid turn on and turn off, with proper timing, and with a suitable voltage level for the SR, with simplicity that increases reliability and decreases cost. For example, the drive circuit of the present invention provides an advantage over prior art self-driven synchronous rectification schemes because it provides a manner for eliminating delay in the turn-off of a synchronous rectifier, thus providing the advantage of eliminating the shorting effect of the secondary winding of the transformer. Embodiments of the present invention also provide the advantage of having a mechanized synchronous rectifier turn-on system operable at, for example, low output voltages.

According to another embodiment, the present invention is directed to a power converter including the drive circuit for a synchronous rectifier. The power converter may be any type of power converter including a synchronous rectifier including but not limited to forward converters, flyback converters, and double ended converters such as, for example half-bridge converters, full-bridge converter and push-pull converters.

#### DESCRIPTION OF THE FIGURES

For the present invention to be clearly understood and readily practiced, embodiments of the present invention will be described in conjunction with the following figures, wherein:

FIG. 1 is a schematic diagram of a power converter circuit according to one embodiment of the present invention;

FIGS. 2a-c are voltage waveform diagrams illustrating the operation of the power converter circuit of FIG. 1 according to one embodiment of the present invention;

FIG. 3 is a schematic diagram of a power converter circuit according to another embodiment of the present invention;

FIG. 4 is a schematic diagram of a power converter circuit according to another embodiment of the present invention;

FIG. 5 is a schematic diagram of a power supply according to another embodiment of the present invention;

FIGS. 6a-f are voltage waveform diagrams illustrating the operation of the power supply of FIG. 5 according to one embodiment of the present invention;

FIG. 7 is a schematic diagram of a power supply according to another embodiment of the present invention;

FIG. 8 is a schematic diagram of a synchronous buck converter that may be used in conjunction with the power supply of FIG. 7 according to one embodiment of the present invention; and

FIG. 9 is a schematic diagram of a power supply according to another embodiment of the present invention.

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#### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic diagram of a power converter circuit 10 according to one embodiment of the present invention. The power converter circuit 10 includes an isolation transformer 12, a primary power switch 14, a synchronous rectifier (SR) 16, and an output capacitor 18. The SR may be, for example, a MOSFET, such as an n-channel MOSFET as illustrated in FIG. 1. The isolation transformer includes a primary winding 20 and a secondary winding 22. The primary power switch 14 may be, for example, a transistor, such as an n-channel MOSFET as illustrated in FIG. 1. The primary power switch 14 cyclically couples the input voltage ( $V_{in}$ ) from a voltage source (not shown) to the primary winding 20 of the transformer 12 to generate an alternating voltage at the secondary winding 22. This alternating voltage is converted to a DC voltage by the SR 16, producing a filtered DC output voltage ( $V_{out}$ ) across the output capacitor 18, which is used to power a load (not shown).

The duty cycle of the primary power switch 14 is controlled by a pulse width modulated (PWM) signal output from a PWM control circuit 24. When the primary power switch 14 is closed, i.e., when the PWM signal drives the primary power switch 14 into conduction, the input voltage  $V_{in}$  is coupled to the primary winding 20, causing current in the primary winding 20 to increase linearly and causing energy to be stored within the transformer 12. During this time period, the SR 16 is non-conductive, as described further hereinbelow, and the output capacitor 18 supplies the load current. Accordingly, the output capacitor 18 may be chosen to have a capacitance large enough in order that it provides sufficient load current during the period that the SR 16 is non-conductive.

When the primary power switch 14 is opened, i.e., when the PWM signal drives the primary switch 14 into non-conduction, the energy stored in the transformer 12 is transferred to the secondary of the power converter circuit 10. The SR 16 is turned on, as discussed hereinbelow, causing load current to flow through the SR 16. The secondary current of the power converter 10, i.e., the forward current through the SR 16, decreases linearly until this interval terminates as determined by the particular operating point of the converter 10.

Accordingly, by regulating the duty cycle of the PWM signal, the output voltage  $V_{out}$  may be controlled. According to one embodiment, the PWM control circuit 24 may be responsive to the output voltage  $V_{out}$  and regulate the PWM signal based on the output voltage  $V_{out}$  to realize a desired output. As illustrated in FIG. 1, the PWM control circuit 24 may receive power from the input voltage  $V_{in}$  via a resistor 26, which may be regulated by a Zener diode 27 and filtered by a capacitor 28.

Conduction of the SR 16 is controlled by a gate drive circuit 29. According to one embodiment, as illustrated in FIG. 1, the gate drive circuit 29 includes a pulse transformer, having a primary winding 30 magnetically coupled to a second winding 32, but which are shown detached in FIG. 1 for clarity. The gate drive circuit 29 also includes a turn-off switch 34 and a turn-on switch 36. Both switches 34, 36 may be transistors such as, for example, MOSFETs. According to one embodiment, as illustrated in FIG. 1, the switch 34 may be an n-channel MOSFET and the switch 36 may be a p-channel MOSFET. According to other embodiments described below, the drive circuit may include a charge pump for driving the turn-on switch 36. The SR drive circuit described herein may be used in any type of converter topology employing a synchronous rectifier(s).

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The switch 34 may provide a conduction path between the secondary winding 22 of the isolation transformer 12 and the gate terminal of the SR 16. In addition, the control terminal of the switch 34 may be coupled to the secondary winding 32 of the pulse transformer. The switch 36 may also provide a conduction path between the secondary winding 22 of the isolation transformer 12 and the gate terminal of the SR 16, although a capacitor 38 may be provided between the secondary winding 22 and the switch 36, and a resistor 40 may be provided between the switch 36 and the gate terminal of the SR 16. The control terminal of the switch 36 may be coupled to the drain terminal of the SR MOSFET 16.

The primary winding 30 of the pulse transformer may be pulsed with the PWM signal from the PWM control circuit 24 via a capacitor 42. In addition, a resistor 44 may be shunt loaded with the primary winding 30. The capacitor 42 and resistor 44 may form a differentiator circuit, discussed further hereinbelow.

The operation of the gate drive circuit 29 of FIG. 1 will be discussed in conjunction with the idealized voltage waveform diagrams of FIGS. 2a-c. FIG. 2a is a diagram showing the gate-source voltage of the primary power switch 14. FIG. 2b is a diagram showing the gate-source voltage of the switch 34. FIG. 2c is a diagram showing the gate-source voltage of the SR 16. The duty cycle of the PWM signal is  $(t_1 - t_0)/(t_2 - t_0)$ .

According to one embodiment, when the primary power switch 14 is closed, the capacitor 38 is charged to  $V_{in}/N$ , where  $N$  is the turns ratio of the transformer 12. When the primary power switch 14 is opened at  $t_1$ , the polarity of the voltage at the secondary winding 22 of the transformer 12 will reverse. This will forward bias the intrinsic body diode of the SR 16 and cause the switch 36 to conduct, thereby driving the gate terminal of the SR 16 to turn on the SR 16.

When the primary power switch 14 is then turned on at  $t_2$  by the PWM signal of the PWM control circuit 24, the PWM signal is differentiated by the differentiator circuit comprising the capacitor 42 and the resistor 44, and the differentiated PWM signal is applied to the primary winding 30 of the pulse transformer. The switch 34 is therefore instantaneously turned on by the voltage across the secondary winding 32 of the pulse transformer. The turning-on of the switch 34 turns off the SR 16 and shunts drive current from the switch 36, limited by the resistor 40, away from the gate terminal of the SR 16. In this interval, the primary power switch 14 turns on, causing the voltage on the primary winding 20 of the isolation transformer 12 to reverse.

Subsequently, the voltage at the secondary winding 22 reverses, and because the SR 16 has been turned off, the possibility of reverse current through the SR 16 is eliminated and shorting of the secondary winding 22 is prevented. As reverse voltage appears across the SR 16, the switch 36 may be turned off, thus removing the drive current from the gate terminal of the SR 16 and limiting further dissipation in the resistor 40. With the switch 36 turned off, no drive is available for the SR 16, and the switch 34 is turned off by the decay of the differential pulse at its gate terminal.

The values of the capacitor 42 and the resistor 44 of the differentiator circuit may be chosen such that the differential time constant provided by the differentiator circuit is long enough to keep the switch 34 turned on during the switching interval, but short enough to significantly reduce the volt-second product applied across the pulse transformer.

According to one embodiment, as illustrated in FIG. 1, power for the gate drive circuit 29 may be derived from the secondary winding 22 of the isolation transformer 12

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through a diode 50 and a resistor 52. Drive energy may be stored in the capacitor 38, allowing the on-time of the SR 16 to be non-responsive to the magnitude of the voltage at the secondary winding 22. Consequently, in contrast to prior art self-driven synchronous rectification schemes, the present invention does not use the secondary voltage to directly drive the SR 16. According to another embodiment, a bias voltage supply may be used to provide steady drive power to the SR 16.

FIG. 3 is a schematic diagram of the power converter circuit 10 according to another embodiment of the present invention. The power converter circuit 10 illustrated in FIG. 10 is similar to that of FIG. 1, except that it provides a dual output ( $V_{out1}$  and  $V_{out2}$ ). The illustrated embodiment includes a second SR 60 and a second output capacitor 62. In addition, the transformer 12 may include a second secondary winding 64. The second SR 60 may be, for example, a MOSFET, as illustrated in FIG. 3.

The cyclic switching of the primary power switch 14 additionally generates an alternating voltage across the second secondary winding 64. This alternating voltage is converted to a DC voltage by the second SR 60, producing a filtered DC output voltage ( $V_{out2}$ ) across the output capacitor 62 to power a second load (not shown).

The gate drive circuit 29 described hereinbefore may drive each of the SRs 16, 60. According to such an embodiment, the gate terminal of the second SR 60 may be coupled to the gate terminal of the first SR 16. Consequently, as described hereinbefore with respect to FIGS. 1 and 2, as a reverse voltage appears across the SR 60 due to the polarity of the second secondary winding 64, the switch 36 may be turned off, thus removing the drive current from the gate terminal of the SR 60. With the switch 36 turned off, no drive is available for the SR 60, and the switch 34 is turned off by the decay of the differential pulse at its gate terminal.

The power converter circuit 10 of FIGS. 1 and 3 utilizes a flyback topology. Benefits of the gate drive circuit 29 of the present invention, however, may be realized with other types of power conversion topologies. For example, FIG. 4 is a schematic diagram of a half-bridge power converter circuit 90 with a current doubler including a gate drive circuit according to an embodiment of the present invention. The circuit 90 includes two series-connected capacitors 92, 94 connected across the input voltage source ( $V_{in}$ ). The primary winding 20 of the isolation transformer 12 may be coupled between a common node the two capacitors 92, 94 and a common node of the two primary input power switches 14<sub>A</sub>, 14<sub>B</sub>.

The secondary of the circuit 90 includes two SRs 102, 104, which may be, for example, MOSFETs as illustrated in FIG. 4. The SRs 102, 104 may alternately convert an alternating voltage across the secondary winding 22 of the isolation transformer 12 to produce a regulated DC output voltage  $V_{out}$  across the output capacitor 18. A pair of output inductors 106, 108, in conjunction with the output capacitor 18, may filter the DC voltages generated by the SRs 102, 104.

The illustrated half-bridge power converter circuit 90 includes two gate drive circuits to respectively control the drive supplied to each of the SRs 102, 104. Similar to the gate drive circuits described hereinbefore, the first gate drive circuit of circuit 90, which controls the gate drive for the first SR 102, may include a pulse transformer including a primary winding 30<sub>A</sub> and a secondary winding 32<sub>A</sub>. The first gate drive circuit may also include first and second switches 34<sub>A</sub> and 36<sub>A</sub> coupled by a resistor 40<sub>A</sub>. In addition, as

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discussed hereinbefore, a differentiator circuit comprising a capacitor 42<sub>A</sub> and a resistor 44<sub>A</sub> may differentiate a first PWM signal, PWM<sub>A</sub>, which controls the switching of the first primary power switch 14<sub>A</sub>.

Similarly, the second gate drive circuit, which controls the drive supplied to the second SR 104, may include a second pulse transformer including a primary winding 30<sub>B</sub> and a secondary winding 32<sub>B</sub>, a pair of switches 34<sub>B</sub> and 36<sub>B</sub> coupled by a resistor 40<sub>B</sub>, and a differentiator circuit comprising a capacitor 42<sub>B</sub> and a resistor 44<sub>B</sub>.

In a manner analogous to that described hereinbefore with respect to FIGS. 1 and 2, the first and second drive circuits may respectively prevent the SRs 102, 104 from conducting reverse current, thereby preventing the shorting effect of the secondary winding 22, except that for a half-bridge configuration, as illustrated in FIG. 4, the SRs 102, 104 may be turned off only during the interval that the opposite primary power switches 14<sub>A</sub>, 14<sub>B</sub> are turned on. That is, the SR 102 may be turned off only for the interval that primary power switch 14<sub>B</sub> is turned on, and the SR 104 may be turned off only for the interval that primary power switch 14<sub>A</sub> is turned on. This may be realized in the half-bridge circuit 90 because the secondary winding 22 of the isolation transformer 12 has the same polarity as the primary winding 20.

Power for each of the gate drive circuits may be derived from the secondary winding 22 of the isolation transformer 12, for the first gate drive circuit, through a diode 50<sub>A</sub> and a resistor 52<sub>A</sub>, and for the second gate drive circuit, through a diode 50<sub>B</sub> and a resistor 52<sub>B</sub>.

FIG. 5 is a diagram of a power supply 200 according to another embodiment of the present invention. The power supply 200 illustrated in FIG. 5 includes two parallel-connected converters 202, 204. The converters 202, 204 may be, for example, flyback converters sharing a common output capacitor 206. Each converter 202, 204 may be similar to the converter 10 described hereinbefore with respect to FIG. 1, including an isolation transformer 12<sub>1,2</sub>, a primary power switch 14<sub>1,2</sub>, a synchronous rectifier 16<sub>1,2</sub>, and a PWM control circuit 24<sub>1,2</sub>. The PWM signals PWM1 and PWM2 from the respective PWM control circuits 24<sub>1,2</sub> may be, for example, 180 degrees out of phase such that the parallel-connected converters 202, 204 operate in an interleaved mode.

Similarly, each converter 202, 204 may include a gate drive circuit as described hereinbefore including, for example, a pulse transformer including a primary winding 30<sub>1,2</sub> and a secondary winding 32<sub>1,2</sub>, a differential circuit including a capacitor 42<sub>1,2</sub> and a resistor 44<sub>1,2</sub> (in FIG. 5 the resistors 44<sub>1,2</sub> are shown in parallel across the secondary windings 30<sub>1,2</sub> of the pulse transformers), switches 34<sub>1,2</sub>, 36<sub>1,2</sub>, and a resistor 40<sub>1,2</sub>. In addition, each converter 202, 204 may include a capacitor 38<sub>1,2</sub>, a resistor 52<sub>1,2</sub>, and a diode 50<sub>1,2</sub> connected across the secondary winding of the isolation transformer 12<sub>1,2</sub>.

In contrast to the converter 10 described hereinbefore, the turn-on function for the synchronous rectifiers 16<sub>1,2</sub> of the converters 202, 204 may be mechanized by use of a cross-coupled charge pump arrangement. According to one such embodiment, each converter 202, 204 may include a capacitor 210<sub>1,2</sub> and a diode 212<sub>1,2</sub>. The diode 212<sub>1</sub> may be connected between the diode 50<sub>2</sub> and the source terminal of the switch 36<sub>1</sub>. The capacitor 210<sub>1</sub> may be connected between the source terminal of the switch 36<sub>1</sub> and the secondary winding of the transformer 12<sub>1</sub>. The gate terminal of the switch 36<sub>1</sub> may also be connected to the diode 50<sub>2</sub>.

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Similarly, the diode 212<sub>2</sub> may be connected between the diode 50<sub>1</sub> and the source terminal of the switch 36<sub>2</sub>, and the capacitor 210<sub>2</sub> may be connected between the source terminal of the switch 36<sub>2</sub> and the secondary winding of the transformer 12<sub>2</sub>. The gate terminal of the switch 36<sub>2</sub> may also be connected to the diode 50<sub>1</sub>.

The charge pump for the synchronous rectifier 16<sub>1</sub> of the converter 202 may include the capacitors 38<sub>2</sub>, 210<sub>1</sub>, the diodes 50<sub>2</sub>, 212<sub>1</sub>, and the resistor 52<sub>2</sub>. Similarly, the charge pump for the synchronous rectifier 16<sub>2</sub> of the converter 204 may include the capacitors 38<sub>1</sub>, 210<sub>2</sub>, the diodes 50<sub>1</sub>, 212<sub>2</sub>, and the resistor 52<sub>1</sub>. The resistors 52<sub>1,2</sub> may provide a current limit function during the charge pump conversion intervals.

The power supply 200 of FIG. 5 may be beneficial, for example, for low output voltage applications. For example, for a low output voltage converter, the turns ratio of the isolation transformers may be sufficiently high that the appropriate drive level to forward bias the synchronous rectifier cannot be developed for all input voltage conditions of Vin. As described hereinbelow, the cross-coupled charge pump arrangement may yield the required synchronous rectifier drive levels and gating functions when using high step-down ratios as are ordinarily required for optimized low voltage output converters.

FIGS. 6a-f illustrate idealized voltage waveforms for the power supply 200 at an arbitrary operating point. FIG. 6a is a diagram of the PWM signal from the first PWM control circuit 24<sub>1</sub> (PWM1). FIG. 6b is a diagram of the PWM signal from the second PWM control circuit 24<sub>2</sub> (PWM2). FIG. 6c is a diagram of the voltage at a node (V<sub>1</sub>) in the converter 202 between the capacitor 38<sub>1</sub> and the secondary winding of the transformer 12<sub>1</sub>. FIG. 6d is a diagram of the voltage at a node (V<sub>2</sub>) in the converter 204 between the capacitor 38<sub>2</sub> and the secondary winding of the transformer 12<sub>2</sub>. FIG. 6e is a diagram of the gate-source voltage of the transistor 36<sub>1</sub>. And FIG. 6f is a diagram of the gate-source voltage of the transistor 36<sub>2</sub>.

From FIGS. 6a-f, it is recognized that when the signal PWM2 is high, the capacitor 38<sub>2</sub> is charged to a voltage of Vin/N, where N is the turns ratio of the transformers 12<sub>1,2</sub>. Subsequently, the signal PWM2 goes low prior to the signal PWM1 going high. This causes the voltage at the node "A" of the converter 204 to become (V<sub>in</sub>/N)+V<sub>out</sub>. When the signal PWM1 goes high, the capacitor 210<sub>1</sub> is charged via the capacitor 38<sub>2</sub>, the diode 212<sub>1</sub> and the transformer 12<sub>1</sub> to a value of (2V<sub>in</sub>/N)+V<sub>out</sub>. By appropriate selection of these values, this voltage may be suitable over all line conditions (i.e., input voltages Vin) and during a short circuit (i.e., V<sub>out</sub>=0) to forward bias the synchronous rectifier 16<sub>1</sub>.

Turn-on of the synchronous rectifier 16<sub>1</sub> may be accomplished by the turn-on switch 36<sub>1</sub>. During the interval where PWM1 is high, the node voltage V<sub>1</sub> is at -V<sub>in</sub>/N. Thus, the gate-source voltage (V<sub>gs</sub>) of the p-channel switch 36<sub>1</sub> equals:

$$((V_{in}/N)+V_{out})-((2V_{in}/N)+V_{out}-(V_{in}/N))=0.$$

As such, the switch 36<sub>1</sub> is in a non-conducting state. When PWM1 goes low, the voltage at node B of the converter 202 will be forced to V<sub>out</sub>. As such, the gate-source voltage (V<sub>gs</sub>) of the switch 36<sub>1</sub> will be forced to -V<sub>in</sub>/N. Thus, the switch 36<sub>1</sub> will be in a conducting state and will transfer charge from the capacitor 210<sub>1</sub> to the synchronous rectifier 16<sub>1</sub>, forcing the synchronous rectifier 16<sub>1</sub> into the conducting third quadrant state. During the interval when PWM2 goes high, the switch 36<sub>1</sub> is biased on

to the entire charge pump level of  $2(V_{in} + V_{out})$ . Because the synchronous rectifier 16<sub>1</sub> is already conductive, this has no effect in the conduction interval.

Turn-off and turn-on of the synchronous rectifier 16<sub>2</sub> may be accomplished in an analogous manner and is, therefore, not further described herein.

FIG. 7 is a diagram of the power supply 200 according to another embodiment of the present invention. The power supply 200 is similar to that of FIG. 5, except that the transformers 12<sub>1,2</sub> are forward-mode transformers and that the drive signals to the primary power switches 16<sub>1,2</sub> are supplied by first and second clock circuits 220<sub>1,2</sub> respectively. The signals from the first and second clock circuits 220<sub>1,2</sub> (CLOCK1 and CLOCK2) may be, for example, 180 degrees out of phase but with some overlapping high period. Thus, for the overlapping interval, both the transformers 12<sub>1,2</sub> deliver energy to the output at the same time. In addition, for the power supply 200 of FIG. 7, the pulse transformer sense may be reversed (i.e., the polarities of the primary windings 30<sub>1,2</sub> and the secondary windings 32<sub>1,2</sub> of the pulse transformers are the same) since the transformers 12<sub>1,2</sub> operate in the forward mode.

According to one embodiment, the input voltage  $V_{in}$  for the power supply 200 of FIG. 7 may be supplied by, for example, a synchronous buck converter, as illustrated in FIG. 8. The synchronous buck converter 230 of FIG. 8 includes two switches 232, 234, and inductor 236, and a capacitor 238. The switches 232, 234 may be, for example, transistors such as, for example, bipolar junction transistors or field effect transistors. The voltage across the capacitor 238 ( $V_{out}$ ) may be the input voltage ( $V_{in}$ ) for the power supply 200 of FIG. 7. The switches 232, 234 may be driven by PWM control circuit 240, which may be responsive to the output voltage  $V_{out}$  of the power supply 200 of FIG. 7, to thereby regulate the output voltage of the power supply 200. An inverter 242 may be connected between the PWM control circuit 240 and the switch 234 such that the switches 232, 234 are oppositely driven.

FIG. 9 is a schematic diagram of a converter 300 according to another embodiment of the present invention. The converter 300 includes a SR 16 and a drive circuit for driving the SR 16. The drive circuit includes the turn-on and turn-off switches 36, 34, the pulse transformer comprising windings 30 and 32, and a charge pump circuit 301, comprising capacitor 302 and diode 304. The converter 300 illustrated in FIG. 9 is a flyback converter, although the drive circuit for driving the synchronous rectifier 16 may be used in other converter topologies including, but not limited to, forward converters, half-bridge converters, full-bridge converter and push-pull converters.

In operation, similar to the operation of the converter described previously in connection with FIG. 1, at the instant the primary switch 14 is turned ON by the PWM control circuit 24, the turn-off switch 34 of the drive circuit is driven to conduction by the pulse transformer (windings 30, 32), and SR 16 is turned OFF. The resistor 40 connected to the drains of the turn-on switch 36 and the turn-off switch 34 limits cross-conduction between the two switches 34, 36 that may result if both switches are simultaneously ON. The operation is described previously in paragraphs 23 and 24. The switching operation of the turn-off switch 34 is described previously, such as at paragraphs 23–25. Subsequently, the voltage on the secondary winding 22 reverses and the SR 16 is then OFF to block reverse current flow. During this period, the diode 304 conducts to charge the charge pump capacitor 302 to the secondary winding voltage. When the primary switch 14 is turned OFF by the control circuit 24, the voltage on the secondary winding 22 begins to reverse again; the pulse transformer is inactive during this time. As the secondary winding 22 voltage rises, the charge pump capacitor 302 carries the source terminal of

the turn-on switch 36 to a voltage above the output voltage ( $V_{out}$ ). The gate terminal of the turn-on switch 36, which may be a p-type device as illustrated in FIG. 9, may be held to the output voltage ( $V_{out}$ ) or to the voltage at a tap on the main power transformer 12, as described below. When the voltage between the terminals exceeds the threshold voltage of the switch 36, the switch 36 turns on to turn on the SR 16.

As shown in FIG. 9, the secondary winding of the transformer 12 may be tapped to provide the appropriate voltage for the charge pump capacitor 302. The number of turns between the tap and the winding end may be chosen to provide a suitable voltage for the gate of the SR 16. Further, as shown in FIG. 9, the gate of the turn-on switch 36 may be connected to the anode of the charge pump diode 302 instead of the output voltage. This may prevent excessive voltage from appearing at the gate of the turn-on switch 36 during the ON period of the primary switch 14. In addition, the circuit may include a resistor 306 in series with the diode 304 to limit the current through the diode 304 into the charge pump capacitor 302.

As shown in FIGS. 5–7, a cross-coupled charge pump arrangement may be used for paralleled converters. Without the cross coupling of the charge pumps, the charge pump voltage may be too low to provide adequate drive to the SRs. By cross-coupling the charge pumps between the two converters, as shown in FIGS. 5 and 7, the output voltage may be added to the charge pump capacitor.

As is apparent from the above-description, embodiments of the drive circuit of the present invention provide the advantage of creating a reservoir of stored energy for turn on of the SR and initiate the turn-on current based on forward bias of the SR 16. Thus, conduction by the body diode of the SR is minimized, thereby reducing losses. Also, turn off the SR may be initiated through a fast pulse transformer at a time determined by the control signal for the primary switch 14, and the secondary winding voltage does not begin to charge until the turn-on delay of the primary switch 14. Therefore, at least turn-on delay of the primary switch 14 may compensate for the turn-off delay of the SRs. In addition to this delay, the leakage inductance of the transformer 12 and transition time of the secondary voltage may create additional small delays that ensure that the SRs are off before the reverse voltage is applied. Further, embodiments of the present invention may provide high performance, reliability and simplicity because they combine discrete drive switches 34, 36 with a reliable charge pump circuit 301 and small pulse transformer.

Although the present invention has been described herein with respect to certain embodiments, those of ordinary skill in the art will recognize that many modifications and variations of the present invention may be implemented. For example, the isolation transformer 12 may include multiple primary, secondary, or tertiary windings. In addition, the power converter circuit 10 may have a mechanism for resetting the core of the transformer 12. The foregoing description and the following claims are intended to cover all such modifications and variations.

What is claimed is:

1. A drive circuit for a synchronous rectifier of a switch mode power converter, wherein the power converter includes a main power transformer and a primary switch for cyclically coupling the main power transformer to an input source, the drive circuit comprising:
  - a charge pump coupled to a secondary winding of the main power transformer;
  - a turn-on switch for turning on the synchronous rectifier, wherein the turn-on switch is coupled to the charge pump;
  - a pulse transformer having primary and secondary windings, wherein the primary winding is responsive to a control signal supplied to the primary switch; and

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a turn-off switch for turning off the synchronous rectifier, wherein the turn-off switch includes a control terminal coupled to the secondary winding of the pulse transformer.

2. The drive circuit of claim 1, wherein the charge pump is for providing drive and a power supply for the turn-on switch.

3. The drive circuit of claim 1, wherein the charge pump includes a capacitor and a diode.

4. The drive circuit of claim 3, wherein:  
the main power transformer includes first and second secondary windings connected in series at a common node; and

the turn-on switch includes a FET having a source terminal, a drain terminal and a gate terminal, wherein the gate terminal is coupled to the common node between the first and second secondary windings of the main power transformer and the drain terminal is coupled to the control terminal of the synchronous rectifier.

5. The drive circuit of claim 4, wherein the diode of the charge pump includes an anode terminal coupled to the common node of between the first and second secondary windings of the main power transformer and a cathode terminal coupled to the source terminal of the turn-on switch.

6. The drive circuit of claim 5, wherein:  
the first secondary winding of the main power transformer includes a first terminal opposite the common node between the first and second secondary windings, wherein the synchronous rectifier is coupled to the first terminal of the first secondary winding; and

the capacitor of the charge pump is coupled between the first terminal of the first secondary winding and the source terminal of the turn-on switch.

7. The drive circuit of claim 6, further comprising a differentiator circuit coupled to the pulse transformer.

8. The drive circuit of claim 7, wherein the differentiator circuit includes:

a capacitor connected to the primary winding of the pulse transformer; and

a resistor connected in parallel with the primary winding of the pulse transformer.

9. The drive circuit of claim 1, further comprising a differentiator circuit coupled to the pulse transformer.

10. The drive circuit of claim 9, wherein the differentiator circuit includes:

a capacitor connected to the primary winding of the pulse transformer; and

a resistor connected in parallel with the primary winding of the pulse transformer.

11. The drive circuit of claim 1, wherein the power converter includes first and second paralleled power converters, each paralleled power converter including a synchronous rectifier, a main power transformer, and a primary switch for cyclically coupling the input voltage to the main power transformer, wherein:

the charge pump for the drive circuit for the first power converter is coupled to the secondary winding of the main power transformer of the second power converter; and

the charge pump for the drive circuit for the second power converter is coupled to the secondary winding of the main power transformer of the first power converter.

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12. The drive circuit of claim 11, wherein the first and second power converters are interleaved.

13. The drive circuit of claim 1, wherein the switch mode power converter is selected from the group consisting of a forward converter, a flyback converter, a half-bridge converter, a full-bridge converter and a push-pull converter.

14. A power converter, comprising:

a main power transformer;

a synchronous rectifier coupled to a secondary winding of the main power transformer for rectifying a voltage across the secondary winding;

a primary switch for cyclically coupling an input voltage to a primary winding of the main power transformer; and

a drive circuit for driving the synchronous rectifier, the drive circuit comprising:

a charge pump coupled to the secondary winding of the main power transformer;

a turn-on switch for turning on the synchronous rectifier, wherein the turn-on switch is coupled to the charge pump;

a pulse transformer having primary and secondary windings, wherein the primary winding is responsive to a control signal supplied to the primary switch; and

a turn-off switch for turning off the synchronous rectifier, wherein the turn-off switch includes a control terminal coupled to the secondary winding of the pulse transformer.

15. The power converter of claim 14, wherein the charge pump is for providing drive and a power supply for the turn-on switch.

16. The power converter of claim 14, wherein the charge pump includes a capacitor and a diode.

17. The power converter of claim 16, wherein:

the main power transformer includes first and second secondary windings connected in series at a common node; and

the turn-on switch includes a FET having a source terminal, a drain terminal and a gate terminal, wherein the gate terminal is coupled to the common node between the first and second secondary windings of the main power transformer and the drain terminal is coupled to the control terminal of the synchronous rectifier.

18. The power converter of claim 17, wherein the diode of the charge pump includes an anode terminal coupled to the common node of between the first and second secondary windings of the main power transformer and a cathode terminal coupled to the source terminal of the turn-on switch.

19. The power converter of claim 18, wherein:

the first secondary winding of the main power transformer includes a first terminal opposite the common node between the first and second secondary windings, wherein the synchronous rectifier is coupled to the first terminal of the first secondary winding; and

the capacitor of the charge pump is coupled between the first terminal of the first secondary winding and the source terminal of the turn-on switch.

20. The power converter of claim 14, further comprising a differentiator circuit coupled to the pulse transformer.

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